THE GRAPHENE FIELD EFFECT TRANSISTOR:

A LARGE SCALE INTEGRATION APPROACH

by

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To my family and my group members for making this possible.

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The University of Texas at Dallas, 2016

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Owing to the continuous down scaling of devices as per Moore's law and the simultaneous need to increase the processing efficiency of the transistor, graphene was found to be the potential candidate for the post silicon electronics due to its predicted theoretical mobility of 200,000 $cm^2/V.$ s and one atom thickness. However, due to its semi metallic nature with no bandgap and a linear electronic dispersion structure, the use of graphene field effect transistors in logic circuits is not feasible as there is no off state and the on to off ratio is lesser than the required criteria of 10^4. Nevertheless, its usability in radio frequency applications is still significant because of the higher cut-off frequency and the predicted ability to saturate the mobility at higher electric fields. Mechanically exfoliated, epitaxially grown graphene has limitations in terms of reproducibility and scalability. CVD graphene is a viable source for fabricating transistors on a large scale. Different processes developed with the objective of making consistent and reliable graphene field effect transistors, packaging them for practical applications are discussed in this thesis.

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CHAPTER 1

INTRODUCTION

1.1 Introduction to this work

The need to continuously downscale the device dimensions of a transistor as per Moore's law [1] with significant improvements in its mobility when compared to Si posed graphene as the prime candidate for post Si CMOS application. It's usage in the field of logic circuits is still questionable due to the absence of an off state attributed primarily to its semi-metallic nature with no absolute bandgap [2]. Hence transistors made using graphene as the channel material cannot turn off, leading to a higher static power consumption. A lower static power consumption is one of the prime advantage in CMOS configuration which cannot be met by graphene field effect transistors [3]. However, graphene can still be used for radio frequency application mainly because of it's potential to get higher cut-off frequencies with simultaneous saturation of drain current [3-5] when compared to Si and other III-V semiconductors available now. Graphene is also sought out for its application in electronic sensing [7].

Mechanical exfoliation of graphene, epitaxial growth of graphene on SiC and chemical reduction of graphitic oxide are not commercially exploitable due to lesser throughput. CVD graphene on the other hand, can be extensively used to fabricate graphene field effect transistors on a large scale using the currently available technology for semiconductor fabrication. Conventional lift-off process used in transistor fabrication has complexities arising at each

processing step especially with a sensitive material like graphene involved in it. Graphene is known to get doped by surface transfer or substitutional doping. For example, graphene is doped n-type by ethanol and ammonia which are the common ingredients of various chemicals used in the device processing [6]. The involvement of photoresists and etchants at various stages of processing also complicates and contributes to doping (n or p type) in graphene which in turn affects the device behavior and performance. The chemical doping of graphene does not have any deleterious effect on the mobility but shifts the Dirac point or the Charge Neutrality Point (CNP) of graphene [6]. Additionally, the presence of photoresist and improper etching of the dielectric in the contact region can lead to a higher contact resistance. So, an optimized process aimed at achieving a higher mobility, lower contact resistance and most importantly fabricating graphene transistors on a large scale with packaging ability for use in commercial applications is the need of the hour and is discussed in this thesis.

1.2 Graphene Field Effect Transistors (GFETs)

A graphene field effect transistor is typically a three or four terminal device. The device can be controlled by a universal back gate, top gate or dual gates as shown in the figure 1.1

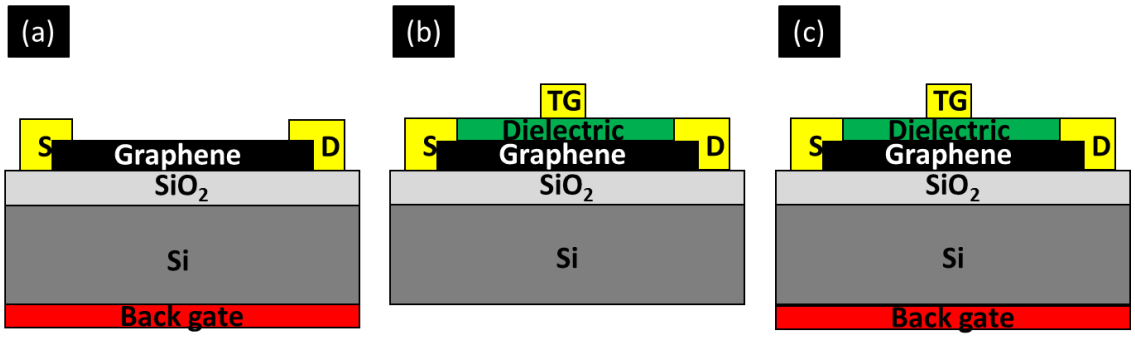

Figure 1.1 A typical structure of Graphene Field Effect Transistor a) with a universal back gate b) with a top gate and c) dual gates.

The carrier concentration in the graphene channel can be modulated by the application of the gate bias. Graphene field effect transistors show ambipolar behavior with hole carrier conduction in the graphene channel region under applied negative bias and electron conduction at any applied positive bias [3]. The two regimes are separated by the Dirac or Charge neutrality point as shown in figure 1.2

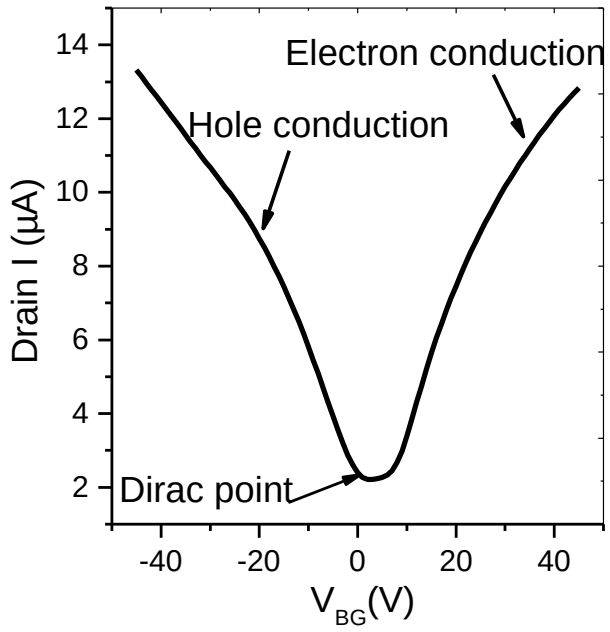

Figure 1.2 Typical ambipolar transfer characteristic of a graphene field effect transistor under an applied back gate bias.

The valence and conduction bands of graphene meet at the charge neutrality point where the density of states and the induced carrier concentration is theoretically zero. However, in experimentally measured graphene there is an intrinsic charge carrier concentration even at the charge neutrality point. This has been attributed to puddles, charge impurities originating from the underlying rough SiO_2 and rippling of graphene [45]. The ambipolar behavior of graphene has

been taken advantage of in the establishment of ambipolar electronic circuits like high performance frequency doublers, radio frequency mixers, digital moderators and phase detectors [8-9].

1.3 Previous Graphene FET studies in UTD

1.3.1 Earlier GFET studies

Most of the previous studies in the fabrication of GFETs at UTD were mainly dedicated to developing of processes to deposit high-k dielectric using ozone [10], examining the effect of contacts, graphene type and substrate on its transport properties [11] and functionalization of graphene by covalent and non-covalent methods for enabling the growth of high quality dielectric on top of graphene [12]. Most of the studies on the development of high-k dielectric and functionalization of graphene utilized mechanically exfoliated graphene. The ozone based high-k dielectric deposition process demonstrated a high quality and conformal dielectric deposition with top gated mobility values in the range of 3000~5000 $cm^2/V.$ s [10] The contact resistivity was determined to be independent of the applied back gate voltage and the number of layers in a mechanically exfoliated graphene stack [11]. The reduction of contact resistance in Ni-Au contacts was realized using a thinner PMMA for transfer and Ti based interface cleaning procedure [11] A higher sheet resistance was identified in CVD graphene when compared to exfoliated flakes and the dependence of mobility on device dimensions were identified using both exfoliated and CVD graphene [11,13]. For a given channel length, the initial increase in the mobility and the subsequent decrease with its channel width was attributed to edge scattering and electrostatically induced accumulation of charges at the edges [13] in case of exfoliated graphene. An analogous trend was observed in the case of CVD grown graphene but with a lower mobility when compared to its

exfoliated counterpart with comparable channel lengths and widths [13]. This decrease in mobility is associated with domain boundaries, wrinkles and residues from the transfer process [11,13]. It should be noted that all the extracted mobility values and observation of particular trends are based on the back gate modulation of the graphene FETs as stated in references 12 and 34. The applicability of using ozone at room temperature to functionalize the surface of graphene as the possible method for seeding dielectrics on CVD grown graphene was evaluated [12], the importance of having a high-quality defect free graphene in order to avoid any damages caused by O_3 were realized [12]. The changes in the properties of GFETs like mobility, Dirac voltage shift were identified by the development of *in-situ* electrical characterization using back gated GFETs where the interaction of the graphene with different ALD precursors were studied [12]. Development of Low-k dielectrics for BiSFETs were also studied [12]. Even though few of the studies did not call for the fabrication of the transistor, all these references provide a proper guideline and back bone for the development of processes aimed at the fabrication of GFETs on a larger scale.

1.3.2 Earlier GFET fabrication techniques

Most of the earlier works were mostly confined to GFETs fabricated using mechanically exfoliated graphene. In this technique, graphene is mechanically exfoliated from a bulk graphite using the scotch tape method [16] and characterized using optical microscope and Raman spectroscopy. The graphene obtained by this technique is of good quality but not commercially scalable. The mechanically exfoliated flakes are then spin coated with polymethylmethacrylate-PMMA and baked at 180°C for 2 minutes [12]. The source/drain contact regions are defined using the e-beam lithography and the contact metal of desired thickness is deposited using e-beam

evaporator. The dielectric is then deposited on top of the device followed by similar steps for top gate patterning and metal deposition. The details of the device fabrication are as stated in reference 12.

Epitaxially grown graphene on SiC have also been used to fabricate transistors but controlling the number of layers of graphene during the growth, its uniformity and the phase on which they are grown (Si face or C face) determined the properties of graphene [46]. The performance of the transistors is not reproducible owing to a lot of variables involved in determining the end performance. The outline for transistor fabrication using photolithography with epitaxial graphene is as described in reference 47. The device fabrication is similar to the one used in this work apart from the occasional surface treatments done to the substrate. Scalable fabrication of graphene devices using photolithography with field effect mobility of ~ 2500 cm^2/V.s was demonstrated [48] . CVD graphene combined with the ability to fabricate devices using photolithography makes it a promising candidate for transistor fabrication.

1.4 Motivation and outline

All of the previous studies were focused on the development of processes to integrate graphene in the fabrication of field effect transistors with extra attention on the scaling as well as the deposition of high-k dielectrics on top of the graphene surface. Few studies were also performed to evaluate the effect of contacts, inherent graphene quality and substrates on the transport properties of graphene. Most of the experiments performed earlier involved the usage of mechanically exfoliated graphene which is not commercially scalable and hence fabrication of GFETs using large area CVD grown graphene as a viable source using exploitable state of the art semiconductor processing technology is required. This is the main motivation of this work and this

dissertation evaluates processes for fabricating GFETs using conventional lift-off method on a large scale with a special focus on its ability to be packaged for commercial use.

Chapter 2 describes the sources of graphene used for this study, the mask set used for the fabrication of the transistors and the basic process flow used for the fabrication of the transistor along with the material as well as the electrical characterization used. The basic CVD graphene transfer process along with the preliminary work done on capping the CVD graphene before transferring to the substrate is also discussed in this chapter. Chapter 3 provides an insight on the electrical behavior of different sets of devices starting from the basic process followed by the effect of UHV annealing, Ti based graphene surface cleaning, seeding layer, different oxygen source for the dielectric formation and dielectric first GFET process. Chapter 4 deals with the contact resistance issue with a focus on the effect of plasma cleaning on the contact resistance and Dirac point shifts observed in the GFETs along with its optimization and different metal contact used for fabricating the transistor. Chapter 5 summarizes the overall results of this study and the future direction required in terms of ameliorating the device behavior and performance for its practical applicability.

CHAPTER 2

FABRICATION OF GRAPHENE FIELD EFFECT TRANSISTORS

This chapter describes the sources of graphene used, the details of the GFET masks used for the photolithography and the fabrication techniques used in this work.

2.1 Sources of Graphene

The graphene used for the fabrication of transistors are from an amalgamation of different sources. Some were purchased from Graphene Platform (Japanese vendor) where the 2"X2" CVD graphene is transferred on top of heavily doped n- type Si wafer with 100nm thermal oxide (resistivity < 50Ω-cm) and some were purchased from Graphenea (Europe based vendor), others are CVD grown graphene on Cu foil from Graphene supermarket, Graphene platform and UT Austin transferred onto heavily doped n-type Si wafer with 300nm/90nm thermal oxide grown at UTD. In terms of purchased graphene, the Graphene platform based GFETs provided a higher mobility when compared to the Graphenea samples. Hence, most of the later studies were done using the Graphene platform samples. The source of graphene is mentioned in each device fabrication process flow as well as in the discussion of electrical results to provide an understanding of the properties which might vary based on the inherent quality of the graphene used.

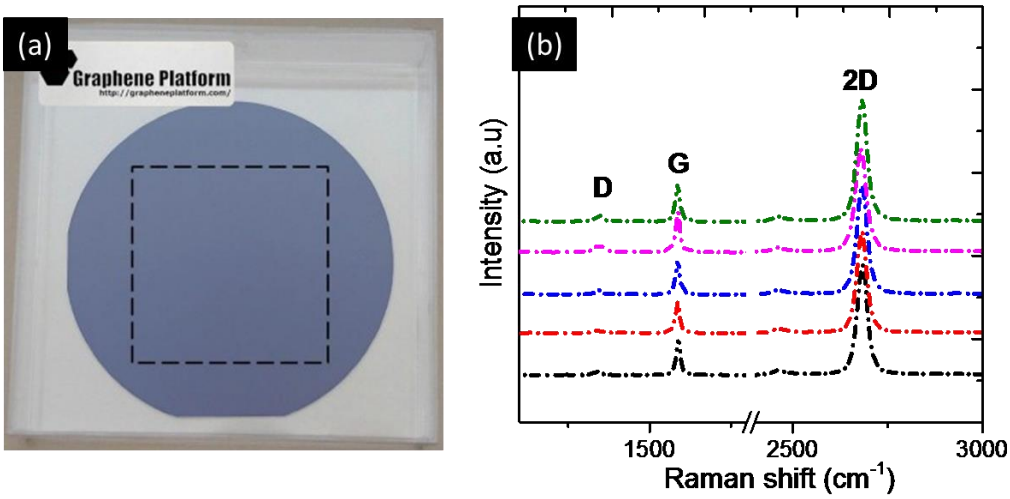

Figure 2.1 a) Purchased Graphene platform wafer where 2"x2" CVD graphene is transferred on top of 100nm SiO_2 on n-type doped Si wafer b) Raman spectra at 5 different spots on the 2"x2" CVD graphene area.

2.2 Mask set and structure details

The current mask set contains 3 GFETs with top gate under each Gate Length (GL) and Gate Width (GW) hereon denoted as GLxGW with varying sets of dimension (3µmx3µm,3µmx5µm etc.) as mentioned in the table below:

Table 2.1 Gate length and gate widths of the GFETs.

Table 2.1 GFET gate dimension	
Gate Length (µm)	**Gate width (µm)**
3	3
5	5
10	10
30	-

A similar number of back gated GFETs are also available in this mask set. The source and drain pad pitch has an additional 8µm apart from the gate length dimension.

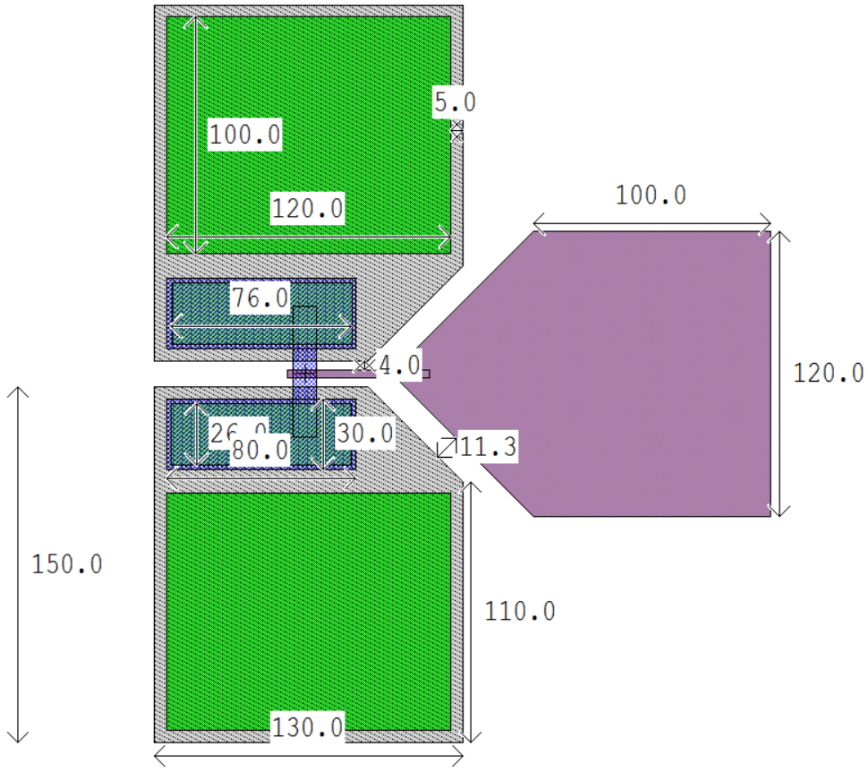

Figure 2.2: A typical GFET structure using the mask design for a top gated transistor. The green region represents the final contact opened area available for wire bonding.

Special structures like Cross- Bridge Kelvin Resistor (CBKR) for the measurement of low contact resistance [14], Greek Cross structures for measuring sheet resistance [17] Transmission Line Measurement (TLM) structures for measuring specific contact resistance [18,19] and contact area GFETs with varying graphene-metal contact area is also present in this mask set. The device dimensions for each structure is presented in the table below

Table 2.2 X and Y dimensions of the CBKR and Greek cross structure.

X(μm)	Y(μm)
10	10
20	20
30	30
40	40
50	50

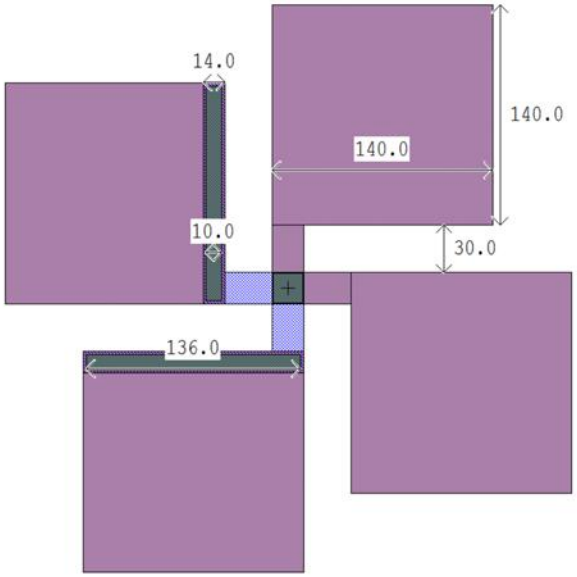

Figure 2.3 A typical CBKR structure

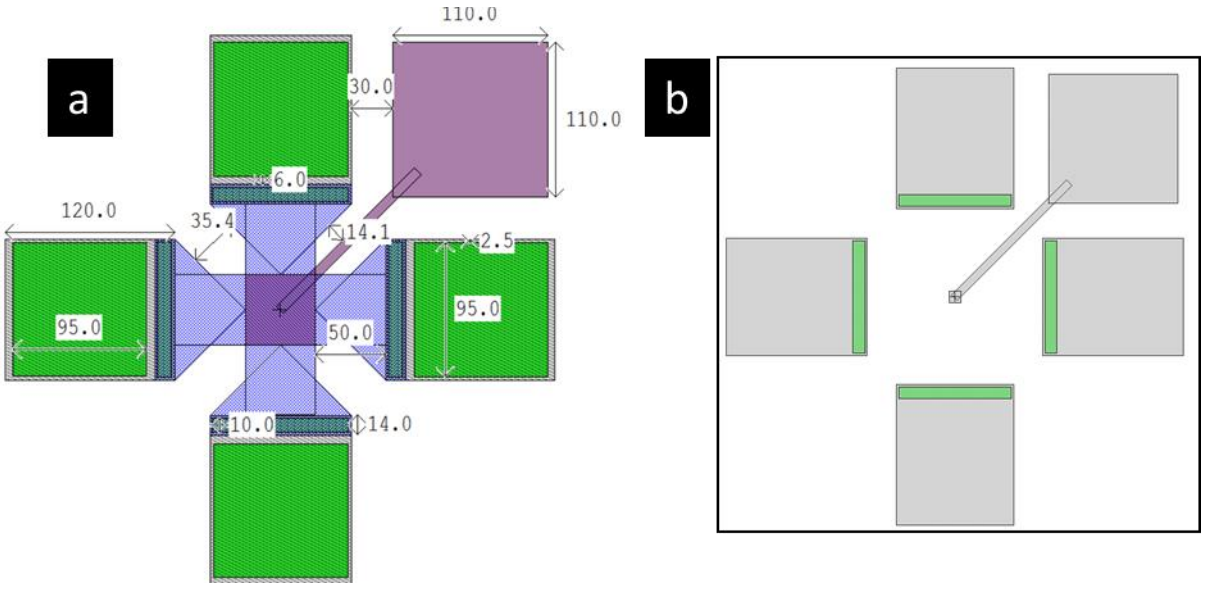

Figure 2.4 a) A typical Greek cross structure and b) Greek cross structure without the graphene channel area

Table 2.3 Gate width, gate length and distance (d) between the TLM structures

TLM structure dimension		
Gate Width (µm)	**Gate Length (µm)**	**d (µm)**
3	3	2
5	10	5
10		10
30		20

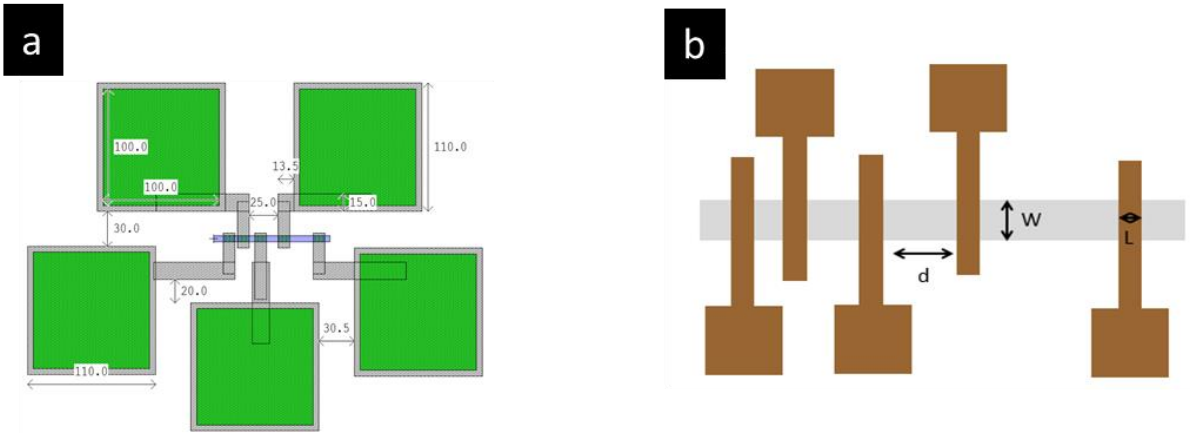

Figure 2.5 a) A typical TLM structure and b) Schematic of the design parameters used in the TLM structure

2.3 Characterization Techniques

2.3.1 Material Characterization Techniques

In this work, optical microscopy and Raman spectroscopy were extensively used to characterize the quality of graphene used. Atomic force microscopy (AFM) and X-ray photoelectron spectroscopy (XPS) were the other techniques used to investigate the surface morphology and surface analysis respectively. Graphene has a transmittance of ~ 97% under visible wavelength [20] and shows a good contrast with respect to the substrate (90nm/300nm of

SiO_2) which can be identified using an optical microscope [21]. Optical microscopy also helps in the identification of a lot of bilayer graphene features present in the CVD graphene as shown in figure 2.6 (a).

Raman spectroscopy has a signature spectrum to identify single layer, bilayer and thicker graphene layers. The three major characteristic Raman peaks are G, D and 2D peaks. The G peak corresponds to the first order Raman scattering and 2D as well as D peaks correspond to the second order Raman scattering. It is pivotal to note that the D peak is seen only in the presence of the defects in graphene thereby denoting its quality. The D, G and 2D peaks are approximately located at 1350cm^{-1}, 1580cm^{-1} and 2700 cm^{-1} respectively and their position is a function of the energy of the laser used [22].

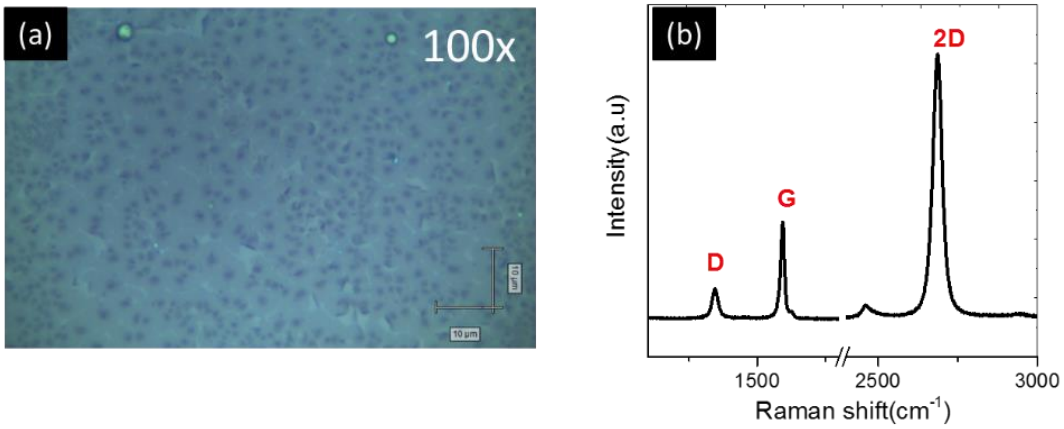

Figure 2.6 a) Optical microscope image of CVD graphene with a lot of bilayer features and b) Characteristic Raman spectra of a single layer CVD graphene on SiO_2/Si substrate.

2.3.2 Electrical Characterization

Electrical characterization of the graphene FETs is important in order as it directly evaluates the final output of the device fabrication process. The drain current (I_{DS}) in the graphene channel

is measured as a function of the applied gate bias (V_G) (top gate/ back gate) under a small applied drain voltage (V_{DS}). Mobility is the most commonly reported parameter to estimate the graphene quality and also to evaluate the device fabrication process. Drude model and Constant mobility model are the mostly frequently used methods to calculate the mobility. In the Drude model, the mobility is a function of the carrier concentration and can be extracted using the following equation

$$R_{Total} = \frac{(L / w)}{|n_{ind}| \cdot e \cdot \mu_{Drude}}$$

Where L and W correspond to the length as well as the width of the graphene channel in the transistor, e is the charge of the electron, μ_{Drude} is the extracted Drude mobility,$|n_{ind}| = C_{\frac{g \cdot |Vg - V_{Dirac}|}{e}}$ is the induced charge carrier density and C_g is the gate capacitance which comprises of a series combination of the oxide capacitance (C_{ox}) and quantum capacitance of the graphene channel (C_q). C_{ox} is a constant function of the applied gate bias V_G and C_q is a function of the density of states in graphene. C_q is considered into account in case of thin high-k dielectrics and can be neglected for thicker dielectrics (low C_{ox}).

Kim *et.al* proposed the constant mobility model [34] which is used to extract the mobility and is independent of the carrier concentration. The constant mobility model is given by

$R_{Total} = R_{Contact} + R_{Channel} = 2R_{S/D} + \frac{(L/W)}{\left(\sqrt{n_o^2 + n_{ind}^2}\right) \cdot e \cdot \mu_{Constant}}$ where R_C is the contact resistance, $R_{Channel}$ is the resistance of the graphene channel, n_O is the intrinsic or residual carrier concentration and $\mu_{Constant}$ is the constant mobility. The mobility values are extracted by fitting the experimental R_{Total}-V_G curves with the constant mobility model by varying R_C,n_o and $\mu_{Constant}$. The

constant mobility model was extensively used in this work to calculate the mobility ($\mu_{Constant}$), $R_{C,}n_O$ and the Dirac point of the measured graphene FETs.

Keithley 4200A-SCS parameter analyzer was used to measure the fabricated graphene FETs. The backgate modulation was from -45 to +45V with a 0.5V step for a 100nm/90nm SiO_2 substrate with a V_{DS} of 0.1V.

2.4 CVD graphene transfer

Be it the purchased graphene or the CVD graphene transferred here at UTD, transferring of the CVD graphene to the target substrate is one of the pivotal steps and plays a major role in determining the quality of the fabricated field effect transistors. Though a lot of improvements are being made in the transfer process, alternative polymer scaffolds other than the commonly used PMMA transfer [41,42] and scaffold free graphene transfer [43,44] are currently being analyzed. However, the essence of the large area CVD graphene transfer using the PMMA scaffold is essentially the same as illustrated in figure 2.7

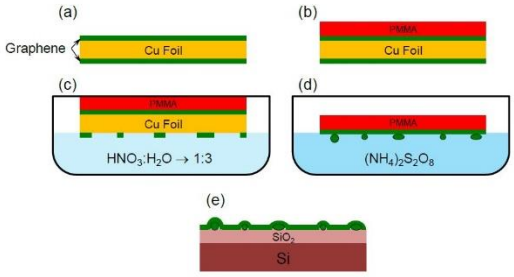

Figure 2.7 Schematics of the major steps involved in the standard graphene transfer process. (a) Graphene grown on both sides of the Cu foil. (b) PMMA scaffold layer spin coated on top of the Cu foil. (c) Backside etching of graphene in dilute Nitric acid leaves smaller strips of graphene. (d) Graphene scrolls tethered to the graphene during etching of Copper foil in ammonium persulfate ($(NH_4)_2S_2O_8$). (e) Graphene scrolls are attached between the graphene and the target substrate after the completion of transfer process followed by PMMA removal. [Schematic is from reference 12]

2.4.1 Encapsulation of CVD graphene before transfer

Encapsulation of the CVD graphene using a metal oxide before transferring it to the target substrate could be one way of protecting the intrinsic properties of as grown graphene. The encapsulation layer acts as a barrier between the graphene surface and the polymer scaffold used for the transfer process. It could also prevent the photoresists to come in direct contact with the graphene surface and avoid any unintentional doping of graphene. The schematic for this process is shown below

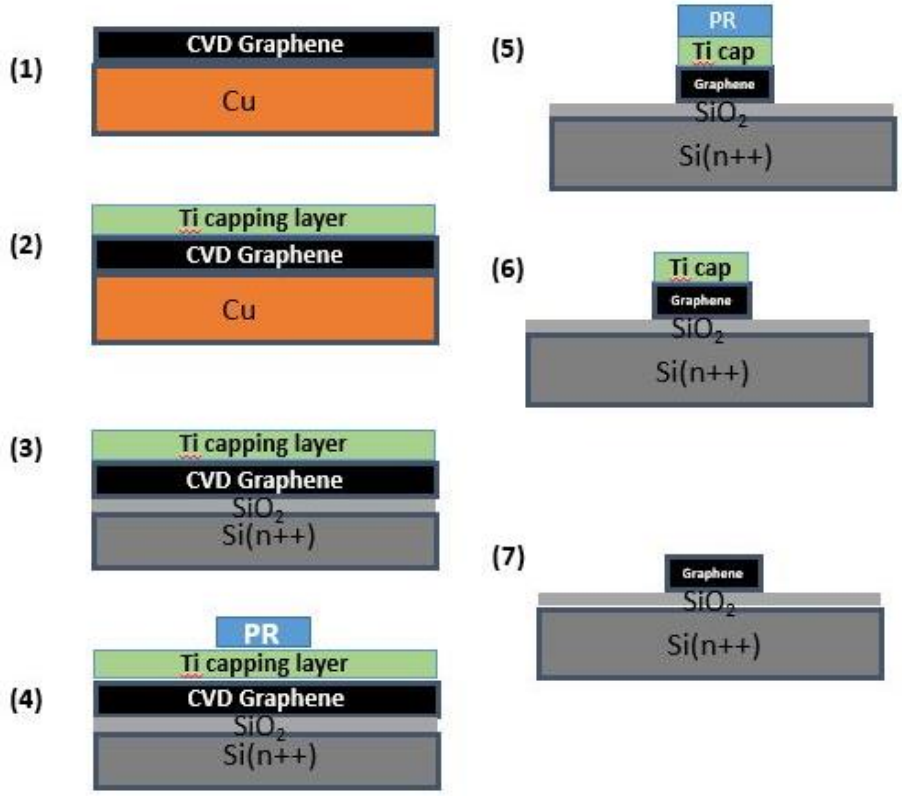

Figure 2.8 Schematic of encapsulation of CVD graphene before transferring to the target substrate. (1) CVD graphene on Cu foil (2) Encapsulation of the graphene surface using Ti layer by e-beam deposition (3) Transfer of the encapsulated graphene on SiO_2/Si. (4) Graphene channel patterning. (5) Etching of Ti capping layer and graphene from other areas. (6) Removal of the channel pattern photoresist and (7) Removal of the Ti encapsulation layer.

CVD graphene on Cu foil purchased from Graphene platform and CVD graphene on Cu foil obtained from UT Austin were capped with 0.5nm Ti using the cryo e-beam evaporator. The optical images at 100x after the transfer onto the SiO_2/Si substrate using the previously described conventional transfer technique using PMMA scaffold is shown below

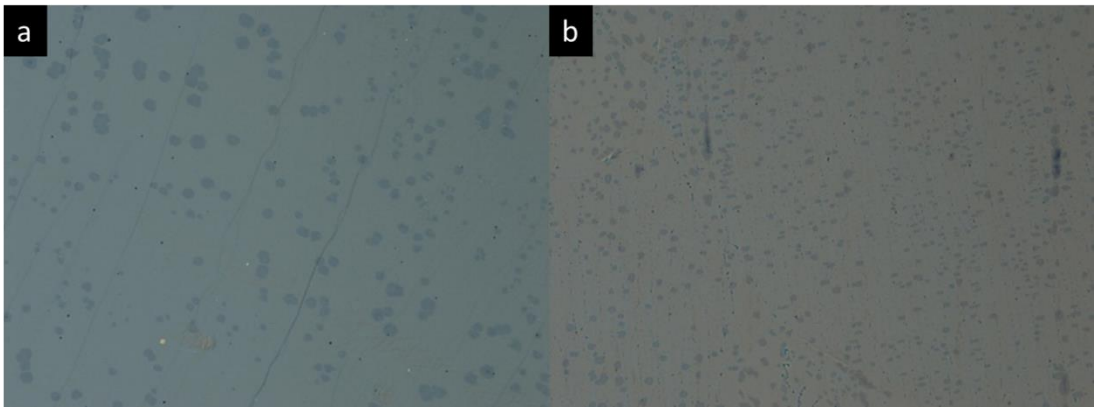

Figure 2.9 a) 0.5nm Ti encapsulated Graphene Platform CVD graphene after transfer on 90nm SiO_2/Si at 100x magnification b)0.5nm Ti encapsulated UT Austin CVD graphene after transfer on 90nm SiO_2/Si at 100x magnification.

After step 5 shown in the schematic, where the graphene channel area is defined followed by etching the Ti capping layer using 100:1 HF, most of the graphene surface got lifted off from the substrate (Figure 2.18). In spite of this, further steps as described in the schematic were carried out due to the protection of the region of interest (graphene channel) by the photoresist. After etching the Ti capping layer from the graphene channel area using 100:1 HF for ~12s (etching time determined by the standard H-terminated Si sample with the Ti capping layer deposited under the same conditions as graphene), almost all the graphene channel got lifted off from the substrate. This kind of behavior could be attributed to the following reasons:

a. The CVD graphene on Cu foil was not perfectly flat during the Ti deposition using the cryo e-beam evaporator resulting in a non-uniform coverage of the capping layer on top of

graphene. This might result in the possible seeping in of 100:1 HF in areas with lower Ti coverage and lifting out the sample by attacking the underlying SiO_2 layer.

b. There is an inherent degradation in the quality of the CVD graphene transferred on to the target substrate using the polymer scaffold and affects the interface of the CVD graphene and underlying substrate.

c. Insufficient thickness of the encapsulation layer for a conformal deposition over the CVD graphene surface.

These shortcomings can be overcome by making sure that the CVD graphene on Cu foil is as flat as possible during the encapsulation layer deposition, increasing the thickness of the encapsulation layer for more conformal deposition and careful optimization of the CVD graphene transfer process with special attention on improving the adhesion of the encapsulated CVD graphene on top of the SiO_2 layer. Apart from Ti as the encapsulation material, metals like Al, Cr could also be tried as a potential capping layer.

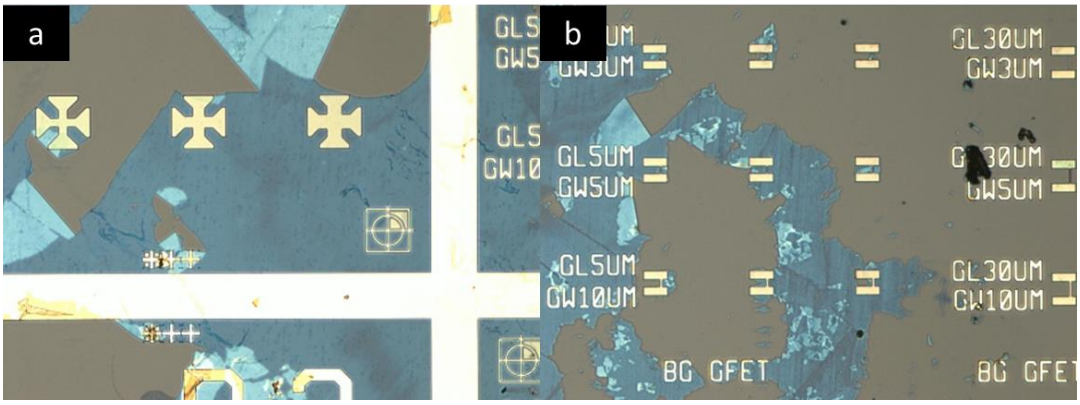

Figure 2.10 Lifting off of the graphene after etching the Ti capping layer using 100:1 HF for approximately 12s a) in Graphene platform and b) in UT Austin samples at 100x.

2.5 GFETs fabrication from CVD graphene using the basic process

The conventional lift off method for the fabrication of graphene field effect transistor using the transferred CVD graphene was done to set up the initial base line for the process and to determine the behavior of the transistors. Initial graphene transferred onto SiO_2 had some issues like cracking, folding of graphene and wrinkles of graphene due to improper etching of the graphene on the backside of the Cu foil as shown in the figure below (a,b and c). Figure d corresponds to the purchased graphene sample where the CVD graphene was already transferred onto the SiO_2/Si substrate. The etching time and transfer process was later optimized to yield good quality transferred CVD graphene here at UTD.

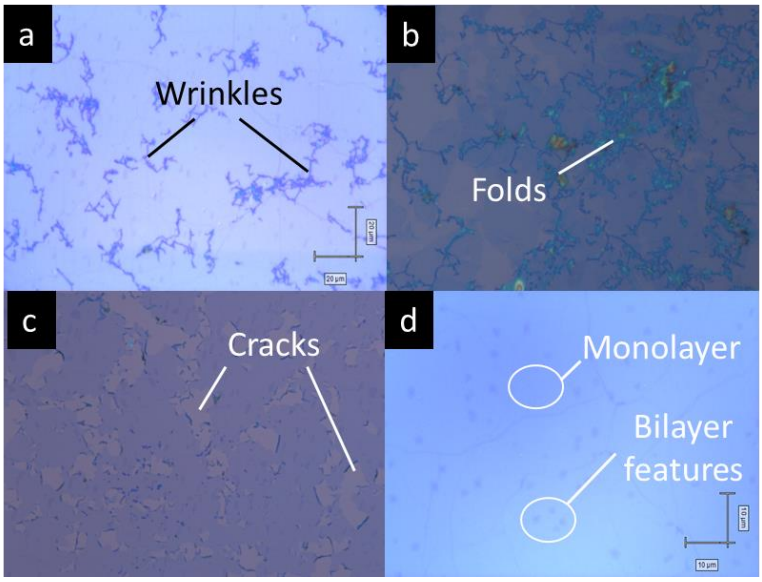

Figure 2.11 a,b and c correspond to the optical images of CVD graphene transferred on top of SiO_2/Si in UTD and d corresponds to the optical image of purchased CVD graphene transferred on top of SiO_2/Si.

The first set of mask was used to make alignment markers on the substrate which would enable the alignment of different levels of masks for the successive fabrication steps. This was followed by defining the graphene channel area and etching away the rest to avoid any conductive

path other than the channel area. Source/Drain (20nm Ni/200nm Au) contacts were made to the graphene channel region using the cryo e-beam evaporator followed by which the channel is encapsulated by ~20nm thick Al_2O_3. The backside of the substrate was cleaned using BOE 7:1 for ~ 2 minutes to etch away the oxide present in that area followed by which 300nm thick Al backgate is deposited using the cryo e-beam evaporator. The devices were measured using the Keithley 4200 Semiconductor Characterization System (SCS) for back gate modulated measurements. The top gate is then formed followed by subsequent electrical measurements to evaluate the device behavior with the dual gates. The backgate is deposited earlier than the one described in the process flow in order to have a prior knowledge on the device characteristics before top gate definition and deposition. The basic GFET fabrication process flow is as shown in fig 2.12

The step by step details of the device fabrication is as described below:

(1) Substrate preparation

(a)For the substrate, heavily doped (n^{++}) Si wafer with 90nm/100nm thermal silicon oxide was used. First level of processing involves the patterning and definition of alignment markers

(b)Spin coat the substrate with graphene with positive photoresist nLOF2020 at 3000rpm with an acceleration of 2000rpm for 60s followed by baking it at 115°C for 1 minute to yield a resist thickness of 1.5~2µm.

(c) Expose the photoresist to the UV light using Karl Suss MA6B contact printer with the appropriate mask placed in the correct position. The dosage for this thickness is ~65mJ/cm^2 and the time duration of exposure is calculated each time based on the intensity of the I-line

in the Hg lamp. Bake the sample at 115°C post exposure. Develop the pattern using AZ300 for 90 seconds followed by rinsing it in DI water and blow dry using N_2 gun.

(d) Ashing with O_2 plasma (50W, 10 sccm of O_2 flow, ~180mTorr, 120s) using March Asher to remove photoresist residue in the defined region in case of substrates before CVD graphene transfer and to etch the graphene in the defined region in case of substrates with the CVD graphene already transferred on top of SiO_2/Si.

(e)Deposit a metal stack of Ni(20nm)/ Au(100nm) using the cryo e-beam evaporator.

(d) Lift off in acetone at room temperature for 5-10 minutes followed by IPA rinse and blow dry it using N_2 gun.

(2) Channel definition

(a) Spin coat the substrate with graphene with positive photoresist S1813 at 3000rpm with an acceleration of 2000rpm for 60s followed by baking it at 115°C for 1 minute to yield a resist thickness of 1.5~2µm.

(b)Expose the photoresist to the UV light using Karl Suss MA6B contact printer with appropriate mask placed in the correct position. The dosage for this thickness is ~130mJ/cm2 and the time duration of exposure is calculated each time based on the intensity of the G-line in the Hg lamp. Develop the pattern using MF 319 for 1 minute followed by rinsing it in DI water and blow dry using N2 gun.

(c)Follow step described in 1(d) which removes the graphene in all regions except the channel area covered by the photoresist

(d) Strip the photoresist by following step 1 (d)

(3) Source/Drain contacts

(i) Follow steps outlined in 1(b-c) and deposit a metal stack of Ni(20nm)/Au(200nm) using the cryo e-beam evaporator.

(4) Top gate dielectric deposition

(i) Set the Cambridge Nanotech (CNT) Inc. Savannah 200 ALD at 200°C

(ii) After the temperature is stabilized, pre-coat the chamber with Al_2O_3 using 50 cycles (0.1s-10s-0.1s-10s) or more of TMA/H_2O.

(iii) Load the sample in the ALD chamber along with a H-terminated Si for monitoring the thickness.

(iv) Start the dielectric deposition using 200 cycles (0.15s-30s-0.1s-30s) TMA/H_2O for a thickness of ~ 20nm with a growth rate per cycle (GPC) of 0.1nm/cycle.

(5) Back gate contact

(i) Etch the oxide present in the backside of the substrate using Buffer oxide etch (BOE) 7:1 for approximately 1 minute.

(ii) Rinse it in DI water and blow dry it with N_2 gun

(iii) Make some scratches for promoting adhesion of back gate metal

(iv) Deposit 300nm Al using cryo e-beam evaporator.

(6) Top gate contact

(i) Follow steps outlined in 1(b-c) and deposit a metal stack of Ni(20nm)/Au(200nm) using the cryo e-beam evaporator.

(ii) Follow steps outlined in 1 (d)

(7) Contact opening for wire bonding

(i) Follow steps described in 2 (a-b)

(ii) Etch the defined region using HF 100:1 for ~120s. Time duration is determined testing the etch rate on H-terminated Si loaded during the dielectric deposition.

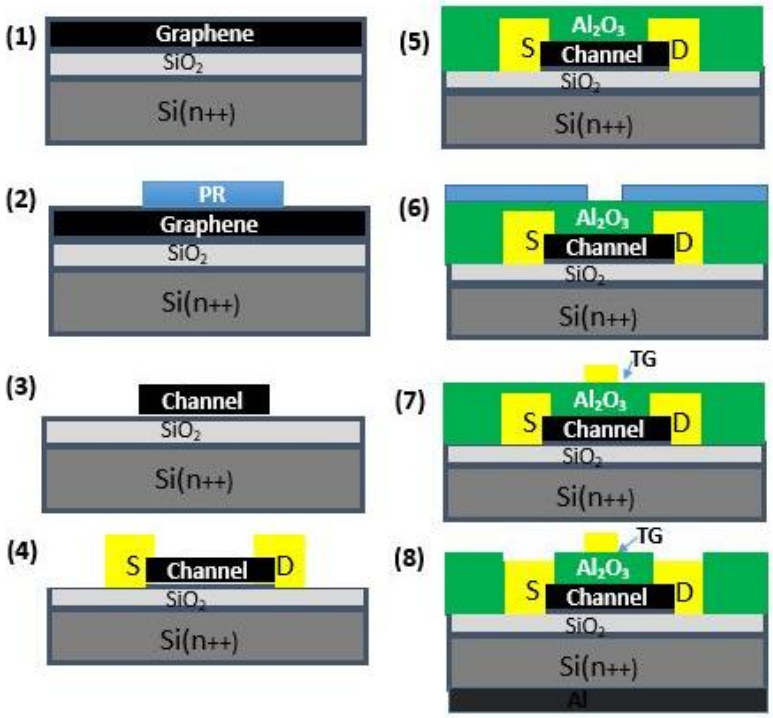

Figure 2.12 Schematic of the important GFET fabrication process steps. (1) As received CVD graphene on SiO_2. (2) Definition of channel area. (3) Etching of graphene from other areas and removal of the photoresist. (4) Source and drain definition followed by Ni/Au (20nm/200nm) deposition using cryo e-beam evaporator and lift off. (5) Dielectric deposition using ALD.(6) Top gate definition. (7) Top gate contact, Ni/Au (20nm/200nm) deposition using cryo e-beam evaporator. (8) 300nm Al backgate deposition using the e-beam evaporator and dielectric contact opening to facilitate wire bonding

2.6 Dielectric first GFET fabrication process

All the previous GFET fabrication processes involved the formation of source/ drain contacts after defining the channel. This was followed by the dielectric deposition as shown in the

schematic 2.9 The top gate was patterned on top of the dielectric after which the top gate metal was deposited. In this process flow, the source/drain contact metal (Ni/Au) was on top of graphene and a larger part of thermally grown SiO_2 under graphene. The source/drain region got peeled off when during the wire bonding process as shown in the figure 2.13. However, the top gates were wire bondable and it lies on top of Al_2O_3.So, the peeling off of source/drain contacts can be attributed to the poor adhesion of Ni with the underlying SiO_2. This called for an alternative process flow where the dielectric was deposited first after the channel definition followed by which the dielectric was etched only in the graphene/metal contact region. In this scenario, a larger part of the contact metal is on top of Al_2O_3 which in turn would facilitate the wire bonding capability of the fabricated GFETs.

The source-drain and top gate contacts can be defined as well as deposited in two separate steps or in a single step as shown in the schematic (figure 2.14) below

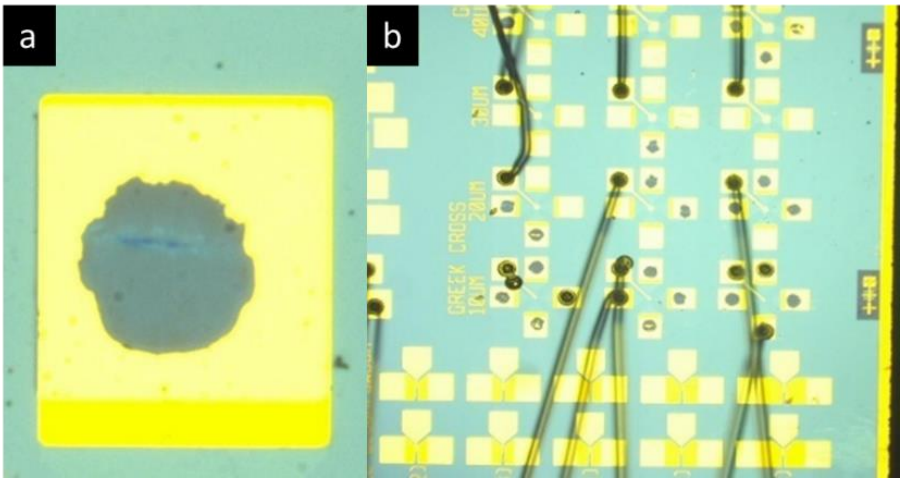

Figure 2.13 a) Peeling off of the source/drain pad in the earlier processes b) Low magnification image of all the wire bonded devices [Image Courtesy- Texas Instruments Inc.]

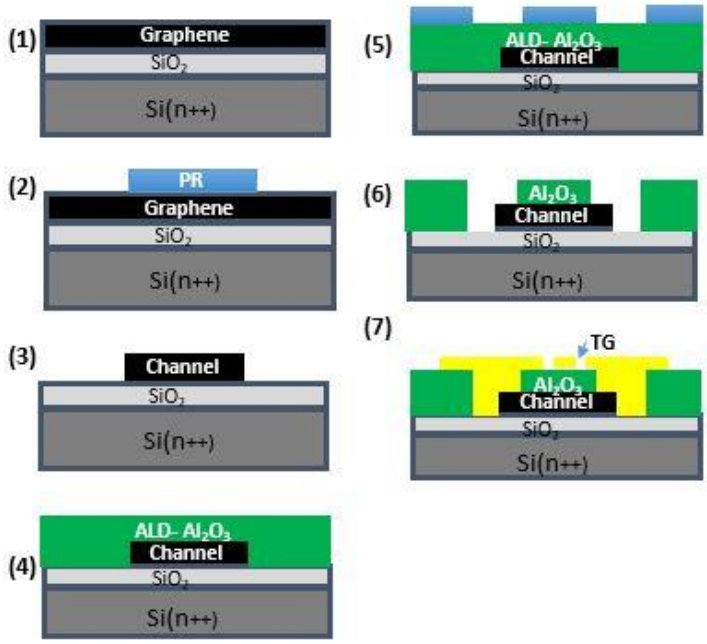

Figure 2.14 Schematic of the dielectric first GFET fabrication process. (1) As received CVD graphene on SiO_2. (2) Definition of channel area. (3) Etching of graphene from other areas and removal of the photoresist. (4) Deposition of ~20nm Al_2O_3 using ALD. (5) Dielectric etch in the graphene/metal contact region definition. (6) Etching of Al_2O_3 in the pre-defined area using 100:1 HF. (7) Source/Drain and Top gate contact, Ni/Au (20nm/200nm) deposition using cryo e-beam evaporator

CHAPTER 3

INTERFACE AND DIELECTRIC OPTIMIZATION

3.1 GFETs using the basic fabrication technique

The electrical results of the graphene FETs fabricated using the basic outline for the transistor fabrication as shown in section 2.2.4 is discussed here. Purchased Graphene Platform samples were used for this study. The back gate modulated mobility values of these devices were in the range of 1500 to 2300 $cm^2/V.s$ based on the constant mobility model fit. After the top gate formation, the top gate modulated mobility values show a higher carrier concentration ($10^{12}/cm^2$) and a degradation in the device performance.

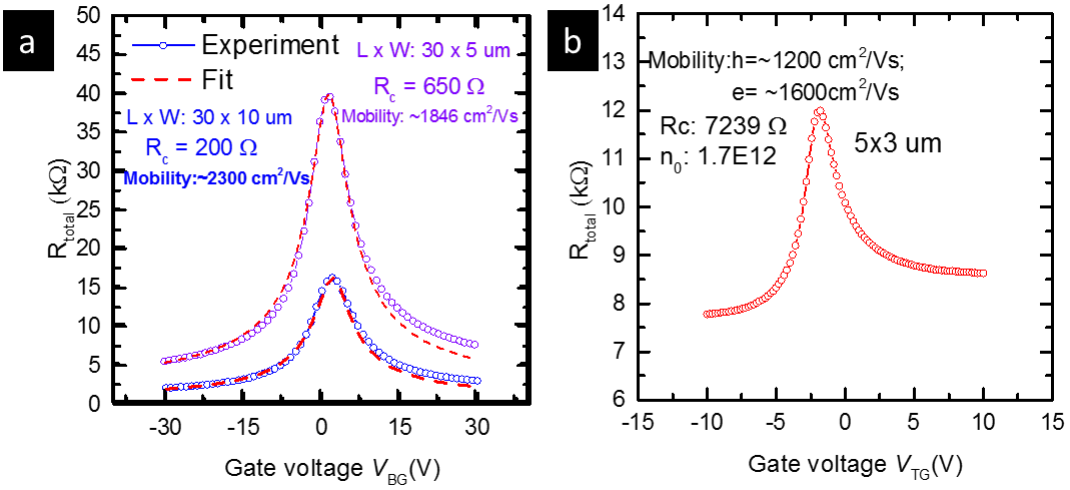

Figure 3.1 Shows the constant mobility model fit with the experimentally obtained data for back gate modulated device (30x5µm and 30x10µm device) in R_{Total} Vs V_{BG} plot b) top gate modulated mobility in a 5x3µm device

3.2 Effect of pre-annealing graphene to reduce polymer residues

Poly(Methyl Methacrylate) (PMMA) is the commonly used polymer as a supporting scaffold during the transfer of CVD grown graphene onto the desired target substrate[23-26]. It is not completely removed after the transfer process even after treating it with acetone for longer duration of time. This can leave a higher amount of residue on the graphene surface and can in turn act as point scatterer as well as can cause unintentional p-type doping of the graphene [27]. Vacuum annealing of graphene is reported to be one of the effective methods in reducing the polymer residue [27] and this step was incorporated in as the first step in current process flow. Irrespective of the source of graphene (Transferred CVD graphene here at UTD or Purchased CVD graphene transferred on top of SiO_2), this step was inculcated to reduce the PMMA residue. Initial annealing was done in the Savannah Nanotech Cambridge ALD and based on the AFM scans performed, the PMMA residue seems to have been reduced slightly after annealing the sample at 250°C for 2h as seen from the 10x10µm AFM scans performed on top of the graphene using DM01 Veeco Dimension 5000 AFM

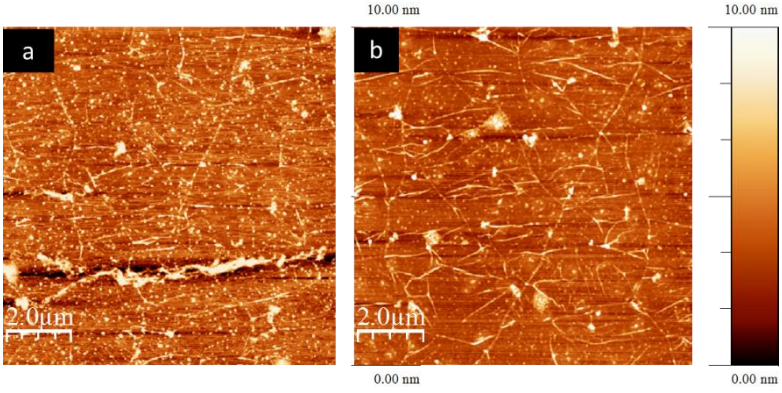

Figure 3.2 a) 10x10µm AFM scans on the surface of CVD graphene with PMMA residue after transfer with a RMS roughness of 1.64nm b) The slight reduction in PMMA residue after annealing at 250°C for 2h in the Cambridge ALD with a RMS roughness of 1.60nm

Since the effectiveness of the annealing in reducing the PMMA residues might increase under high vacuum, a dedicated homemade tool for graphene annealing was setup by Dr.Lucero. This chamber is connected to a turbo pump to reach higher vacuum (typically medium to lower 10^{-8} torr after pumping overnight) and has a 2'x2' AlN heater is connected to a variable thermostat to control the heater temperature. As a good quality of vacuum is reached, the annealing temperature has been increased to 300°C as graphene is prone to damage under the presence of oxygen at temperatures greater than 250°C [28]. Graphene samples annealed using the homemade tool at 300°C for 2h show no increase in the D peak denoting no damage caused to the graphene layer during the process. AFM scans of graphene annealed in the home built chamber (Figure 2.10) show a significant reduction in the PMMA residue when compared to the annealing done using Cambridge ALD.

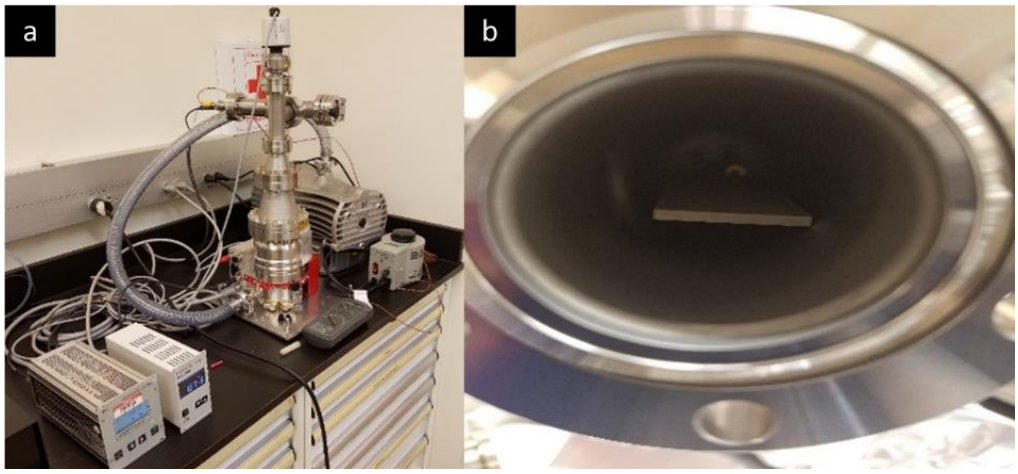

Figure 3.3 a) Dedicated homemade annealing chamber for UHV annealing of graphene and b) The view of the annealing chamber with the AlN heater inside.

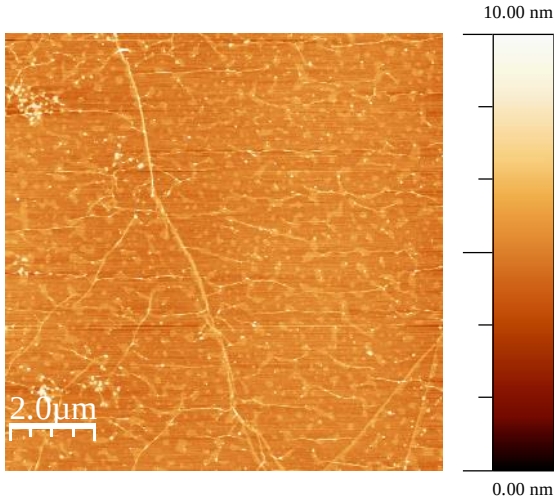

Figure 3.4 10x10µm AFM scan on top of the CVD graphene annealed at UHV for 300°C for 2 hours having an RMS roughness of 0.68nm

The XPS results shown below provides information on the reduction in polymer residue after the UHV annealing both in the purchased graphene as well as the transferred graphene.

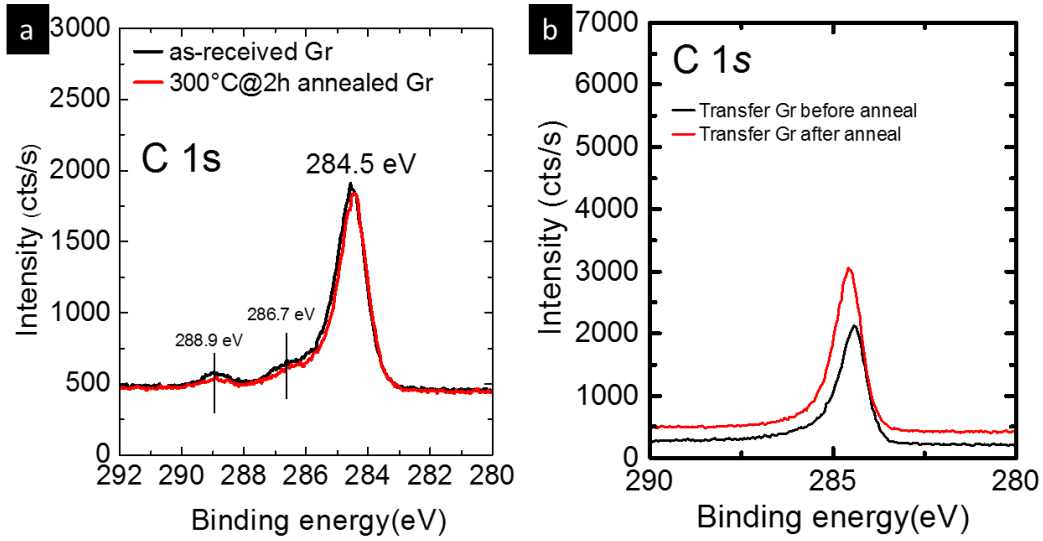

Figure 3.5 XPS spectra of C1s on a) purchased graphene before and after annealing and b) Transferred CVD graphene before and after annealing

3.3 Effect of UHV annealing on graphene

The electrical results of the fabricated FETs with the pre-annealing step aimed at reducing the PMMA residues is discussed here. Two samples purchased from Graphene platform (batch 1 and batch 2) were used for this study. One of the samples (batch 2) had a higher D peak in their Raman spectra which corresponds to the increased defect density in that sample.Raman measurements were done at few different spots to make sure that the obtained spectra is reproducible in all areas.

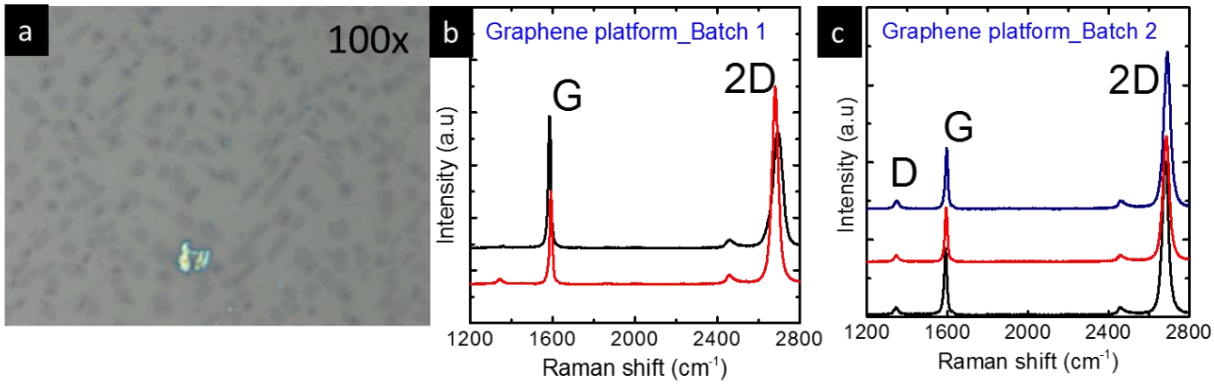

Figure 3.6 a) Optical microscope image of the CVD graphene with bilayer features at 100X b) and c) Raman spectra of the purchased CVD graphene from Graphene Platform batch 1 and 2 respectively.

The samples as received graphene samples were annealed at 300°C for 2 hours in Ultra High Vacuum (UHV ~ 10^{-7} Torr). The extracted back gate mobility values were comparable to the one without pre-annealing. There is no significant variation in the mobility values based on the changes in the D peak of the graphene sample.

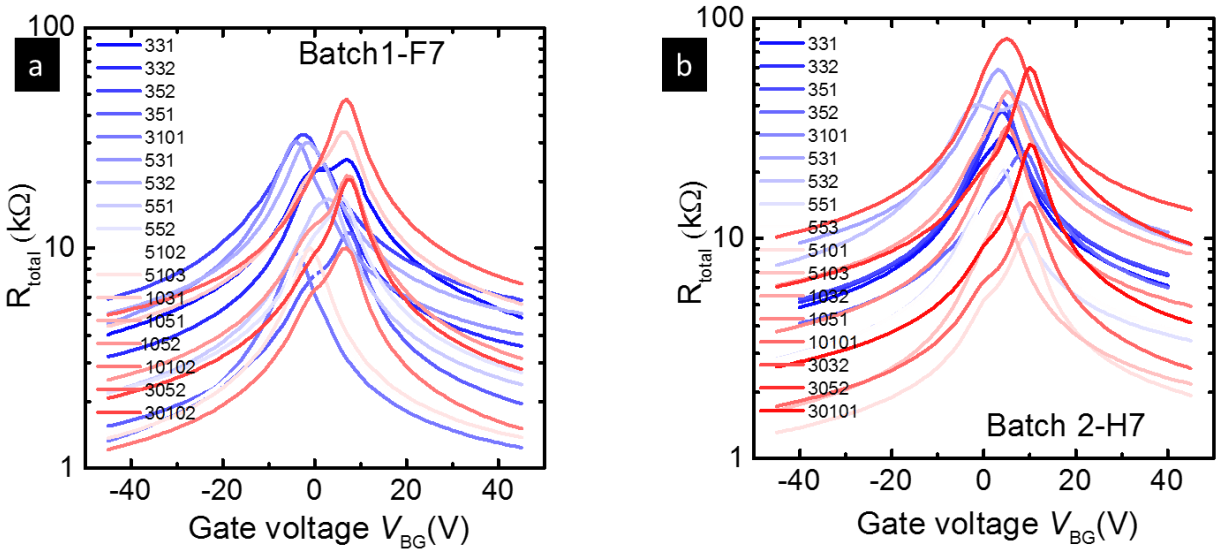

Figure 3.7 a) R_{Total} Vs BG transfer characteristics of GFETs fabricated from graphene platform batch-1 b) R_{Total} Vs BG transfer characteristics of GFETs fabricated from graphene platform batch-2

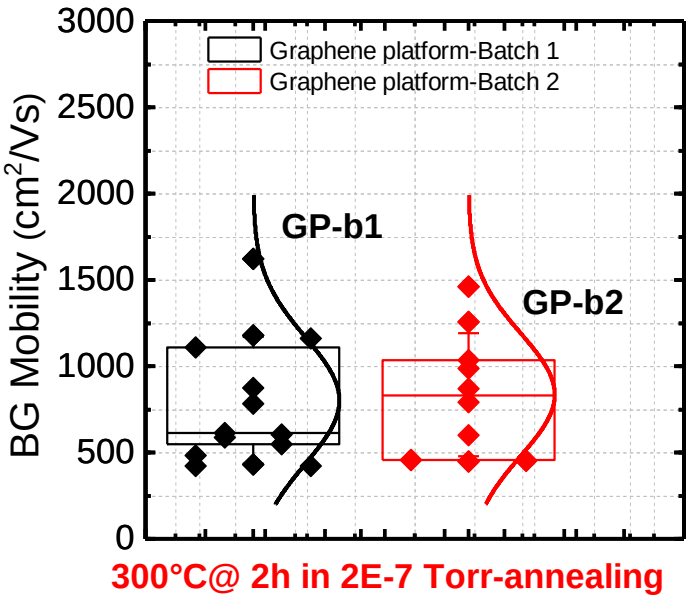

Figure 3.8 Back gate mobility values extracted from the constant mobility model based on the GFETs fabricated from the two graphene sources.

3.4 Ti based graphene surface cleaning process

Ti being a low work function metal, tends to oxidize readily and henceforth used as a gettering agent. Ti is also known to form an ordered structure on top of graphene with a uniform surface coverage [32]. This combined with the need of having a cleaner graphene surface, paved way for the fabrication of GFETs using a Ti-TiO_x hard mask process proposed by Venugopal [11]. In this process, a uniform layer of Ti is deposited on top of graphene and allowed to oxidize in ambient air resulting in the formation of TiO_x. The formed TiO_x layer can then be etched as required when there is a need to make a contact with the underlying graphene. Ti was suggested to remove any unintentional residues lying on top of the graphene surface. The work of Joiner *et.al* supports this theory wherein a sacrificial layer of Ti was used to clean the pristine graphene surface. Their calculated mobility when compared to the as fabricated devices without any cleaning procedure and HF cleaned graphene is higher. The Dirac point shift and the intrinsic carrier concentration were also found to be lower when compared to the HF treated and untreated graphene devices [33]. This initial results provided the main motivation for using TiO_x as the capping layer on top of the graphene surface. A thin layer of Ti (0.5nm) was deposited on top of the graphene surface and allowed to oxidize in the ambient air for the formation of TiO_x layer. Subsequent device fabrication steps were followed as described in the process flow wherein the TiO_x layer was etched at each steps whenever the contact is to be made with the graphene surface. Raman spectra show no significant damage of the graphene layer after the TiO_x etching in 100:1 HF. XPS results show a complete etching of the TiO_x layer in HF 100:1 solution.

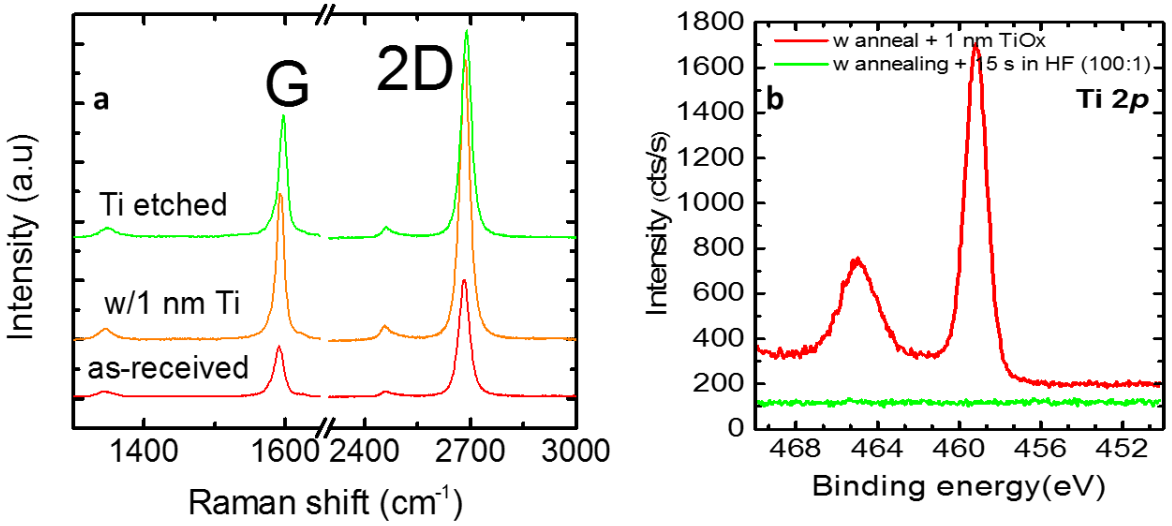

Figure 3.9 a) Raman spectra of graphene as received graphene, before and after TiO_x etch b) XPS spectra showing the complete removal of Ti from the graphene surface using 100:1 HF.

3.4.1 GFET performance with the TiO_x capping layer

Graphene FETs with the initial TiO_x capping layer with the provision of cleaning the interface is discussed in this section. In this study, 1nm Ti was deposited on top of the graphene surface as the sacrificial layer using the cryo e-beam evaporator. Purchased Graphene Platform samples were used for this study. Another GFET sample without the sacrificial Ti layer was fabricated to for process evaluation and comparison purposes. This set of devices has the 0.5nm Al seeding layer based on the results of the previous batch. Based on the R_{Total} Vs V_{BG} transfer curves, presence of Ti layer seems to have a reduced doping effect and slightly higher mobility when compared to the one without the protective layer .

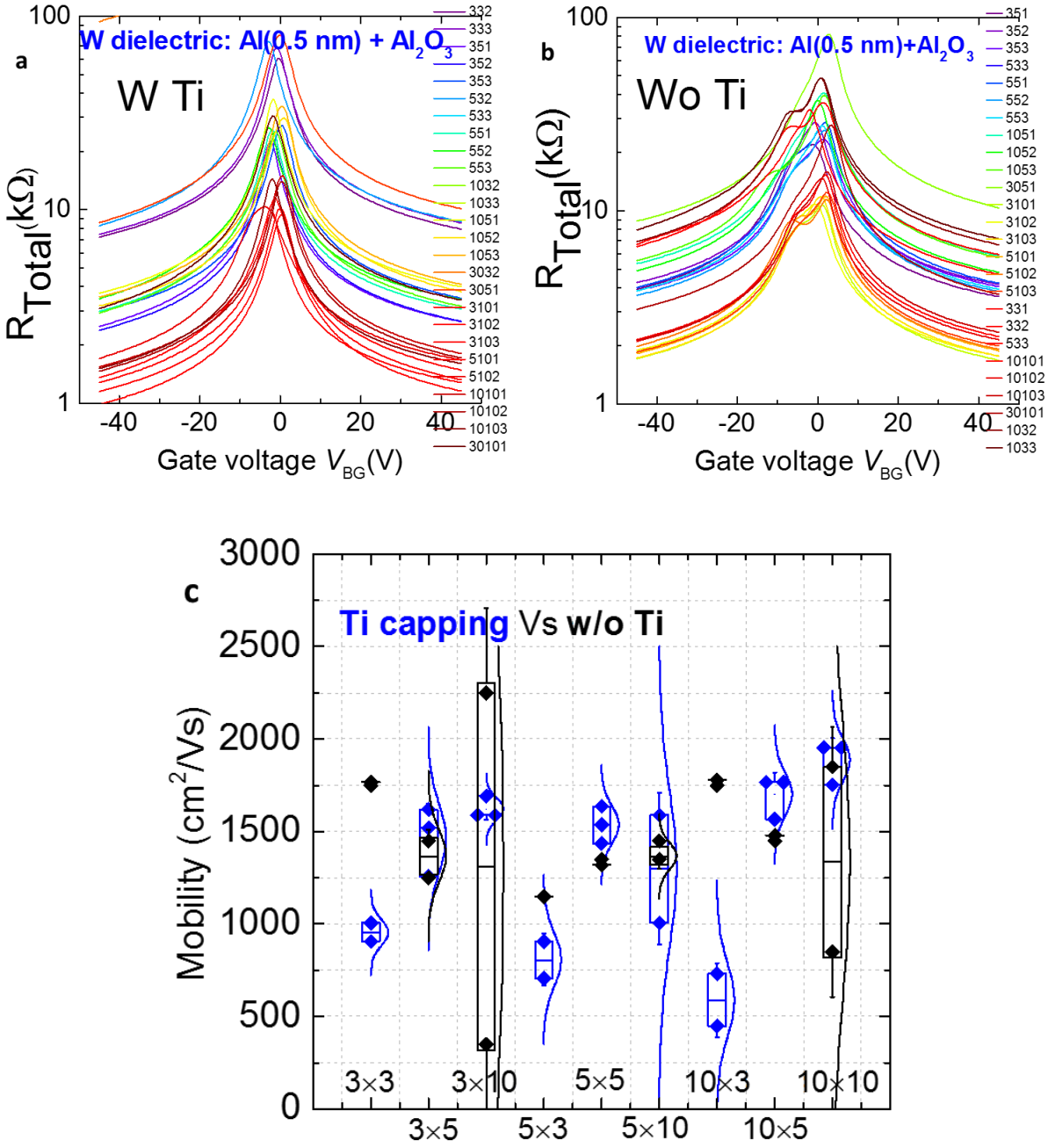

Figure 3.10 a) R_{Total} Vs V_{BG} transfer curves of GFETs with Ti capping, b) without Ti capping layer c) Extracted back gate mobility values of GFETs with and without Ti capping layer

The calculated mobility values in this set of devices were slightly lower than the previous batch and might be associated with the complexities involved in etching the TiO_x capping layer at various

stages of device fabrication whenever a direct contact with graphene is required. The schematic for this process is as shown in figure 3.12.

The reason for the appearance of the extra charge neutrality point (CNP) has been attributed to the difference in the Fermi level alignment in graphene at the contacts with respect to the bulk channel [36]. The separation of the two peaks is suggested to be the difference in the initial carrier concentration difference between the channel and the contact region. Irrespective of the choice of contact metal, the extra Dirac point seems to always appear in the p-branch in the transfer curves and is assumed that the positive charges are quite easier to be injected into the underlying SiO_2 trap centers rather than the electrons [36].

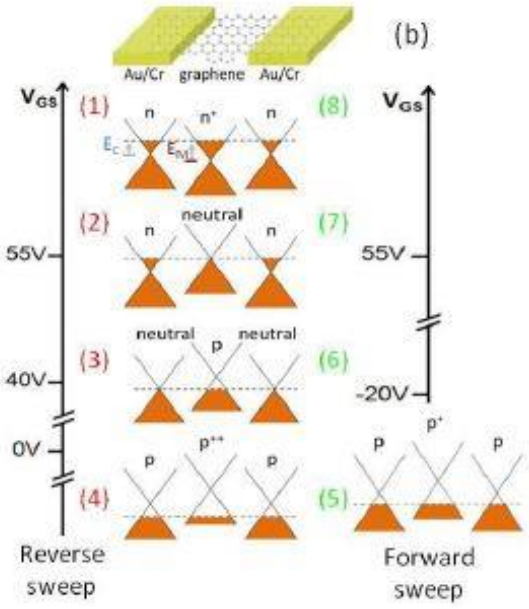

Figure 3.11 Band diagrams of graphene between source and drain as well as the position of the Fermi level at different V_{GS} from reference 36.

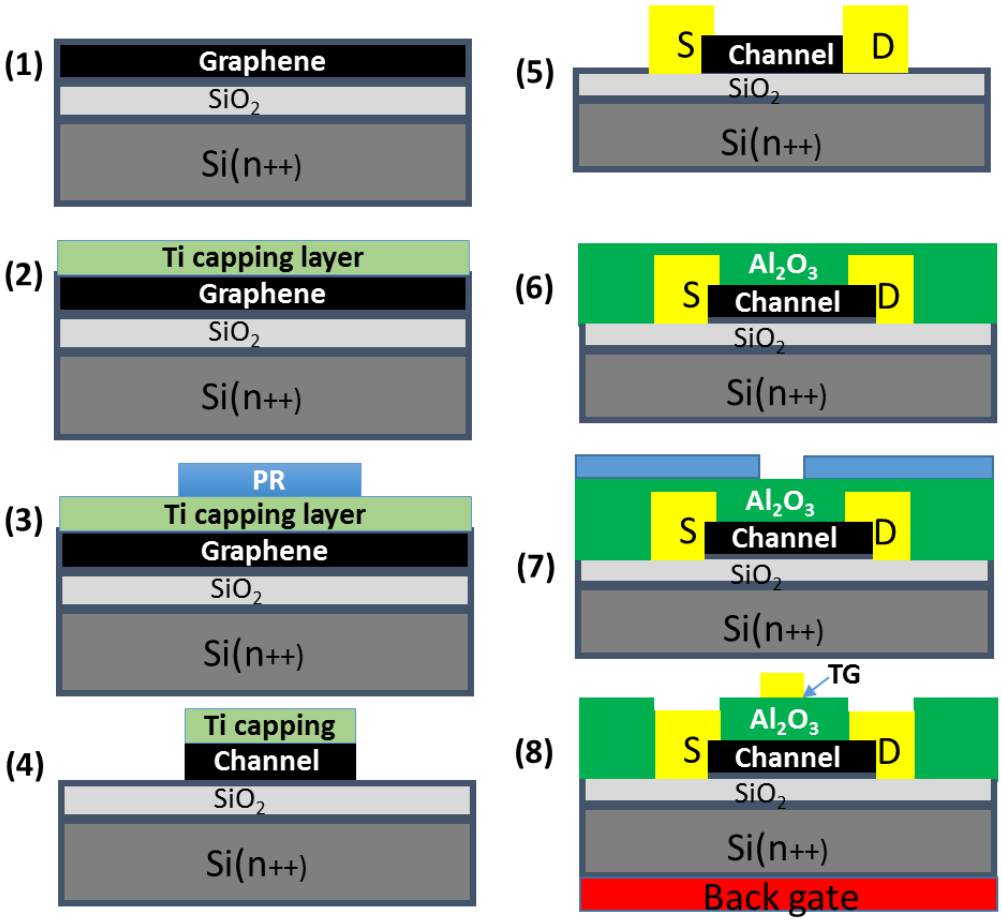

Figure 3.12 Schematic of the important GFET fabrication process steps with Ti capping layer. (1) As received CVD graphene on SiO_2. (2) Deposition of Ti capping layer. (3) Channel definition. (4) Etching of Ti capping layer and graphene in areas other than the channel. (5) Source and drain definition followed by Ni/Au (20nm/200nm) deposition using cryo e-beam evaporator and lift off. (6) Dielectric deposition using ALD. (7) Top gate definition. (8) Top gate contact, Ni/Au (20nm/200nm) deposition using cryo e-beam evaporator and 300nm Al backgate deposition using the e-beam evaporator followed by dielectric contact opening to facilitate wire bonding

3.5 Effect of seeding layer on the performance of GFETs

One of the important parameters in achieving high mobility in the graphene transistor is the encapsulation of the channel region with a good quality dielectric. As graphene is sp^2 hybridized with no out of plane bond to facilitate the nucleation of the dielectric [15], a seed layer is necessary to act as a nucleation site where the ALD surface limited reaction can be initiated. Previous work by Kim *et.al* has resulted in a mobility of ~8000cm^2/V. s after top gate processing wherein a thin layer of Al was used as a seeding layer before the deposition of the dielectric [29]. Pirkle *et.al* had demonstrated the integration of the dielectric using a thin seeding layer of Hf by e-beam evaporation although the XPS studies revealed the formation of HfC at the interface [30]..The effect of using different nucleation materials like Hf, Al, Ti and Ta on epitaxial graphene were analyzed by Robinson *et.al* and have demonstrated the conformal deposition of Al_2O_3, HfO_2 and TiO_2 with minimal degradation while Ta_2O_5 seems to degrade the graphene quality[31]. In order to optimize this part of the GFET fabrication process, two sets of nucleating agent namely 0.5nm Al and 0.5nm of Ti were deposited on top of graphene using the e-beam evaporator to facilitate conformal dielectric deposition. 200 cycles of Trimethyl Aluminum and Water were pulsed at 200°C with a growth rate of 0.1nm/cycle resulting in a total dielectric thickness of 20nm.

Purchased Graphene Platform samples were used for this study where a thin seeding layer (0.5nm) of Al and Ti were used to improve the dielectric conformity on top of the graphene surface. 200 cycles of Trimethyl Aluminum (TMA) and Water were pulsed at 200°C using the standard recipe as described in the appendix with ~0.1nm growth per cycle.

Keithley 4200A-SCS parameter analyzer was used to measure the fabricated graphene FETs. The backgate modulation was from -45 to +45V with a 0.5V step for a 100nm SiO_2 substrate

with a V_{DS} of 0.1V. As fabricated devices without the dielectric were also measured using the cryo-probe station (Lake Shore) to reduce any adsorption on the graphene from the ambient air. The samples were heated to 350K in the cryo-probe station for approximately 12 hours to remove O_2 and H_2O adsorption as there is a prior knowledge on the p-type doping of graphene by these species on CVD graphene [35]. The samples are then allowed to cool down to 300K followed by which the electrical measurements were performed using Agilent HP 4155A semiconductor analyzer. The mobility values calculated based on constant mobility model showed an increase in the mobility values for devices with 0.5nm Al seeding layer when compared to the devices with 0.5nm Ti seeding layer. This might be attributed to the dielectric used (Al_2O_3) where in the 0.5nm Al seed layer deposited using the cryo e-beam evaporator gets oxidized before transferring the devices to the Savannah Cambridge ALD chamber and acts as a template for the further dielectric growth. Therefore, a seeding layer of 0.5nm Al is preferred before the actual dielectric deposition for the complete integration of the dielectric with the graphene channel.

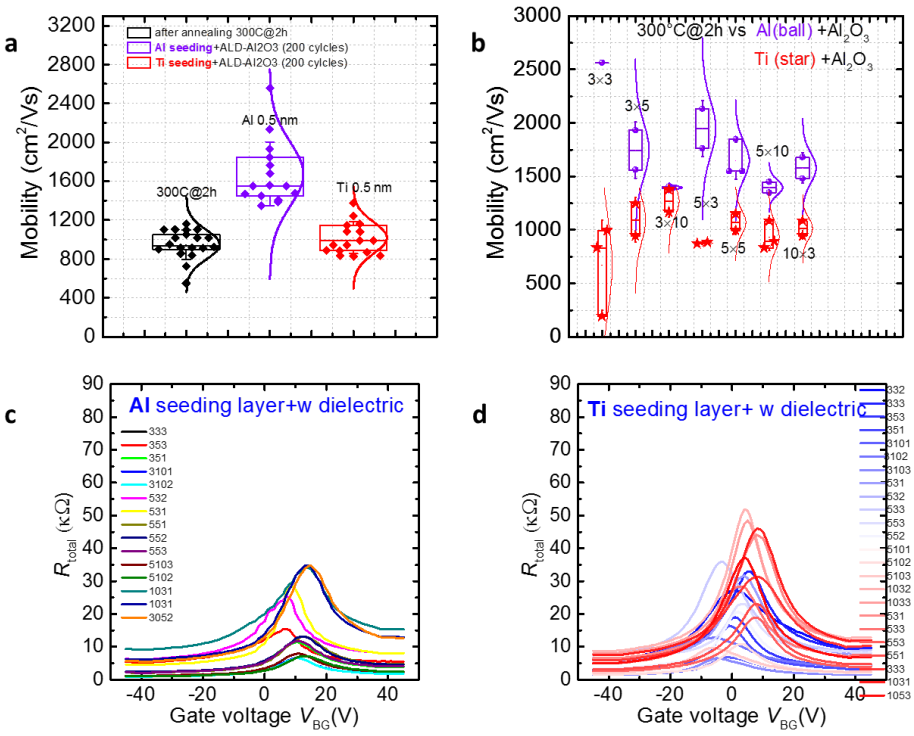

Figure 3.13 a) Mobility values of as fabricated and annealed sample, 0.5nm Al seed layer and 0.5nm Ti seed layer samples b) Mobility values of the devices based on different GLxGW dimensions c) and d) Total resistance (R_{Total}) of the device as a function of back gate modulation with Al and Ti seeding layer respectively

3.6 Effect of different oxygen source for the dielectric formation

In this study, the effect of H_2O and O_3 as the oxygen source for the dielectric formation was evaluated. Two sets of samples with and without Ti capping layer were fabricated and among them one had H_2O as the oxygen source for the dielectric deposition and the other had O_3. 200 cycles of TMA and H_2O were used to deposit Al_2O_3 at 200°C and 200 cycles of TMA and O_3 were used to deposit Al_2O_3 at 250°C. As fabricated GFETs without the Ti capping layer showed an increased mobility in this batch and after annealing, the mobility increases with a slight decrease

in n_O value. The lower mobility and higher n_O values could be attributed to possible Ti capping layer not getting etched completely as evident from the decrease in mobility after annealing. TMA and O_3 based Al_2O_3 dielectric showed a higher mobility after annealing.

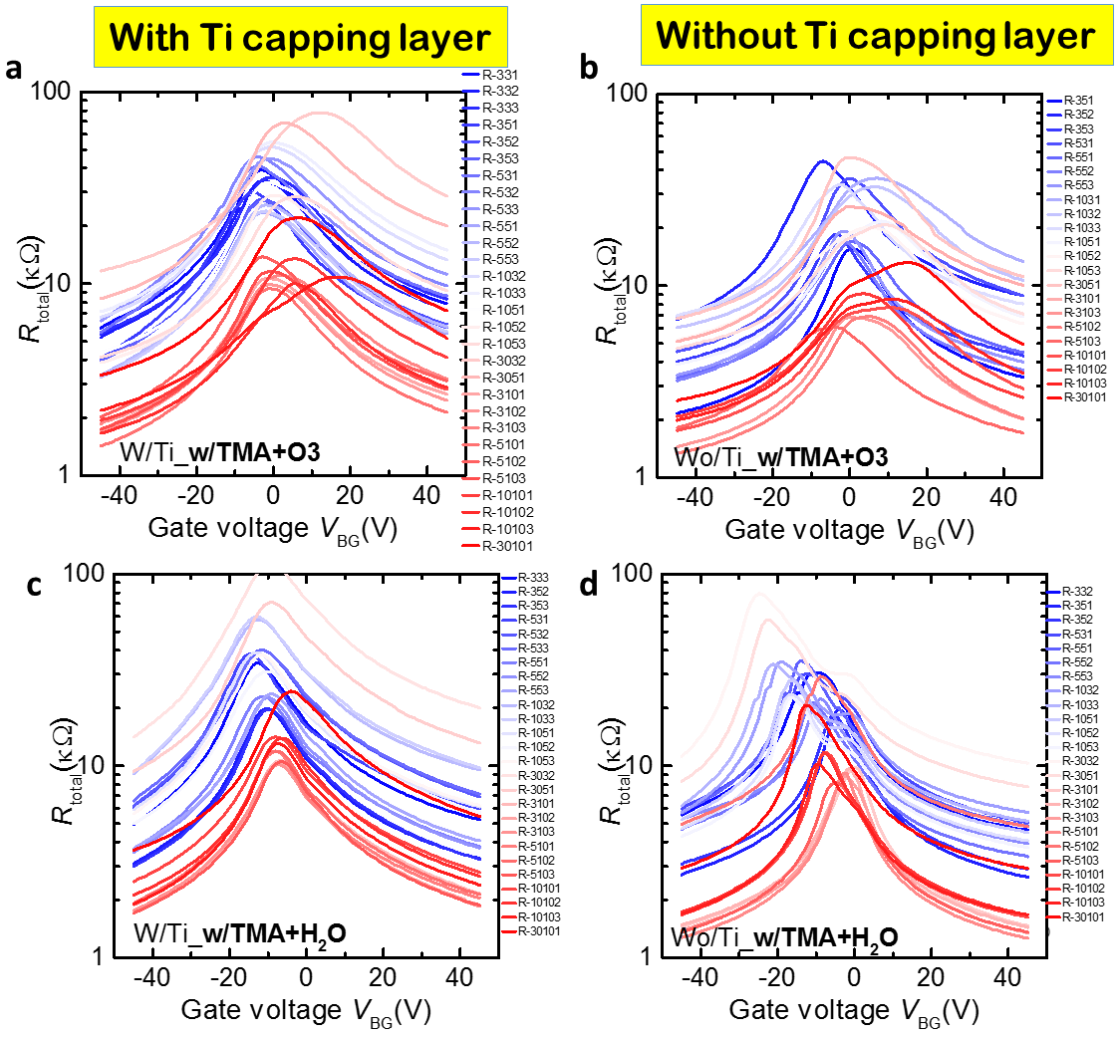

Figure 3.14 Transfer characteristic of GFETs with and without Ti capping layer a)and c)with Ti capping layer and with O_3/H_2O as the oxygen source respectively b)and d) without Ti capping layer O_3/H_2O as the oxygen source for the dielectric deposition respectively

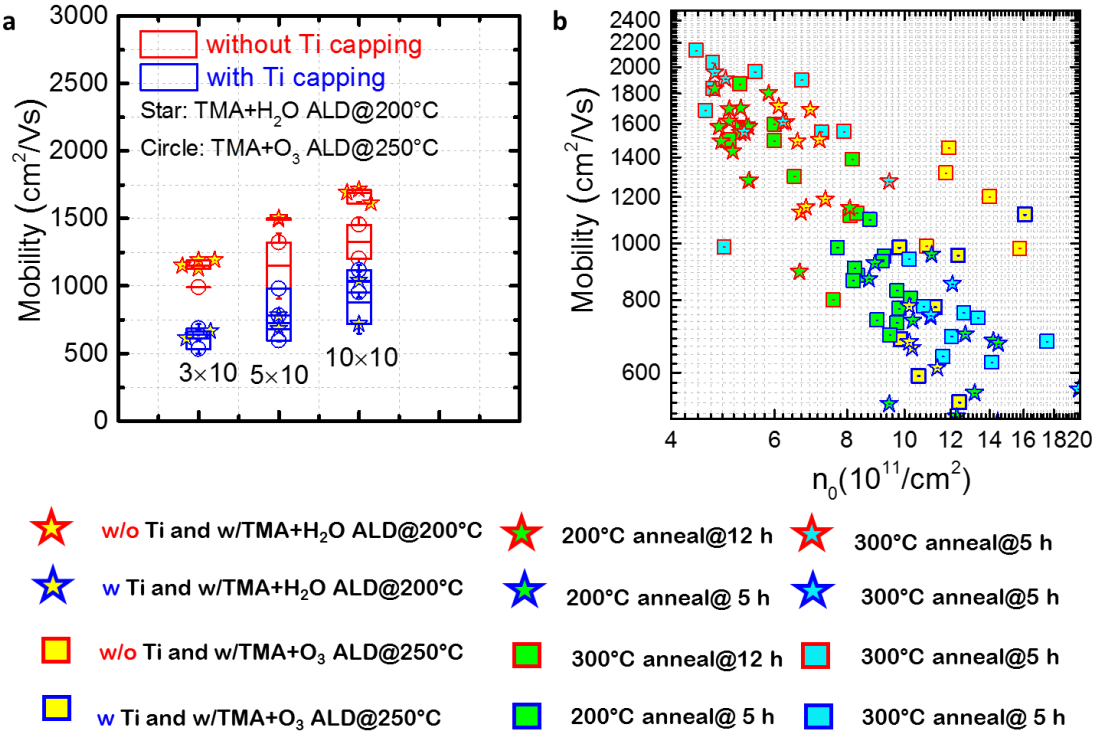

Figure 3.15 a) Back gate mobility of the GFETs with and without capping layer and b) mobility as a function of carrier concentration after annealing

3.7 Dielectric first GFET

The wire bondable dielectric first GFET electrical results are discussed in this section. One set of devices with the normal process where the source drain contacts were deposited after channel definition was made along with the dielectric first process for comparison. The contact resistance of the dielectric first processed devices was higher in this batch and the intrinsic carrier concentration was higher as a result of which the mobility extraction was difficult and the approximate value was calculated using the constant mobility model for comparing purpose.

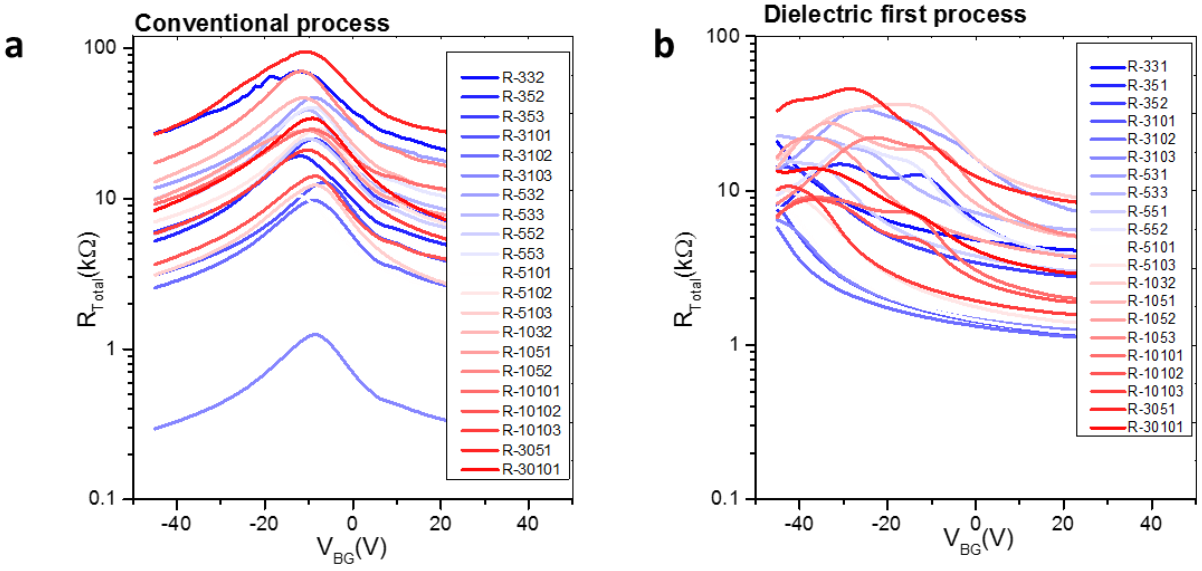

Figure 3.16 a) Transfer characteristics of the GFET (R_{Total} Vs BG) using the conventional device fabrication and b) Transfer characteristics of the GFET (R_{Total} Vs BG) using the dielectric first process

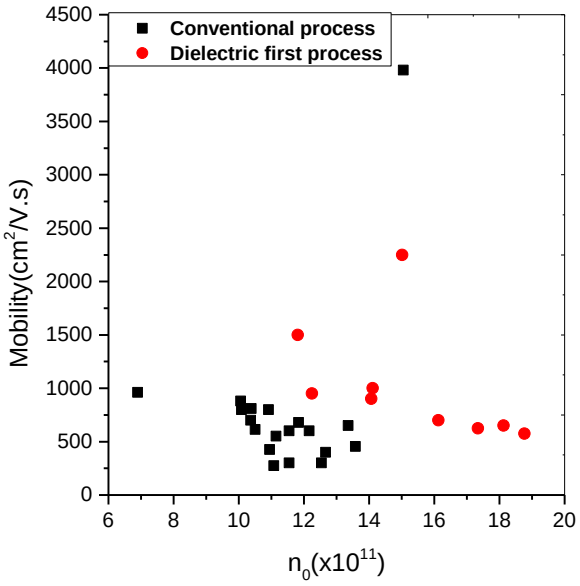

Figure 3.17 Mobility as a function of the intrinsic carrier concentration for the device fabricated using the conventional process flow and dielectric first process.

The higher intrinsic carrier concentration and higher contact resistance in the dielectric first processed devices could be attributed to the process residue introduced during the fabrication of the devices. Hence, a cleaning method before depositing the contact metal is required. Plasma cleaning id found to be one of the effective way in minimizing the unwanted process residues from the photoresist. The details of the plasma cleaning step and the corresponding electrical results are discussed in Chapter 4.

CHAPTER 4

CONTACT RESISTANCE

4.1 Plasma cleaning effect on reducing R_c

Contact resistance is a crucial parameter that determines the usability of a device. A higher contact resistance leads to a poor mobility in the graphene channel and attributed to the obstacle faced in the current injection. Under normal conditions, carriers are injected from the metal to the underlying graphene which transports it to the channel area [37]. In order to reduce the contact resistance of the device and reduce the doping effect on graphene, a suitable technique to satiate both were required. Plasma cleaning was found to be the suitable method to achieve the same. Reactive Ion Etch (RIE) and Direct Plasma ashing are the common techniques used for defining the graphene channel region. Direct plasma cleaning using the March Asher was found to be better than using Technics RIE system in terms of the damage created to the graphene as well as the difficulty involved in cleaning the photoresist residues on graphene after using RIE.

Robinson *et.al* had demonstrated the reduction in contact resistance in epitaxially grown graphene using a gentle O_2 plasma etch followed by heat treatment using TLM structures [38]. The oxygen plasma clean is suggested to form a "edge contact" with the graphene using a Cr/Pd/Au stack as contact metal [39-40].

The sequence of plasma cleaning is shown in the schematic below:

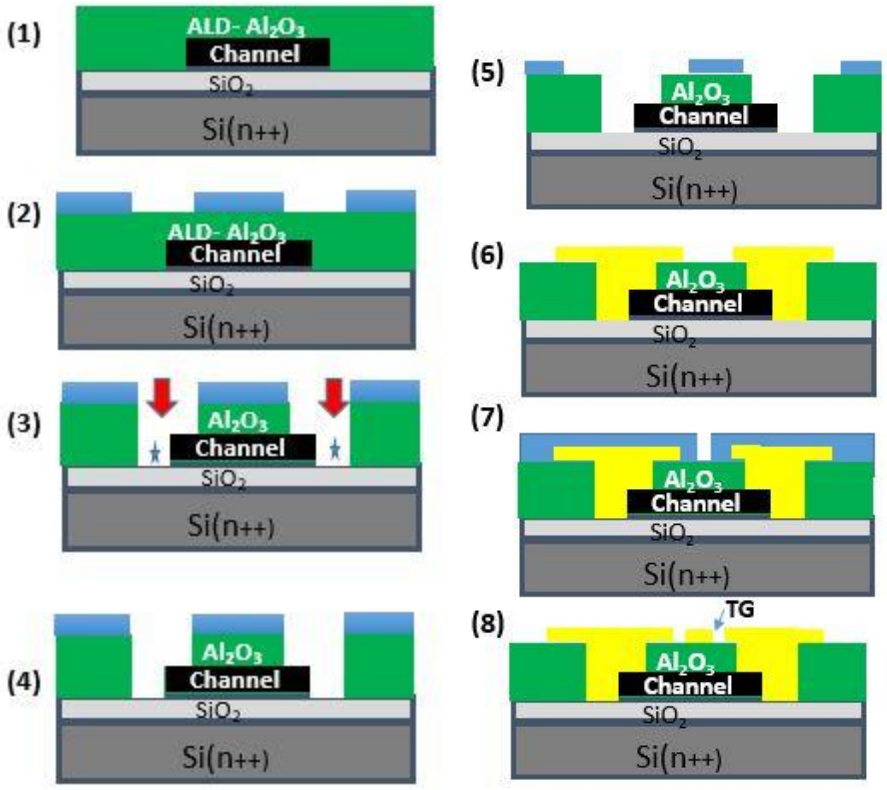

Figure 4.1 Schematic of the plasma cleaning process before contact metal deposition (1) Dielectric deposition after channel definition (2) Dielectric etch region definition (3) Etching the defined region using 100:1 HF solution (4) Plasma cleaned surface (5) Source/drain contact definition (6) Contact metal deposition using cryo e-beam evaporator and then lift-off in acetone at room temperature followed by IPA rinse and blow drying using N_2 gun (7)Top gate definition and (8) Top gate metal deposition and lift-off.

Based on these results, after the dielectric etch to access the graphene contact region, a mild direct plasma cleaning in the March Asher in Direct Plasma mode with a power of 50W, 10sccm of O_2 flow with a working pressure of ~180mTorr was utilized. The source and drain metal (Cr/Pd/Au)contacts were deposited using the e-beam evaporator after the plasma cleaning.

The devices subjected to the plasma clean showed a lower resistance (R_{Total}) when compared to the one without the treatment and also the Dirac point was close to 0V.

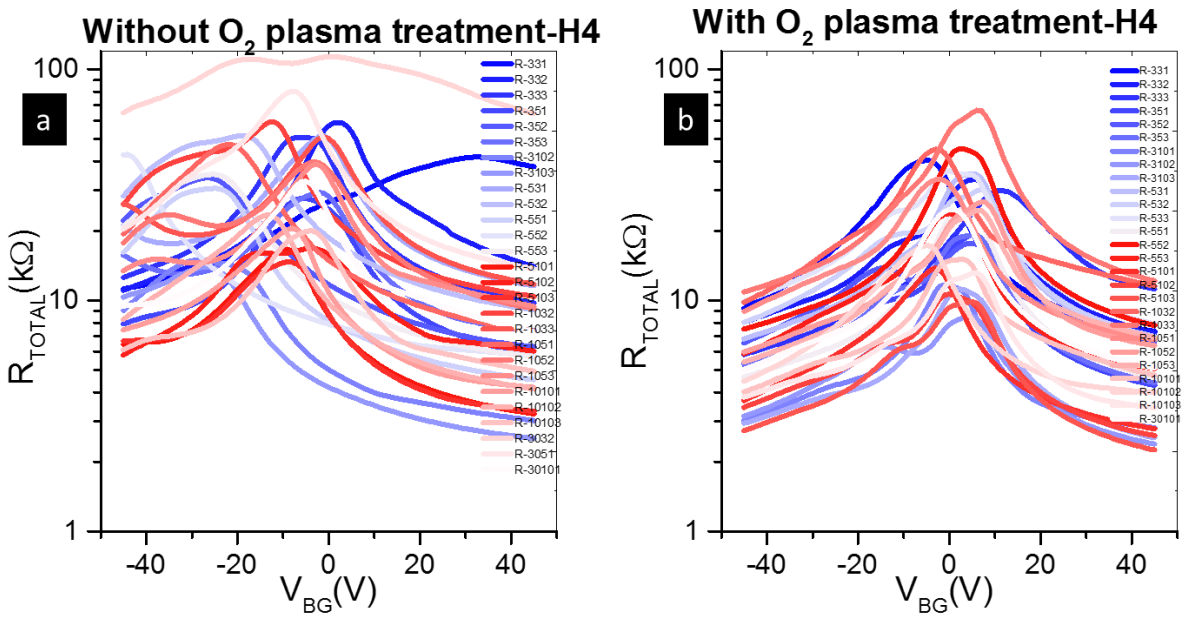

Figure 4.2 Transfer curves of the devices without O_2 plasma clean and with O_2 plasma cleaning. Both the devices were annealed at 200°C for 2h and H4 corresponds to the die number of the measured devices

After the top gate formation, the devices got degraded and the devices were open in the case of plasma treated condition. The thickness of the dielectric was increased to 30nm in order to evaluate if the degradation of devices were a result of the thickness of the dielectric used.

4.2 Optimization of plasma treatment conditions

Different plasma treatment conditions by changing the time duration for plasma treatment were evaluated and the dependence of device behavior were studied. The plasma power was maintained at 50W and the time duration of plasma exposure were set at 30s and 60s.

Based on the Raman spectra shown in figure 4.3, there is an increase in the intensity of D peak after 30s of plasma treatment and is more pronounced after 60s. There is also a shoulder peak

appearing after 30s of plasma treatment at ~1620 cm^{-1} next to the G peak and it represents the active surface defect modes corresponding to the sp^2 bonded carbon. The intensity of the shoulder peak increased after 60s of plasma exposure indicating the increase in surface defects.

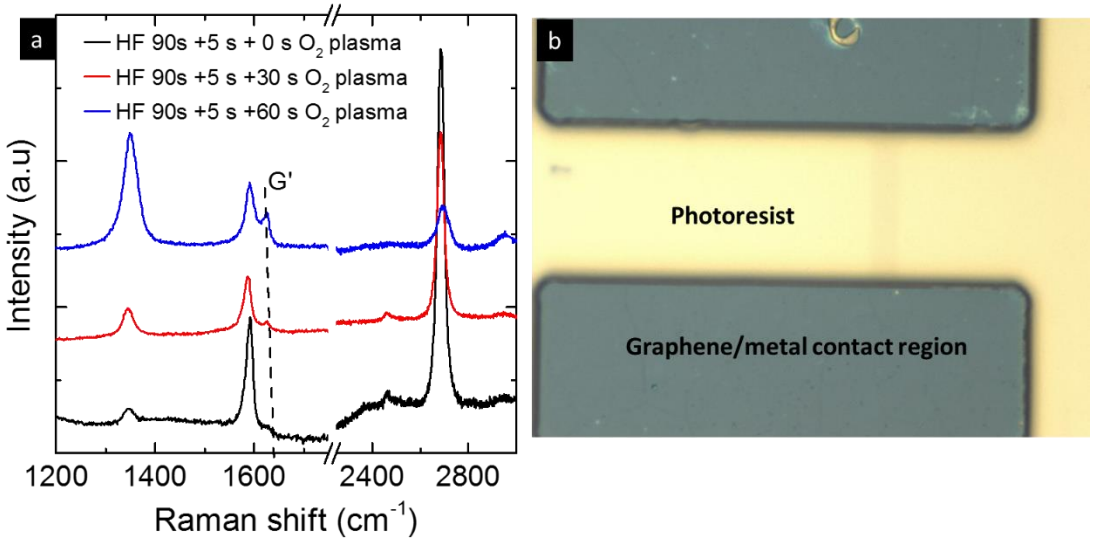

Figure 4.3 a) Raman spectra before and after plasma treatment using the March Asher at 50W RF power and b) the optical microscope of the graphene region that was subjected to the plasma clean

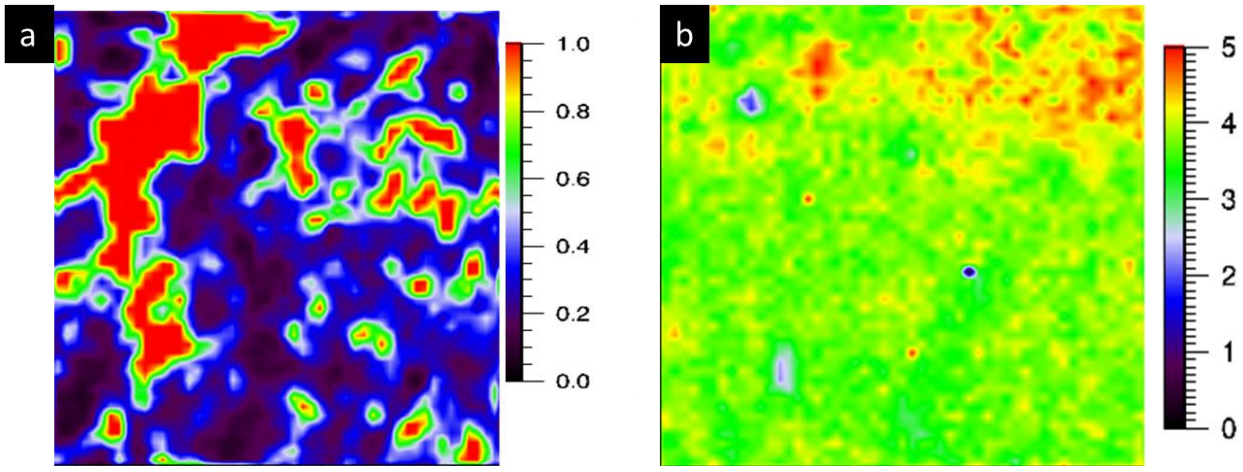

Figure 4.4 a) I_D/I_G ratio 10x10µm Raman maps on the graphene region after 30s plasma treatment b) I_D/I_G ratio 10x10µm Raman maps on the graphene region after 60s plasma treatment

The I_D/I_G ratio of a 10x10µm Raman maps on the graphene region also show the increase in the defect density by the increase in the plasma processing time. The I_D/I_G ratio has almost increased by a factor of 4 when compared from the 30s to the 60s plasma treatment in the graphene contact region.

The increase in the defects of graphene in the contact region is expected to create more edge contacts and thereby a reduction in the contact resistance resulting in improvised device performance. The transfer characteristics of the 30s and 60s plasma treated GFETs as a function of back gate modulation are shown below along with devices with no plasma treatment and devices with 90s (short dielectric etch time compared to 90+5s) HF 100:1 treatment.

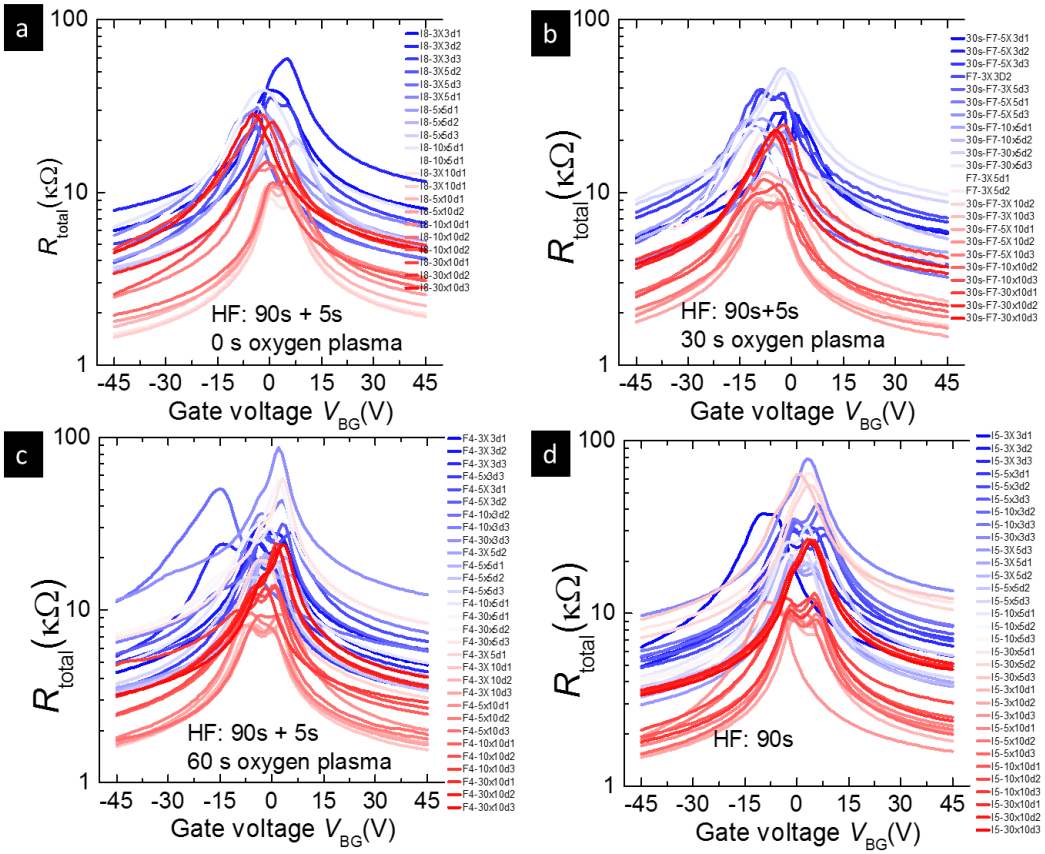

Figure 4.5 a) Transfer characteristics of GFETs with no O_2 plasma treatment b) with 30s O_2 plasma treatment c) with 60s plasma treatment and d) with short dielectric etching time

The appearance of 'Double-Dirac' point denotes the unintentional doping of graphene during the device fabrication. The extracted mobility values based on the back gate modulation using the constant mobility model is as shown below along with a plot showing the mobility as a function of intrinsic carrier concentration.

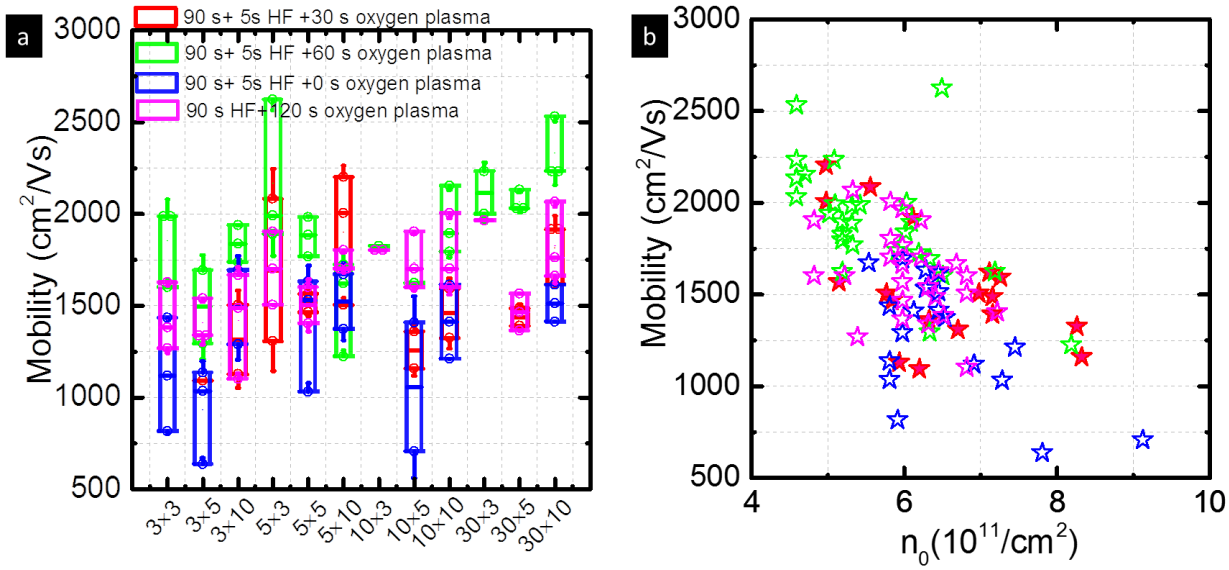

Figure 4.6 a) Back gate modulated mobility using the constant mobility model as a function of different GLxGW and b) Mobility as a function of intrinsic carrier concentration. The same color has been used in both the figures to differentiate the different process parameters used.

GFETs with 30s and 60 s O_2 plasma treatment show a higher mobility when compared to no plasma treatment and incompletely dielectric etched devices (90s etching in 100:1 HF). This behavior can be attributed to the higher contact resistance in the devices as a result of unintentional process residues and improper dielectric etching respectively. This also shows that the graphene channel quality is not deteriorated during the O_2 plasma treatment. On the whole, 30s to 60s O_2 plasma cleaning improves the mobility of the GFETs by the removal of residues generated during the processing of the devices. The extracted $2R_C$ values based on the back gate modulation does not

show a particular trend as of now. Further detailed analysis on the impact of O_2 plasma cleaning on the contact resistance is required. Advanced technique like Transmission electron microscopy (TEM) imaging is required to get an idea on the type edge contact created using the O_2 plasma treatment.

4.3 Metal contact study

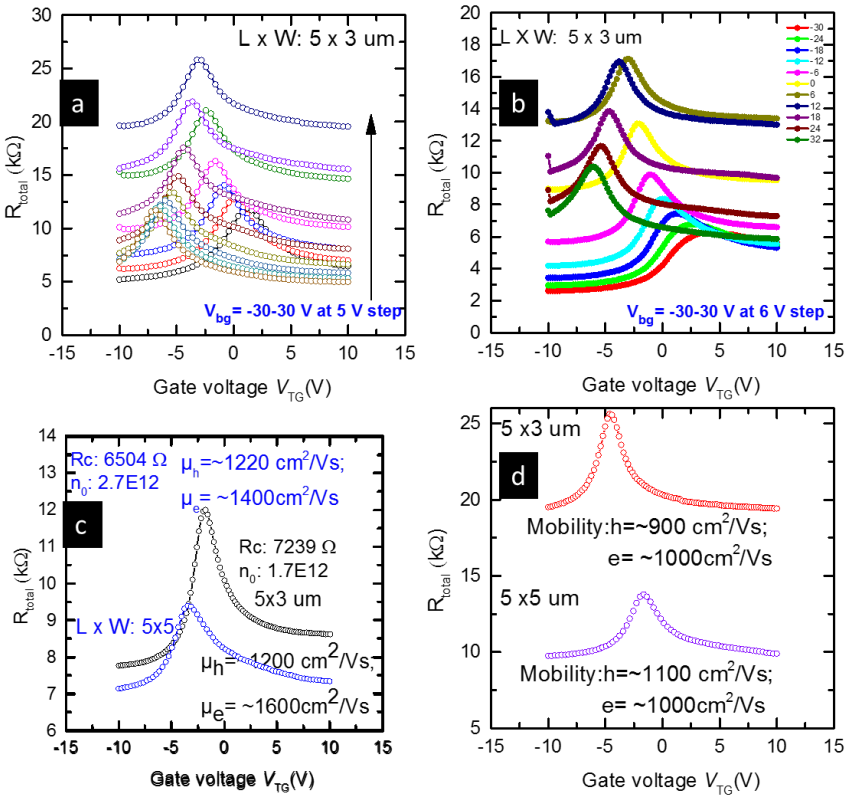

Figure 4.7 a) Resistance (R_{tot}) versus V_{TG} curves at different V_{BG} with a step of 5V for a GFET with Cr(15nm)/Au(65nm) contact metal for a device with a Gate Length (GL)x Gate Width (GW) of 5X3µm b) Resistance (R_{tot}) versus V_{TG} curves at different V_{BG} with a step of 6V for a GFET with Ni(20nm)/Au(100nm) contact metal for a device with a Gate Length (GL)x Gate Width (GW) of 5X3µm c) Resistance (R_{tot}) versus V_{TG} curves for a device with GLxGW 5x5µm, 5x3µm with Ni(20nm)/Au(10nm) contact metal d) Resistance (R_{tot}) versus V_{TG} curves for a device with GLxGW 5x5µm, 5x3µm with Cr(15nm)/Au(65nm) contact metal.

In this study, two different contact metal stacks Cr(15nm)/Au(65nm) and Ni(20nm)/Au(100nm) were used as source/drain contacts in the graphene FETs. Figure 4.7 shows the electrical characteristics of dual gated graphene FETs. Figure 4.7 (a) shows the R_{total} versus V_{TG} curves at different V_{BG} with a step of 5V for a GFET with Cr/Au contact and Figure 4.7 (b) shows the R_{total} versus V_{TG} curves at different V_{BG} with a step of 6V for a GFET with Ni/Au contact.

Figure 4.7 (c) and (d) shows the top gate modulation for devices with Cr/Au and Ni/Au contacts respectively. In both the cases, the device with bigger gate length and width dimension (5x5µm) has a lower total resistance. The devices with Ni/Au as the contact metal exhibit a lower total resistance with a higher mobility. Based on these results, Ni/Au was used as the source/drain and top gate contacts for most of the graphene FETs fabricated.

Further studies are required and planned to evaluate the contact resistance of other known ohmic contact formers with graphene like Ti/Au and Pd/Au. This will give an insight on the contact resistance dependence on the metals with different work function.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The mobility values extracted using the constant mobility model were used to determine the effectiveness of the GFET fabrication process. Based on these results, various steps in the basic GFET fabrication process were optimized. Incorporation of UHV annealing of graphene reduces the PMMA residue imparted during the CVD graphene transfer process, while a 0.5nm Al seeding layer before the dielectric deposition has resulted in a conformal dielectric layer with improved mobility. O_3 based dielectric deposition shows an improved performance after annealing although proper care should be taken in order to prevent the damage of graphene by O_3. The TiO_x capping layer for cleaning the interface is currently not reproducible due to the possible complexities involved in depositing a conformal 0.5nm Ti layer and etching the TiO_x layer at various stages of device processing as described earlier. Dielectric first process is more suitable for wire bonding the devices during packaging as the adhesion of Ni seems to be better on Al_2O_3 rather than on SiO_2. Plasma cleaning has reduced the shift in Dirac points and is closer to 0V implying the control over the doping of graphene in contact region. An increase in the defect density of graphene by the plasma cleaning step is expected to create more edge contacts. Initial $2R_C$ values extracted from the back gate modulated mobility fit of the plasma cleaning step incorporated devices does not not follow a particular trend. Further analysis is required to comprehend the reason for the

improved mobility without any significant variation in the contact resistance. Using the UHV annealing, 0.5nm Al as dielectric seeding layer with the process flow outlined in figure 2.12 has resulted in a higher mobility value of ~3000cm^2/V.s compared to the initial value of ~1000cm^2/V.s. From the packaging point of view, the dielectric first process is preferred and still needs minor optimization in order to achieve a higher mobility value.

5.2 Future Work

We have developed a process for the fabrication of graphene field effect transistor on a large scale with good back gate modulation of the graphene in the transistor. Transistors with top gate modulation is preferred for practical applications owing to its lower parasitic capacitance and further optimization of the top gate formation steps are required to achieve the same. All the transistors fabricated in this work had thermally grown SiO_2 as the back gate dielectric, different substrates like Al_2O_3, hBN or SAMs could provide a transistor having improved mobility due to charge screening and lesser scattering which could be one of the potential venues to be explored. Capping of CVD grown graphene with a protective metal/ metal oxide layer using the e-beam evaporator before its transfer to the desired substrate could prevent the possibility of inflicting any damage to the surface of the graphene. Fabrication of GFETs using this capping layer could be evaluated. Metal etching process where the metal is first deposited using the e-beam evaporator followed by source/drain and top gate definition using photolithography followed by etching the metal in regions other than the desired area could be explored for large scale fabrication of FETs. This alternative route could overcome the difficulties faced in the conventional lift-off process where there are regions without proper lifting off of metals and the risk of having higher photoresist

residues at the contact metal/graphene interface. A basic outline of the fabrication of the GFETs using the metal etching process is shown in the schematic below.

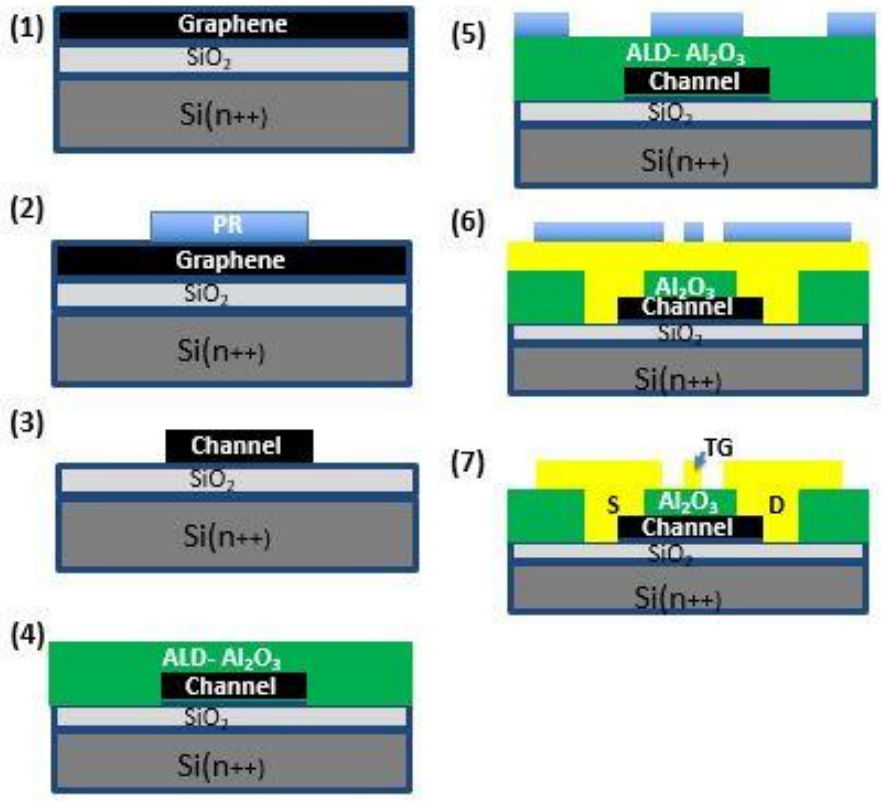

Figure 5.1 Schematic of the GFET fabrication using the metal etching process. (1) As received graphene on SiO_2/Si. (2) Graphene channel definition. (3) Ashing of graphene from other areas and removal of photoresist. (4) Dielectric deposition on the channel region. (5) Definition of graphene/metal contact region to etch the dielectric. (6) Source/drain and top gate metal deposition followed be defining the source/drain and top gate regions by photolithography. (7) Etching the contact metal at other regions using their respective etchant and removal of the photoresist used earlier to define the area.

Initial studies on fabrication of graphene transistors by metal etching process using Au as the contact material had been investigated. The reported mobility values are quite low, proper process optimization and usage of known ohmic contact formers with graphene could help in the development of metal etching process.

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