A 0.1 PS RESOLUTION COARSE-FINE TIME-TO-DIGITAL CONVERTER

WITH 2.21 PS SINGLE-SHOT PRECISION

by

Huihua Huang

APPROVED BY SUPERVISORY COMMITTEE:

_____

Carl M. Sechen, Chair

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Jin Liu

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Hoi Lee

_____

Dongsheng Ma

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HUIHUA HUANG, BE, MS

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Huihua Huang, PhD
The University of Texas at Dallas, 2018

Supervising Professor: Carl M. Sechen, PhD

This dissertation proposes a new type of time-to-digital converter based on a resistor-capacitor (RC) delay line that offers low power consumption, high speed and high resolution with error-correction circuitry. The 14-bit, 0.1 picosecond resolution interpolating coarse-fine time-to-digital converter (TDC) has been developed in 45 nm complementary metal–oxide–semiconductor (CMOS) technology. It is based on an asynchronous buffer delay line and an RC delay line. A lookup-table (LUT) based calibration scheme was developed to correct non-linearities due to process, voltage and temperature (PVT) variations. The root mean square (rms) single-shot precision of the TDC is 4.18 picosecond (ps) without the LUT but is 2.21 ps with the LUT. The power consumption is 2.05 mW at 500 MHz with a 1.3 V operating supply voltage. Compared to other high-resolution state-of-the-art TDCs, the proposed TDC achieves the best figure-of-merit (FOM) of 0.723 fJ per conversion step.

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CHAPTER 1

INTRODUCTION[1]

1.1 Introduction to TDC

The time-to-digital converter (TDC) has been used for more than 30 years to measure a time interval, i.e., the time between two events. The time intervals between two rising edges or two electrical timing signals, also called *start* and *stop* signals, will be quantized and then converted into digital data. Nowadays the achieved time resolution has been reduced from hundreds of picoseconds to sub-picosecond.

The TDC has been widely used in many applications such as particle detection in high energy physics, laser range finding, frequency counters and other measurement devices. The performance of a TDC is determined by the resolution, precision, dynamic range, nonlinearity, speed and power consumption.

For many years the development of the TDC has traversed through several generations [1]. The first generation is the analog TDCs, basically implementing current-integration techniques, consisting of a time-to-voltage or a time-to-amplitude conversion (TAC) and an Analog-to-Digital Converter (ADC) [2]. The TAC typically consists of a sample-and-hold circuit, a charge-pump and a capacitor. The ADC converts the sampled voltage to binary codes. But the analog TDCs are

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[1] ©2014 IEEE. Portions Adapted, with permission, from H. Huang, and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS," IEEE, Circuits and Systems Conf. (DCAS), pp. 1-4, Oct. 2014.

not suitable for technology scaling. The complicated architectures and the large power consumption also limit its applications.

The second generation is the digital TDCs, including the counter-based TDCs [3] and the flash TDCs [4]. These TDCs achieve large dynamic measured range, but can only achieve the resolution of the gate delays, limited by the frequency of the reference clock and the technology. Also, they are sensitive to the metastability in the counter's registers, usually flip-flops.

The third generation is the sub-gate delay TDCs, achieving smaller time steps by using delay-line based [5], phase-locked loop (PLL)-based and delay-locked loop (DLL)-based techniques [6]. By using analog delay cells, a built-in DLL and multiphase sampling techniques, sub-gate delay time can be achieved.

The sub-picosecond TDCs, which is the fourth generation, are widely used currently. Examples of the techniques include time stretching [7], Vernier differences [8, 9], cyclic TDC using a pulse-shrinking delay line [10], gated-ring-oscillator TDCs [11], time amplifying [12], successive approximation [13, 14], and Delta-Sigma [15]. These techniques are used in the multi-level interpolation with hybrid architectures to achieve the sub-picosecond resolution, improve the linearity of the interpolators, increase the dynamic range and reduce the power consumption. Nowadays the achieved time resolution has been reduced from hundreds of picoseconds to sub-picosecond.

A TDC using a single DLL and an RC delay line is one of the third generation TDC architectures. The RC delay line can achieve a unit delay on the order of picoseconds. It has the advantage that the unit delay, which is based on the resistance and capacitance, is insensitive to supply and temperature changes. Traditionally, the value of R or C or both will be tuned in an RC delay line to set the unit delay and to achieve a wide tuning range [16-19].

1.2 Introduction to Our Novel Approach

This paper presents a new type of TDC based on an RC delay line that offers low power consumption, high speed and high resolution with error-correction circuitry. Using mostly all-digital components, this proposed TDC will scale with future technologies.

A two-level interpolating TDC, with a coarse-fine architecture is used to implement high-precision time interval measurements. Figure 1.1 shows the basic concept of the proposed TDC. The *start* and *stop* signals are fed into the dynamic buffer delay-line which provides the most significant 7b of resolution. The generated signals go through the time residue generator, indicating the resulting delay residue, and this is propagated along the second level RC-chain, providing the last 7b of resolution. Finally, the digital code is corrected employing LUT-based calibration.

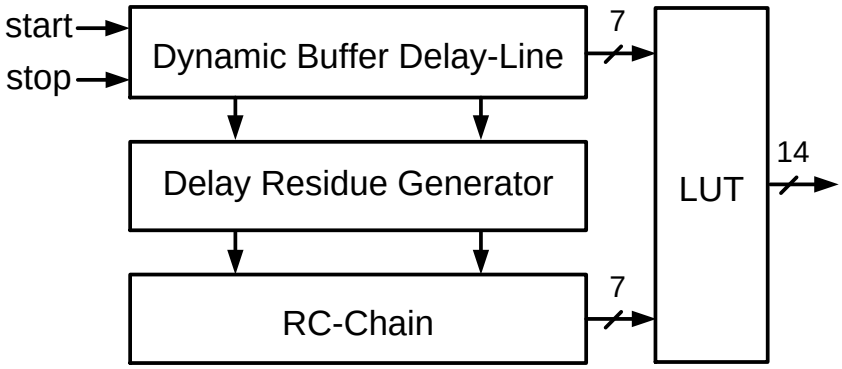

Figure 1.1. TDC block diagram

Chapter 2 gives an overview of the TDC basis, applications and history as well as the characteristics and performance metrics. The description and architectures of the developed TDCs are presented in Chapter 3. Chapter 4 introduces the proposed TDC architecture and describes the design of the building blocks at the architectural level and the circuit level. Chapter 5 presents the experimental results and the summary. The conclusion is given in Chapter 6.

CHAPTER 2

TDC OVERVIEW

2.1 TDC Basis

The time-to-digital converter (TDC) is a device used for measuring a time interval. Two electrical signals, usually called *start* and *stop*, determine the beginning and the end of the time interval respectively. The measuring result will be quantized to a digital representation, as shown in Figure 2.1. TDCs are also called time digitizers (TD), time counters (TC), etc.

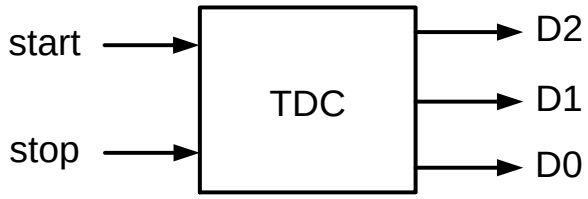

Figure 2.1. TDC block diagram example: a 3-bit TDC

Figure 2.2 shows an example of the input and output signals of the TDC in Figure 2.1. The time interval between *start* and *stop* signal is measured and converted to the output D2D1D0 in binary code.

The relationship between measured time and digital output codes is given by

$$T_{in} = T_{LSB} \cdot \sum_{k=0}^{n-1} D_k \cdot 2^k \tag{2.1}$$

where T_{in} is the measured time interval between *start* and *stop*, T_{LSB} is the minimum unit of time measurements, n is the number of bits and D is the digital code of the TDC outputs.

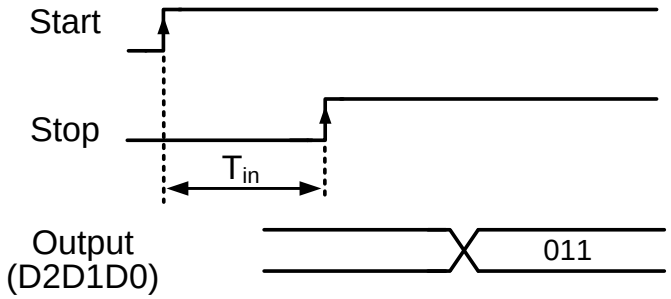

Figure 2.2. TDC signals example: a 3-bit TDC, where T_{in} is the measured time interval

Figure 2.3 shows the ideal transfer function example for a 3-bit TDC.

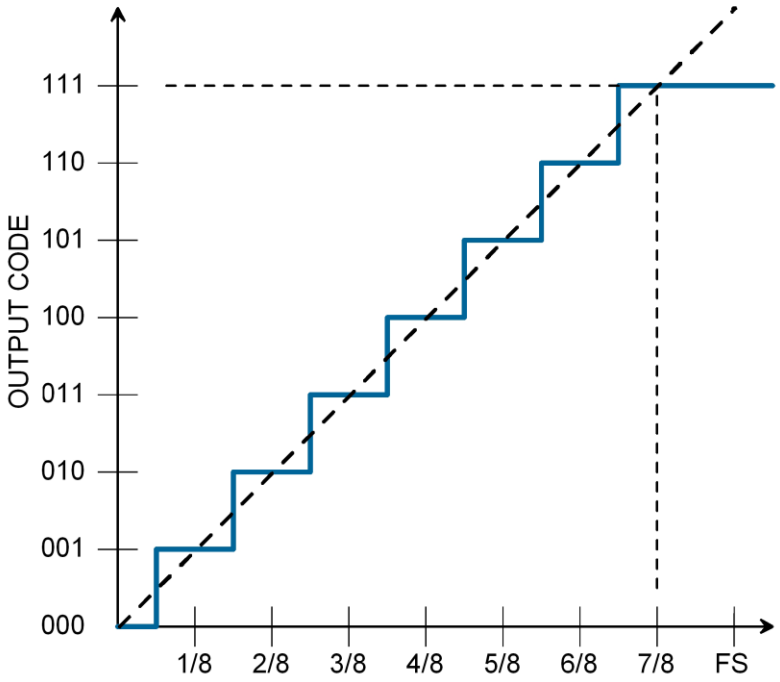

Figure 2.3. Example of a TDC transfer function (a 3-bit TDC)

2.2 TDC Applications and History

The applications of TDCs include applying time interval measurement and using circuit structures applied to time interval measurement. TDCs are widely used as phase detectors in digital PLLs, measurement devices, such as digital scopes and logic analyzers, time of flight measurements, laser distance meters, such as laser range finding, golf range finder or police radar guns, particle detectors, space science instruments, ultrasonic and optical flow meter measurements, as well as high speed signal capturing, demodulators, data converters, *etc*.

The history of TDCs began with experimental high energy physics needing to measure time of flight. Time of flight or TOF is the process of measuring the time a particle, object, signal or stream takes to travel over a known distance. This time of flight time measurement process is accomplished using a detector and a TDC. The all-digital PLL is the first and most famous TDC application.

2.3 Characteristics and Performance Metrics

A set of merits are used to evaluate the performance of a TDC. The important characteristics of a TDC include resolution, single shot precision, dynamic measured range, nonlinearity, conversion time, and power dissipation.

2.3.1 Resolution

The time resolution is specified in terms of the time corresponding to a Least Significant Bit (T_{LSB}) and corresponds to the smallest delay that can be discriminated. It depends on the circuit characteristics and noise performance.

2.3.2 Single-shot precision

Single-shot precision of a TDC is defined as the standard deviation of the distribution of the measurement results around the mean value, when a constant time interval is measured repeatedly [2, 13].

The rms single-shot precision σ_{rms} defines the root mean square value of the interpolator precision over the whole interpolation region. It's based on the repeated measurement of a single time interval and reveals the effects of nonlinearity and quantization noise in a single parameter. The σ_{rms} is given as

$$\sigma_{rms} = \sqrt{\sigma^2_{quantization} + \sigma^2_{std\_INL} + \sigma^2_{clk\_jitter} + \sigma^2_{signal\_jitter}} \tag{2.2}$$

where the other four items are 1) rms quantization error, 2) the standard deviations of the integral nonlinearities of the start and stop interpolators, 3) the rms jitter of the reference clock, and 4) the rms jitter of the start and stop signals.

2.3.3 Dynamic Range

Dynamic range is the maximum time interval to be measured by the TDC, as shown in Figure 2.4. If the TDC resolution is known, the dynamic range is

$$DR = 2^N \cdot T_{LSB} \tag{2.3}$$

where DR is the dynamic range, N is the number of bits of the TDC output, and T_{LSB} is the resolution.

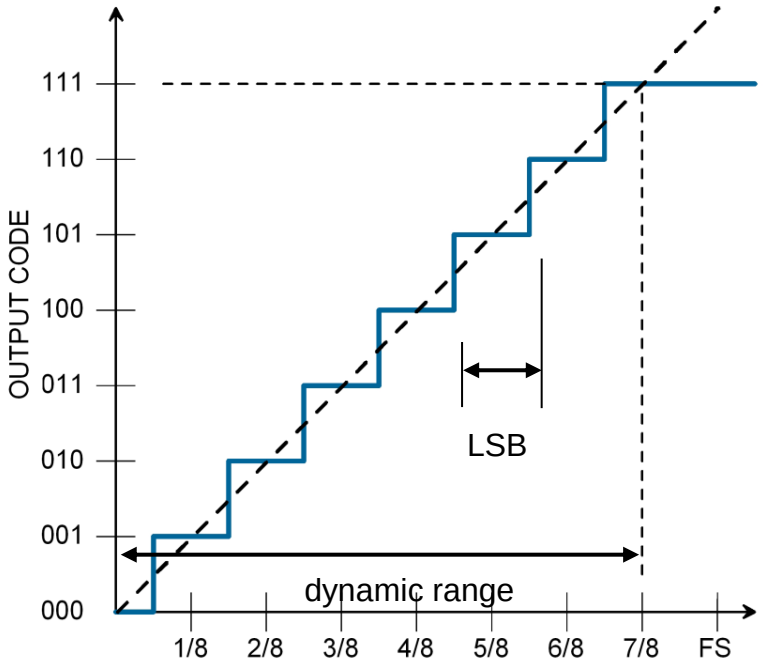

Figure 2.4. Dynamic range example

2.3.4 Nonlinearity

There are two types of nonlinearity performances, differential nonlinearity (DNL) and integral nonlinearity (INL).

The DNL is the deviation of each step from its ideal step size T_{LSB}. The calculation is given as

$$DNL_i = T_i - T_{LSB} = \frac{d_{i+1} - d_i - T_{LSB}}{T_{LSB}}, i = 0 \cdots (N-1) \tag{2.4}$$

Where DNL_i is the i[th] value of the differential nonlinearity, T_i is the width of the i[th] step in the real transfer curve, and d_i is measured cumulative delay from the original.

The INL is the absolute deviation of the step position from its ideal value normalized to one T_{LSB}. It can be calculated as

$$INL_i = \sum_{n=0}^{i-1} DNL_i = \frac{d_i - O_{delay} - i \cdot T_{LSB}}{T_{LSB}}, i = 0 \cdots (N-1) \tag{2.5}$$

where O_{delay} is the offset error, the vertical intercept of the line to which the transfer function is compared in the INL calculation. INL is also cumulative sum of DNL.

Figure 2.5 illustrates the effect of these metrics on the transfer function.

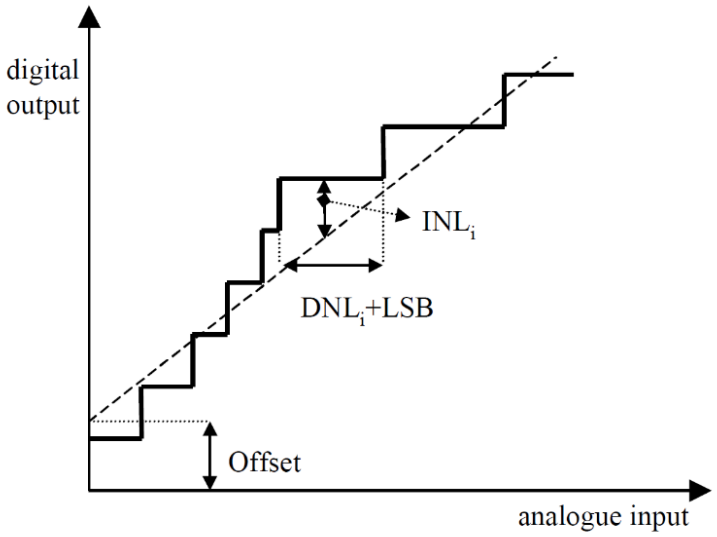

Figure 2.5. Nonlinearity example

2.3.5 Conversion time

The conversion time is the time required to compute the measurement value after a start event is captured, as shown in Figure 2.6. It evaluates the speed of signal processing and device delay at each conversion time window and hence is very important for high-speed applications.

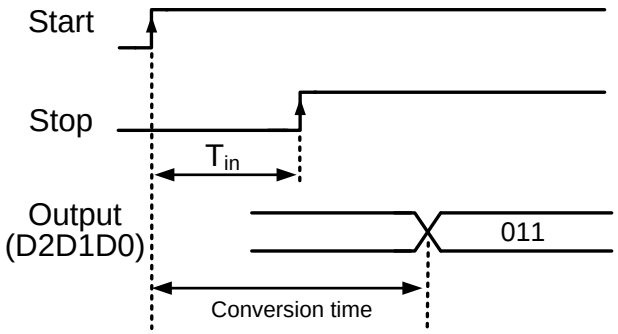

Figure 2.6. Conversion time example

2.3.6 Error Sources

The error sources include quantization error (or quantization noise), jitter (or reference phase noise) and some other noise sources.

The quantization error is an additive noise in the conversion result. It's a random variable distributed uniformly between $-\frac{LSB}{2}$ and $\frac{LSB}{2}$. It's proportional to the T_{LSB}. The standard deviation is given as

$$\sigma_q = \frac{T_{LSB}}{\sqrt{12}} \tag{2.6}$$

The jitter is the reference phase noise of the periodic reference signal in the context of the TDC. Other noise sources include thermal noise, which is a temperature dependent noise, flicker noise (or 1/f noise), which is the quality of the conductive medium with respect to the direct current flow, etc.

2.3.7 Power dissipation

There is static power and dynamic power dissipation. The static power is the leakage power, product of static leakage current and the power supply voltage.

$$P_{static} = V_{dd} \cdot I_{static} \tag{2.7}$$

where V_{dd} is the power supply voltage and I_{static} is the total static current. The leakage current components include the junction leakage, the sub-threshold current, the gate-induced drain leakage and the gate oxide leakage, etc.

The dynamic power includes the dynamic switching power and the dynamic short circuit power. The dynamic switching power is dissipated when charging or discharging internal and net capacitances. It's determined by the effective capacitor, the power supply voltage and the clock frequency.

$$P_{switching} = \alpha C_{eff} \cdot V_{dd}^2 \cdot f \tag{2.8}$$

where α is the active factor, $0 < \alpha < 1$, C_{eff} is the effective switched capacitance, and f is the clock frequency.

The dynamic short circuit power is caused by a direct current between power supply V_{dd} and GND during rising and falling slopes.

$$P_{short-circuit} = I_{sc} \cdot V_{dd} \cdot f \tag{2.9}$$

where I_{SC} is the short-circuit current during switching.

CHAPTER 3

TDC ARCHITECTURES REVIEW

Researchers have explored TDC architectures for more than 30 years. Many types of TDCs have been developed and utilized.

According to the development of TDCs, we can divide the TDCs into several generations [1]. The first generation is the analog TDC, basically implementing the current-integration techniques. The second generation is the digital TDC that can achieve the resolution of the gate delays, normally under 100 ps, including the counter-based TDC [3], and the flash TDC [4]. The third generation is the sub-gate delay TDC, achieving smaller time steps by using delay-line based [5], PLL based and DLL based techniques [6]. Nowadays the sub-picosecond TDCs, which is the fourth generation, are well developed in the multi-level interpolation with hybrid architectures utilizing techniques including time stretching [7], Vernier differences [8, 9], cyclic TDC using pulse-shrinking delay line [10], gated-ring-oscillator TDCs [11], time amplifying [12], successive approximation [13], Delta-Sigma [15], time interpolation using passive RC delay lines [16], *etc*.

The TDCs can also be categorized into the following four main categories according to the architectures and techniques.

3.1 Current-Integration TDC

The current-integration TDC, also call ramp TDC, is the main technique for the first generation

TDCs. It consists of a time-to-amplitude converter (TAC) and a high-resolution high-speed analog-to-digital converter (ADC), as shown in Figure 3.1. The TAC is implemented by a charge-pump and a capacitor [1]. The capacitor is charged by a fixed current for the time interval to be measured. The constant current causes the voltage on the capacitor to increase linearly with time. The voltage on the capacitor is directly proportional to the time interval and can be measured with an ADC and converted to digital codes. Between measurements the capacitor voltage is reset to zero.

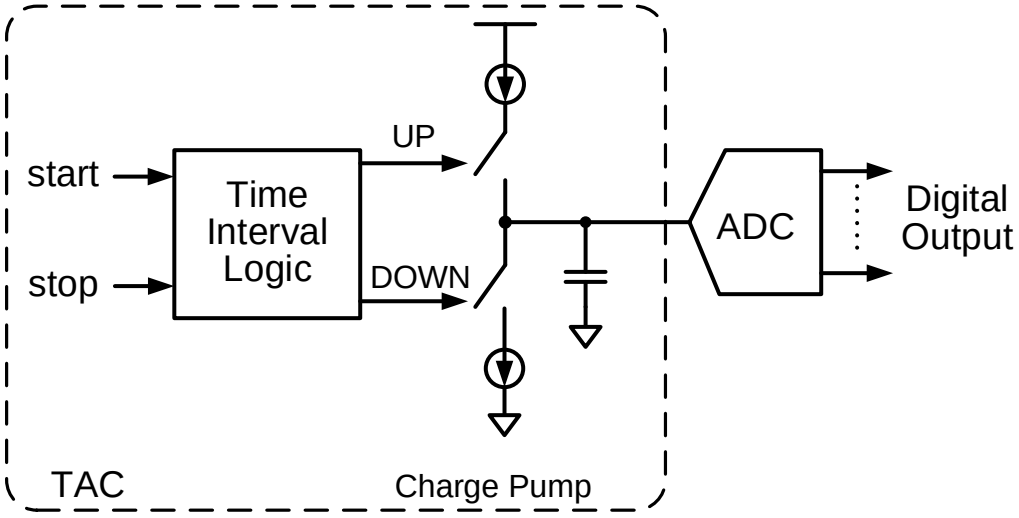

Figure 3.1. Current-integration TDC

Further development resulted in the dual slope TDC by using another constant current to discharge the capacitor in a much slower rate (usually 1/100 to 1/10000) and to stretch the time interval. The charging ramp (or fast ramp) and the discharging ramp (slow ramp) alternate to achieve smaller resolution.

The performance of the TDC mainly depends on the integrated resolution and ADC resolution. Also, since the TAC and the ADC are mainly analog components, the TDC is not scalable with technology, and consumes large static power.

3.2 Counter-Based TDC

The counter-based TDC is the simplest technique to quantize a time interval. The measured time defined by the start and stop signal is completely asynchronous to the reference clock signal. By counting the cycles of a reference clock, the measured time is equal to the multiplication of the counted number and the clock period. Counter-based TDCs achieve large dynamic measured range, yet limited resolution. Also, it's sensitive to the metastability in the counter's registers, usually flip-flops.

The frequency and stability of the reference clock determine the resolution and accuracy. By using a higher clock frequency, the measurement accuracy can be increased, albeit causing the power consumption to increase too. Hence the counter scheme is normally combined with interpolators to get higher resolution while maintaining lower power consumption. Digital delay lines can be used as interpolators.

A combination of a counter and interpolation has been proposed for a large linear dynamic range and high resolution TDC (Nutt 1968, Kalisz 2004). The counter keeps track of the full clock cycles

elapsed since the arrival of the start pulse. The counter is either halted with the stop pulse or the stop pulse stores the state of the counter.

3.3 Delay Line-Based TDC

In general, a delay line contains a certain number (normally 2^n for *n*-bit) of delay elements with stage delay τ. As shown in Figure 3.2, the start signal is synchronized to the rising edge of the reference clock and propagates through this line. The state of the line is sampled upon the arrival of the stop signal and stored to registers. The resolution will be defined by the stage delay of the delay cells. Now the time interval between start and stop signal is proportional to the number of flip-flops that were sampled as transparent. Normally the output is a thermometer code that locates the relative time interval and will be converted to a binary code.

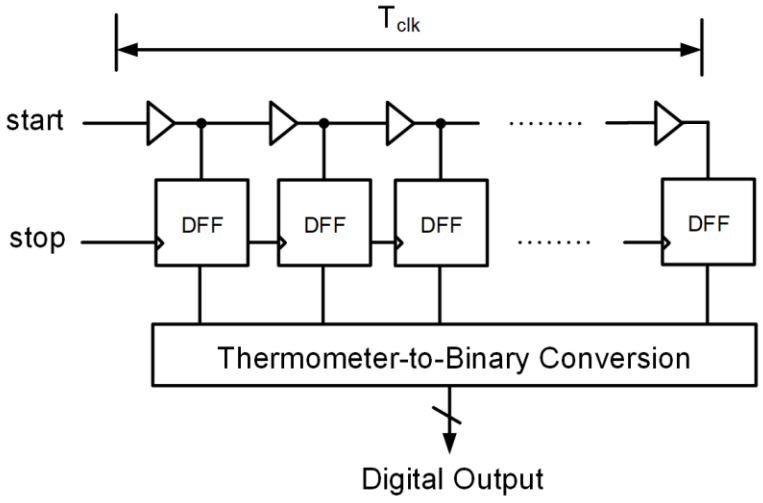

Figure 3.2. Delay line-based TDC

The delay lines can be implemented with several possible delay elements, including inverters, buffers or differential delay cells. Buffer cells generate more stable stage delays since they respect the start signal polarity. Differential cells can achieve smaller delay but may result in higher static power dissipation. The delay of a CMOS gate is highly dependent on the process, temperature and supply voltage, therefore requiring frequent calibration. Also, a very long delay line can be used to achieve large dynamic ranges.

The linearity of the conversion transfer function is determined by the matching of the delay cells. The random variations caused by the device mismatch results in differential nonlinearity (DNL). As the signal propagates along the delay line, this nonlinearity accumulates as integral nonlinearity (INL).

3.4 PLL-Based TDC

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of a reference clock signal. It's composed of a phase-frequency detector, a charge pump, and a low pass filter followed by a voltage controlled ring oscillator (VCO), whose oscillation frequency is controlled by a feedback loop, as shown in Figure 3.3. The phase of a periodic signal generated by the VCO will be compared with the phase of the reference clock signal. The VCO will be adjusted to keep the phases matched by controlling the delay.

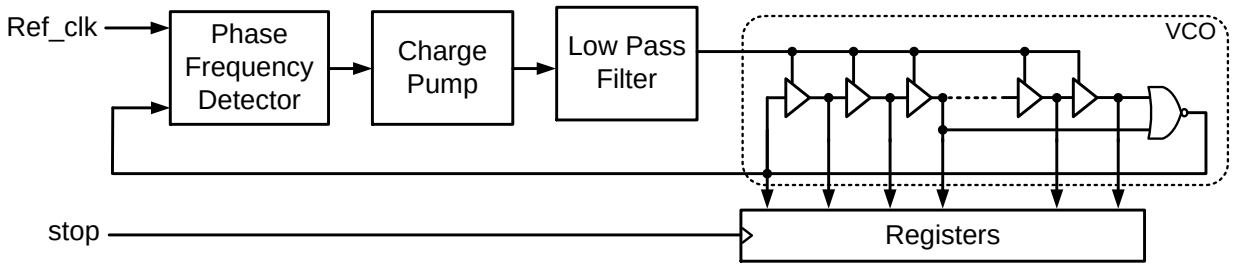

Figure 3.3. Phase-locked loop (PLL) circuit

Since the VCO is included in a closed loop, the PLL-based TDC guarantees self-calibration and low sensitivity to environmental changes and process variations. The conversion linearity is limited by the delay cell mismatch, like in other delay line based TDCs. Also, it can filter out phase noise (jitter) associated with the reference clock. But phase noise generated within the VCO is accumulated between oscillator periods, leading to increased output jitter.

3.5 DLL-Based TDC

A delay-locked loop (DLL) is a digital circuit similar to a PLL, with the VCO replaced by a voltage control delay line (VCDL). As shown in Figure 3.4, the reference clock signal is injected directly into the VCDL and its phase will be compared with the delay line output phase by the phase detector.

A DLL also has the ability to generate precise stage delays with high resolution, has self-calibration and can achieve large dynamic ranges. Also, the jitter does not accumulate in a DLL since the jitter event gets transferred to the output delay line only once. But it is not capable to filter jitter coupled

to the reference signal. Therefore, the time critical paths should be designed to be noise insensitive and the reference clock must be stable.

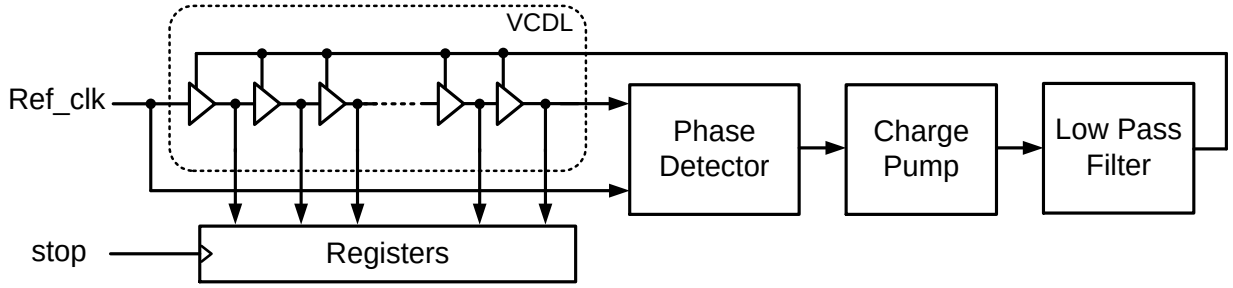

Figure 3.4. Delay-locked loop (DLL) circuit

3.6 Time Interpolation Using Passive RC Delay Line

One of the variations of the delay line-based TDC would be using a resistor-capacitor (RC) delay line. The delay time is dependent on the product of the parasitic resistance and capacitance and may vary due to process variations. But they are insensitive to the supply voltage and temperature variations.

A TDC architecture using a DLL and a passive RC delay line is used in [16] to overcome the limitation of limited dynamic range, as shown in Figure 3.5. With the DLL, it's self-calibrated on-the-fly. In the meantime, it performs a start-up calibration using code density test (CDT) to characterize the RC delay line.

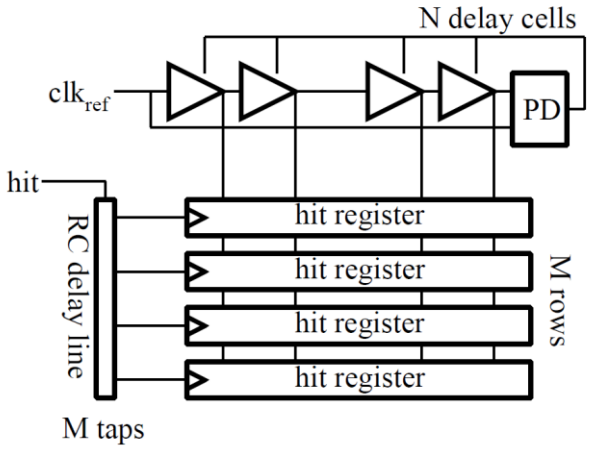

Figure 3.5. A TDC based on a DLL and an RC delay line

3.7 TDCs with Hybrid Architecture to Implement 2-3 Level Interpolation

Nowadays, hybrid TDC architectures are used more frequently to satisfy the demand for better performance. The specific needs of different applications will raise the demand for different hybrid architectures. Some use time interpolation combined with other sampling techniques to obtain high precision. Some use counter-based TDCs to achieve wide measured range.

One of the most popular architectures is the combination of the counter-based TDC with time interpolation by a DLL to get both wide measured range and high resolution. The multi-phase sampling with a Vernier delay line is also popular to achieve high resolution. Also, time amplification is often used to obtain sub-picosecond resolution.

CHAPTER 4

PROPOSED TDC[1]

This dissertation presents a new type of TDC based on an RC delay line that offers low power consumption, high speed and high resolution with error-correction circuitry. Using mostly all-digital components, this TDC will scale with future technologies. Without any analog components like the DLL, the TDC can achieve very low power consumption, and is hence applicable for TDCs requiring low power, such as portable medical equipment.

4.1 Architecture

A two-level interpolating time-to-digital converter (TDC) using a coarse-fine architecture is used to implement high-precision time interval measurement. Figure 4.1 shows the basic concept of the proposed TDC. The *start* and *stop* signal are fed into the dynamic buffer delay-line which provides the most significant 7b of resolution. The generated signals go through the time residue generator, indicating the resulting delay residue, and this is propagated along the second level RC-chain, providing the last 7b of resolution. Finally, the digital code is corrected employing LUT-based calibration.

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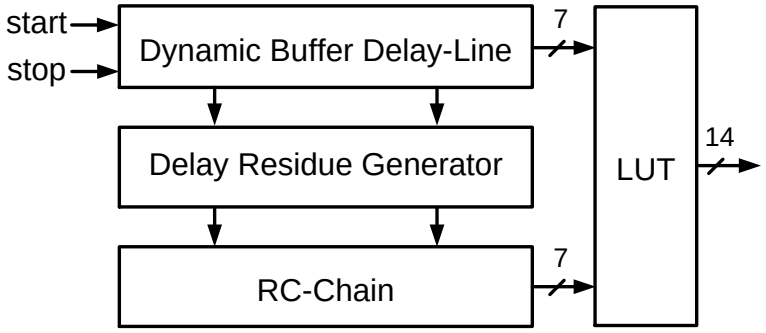


Figure 4.1. Proposed TDC block diagram

4.2 First Level: Dynamic Buffer Delay-Line

Figure 4.2 shows the gate level circuit schematic of the coarse delay-line consisting of the dynamic buffer elements, the MUTEX and the DFFs. The proposed TDC employs a 160-stage buffer chain as the coarse delay line and guarantees 7-bit resolution over ± 25% variation. Nominally, a 7b resolution requires a minimum of 128 buffer stages. However, anticipating PVT (process, voltage and temperature) variations, we allow for a variable start position (the stage in the buffer chain corresponding to zero delay) and a variable stop position (corresponding to the maximum time delay to be measured). Therefore, a total of 160 stages are provided.

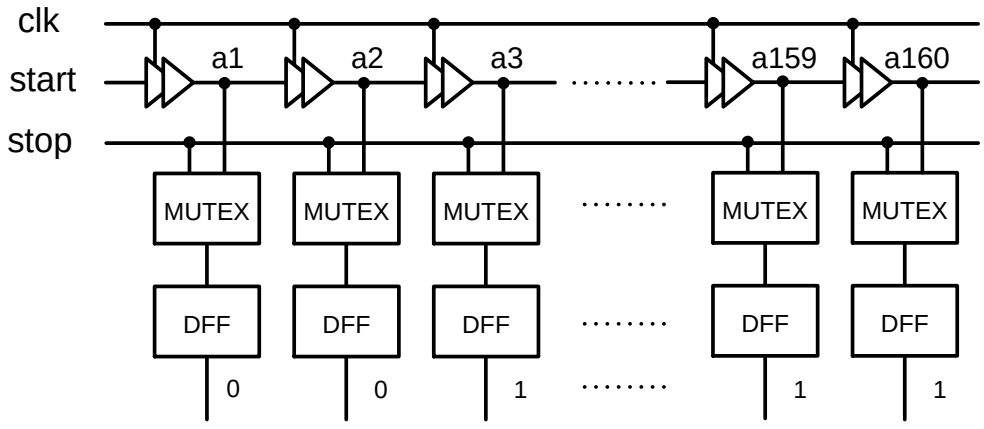


Figure 4.2. Dynamic buffer delay-line basic structure.

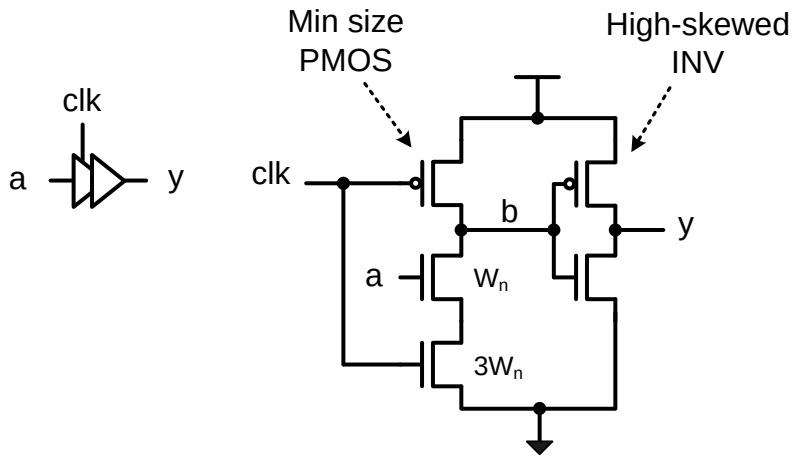


Figure 4.3. The dynamic buffer schematic.

The delay elements of the coarse delay-line are designed to be dynamic buffers, which is a dynamic inverter followed by a static high-skew inverter, as shown in Figure 4.3. The dynamic inverter contains a minimum size PMOS transistor controlled by a clock signal and an NMOS transistor sized W_n as the pull-down logic, in series with another NMOS transistor sized $3W_n$ as the footer or evaluation device. When the clock signal is low, the output is reset to zero. When the clock signal rises, the buffer evaluates its input. Figure 4.4 shows the waveforms for a single dynamic buffer. Once the *start* signal propagates to a certain buffer, the corresponding output rises with a sharp edge and propagates to the next stage. The waveforms of 12 neighboring dynamic buffers are shown in Figure 4.5. Using a 1.3V power supply, this buffer-chain achieves a nominal stage delay of 10ps for the 45nm process.

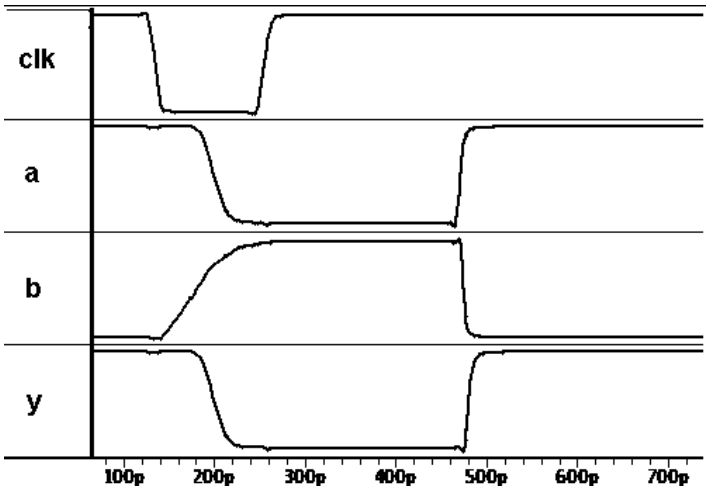


Figure 4.4. Waveforms for a single dynamic buffer.

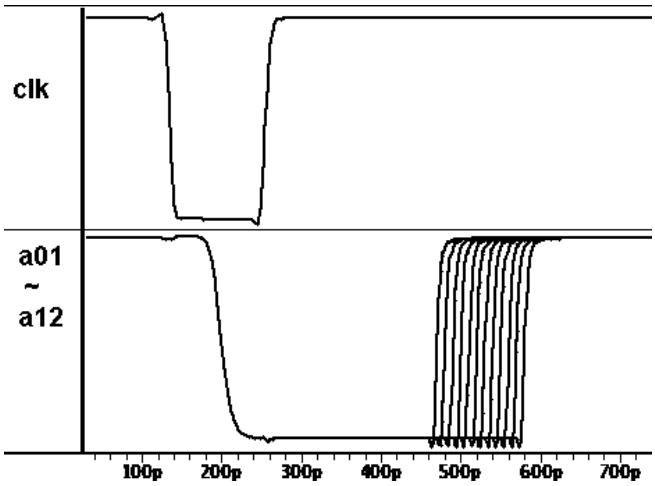


Figure 4.5. Waveforms of 12 neighboring dynamic buffers.

A MUTEX circuit is used to detect the position of the propagating start signal rising edge upon receiving the stop signal. A MUTEX circuit is an arbiter to determine which signal of the two inputs arrives first. As shown in Figure 4.6, it consists of two NAND2 gates, whose outputs are connected to two cross-coupled inverters. The output goes high if *a* rises before *b*, otherwise the output stays low.

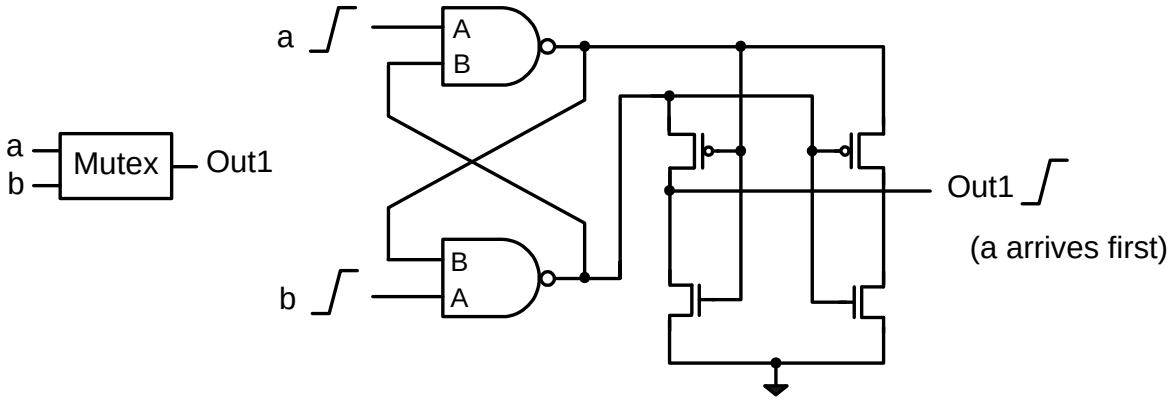


Figure 4.6. MUTEX circuit

The MUTEX array generates a thermometer code, which is a series of 0's followed by a series of 1's. D flip-flops (DFFs) are used to sample and store the outputs of the MUTEX circuits. The propagating *start* signal goes through the dynamic buffer delay line and are buffered through a driving buffer before being fed to the MUTEX. This also generates a clock signal stage by stage through a large delay buffer with a long delay to ensure the proper setup and hold time for the DFFs. The *stop* signal goes through an identical driving buffer before being fed to the MUTEX for matching delays. After the proper logic, as shown in Figure 4.7, a series of AND2 gates with one inverted input will transform the thermometer code to a one-hot code and the result will be converted to a binary code. This encoder generates a 7b binary value.

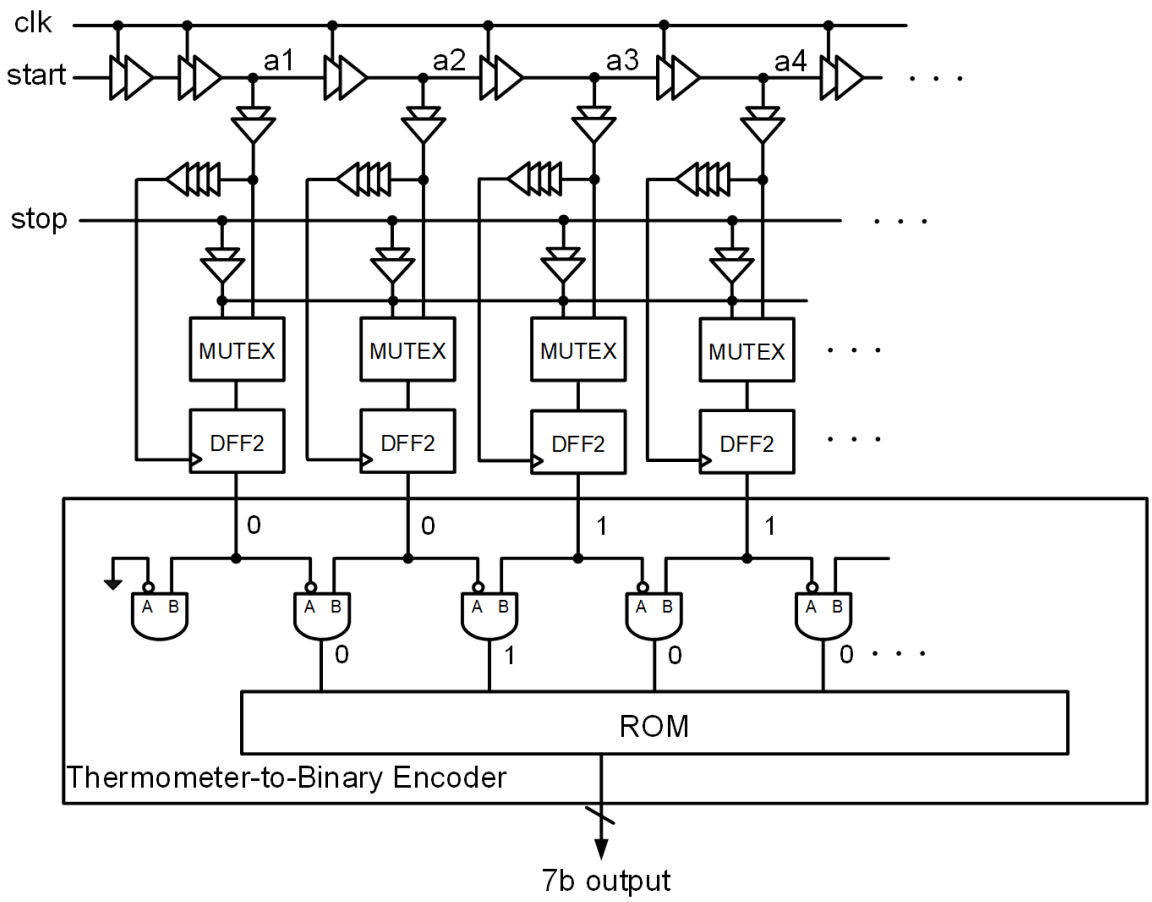


Figure 4.7. Data captured and encoding circuit.

4.3 Delay Residue Generator

The MUTEX chain generates a series of 0's followed by a series of 1's, for example, 0001111, indicating that the "0" to "1" transition point is the position along the buffer chain where the *stop* signal catches the *start* signal. The subsequent DFF, AND and OR gates generate a rising signal *Rstart*. By using an identical logic block fed by the *stop* signal acting as dummy logic, we generate another rising signal *Rstop*, whose difference with *Rstart* is the delay residue we are seeking, as

illustrated in Figure 4.8.

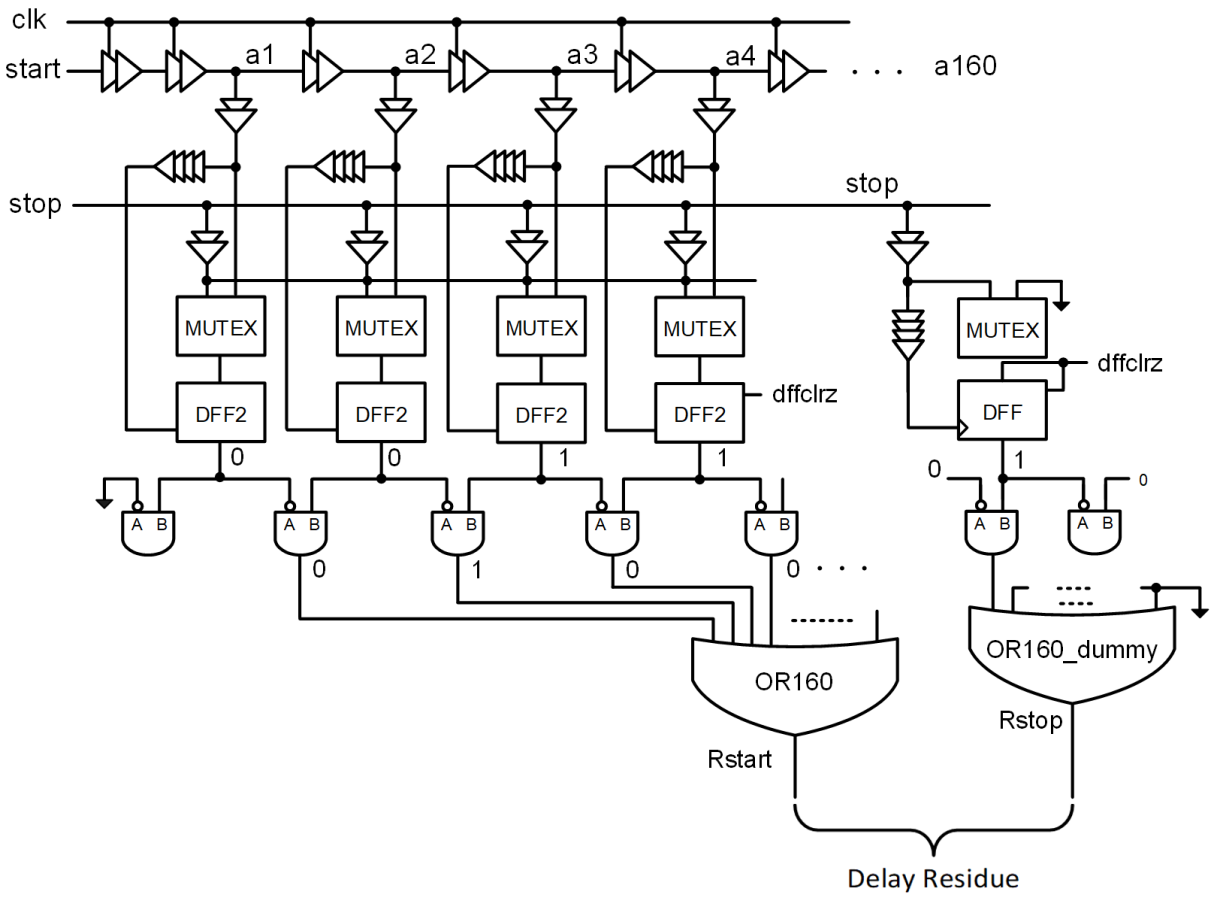


Figure 4.8. The delay residue generation circuit.

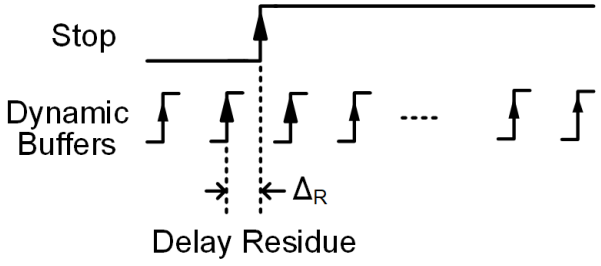


Figure 4.9. Timing diagram for delay residue

The waveforms of the rising signals are shown in Figure 4.9. The difference denoted as Δ_R will be transmitted through the delay residue calibration logic to the second level RC chain for finer step interpolation.

The OR160 in Figure 4.8 is a specially designed dynamic OR gate with 160 inputs. Based on the derivation from the De Morgan's law we can implement OR160 in the way shown in Figure 4.10. Eight 20-input NOR gates with each pair connected to a NAND2 gate, then go through the NOR2 and NAND2 again.

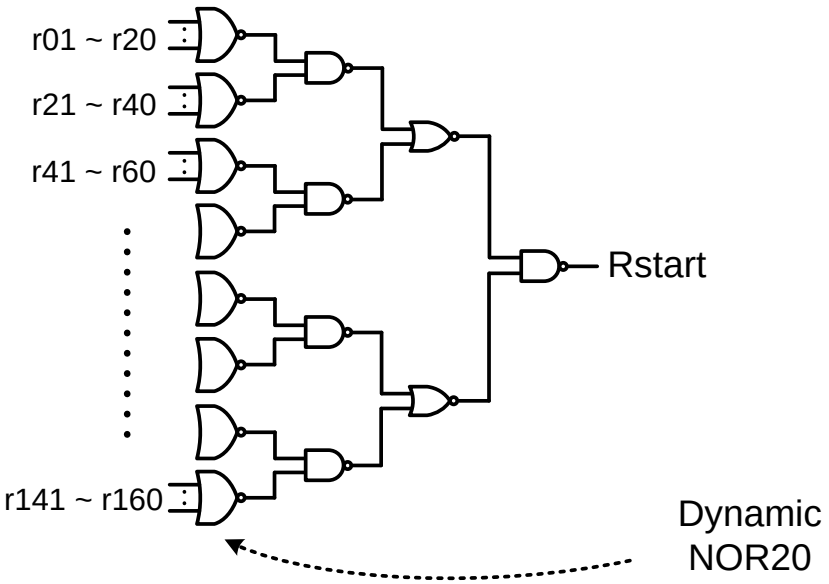


Figure 4.10. OR160 gate in delay residue calibration circuit

The dummy gate of the OR160 is shown in Figure 4.11.

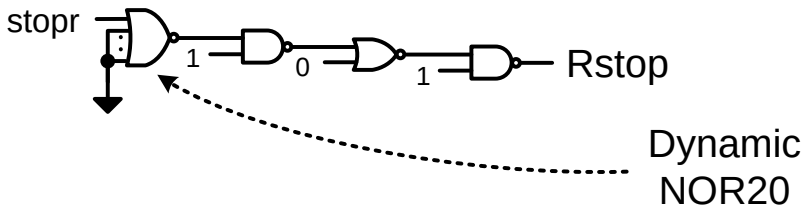


Figure 4.11. OR160_dummy gate in delay residue calibration circuit

The dynamic NOR20 is a clocked dynamic gate with 20 inputs, as shown in Figure 4.12. The pull up network is composed of one PMOS transistor controlled by the clock signal and a half keeper (the inverter and the other PMOS transistor). The pull-down network is twenty minimum size NMOS transistors in parallel. When clock signal is low, the output *y* is charged up to VDD and the half keeper helps to reinforce the output. When the clock signal is high, the gate starts to evaluate the inputs. If there is an input that is high, the output will discharge to zero. The output will be a "1" only when all the inputs are low.

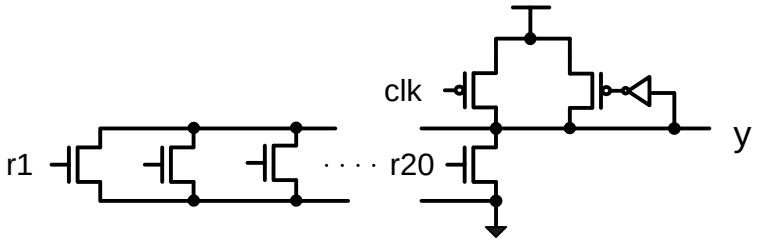


Figure 4.12. Dynamic NOR20 gate used in OR160 and OR160_dummy

To improve the accuracy of the delay residue, we use specific calibration logic between the above circuit and the 2nd level delay chain. The logic is shown in Figure 4.13 and Figure 4.14.

There are four voltage-controlled offset buffers, two in each signal path, with one before and one

after the mode-switching MUXs. The voltage-controlled offset buffer contains four static inverters in series, along with a controllable power supply to tune the delays, as shown in Figure 4.13.

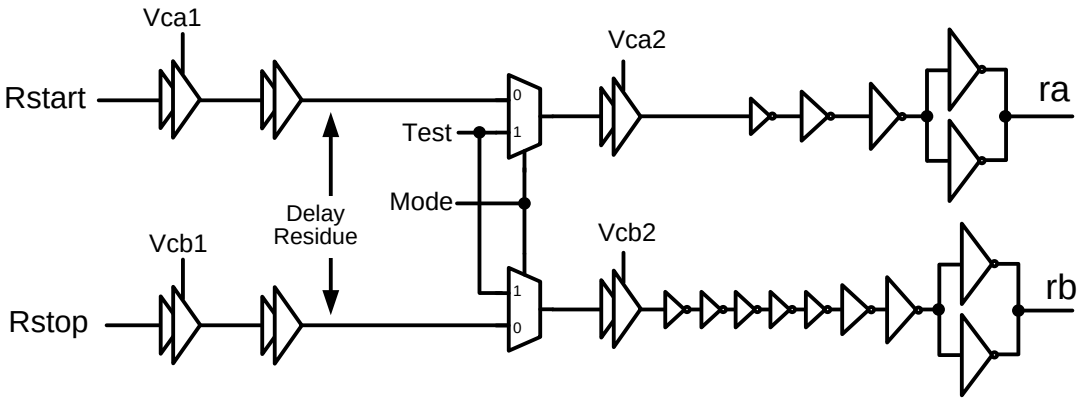
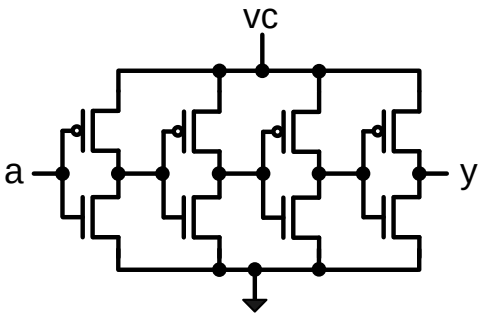


Figure 4.13. The calibration logic for time reisude generation



vc (V)	delay (ps)
1.0	44
1.1	37.4
1.2	33
1.3	29.5

Figure 4.14. The voltage control offset buffer

The delay of the offset buffer varies from 44 ps to 29 ps when the power supply varies from 1.0 V to 1.3 V, as shown in Figure 4.14. We ensured that the tuning range exceeds the resolution of the dynamic buffer delay line, which is 10 ps. By tuning the power supply of one or more offset buffers, we can tune the propagation delay of each path and thus compensate for the delay

mismatches from the previous dynamic buffer chain and from the MUXs to maintain an accurate delay residue and setup time for the second level delay line.

The MUXs are switched between test mode and the normal operating mode. This test mode can be performed along with the start-up calibration and calibrate the circuit into its ultimate matching capability. A series of buffers follows each MUX and offset buffer. With the increasing sizes of these buffers, they have enough drive for the next block, the 120-stage RC chain. The *Rstop* signal path has four more inverters than the *Rstart* signal path to compensate for the DFF setup time of the next level.

4.4 Second Level: RC Chain Fine Delay-Line

The second level of the TDC concatenates a series of wire segments into a long chain. Each segment serves as an RC delay element. Thus, the stage delays along the chain will be related to the RC delays of the wire segments.

The nominal wire resistance is determined by the sheet resistance and the number of squares that each wire segment contains. Also, the wire capacitance per unit length is determined by the capacitance to the adjacent layers and to the layers above and below. To estimate the wire segment delay, distributed RC network theory needs to be applied [20]. By using the same type of material, the delay is proportional to RC, hence proportional to the wire length and width.

The wire segments connect to identical buffers to drive D flip-flops. From the analysis of the RC delay model, we know that in stage *i*, the effective capacitance is related to capacitance of the *i*-th stage as well as the capacitance of the subsequent stages. Hence the effective capacitance grows smaller and smaller from the first stage to the last stage. To keep the RC product constant for each stage, it is necessary that the resistance of each stage increases. The first stage has the smallest resistance, and the last stage has the largest. Also, since the distance between each stage is constant, the width of the wire segments must decrease so as to increase the resistance. Figure 4.15 shows the simulated resistance distribution. In the actual layout the wire segment length is fixed by the RC chain stage cell width, 2180 nm in our case.

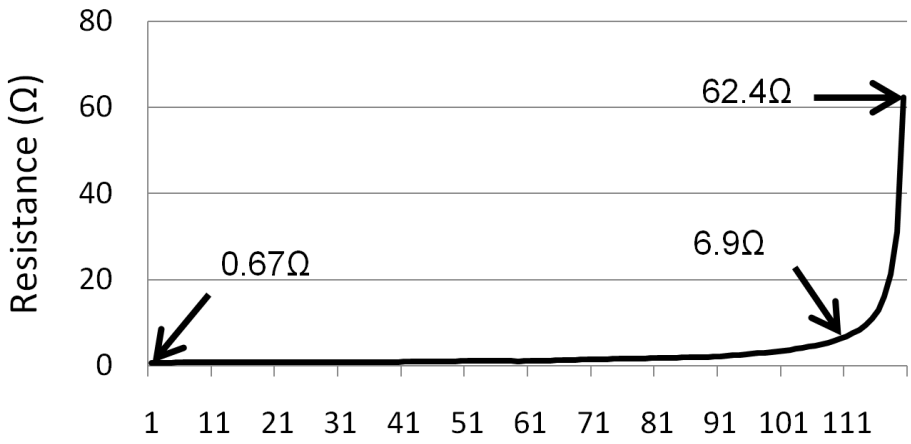


Figure 4.15. RC chain simulated resistance distribution.

Figure 4.16 shows the metal width of the first 108 segments which have a fixed wire length of 2180 nm. Segment number 1 should have the smallest resistance, hence it has the least number of squares. So its wire width is the largest. For segment number 1 to 108 the wire width need to decrease for increasing number of squares to get increasing resistance, until the minumum width

of wire, 70 nm, is reached, which is happening in segment number 108. The segment number 109 to 120 have the fixed wire width of 70 nm. So they have to zigzag to achieve more number of squares for larger resistance. Figure 4.17 shows the metal length of the last 12 segments, each having a fixed wire width of 70 nm.

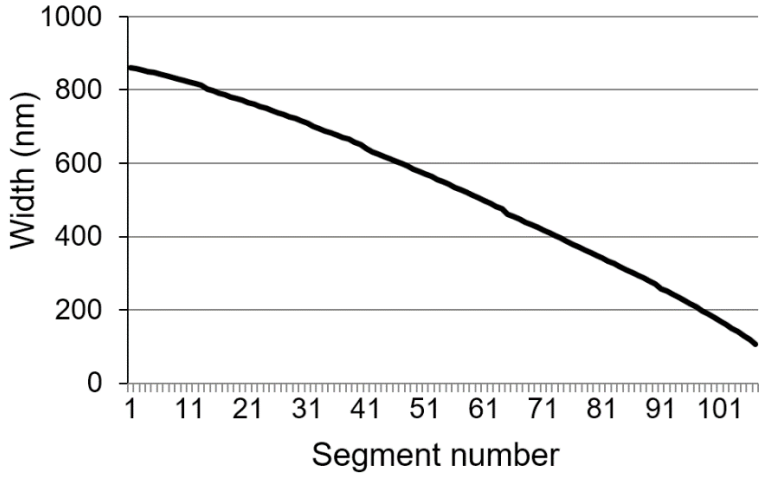


Figure 4.16. RC chain Metal1 layout sizes distribution, (a) metal wire width with a fixed wire length of 2180nm for segments 1 to 108.

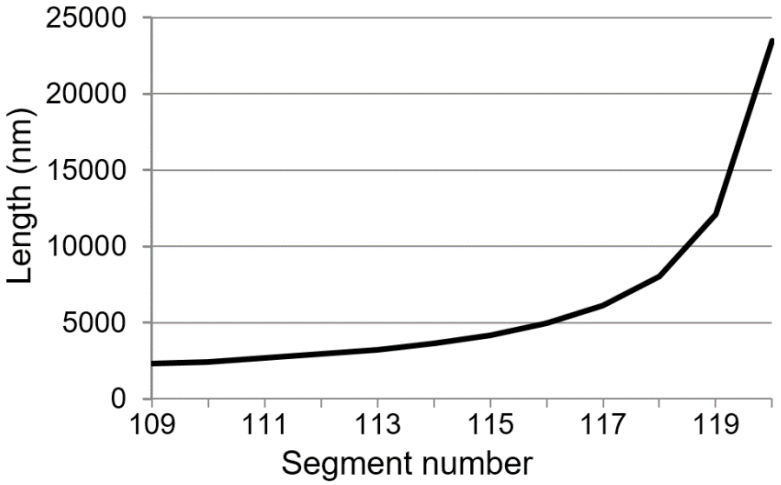


Figure 4.17. RC chain Metal1 layout sizes distribution, metal wire length with a fixed wire width of 70nm for segments 109 to 120.

Table 4.1. Sheet Resistance and Capacitance in 45 nm CMOS Metal RC Characteristics.

Layer	Sheet resistance (Ω/□)	Capacitance(fF/mm)
Metal1	0.527	0.196
Metal2	0.26	0.204
Metal3	0.26	0.204
Metal4	0.26	0.204
Metal5	0.26	0.204
Metal6	0.26	0.188
Poly	16	0.181

Table 4.1 shows some typical values of the metal wire sheet resistance and capacitance of the 45nm CMOS process used in this TDC. For simplicity and effectiveness, the metal1 layer was chosen to implement the wire segments.

As for PVT variations, the RC delay is largely insensitive to the supply voltage and temperature variations. The delay mismatch due to process variations is calibrated using a lookup table approach.

The difference between the *ra* and *rb* signals is the delay residue from the first level delay chain. Since the first level buffer chain resolution is 10ps, to achieve 0.1ps resolution we need at least 100 stages for the second level. To cover an anticipated 20% in PVT variations, we use 120 stages,

as shown in Figure 4.18. The signal *ra* propagates along the RC chain and will be caught by signal *rb* in a particular stage. This position indicates the time difference between the *ra* and *rb* signals plus the DFF setup time. By designing the buffers after the RC chain to compensate for the DFF setup time, and with the use of the lookup table, we can accurately measure the delay residue. The lookup table compensates for PVT variations causing the minimum delay (zero) to have a variable starting point in the chain and the maximum delay (10ps) to traverse a variable number of segments.

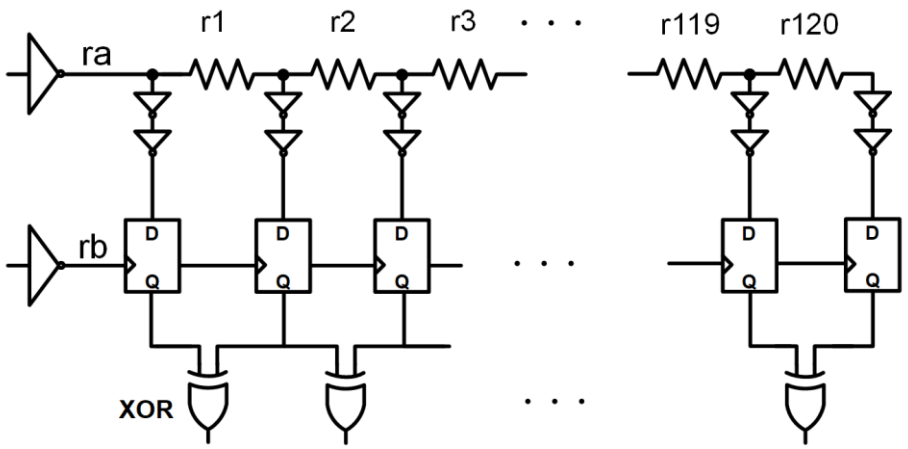


Figure 4.18. RC chain circuit schematic.

The buffers after each segment in the RC chain improve the shape of the waveforms, as shown in Figure 4.19. Before the buffers, the rising edges at each wire segment are distorted. After the buffers, the rising edges are nicely in parallel, thus providing consistent stage delays.

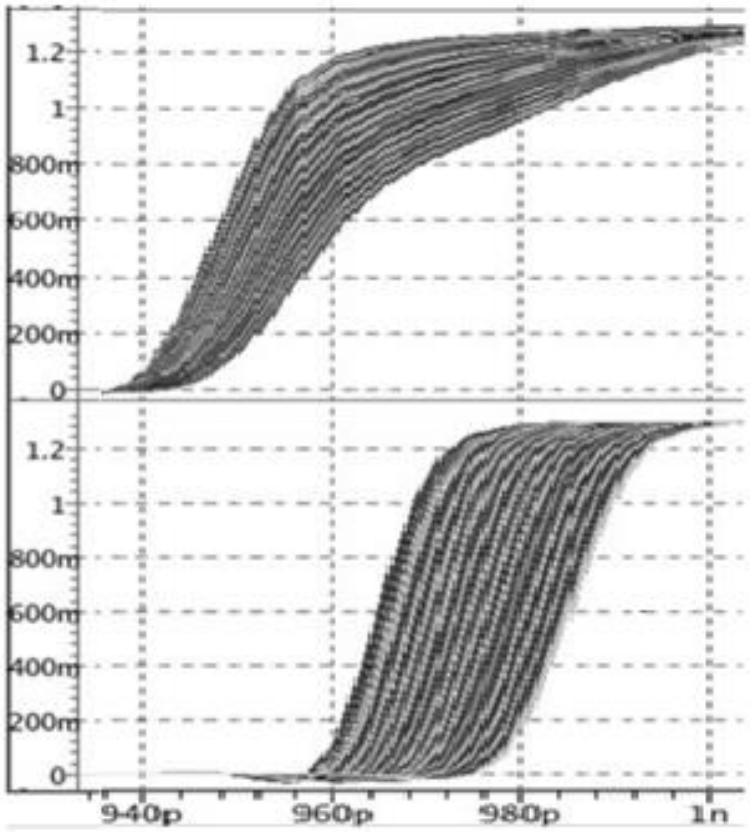


Figure 4.19. RC chain waveforms, before and after the buffers, with 0.1ps LSB.

In this design, we achieve 0.1 ps LSB with the 45 nm process. The “0” and “1” values captured by the DFFs from the RC chain go through XOR gates to generate the one-hot code and are converted to the last 7b digital code output using an encoder. Figure 4.20 shows the RC chain simulated stage delays based on layout with full parasitic extraction. The simulated delays are from 0.099 ps to 0.105 ps, which is -1% to +5% of the ideal delay.

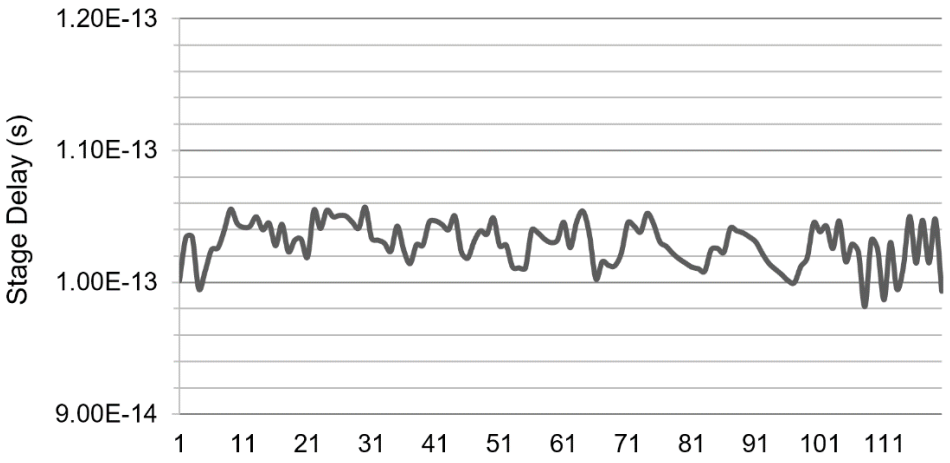


Figure 4.20. RC chain full parasitic extraction simulated stage delays.

4.5 Error Correction Circuitry: Look-Up Table (LUT) Based Calibration

We utilize a LUT-based correction technique to do the calibration. This design avoids the use of traditional calibration components in prior TDCs, such as VCOs, PLLs and DLLs, and hence reduces power consumption. The benefit of the LUT-based circuit includes not only the simpler circuitry, but also faster result settling and significant power savings. It also greatly improves the single-shot precision.

At circuit start up, a one-time calibration cycle is performed. We apply a ramp of time events over the full input dynamic range. For the LUT each address is the obtained measurement value and the stored value is the expected value. That is, after an actual measurement is taken, the corrected digital code from the LUT will be read out, thereby correcting for non-linearities due to PVT variations.

Normally an on-chip SRAM would be used for the LUT, but due to area limitations with this test chip, an off-chip SRAM was used.

CHAPTER 5

EXPERIMENTAL RESULTS [1]

5.1 Layout of the Prototype TDC

The prototype TDC was fabricated using the Texas Instruments 45 nm single-poly, seven-metal digital CMOS process. The layout is shown in Figure 5.1, and the photograph is shown in Figure 5.2. The actual core area of the TDC is 0.03 mm^2 (750 μm × 40 μm). The total area is 1×1 mm^2. including pads. This chip also includes two other unrelated designs. A total of 40 I/O pads are used.

As we can see in the TDC circuit expanded view in Figure 5.1, there are five main blocks in the TDC. The topmost block is the dynamic buffer delay-line, whose length is nearly the full width of the chip. The block below is the encoder for the dynamic buffer delay-line, marked as Encoder-Coarse. The two blocks side by side in the third layer are the delay residue generator and the RC-chain, respectively. The bottom one is the encoder for the RC-chain, marked as Encoder-Fine.

[1] ©2014 IEEE. Portions Adapted, with permission, from H. Huang, and C. Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS," IEEE, Circuits and Systems Conf. (DCAS), pp. 1-4, Oct. 2014.

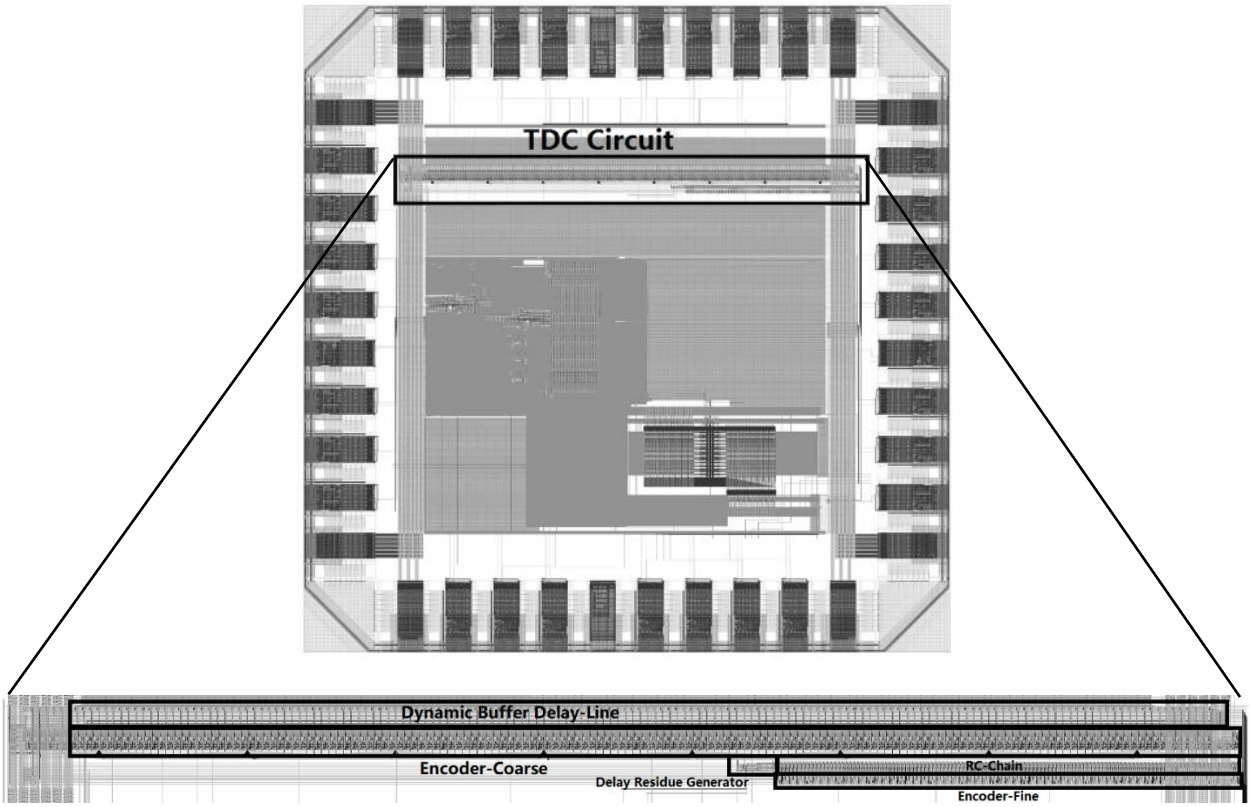


Figure 5.1. Layout and expanded view of the TDC prototype chip.

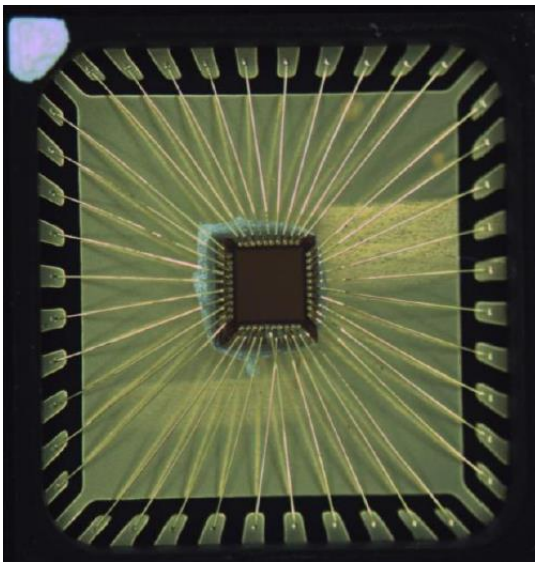


Figure 5.2. Photograph of the TDC prototype chip.

5.2 Measurement Setup

The chip was packaged using a 40 pin open top Quad Flat No Lead package (QFN). During the testing, a QFN socket was mounted using through holes to the printed circuit Board (PCB), as shown in Figure 5.3.

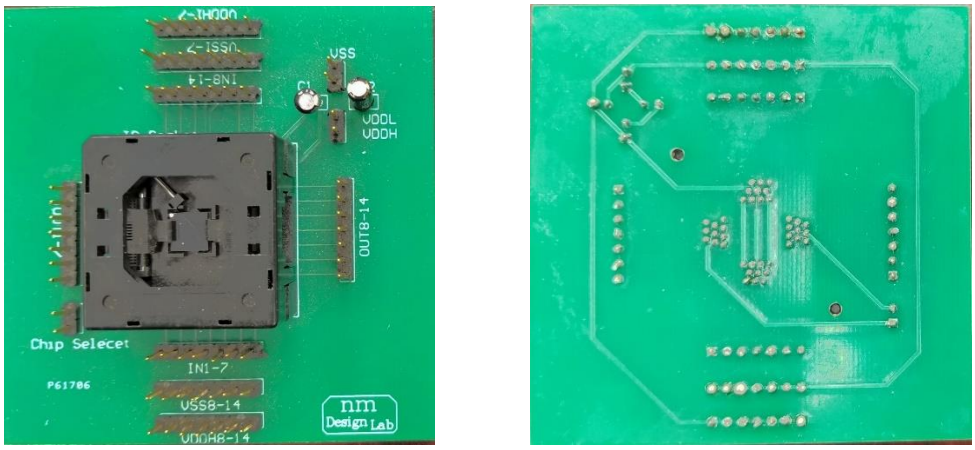


Figure 5.3. The PCB with a QFN socket.

The TDC was tested with the power supply of 1.3V and with reference clock frequency of 500 MHz. The main targets for the chip testing are to measure the key characteristic performance, including the differential nonlinearity and the integral nonlinearity, the precision and the power consumption.

As shown in Figure 5.4, the test setup consists of two signal generators, a logic analyzer, DC power supply and a PCB test board with the TDC chip. To measure the proposed TDC, a ramp of time intervals is generated by two 500 MHz signal tones with a 2.5 KHz frequency difference. The

input pulse ramp generated is 10 fs/cycle. A logic analyzer was used to collect the TDC outputs. The DC power supply is used to tune the delay residue generator.

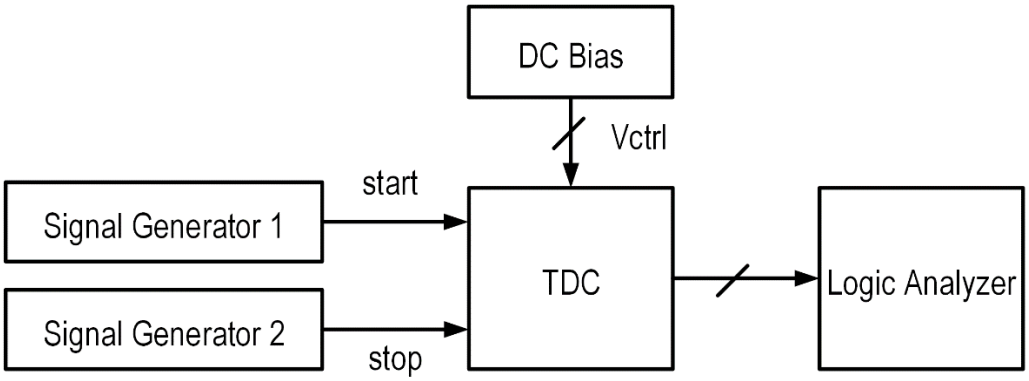


Figure 5.4. Test setup.

At circuit startup a calibration on the delay residue generator is implemented by tuning the control voltages on the voltage controlled offset buffers. Then an INL LUT was collected by making a full input range measurement, which is 160 ×120 = 192,000 time interval measurements. The data is exported and stored for future use.

5.3 Nonlinearity

A ramp histogram in ten times finer steps was used to test the TDC nonlinearity. Ten times of the total amount of the digital code were sampled. Figure 5.5 shows the nonlinearity of the TDC without LUT. The DNL is +0.40 /-0.30 LSB. The INL shows a downside ramp due to the PVT variations. The larger the INL indicates the larger deviation of the step position from its ideal

value. In Figure 5.5, it shows that without LUT the maximum INL is as large as 316.7 LSB. With the calibration by the look-up table (LUT), in Figure 5.6, we can see that the LUT-calibrated INL is greatly reduced to 1.25 LSB. DNL is affected by 0.1 LSB, which is acceptable.

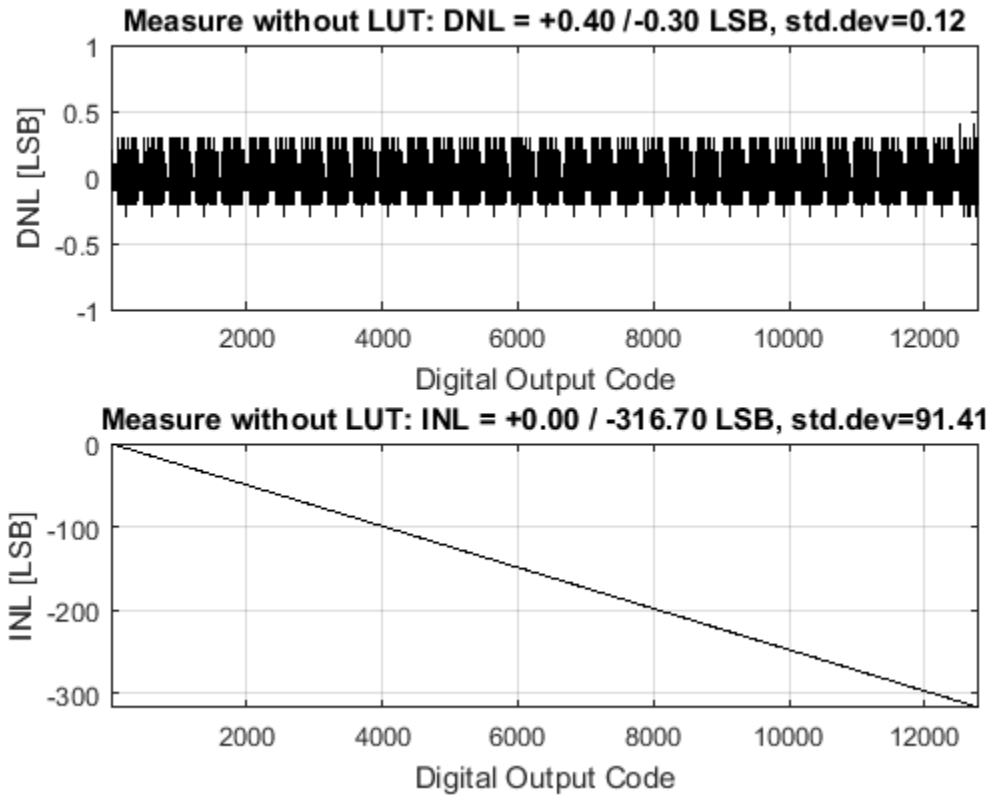


Figure 5.5. Measured nonlinearity, DNL and INL: without LUT.

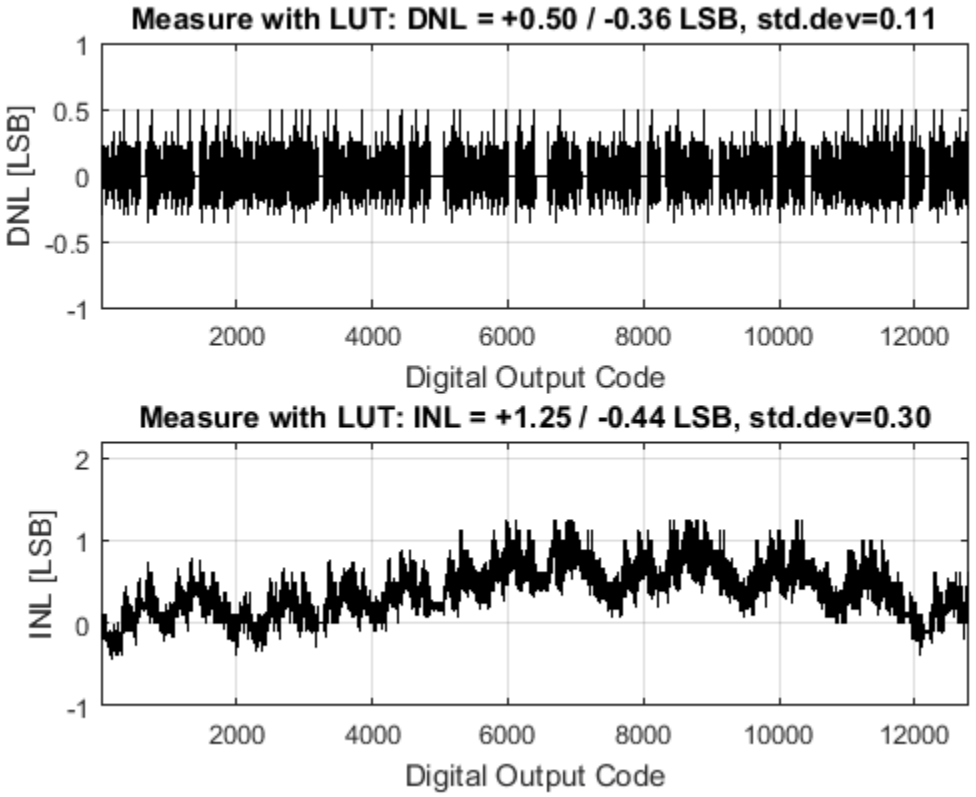


Figure 5.6. Measured nonlinearity, DNL and INL: with LUT.

5.4 Single-shot Precision

Since the jitter and non-linearities of the input signal generator are much larger than those of our TDC itself, the dominant error was because of the input signal generators. To measure the noise performance of the TDC, a single-shot precision test was performed by applying a constant time-difference input.

Single-shot precision is defined as the time interval resolving capability of a TDC [2, 13]. It's indicated by the standard deviation, σ, of the distribution of the measurement results around the mean value, when a constant time interval is measured repeatedly. It describes how reproducible a TDC measurement is in the presence of noise.

A single output pulse was taken from a pulse generator and split into two pulses with a power splitter. One pulse was fed directly into the TDC as the *start* signal. The other pulse was first delayed in a coaxial cable and then fed into the TDC as the *stop* signal. Thus, a constant and nearly jitter-free input time interval was created.

A large number of measurements of time intervals are needed to evaluate this measurement uncertainty. In this work, the constant time interval spanning from 10 ns to 12 ns, covering one full cycle of the measurement clock, are applied to the inputs many times to measure the single-shot precision. The time step is 100 ps. In each step a fixed time interval *Tin* is applied repeatedly to the TDC 11,500 times. Two examples of the measurement results, when *Tin* is 100 ps and when *Tin* is 1.2 ns are shown in Figure 5.7 to Figure 5.10.

When the input time interval is 100 ps, the single-shot σ value is 2.66 ps without the LUT, as shown in Figure 5.7. But with the LUT this value is reduced to 1.95 ps, as shown in Figure 5.8.

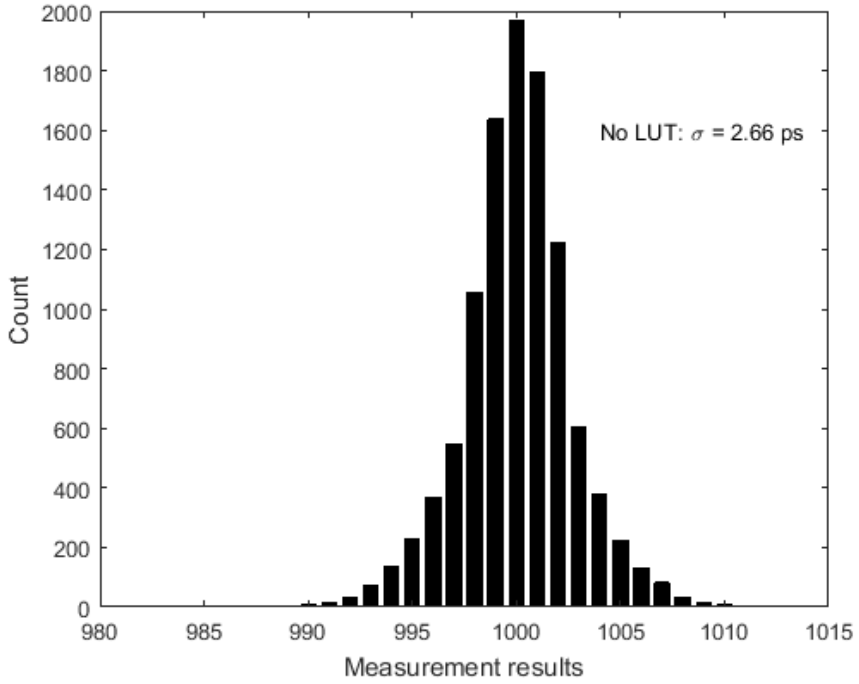


Figure 5.7. Measured single-shot precision when input time interval is 0.1 ns: without LUT.

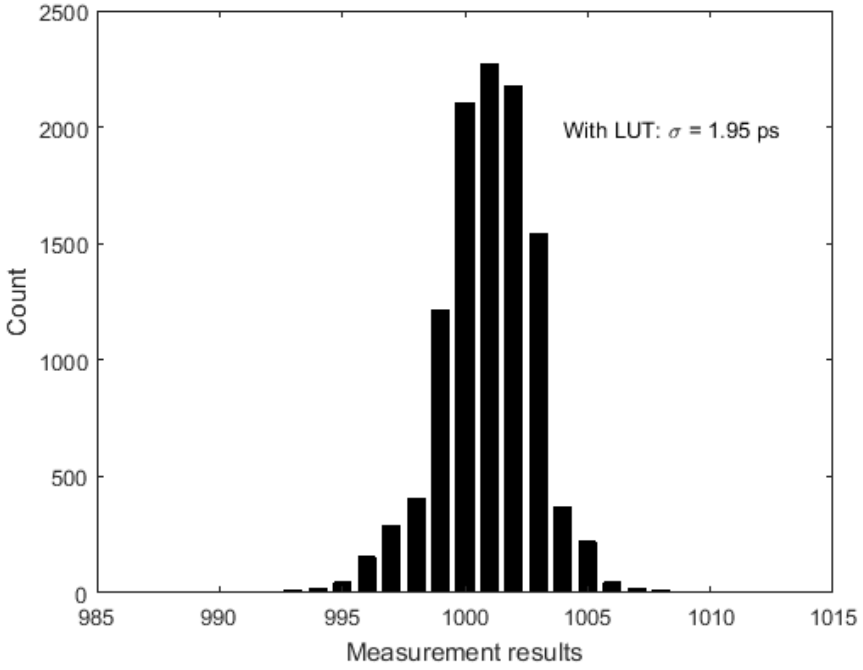


Figure 5.8. Measured single-shot precision when input time interval is 0.1 ns: with LUT.

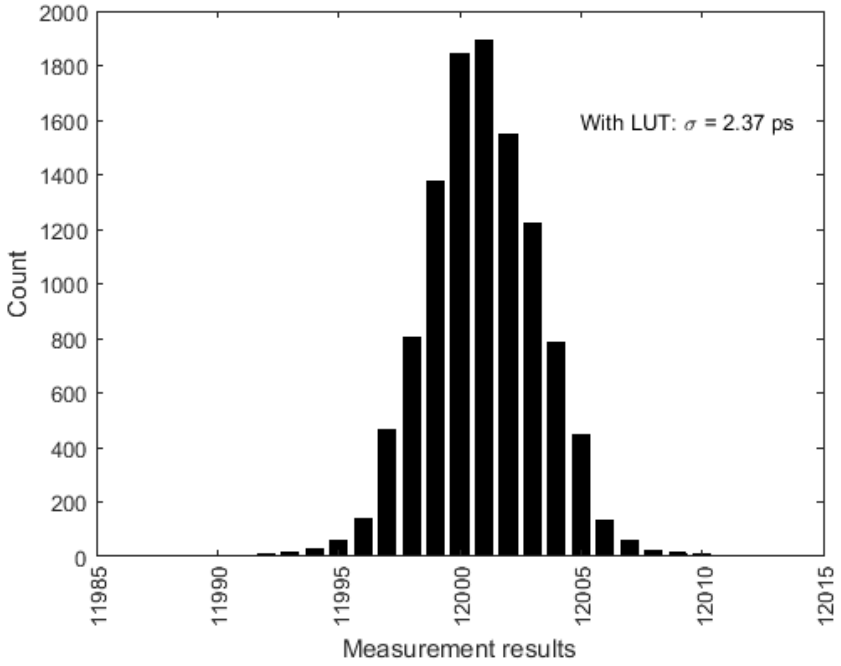


Figure 5.9. Measured single-shot precision when input time interval is 1.2 ns: without LUT.

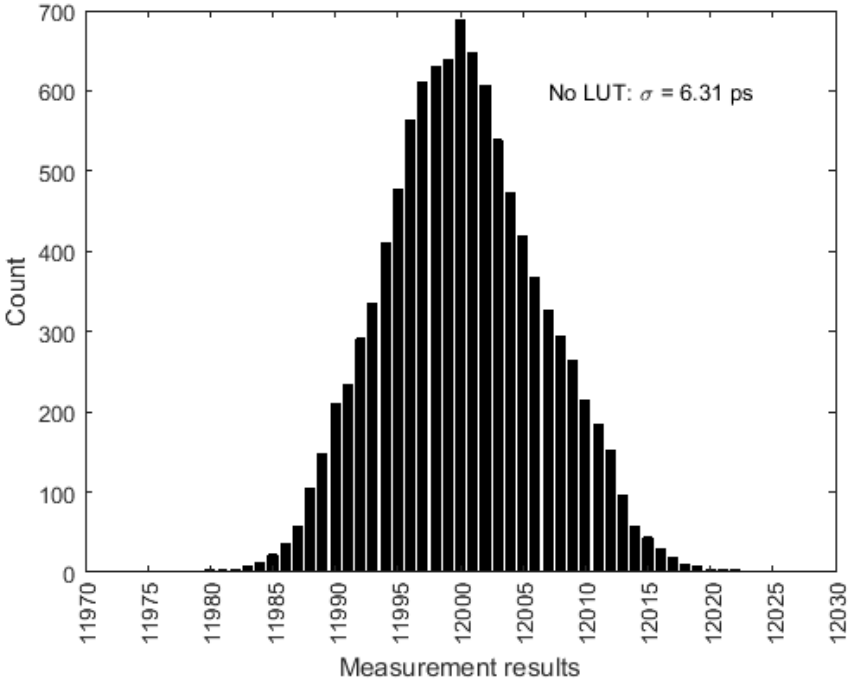


Figure 5.10. Measured single-shot precision when input time interval is 1.2 ns: with LUT

When the input time interval is 1.2 ns, the single-shot precision σ value is 6.31 ps without the LUT, as shown in Figure 5.9. With the LUT this value is reduced to 2.37 ps, as shown in Figure 5.10.

The single-shot precision σ behaves as a function of the input time intervals, as shown in Figure 5.11. The LUT helps minimize the single-shot precision, thus reducing the random measurement uncertainty.

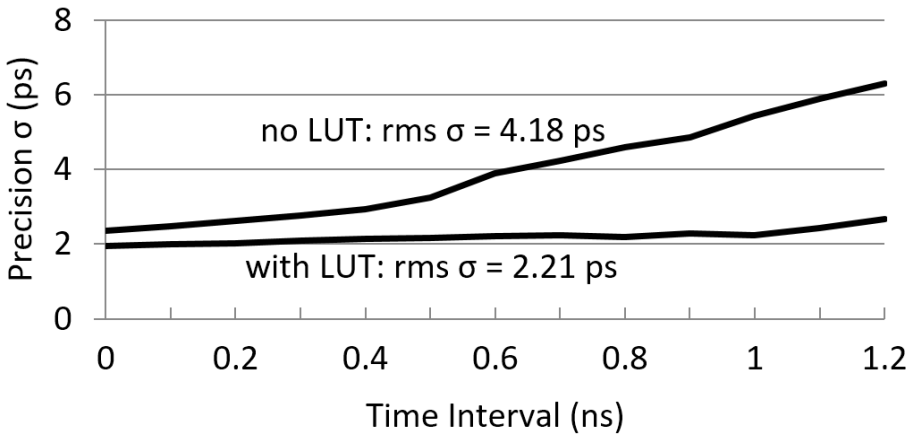


Figure 5.11. Measured single-shot precision σ value, without and with LUT.

5.5 Figure of Merit

In TDCs, a Figure of Merit (FOM) can be used as a performance characteristic indicating the energy per conversion step. It has been defined as the following equation:

$$FOM = \frac{Power}{2^{N_{linear}} \times F_s} \tag{5.1}$$

where the effective number of linear bits, N_{linear}, is defined as

$$N_{linear} = Bits - \log_2(INL + 1) \quad (5.2)$$

The number N_{linear} includes the effect of *Bits*, which is the quantizer resolution, and *INL*, which is the integral nonlinearity [21].

In our design, the TDC resolution was targeted for 13.64 bits, which results from the two-level interpolated coarse-fine delay lines. The 128 stages of coarse delay-line contribute the most significant bits (MSB) of 7 bits, and the 100 stages of fine delay-line contribute the least significant bits (LSB) of $\log_2 100 = 6.64$ bits. So, we have the quantizer resolution *Bits* is 7 + 6.64 = 13.64 bits. The power consumption is 2.05 mW, the *INL* is 1.25 LSB, the N_{linear} is 12.47 bits, the calculated FOM is 0.723 fJ/conversion step.

5.6 Summary of Results

The measurement results are summarized in Table 5.1.

The proposed TDC achieves an input dynamic range of 1.28 ns and a time resolution of 0.1 ps at the conversion rate of 500 M Samples/s. The total power consumption is 2.05 mW with a 1.3 V power supply. The nonlinearity, the figure of merit (FOM) and single-shot precision are given in Table 5.1.

Table 5.1. Proposed TDC Performance Characteristics.

Technology	TI 45nm CMOS
Sample rate	500 M Sample/s
Time resolution	0.1 ps
Expected # of Bits	13.64 bits
Effective # of Bits	12.47 bits
Dynamic range	1.28 ns
Conversion time	6 ns ($3T_{clk}$)
Supply voltage	1.3 V
Power consumption	2.05 mW
Single-shot precision σ (with LUT)	min 1.95 ps, max 2.37 ps, rms 2.21 ps
FOM	0.723 fJ/conv. step
INL	1.25 LSB
DNL	0.5 LSB
Core area	0.75 mm x 0.04 mm = 0.03 mm^2
Chip area	1 x 1 mm^2

The performance of the proposed TDC in comparison with previously high-resolution TDCs is summarized in Table 5.2. Compared with previous works, the proposed TDC achieves fine time resolution and the best FOM.

Table 5.2. Comparison of Performance.

Ref.	Architecture	Tech	Sample Rate	Bits	LSB	rms σ	Range	INL	Power	FOM [b]	Area
		(nm)	(Ms/s)	-	(ps)	(ps)	(ns)	(LSB)	(mW)	(fJ/ conv. step)	(mm^2)
This work	Buffer delay-line and RC delay-line	45	500	13.6	0.1	2.21	1.28	1.25	2.05	0.723	0.03
[12] 2008	Time amplification	90	10	9	1.25	~1.25	0.64	3	4.5	3516	0.6
[13] 2009	Cyclic time domain SAR	350	100	13	1.22	3.2	327K	-	33	-	4.45
[14] 2014	Integrator and SAR-ADC	90	10	9	1	11.74	0.256	2.3	20.4	13148	0.31
[15] 2009	Gated ring oscillator delta-sigma	130	50	11	1	1	-	-	21	-	0.04
[21] 2014	Time register based pipelined	65	250	9	1.12	0.77	0.578	1.7	15.4	325	0.14
[2] 2011	FPGA-based TAC [a]	-	200	-	0.1	1	0~328K	-	5800	-	10000
[22] 2012	Cyclic time amplification	130	50	8	1.25	1.25	±0.16	3	4.3	1344	0.07

[a]Time-to-Amplitude (TAC) architecture: charging a capacitor with a constant current, then analog-to-digital-convert the voltage across the capacitor to produce a binary word.

[b]$FOM = Power/(2^{Nlinear} \times F_s)$(fJ/conversion step), $N_{linear} = Bits - \log_2(INL + 1)$.

CHAPTER 6

CONCLUSION

The purpose of this work was to develop a time-to-digital converter architecture with a fine resolution, low power consumption, small area and low cost.

A novel TDC architecture was proposed and implemented, comprising a 14-bit interpolating coarse-fine time-to-digital converter. The two-level interpolation is based on an asynchronous buffer delay line and a new RC delay line. The asynchronous buffers are clock-controlled dynamic buffers that ensure the precise stage delays and sharp rising edges. The RC delay line concatenates the wire segments as the RC delay stage elements. The insensitivity to the supply voltage and temperature variations of the metal wire eliminates a great deal of the RC delay line non-linearities. A LUT-based calibration scheme was developed to correct non-linearities due to the process variations of the RC delay line and PVT variations of other circuitries in the TDC.

Without the traditional analog components, such as a DLL or PLL, this architecture achieves very low power, very small area and accurate delay measurements. This TDC can therefore be utilized in portable medical equipment.

REFERENCES

[1] W. Gao, et al., Integrated High-Resolution Multi-Channel Time-to-Digital Converters (TDCs) for PET Imaging N. Laskovski, Ed., ISBN: 978-953-307-475-7.

[2] P. Keränen, K. Määttä, and J. Kostamovaara, "Wide-range time-to-digital converter with 1-ps single-shot precision," IEEE Trans. Instrum. Meas., vol. 60, no. 9, pp. 3162–3172, Sep. 2011.

[3] D. I. Porat, Review of sub-nanosecond time-interval measurements, IEEE Transactions on Nuclear Science, Vol. 20, pp. 36-51, 1973.

[4] T. J. Yamaguchi, S. Komatsu, M. Abbas, K. Asada, N. N. Mai-Khanh, and J. Tandon, "A CMOS flash TDC with 0.84–1.3 ps resolution using standard cells," in Proc. IEEE Radio Freq. Integr. Circuits Symp., Montreal, QC, Canada, Jun. 2012, pp. 527–530.

[5] J. Jansson, A. Mäntyniemi, and J. Kostamovaara, "A delay line based time digitizer with 13 ps single-shot precision," Proc. IEEE Int. Symp. Circuits and Systems, May 2005, pp. 4269–4272.

[6] M. Zanuso, P. Madoglio, S. Levantino, C. Samori, and A. L. Lacaita, "Time-to-digital converter for frequency synthesis based on a digital bang-bang DLL," IEEE Trans. Circuits Syst. I, Reg. Papers, Mar. 2010, vol. 57, no. 3, pp. 548–555.

[7] P. Chen, C.-C. Chen and Y. S. Shen, "A low-cost low-power CMOS time-to-digital converter based on pulse stretching", IEEE Trans. Nucl. Sci., 2006, vol. 53, no. 4, pp.2215 -2220.

[8] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line". IEEE Transactions on Solid-State Circuits, February 2000, 35(2):240-247.

[9] J. Yu, et al., "A 12-bit Vernier ring time-to-digital converter in 0.13μm CMOS technology," Symp. on VLSI Circuits, Jun. 2009, pp. 232-233.

[10] C. Chen, S. Lin, and C.Hwang, "An area-efficient CMOS time-to-digital converter based on a pulse-shrinking scheme," IEEE Trans. Circuits Syst. II., vol. 61, no. 3, pp. 163–167, March 2014.

[11] M. Straayer and M. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," IEEE J. Solid-State Circuits, vol. 44, no. 4, pp. 1089–1098, Apr. 2009.

[12] M. Lee and A. A. Abidi, "A 9b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 769–777, Apr. 2008.

[13] A. Mäntyniemi, T. Rahkonen, and J. Kostamovaara, “A CMOS time-to-digital converter (TDC) based on a cyclic time domain successive approximation interpolation method,” IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3067–3078, Nov. 2009.

[14] Z. Xu, M. Miyahara, A. Matsuzawa. “Picosecond resolution time-to-digital converter using Gm-C integrator and SAR-ADC,” IEEE Transaction On Nuclear Science, 2014; 61(2):852–859.

[15] M. Z. Straayer and M. H. Perrott, “A multi-path gated ring oscillator TDC with first-order noise shaping”, IEEE J. Solid-State Circuits, Vol. 44, No. 4, pp. 1089–1098, Apr. 2009.

[16] M. Mota and J. Christiansen, "A high-resolution time interpolator based on a delay locked loop and an RC delay line", IEEE J. Solid-State Circuits, 1999, vol. 34, no. 10, pp.1360 -1366.

[17] M. Mota, “Design and Characterization of CMOS High-Resolution TDCs”, Ph.D. dissertation, Inst. Superior Técnico, Tech. Univ. of Lisbon, Portugal, 2000.

[18] C. Yang and F. Salem, "RC-delay chain-based RF time to digital converter", Proc. IEEE Int. Conf. Mechatronics and Automation, 2006, no. 2528, pp.1543 -1547.

[19] H. Huang, and C. Sechen, “A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS,” IEEE, Circuits and Systems Conf. (DCAS), pp. 1-4, Oct. 2014.

[20] J. Rubinstein, P. Penfield, Jr., and M.A. Horowitz, “Signal delay in RC tree networks," IEEE Transactions on Computer-Aided Design, July 1983, vol. CAD-2, no. 3, pp. 202-210.

[21] K. Kim, W. Yu, and S. Cho, “A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm CMOS using time-register,” IEEE J. Solid-State Circuits, vol. 49, no. 4, pp. 1009–1017, Apr. 2014.

[22] Y. H. Seo, J. S. Kim, H. J. Park, and J. Y. Sim, “A 1.25 ps resolution 8b cyclic TDC in 0.13 m CMOS,” IEEE J. Solid-State Circuits, vol. 47, no. 3, pp. 736–743, Mar. 2012.

BIOGRAPHICAL SKETCH

Huihua Huang was born in Huizhou, Guangdong Province, China. After finishing her high school study in Huizhou NO.1 Middle School, in 1995, she was admitted to South China University of Technology in Guangzhou and majored in Automatic Control Engineering. In the fourth year, she attended the "3+2" Double-Bachelor degree program, with a second major in International Economy and Trade. In July 2000 she received the degree of Bachelor of Engineering and a second degree of Bachelor of Business. After graduation she worked at China Telecom, Guangzhou Co. Ltd. In January 2003 she entered Southern Methodist University in Dallas, TX as a graduate student and received the Master's Degree of Electrical Engineering in December 2004. In January 2006 she entered the doctoral program at The University of Texas at Dallas and majored in Electrical Engineering. She joined the Nanometer Design Laboratory in June 2006. She is currently a Ph.D. student in the area of VLSI design in the Nanometer Design Laboratory.

CURRICULUM VITAE

Huihua Huang

Address: Department of Electrical and Computer Engineering, MS: EC33,
800 W. Campbell Road, Richardson, TX 75080
Email: Huihua.huang@utdallas.edu

EDUCATION

- PhD, Electrical Engineering
  The University of Texas at Dallas, Richardson, Texas, expected in May 2018
  Thesis: *A 0.1 ps Resolution Coarse-Fine Time-to-Digital Converter with 2.21 ps Single-Shot Precision*
  Advisor: Prof. Carl Sechen
- MS, Electrical Engineering
  Southern Methodist University, Dallas, Texas, 2004
- BE, Electrical Engineering
  South China University of Technology, Guangzhou, China, 2000

PROFESSIONAL EXPERIENCE

Engineering Intern, Orora Design Technologies, Inc., Issaquah, Washington
January 2013 – May 2013

- Designed and analyzed analog and mixed-signal IC circuits including PLL, OPAMP, comparator, ADC, etc.
- Participated in projects to develop behavioral models and test benches for customers
- Wrote specifications, implemented functional verification, and evaluated the analog mixed signal design software tool and behavioral modeling platform. Provided Application Engineering support for customers

RESEARCH ASSISTANT EXPERIENCE

Nanometer Design Lab, EE Department, University of Texas at Dallas, Richardson, Texas
September 2006 – present

- Conducted research on optimum architectures for TDC and ADC designs
- Sub-picoseconds High Precision Time-to-Digital Converter (TDC) in TI 45 nm technology
    - Employing 2-level interpolating structure and resolving the difference residue
    - Based on an asynchronous dynamic buffer delay line and an RC delay line
    - 0.1 ps fine resolution, 2.21 ps single-shot precision, 1.25 INL, 2.05 mW ultra-low power with a fabricated chip
    - LUT-based correction technique to cover the PVT variations
- 11b 75 Msps Self-Tuning Analog-to-Digital Converter (ADC) in IBM 130 nm technology
    - Based on time-to-digital conversion, simulated in Spectre and HSPICE
    - Embedded sub-blocks including PLL/DLL, TDC, Comparator, etc.
    - Extra low power consumption of 20 mW (52 fJ/conversion-step), 80% lower than current published results
    - 1 V input range, 1.5 V supply voltage, 66 dB SNR
    - Self-tunable major blocks to address process, voltage and temperature (PVT) variations
- 11-bit High Frequency High Precision Time-to-Digital Converter (TDC) in IBM 130 nm technology
    - Employing novel 3-level interpolating structure
    - Providing 3 ps fine resolution, 10.2-b DNL/ 10-b INL

TEACHING ASSISTANT EXPERIENCE

Teaching Assistant in Department of Electrical Engineering, University of Texas at Dallas, Richardson, Texas

- Classes include: VLSI design, Electronic Circuits, Introduction to Digital Systems
- Lectured and trained students on digital design flow and EDA tools, including Cadence and Synopsis tools, HSPICE simulators
- Designed web pages on lab tools and tutorials
- Tutored students on VLSI concepts in lab sessions and extra sessions after class
- Proctored exams, and graded assignments, project reports and exams

PUBLICATIONS

- Huihua Huang, Carl Sechen, "A 22mW 227Msps 11b Self-Tuning ADC Based on Time-to-Digital Conversion", 4th Annual Austin Conference on Integrated Systems & Circuits (ACISC) 2009, Austin, Texas, Oct. 2009.
- Huihua Huang, Carl Sechen, "A 14-b, 0.1ps Resolution Coarse-Fine Time-to-Digital Converter in 45 nm CMOS", 10th IEEE Dallas Circuits and Systems Conference (DCAS) 2014, Richardson, Texas, Oct. 2014.
- Huihua Huang, Carl Sechen, "A 0.1ps Resolution Coarse-Fine Time-to-Digital Converter with 2.21 ps Single-Shot Precision", submitted for publication, 2018.

TECHNICAL SKILLS

- Design abilities: General analog and mixed-signal blocks design, including A/D Converter, TDC, SRAM, PLL/DLL, Amplifier, Charge Pump, digital blocks design & verification, logic simulation, synthesis, optimization, static-timing analysis, place-and-route, and post layout verification
- Tools: Cadence design tools (Virtuoso, Spectre, Assura, Encounter), Synopsys design tools (Design Compiler, PrimeTime, HSPICE), UNIX, Linux

LANGUAGUES

Verilog, C++, PERL