Effect of Film Thickness on the Ferroelectric and Dielectric Properties of Low-Temperature (400 ºC) $Hf_{0.5}Zr_{0.5}O_2$ Films

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Effect of film thickness on the ferroelectric and dielectric properties of low-temperature (400 °C) $Hf_{0.5}Zr_{0.5}O_2$ films

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We report on the effect of the $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film thickness on the ferroelectric and dielectric properties using pulse write/read measurements. HZO films of thicknesses ranging from 5 to 20 nm were annealed at 400 °C for 1 min in a nitrogen ambient to be compatible with the back-end of the line thermal budget. As the HZO film thickness decreases, low-voltage operation (1.0 V or less) can be achieved without the dead layer effect, although switching polarization (P_{sw}) tends to decrease due to the smaller grain size. Meanwhile, for 20-nm-thick HZO films prepared under the identical stress (similar TiN top electrode thickness and thermal budget), the P_{sw} and dielectric constant are reduced because of additional monoclinic phase formation. *Published by AIP Publishing.*
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Today, embedded planar capacitor ferroelectric random access memory (FRAM) cells using $Pb(Zr,Ti)O_3$ (PZT) are integrated in complementary metal oxide semiconductor (CMOS) flow at the 130 nm node.[1–3] In this technology, 70-nm-thick PZT films have been used to manufacture commercial FRAM devices operating at 1.5 V.[1–3] However, at this time, this technology is limited due to the scaling of the PZT film thickness and the unavailability of a conformal PZT deposition process. Moreover, most conventional ferroelectric (FE) materials require a high thermal budget to ensure uniform FE crystal phases. The high temperature process prevents the integration of FE circuits in the back-end of line (BEOL) to increase the effective memory area and add more functionality for CMOS nodes beyond 130 nm.

Recently, ferroelectricity in thin $Hf_{1-X}B_XO_2$, where B = Si, Al, Y, Zr, etc., films (10 nm) deposited by atomic layer deposition (ALD) has been reported.[3–8] The FE behavior of these $Hf_{1-X}B_XO_2$ films can be influenced by the capping layer, dopant species/concentration, and thermal treatment.[3–9] With the introduction of the dopants or alloying elements as well as integration schemes and processing parameters, the formation of the non-centrosymmetric orthorhombic phase (o-phase, space group: $Pca2_1$) responsible for FE polarization can be enhanced. Large FE polarization has been observed at low temperatures, 400 °C, by controlling the tensile stress from the TiN top electrode during the annealing process.[3,8] This low thermal budget process facilitates the integration of FE circuits in the BEOL, allowing for a wider range of applications. In addition, the $Hf_{1-X}B_XO_2$ films show that the coercive field (E_c, approximately 1–2 MV/cm) is constant regardless of the film thickness.[9,10] This is because, unlike the conventional PZT devices,[11] the interface layer has a relatively low effect on the switching characteristics. Consequently, by further reducing the film thickness, it is expected that the low-voltage operation [i.e., FE saturation voltage (V_{sat})] of the HfO_2-based FRAM devices can be realized without losing the FE characteristics. Apart from memory applications, the use of $Hf_{1-X}B_XO_2$ FE materials has also been proposed to achieve a steep subthreshold swing (<60 mV/decade) and low voltage/low power operation through negative capacitance effects in conventional field-effect transistors.[12,13] This makes FE and dielectric characteristics of $Hf_{1-X}B_XO_2$ films that are influenced by their film scaling more important.

In the present study, the FE and dielectric properties of $Hf_{0.5}Zr_{0.5}O_2$ (HZO) were investigated as a function of film thickness using pulse write/read measurements to simultaneously extract the FE switching polarization (P_{sw}), FE V_{sat}, and dielectric constant (ε_r). The extracted parameters were compared with the parameters calculated from the conventional polarization-electric field (P-E) and small signal capacitance-voltage (C-V) measurements, respectively. All HZO films used in this study were annealed at 400 °C after TiN top electrode (used as a stressor layer) deposition.

The TiN/HZO/TiN capacitor stacks were formed on 100 mm p-type Si wafers with a thermally grown SiO_2 film (300-nm-thick) and annealed at 400 °C for 60 s in an N_2 atmosphere using a rapid thermal annealing (RTA) system. HZO films with thicknesses of 5, 7, 10, and 20 nm were deposited by ALD (Cambridge Nanotech Savannah S100) using tetrakis-dimethylamido-hafnium ($Hf[N(CH_3)_2]_4$), tetrakis-dimethylamido-zirconium ($Zr[N(CH_3)_2]_4$), and O_3 as the Hf-precursor, Zr-precursor, and oxygen source, respectively. The Zr content for maximum FE polarization can be stable at ~50% due to its very similar physical and chemical properties to those of Hf.[5–8] By alternately depositing Hf and Zr precursors (an Hf:Zr ratio of 1:1) through an ALD process, homogenous HZO thin films having satisfactory FE properties can be achieved at low process temperature. During the HZO deposition, the wafer temperature was set to 250 °C, and high concentration O_3 (400 g/m^3) was formed by

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an O_3 generator [OP-250H, Toshiba-Mitsubishi-Electric Industrial Systems Corporation (TMEIC)]. Both bottom and top TiN (90-nm-thick) electrodes were deposited at room temperature by radio frequency magnetron sputtering. A conventional photolithography/etching process was performed using an Au hard mask [(Au (85 nm)/Pd (3 nm)] deposited using an electron-beam evaporator. To estimate the precise area of metal-insulator-metal (MIM) capacitors, the over-etching values were calculated by linear extrapolation of the square root of the capacitance versus the device diameter and included in the following electrical results.

Generally, the total polarization is divided into two components: switching and non-switching contributions. The switching component is responsible for the FE polarization, and the non-switching component is reflected in ε_r. The two components can be extracted simultaneously from the pulse write/read measurements. For the pulse write/read measurement,[3,8] a series of write and read trapezoidal voltage pulses with a pulse width of 4 μs, a rising/falling time of 1 μs, and a delay time of 10 μs were applied to all the TiN/HZO/TiN capacitors using a pulse generator (Agilent 81110A) with an internal resistance of 50 Ω (a shunt resistor) as shown in Fig. 1(a). The applied write voltage was varied based on the HZO film thickness to maintain an electric field of 2.5 MV/cm; the load currents were measured according to the read voltage variations and integrated to estimate P_{sw}. By subtracting the integrated current values of the switching and non-switching pulses, the real FE P_{sw} values were extracted [see the top of Fig. 1(b)]. After 10^5 wake-up cycles at a field of 2.5 MV/cm to achieve the stabilized FE polarization, the 10-nm-thick HZO-based capacitor exhibited the largest P_{sw} of 44.9 μC/cm^2, while the 5-, 7-, and 20-nm-thick HZO-based capacitors yielded P_{sw} values of 8.2, 37.3, and 28.5 μC/cm^2, respectively. As the HZO film thickness decreases, FE V_{sat} determined when the extracted P_{sw} becomes saturated also decreased. The V_{sat} values for the 5-, 7-, 10-, and 20-nm-thick HZO-based capacitors were about 0.8, 1, 1.6, and 3 V, respectively. Moreover, the slope of the non-switching pulse write/read results could be used to extract ε_r of the HZO film as shown in the bottom of Fig. 1(b).

Figure 2 shows the P-E hysteresis curves of 5-, 7-, 10-, and 20-nm-thick HZO-based capacitors measured at 10 kHz using a semiconductor parameter analyzer (Keithley 4200-SCS) after 10^5 wake-up cycles at a field of 2.5 MV/cm. The extracted remnant polarizations ($2P_r$) of the 7- and 10-nm-thick HZO-based capacitors were approximately 40.5 and 50.9 μC/cm^2, respectively, whereas those of the 5- and 20-nm-thick HZO-based capacitors were 11.9 and 32.1 μC/cm^2, respectively. Meanwhile, E_c of all the HZO-based capacitors is about 1 MV/cm independent of the HZO film thickness, unlike the conventional FE films.[11] These results suggest that the operation voltage to achieve an adequate polarization, $2P_r$, can be reduced: for a 5-nm-thick HZO film to 1 V or less.

The polarization can also be estimated from the conventional small signal C-V measurements by

$$P = \frac{1}{A}\int C(V)dV,$$

where A is the area of the HZO device. This equation is used to calculate a voltage-induced polarization change. Small signal C-V hysteresis curves of 5-, 7-, 10-, and 20-nm-thick HZO-based capacitors were measured at a frequency of 10 kHz with an amplitude of 50 mV using an Agilent 4284A[14] and integrated as shown in Fig. 2. A small hysteresis is observed in the integrated C-V hysteresis curve due to the superimposed dc bias, but it is negligible compared to the hysteresis loop of the P-E hysteresis curve. In the saturation

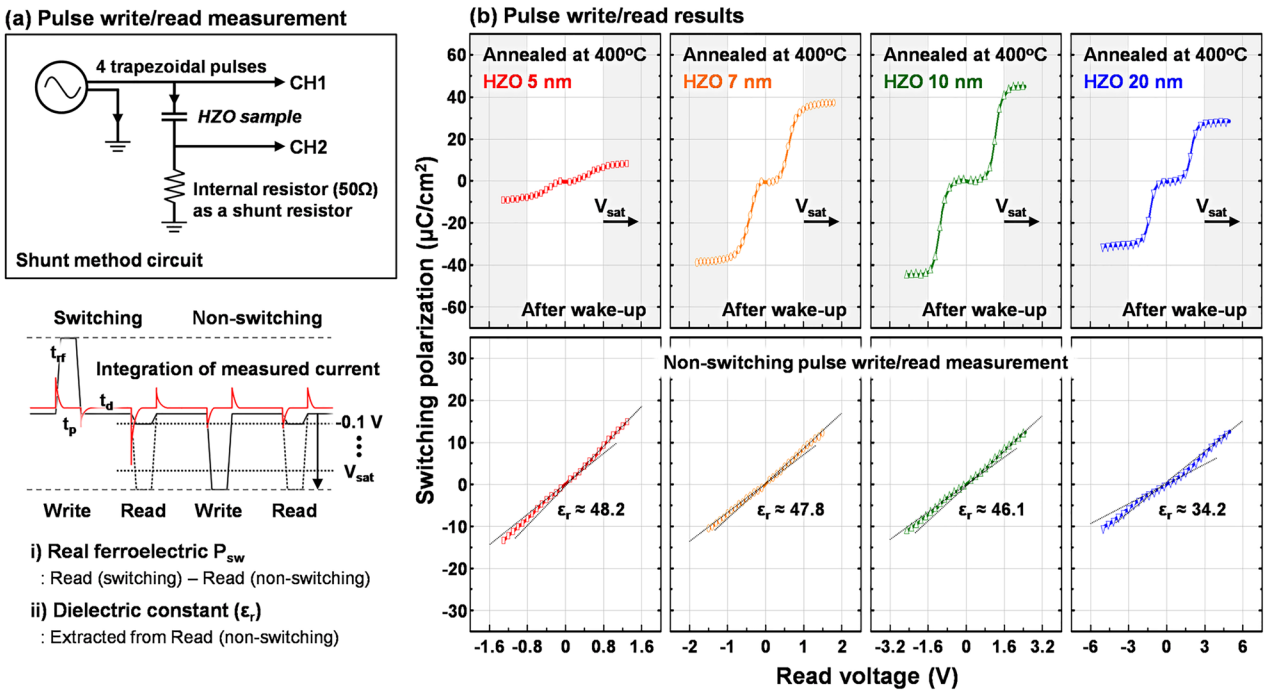

FIG. 1. (a) Schematic diagram of the pulse write/read measurement. (b) Pulse write/read results of 5-, 7-, 10-, and 20-nm-thick HZO-based MIM capacitors after wake-up field cycling (10^5 cycles @ 2.5 MV/cm).

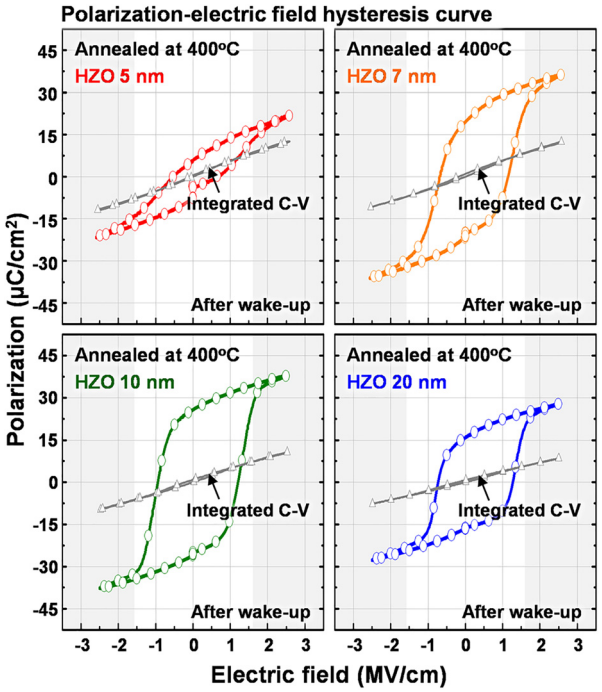

FIG. 2. Polarization-electric field hysteresis and integrated capacitance-voltage hysteresis curves of 5-, 7-, 10-, and 20-nm-thick HZO-based MIM capacitors after wake-up field cycling (10^5 cycles @ 2.5 MV/cm).

region (as indicated by the gray scale), the polarization of the integrated C-V hysteresis curve is much smaller than that of the P-E hysteresis curve because the capacitance was measured with a small amplitude signal (50 mV).[15–17] It should be noted that the slope of the saturation region corresponding to ε_r is almost identical for both the integrated C-V and P-E hysteresis curves. This is so because in the saturation region of the P-E hysteresis curve, the FE switching effect is minimized and only the non-switching polarization (due to ionic and electronic polarization) can be excited. Consequently, the ε_r values extracted from the saturation region of the integrated C-V and P-E hysteresis curves are similar to the ε_r ($<E_c$) extracted from the non-switching pulse write/read results when the read voltage is much lower than the coercive voltage.

The switching component can also be determined by subtracting the non-switching component (i.e., integrated C-V hysteresis curve) from the total polarization (i.e., P-E hysteresis curve).[15,17] This method is the same as the FE P_{sw} extraction method using pulse write/read measurements as shown in the top of Fig. 1(b). For the 5-nm-thick HZO-based capacitor, the ratio (~40%) of P_{sw} to total polarization at 2.5 MV/cm is smaller than that (~70%) of the other HZO samples [see Fig. 3(c)].

Figure 3 shows a comparison of the FE parameters of 5-, 7-, 10-, and 20-nm-thick HZO-based capacitors used in this work. P_{sw} and $2P_r$ extracted from the pulse write/read measurement and P-E hysteresis curve tend to increase as the HZO film thickness increases, respectively, but decrease with the 20-nm-thick HZO-based capacitor. ε_r of the 20-nm-thick HZO-based capacitor is also lower than that of other HZO samples. These results can be attributed to the partial formation of the monoclinic phase (m-phase, space group: $P2_1/c$) in a 20-nm-thick HZO film during the annealing

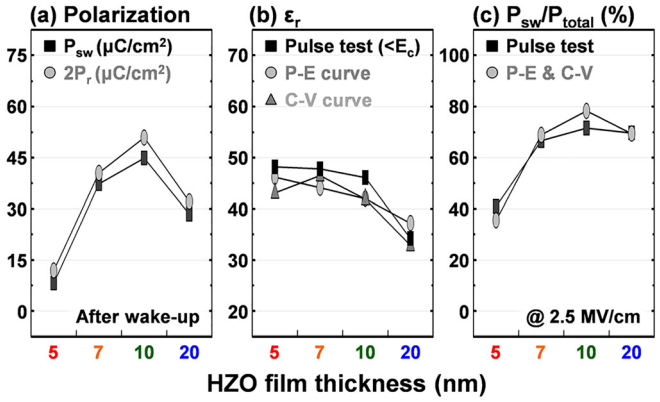

FIG. 3. Comparison of the parameters of 5-, 7-, 10-, and 20-nm-thick HZO-based MIM capacitors used in this work: (a) polarization extracted using the pulse write/read measurement and the P-E hysteresis curve and (b) dielectric constants extracted using pulse write/read measurements, P-E hysteresis curves, and integrating small signal C-V hysteresis curves. (c) Ratio of switching polarization to total polarization.

process.[9] Meanwhile, the low P_{sw} and $2P_r$ of the 5-nm-thick HZO-based capacitor are associated with a relatively low FE switching contribution, as shown by the ratio of P_{sw} to total polarization (i.e., P_{sw}/P_{total}) at 2.5 MV/cm.

The crystal structure of 5-, 7-, 10-, and 20-nm-thick HZO films annealed at 400 °C was determined by grazing-angle incidence X-ray diffraction (GIXRD) measurements, using a Rigaku SmartLab system, in the 2θ range of 26°–40° with an incidence angle of 0.5° as shown in Fig. 4. HZO peaks centered at ~30.5° and ~35.5° are assigned to the o(1 1 1) and o(2 0 0) phases.[8,9,18] The HZO (-1 1 1) and (1 1 1) peaks from the m-phase and TiN (1 1 1) peaks from the bottom electrodes are centered at ~28.5°, ~31.5°, and 36.7°, respectively.[8,9,18] It is believed that the non-centrosymmetric o-phase responsible for FE polarization is achieved under large tensile strain.[8,19] By controlling the mechanical stress from the TiN top electrode during the annealing process (known as the "capping layer effect"), HZO films can phase transform to the o-phase formation with inhibition of m-phase formation even at low process temperature (400 °C).[8] However, all the HZO samples used in this study were fabricated with identical stress (similar TiN thickness and thermal budget) in order to focus on the HZO film thickness effect. Consequently, the 5-, 7-, and 10-nm-thick HZO films

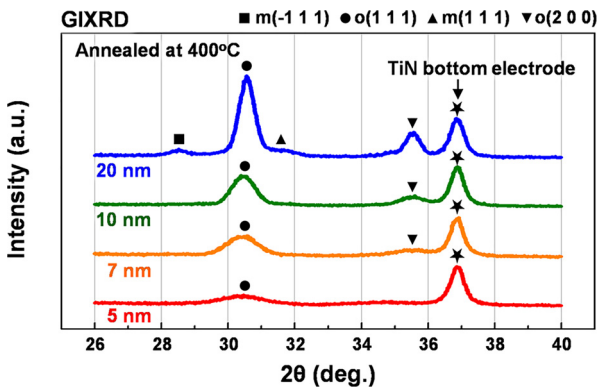

FIG. 4. GIXRD patterns of 5-, 7-, 10-, and 20-nm-thick HZO films annealed at 400 °C after TiN top electrode deposition. The X-ray data are taken after chemical removal of the TiN top electrode.

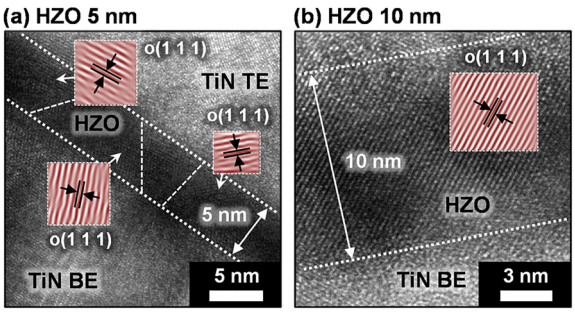

FIG. 5. Cross-sectional HR-TEM images of (a) 5-nm-thick and (b) 10-nm-thick HZO-based MIM capacitors. For better visibility, the reverse FFT images obtained from the filtered FFT images by mask are artificially colored.

annealed at 400 °C exhibit o-phase formation, whereas the 20-nm-thick HZO film reveals the formation of both the o-phase and the m-phase. Because the m-phase has the lowest ε_r among the polycrystalline HfO_2 and ZrO_2 phases,[20,21] the 20-nm-thick HZO-based capacitor exhibited relatively low ε_r compared to other HZO samples.

Figure 5 shows cross-sectional high-resolution transmission electron microscopy (HR-TEM, JEOL JEM-2100F) images of the 5- and 10-nm-thick HZO-based capacitors. The 5-nm-thick HZO film consists of many separate grains with an average length of about 5 nm in the horizontal direction, as identified by lattice fringes with different directions in different areas as shown in Fig. 5(a). However, large and well-orientated grains of the 10-nm-thick HZO film with a length of approximately 30 nm in the horizontal direction were formed as shown in Fig. 5(b). In the case of the 5-nm-thick HZO film, the o-phase seems to be more stable than the m-phase due to the surface and grain boundary energy effects,[18] but the smaller grain size results in a lower FE switching contribution because the domain wall motion may be more difficult. When the 5-nm-thick HZO films are annealed again at high temperature (450 °C or higher), the grain size increases significantly in the horizontal direction, and the FE switching contribution can be increased (i.e., P_{sw} and $2P_r$ increase).[14] The diffraction spots from the o(1 1 1) phase of both HZO films are marked in fast Fourier transformation (FFT) images, and the inter-atomic distance in both HZO films, measured using its reverse images filtered by a mask, was approximately 2.94 Å. The value is consistent with the d-spacing value achieved from GIXRD results in this study.

In conclusion, we have investigated the effect of the film thickness on the FE and dielectric properties of 400 °C annealed HZO films prepared by ALD. The pulse write/read measurements used in this work are useful for simultaneously describing the FE and dielectric properties. All the HZO films annealed after TiN top electrode deposition formed in the o-phase responsible for FE properties regardless of the film thickness. For low temperature FE HZO films, P_{sw} tends to increase as the HZO film thickness increases, but decreases for the 20-nm-thick HZO-based capacitor. This is associated with the formation of the m-phase in addition to the o-phase in the 20-nm-thick HZO film after annealing, which is also related to the lower ε_r. On the other hand, the 5-nm-thick HZO-based capacitor also showed low P_{sw} due to the smaller grain size, but the low-voltage operation (1.0 V or less) can be achieved without ε_r reduction. Our results indicate that the low thermal budget HZO FE films can be integrated in the BEOL (i.e., no impact on transistor process flow and performance) for embedded smart memory and multi-functional device applications.

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