CIRCUIT LEVEL MODELING OF SPINTRONIC DEVICES

by

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To my brave, beautiful, kind mother,

Renu Sharma

CIRCUIT LEVEL MODELING OF SPINTRONIC DEVICES

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CIRCUIT LEVEL MODELING OF SPINTRONIC DEVICES

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It is an exciting time for circuit designers working on beyond-CMOS logic and memory design. Many alternative technologies to conventional Complementary Metal Oxide Semiconductor (CMOS) technology have been proposed in recent years and there is an ongoing effort by many state of the art research institutes around the world to fabricate these devices. The magneto-electric (ME) devices are just one class of beyond-CMOS device, but they offer some advantages which make them a very promising group of devices, including non-volatility, voltage control and low-power operation. These devices are extremely compact compared to the CMOS equivalents. Many advantages of the ME devices are known although there have been no quantitative studies for the calculation of the energy requirements of the voltage control of magnetism, thus it is important to understand the trade-offs of the components. Perceiving a need for a modeling platform for simulating the possible logic circuits that can be derived from the ME devices and also perform an energy-delay evaluation of these devices, we developed Verilog-A models. These models are used in Spectre to simulate ME based circuits and evaluate their performance compared to the CMOS equivalents.

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CHAPTER 1

INTRODUCTION

This dissertation will cover the operation, modeling and circuit development of the voltage controlled magneto-electric (ME) devices such as, the Magneto-electric Magnetic Tunnel Junction (ME-MTJ), the Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) and the Magneto-electric Field Effect Transistor (MEFET). These devices are modeled using MATLAB and Verilog-A. Circuit simulations are performed using the Cadence suite, primarily Spectre and the schematic editor and the layouts are designed using Cadence Virtuoso. Bẹnchmarking has been performed on these devices in comparison with Complementary Metal Oxide Semiconductor (CMOS) based circuits in terms of the energy and delay. These results are valuable in analyzing the benefits of these emerging technologies compared to conventional CMOS.

1.1 Motivation

Silicon based CMOS devices have dominated the semiconductor industry for over 40 years [1-2]. As the process node is scaled, to increase the density and performance of the chip, efficient circuit design becomes challenging due to increased leakage and physical scaling limits of the materials used. One of the leakage components comes from the silicon dioxide (SiO_2) layer, used in the CMOS gates due to the reduced thickness at scaled processes. This limitation can be managed by replacing the SiO_2 layer by a physically thicker layer of a higher dielectric constant or 'high- K' such as hafnium oxide [3], which increases the gate capacitance and the drive current in order to enhance the device performance. Also, there is a thrust in the industry towards vertical

transistor design which reduces the short-channel effects and allows better control of the electrostatics. New materials such as III-Vs, SiGe as well as new structures, such as, FinFETs [4], gate-all-around can be employed to overcome the limitations associated with CMOS scaling.

Another approach is to work with alternate device schemes sometimes referred to as beyond-CMOS devices employing novel materials and structures which are extremely power efficient, provide the same functionality as CMOS and are more area efficient. The latter option forms the basis of this dissertation. The International Roadmap for Emerging Technologies (ITRS) roadmap from 2013 [5,6] is shown in Figure 1.1 which illustrates the scaling of process nodes and the application areas. It is noted that as the node is scaled below 22 nm, the miniaturization would still occur, but with constraints in power and performance. Figure 1.1 also indicates that beyond-CMOS devices can enable furthur scaling. Comparisons between the CMOS and beyond-CMOS devices have previously been made in the benchmarking papers by Nikonov and Young [7-9]. Beyond-CMOS devices have the potential to replace CMOS, or work with CMOS as a part of merged technology to form hybrid circuits for logic and memory applications.

Various spin based or spintronic devices have been considered for next generation integrated circuits [10-15]. These devices substitute electron's spin orientation for the state variable (logic level) representation, compared to electrical charge (usually voltage level) in CMOS. In addition to power and area efficiency, spintronic devices promise a potential solution to leakage issues expected in scaled CMOS processes.

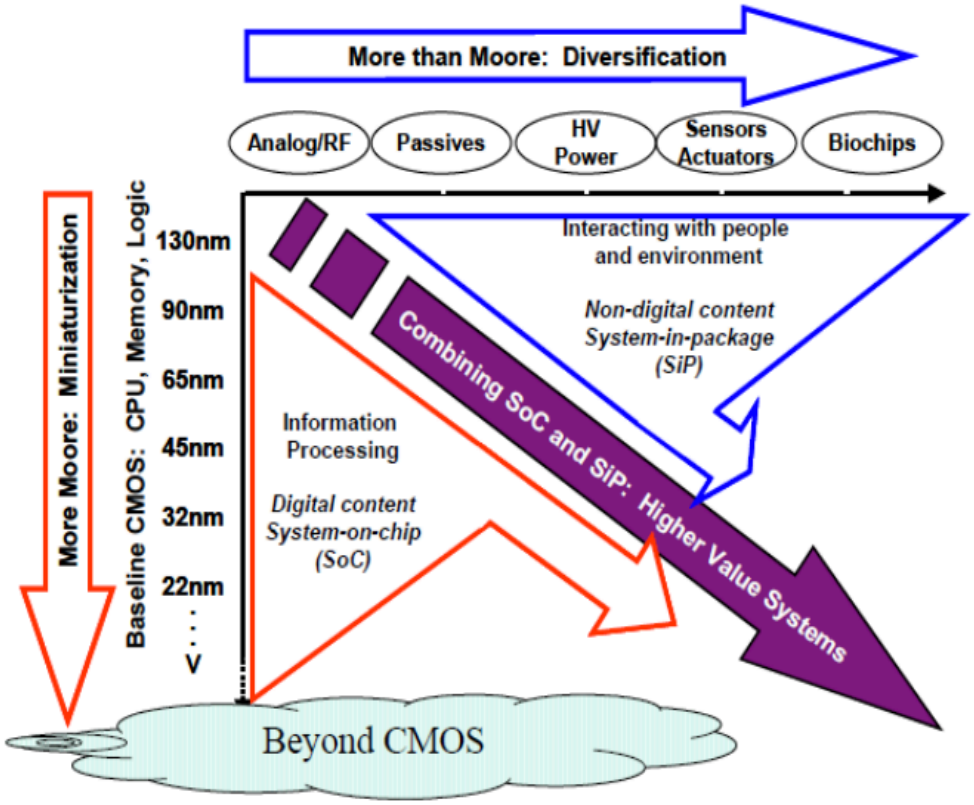

Figure 1.1: ITRS roadmap [6].

Spintronics is already successful for applications in magnetic read-heads and sensors [16]. The device takes advantage of the giant magnetoresistance (GMR) [17-19] in which the stack consists of a 'fixed' and 'free' ferromagnetic (FM) layer sandwiching a metallic spacer. This stack forms a Magnetic Tunnel Junction (MTJ) device [20] which provides a change of resistance related to modification of the magnetic configuration between the two neighboring FM films. The spin orientation of fixed FM layer is 'fixed' in a given direction whereas the free FM layer is allowed to switch freely. If the relative spin orientation in the two FM layers is parallel, the resistance is low and is represented by bit "0" and if the orientation is anti-parallel, the resistance is high,

represented by bit "1". To improve the magnetoresistance (MR) of tunnel junctions, the metallic spacer is replaced by an insulating non-metallic barrier. These devices were first proposed in [20] and further discussed in [21-23] where it was calculated that crystalline MgO (001) would have superior properties compared to the aluminum oxide (Al_2O_x) as the insulating barrier. There is continued research to enhance the Tunneling Magnetoresistance (TMR) ratio which has led to recent room temperature TMR values as high as 600% [24] and 1000% [25].

The MTJ device forms an integral part of the memory element known as Magneto-resistive Random-Access Memory (MRAM) which is a way of storing bits via the magnetic moments in the FM layers. There are several flavors of MRAM memory for ex- field assisted random-access memory, Ferroelectric Random-Access Memory (FeRAM), Phase Change Memory (PCM), Resistive Random-Access Memory (ReRAM) and Spin Transfer Torque Random-Access Memory (STT-MRAM). Field assisted MRAM uses magnetic field generated by the current carrying coil in order to switch the magnetic moments in FM materials.

This has severe limitations in terms of energy efficiency since large electric currents are required to generate the fields necessary for switching. An alternate scheme is to switch the magnetic element using a spin polarized current where the spins of conduction electrons is aligned in a given direction. STT-MRAM uses this scheme to switch the free FM layer. The MTJ stack is accessed by a CMOS device. This device is commercially available [26] and is one of the most promising devices as the next generation memory devices. In fact, the perpendicular STT-MRAM is ready to be deployed as an embedded 22nm memory [27]. The spin transfer torque (STT) mechanism currently provides the lowest-energy path to electrical switching of magnetism but nonetheless requires energetically-costly current densities of as high as ~1 MA/m^2 [28].

In contrast, incorporating a voltage controlled non-volatile state variable eliminates high current densities. Electric control of magnetism provides a path to design devices with lower-power, high integration density and logic functionality compared to CMOS. A novel approach to voltage controlled magnetic devices envisions the use of the magneto-electric materials [29-32]. While the energy requirements of these devices are lower, compared to conventional STT MRAMs, there have nonetheless been no quantitative studies to date of the energy requirements of voltage controlled magnetism (VCM) technology thus it is important to understand the trade-offs of these devices.

Important questions here concern the energy-delay product for such devices [7,8] together with their capacity to be scaled to larger circuits. Critical here is the whether these new devices and circuits have the potential to compete with CMOS. The addition of non-volatile functionality through the use of ME elements is useful but the circuits should also be comparable to CMOS in terms of their energy requirements, delay and costs which is the focus point of this research and has also been presented in [33-43]. Perceiving a need for a modeling platform for simulating the possible logic circuits that can be derived from the ME devices and also perform an energy-delay evaluation of these devices, we developed Verilog-A models. These are used as a modeling platform for simulating ME devices in Spectre to evaluating their performance compared to conventional CMOS at the circuit level.

1.2 Materials for ME Device Design

1.2.1 Magneto-electric Materials

MEs are materials in which a static magnetization may be induced by applying suitable electric field. As highly-insulating dielectrics, magnetization may be induced without the need to drive any significant electrical current, thereby providing a low-power pathway to the electrical manipulation of magnetism. The characteristic of VCM makes MEs increasingly attractive for various beyond-CMOS spin based technologies [7,8].

MEs in which the induced magnetization is associated with a sizable, and electrically-switchable, interfacial spin polarization are of particular interest [44-49]. The boundary magnetism promises a number of advantages for the development of post-CMOS devices, which in turn may be integrated into circuits that are capable of exhibiting the key characteristics of non-volatility and low-power operation [32].

Chromia (Cr_2O_3) [31,50,51] is an antiferromagnetic (AFM) ME that exhibits interfacial spin polarization at temperatures below its Néel temperature (T_N) of 308K. It displays significant boundary magnetization demonstrated by photoemission [46]. This boundary magnetization exchange couples to the free FM layer such that the switching is voltage controlled. Recently, a strategy based on boron doping of this material has been found to raise its T_N to above 420K [48], suggesting that doped chromia may allow the realization of practical circuits, stable at room temperature. Such an approach represents a significant advance over existing technologies. The high intrinsic resistivity of chromia (~100 TΩcm at room temperature [52]) is able to support VCM

with little loss, allowing chromia to be utilized for robust implementation of the computational state variable in suitably designed devices [29,31,50,51,53].

1.2.2 Two-Dimensional Channel Materials

Since, the switching of the AFM order of the ME antiferromagnets switched by external electric fields is limited by the switching of the FM layer, the operation speeds are low. There is an alternative way of making use of the interfacial magnetism of the ME gate resulting in better performance. This is achieved by the use of proximity effect between the ME and the two-dimensional (2D) channel. ME materials have the potential to polarize the spin vectors in a thin narrow channel semiconductor made of a 2D material. The switching of the induced spin polarization is instantaneous and the switching of ME AFM is intrinsically much faster than the ferromagnets. Also, the AFM order of ME is intrinsically non-volatile.

There is a wide variety of 2D materials that are currently being researched on including graphene, Transition Metal Dichalcogenides (TMDs), black phosphorus etc. [54,55]. Graphene possesses the property of being polarized by the proximity of magnetic atoms [42-48]. In Renu et. al. [56], it is experimentally shown that even though the net magnetization of graphene is small, there is spin polarized electron transport due to the pronounced peaks exhibited by energy-dependent spin polarization. Although, single layer graphene has high mobilities > 100,000 cm^2/Vs at room temperature [57], it is ill-suited for field-effect transistor (FET) applications due to low on-off ratios as a result of zero band-gap and high output conductance [55]. TMDs such as Tungsten Selenide (WSe_2) and Molybdebum Sulfide (MoS_2) are promising 2D materials suitable for FET applications. MoS_2 has a direct band-gap of 1.9 eV and it has potential for high-

performance (HP) n-type FETs. WSe_2 displays strong spin-orbit coupling energy of 513 meV [58] which allows room temperature operation [59-62].

1.3 Need for Compact Models

Compact model development has become a cornerstone in the circuit/system design and verification tool flow [63]. Compact modeling refers to the development of models for integrated semiconductor devices in circuit simulations [64]. This is well developed for CMOS where extremely accurate models, for example the Berkeley Short-channel Insulated-Gate Field Effect Transistor Model (BSIM) [65], are used to simulate large circuits before the circuit is fabricated in silicon, but not for the ME devices, which is still an open research task. Through this work, different modeling techniques are proposed to provide a platform for circuit designers to model the proposed ME devices for the evaluation of energy and delay.

The MATLAB physical model has been developed to compute the ME-MTJ device performances in terms of energy and delay [37] and the Verilog-A model has been developed to implement ME circuits [35,38,40,41]. Both the models break down the switching process into three key stages of operation: electrical-to-magnetic conversion, magnetization transfer, and electrical readout of the final stage. Various physical models have been incorporated in both the platforms for accuracy.

1.3.1 MATLAB Model

MATLAB as a high-performance language for technical computing is often used for compact model development. It is a powerful data manipulation and advanced visualization

routines [66]. As previously discussed, the ME-MTJ and its derived devices have been modeled in MATLAB and the energy and delay terms are estimated from the physical equations and compared to CMOS equivalents [37].

The limitation of using MATLAB is that it is not well suited for use as a component model since it does not have the capability to analyze details of large circuits. Thus, in order to analyze larger, more complex circuits along with the back-end-of-line (BEOL) effects such as device to device interactions and interconnect effects, Verilog-A models are used. These models are compatible with circuit level simulators such as SPICE or Cadence Spectre [67].

1.3.2 Verilog-A

It is crucial to test the circuit functionality in the early stages of the design cycle. This can be done with ease using the Verilog-A platform. It is an industry standard modeling language, which we used here to generate a compact model that can be used with a circuit level simulator. It includes many mathematical built-in functions providing easier mathematical descriptions of components and the modeling process is straightforward [66]. It is primarily designed to allow users of SPICE simulators to incorporate mathematical models for circuit simulations.

1.4 Contribution of this Research

The main contributions of this research are as follows:

- We demonstrate the development of the first compact model of the ME-MTJ and its derived devices in MATLAB and estimate the energy and delay using the device parameters [37].

- We show the development of the first compact model of the ME-MTJ devices in Verilog-A and use these models to design and test ME-MTJ based analog and digital circuits. The digital circuits include inverter, buffer, NAND, NOR, XNOR, 1-bit and 5-bit full adder etc. and the analog circuits include comparator, flash and serial analog to digital converter (ADC) [35,38,40-43].
- We propose novel designs for the ME-MTJ based Static Random-Access Memory (SRAM) cell to introduce non-volatility in the circuit [33].
- We demonstrate a new device concept known as the UMMTJ device which requires unipolar input supply reducing the number of CMOS components for operation [39]. We also show the programming techniques as well as simulation results for the UMMTJ based devices designed using Verilog-A models.
- We demonstrate the development of the compact modeling of the single source and dual source MEFETs and their derived devices. These devices are modeled in Verilog-A and designed and simulated in Cadence environment [43].
- We show the benchmarking results of the ME devices and the CMOS equivalents.

1.5 Scope and Organization of the Dissertation

This dissertation is organized into seven chapters including introduction.

Chapter 2 discusses the ME-MTJ device and its derived structures along with the two modeling techniques, i.e., MATLAB and Verilog-A. The circuit simulation results have been

presented for the ME-MTJ digital and analog circuits. The memory applications of the ME-MTJ devices are also demonstrated and ME-MTJ-CMOS hybrid circuits are proposed.

Chapter 3 describes an enhanced version of the ME-MTJ device, i.e., the UMMTJ device and its derived devices. Various programming schemes and applications have also been proposed for this device. Experimental work done in collaboration with the University of Nebraksa at Lincoln has also been included.

In chapter 4, the single and dual source MEFET device and their derived logic functions have been introduced and the Verilog-A modeling framework has been described. This chapter also presents the transient simulation results of the MEFET based logic gates.

In chapter 5, the benchmarking of the ME-MTJ and MEFET devices with respect to CMOS has been presented. Also, the comparison results of the CMOS based devices (DRAM, NAND flash) with beyond-CMOS devices (ME-MTJ, Ferroelectric Tunnel Junction (FTJ) and Ferroelectric Field-Effect Transistor (FE-FET)) based on performance have been considered.

Chapter 6 presents the performance comparison of CMOS based devices (high-performance and low-power SRAM cell) and resonant charge-based devices, i.e., the Bilayer PseudoSpin Field-Effect Transistor (BiSFET), Bilayer Pseudospin Junction Transistor (BiSJT) and the Interlayer Tunnel Field-Effect Transistor (ITFET).

In chapter 7, the future research directions for circuit design of ME devices have been outlined. The hierarchy of the work in this study is shown in Figure 1.2.

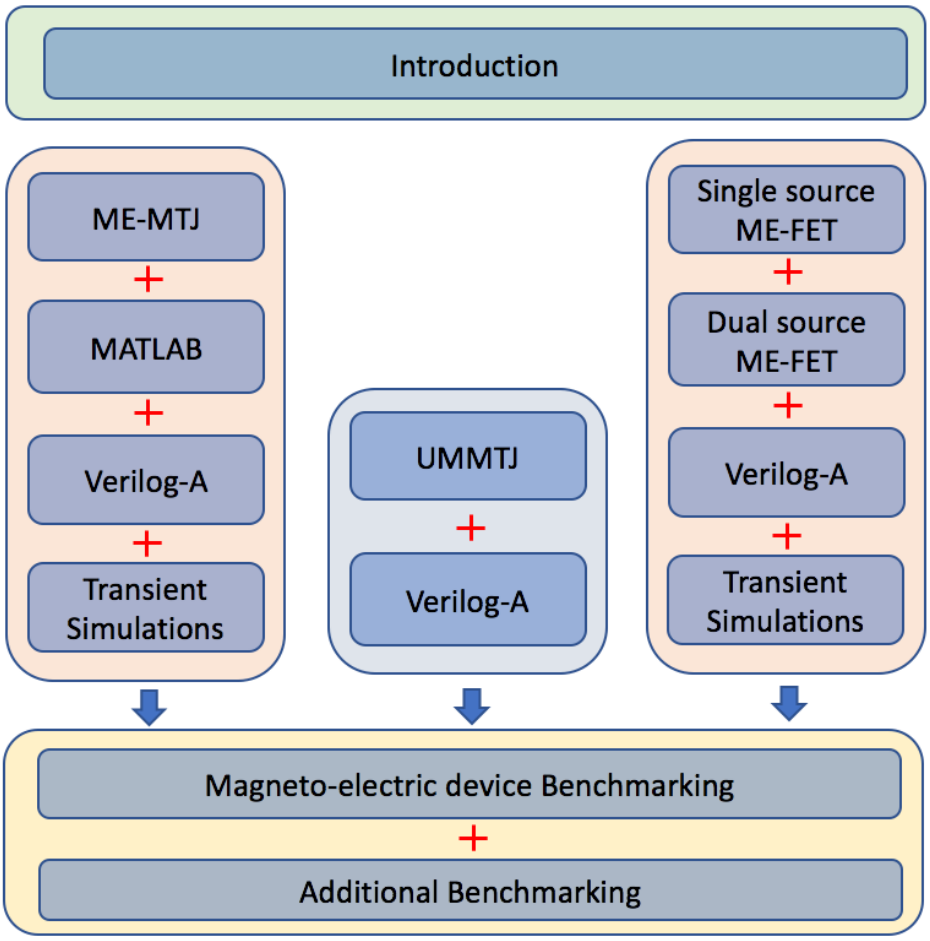

Figure 1.2: Organization of the study.

CHAPTER 2

MAGNETO-ELECTRIC MAGNETIC TUNNEL JUNCTION[1, 2, 3, 4, 5, 6, 7, 8]

2.1 ME-MTJ Device

An interesting beyond-CMOS device that has been proposed to take advantage of voltage controlled magnetism (VCM) is the Magneto-electric Magnetic Tunnel Junction (ME-MTJ) [31], [50,51,53]. This device utilizes voltage controlled exchange bias in heterostructures which uses a magneto-electric antiferromagnet (ME AFM) exchange coupled with a ferromagnetic (FM) layer [6-8,28,31,32,34,37,49,52,68]. This device is constructed around a common Magnetic Tunnel Junction (MTJ) stack consisting of two FM (i.e., the 'free' and 'fixed') layers that are separated from each other by a thin tunnel insulator as shown in Figure 2.1(a) [69]. Here, the lower ferromagnet has its magnetic state pinned by the exchange bias generated by the underlying non-ME AFM, forming the so-called 'fixed' electrode. The magnetization of the upper 'free' FM is also determined by the exchange bias produced by an antiferromagnetic (AFM) film, but in this case this film is very different in nature to that used to fix the magnetization of the lower fixed FM.

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While the lower (non-ME) AFM produces a permanent pinning of the fixed layer's magnetism, the ME AFM is formed from chromia (Cr_2O_3), whose boundary magnetism can be controllably reversed to switch the magnetic state of the free electrode [47].

In one approach, it is possible that the bias magnetic field (H) needed for the ME switching may be provided by the fringing fields emanating from the free FM itself. With a typical value of ~ 10^2 Oe, this would result in a manageable switching Electric field (E) of ~10^4 kV cm^{-1}=1 Vμm^{-1}; reversing the direction of this E- field, in the presence of the fixed bias H- field, the free layer will then similarly undergo magnetic reversal. The principle of using chromia to generate reversible exchange bias in a nearby ferromagnet has been demonstrated previously in experiment (see, for example [46,47]), and is illustrated schematically in Figure 2.1(b).

This depicts the situation considered in [46], where the authors used the exchange bias generated by a chromia substrate to modulate the hysteresis curves exhibited by a Co/Pd multilayer stack. In Figure 2.1(b), blue (solid) and red (dotted) lines represent the hysteresis loops of the stack, measured for different boundary magnetization conditions in the chromia. Switching between these hysteresis loops is controlled by the polarity and strength of the E- field applied across the chromia layer. By reversing the direction of the E- field applied across the chromia, the direction of its boundary magnetism is reversed, resulting in a measurable change.

Figure 2.1(c) shows the exchange coupling between the ME and free FM layer. In order to achieve ME reversal, it is necessary that it simultaneously be subjected to a combination of H and E fields, with an EH product that exceeds a critical value in the range of 10^6 kV-Oe cm^{-1} [29,46,70]. This phenomenon allows an innovative approach to the switching of MTJs, using a voltage

controlled switching mechanism that avoids the need to drive energetically-costly currents (as in the spin transfer torque (STT) mechanism). Dependent upon the relative orientation of the magnetization (parallel versus anti-parallel) of the two FM layers, the resistance of the tunnel junction is determined (low versus high, respectively).

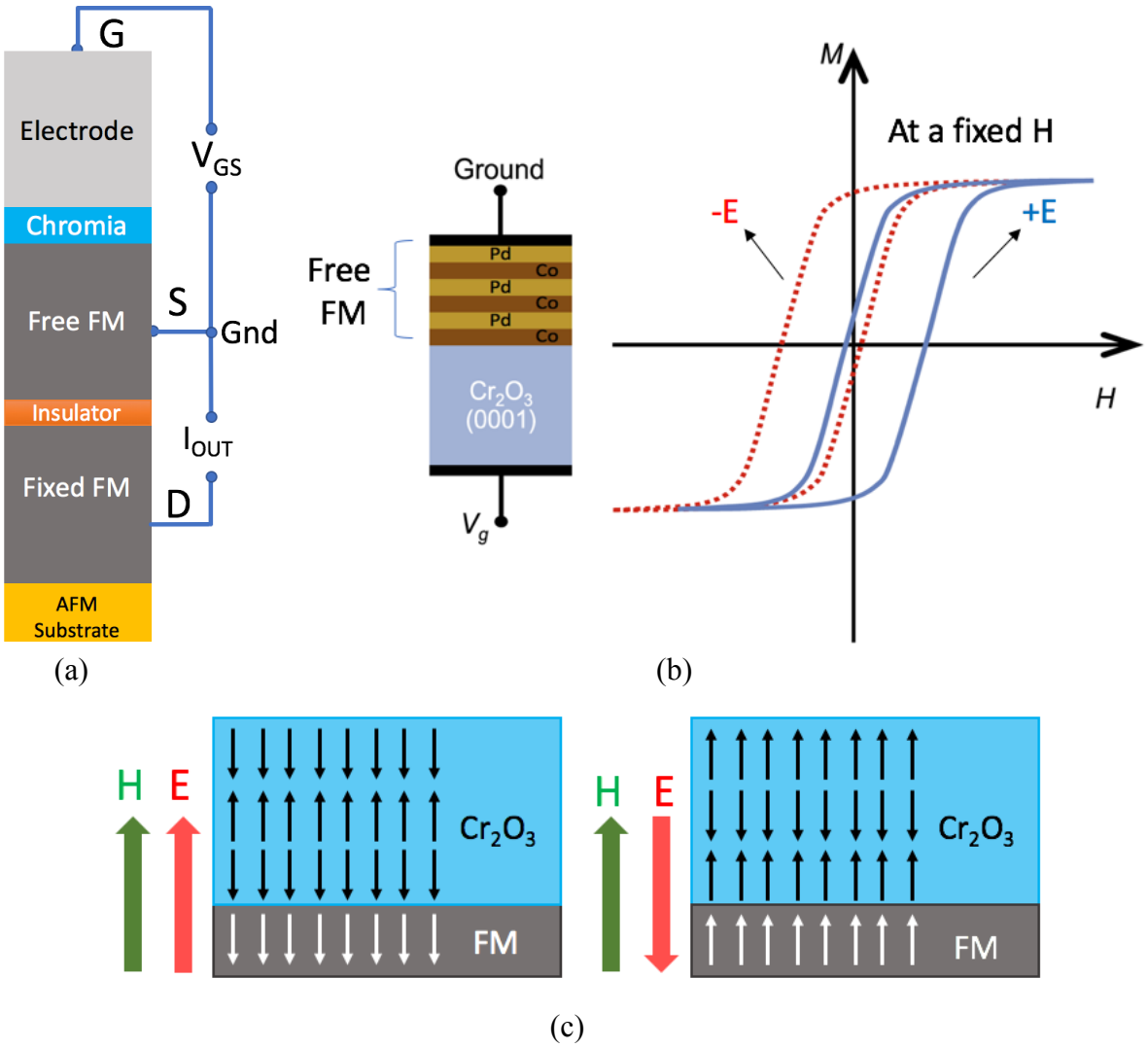


Figure 2.1: (a) Schematic layer structure of the ME-MTJ proposed by Binek and Doudin [29] and later by Bibes and Barthelemy [53]. (b) Schematic illustration of the experiment of [46]. (c) Exchange coupling between chromia and free FM layer. © IOP Publishing 2016

The resistance state represents the state variable of the device, i.e., low resistance represents a bit "0" and high-resistance represents bit "1". Changes in the relative magnetization of the two FMs, induced by switching the direction of the boundary magnetism at the chromia surface, can therefore be detected as a change in the tunneling resistance across the MTJ cell shown in Figure 2.1(a). The voltage-driven switching scheme thus described, introduces three-terminal transistor functionality to the MTJ, a device that has traditionally been restricted to two-terminal operation. The output characteristics of this device correspond to that of an inverter, or buffer, the CMOS equivalent of which requires two CMOS components rather than the single ME-MTJ used here. The electric field induced switching of the magnetic state that is central to the operation of the ME-MTJ has already been demonstrated in a number of experimental studies [30,46-49].

2.2 Additional ME-MTJ Concepts

Two new device concepts in which feature the voltage controlled boundary magnetism of the ME-MTJ have also been proposed: The ME-MTJ majority/minority gate and the exclusive-NOR (XNOR)/exclusive-OR (XOR) gate.

2.2.1 ME-MTJ Majority/Minority Gate

This device has been proposed previously for spin based logic, since it may be cascaded into larger circuits without the need to convert information from spin- to charge-based forms at every input or output [7]. In its simplest form, the majority gate consists of three separate inputs, the majority of which "win" to impose their value on the output. A spin-majority gate has been proposed previously [71] in which three separate MTJs are used to form the three logical inputs.

These devices are then coupled through a common FM base layer to a fourth MTJ, which forms the output of the logic gate. The majority function in this geometry arises from the fact that the magnetization of the base layer is determined by the majority of the inputs [71], and that base layer forms the free FM of the output MTJ.

While this scheme yields logical outputs consistent with a majority gate, in this work, we developed a much simpler implementation as shown in Figure 2.2(a). This exploits the properties of ME domains in chromia to achieve the majority gate function. In contrast to the structure of Figure 2.1(a), the ME layer of this device is influenced by three different inputs that are biased at separate voltages V_{g1}, V_{g2} & V_{g3}. Chromia is known to exhibit a sharp threshold switching of its boundary magnetization under the action of an external electric field [46-49,70]. Moreover, these experiments have shown that the reversal of boundary magnetization in suitably small areas may be induced by forcing the local E- field in some nanoscale region to exceed the critical value required for switching.

By seeding a domain in which the local magnetization has been reversed in this manner, the reversal rapidly propagates across the entire area of the film. The single domain limit has been measured experimentally and has been found to be around a micron [49], a value consistent with the micromagnetic requirements of the devices [56]. As with the ME-MTJ, readout of the logical states of the majority gate is achieved by determining the MTJ tunnel resistance. The full truth table for the majority gate is indicated in Figure 2.2(a). The layout of the ME-MTJ majority gate, constructed using standard scaling rules [7,8] is indicated in Figure 2.2(b). The total area required for this gate is 45 F^2 (where F is the critical feature size) and is assumed to be 15 nm for most of the current work.

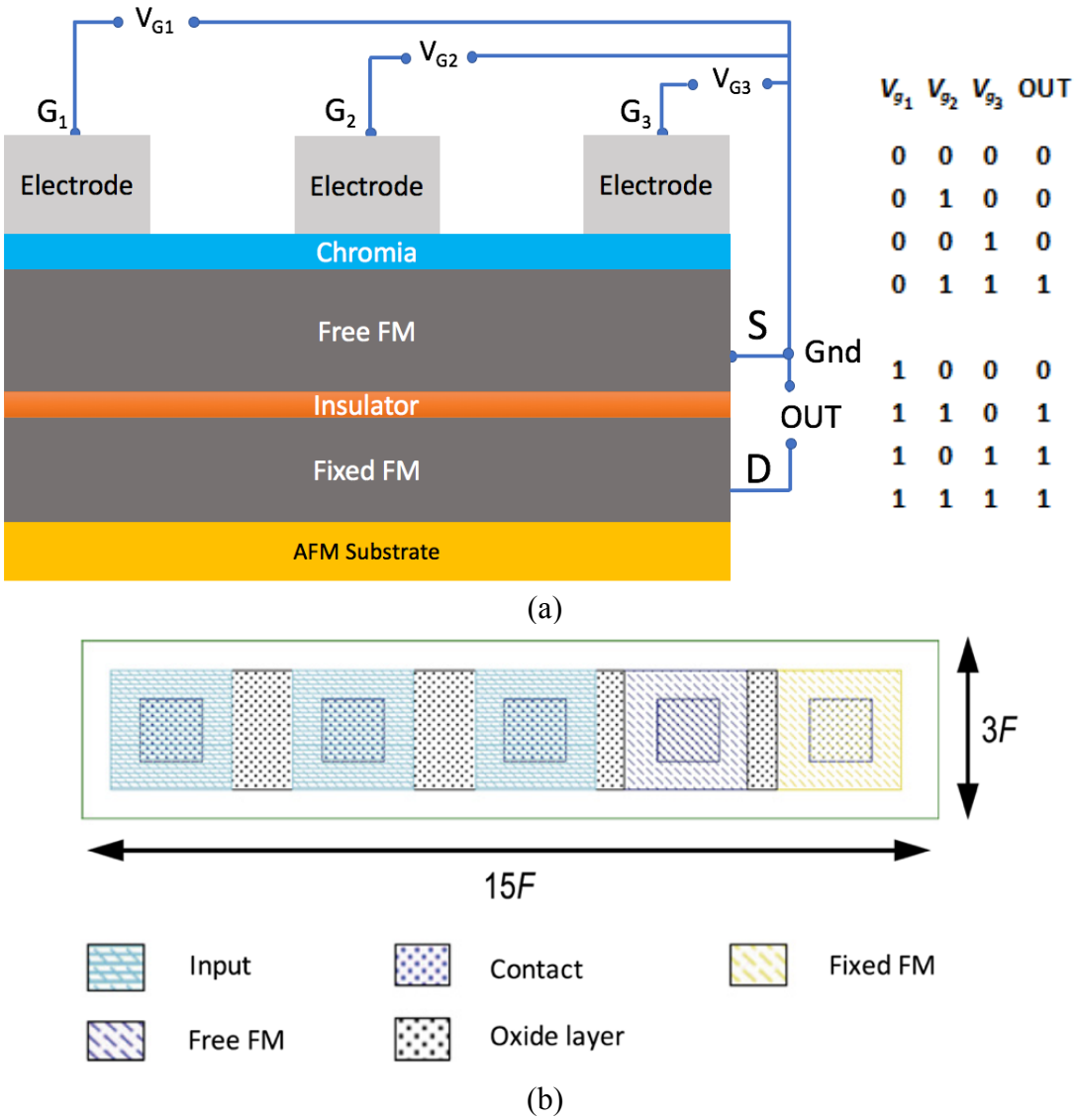


Figure 2.2: (a) Schematic illustration of a majority gate implemented using a single MTJ and its truth table. (b) Layout for the ME-MTJ majority gate. © IOP Publishing 2016

This compares favorably to the larger area requirement of 64 F^2 estimated for the STT-MRAM majority gate implementations [7]. The compact size is achieved as a result of being able to arrange the three inputs in a linear design, in which the chromia layer extends completely under all three of these electrodes.

By extension, the same device may also function as a NAND or NOR gate, by holding one of the inputs at either "0" or "1" and then separately varying the other two inputs. The inverse functions of the majority gate, AND and OR can be constituted by reversing the fixed FM layer spin state.

2.2.2 ME-MTJ XNOR Gate

In another variation, the ME-MTJ may also be used to realize an exclusive-NOR (XNOR) gate. This is achieved by modifying the MTJ geometry as indicated in Figure 2.3(a). This shows that the main modification has been to replace the passive AFM layer that pins the fixed FM in Figure 2.1(a) with a separate ME layer.

The modified device therefore has two ME layers, the exchange bias generated by each of which is determined by the separate voltages V_{g1} & V_{g2}. In the case where the polarity of these two inputs is opposite (i.e., "1" & "0" or "0" & "1"), the magnetization of the two FMs will be parallel, leading to low MTJ resistance and an output state of "0". For similar inputs (i.e., "0" & "0" or "1" & "1"), however, the opposite holds; the two FMs will be anti-parallel alignment and MTJ resistance will be high (logic level "1"). Functionally, the behavior is similar to a CMOS XNOR gate (see the truth table in Figure 2.3(a)).

XNOR to XOR Operation

The device function can switch from XNOR to XOR operation based on the presence of either a single, common magnetic field or individual field dominating the direction of spin vectors in both the top and bottom chromia layers shown in Figure 2.3(b).

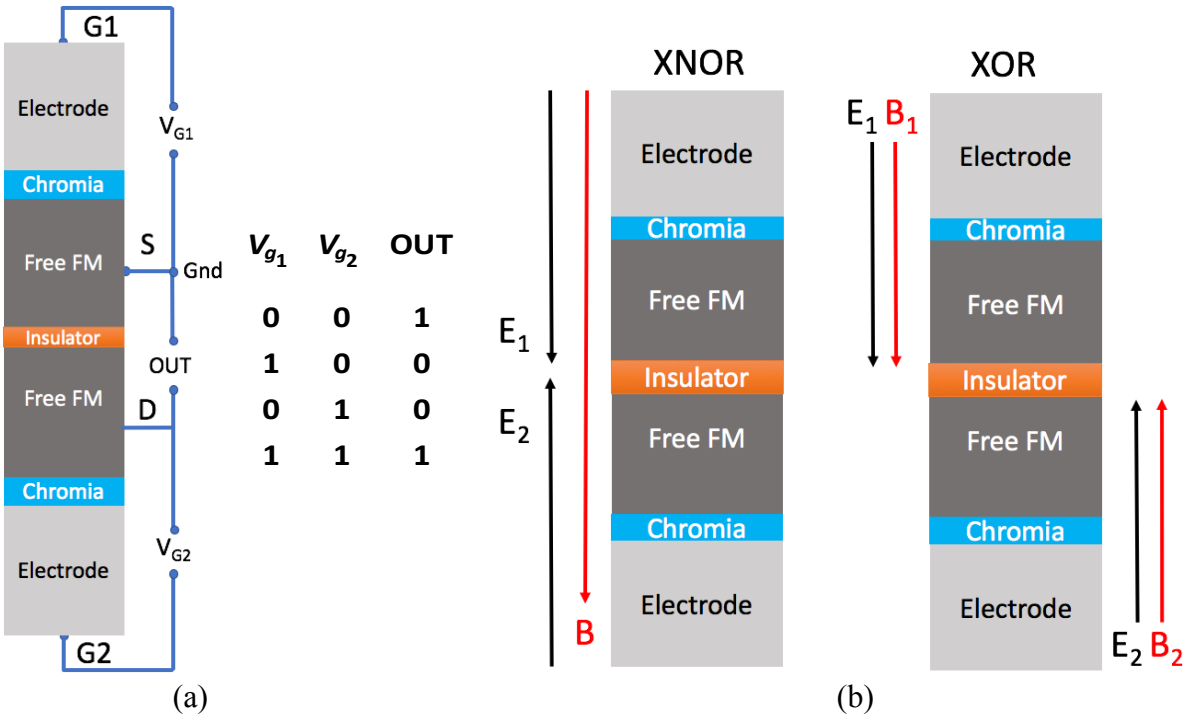


Figure 2.3: (a) XNOR/XOR gate structure implemented with a ME-MTJ in which both the free and fixed ferromagnetic electrodes are programmed by means of their own ME layers (controlled by the voltages V_{g1} & V_{g2}). The truth table for XNOR operation is also indicated. (b) ME-MTJ based XNOR and XOR gate. © 2017 IEEE

In the XNOR gate, a single magnetic field, B, exists across the device whereas in the XOR gate, there are two separate magnetic fields, B_1 and B_2 to influence the spin vector orientation of the chromia layers. The electric fields, E_1 and E_2, in both cases correspond to the two inputs applied across the top and bottom chromia layers. For the transient simulations, we have assumed the XNOR gate operation.

2.3 MATLAB Model

In this section, the features of the MATLAB model are described. As previously mentioned, these allow energy-delay analysis of the different ME devices. The energy associated

with switching of the ME-MTJ, and the total switching time are determined by separately analyzing the contributions from sections 1-3 in Figure 2.4(a) and the small signal model in terms of resistances and capacitances shown in Figure 2.4(b).

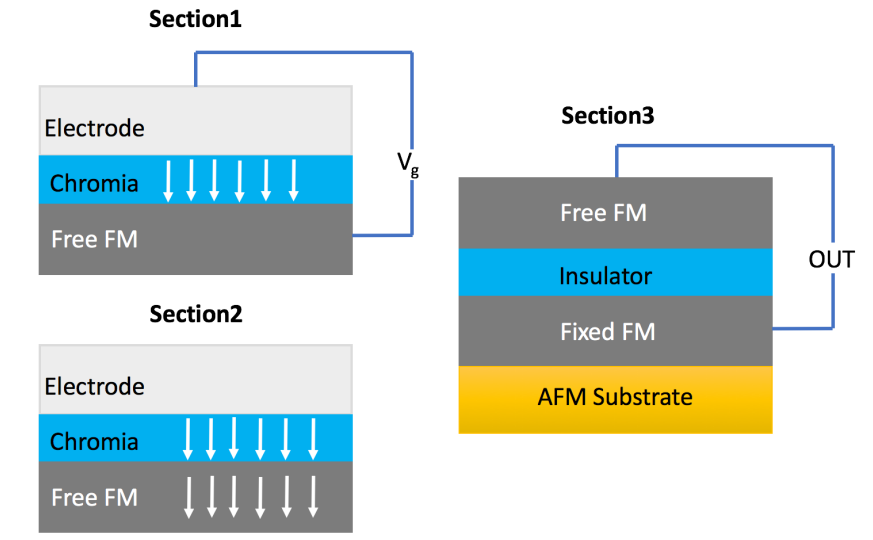
Section 1 is the 'electric-to-magnetic' conversion takes into account the physical phenomenon at the input to the device. Through ME coupling, the electric field associated with this voltage induces a change in magnetization with the chromia layer. The switching of the boundary magnetization accompanies the reversal of the magnetic ordering in the bulk shown in Figure 2.4(a). Within the bulk of the ME this reversal involves the two different sub-lattices that produce the AFM order.

This is described in terms of charging of an RC-capacitor network, in which the capacitance is the ME layer ($C_{ME} = \varepsilon_{ME}\varepsilon_0 A/t_{ME}$), where ε_{ME} is the dielectric constant of the ME layer of thickness (t_{ME}) and A is the cross-sectional area of the device) and the resistance (R_{in}) is the load of the driving stage. The RC-constant associated with this capacitor ($\tau_{ME} = R_{in}C_{ME}$) defines a transient charging current $I_{ME} = C_{ME}V_g/\tau_{ME}$, where V_g is in the range of 100 - 200 mV for sufficiently thin films. In this way, the energy cost associated with the electric-to-magnetic conversion step can be computed as:

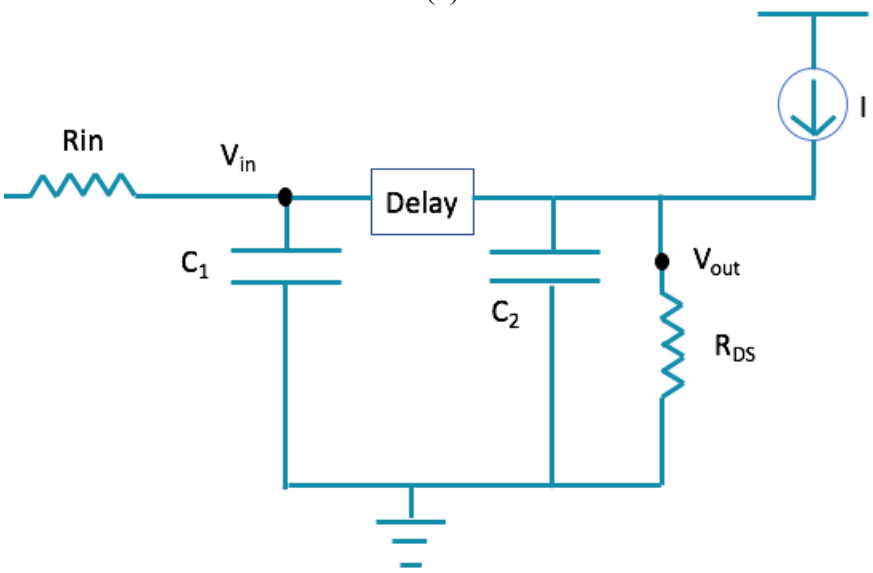
$$E_{ME} = \frac{1}{2} C_{ME} V_g^2 \quad (1)$$

The next section is the 'magnetization transfer' stage in which the induced boundary magnetism in chromia causes a rotation of the magnetization throughout the free FM and generates an exchange bias that reverses the magnetization of the free FM as shown in Figure 2.4(a). This

stage represents the most uncertain aspect of the compact model, that there is presently little that is known experimental data about this problem.



(a)



(b)

Figure 2.4: (a) Breaking down the ME-MTJ into its key physical processes. (b) Small signal model of the ME-MTJ device. © IOP Publishing 2016

In the absence of detailed experimental results, a reasonable estimate for the time (τ_{xfer}) is made. τ_{xfer} is considered to be 200 ps, a value that is smaller than the experimental switching speeds (~500 ps) of some STT magnetic MTJ devices [72], but consistent with the estimate of 178 ps in [9]. This estimate does not, however, consider the passive influence of Gilbert damping, a process that may add significant viscous drag [73] to the ME domain-wall motion. It has been proposed that the domain-wall velocity should be limited to a maximum value $v_{max} = \gamma H \lambda_o/4$, where γ is the gyromagnetic ratio, γH is the free-electron spin-resonance frequency, with the length parameter λ_o related to the scale of the domain-wall width. In [49], this expression was used to estimate a velocity $v_{max} = 5$ nm/ns, implying a switching time of 2 – 3 ns for a device with a critical dimension of 15 nm. Since this significantly longer than the value of 200 ps indicated above, the estimates of the delay time should be interpreted with some caution until experimental results are available, in spite of the results of [9].

To determine the energy cost (E_{xfer}) associated with the magnetization transfer process we use:

$$E_{xfer} = \frac{V}{2}\mu_r \mu_0 H_c^2 \quad (2)$$

where μ_r is the relative permeability of the free FM, μ_0 is the permeability of free space, and V is the volume of the free layer. The field strength (H_c) in this relation is the interfacial magnetic field responsible for the magnetization rotation in the free FM and is calculated as [74]:

$$H_c = 2\frac{\sqrt{A_{AF}K_{AF}}}{M_{FM}t_{FM}} \quad (3)$$

where K_{AF} is the magnetocrystalline anisotropy of the antiferromagnetic magneto-electric, and A_{AF}, M_{FM} and t_{FM} are the exchange stiffness, magnetization and thickness, respectively, of the free FM.

The final process illustrated in Figure 2.4(a) (see section 3) is known as 'electrical readout of the relative alignment of the two ferromagnetic layers'. In this stage, electrical readout of the MTJ is performed as a means to detect the relative alignments of the pinned and free FMs in the MTJ in the form of resistance change. To determine the energy cost associated with this stage of the device it is again treated as a capacitor-charging problem in which the relevant resistance now involved is dominated by that of the MTJ. For a parameterization of the resistance of the MTJ, the resistance (R_{P}) when the magnetization of the two FMs is parallel is written as [75]:

$$R_P = \frac{t_{Ox}}{FA\varphi^{0.5}} e^{1.025\varphi^{0.5}t_{ox}} \quad (4)$$

where t_{ox} and φ are the thickness and the potential-barrier height of the (Magnesium oxide) MgO MTJ dielectric layer, A is the cross-sectional area of the device and F is a factor that is calculated from the resistance-area product of the junction. This parameter is material dependent, and is assumed to be 332 based on [75]. With the resistance for parallel magnetizations defined this way, the resistance (R_{AP}) of the MTJ with anti-parallel magnetization of the two FMs is expressed as [75]:

$$R_{AP} = R_P(1 + TMR) \quad (5)$$

where, TMR is the tunneling magnetoresistance. It is noted that the readout current (I_{OUT}) shown in Figure 2.4(a) is governed by a time-constant (τ_{OUT}) that can be expressed as $\tau_{OUT} = R_{Av}C_{MTJ}$. Here, $R_{Av} = \frac{1}{2}(R_P + R_{AP})$ is the average resistance of the MTJ and $C_{MTJ} = \varepsilon_{MTJ}\varepsilon_0 A/t_{MTJ}$ is its capacitance (with ε_{MTJ} dielectric constant of the MTJ insulator). With these various parameters defined, the readout current is easily calculated as $I_{OUT} = (C_{MTJ}V_{OUT})/\tau_{OUT}$ while energy cost associated is:

$$E_{OUT} = C_{MTJ} I_{OUT} \tau_{OUT} \ . \quad (6)$$

While Eqs. (1) – (6) describe the energy cost associated with switching of the MTJ, another factor that must be considered is that of "off-current" leakage. The small value of the TMR (~10) in realistic MTJs means that even in their high-resistance state they can still consume significant power. This is very different to CMOS, where one transistor in any inverter pair is typically in a highly-resistive off-state. To account for dissipation in the MTJs we consider a circuit driven at a fairly typical frequency of 1 GHz. Assuming a 4-phase clocking scheme, the leakage energy reduces significantly and is calculated as:

$$E_{Leak} = \frac{1}{4}\frac{V_{OUT}^2}{R_{Av}} T \quad (7)$$

Where T = 1 ns is the period of the 1 GHz signal.

Table 2.1 lists the key parameters of the model, together with the values assigned to them in the calculations. A comment should be made here on the magnetic properties of the free FM,

we require this to exhibit perpendicular magnetic anisotropy to match the direction of the out-of-plane boundary magnetization of the chromia. For a free FM layer thickness of 30 nm meeting these anisotropy requirements will likely require the use of a magnetic multilayer, such as Co/Pd [76] or Co/Pt [77].

The modeling approach is easily adapted to the analysis of devices such as the majority gate of Figure 2.2(a) and the XNOR gate of Figure 2.3(a). For the majority gate, the only difference with the ME-MTJ model lies in the first stage of electric-to-magnetic conversion, where the gate voltage is now applied to three separate electrodes. At the same time, a slightly higher voltage is required for each of these electrodes in order to be able to induce the collective switching of the chromia that provides the majority gate function. Similarly, for the XNOR/XOR gate, we now have two-input stages as a result of replacing the fixed FM with an additional, ME-controlled, free layer. The effect of this additional gate stage is easily incorporated into the calculations, by replicating the stages of electric-to-magnetic conversion and magnetization transfer for the two inputs.

2.4 Verilog-A Model

This section describes the Verilog-A modeling approach. Figure 2.5 shows the parameters used to model the device at each stage. Similar to the modeling scheme shown in Figure 2.4(a), the ME-MTJ device is modeled as having three sections namely ‘quasi electric-to-magnetic conversion’, ‘boundary magnetization to magnetization change’ and ‘electrical readout of magnetic layer alignment’.

Table 2.1: Key parameters used in compact model of the ME-MTJ. © IOP Publishing 2016

Parameter	Value	Description of Parameter and units
A	900 nm^2	Area of ME-MTJ stack
A_{AF}	8.4 x 10^{-12} J/m	Exchange stiffness [78]
ε_{ME}	12	Dielectric constant of chromia [70]
ε_{MTJ}	9.90	Dielectric constant of MTJ dielectric (MgO) [79]
φ	0.4 eV	Potential-barrier height of the MTJ tunnel dielectric [80]
K_{AF}	10^{-6} J/m^3	Magnetocrystalline anisotropy of AFM layer [81]
M_{FM}	0.456 x 10^6 A/m	Perpendicular magnetization of FM layers [75]
$\mu_r\mu_o$	4	Permeability of the free FM [9]
R_{in}	1100 Ω	Load resistance from driving stage and interconnects
T	1 ns	Time period of the 1-GHz clocking signal
t_{FM}	30 nm	Thickness of the free FM layer [47]
t_{ME}	10 nm	Thickness of the ME layer
t_{MTJ}	2 nm	Thickness of the MTJ dielectric (magnesium oxide)
TMR	10	Tunneling magnetoresistance
V	$A \times t_{Free}$	Volume of the free FM layer
V_g	0.1 V	Voltage applied across ME layer

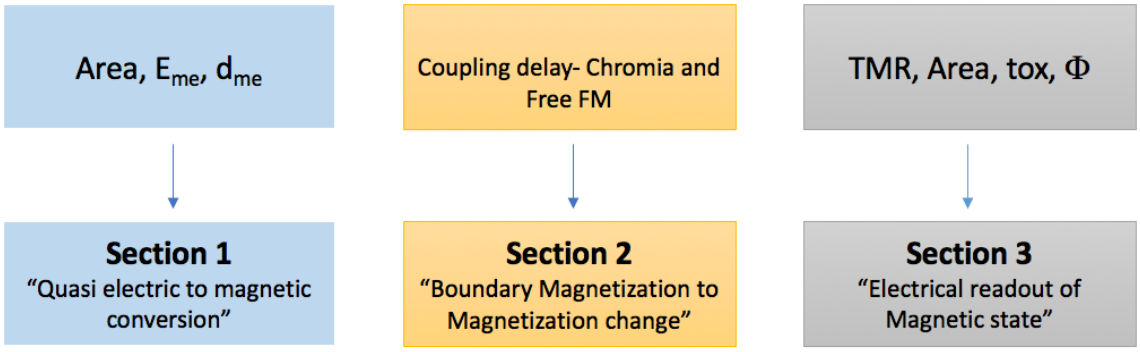


Figure 2.5: Input parameters to the sections of the ME-MTJ device. © 2017 IEEE

Section 1 comprises the electrode, chromia and the free FM layer. The modeling is described in terms of the charging of an RC-capacitor network, in which the relevant capacitance is that of the ME layer ($C_{ME} = \varepsilon_{ME}\varepsilon_0 A/t_{ME}$, where ε_{ME} is the dielectric constant of the ME layer of thickness t_{ME} and A is the cross-sectional area of the device) and the resistance (R_{in}) the load of the driving stage on the input. When a voltage difference is applied between the electrode and the free FM, the capacitor charges up.

Through magneto-electric coupling, the electric field associated with this voltage induces a change in magnetization with the chromia layer and, eventually, if sufficiently high, reverses the polarity of the boundary magnetism at the interface with the free FM. The threshold voltage (V_{ME}) at which the spin vectors in the chromia layer switches is assumed to be 50 mV. It is also assumed that the chromia spin vectors switch instantaneously when the applied voltage exceeds V_{ME}. The RC-constant associated with this capacitor defines a transient charging current I_{ME}, where V_g should be in the range of 100 – 200 mV for sufficiently thin films.

$$\tau_{ME} = R_{in} * C_{ME} \quad (1)$$

$$I_{ME} = \frac{C_{ME} * V_g}{\tau_{ME}} \quad (2)$$

Section 2 accounts for the coupling delay between chromia and the free FM layer. The coupling time is taken as 200 ps, keeping in line with the assumption for the MATLAB based model. Section 3 comprises the magnetic tunnel junction. As described above, it is the stack of a free ferromagnetic layer and a fixed ferromagnetic layer sandwiching a tunneling oxide layer (here, MgO). Electrical readout of the MTJ is achieved by passing a current through the cell. This section is modeled as a capacitor-charging problem in which the relevant resistance now involved is dominated by that of the MTJ. This has similarities to the MATLAB based model.

Here, the bias voltage is taken to be 110 mV and the initial TMR is assumed to be 10. Since the output is read from the MTJ device as a change in resistance, the bias voltage dependent TMR model is taken into account as well. Based on experimental results, the TMR decreases with read bias voltage [75]. The model accounts for the MgO barrier tunnel resistance described in [75]. The physical model of the tunnel junction conductance is described in [82]. The MTJ cell uses a CoFeB/MgO/CoFeB layer structure because of the large TMR values [24], that includes the possibility of retaining the necessary perpendicular anisotropy that can occur with CoFeB [83-84]. The exchange biasing of chromia with CoFeB is under investigation. Some of the Equations and modeling of Verilog-A model bears similarities to similarities to the MATLAB models. Nevertheless, we describe this again since several equations are added in this model.

For parameterization of the resistance of the MTJ, the resistance (R_P) when the magnetization of the two FMs is parallel is written as [75]:

$$R_P = \frac{t_{Ox}}{FA*A*\varphi^{0.5}} e^{1.025\varphi^{0.5}t_{ox}} \quad (3)$$

$$TMR_0 = \frac{R_{ap}-R_p}{R_p} \quad (4)$$

$$TMR_{real} = \frac{TMR}{1+\frac{V_b^2}{V_h^2}} \quad (5)$$

where t_{ox} is the thickness of the MTJ dielectric layer, assumed to consist of MgO. ϕ is the potential-barrier height of the tunnel dielectric, A is the cross-sectional area of the device and F is calculated from the resistance-area product of the junction. The value of this parameter is material dependent, and in these simulations we use a value of 332 based on [75] as used in the MATLAB model. With resistance for parallel magnetizations defined this way, the resistance (R_{AP}) of the MTJ with anti-parallel magnetization of the two FMs is expressed as [75]:

$$R_{AP} = R_P(1 + TMR_{real}) \quad (6)$$

Using the resistances defined in Eqs. (3) & (6), the readout current (I_{OUT} in Figure 2.1(a)) across the two FMs is governed by a time-constant (τ_{OUT}).

$$R_{AV} = \frac{(R_P+R_{AP})}{2} \quad (7)$$

$$\tau_{OUT} = R_{Av} * C_{MTJ} \quad (8)$$

$$C_{MTJ} = \frac{\varepsilon_{MTJ}*\varepsilon_0*A}{t_{MTJ}} \quad (9)$$

Here R_{Av} is the average resistance of the MTJ and C_{MTJ} is its capacitance (with ε_{MTJ} dielectric constant of the MTJ insulator). With these various parameters defined, the MTJ capacitance is easily calculated as C_{MTJ}.

2.4.1 Physical Modeling of the ME-MTJ Derived Devices

As with the MATLAB model, the approach here is easily adapted to the analysis of devices such as the majority gate (Figure 2.2(a)) and the XNOR gate (Figure 2.3(a)). For the majority gate, the only difference with the ME-MTJ model lies in the first stage of electric-to-magnetic conversion, where the gate voltage is now applied to three separate electrodes. As with the MATLAB model, a slightly higher input is required for each of these electrodes in order to be able to induce the collective switching of the chromia that provides the majority gate function.

The majority gate switching works on the principle of averaging. If the average of all the voltages applied to three inputs exceeds the V_{ME}, then the spin vectors are aligned in the favored direction (upwards). Conversely, if the applied voltage exceeds the threshold voltage in the negative regime ($-V_{ME}$), the spin vectors are aligned in the other favored direction (downwards). The switching of the ME layer electrically involves the charging/discharging of a capacitor, therefore the model includes a capacitor at each input.

$$C_{ME} = \frac{\varepsilon_{ME} * \varepsilon_0 * A}{3 * t_{ME}} \quad (10)$$

Similarly, for the XNOR/XOR gate, there are two-input stages as a result of replacing the fixed FM with an additional, ME-controlled, free layer. The effect of this additional gate stage is

easily incorporated into the calculations, by replicating the stages of electric-to-magnetic conversion and magnetization transfer. Since the XNOR device has two chromia layers exchange biased with two free ferromagnetic layers, there are two additional sections ('quasi electric-to-magnetic conversion' and 'boundary magnetization to magnetization change') in the Verilog-A model to account for the additional input. Sun's model [45] for minimum write time in the MTJ cell was not included since the coupling delay is dominant and also there is a clocking system which is adjusted externally. The leakage energy is estimated by:

$$E_{Leak} = \frac{1}{4}\frac{V_{OUT}^2}{R_{Av}}T \quad (11)$$

2.4.2 Read and Write Circuit

Figure 2.6 shows the ME-MTJ device with pull-up and reset transistor. A sensing component is used to read the resistance change in the MTJ cell. A p-channel metal oxide semiconductor (PMOS) transistor with a clocked input is used as the sensor for our analysis to sense the output electrically. Since the input of this device is clocked, the output can be either asynchronously or synchronously read depending on the requirement and fed into the next stage. There is a requirement for another active component for multi-stage circuit, i.e., the reset at the output which pulls down the node to a negative voltage. This is because the chromia spin vectors switch at either '+EH' or '-EH' product with H kept constant.

If a pull-down transistor is not used, due to unipolar voltages obtained at the output, the switching condition for negative input condition is not met thus giving incorrect output based on

the memory in the system. The reset transistor thus resets the state of the system to enable switching for a multi-stage system. The scheme described requires the use of a negative power supply for reset which is active prior to clocking sequence. It may be either a global reset or separate reset signals for each stage.

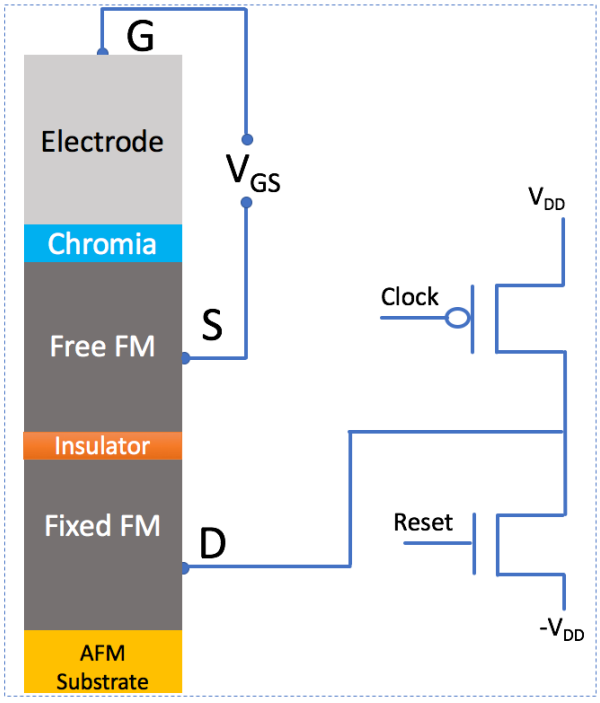


Figure 2.6: ME-MTJ device with a pull-up and reset transistor at the output node.

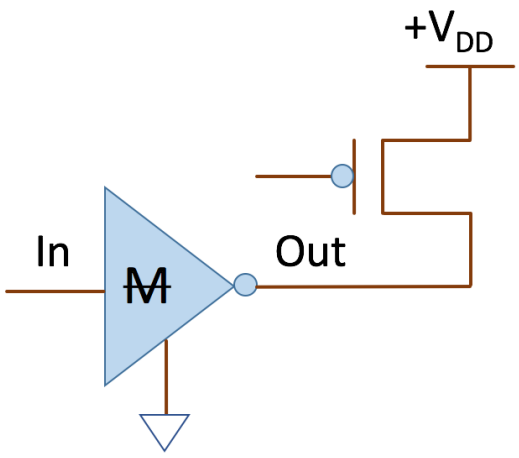
2.5 Circuit Design and Simulation Results

The set of Verilog-A models and associated symbols were integrated for use with the Spectre simulator. The simulation results have been compared to those from MATLAB modeling of the device and similar results are obtained. DC and transient simulations have been performed for each device to ensure model efficiency and accuracy.

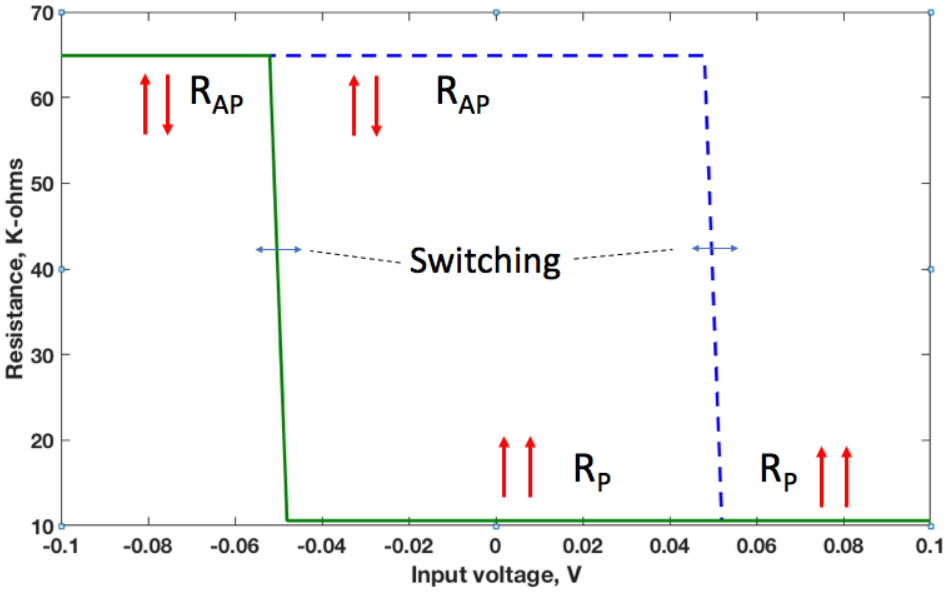
2.5.1 Digital Circuit Design

2.5.1.1 ME-MTJ Inverter

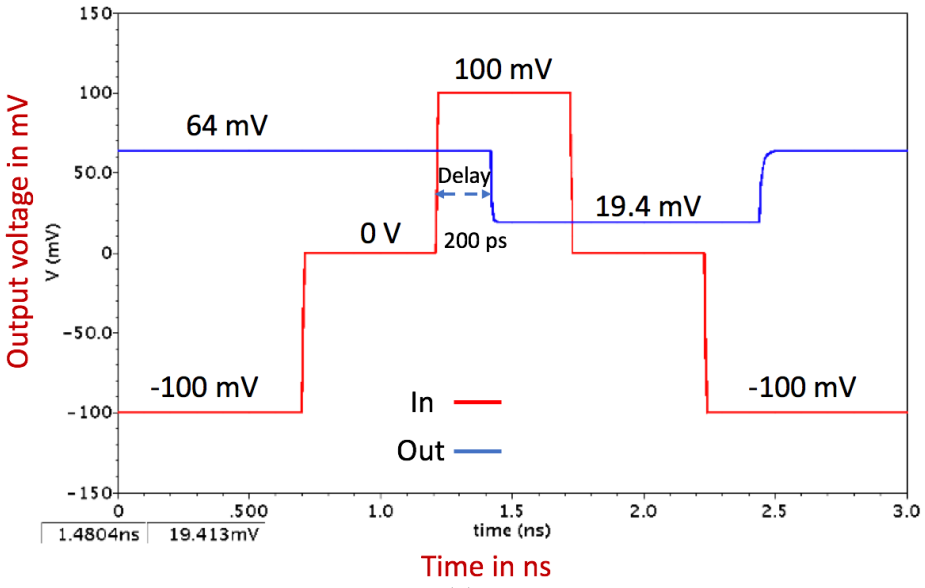
Figure 2.7 shows the circuit schematic, the DC and the transient behavior of the ME-MTJ inverter. The schematic consists of a ME-MTJ device along with the read transistor (Figure 2.7(a)). The input (in) is designed for operation between ~+0.1/-0.1 V, and V_{ME} is taken to be +/-50 mV. DC simulation validates the static behavior of the device in Figure 2.7(b). The spin state in the FM layer switches from parallel (P) to anti-parallel (AP) at $-V_{ME}$ and from AP to P state at $+V_{ME}$. The current through the circuit follows a hysteresis curve, as different input voltages are applied, indicating inherent memory in the system. For the transient simulations shown in Figure 2.7(c), the initial state is assumed to be high (~64 mV). As the voltage is ramped up from -100 mV to 100 mV, the cell switches from high to low at V_{ME} (+50 mV) and the output voltage (out) is 19.4 mV.



(a)



(b)



(c)

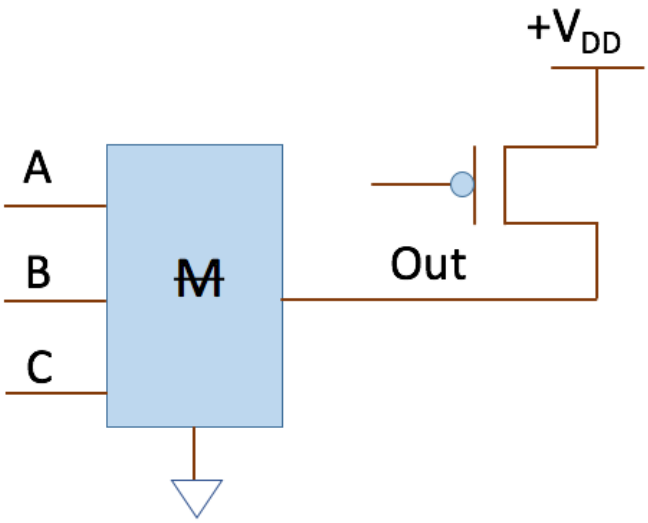
Figure 2.7: (a) Circuit schematic, (b) DC simulation and (c) transient simulation of the ME-MTJ inverter. © 2016 IEEE

Conversely, the output voltage goes high when the input signal is below $-V_{ME}$ (-50 mV). The P and AP state currents obtained are 987 nA and 1.83 µA respectively. The output voltages

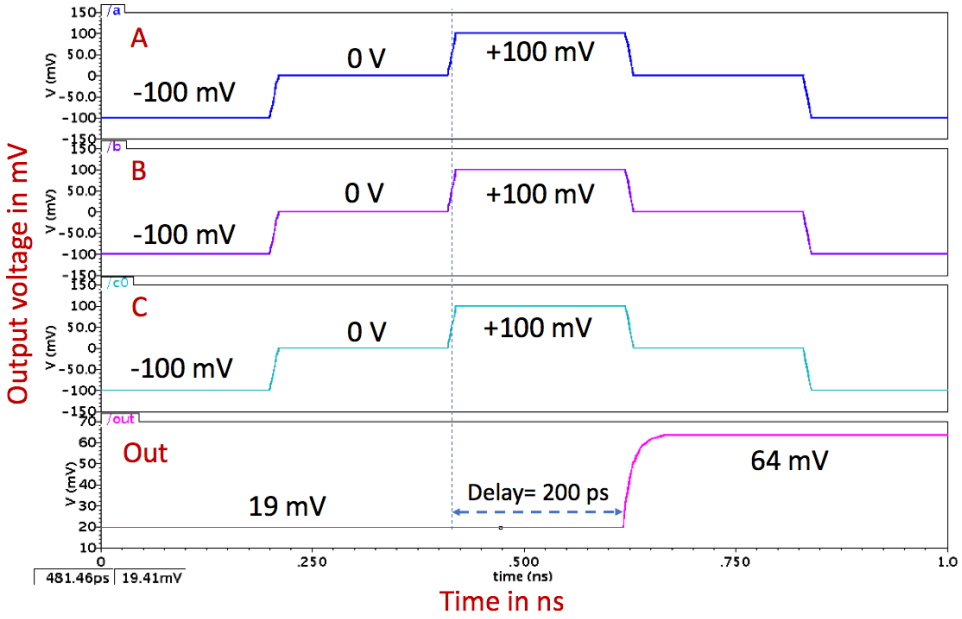
representing the actual transition voltages for high and low states are 64 mV and 19.4 mV respectively.

2.5.1.2 ME-MTJ Majority Gate

The circuit schematic and transient simulation results of a ME-MTJ majority gate is shown in Figure 2.8. As with the ME-MTJ inverter, the input voltages here range from -100 mV to 100 mV. As shown in Figure 2.8(b), the state of the system is low (19 mV) initially. When at least two of the inputs go high, the output switches to the high (63 mV) state after a coupling delay of 200 ps. The ME-MTJ majority gate is used to design the adder and thus serves as a useful gate. As mentioned above, various logic gates like NAND and NOR can be derived from this gate by fixing one the three inputs at a low and high voltage respectively.



(a)



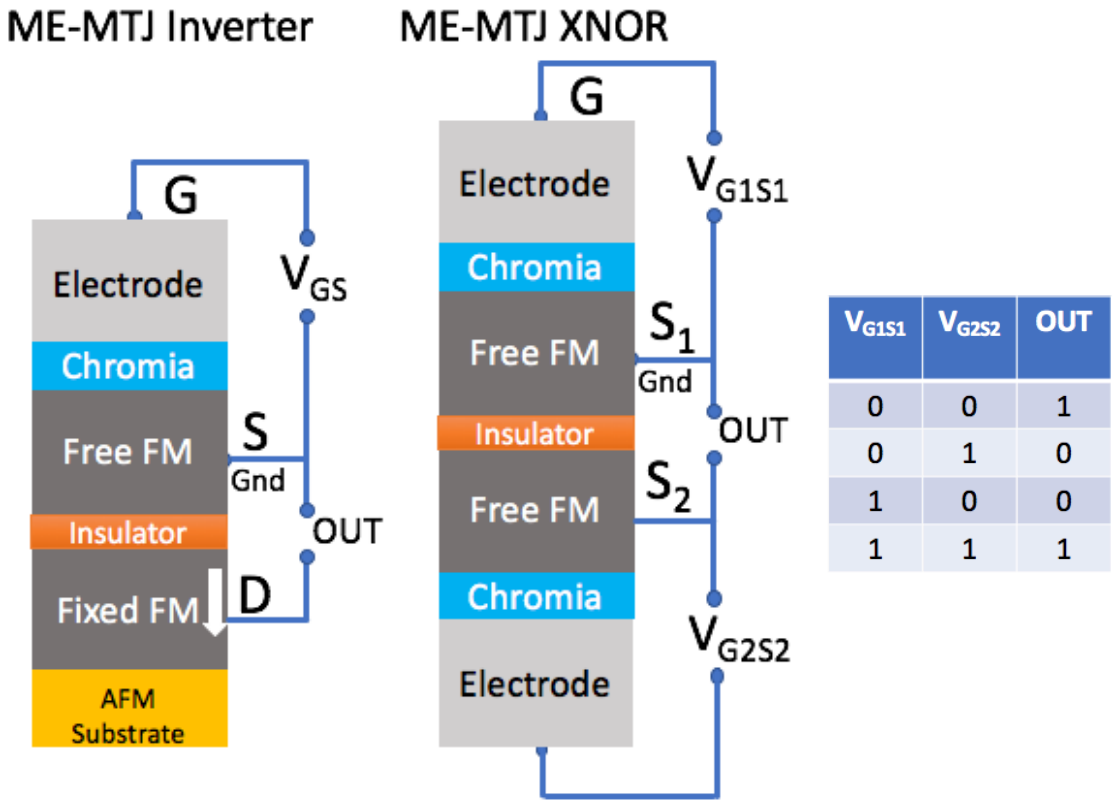
(b)

Figure 2.8: (a) Circuit schematic and (b) transient simulation of the ME-MTJ majority gate. © 2016 IEEE

2.5.1.3 ME-MTJ XNOR/NOR Gate

As previously described, a ME-MTJ XNOR gate may also be derived from the ME-MTJ structure shown in Figure 2.1(a) [85]. It consists of two chromia layers capping individual free FM layers (top FM and bottom FM) shown in Figure 2.9. The chromia layers are used to change the magnetization of the FM layers through exchange bias [53] and the spin vectors in the FM layers are free to switch depending on the polarity of inputs applied. The terminals of the XNOR device are marked as 'S_1/D', 'S_2', 'G_1' and 'G_2'. 'S_1/D' and 'S_2' are the top and bottom free FM layer (Figure 2.9).

In the original configuration, the source terminal is connected to ground, the input is applied between the gate ('G') and drain ('D') terminal and the output is taken across drain ('D') and source ('S') terminal in Figure 2.1(a). In this device, one of the free FM layers ('S_2') is grounded and the output is measured across the floating ('S_1/D') and grounded ('S_2') free FM layers. The device can also be designed such that the terminal 'S_1' is grounded and the output is measured from the bottom FM layer, i.e., 'S_2/D'.



V_{G1S1}	V_{G2S2}	OUT
0	0	1
0	1	0
1	0	0
1	1	1

Figure 2.9**:** Device structure of the ME-MTJ inverter (left) and ME-MTJ XNOR gate with the logic truth table. © 2017 IEEE

Operation of the XNOR Gate

Voltages are applied to two separate input terminals, i.e., the 'V_{G1S1}' and 'V_{G2S2}'. The bits "0" and "1" correspond to voltages -100 mV and +100 mV respectively. When a low voltage (-100 mV) is applied across the top chromia layer and a high voltage is applied across the bottom chromia layer, the spin vectors of the top chromia layer are oriented in 'down' direction resulting in the spin vectors of the free FM layer resulting in the 'down' spin orientation. The spin vectors of the bottom chromia layer are oriented in 'down' direction, resulting in the spin vectors of the free FM layer resulting in a 'down' spin orientation. Since the relative spin vector orientation of the free FM layers ('S_1' and 'S_2') is parallel, the current is maximum across the tunnel junction, thus resulting in a bit "0" at the output.

If, however, a low voltage is applied to both the input terminals, then spin vectors of the top chromia vectors are oriented in the 'down' direction, aligning the top free FM in the 'down' direction and the spin vectors of the bottom chromia layer are oriented in the 'up' direction, aligning the spin vectors of the bottom free FM in 'up' direction. The relative orientation of the free top and bottom FM is anti-parallel, resulting in a bit "1" at the output. This validates two of the cases in the XNOR truth table. Based on the voltages applied at the inputs, the entire truth table can be verified.

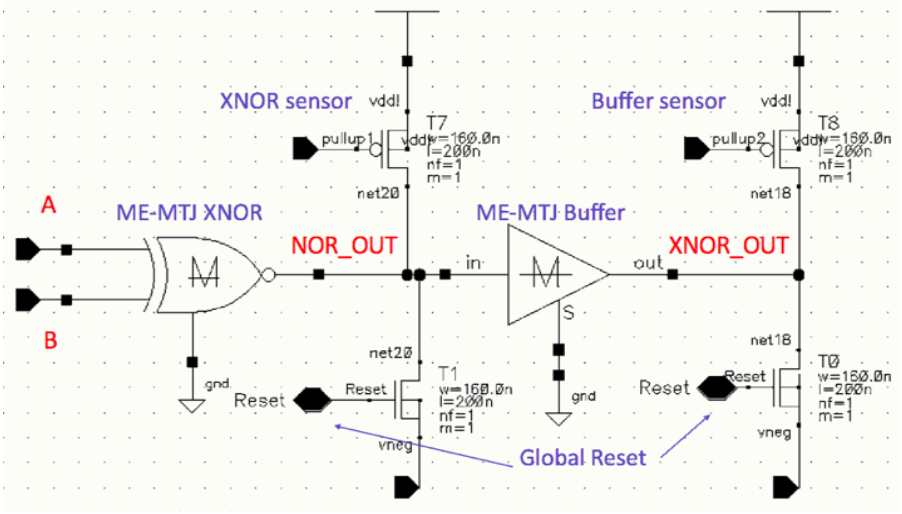
Operating the XNOR Gate as a NOR Gate

The ME-MTJ device as described, has the characteristics of an XNOR gate, but, unlike conventional logic, which has a fixed function, it is also possible for this device to operate as a NOR gate. The condition in which this occurs is as follows: When both inputs are high, the output

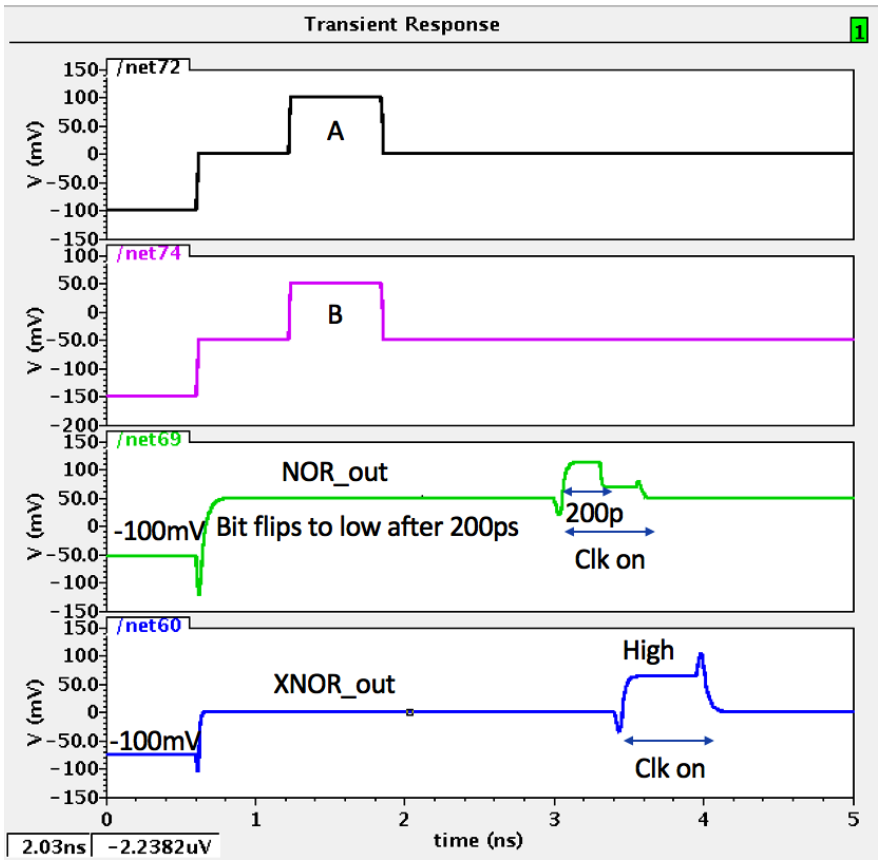
is also high. Since the top free FM ('D/S_1') is floating, when the sense transistor is on to read the output node, while its input is grounded or floating, reverse bias is induced across the top chromia layer. In terms of the electric field across chromia, this condition is equivalent to a reset condition. The spin vectors start to switch in the opposite direction after the coupling delay. Once the state is reset, the output switches, into a NOR function, so, if the state is captured soon after switching, the logic gate functions as an XNOR, but if left, the partial reset resets the state, resulting in the output being a NOR function. This dual-purpose gate function is validated in the simulations section using the Verilog-A based models [40].

The compact model and transient simulations verified the functionality of the models for the ME-MTJ XNOR/NOR gate and a 1-bit full adder. Figure 2.10(a) shows the schematic of the ME-MTJ XNOR/NOR gate. In the transient simulation results shown in Figure 2.10(b), both the inputs are varied between 0 V and +100 mV and a global reset signal is passed at the start of the cycle to enforce start-up condition. After the reset signal goes low, the inputs are sampled into the system.

When both the inputs ramp up from 0 V to 0.1 V, the output goes high, corresponding to the function expected from an XNOR gate. However, due to the reset condition across node 'A' and 'NOR_out', the output goes low after a delay of 200 ps. This corresponds to a NOR logic function. Alternatively, a ME-MTJ buffer can be added at the output to provide a known stabilized output to resolve the obtained state shown in Figure 2.10(b).



(a)

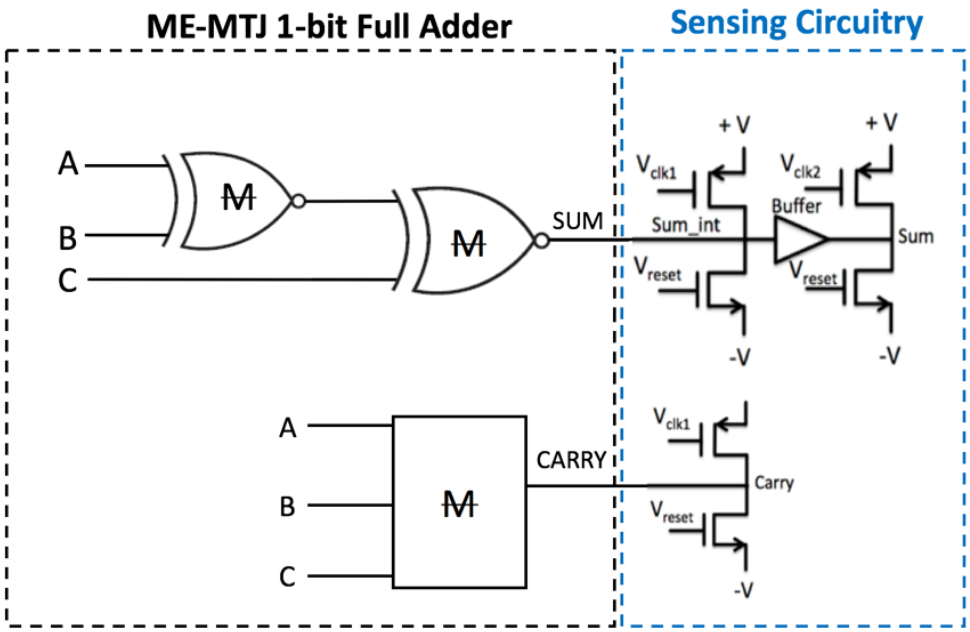


(b)

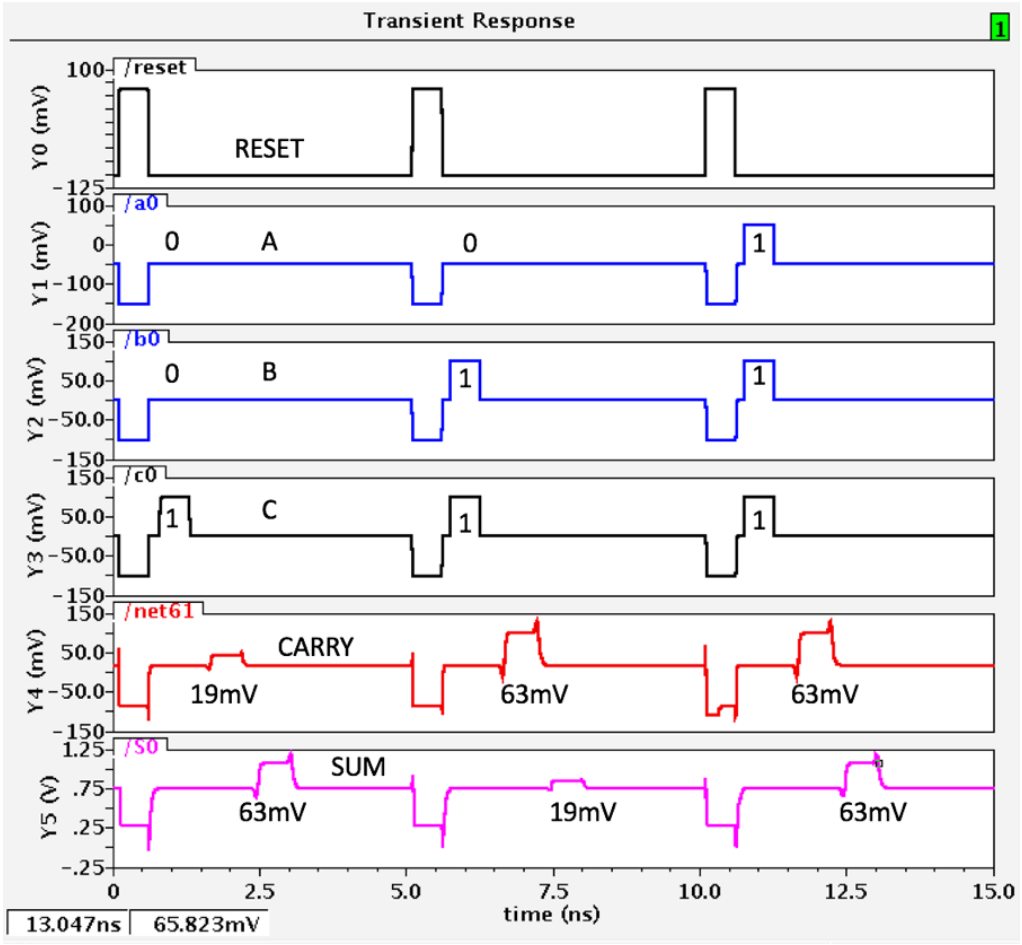
Figure 2.10: (a) ME-MTJ XNOR/NOR gate with the sense and reset circuitry and the additional ME-MTJ buffer to stabilize the output. (b) Transient simulation results of ME-MTJ XNOR/NOR gate. © 2017 IEEE

A potential concern with the implementation of the ME-MTJ XNOR gate described above is that it is assumed to have a symmetric structure, which may be difficult to realize in practice. More specifically, one might expect that the in-plane strain exerted on the lower chromia layer by the multilayer stack will differ from that exerted on the upper layer. The fact, however, is that the chromia lattice is rather stiff, so that interfacial conditions are unlikely to affect the exchange bias. More likely is an effect of interfacial strain on T_N, through a piezo-magnetic response [32]. Such an effect is again not expected to yield a pronounced effect upon the interfacial exchange bias.

2.5.1.4 ME-MTJ XNOR based 1-bit Full Adder



(a)



(b)

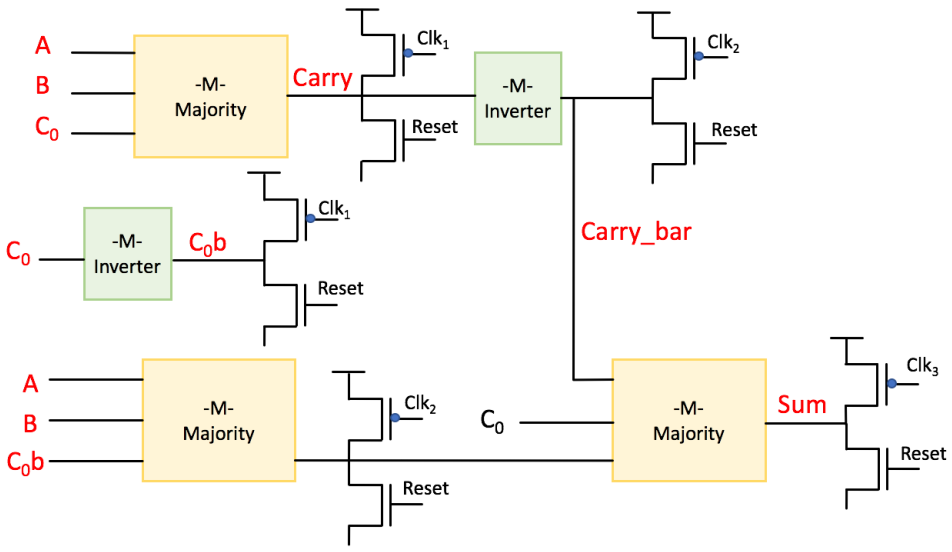
Figure 2.11: (a) Circuit schematic and (b) transient simulation of the ME-MTJ XNOR based adder. © 2017 IEEE

The ME-MTJ XNOR based 1-bit full adder is designed using a ME-MTJ based majority gate to provide the 'carry' function and two XNOR gates to provide the 'sum' function. Figure 2.11(a) shows the schematic for the full adder with a pair of CMOS transistors for read and reset operation as the sense circuitry. The critical path for the adder consists of a ME-MTJ majority gate. In Figure 2.11(b), three different input conditions are verified. For the condition, A=0, B=0 and C=0, the 'sum' and 'carry' signals reaches 63 mV (bit "1") and 19 mV (bit "0") respectively.

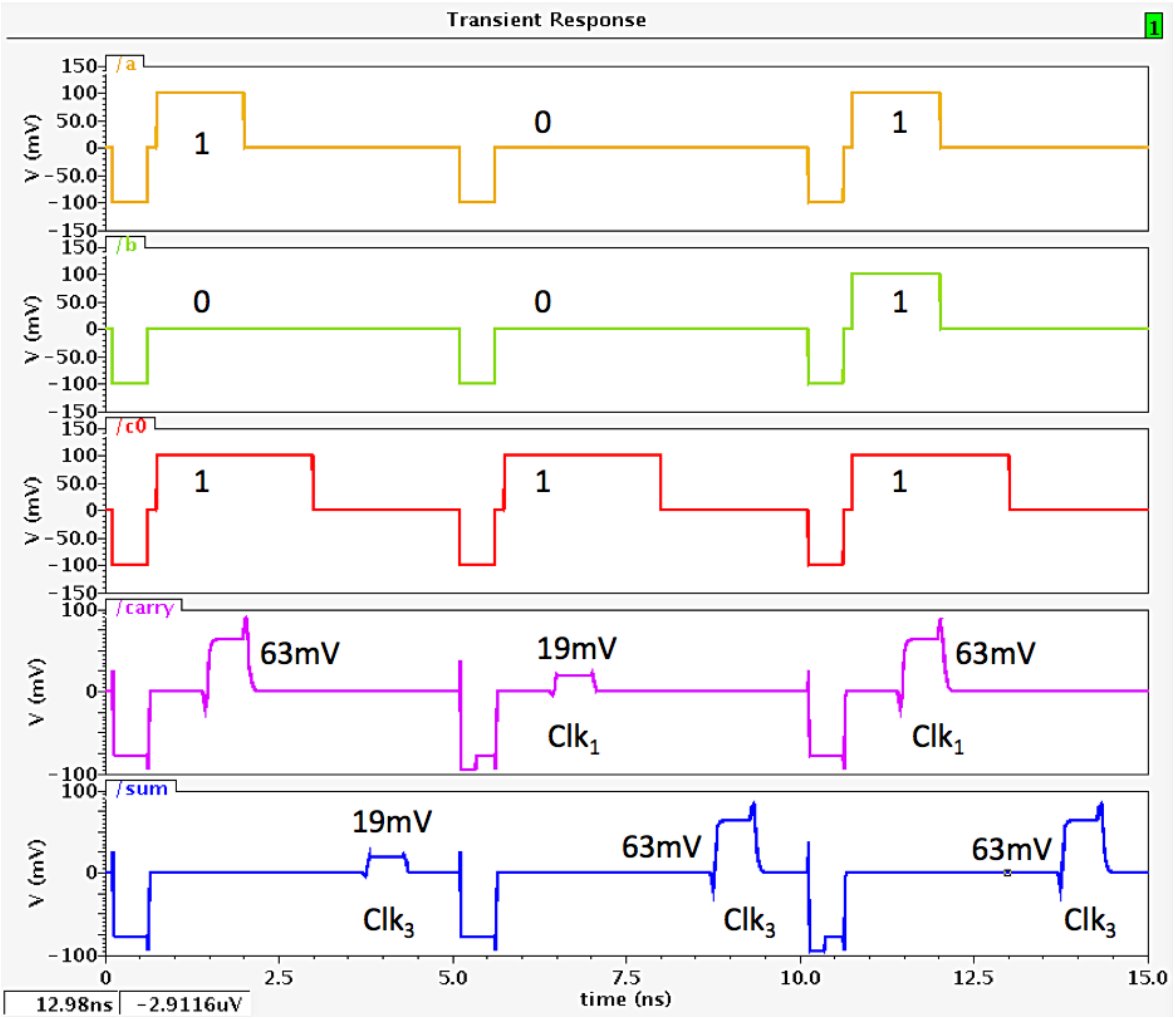
For A=0, B=1 and C=1, ‘sum’ and ‘carry’ are 19 mV and 63 mV. For these two cases, the ‘sum’ output is not susceptible to the input reset condition described earlier. The third condition, where all three inputs are high, the ME-MTJ XNOR is susceptible to feedback reset due to the field reversal across the chromia layer. This can be handled by the addition of the buffer to the output of the ‘sum’ function to add stability to the circuit and to give correct output as described above.

2.5.1.5 ME-MTJ Majority Gate based 1-bit Full Adder

Figure 2.12(a) shows the 1-bit full adder schematic with the sense and reset circuit. The clocking scheme includes four clock signals and one global reset signal at each node of the circuit to reset the memory. The ‘carry’ output is obtained at Clk_1 so the critical path is just one clock period/full adder and the ‘sum’ output is obtained at Clk_3. The transient simulation results for the 1-bit adder are shown in Figure 2.12(b).



(a)



(b)

Figure 2.12: (a) Circuit schematic and (b) transient simulation results of ME-MTJ majority gate based 1-bit full adder. © 2016 IEEE

2.5.1.6 ME-MTJ Majority Gate based 5-bit Full Adder

The 1-bit majority gate adder design can be extended to higher order bits [38]. The schematic of the 5-bit adder is shown in Figure 2.13(a). The 5-bit adder was chosen because it covers all the clocking phases needed to complete any bit length adder. The clocking scheme is shown in Figure 2.13(b) and consists of a 4-phase clock (Clk_0, Clk_1 and Clk_2) and global reset.

This is in contrast to the simulations above, where a 5-phase clock is used. Here, the Clk_3 signal is shared with the reset signal.

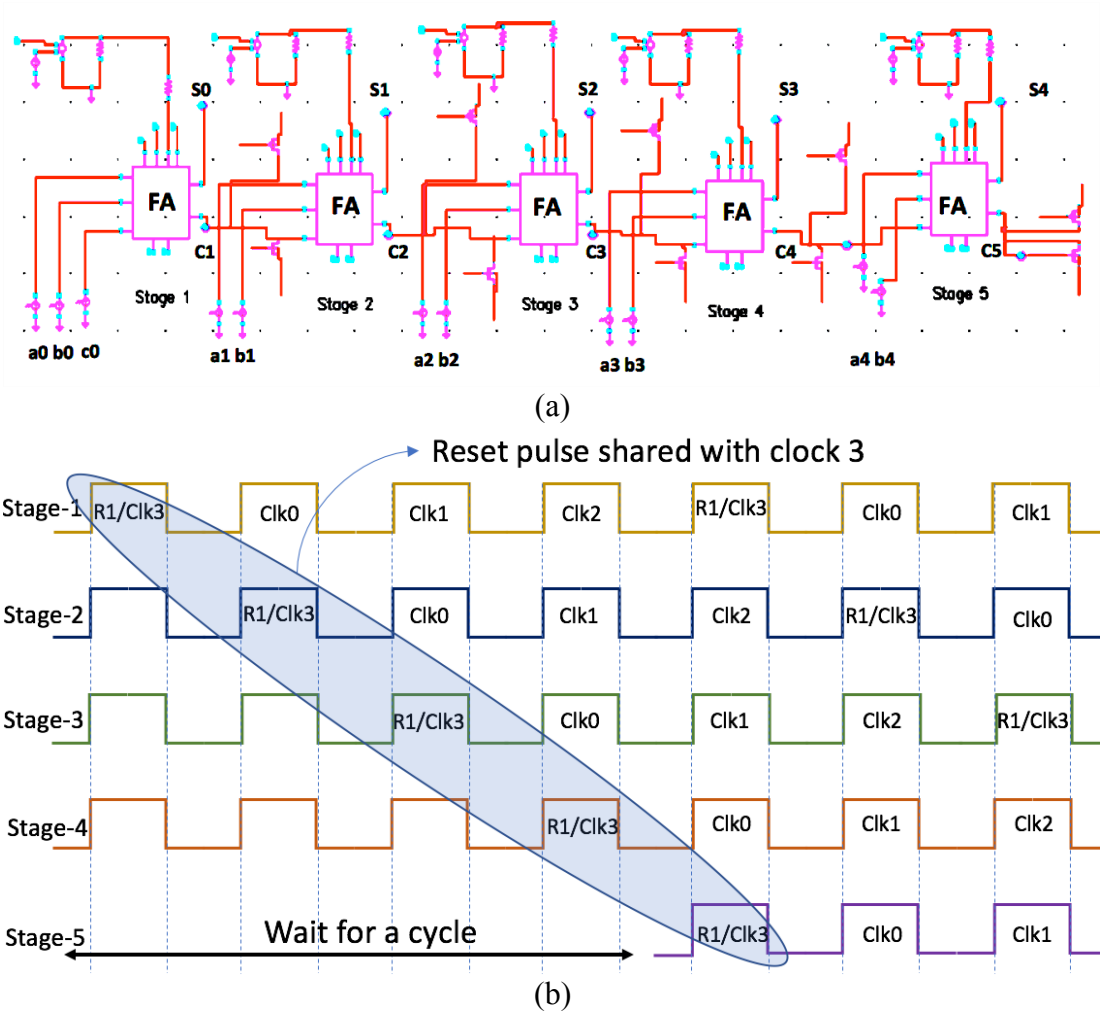


Figure 2.13: (a) Circuit schematic of ME-MTJ majority gate based 5-bit adder in Cadence Spectre. FA stands for ME-MTJ majority gate full adder. (b) 4-phase clocking scheme designed for the adder operation. © 2016 IEEE

As shown in Figure 2.14, the sampled input bits are a4,a3,a2,a1,a0=[0,0,0,0,0], b4,b3,b2,b1,b0=[1,1,1,1,1] and c0=1. The 'sum' and 'carry' output obtained is

s4,s3,s2,s1,s0=[0,0,0,0,0] and c5,c4,c3,c2,c1=[1,1,1,1,1]. Simulation results indicate that the ME-MTJ models can be used for more complex circuit design. Stage 5 is the time-delayed version of stage 1, and further stages can also be added in a similar way.

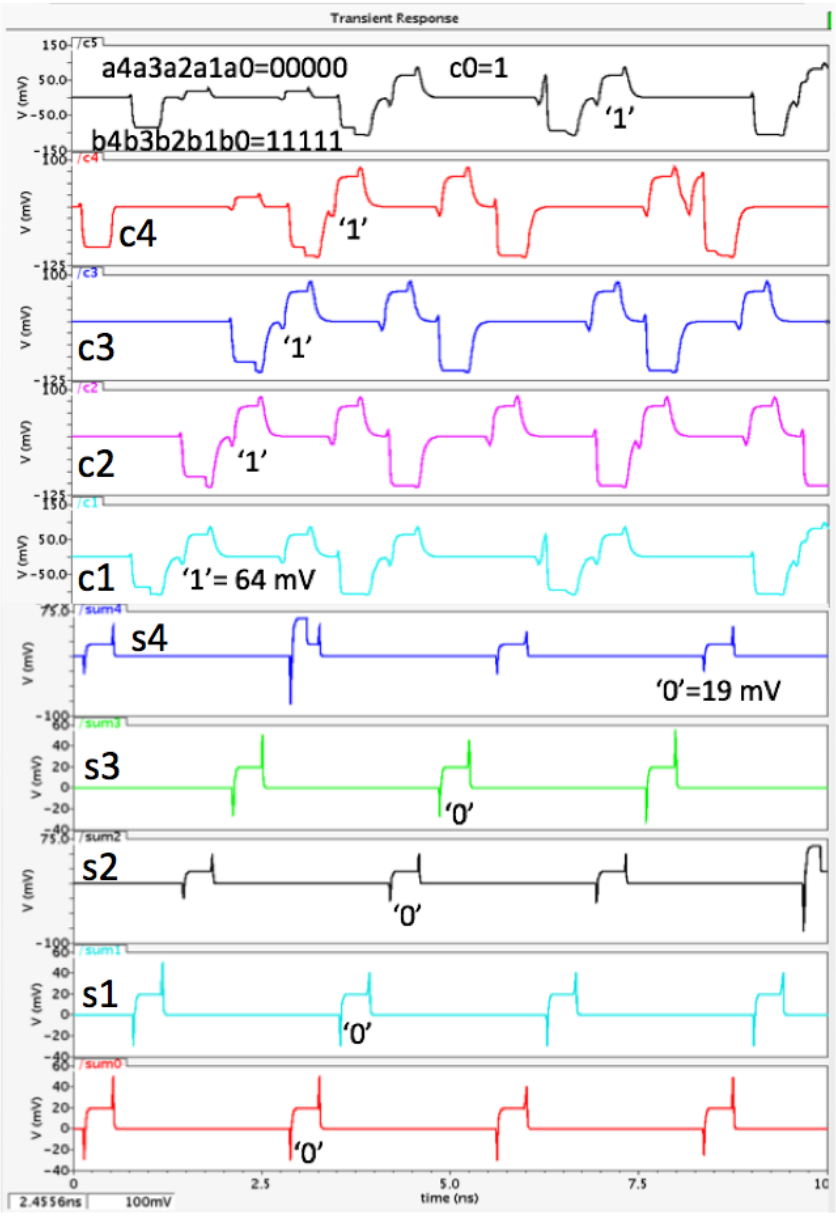


Figure 2.14: Transient simulation results of a 5-bit ME-MTJ full adder. © 2016 IEEE

2.5.1.7 ME-MTJ Ring Oscillator

A CMOS logic ring oscillator consists of an odd number of inverters connected in series to form a closed loop, with each inverter having an intrinsic propagation delay and an output after finite time period [86]. Three oscillators based on the ME-MTJ devices have been developed [42]. Each design has the ME-MTJ device and a resistive pull-up to read the output state. A level shifter is required at each stage and its voltage range depends on the type of ME-MTJ device used. the input reference voltage (V_{ref}) for the level shifter is taken as 50 mV and the output swings between 61 mV (bit "1") and 19 mV (bit "0").

2.5.1.7.1 ME-MTJ Buffer based Oscillator

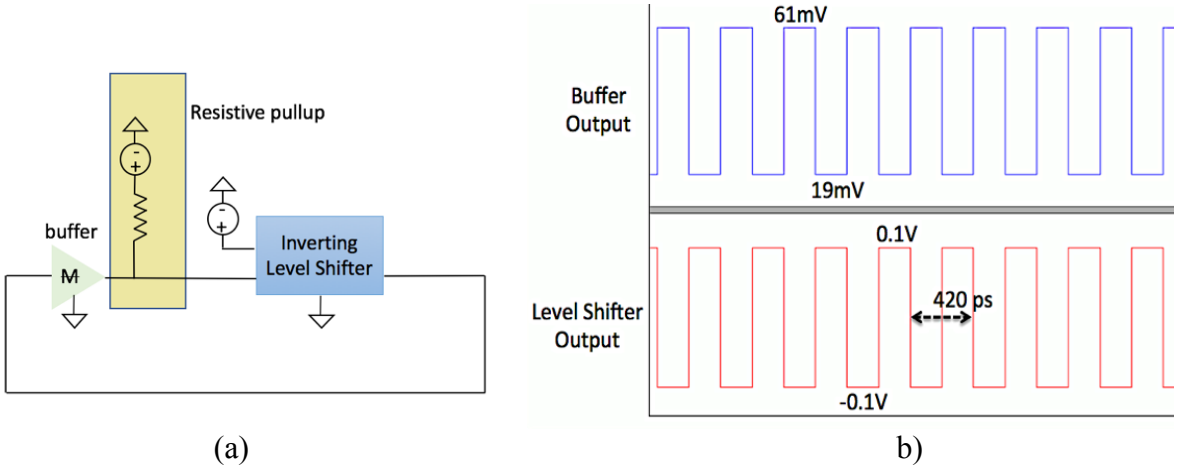


Figure 2.15: (a) Circuit schematic and (b) transient simulation results of the ME-MTJ buffer based oscillator. © 2017 IEEE

This oscillator is designed using ME-MTJ buffer with a resistive pull-up shown in Figure 2.15(a). The level shifter used here is an inverting type device that converts buffer's output

voltages varying between 19 mV and 61 mV to 100 mV and -100 mV respectively (Figure 2.15(b)). This is required in order to meet the essential ME switching criteria. The threshold voltage of the level shifter is assumed to be 50 mV. The period of oscillation achieved is 420 ps (Figure 2.15(b)).

2.5.1.7.2 ME-MTJ Majority Gate based Oscillator

In the ME-MTJ majority gate oscillator, one of the three inputs act as an 'enable' signal of the configuration and is tied to logic level equal to "1" as shown in Figure 2.16(a). The rest of the inputs are tied together to achieve a buffer function and are fed back from the output of the level shifter.

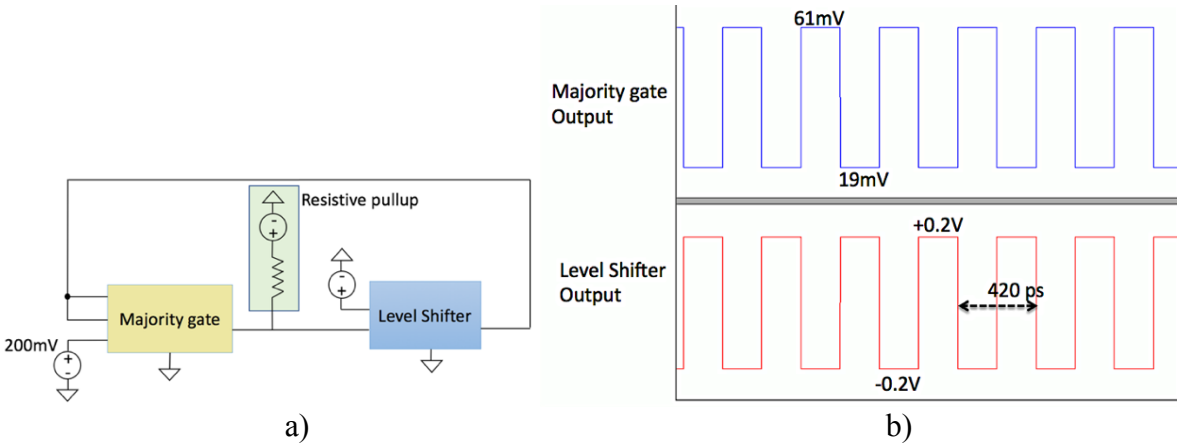
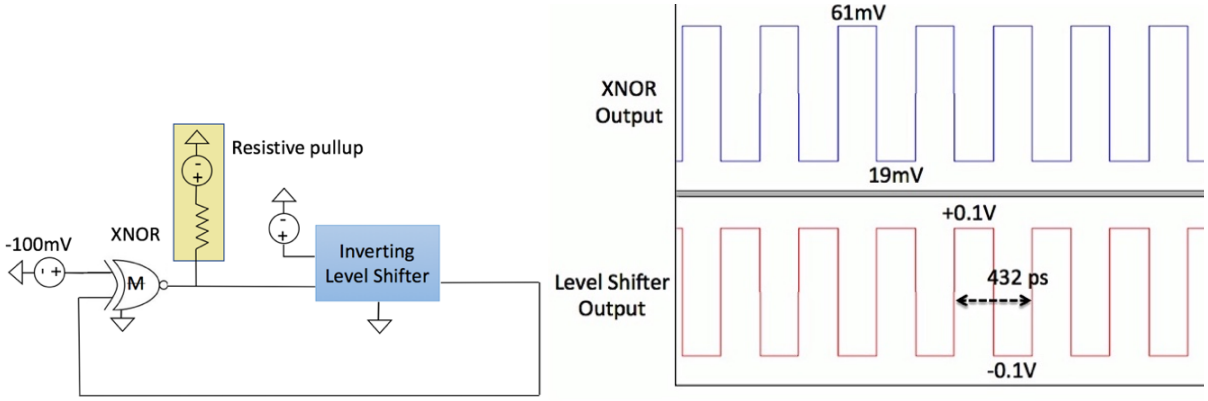


Figure 2.16: (a) Circuit schematic and (b) transient simulation results of the ME-MTJ majority gate based oscillator.

The level shifter is an inverting type that converts the majority gate's output voltages varying between 19 mV and 61 mV to +200 mV and -200 mV respectively, to enable switching for the next stage. The period of oscillation is 420 ps, which is dominated by the coupling delay between the free FM layer and chromia shown in Figure 2.16(b).

2.5.1.7.3 ME-MTJ XNOR Gate based Oscillator

In the ME-MTJ XNOR oscillator, one of the two inputs are tied to logic level "1", to achieve buffer functionality as shown in Figure 2.17(a). The level shifter is an inverting type that converts the XNOR gate's output voltages varying between 19 mV and 61 mV to +100 mV and -100 mV respectively. The level shifter switches between +100 mV and -100 mV, with a period of 432 ps, dominated by the coupling delay between the free FM layer and chromia similar to the majority gate oscillator (Figure 2.17(b)).



(a) (b)

Figure 2.17: (a) Circuit schematic and (b) transient simulation results of the ME-MTJ XNOR gate based oscillator.

2.5.1.7.4 ME-MTJ based 2-Stage Ring Oscillator

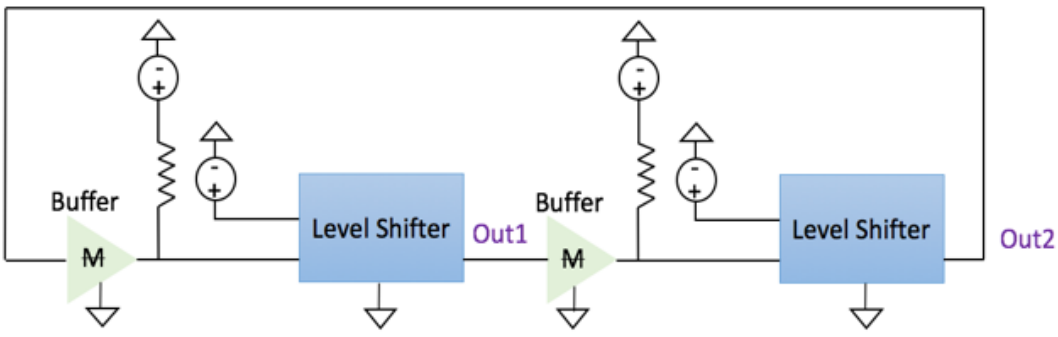
A 2-stage ring oscillator has been designed using the ME-MTJ buffers shown in Figure 2.18(a). The output oscillates since one of the level shifters has an inverting configuration. These are used to convert the voltage level from 61 mV and 19 mV to +200 mV and -200 mV respectively. The voltage range is higher since stage 1 and 2 outputs are used to trigger the majority

gate switching used in the clocking scheme design. This oscillator can be used to generate clock signals for a ME-MTJ adder with the help of additional circuitry shown in Figure 2.18(b). The clock signals, i.e., Reset, Clk0, Clk1, Clk2 are derived from the ME-MTJ clocking scheme are shown in Figure 2.18(c).

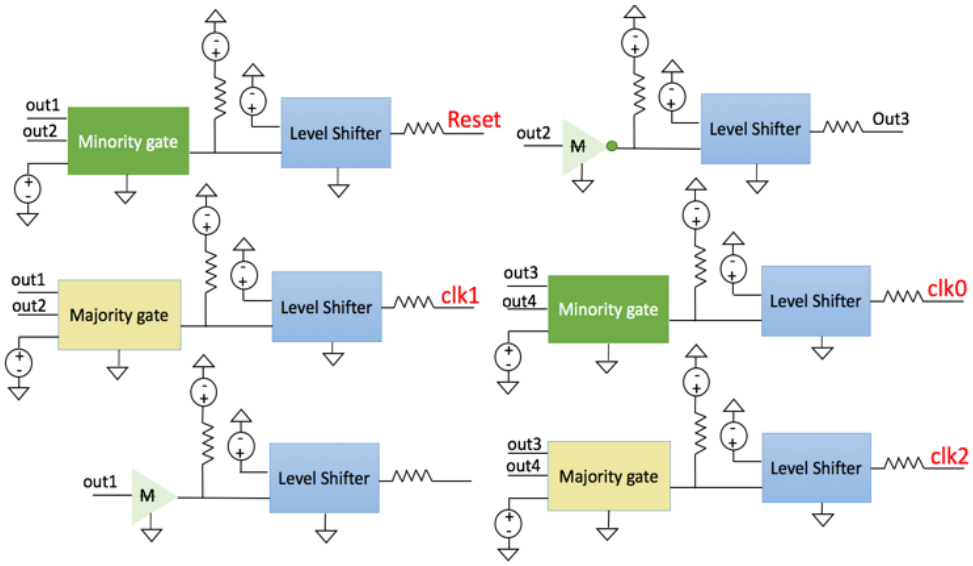
The benefits of having ME-MTJ clocking are multi-fold: Performance of the ME-MTJ based circuits is greatly enhanced with the incorporation of ME-MTJ devices in the clocking scheme since the voltage requirement is the same for all the devices and the clocking times of the ring oscillator vary in accordance with the temperature and power supply along with the device characteristics, in the same way on the logic circuit. As a result, the clocking can be optimized in a much better way than CMOS based clocking.

2.5.1.7.5 ME-MTJ 1-bit Full Adder with ME-MTJ Clocking

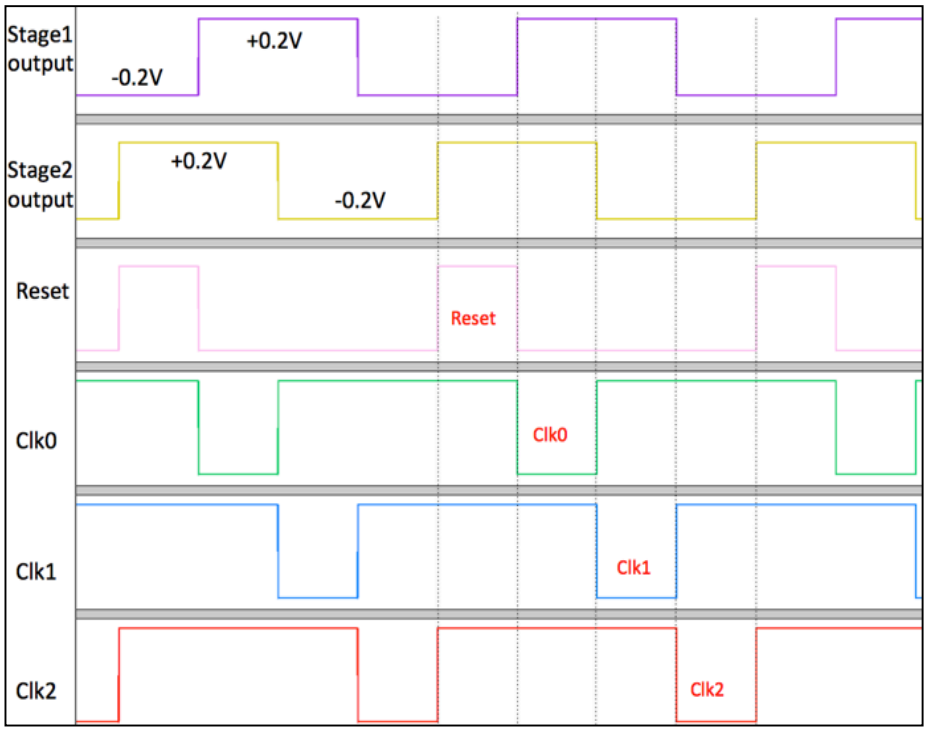
By creating an optimal ME-MTJ ring oscillator and a specific full adder clocking scheme, we can make best use of the ME-MTJ device options.



(a)



(b)



(c)

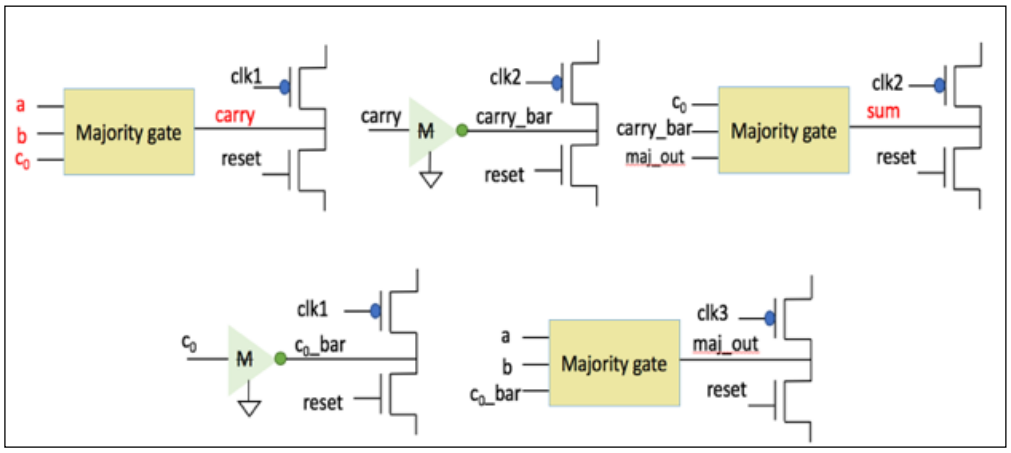
Figure 2.18: (a) Circuit schematic of a 2-stage ring oscillator designed using ME-MTJ gates. (b) Additional ME circuitry to derive the clock signals. (c) Clocking scheme designed using a ME-MTJ based ring oscillator. © 2017 IEEE

Figure 2.19 shows the circuit schematic of the ME-MTJ majority gate based 1-bit full adder along with the transient simulation of the adder validating four cases. The adder is fed with clock signals generated using the ME-MTJ oscillator described in Figure 2.18(c).

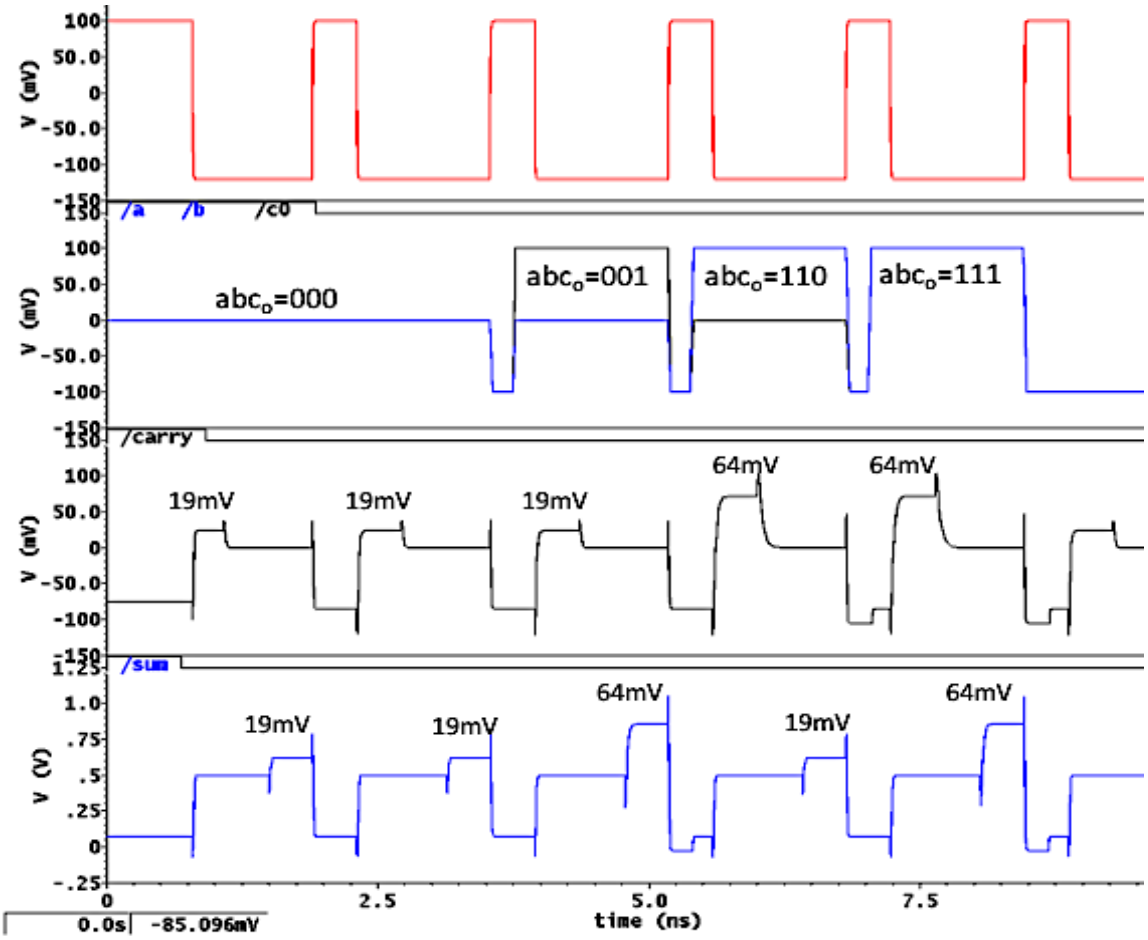
2.5.2 Analog Circuit Design

Previously, the ME-MTJ devices have been used to demonstrate their capabilities for digital applications. Here, their analog possibilities with a variety of circuits adapted specifically for ME-MTJ are demonstrated. Many system applications deal with quantities that are analog in nature, such as temperature, weight, humidity etc. An analog to digital converter (ADC) is needed to process the analog data and give a digital result understood by the application [87-89].

The circuit options include a ME-MTJ based analog comparator and two variations of the 8-level ADC using serial and parallel ME-MTJ circuit configurations. These circuits use the Verilog-A based models for the ME-MTJ device introduced earlier in the chapter for design and simulation of the ME-MTJ based ADC circuits and Cadence Spectre to validate the circuit functionality. For the simulations, a commercially available CMOS based foundry process is used. While the ME-MTJ majority gate which is a three-input device can be used directly, of more use for analog applications is a two-input device, which permits single voltage trim for precision input threshold, in much the same way as with a CMOS comparator. As shown in Figure 2.20, this device has two inputs (V_{G1S},V_{G2S}) and works on the principle of averaging of the input voltages just like the majority gate version.



(a)



(b)

Figure 2.19: (a) Circuit schematic of ME-MTJ based full adder. (b) Transient simulation results of the adder simulated using the ME-MTJ designed clocking. © 2017 IEEE

The ME-MTJ comparator operation is described as follows: If the average of the applied input voltage (V_{in}) and the reference voltage (V_{ref}) exceeds the switching threshold of the device (V_{ME}), then the output goes high. This is because the spin vectors in chromia and the exchange biased free FM layer have 'up' spin orientation whereas the fixed FM pinned by an AFM substrate is assumed to have 'down' spin shown in Figure 2.20. Since the relative spin vector orientation between the fixed and free FM is anti-parallel, this results in maximum resistance across the MTJ cell and the output is represented by a bit "1". In contrast, if the average exceeds V_{ME} in the negative domain, i.e., less than -50 mV, the output is set to "0" due to minimum resistance across the MTJ cell. The operation can also be described using equations shown in Figure 2.20. This device is used as the unit cell for the ME-MTJ based 8-level ADC designs.

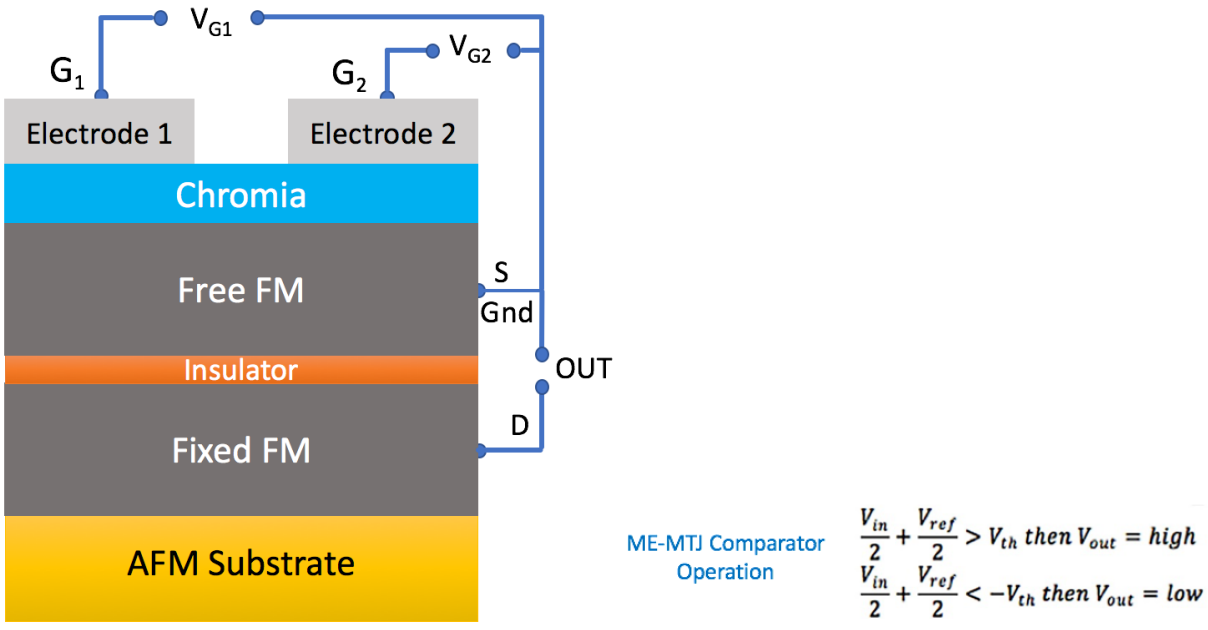


Figure 2.20: Two-input ME-comparator with the mathematical equation for the operation.

2.5.2.1 ME-MTJ Comparator

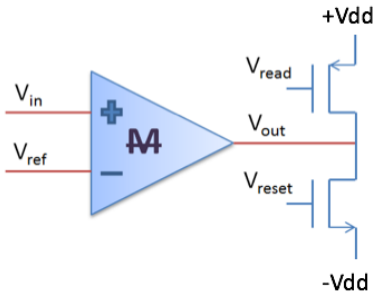
The circuit schematic of the ME-MTJ comparator with pull-up and reset transistor is shown in Figure 2.21(a). In the simulations presented here, the PMOS transistor used to read the output state, is 'on' throughout the cycle once the reset signal goes low. The sense circuitry is clocked to reduce the static leakage.

Transient simulations have been performed for the ME-MTJ comparator with the reference voltage (V_{ref}) set at 110 mV and the input voltage (V_{in}) varied from -100 mV to 100 mV as shown in Figure 2.21(b). At the beginning of the cycle, a reset signal is passed through the system pulling all the nodes down to -100 mV.

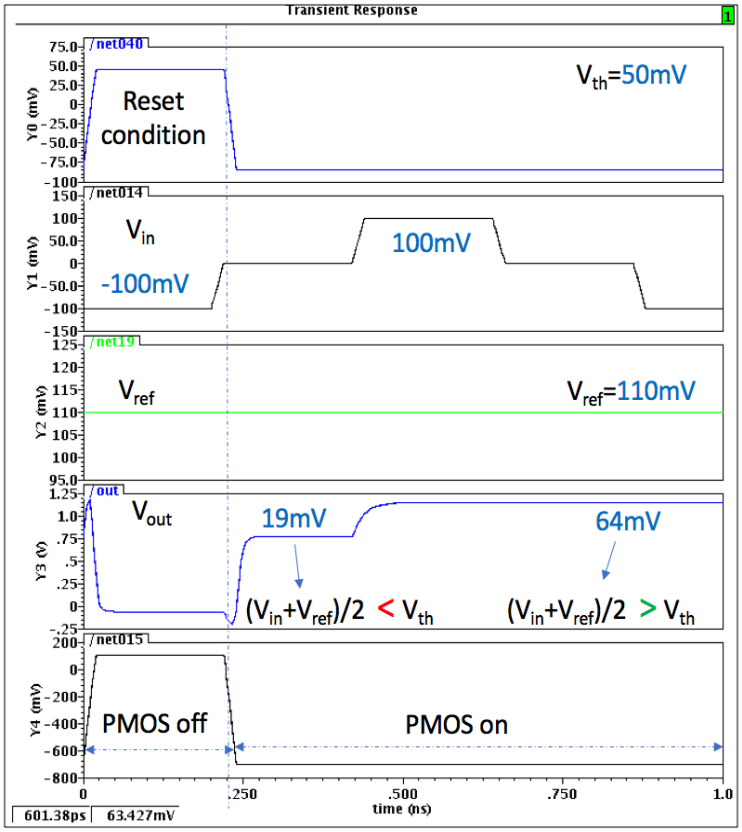
The output memory state is thus initially 'low' (19 mV). At t=250 ps, the sensing transistor is switched 'on' while the input (V_{in}) of the ME-MTJ comparator is ramped up from -100 mV to 100 mV. At V_{in}=0 V, the output of the comparator goes high (64 mV) after a coupling delay of 200 ps, as the average of the inputs applied exceeds $+V_{ME}$ fulfilling the switching criteria. After the input goes back to -100 mV, the output still remains high at 64 mV shown in Figure 2.21(b).

2.5.2.2 Serial ADC - Design and Operation

For an 8-bit ADC, each ME-MTJ comparator shown (Figure 2.22) has a different reference voltage (V_{ref}) depending on the number of quantization levels, here, 7. The step voltage is taken as 15.7 mV since the input range is 0-110 mV and number of levels is 7. A current source is used at the output of the ADC to enable voltage sensing. 'N' ME-MTJ comparators are used to design the 'N+1' level ADC, here, N=7.



(a)



(b)

Figure 2.21: (a) ME-MTJ based comparator with CMOS pull-up and reset transistor and (b) transient simulation results. © 2017 IEEE

In this configuration, the input source (in) is connected to the input terminals of all the ME-MTJ comparators in series. The source of the first comparator is connected to ground. CMOS transistors connect the source to ground for the next six ME-MTJ comparators. The input to these

transistors is a clock signal. When the clock signal goes low, these transistors turn off; the output node of the ME-MTJ device maintains the voltage level and can be read using the current source. When the clock signal is high, the output node is pulled to ground.

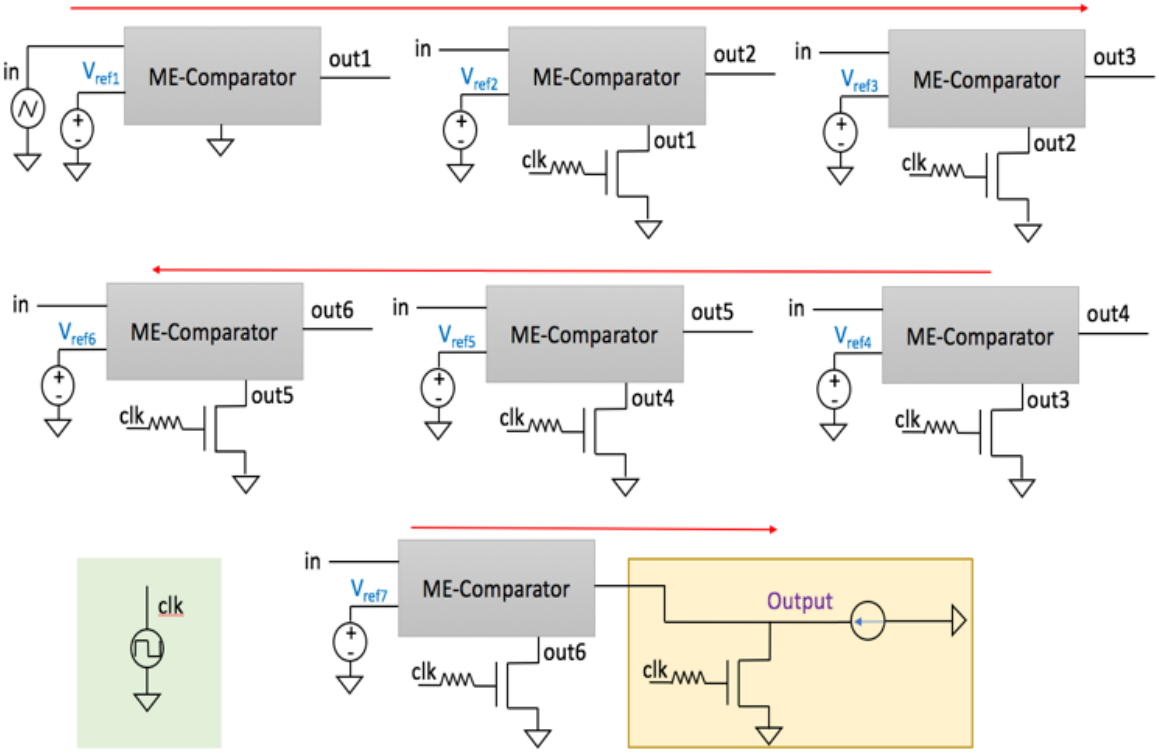


Figure 2.22: Circuit schematic of the serial ADC design. © 2017 IEEE

This configuration enables high precision for sensing. Transient simulations have been performed with the input voltage (V_{in}) ramping up from 0 to 110 mV as shown in Figure 2.23. A pulsed input (V_{clk}) is connected to the gates of the n-channel metal oxide semiconductor (NMOS) transistors. As the input ramps, voltage steps ranging from 14 mV to 89 mV are observed at the output. The drafts observed in the output voltage signal are due to the clock transistors turning off,

when the clock signal goes low. The current bit remains high if the ME-MTJ comparator output is high. The bit turns low and the next bit turns high if the comparator output is low.

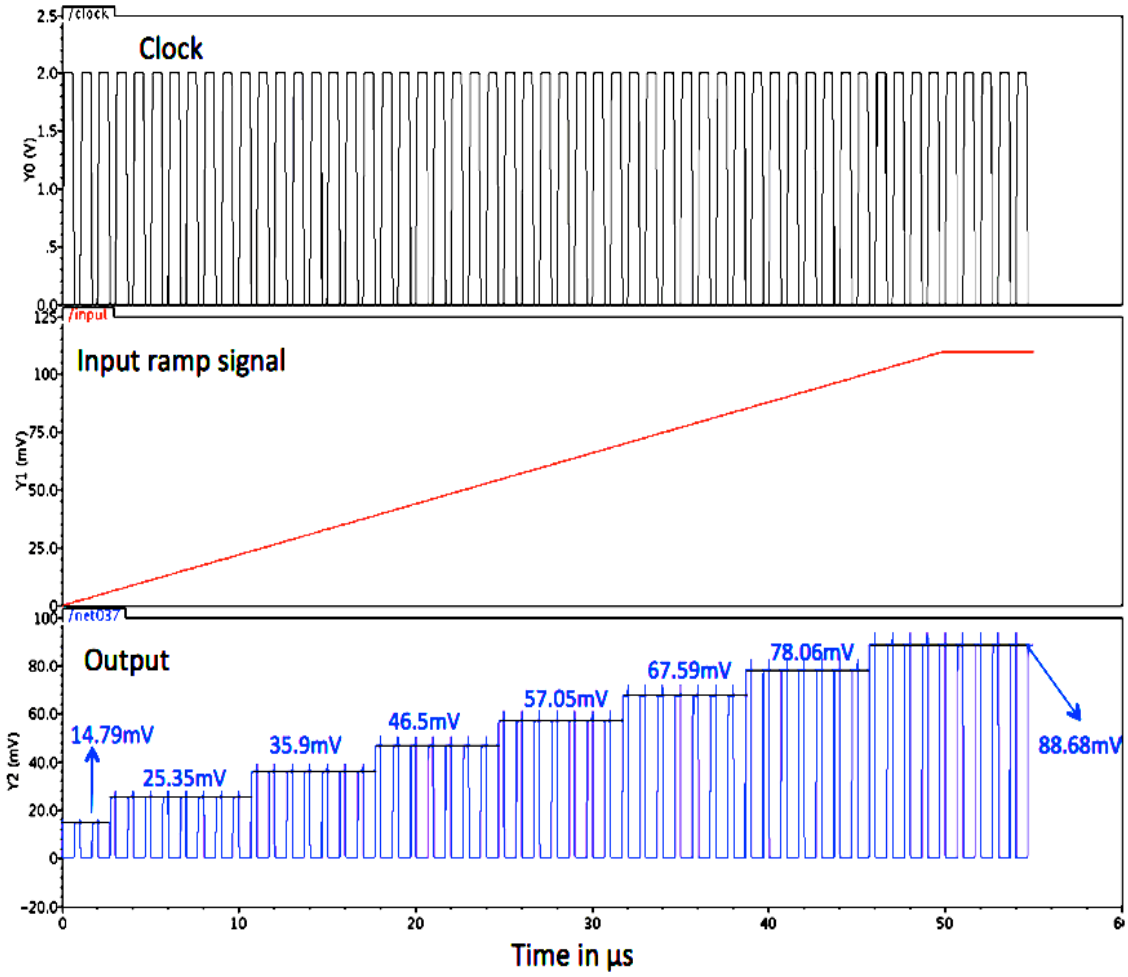


Figure 2.23: Transient simulation results of the serial ADC design. © 2017 IEEE

2.5.2.3 Flash ADC and Peak Detector - Design and Operation

Figure 2.24 shows the circuit schematic of the ME-MTJ based flash ADC. It also behaves as a peak detector, since it detects the peak current states. The comparators are connected in a

parallel configuration. All the node outputs are connected to the pull-up resistor for voltage sensing. Figure 2.25 shows the transfer function of the ADC. In case of an ideal transfer function plot, the dotted red line passes through the midpoint of the voltage steps. The input voltage (V_{in}) is ramped up from 0 to 110 mV. The reference voltages (V_{ref}) are shown in Figure 2.25.

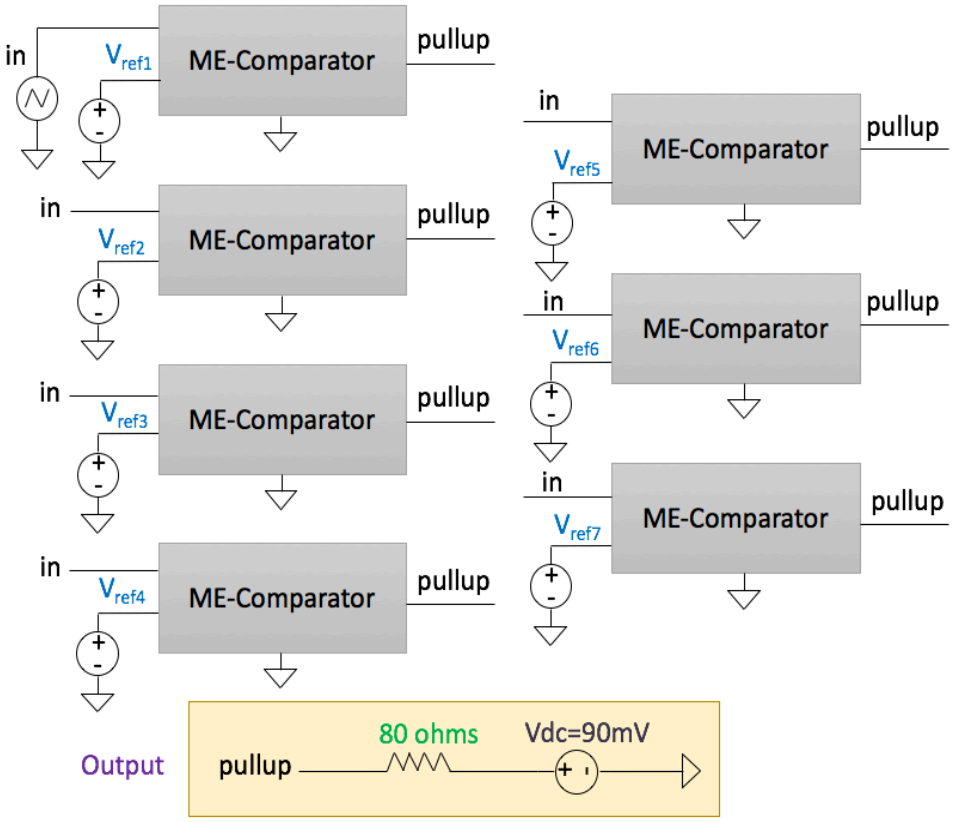


Figure 2.24: Circuit schematic of 8-level ME-MTJ based flash ADC. © 2017 IEEE

As the positive switching condition of each comparator is fulfilled, the output starts to ramp up. The output voltage steps up as each comparator starts to turn-on. The difference in voltage between consecutive steps is ~52 mV with a +/-3 mV error.

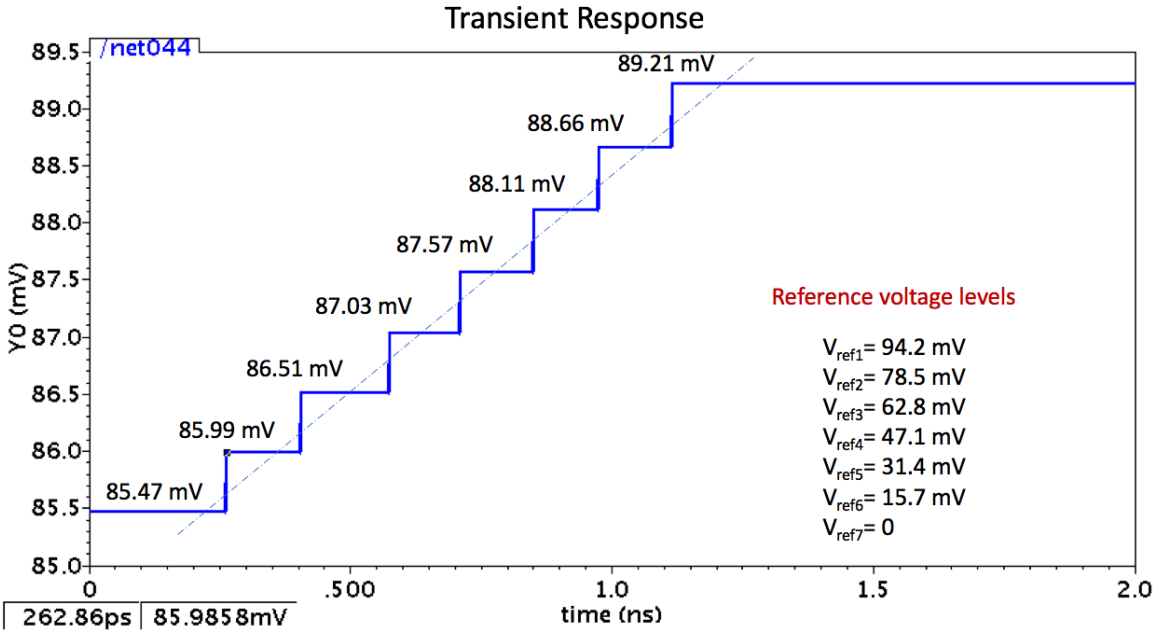


Figure 2.25: Transient simulation results of 8-level ME-MTJ based flash ADC. © 2017 IEEE

2.5.3 ME-MTJ Integration with CMOS (Memory Circuit)

It is recognized that "The current six transistor (6T) SRAM structure is area consuming, and a challenge is to seek a revolutionary replacement solution which would be highly rewarding" [90]. That being said, the 6T SRAM cell is available and in use at the 14 nm CMOS process node. Figure 2.26(a) shows a typical 6T SRAM circuit. It is designed using two inverters (the "true" memory element) and two NMOS gates (the selectors or access devices for the memory element operation), generally close to or less than minimum logic geometries for the same process node. One possible layout design for the 6T memory cell, based on the simple design rule set at F=15 nm is shown in Figure 2.26(b). The area of this cell is 7*20 F^2 or 140 F^2. The storage portion of the cell is 2/3 of the area, and the selector/access devices are 1/3. Conventional SRAM cells lose data once the power supply is switched off.

The ME-MTJ device can be used in conjunction with an SRAM cell to provide non-volatility. This achieves the capability of non-volatile memory arrays, while also enabling zero leakage memory configurations and thus reduced power consumption, since the power in the quiescent state is reduced to just the leakage of the SRAM control circuitry compared with having to retain the SRAM in a standby state.

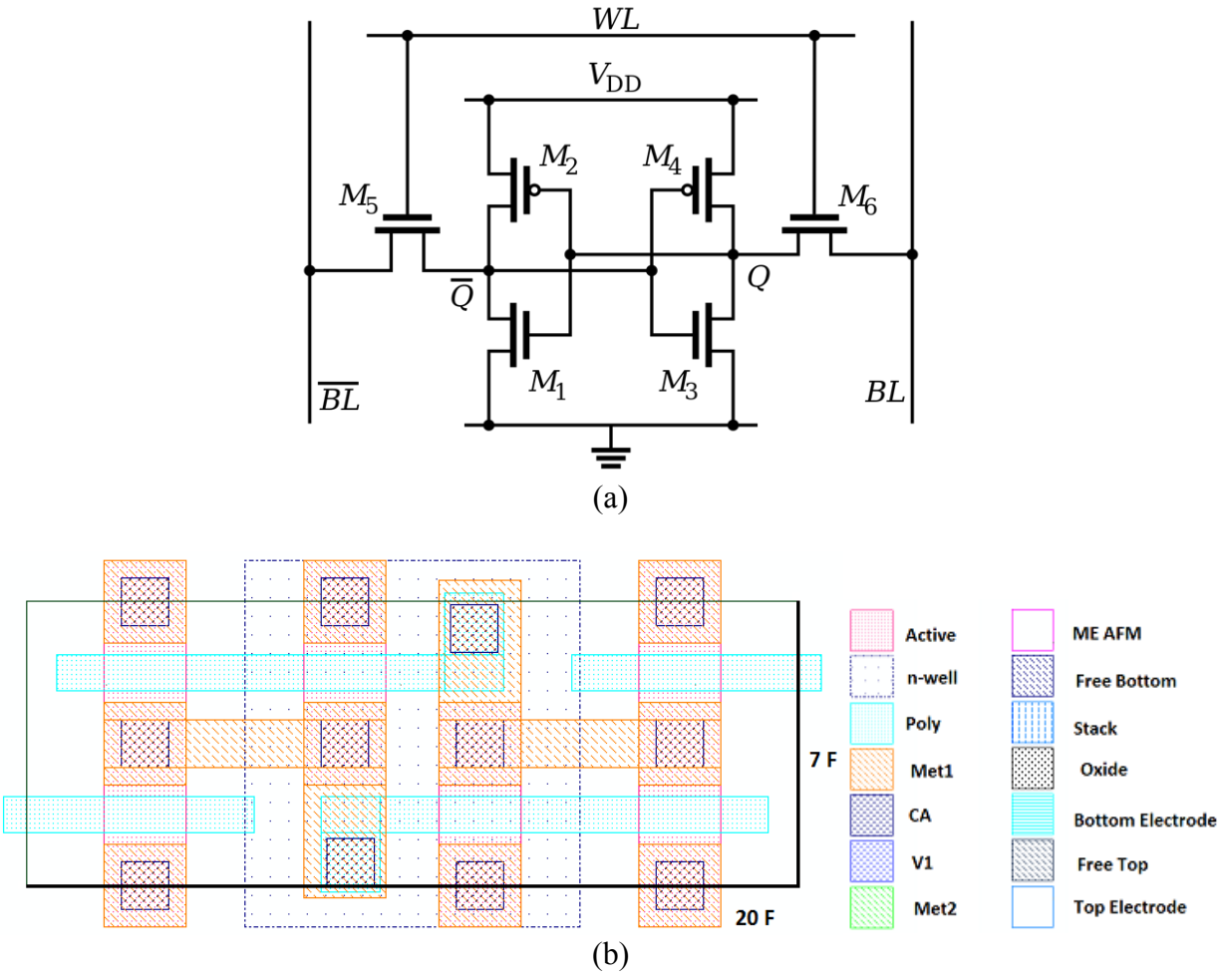


Figure 2.26: (a) Typical CMOS 6T SRAM cell schematic [91]. (b) Layout of a 6T SRAM cell, using the basic layout rules. Area for the layout = 140 F^2 and the layer key is also shown, and is also applicable to Figures 2.29 and 2.31. © 2015 IEEE

2.5.3.1 Circuits for Interfacing ME-MTJ with CMOS

The two ME-MTJ device configurations shown here indicate how these beyond-CMOS technology can be interfaced with conventional CMOS to provide efficient and robust memory latches [33,92]. Since ME-MTJ devices can be integrated at the BEOL of CMOS; the device itself doesn't take additional space, while adding non-volatility to the memory. The PMOS transistor (P_{ON}) is used to start up the circuit with the same operating conditions for the transistors of the bi-stable latch in the circuits. The output of the SRAM cell swings between 0 and $+V_{DD}$ while programming of ME-MTJ device requires –V and +V (where V=0.1 Volts). Because of the different voltage requirements of the ME-MTJ devices with respect to CMOS, level shifters are required. The 10 transistor (10T) level shifter is shown in Figure 2.27.

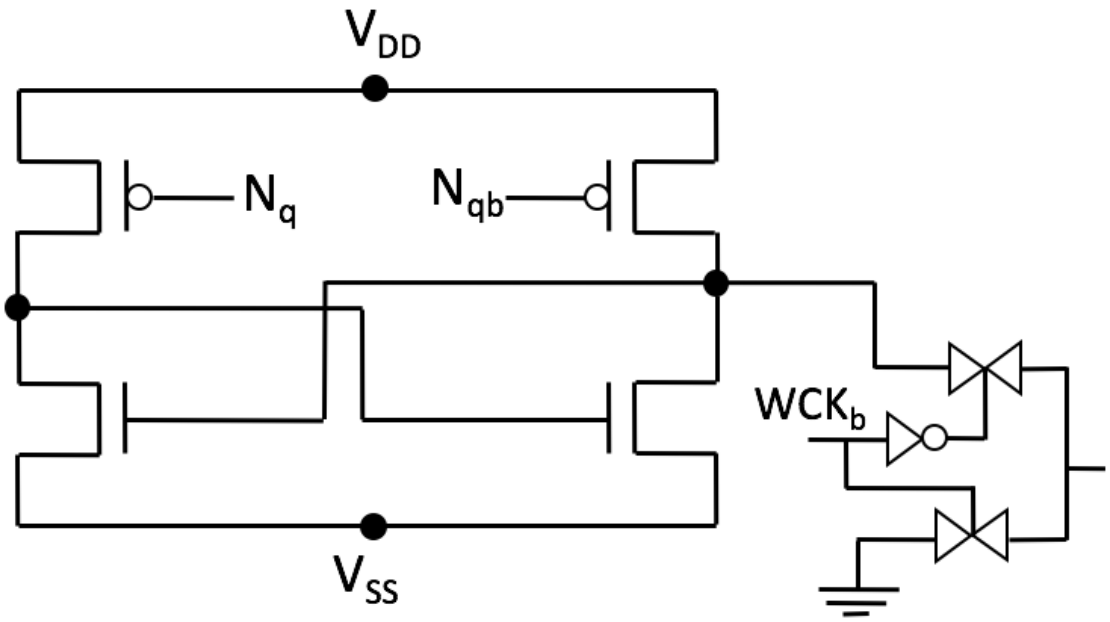


Figure 2.27: 10T level shifter used to translate the CMOS voltage levels to program the ME-MTJ devices [92,93].

The first device configuration for interfacing the ME-MTJ with SRAM cell is shown in Figure 2.28. Here, M4 holds the SRAM at a standby state. The ME-MTJ defines the start-up condition due to the resistance difference between ME-MTJ devices, which introduces the offset. Circuit operation of the CMOS ME-MTJ hybrid circuit is as follows: The ME-MTJ is programmed such that the voltage level stored in the latch biases the starting SRAM into its correct state. It is assumed that data write to the cell is complete and a bit "1" is stored at node nq (bit "0" at node nqb) in Figure 2.28. With M3 off and its source connected to the pinned (fixed) FM layer, the corresponding ME-MTJ is in the high-resistance state (bit "1"), enhancing the stored state in the SRAM cell. Similarly, since the transistor M3' is on, the ME-MTJ on the right is in the low resistance state enhancing the "0" at the node nqb when the SRAM state is not switching.

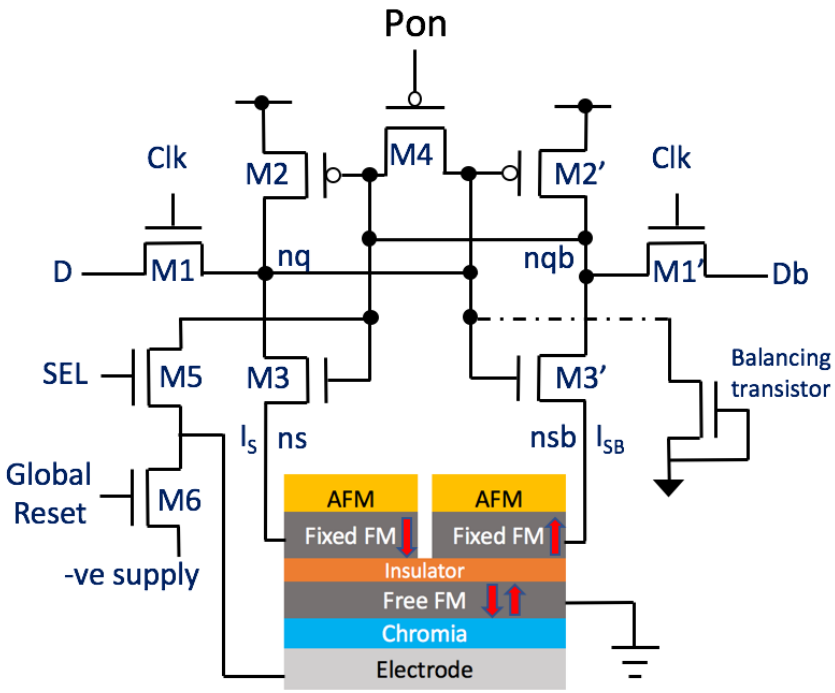


Figure 2.28: SRAM cell schematic with ME-MTJ circuitry.

To verify the non-volatility in the SRAM cell, the power supply is removed. When the power is returned, the high-resistance state of the ME-MTJ causes the source of M3 to be at a higher voltage, forcing M3 to turn off, thus returning the latch to its original state. The layout area is 843 F^2 for this configuration and is shown in Figure 2.29.

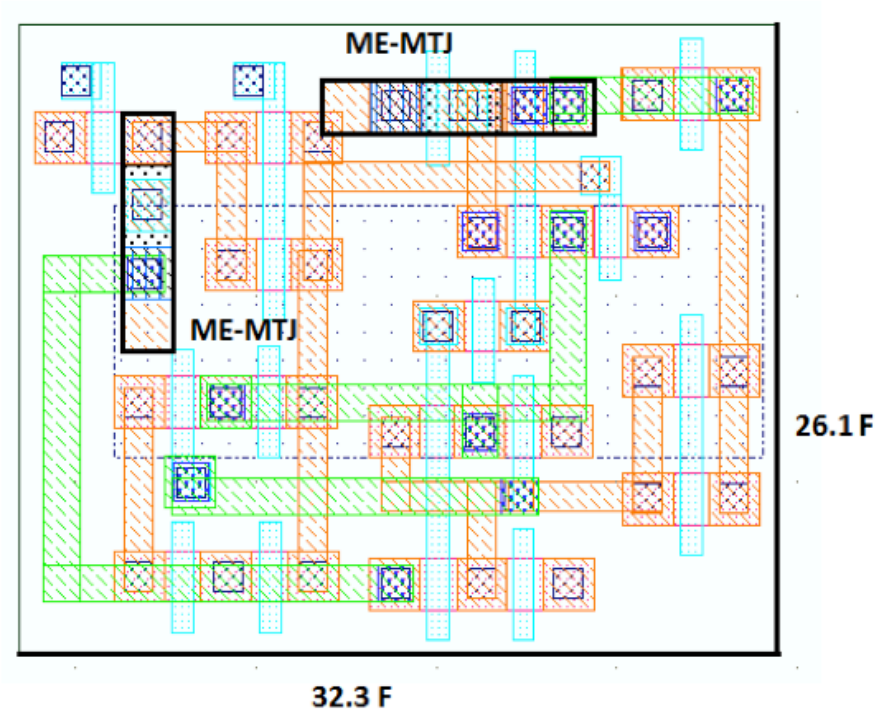


Figure 2.29: Layout of the SRAM cell with ME-MTJ devices placed at the back-end-of-line of CMOS process. The area of this configuration is 843 F^2. © 2015 IEEE

Since this is not area efficient, we also considered alternatives, one of which is presented here. In this configuration shown in Figure 2.29, the electrode and free FM layers are shared by the two ME-MTJs making the device area efficient. The device is modified to have a dual output with two pinned layers - one with spin orientation fixed in ‘up’ direction and the other in ‘down’

direction. This will give both low and high-resistance states from a single shared ME-MTJ device [93].

Even though the 10T level shifter circuit (Figure 2.27) provides the voltage range required for their proper functioning, the substantial layout area is a drawback. A solution is to modify the reset circuitry to incorporate two transistors (i.e., 'SEL' and 'Global reset'). The circuit operates as follows: Assume that the data write operation in the cell is complete and bit "1" is stored at node nq (bit "0" at node nqb) (Figure 2.30). Since M3 is off and its source is connected to the fixed layer, the ME-MTJ on the left side is in high-resistance (bit "1"), enhancing the stored state.

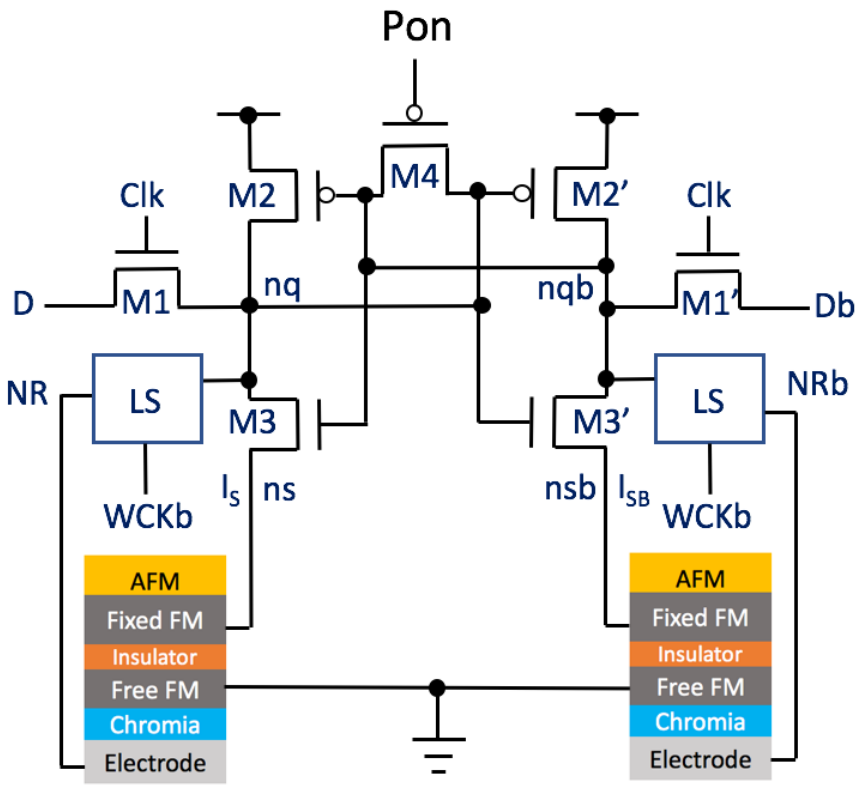


Figure 2.30: Circuit modified to include the global reset circuitry [92,93]. © 2015 IEEE

When the supply is removed, the source of M3 is held at a higher voltage, causing M3 to turn off. The ME-MTJ on the right side is in low resistance state (bit "0"), forcing turn-on of M3'. Thus, the SRAM cell is flipped back to the state it was in before power was taken off. If 'SEL' signal is off and 'global reset' is on, the shared ME-MTJ electrode is pulled down to -V. This flips the state of the free layer, thus switching the bit stored in the ME-MTJ device. When 'global reset' is off and 'SEL' is on, the previous stored state is recorded by the ME-MTJ. The layout area for this circuit with global reset is 260 F^2 shown in Figure 2.31. A significant area improvement compared to the standalone circuit configuration, however it does require a global reset, rather than an individual reset, so is probably only applicable to memory arrays.

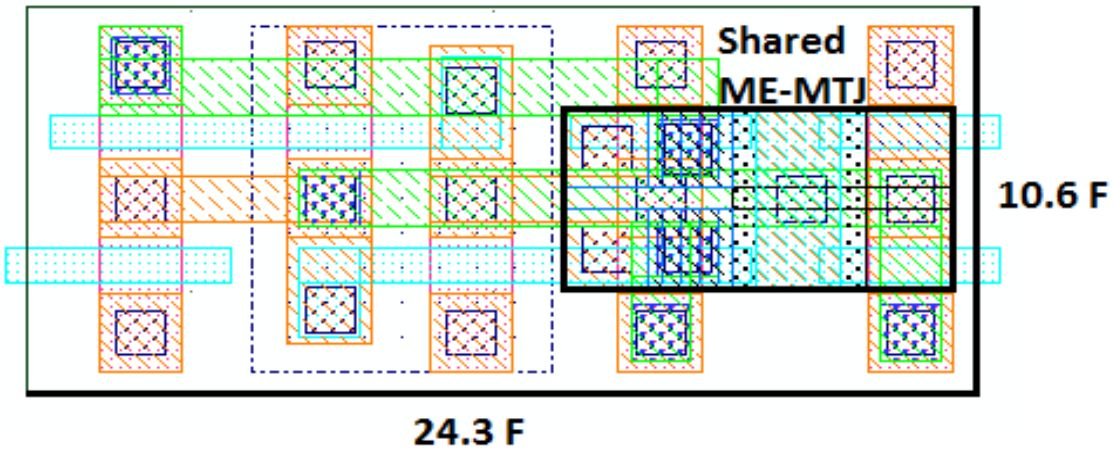


Figure 2.31: Layout area for the circuit configuration is 259.9 F^2 [92,93]. © 2015 IEEE

CHAPTER 3

UNIPOLAR MAGNETO-ELECTRIC MAGNETIC TUNNEL JUNCTION[9]

3.1 Limitations of the ME-MTJ Device

One issue with the Magneto-electric Magnetic Tunnel Junction (ME-MTJ) devices is that their switching requires a bipolar logic, i.e., positive and negative polarity of the supply voltage, i.e., +0.1 V and -0.1 V, and a ground supply. Thus, as discussed in chapter 2, periodic resetting or level-shifting is needed. Both are undesirable.

3.2 UMMTJ Device

Here, we introduce a new device adaptation that enables direct coupling between the ME-MTJ devices. The Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) device concept [94] allows direct coupling of devices, using only a unipolar (positive) supply. This is achieved by adjusting the switching threshold of the ME-MTJ device. The operation of the UMMTJ device is similar to that of the ME-MTJ. The voltage adjustment can be done in one of the two ways described in detail in the following section.

3.2.1 Device Design

The switching threshold (V_{ME}) of the ME-MTJ device is defined as the voltage required for switching the spin vectors of the chromia layer exchange biased to the 'free' ferromagnetic

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[9] © 2017 IEEE. Reprinted, with permission, from Nishtha Sharma, Andrew Marshall, Jonathan Bird, Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) Devices and Circuits, IEEE Fifth Berkeley Symposium on Energy Efficient Systems, July 2017.

(FM) layer. To adjust this voltage, we introduce an additional level-shifting layer into the gate of the device which can be done in two ways:

3.2.1.1 Switching Voltage Adjustment - Scheme 1

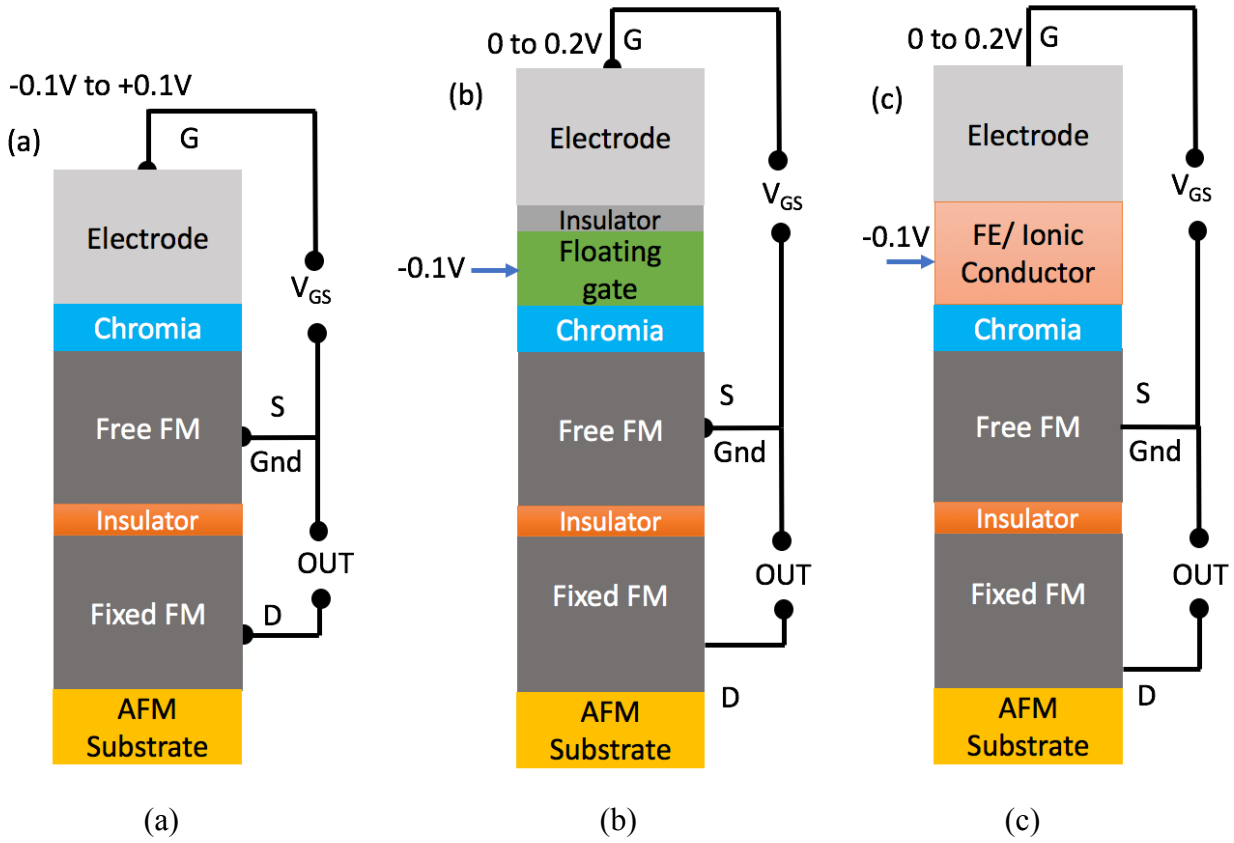
The first way to adjust the V_{ME} is by placing a floating gate in between the electrode and chromia layer in the ME-MTJ device shown in Figure 3.1(a). The floating gate may be programmed to offset the input voltage requirement, so it can be switched between a positive supply ($+V_{DD}$) and ground.

This has similarities to Complementary Metal Oxide Semiconductor (CMOS) logic flash memory, which utilizes a floating gate for memory storage, and 'analog floating gate' CMOS, which utilizes floating gates for threshold trimming. The floating gate has a programmable charge, trimmed here to -0.1 V (Figure 3.1(b)). The net voltage seen by the chromia layer again ranges from -0.1 V to +0.1 V after the adjustment as shown in Figure 3.1, fulfilling the input switching condition of the ME-MTJ device.

3.2.1.2 Switching Voltage Adjustment - Scheme 2

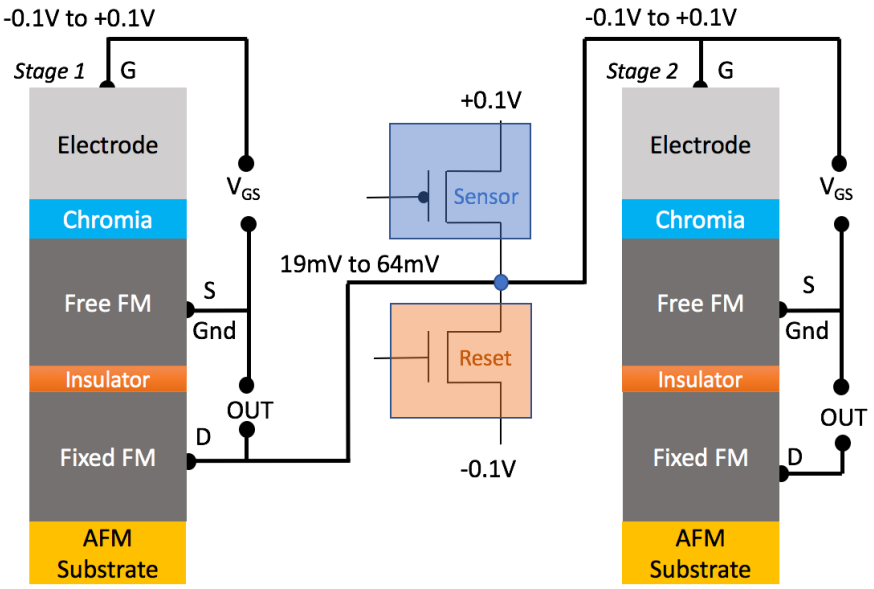
An alternative way to modify the threshold is to add a ferroelectric layer or ionic conductor shown in Figure 3.1(c), which can be programmed initially to the desired state and then it maintains its memory state for a long time. The voltage shifting is the same as described for the floating gate version. Thus, a level-shifted input is constructed, such that the input and output voltage range is the same. As shown in Figure 3.2(a), pair of CMOS transistors are used at each stage to enable

read and reset operation of the ME-MTJ devices, whereas only the read transistor is required for the UMMTJ based devices (Figure 3.2(b)).

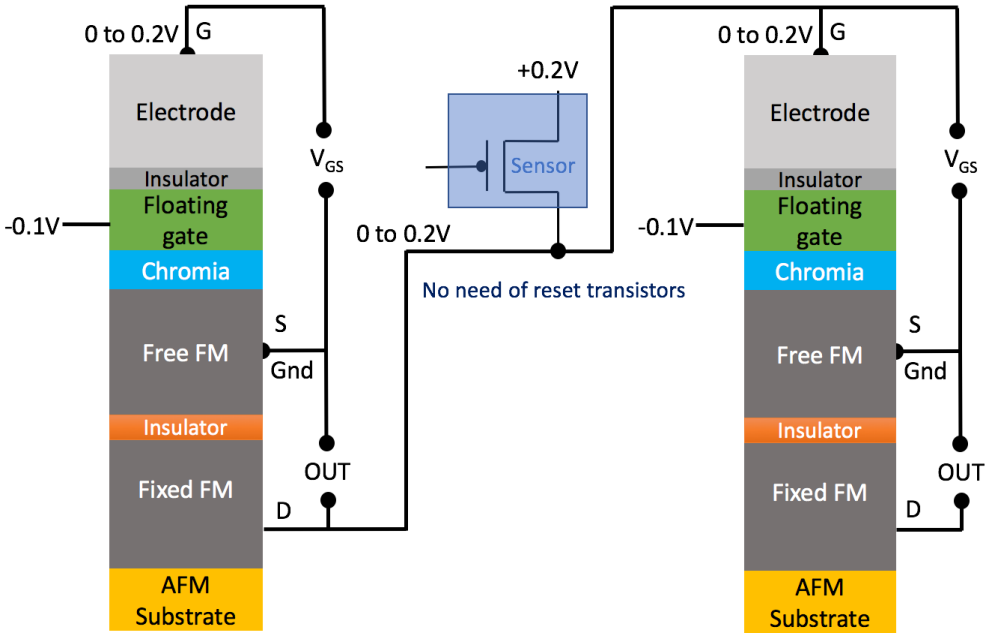


(a) (b) (c)

Figure 3.1: (a) Cross-section of the ME-MTJ device. (b) The UMMTJ device structure showing a floating gate between the electrode and chromia layer. (c) The UMMTJ device structure showing a ferroelectric (FE)/ionic conductor inserted between the electrode and chromia layer. © 2017 IEEE



(a)

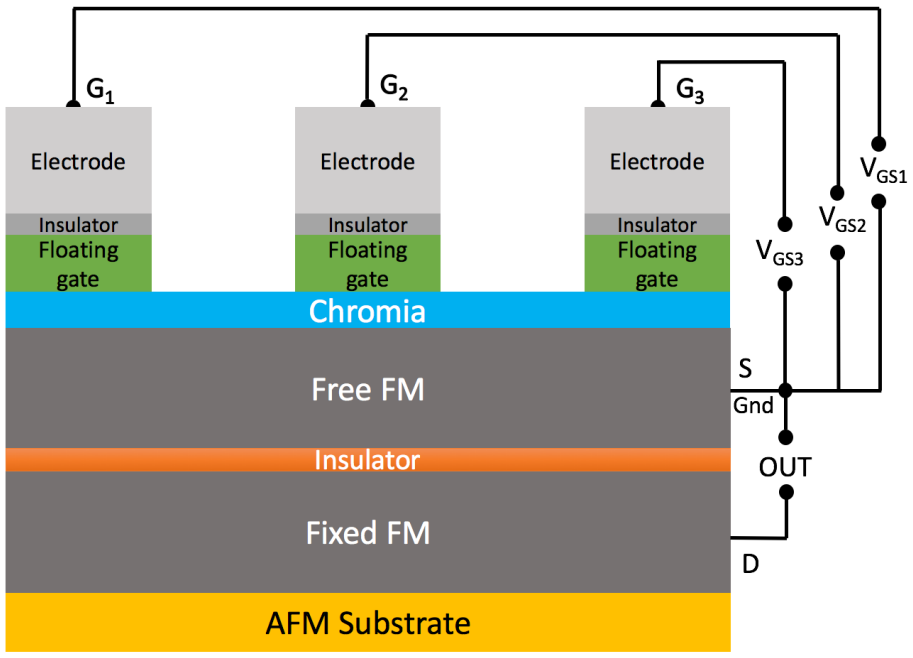


(b)

Figure 3.2: (a) Block diagram of a 2-stage ME-MTJ device with MOS pair for read/write operation. (b) Block diagram of a 2-stage UMMTJ device with a single transistor for read/write operation. © 2017 IEEE

3.3 UMMTJ based Devices

The variants of the UMMTJ devices are used to construct the majority gate logic and XNOR logic as shown in Figure 3.3. The majority gate version has three separate inputs influencing the electric field across the three individual chromia layers (Figure 3.3(a)) [93]. The version with a merged floating gate shown in Figure 3.3(b) is easier to program, but does not have the flexibility to individually program threshold voltages. The XNOR version [85] has two floating gates modifying the input voltages seen by the top and bottom chromia layers, level-shifting the input voltages applied shown in Figure 3.3(c). The operation of the UMMTJ based majority and XNOR gate remains the same as the ME-MTJ version [35,40,85,93].



(a)

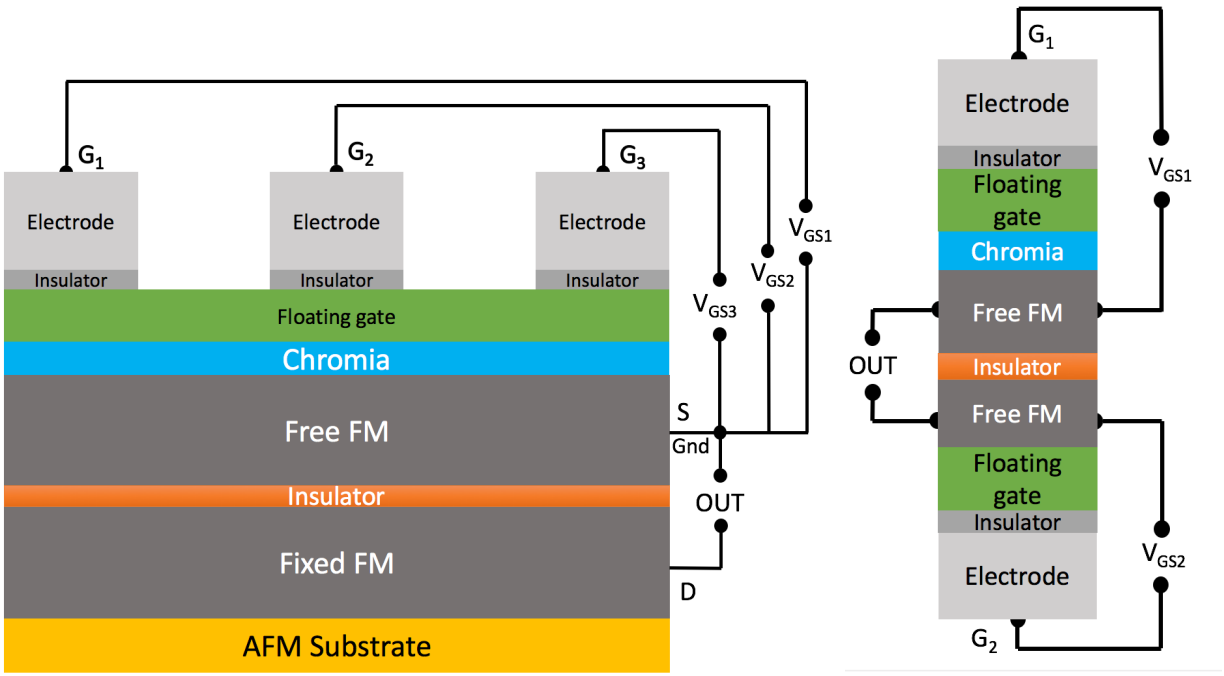


Figure 3.3: (a) UMMTJ based majority gate with separate floating gates (b) UMMTJ based majority gate with a merged floating gate (c) XNOR with two floating gates modifying the thresholds of the chromia layers. © 2017 IEEE

3.4 UMMTJ Device Programming

A CMOS flash memory cell (Figure 3.4(a)) uses a floating gate to store a bit by the presence or absence of a charge. If the floating gate is not charged (i.e., neutral), then the device operates almost like a conventional non-floating gate Metal Oxide Semiconductor Field-Effect Transistor (MOSFET). A positive charge in the control gate creates a channel in the p-substrate that carries a current from source to drain.

If, however, the floating gate is negatively charged, then this charge shields the channel region somewhat from the control gate and prevents the formation of a channel between source and drain as shown in Figure 3.4(a). While the UMMTJ device can be programmed using several

different techniques, it rather depends on the type of the UMMTJ device. Figure 3.4(b) shows the top view and cross-section view of the analog floating gate cell [95].

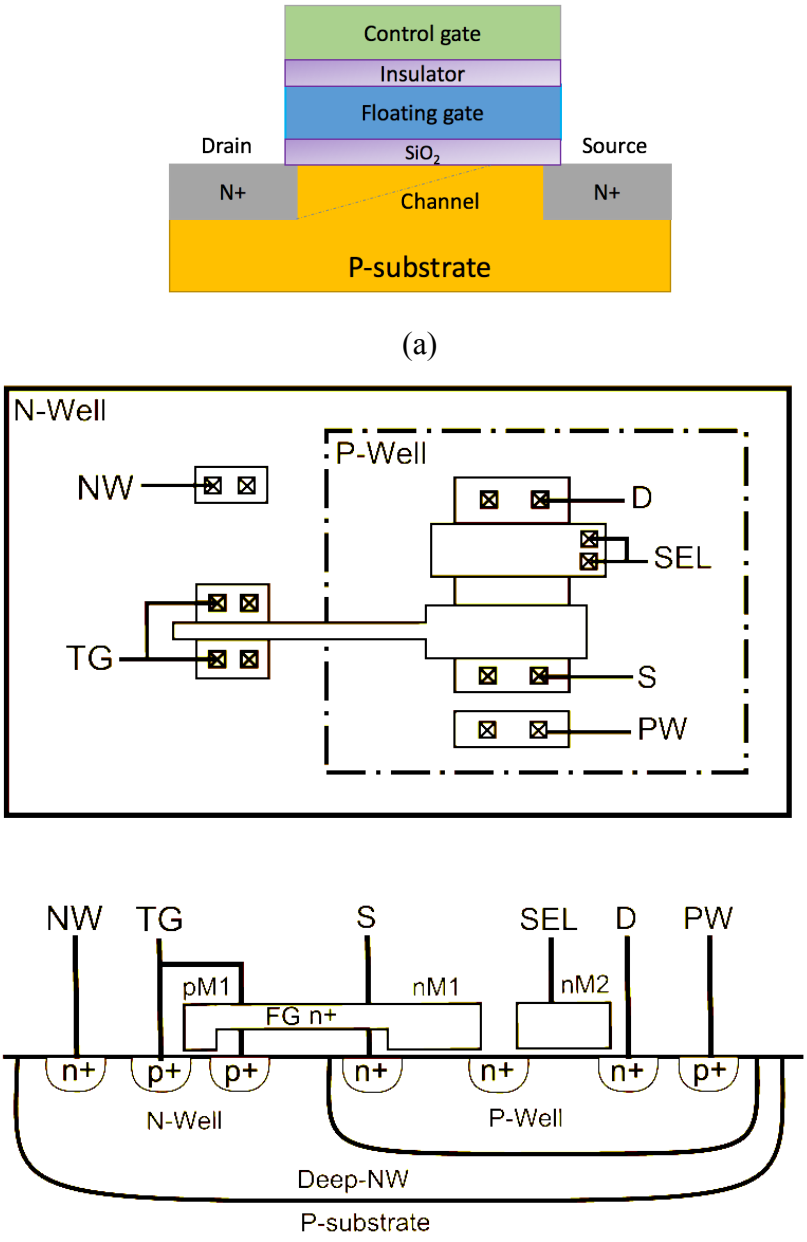


Figure 3.4: (a) CMOS flash memory cell. (b) Analog floating gate construction. © 2015 IEEE

3.4.1 Floating Gate UMMTJ

One of the mechanisms to program the floating gate in the UMMTJ device is by making use of Fowler Nordheim tunneling [96]. Analog floating gate devices use this form of charging/discharging of the tunneling layer. Appropriate programming voltages are applied through the tunnel junction. This is programmed once, during final test of the component and does not need programming subsequently since the charge is maintained for several years.

Multiple floating gate based UMMTJ devices can be accessed through a programming transistor that contacts to the tunnel diodes used to program each floating gate. This circuitry may be housed as CMOS support circuitry beneath the ME-MTJ circuitry. If multiple floating gates based UMMTJ devices need to be programmed to the same level, i.e., if we needed to 'add' or 'subtract' 0.1 V from a stack of devices, it is most efficient to program a group of devices at the same time, using global programming techniques.

3.4.2 Ionic Conductor/Ferroelectric UMMTJ

For an ionic conductor/ferroelectric based UMMTJ device (Figure 3.1(c)), programming of the switching voltage is as follows: A large voltage (~ 5-10 V) is applied across the gate and free ferromagnetic layer. This is sufficient to modify the state of the conductor which is set to the required state, and from there on, the device can then be operated in ME-MTJ mode, where the voltage range is suitable for switching between the ME states.

Unlike the floating gate based UMMTJ device, here, we cannot use a global programming device, as this would short-circuit all the inputs. In this case, we have a global control circuit, but

with individual transistors to each gate input, in a manner like a global reset (indeed, if a global signal is required, the programming and global signal may serve dual-purpose, changing only the input voltage between functions). The best way to program these devices, where precision trimming of individual devices is required in a real circuit with individual mismatch, is using a memory array type configuration such that the devices can be programmed individually. The configuration looks like a Dynamic Random-Access Memory (DRAM) cell, with an access transistor providing access to the tunnel diode or device gate, depending on the type of configuration. Each gate is accessed through a word and bit line; the only difference being the adjustment of the bit line in voltage depending on the requirement of the programming voltage. Alternatively, the word line may also be adjusted to limit the programming time.

3.4.3 Retention Loss

Retention loss may or may not be a concern in one or the other type of the UMMTJ devices. Although, it is beneficial to have the built-in structures to enable re-programming, the options differ depending on the type of programmable gate version being employed. It is highly likely that the charge (floating gate) based system will only need programming once. This is because the voltage of the programmed gate may typically be only of the order of a hundred millivolts higher or lower than the gate or supply voltages. The field across the oxide and thus the charge loss would be very low. The programming mechanism would most likely be in place, if field re-programming was required, though additional voltages (charge pumped potentially) would be needed in some cases.

For ferroelectric based gate voltage requirement manipulation, it is expected that charge loss may occur over a period of weeks to months. Thus, re-programming is necessary. Additional programming and selection voltages would be needed in some cases, and must be included in the circuit design. Re-programming is relatively easier than initial programming, as the re-programming would generally just need 'topping off', likely as a batch charging process.

In general, for correcting retention loss, various auto-zeroing system used in op-amp design can be applied here. A charge capacitor can be used to correct input offset in op-amp and amplifier. It is easy to apply this technique globally, but it gets more complicated if individual devices need to be corrected for the loss. Another way of solving this is to initially apply the correction to individual devices and then globally for the rest of the cycles. This will depend on the application requirement.

3.5 UMMTJ based Circuits

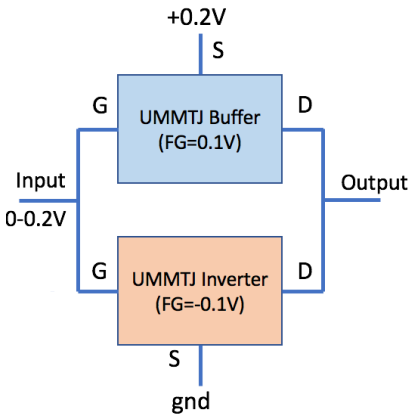
CMOS-like logic circuits can be designed using UMMTJ gates. Two examples of such circuits, i.e., the CMOS-like UMMTJ based push-pull schematic (Figure 3.5(a)) and the UMMTJ ring oscillator (Figure 3.6) are shown here. The previously developed Verilog-A models for the ME-MTJ device presented in [35] have been modified to create UMMTJ models. As shown previously in Figure 3.2, the circuits use lesser components compared to the ME-MTJ based circuits due to internal voltage translation.

3.5.1 UMMTJ Push-Pull Configuration

Figure 3.5(a) shows the schematic of the UMMTJ based push-pull circuit. Two UMMTJ devices, one acting as a buffer and the other one as an inverter, form the push-pull configuration. The floating gates/ionic conductor/ferroelectric layers are programmed so the voltage across the chromia layer is approximately -0.1 V and +0.1 V depending on the unipolar voltage applied. The buffer and inverter are programmed to hold charge equivalent to +0.1 V and -0.1 V respectively. The operation of the circuit is as follows: The output is initially high. As shown in Figure 3.5(b), when the input goes high (0.2 V), the resistance states of the UMMTJ buffer and inverter are is low (R_P) and high (R_{AP}) respectively. Thus, the output goes low to 16 mV after 200 ps which is the intrinsic device delay in ME-MTJ based devices [8].

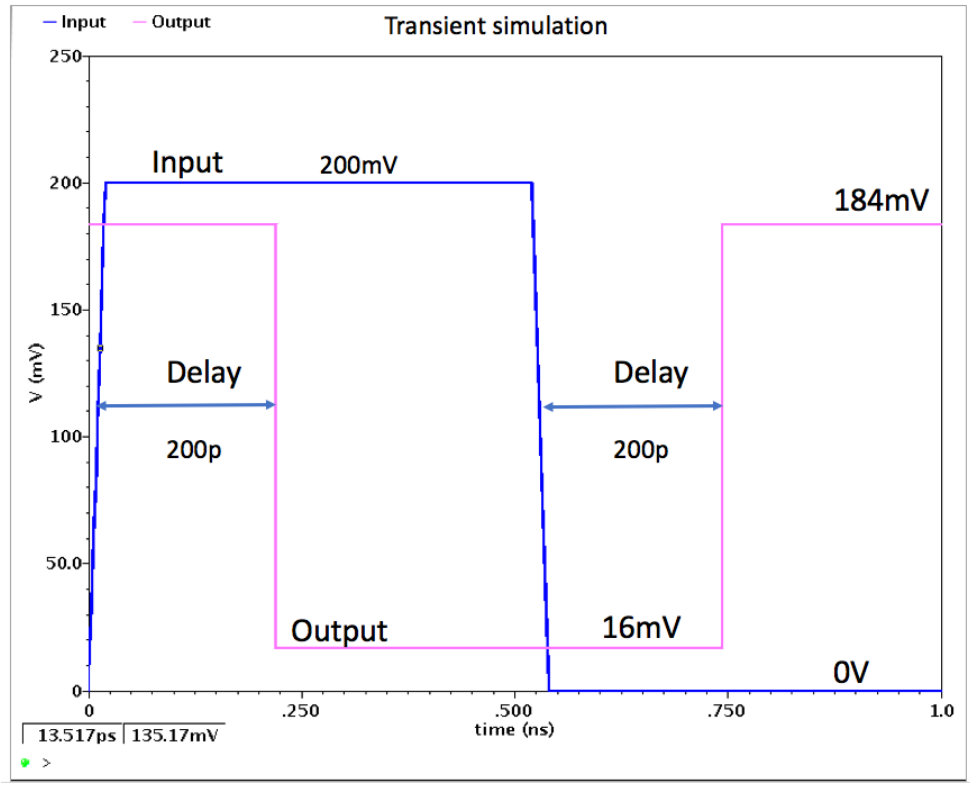
When the input goes low (0 V), the resistance state of the buffer is high (R_{AP}) and the inverter is low (R_P), resulting in high voltage (184 mV) at the output after the device delay. This circuit has the same logic operation as a CMOS inverter. The output voltage swing (16-184 mV) is remarkably higher than the ME-MTJ output voltage swing (16-64 mV) presented in [35].

Resistance states of the UMMTJ based buffer and inverter with the input/output voltage ranges are shown in Figure 3.5(b). The major advantage of this configuration is that it is doesn't require any CMOS component for operation. It also removes the requirement of a CMOS pull-up transistor for the UMMTJ device to sense the resistance across the free and fixed FM layer at each stage.



In	PMOS	NMOS	OUT (Ideal)	OUT (Actual)
0 V	High Resistance	Low Resistance	200 mV	184 mV
200 mV	Low Resistance	High Resistance	0	16 mV

(a)



(b)

Figure 3.5: (a) Two UMMTJ devices are stacked with one in buffer mode and the other in inverter mode (left) and their resistance states. (b) Transient simulation results and resistance states of the UMMTJ push-pull configuration. © 2017 IEEE

3.5.2 UMMTJ based Ring Oscillator

Another application of UMMTJ based devices is ring oscillators. Figure 3.6(a) shows a 3-stage ring oscillator schematic using UMMTJ devices. The oscillator is constructed using two UMMTJ buffers and a UMMTJ inverter. This compares favorably to the ME-MTJ circuit for a 3-stage ring oscillator shown in Figure 3.6(b), as it eliminates the need of inter-device level-shifting circuitry.

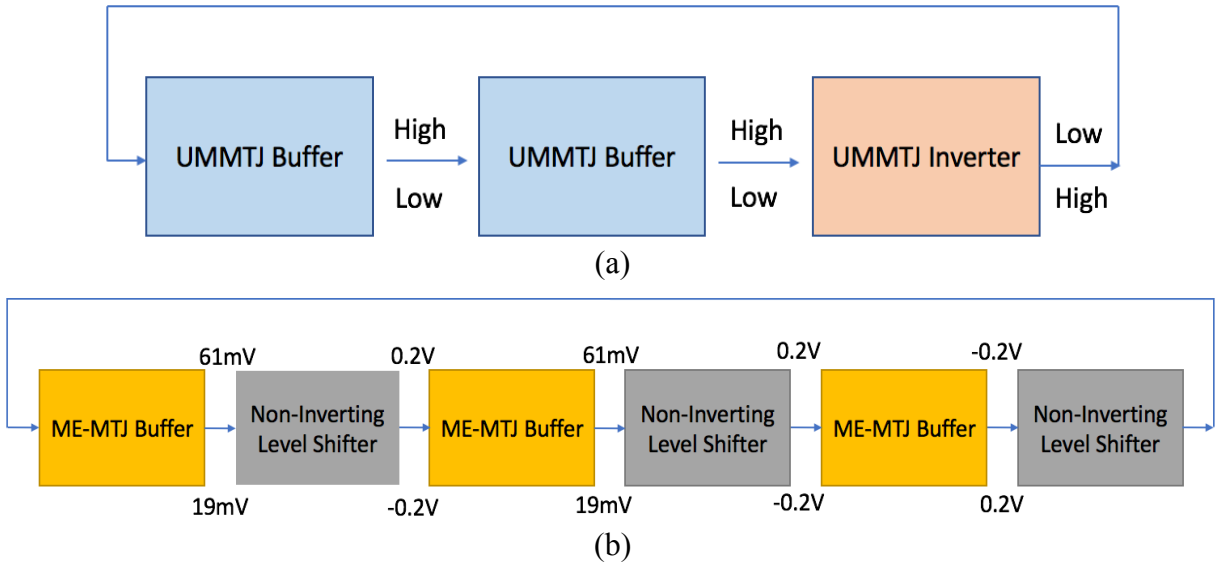


Figure 3.6: (a) 3-stage ring oscillator designed using UMMTJ devices, showing direct coupling between devices. (b) 3-stage ring oscillator using ME-MTJ. UMMTJ version does not require additional current sources, but the level shifter block requires several active components such as CMOS or TFET. © 2017 IEEE

3.6 Voltage Controlled Magnetic Anisotropy in Co/Gd_2O_3

As described above, one way to trim the ME-MTJ structure is to add an ionic conductor where the voltage controlled changes to the interface are very slow compared to the switching

speed of the MTJ cell. Some of the ionic conductors which can be considered for use in the UMMTJ device are Gd_2O_3 [96-104], ZrO_2 [94], NiCoO [105] and $Li_2B_4O_7$ [106]. The cobalt on Gadolinium Oxide (Gd_2O_3) heterostructures thin films have previously been investigated for reversible voltage controlled anisotropy [96-104]. The perpendicular magnetic anisotropy in Platinum (Pt) or Palladium (Pd) capped cobalt films [76,107-112], as well as the influence of oxygen on the magnetic anisotropy in cobalt, has been investigated [96-104,113-116]. The Pt/Co and Pd/Co multilayers can be used as the free layer in a magnetic tunnel junction [117-119], so Pt/Co and Pd/Co bilayers on the ionic conductor Gd_2O_3 is pertinent to the UMMTJ device.

We investigated the voltage controlled magnetic anisotropy of cobalt-gadolinium oxide heterostructures in collaboration with the Center for NanoFerroic Devices (CNFD) team at the University of Nebraska at Lincoln. The principle behind this concept is that at the interface between an oxide layer and a cobalt layer, there will be an exchange of oxygen due to an applied voltage [96-98]. This in turn oxidizes the cobalt and changes the magnetization state of this layer. This process is reversible and non-volatile [96-98], so a bi-stable magnetic layer, controlled by voltage, is produced.

3.6.1 Experimental Work

The Pt/Co/Gd_2O_3/Si and Pd/Co/ Gd_2O_3/Si heterostructure films were grown on a P-type Si (111) substrates. This structure is evident in cross-sectional Transmission Electron Microscopy (TEM). The gadolinium oxide and the cobalt films are visible from right to left between the silicon wafer on the right, in this cross-sectional TEM (Figure 3.7) and the thin platinum cap and the glue on upper left.

The magneto-optic Kerr effect (MOKE) apparatus [97] is based on a 633 nm helium-neon intensity stabilized laser that is then linearly polarized and passes through a photo-elastic modulator. The reflected beam passes through an analyzing polarizer before reaching the photodetector. The interaction between the photons and the surface of the magnetic material, in an applied magnetic field produces a shift in polarization angle thus creating a detectable change in beam intensity as described by Malus' law [98]. The MOKE intensity is related to the strength and direction of the sample's magnetization state [99] and plotted as a function of external magnetic field applied to the sample. The longitudinal and polar MOKE measurements were performed, with an applied voltage across the Pt/Co/Gd_2O_3/Si stack, perpendicular to the external magnetic field as longitudinal MOKE measurements were recorded. Hysteresis loops were observed as expected due to the ferromagnetic nature of cobalt.

Anomalous Hall effect was performed on pre-patterned by conventional optical lithography six-terminal Hall bar device (30 μm strip width and 30 μm electrodes separation). KI 2400 source meter was used as the current source and KI 2182 nanovoltmeter for Hall potential measurements. The perpendicular magnetic anisotropy of a Si/Gd_2O_3 (17 nm)/Co(5 nm)/Pt(1 nm) multilayer stack is voltage dependent. The longitudinal MOKE measurements (Figure 3.8) illustrates the relationship between applied voltage and the in-plane magnetization at various voltages.

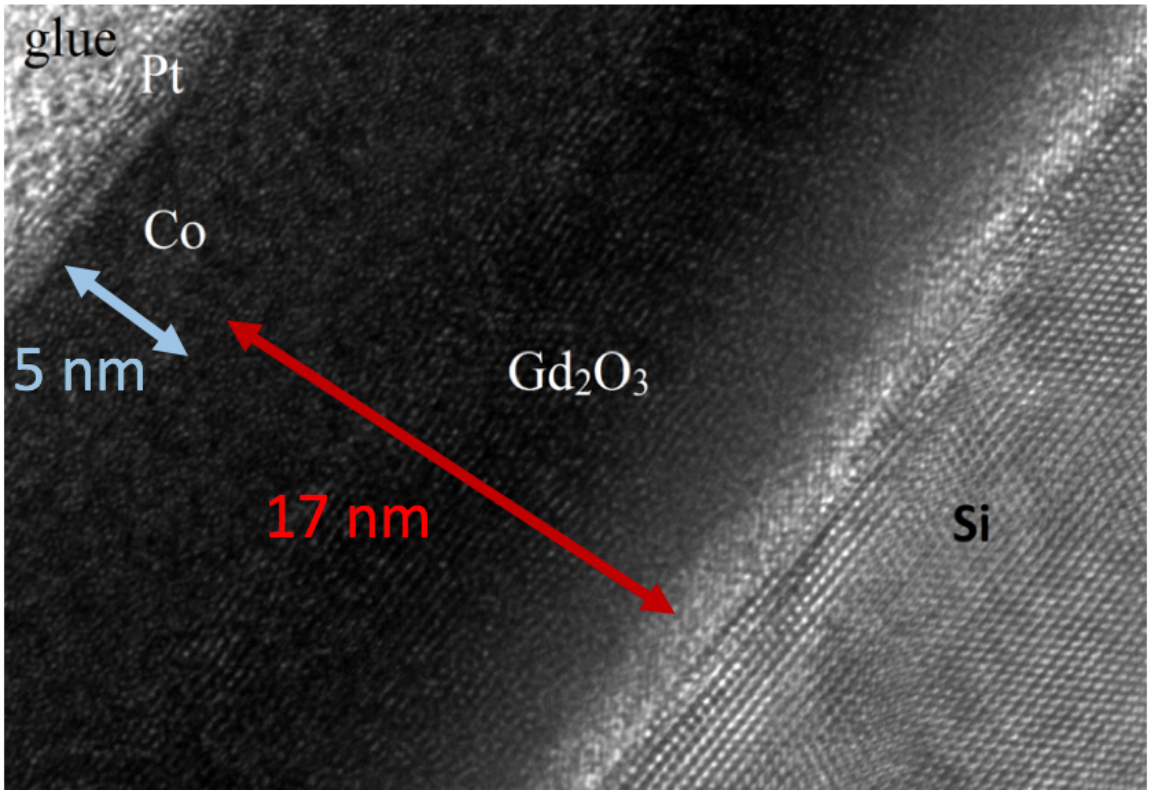


Figure 3.7: Image taken with TEM transmission electron microscope showing (lower right to upper left) the silicon wafer, the gadolinium oxide, the cobalt, ending with the thin platinum cap and the glue.

The longitudinal magnetic anisotropy (LMA), evident in the sharp magnetic hysteresis loop, disappears upon applying a gate voltage of 32 V across the p-type Si/ Gd_2O_3 (17 nm)/ Co (5 nm)/ Pt (1 nm) multilayer stack for several hours. This changing magnetic anisotropy of Co/ Gd_2O_3 heterostructure, under applied voltage has been much reported elsewhere [100-104] and is attributed to voltage controlled oxidation of Co at the Co/Gd_2O_3 interface [100-103].

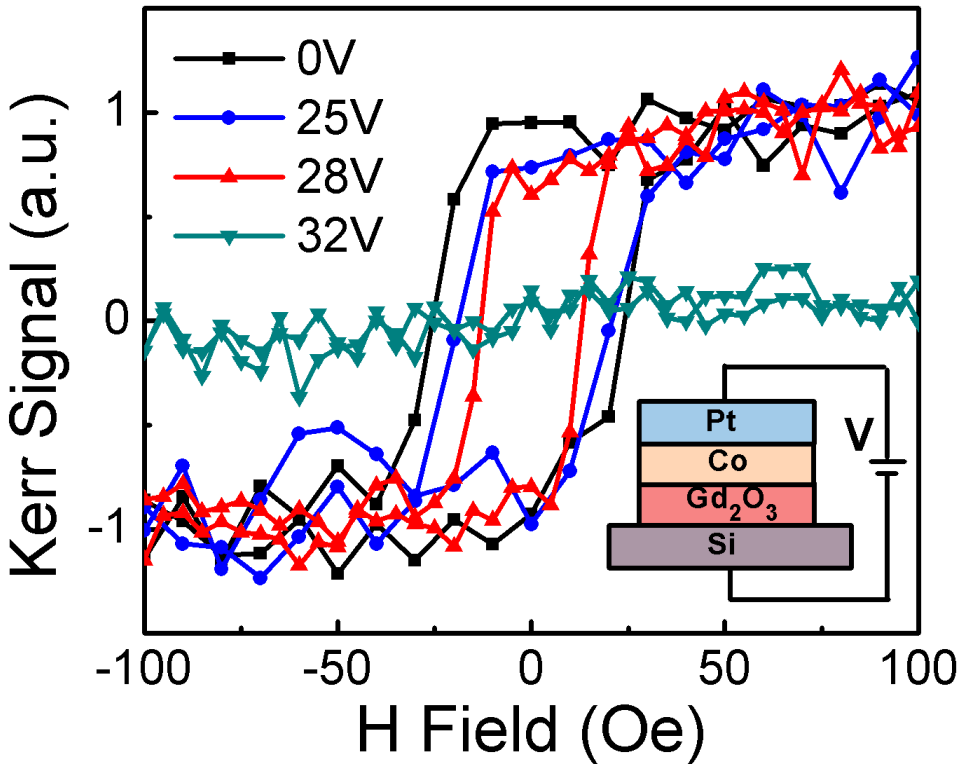


Figure 3.8: MOKE hysteresis loops measurements under different applied voltages; the schematic of the sample (inset).

This magneto-ionic voltage control of this perpendicular magnetic anisotropy of Si/Gd_2O_3 (17 nm)/Co (5 nm)/Pt (1 nm) multilayer stack is also evident in the anomalous Hall effect measurements. The anomalous Hall effect measurements indicate a significant changes in the magnetic hysteresis with a change in the sign of the applied bias across the Si/Gd_2O_3 (17 nm)/Co(5 nm)/Pt(1 nm) multilayer stack.

Figure 3.9 plots the Hall resistance after application of bias (+/- 20 V) for ten minutes, as a function of magnetic field for positive and negative biases. The hysteresis, after application of negative bias, shows a higher Hall resistance at the high applied magnetic field and a narrowing of the hysteresis loop.

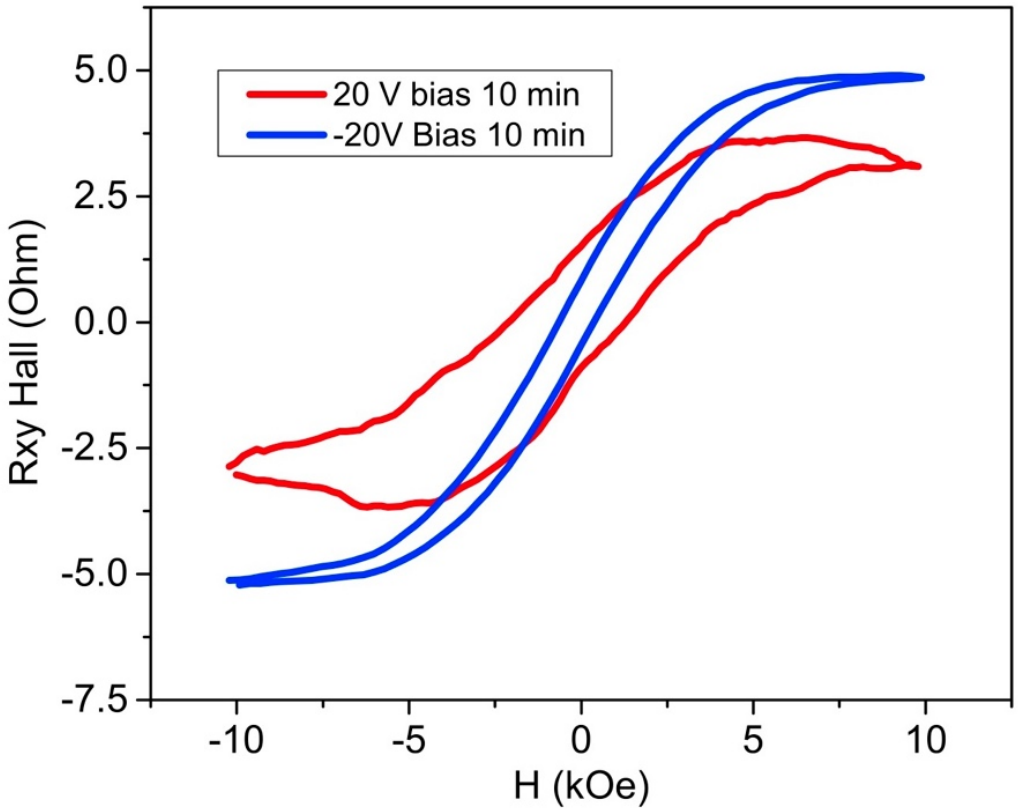


Figure 3.9: Anomalous Hall Effect measurements indicate a significant hysteresis change with a change in bias sign. The wider hysteresis obtained after 10 minutes of positive 20 V bias (red) indicates a higher perpendicular magnetic anisotropy. After 10 minutes at negative bias of - 20 V, the material becomes softer, exhibiting a lower perpendicular magnetic anisotropy.

More specifically, the wider hysteresis obtained after 10 minutes of positive 20 V bias exposure (red) indicates a higher perpendicular magnetic anisotropy. After 10 minutes at negative 20 V bias, the material becomes softer, exhibiting a lower perpendicular magnetic anisotropy. Moreover, the two curves indicate the same residual magnetization for both measurements. This indicates that the magnetic anisotropy is influenced by the external electric field.

It has been noted that these observed changes in magnetic anisotropy, with applied voltage for Co/Gd_2O_3 heterostructures, are not abrupt [100,102,103,105]. We confirm this observation

through the measured magnetic hysteresis loops, using MOKE, following application of small voltages on Co/Gd_2O_3 heterostructures, as seen in Figure 3.10. With application of a positive bias, the magnetic hysteresis loop shrinks, with a decrease of the coercive field (H_c), as is also seen in Figure 3.8. Applying 20 V on the sample, H_c is reduced by 10.52% (Figure 3.10). Changes to the magnetic hysteresis loops are quite noticeable near saturation.

As the oxygen ions move under the effect of the electric field towards the cobalt layer, creating cobalt oxide, it is expected that these magneto-ionic changes to the magnetic anisotropy depend upon both voltage and time [100,105] and also, the preference for in-plane magnetization is overcome. The original LMA can be restored following the application of a negative bias.

While domain-wall motion has been measured down a Co/Gd_2O_3 heterostructure strip [105,106], the magnetoresistance (MR) perpendicular to the plane must also exist and should vary under different applied magnetic fields and vary with voltage bias. Previous literatures showed that Co thin film has an anisotropic magnetoresistance (AMR) behavior [107], and the MR effect is negative in transverse direction with the magnitude around 2% [107]. Figure 3.11 gives the percent difference magnetoresistance ($R_\perp$) measured between H = 0 T and H = 0.2 T with the MR(%) defined as $(R_{0.2T} - R_{0T})/ R_{0T}$. Surprisingly, the system exhibits a huge negative MR at low positive voltage.

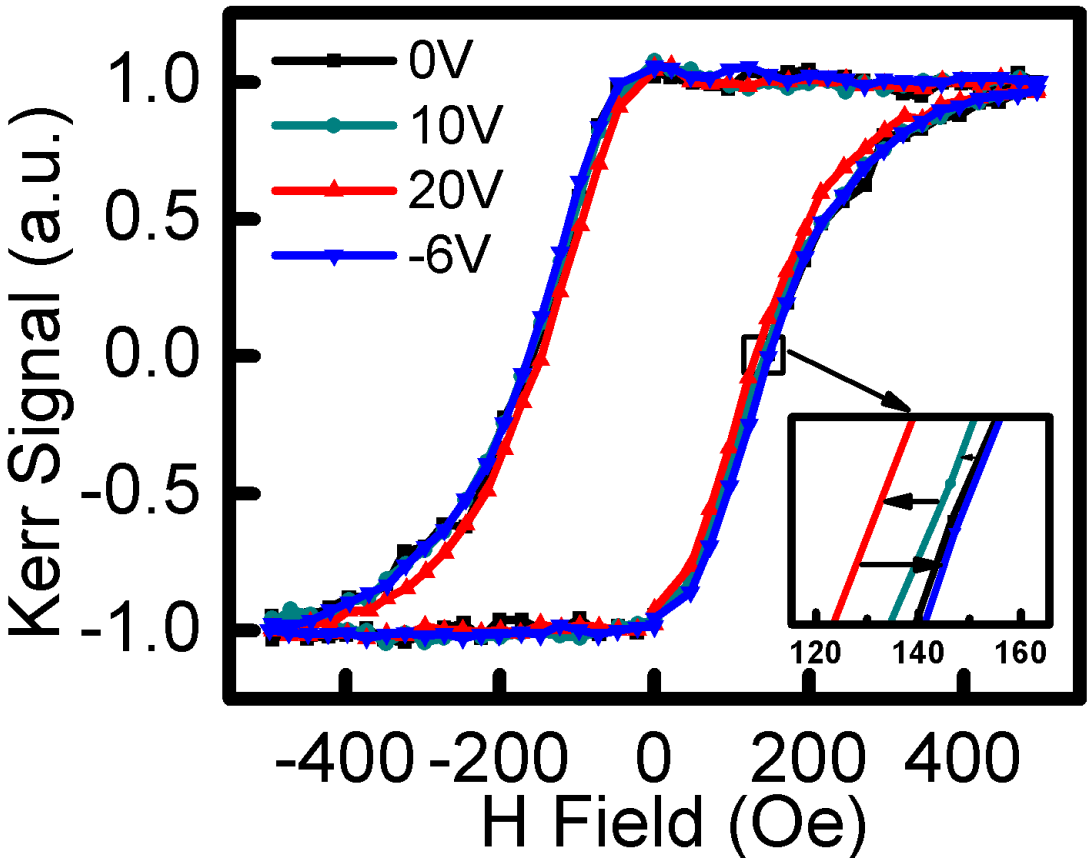


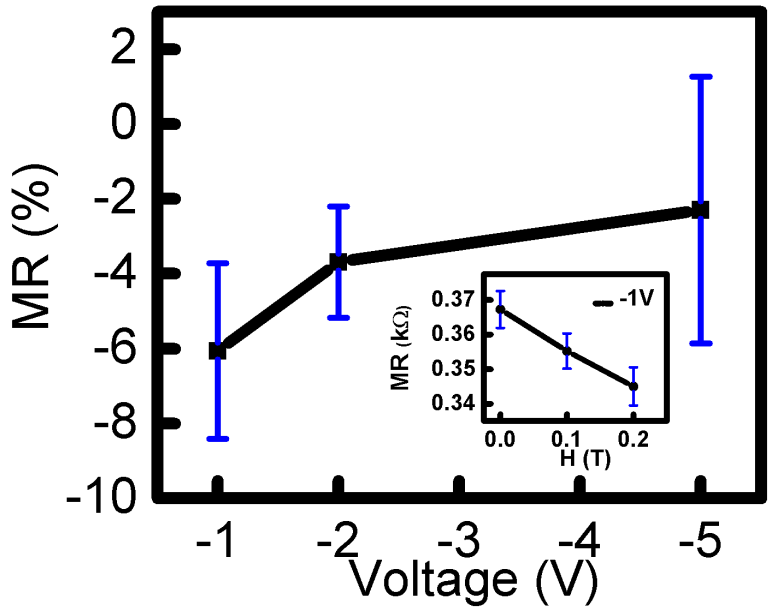
Figure 3.10: The evolution of loops under series change of bias: no bias (black, after applying V = + 10 V (green), V = + 20 V (red) and V = - 6 V (blue). The change is gradual, reversible and non-volatile.

The biggest MR ratio (-23%) in positive bias comes at the lowest voltage measured here (1 V), and under the negative bias MR is about – 6 % at – 1 V. In both cases, MR is decreased as voltage goes up. This unique large MR here may due to the metal to insulator interface at the cobalt to CoO_x/Gd_2O_3 interface. Similar large MR values were seen in ferromagnetic cobalt tunnel junctions [20], also at low bias voltages, as seen here. The fact that the MR is not symmetric with both positive and negative applied bias, as is observed here, suggests that even at low bias, I_{ON} conduction may contribute to the overall conductance.

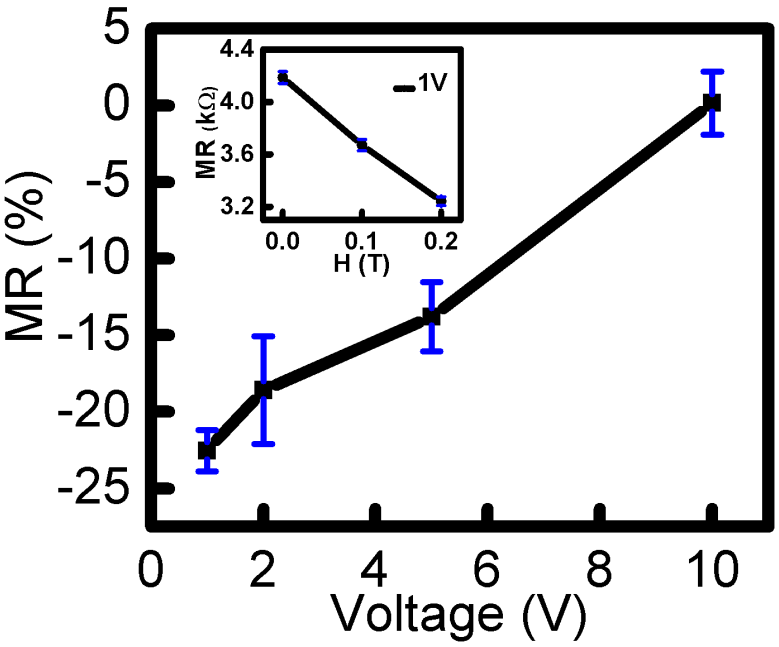
3.6.2 Summary

By conducting longitudinal MOKE measurements, our study indicates that this metal/oxide bilayer thin film has an initial in-plane magnetic anisotropy which related to the thickness of the Co layer. Applying a perpendicular voltage across the sample, results in both anomalous Hall effect (AHE) and longitudinal MOKE data indicating there is a reversible change of the magnetic anisotropy, as has been noted elsewhere [100-106], [108,109], but here is seen to be related to an anisotropic magnetoresistance.

Like the voltage controlled magnetic anisotropy known to result from changing interfacial chemistry of this system, the asymmetry in the magnetoresistance may also have an origin in this magneto-ionic effect. The results show that magneto-electric (ME) effects do not always require a ME coupling tensor. Here this is non-volatile on the scale of ME switching (<200 ps [72]) compared with much slower charge migration. This could provide some measure of non-volatility to the ME effect. These results may lead to design of new types of spintronic device, as have been recently proposed. Both trapped charge as well as a magnetic anisotropy may be exploited. Ionic conductors that would possibly provide a trapped charge, include not only Gd_2O_3 discussed here, but also NiCoO, ZrO_2 and $Li_2B_4O_7$.



(a)



(b)

Figure 3.11: The magnetoresistance (MR) ratio and MR-H curves (inset) under (a) positive bias and (b) negative bias.

CHAPTER 4

MAGNETO-ELECTRIC FIELD EFFECT TRANSISTOR[10]

4.1 Introduction

The first Spin Field-Effect Transistor (SpinFET) was proposed by Dutta and Das in 1990 [110]. Since then, there has been a lot of active research on the spin based transistors in academia and the semiconductor industry. Superficially, the device structure resembles a CMOS transistor with a source and drain acting as a spin polarizer and spin detector respectively (Figure 4.1). The voltage applied to the gate controls the channel spin precession, by the way of electric field generated due to the spin-orbit dependent Rashba effect.

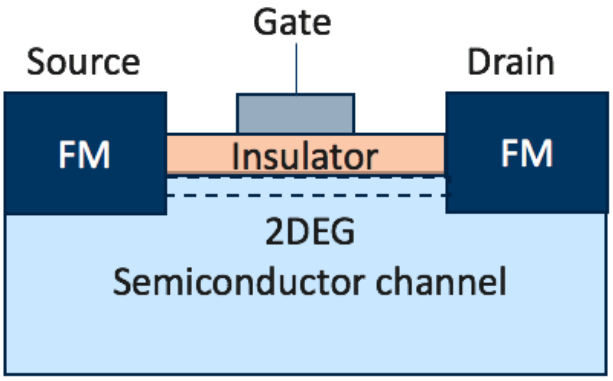


Figure 4.1: Dutta-Das SpinFET device structure.

[10]© 2017 IEEE. Reprinted, with permission, from Nishtha Sharma, Andrew Marshall, Jonathan Bird, Verilog-A based Compact Modeling of the magneto-electric FET device, 2017.

This results in a change in the drain to source (I_{DS}) current which represents the state variable of the device. Verilog-A based models have previously been proposed for the Rashba effect based SpinFET transistors in [111,112]. Unfortunately, the Rashba effect is weak making it difficult for the realization of an effective room temperature Datta-Das transistor.

As an enhancement to the SpinFET transistor, the Magneto-electric Field Effect Transistor (MEFET) device was first proposed in [113-116]. It is different from the other spin transistors as the channel is polarized by the magneto-electric (ME) chromia layer through a proximity effect. This can be exploited in the proposed device. The device works on voltages around 100 mV, possesses non-volatility due to the non-volatile AFM order of the ME and has a very high and sharp turn-on voltage [30,70]. Depending on the direction of orientation of chromia spin vectors, the channel spin vectors are oriented either 'up' or 'down'. The SpinFET also features low switching delay of 3 ps.

Two versions of the MEFET device are envisioned with a single and a dual source MEFET. Both of these allow capitalization of the devices' beneficial features, while making significant improvements to circuit capability compared to CMOS.

4.2 Single Source MEFET Device

The single source version of the MEFET, shown in Figure 4.2 is a 4-terminal device with source ('S'), drain ('D'), gate ('G') and back gate ('BG') terminals [117]. The source consists of a fixed spin ferromagnetic (FM) polarizer with chromia acting as the channel spin polarizer. The channel is made of p-type tungsten diselenide (WSe_2) which is a single layered semiconductor

with high hole mobility of ~250 cm^2/Vs and on-off ratio of ~ 10^6 [59]. There are two dielectrics at the top and bottom of the channel. The bottom gate electrode contacts the highly-resistive chromia layer [52] and the top-gate electrode contacts alumina.

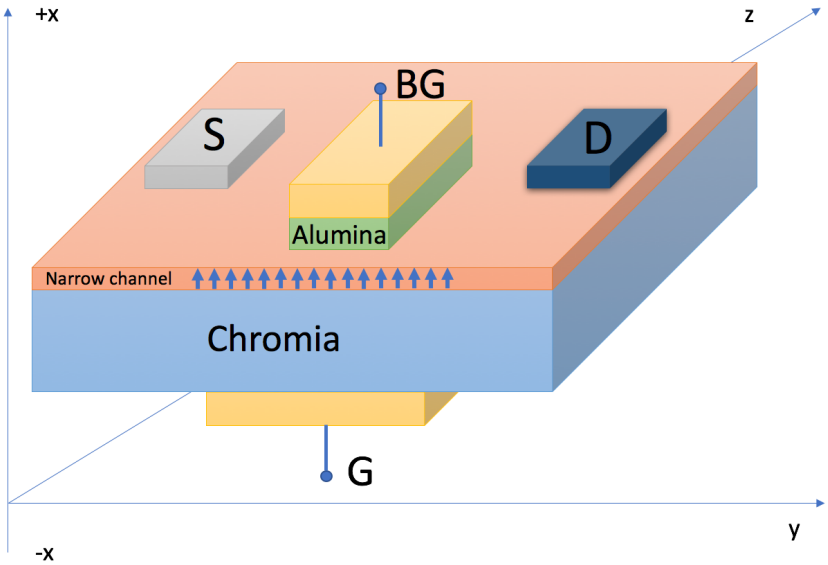


Figure 4.2: Single source MEFET device structure. © 2017 IEEE

The spin polarized current is injected into the channel through the source terminal and polarized by the chromia, resulting in a spin polarized current at the drain. Both 'up' and 'down' spins can be detected at the drain end. The 'BG' terminal is grounded and the input voltage is applied across the 'G' and 'BG' terminals to create a vertical field across the chromia layer. This is to align the chromia spin vectors either along +x or –x axis depending on the polarity of voltage applied. The state of the device is read using a MOS pull-up device.

4.2.1 Derived Devices

Complex functions like ‘NAND’, ‘OR’, majority/minority gates etc. can be obtained using the single source MEFET device. Figure 4.3 shows the circuit schematics of some of the derived functions.

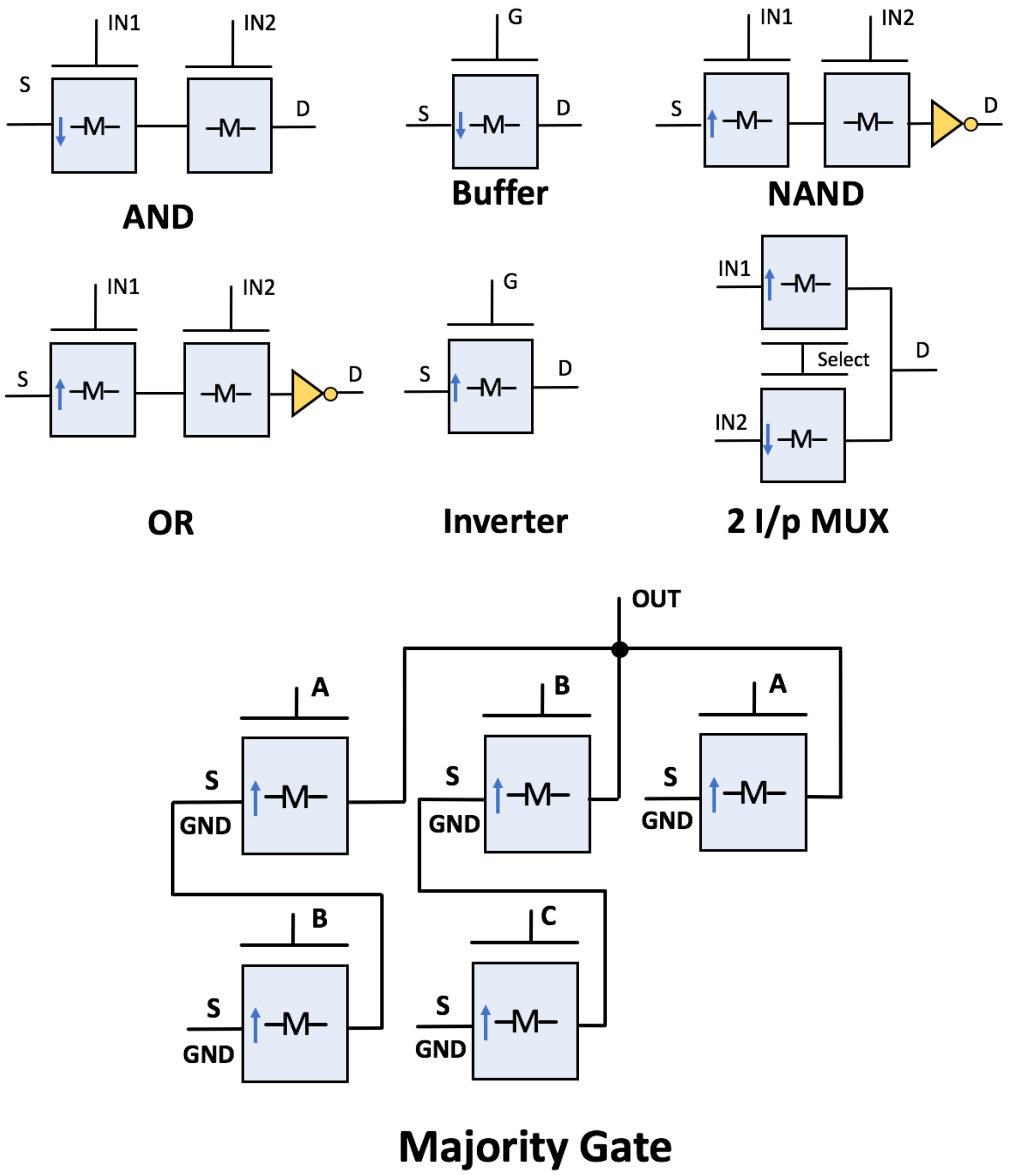


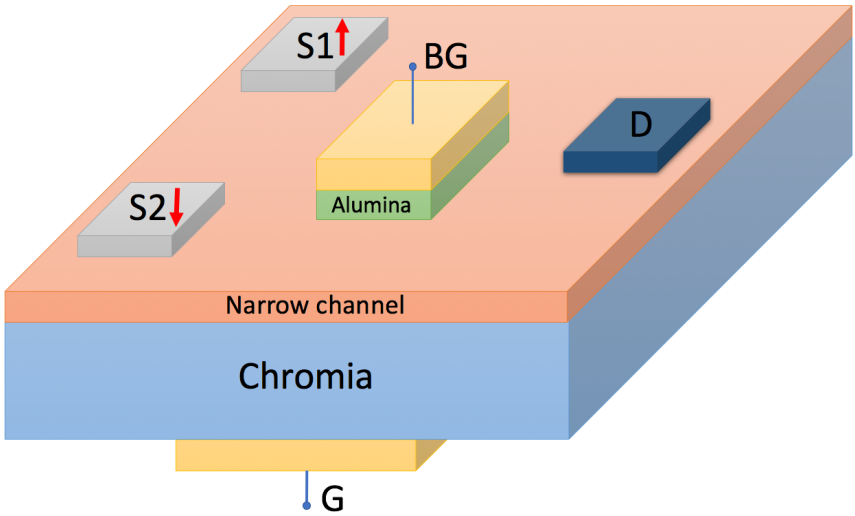
Figure 4.3: MEFET derived logic gates.

4.3 Dual Source MEFET Device

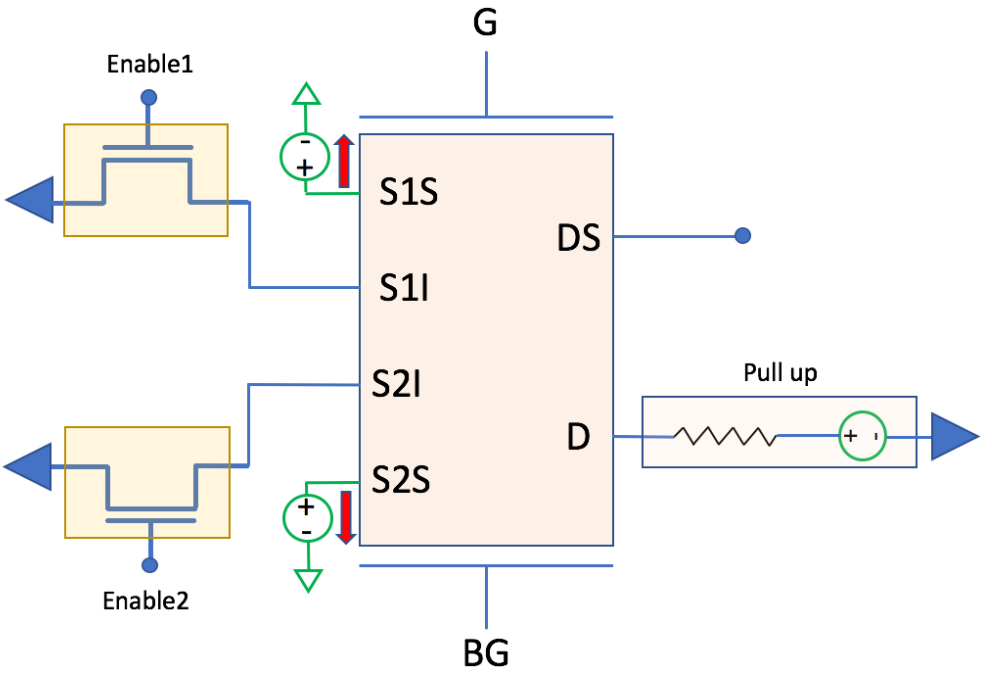
The dual source version shown in Figure 4.4(a) is a 5-terminal device with dual sources ('S_1' and 'S_2') with opposite spin polarizations, drain ('D'), gate ('G') and back gate ('BG') terminals. There are three additional terminals included in the model to detect the state of spin current injected into the source, (i.e., 'S_{1S}' and 'S_{2S}') and the corresponding spin current detected at the drain terminal ('D_S') in Figure 4.4(b). The two source inputs have fixed 'up' and 'down' spin respectively. Two NMOS transistors are used to control spin injection into the dual source MEFET. The device structure is otherwise similar to the single source version.

4.3.1 Derived Devices

In static CMOS, a minimum of two Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) are needed to implement the most basic logic function (Inverter/NOT), while the next level of logic functions such as NOR and NAND gates require four MOSFETs in most implementations to achieve two-input static logic. Each of these gates has no memory and each loses all data when powered off whereas the MEFET devices are non-volatile.



(a)

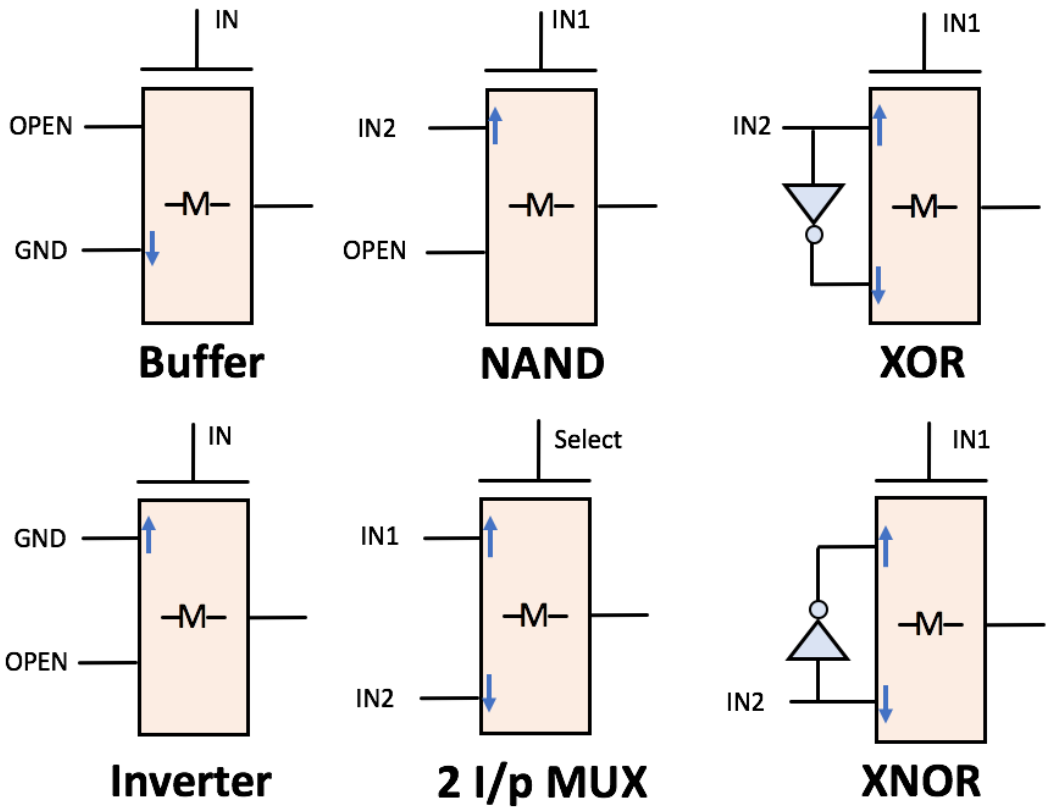


(b)

Figure 4.4: (a) Dual source MEFET device structure. (b) Circuit schematic of the device where S1S and S2S represent the source spin states and S1I and S2I represents the injected spin current.

Using the devices of Figures 4.2 and 4.4, and their memory and spin properties, we can create several logic devices. Some of these are illustrated in Figure 4.5. The non-volatility of the

logic enables supply gating, by applying appropriate clocking we are able to significantly reduce the standby power. For self-powered circuits with only an intermittent supply outage, the non-volatility feature eliminates the need for frequent back up operations, which can be time and energy consuming. The XNOR and XOR gates in MEFET are efficient compared to conventional CMOS and can be used to construct one of the standard benchmarking circuits, the 32-bit full adder.



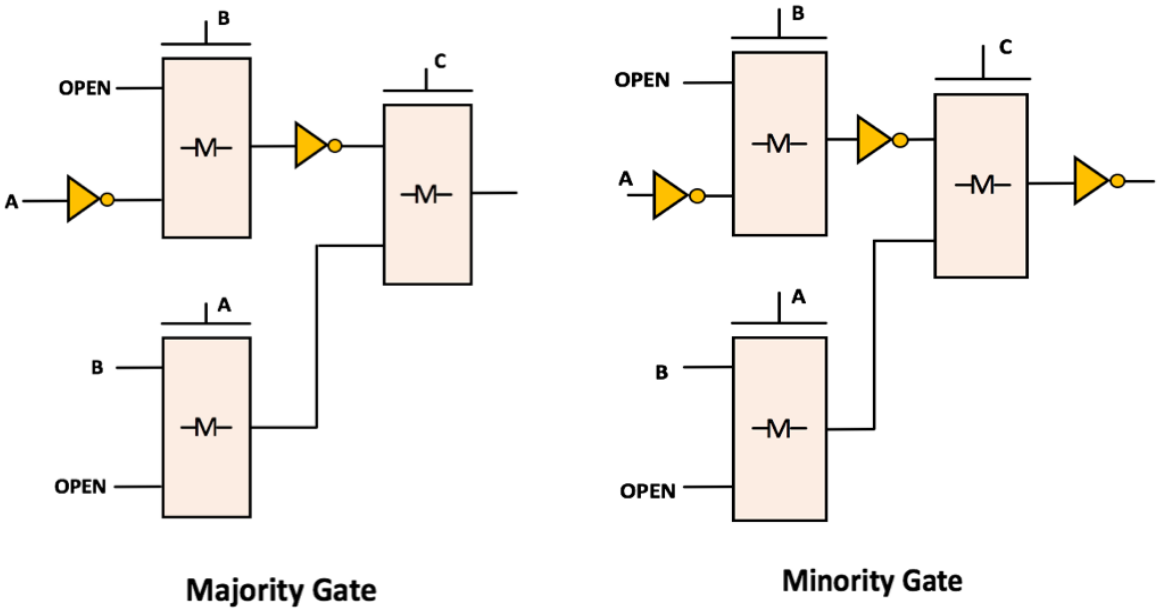


Figure 4.5: Dual source MEFET derived gates

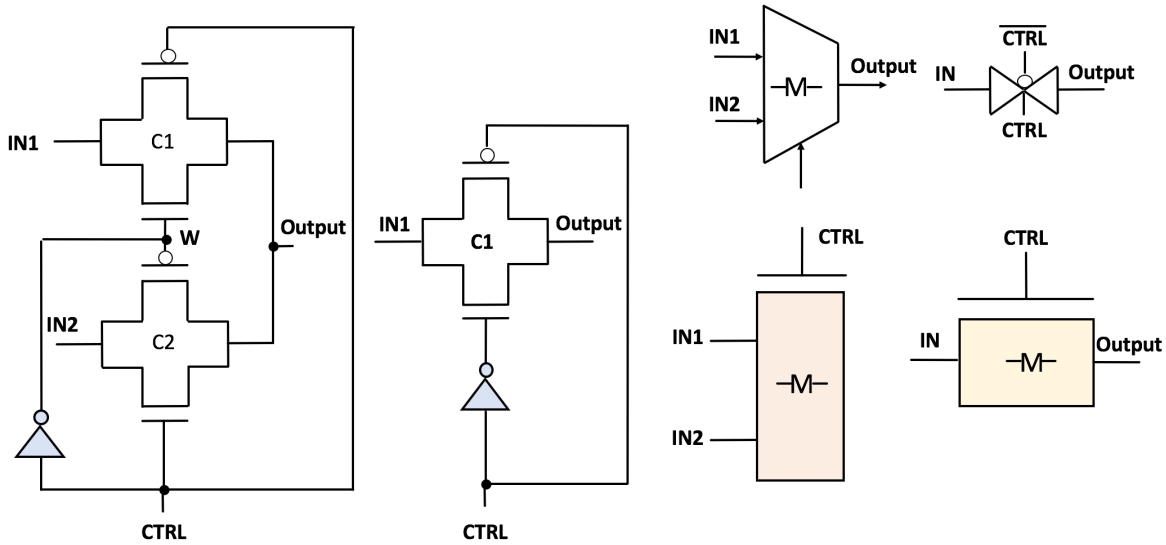


Figure 4.6: The CMOS equivalent of the MEFET multiplexer. The spin-MUXER has two inputs, one is directed via the right spin source (in1), the other via the left spin source (in2).

A very efficient 2 -input multiplexer (MUX) can also be made known as the spin-MUXer, from the dual source ME FET as shown in Figure 4.6. For a 1-bit full adder design, the spin-MUXer reduces the number of elements from roughly the 36 (comparable to CMOS), to 8, and the reduction of device elements improves the overall performance even further as shown in Figure 4.7.

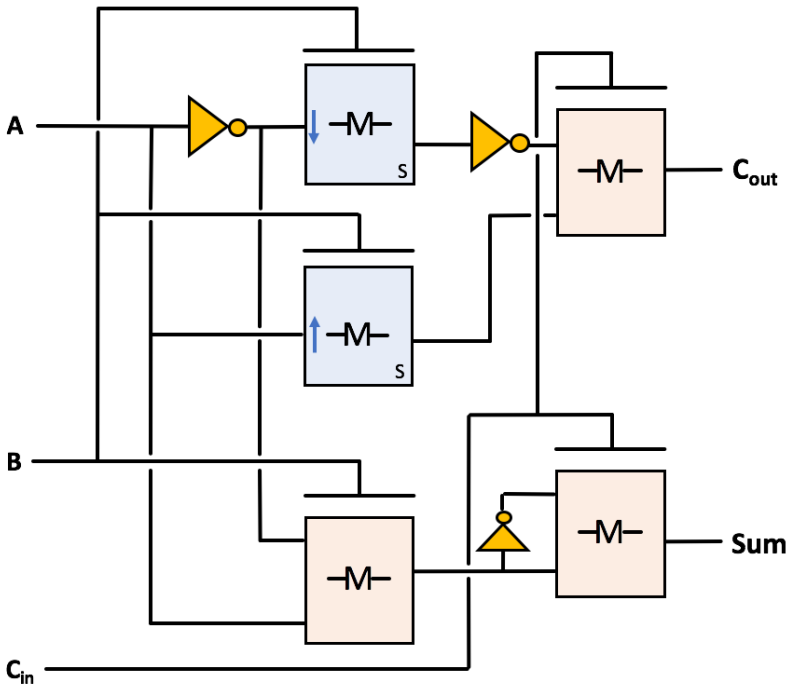


Figure 4.7: A full adder design scheme using single and dual source MEFET where the '-M-' indicates a magneto-electric FET.

4.4 Verilog-A Model

The MEFET devices can be modeled using a similar framework to that of ME-MTJ. We use a Verilog-A model, compatible with Cadence Spectre. These models accurately capture the energy consumption and the delay of the MEFET devices in a circuit configuration. The device

operation is split into three sections as shown in Figure 4.8(a). The first (input) section captures the electrical charging of the ME capacitor. Section 2 captures the delay associated with the boundary magnetization between the ME film and the interface of the narrow channel semiconductor. The final (output) section is the electrical readout of the channel spin vectors state.

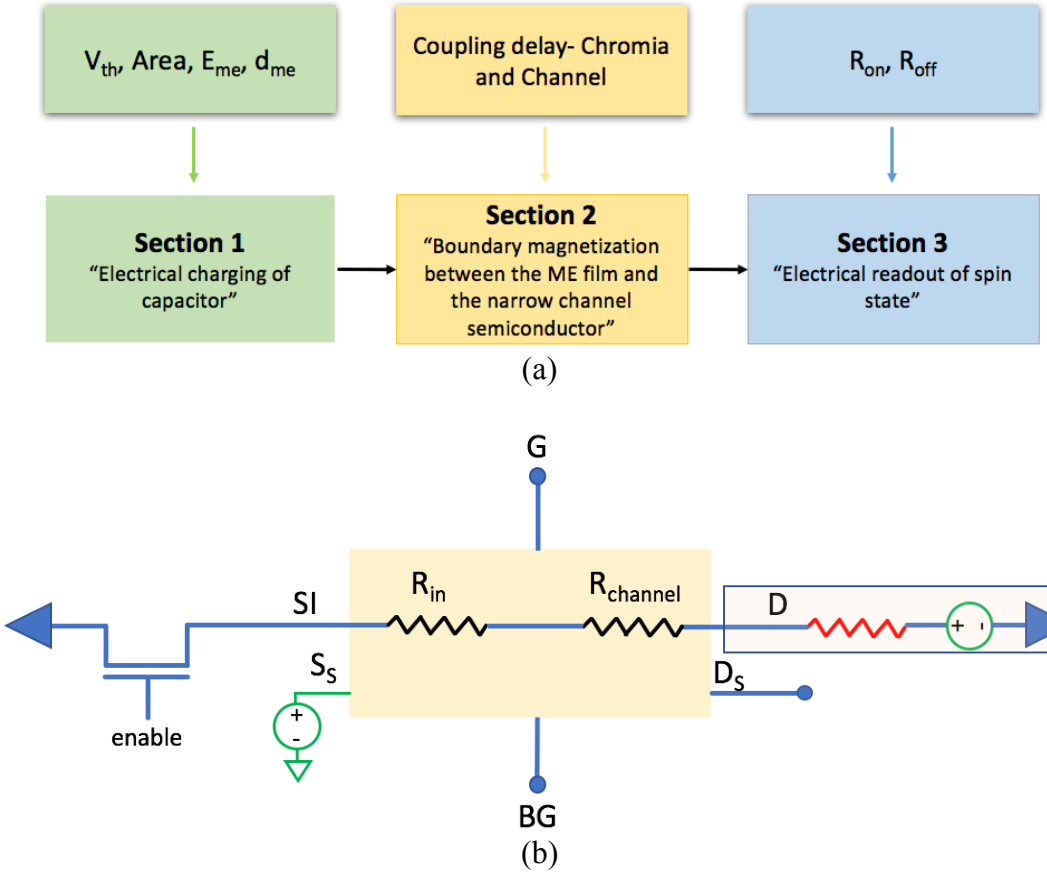


Figure 4.8: (a) MEFET modeling scheme. (b) Schematic of a single source MEFET. R_{in} and $R_{channel}$ represents the internal and channel resistance. © 2017 IEEE

For the single source version, additional spin state terminals (S_S and D_S) are added to validate the spin state injected/detected at the source/drain terminals as shown in Figure 4.8(b). S_S

is the spin state at the source (input) end and D_S is the spin state at the drain (output) end of the device. The 'up' and 'down' spins are represented by constant voltages sources with +1 V and -1 V respectively at the 'S_S' terminal.

For the dual source version, the terminals 'S_{1S}', 'S_{2S}' and 'D_S' are added shown in Figure 4.9. The model is developed such that, before the simulation is run, the injected spin orientation can be selected, making the model flexible to obtain various logic functions. $R_{channel}$ is the resistance across the WSe_2 channel and an additional resistance R_{int} is added in series to the $R_{channel}$ to define the boundary conditions for switching. The NMOS transistors are used to control the spin injection into the device. Alternatively, a MEFET device can also be used as the enable switch. Table 4.1 lists all the parameters used in the model.

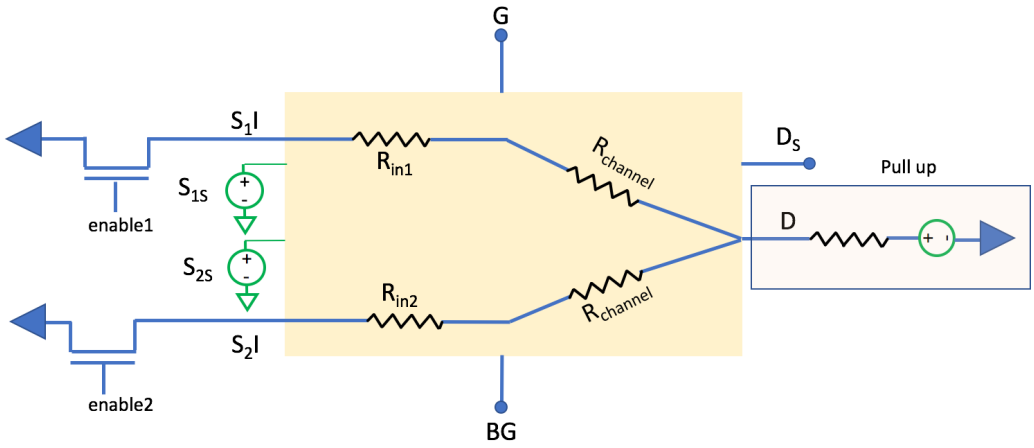


Figure 4.9: Schematic of a dual source MEFET. R_{in} and $R_{channel}$ represents the internal and channel resistance. © 2017 IEEE

Table 4.1: Compact model parameters used in the Verilog-A model. © 2017 IEEE

Parameter	Value	Description
ε_{ME}	12	Relative dielectric constant of chromia
ε_{Al2O3}	10	Relative dielectric constant of alumina
R_{off}	10^6kΩ	Off-state resistance across the channel
R_{on}	1kΩ	On-state resistance across the channel
V_{DD}	0.2V	Supply voltage in volts

4.5 Circuit Simulation

Transient simulations have been performed using the Cadence suite at a technology equivalent to the 15 nm node.

4.5.1 Single Source MEFET Device

4.5.1.1 Inverter/Buffer

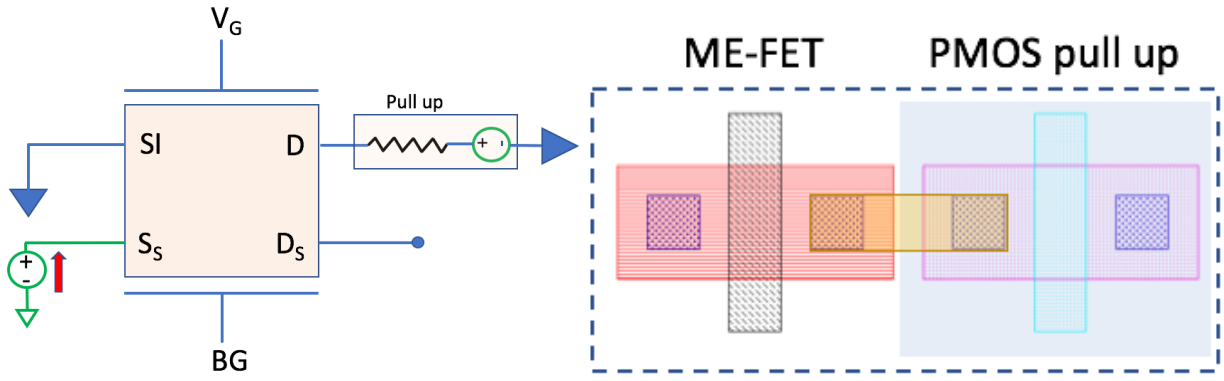


Figure 4.10: Circuit schematic (left), Cadence layout of the MEFET inverter. © 2017 IEEE

The single source MEFET device behaves like an inverter/buffer depending on the direction of spins injected into the source. Figure 4.10 shows the circuit schematic and layout of

the single source MEFET based inverter. As the gate voltage exceeds the positive switching threshold of chromia, i.e., $+V_{ME}$, the spin vectors are oriented in 'up' direction, orienting the spin vectors in the channel along the +x axis.

Thus, the spin state detected at the drain end is along +x axis, i.e., 'up' direction resulting in a low voltage at the output (18 mV) after a delay of 3 ps. As shown in Figure 4.11, when the gate input exceeds the negative switching threshold, the drain spin state and the output voltage is 'down' and high (200 mV) respectively. Similarly, a MEFET based buffer can be designed by injecting 'down' spins into the source.

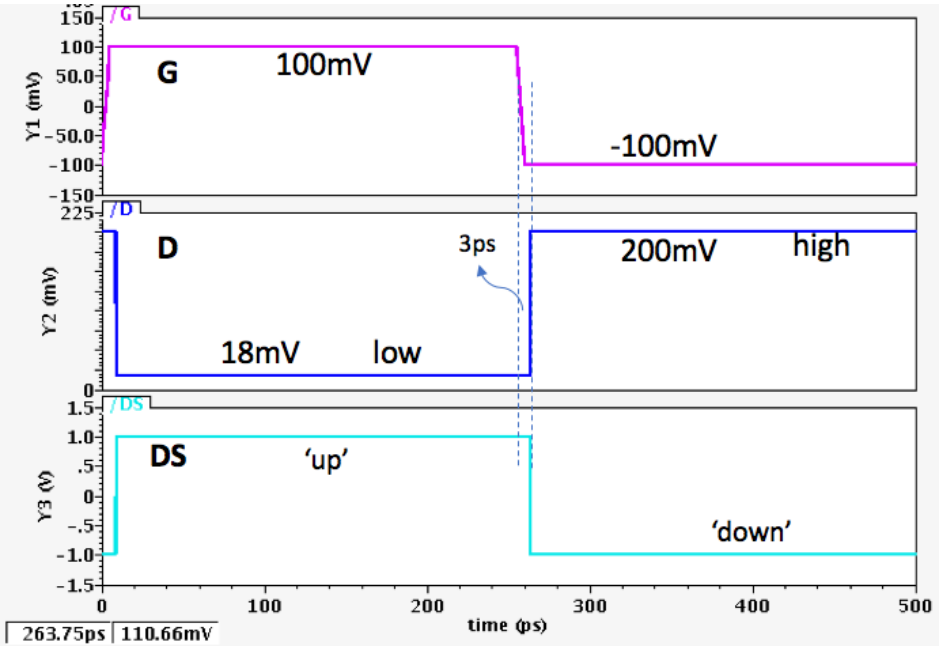
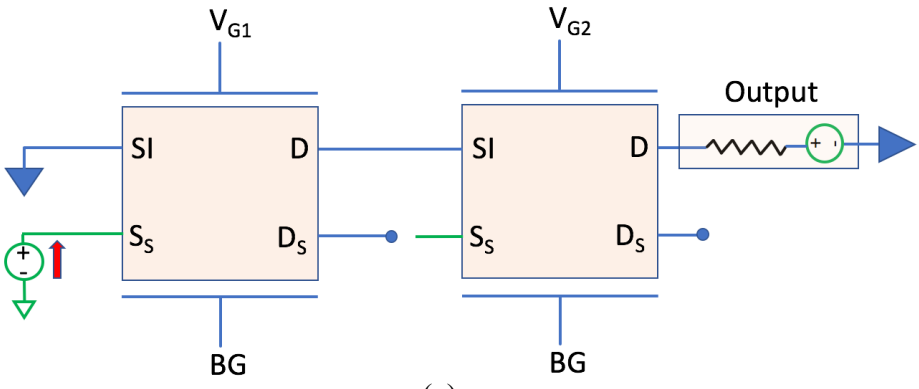


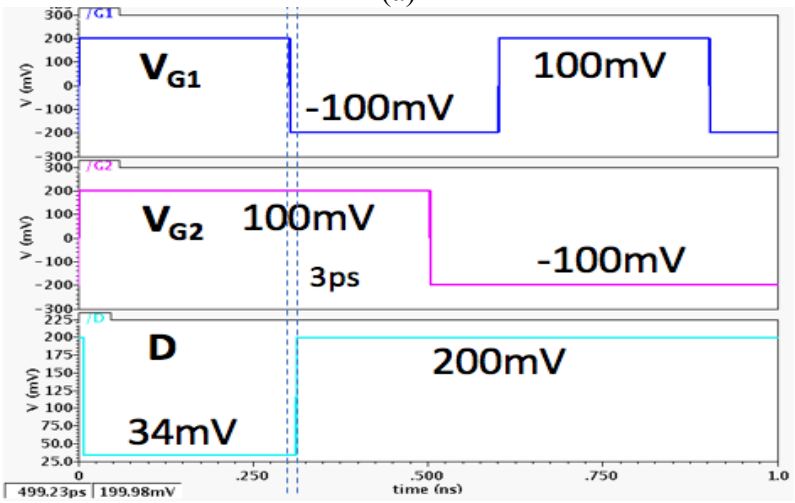
Figure 4.11: Transient simulations of the MEFET inverter. © 2017 IEEE

4.5.1.2 NAND Gate

Figure 4.12 shows the circuit schematic and transient simulation results of the MEFET based NAND gate. Two MEFETs are stacked in series such that the output spin current obtained at the drain of the first device goes into the source terminal of the second device.



(a)



(b)

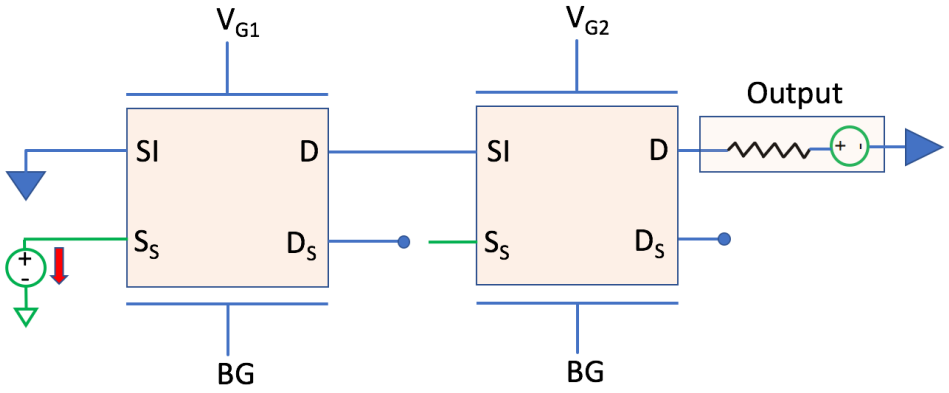
Figure 4.12: (a) Circuit schematic and (b) transient simulation results of the MEFET NAND gate. © 2017 IEEE

When ‘up’ spin current is injected into the source, the spin vectors can pass through the channel, only when both the chromia spin vectors in both the devices are oriented ‘up’ as a result

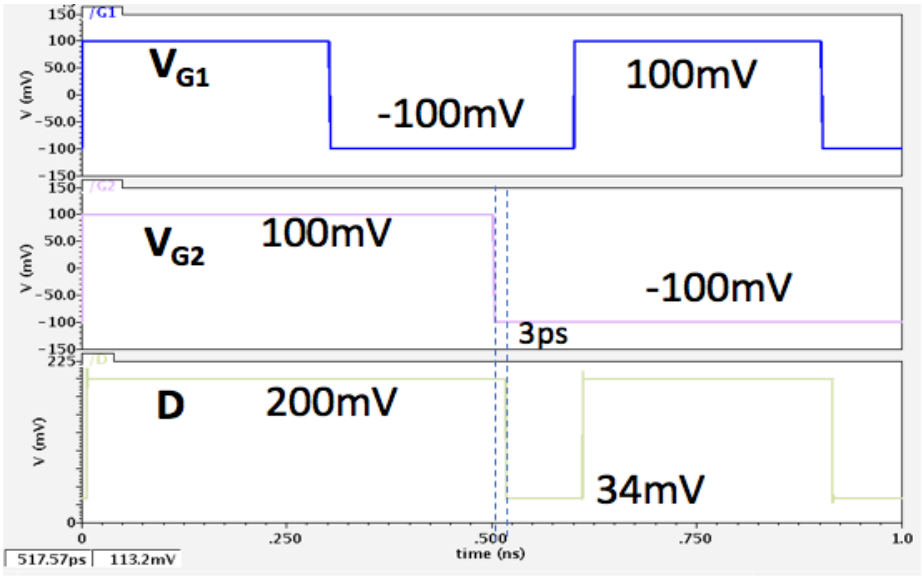
of positive voltages across both the gate terminals. The output voltage (34 mV) detected at the drain end is thus low due to there being a low resistance state across both channels. If either channel is non-conducting (high-resistance state), the voltage remains high (200 mV).

4.5.1.3 OR Gate

The same device configuration behaves like an 'OR' gate when 'down' spins are injected into the source of the first MEFET device shown in Figure 4.11. When 'down' spin current is injected into the source, the spin vectors can pass through the channel, only when both the chromia spin vectors in both the devices are oriented 'down' as a result of negative voltages across both the gate terminals. The output voltage (34 mV) detected at the drain end is thus low due to there being a low resistance state across both channels. If either channel is non-conducting (high-resistance state), the voltage remains high (200 mV).



(a)



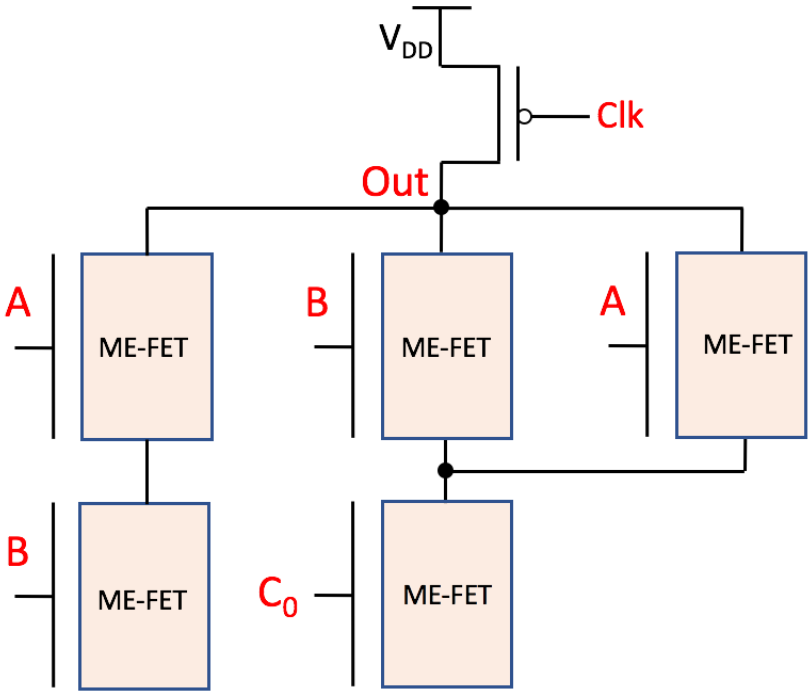
(b)

Figure 4.13: (a) Circuit schematic and (b) transient simulation results of the MEFET OR gate.

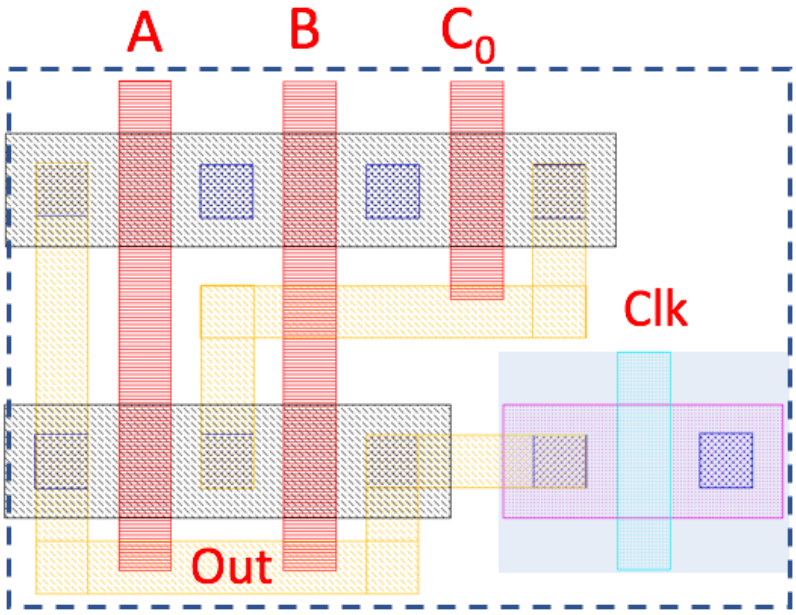
4.5.1.4 Majority Gate

A majority gate can be designed using five single source MEFET devices compared to the CMOS equivalent which requires 20 MOSFETs. This results in substantial area savings and increased performance due to reduced interconnect and fewer logic states. This gate is used in designing more complex circuits like the adder.

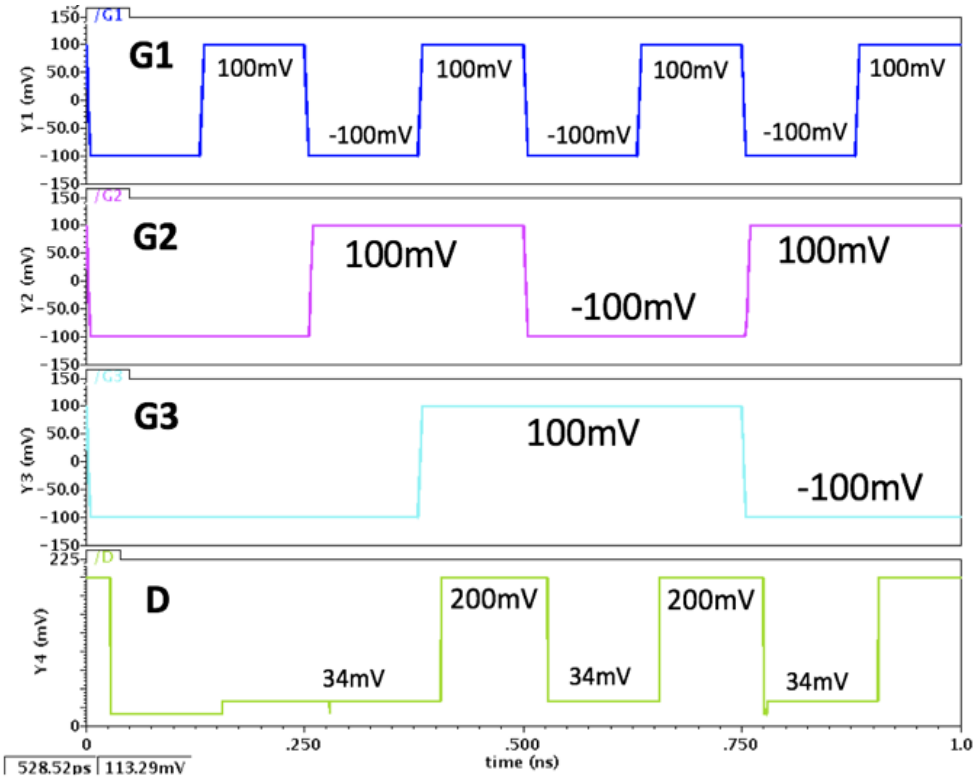
Figure 4.14 shows the circuit schematic, layout and transient simulation results of the majority gate. The operation of this gate is the same as ME-MTJ majority gate [35,93]. For obtaining the majority gate operation, ‘down’ spins are injected into the source of the single source MEFETs. The output swings between 34 mV (low) and 200 mV (high). To obtain a minority gate operation, ‘up’ spin current is injected into the source of the MEFET devices.


V_{DD}
Clk
Out
A
ME-FET
B
ME-FET
A
ME-FET
B
ME-FET
C_0
ME-FET

(a)


A
B
C_0
Clk
Out

(b)



(c)

Figure 4.14: (a) Circuit schematic (b) Cadence layout and (c) transient simulation results of the single source MEFET majority gate. © 2017 IEEE

4.5.1.5 1-bit Full Adder

A 1-bit full adder can be designed using MEFET circuit options. The full adder can be made from eight devices, as schematically shown in Figure 4.15, in around a third of the minimum number of transistors needed for the CMOS equivalent. Thus, the maximum path through the adder is just four device elements.

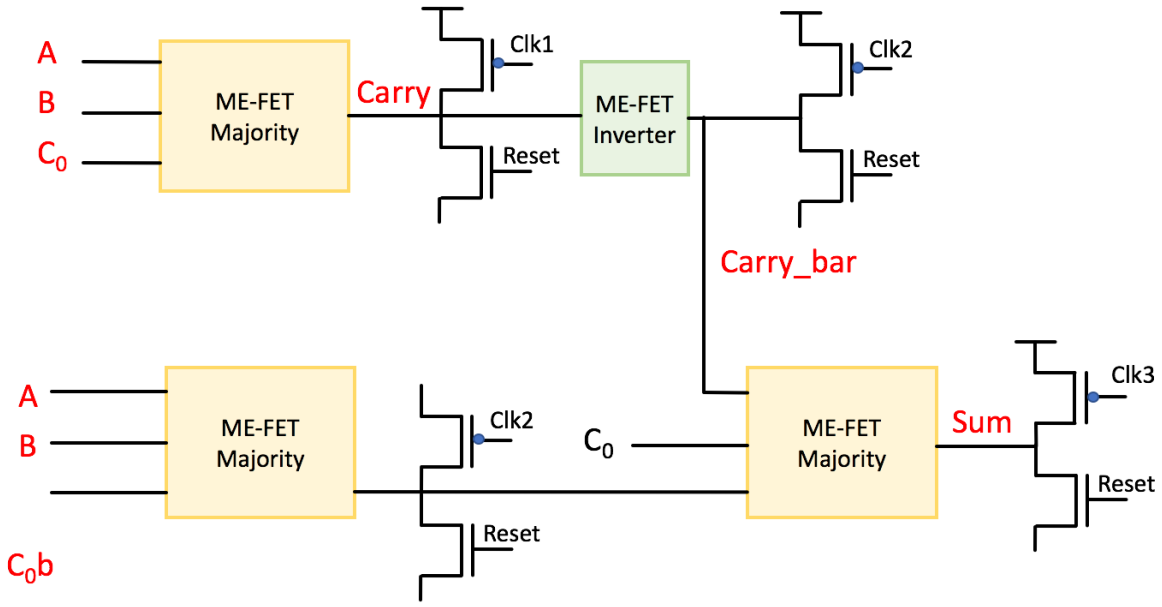
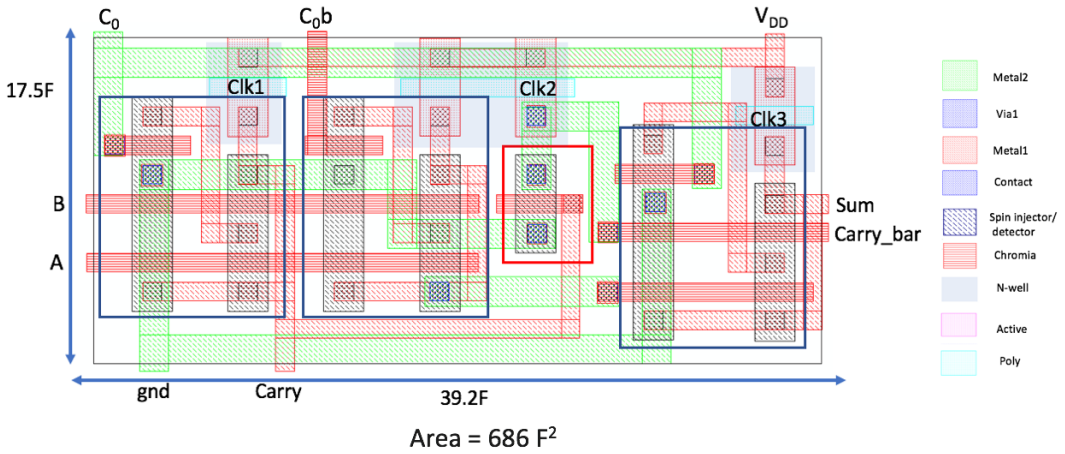


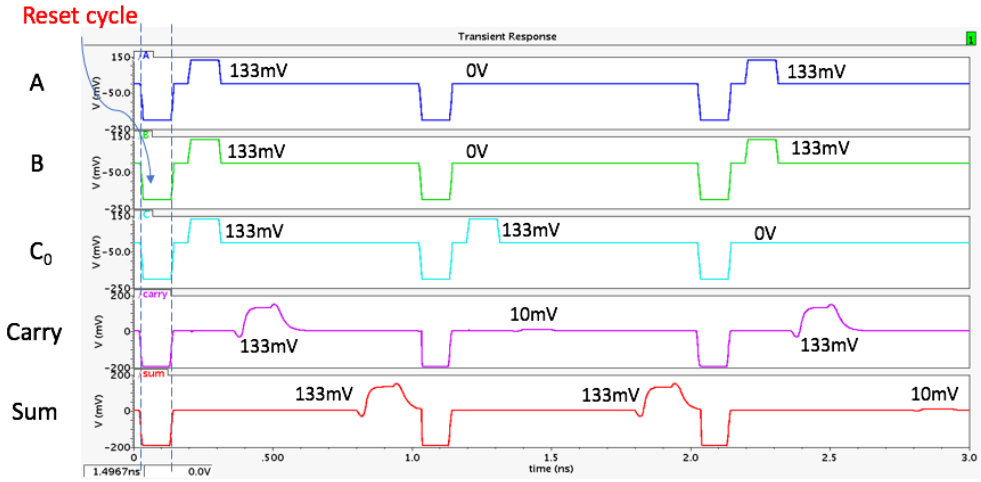
Figure 4.15: Circuit schematic of the single source MEFET 1-bit full adder.

However, the path from carry-in to carry-out is just one gate, so assuming the A and B states can be pre-loaded, the signal path through the adder is defined by a single gate. Leakage is defined by the number of gates and the clocking details. The circuit functionality is validated using Cadence Spectre. For multi-stage circuit design, reset functionality is needed to reset the state of the chromia spin vectors. At the beginning of each cycle, the circuit path is reset. The output voltage for the logic level "1" and "0" is 133 mV (high) and 10 mV (low) respectively (Figure 4.16(a)). The layout of this circuit is 674 F^2 as shown in Figure 4.16(b) compared to an area of 1590 F^2 for a CMOS based full adder [34].



Area = 686 F^2

(a)



(b)

Figure 4.16: (a) Layout and (b) transient simulation results of the single source MEFET 1-bit full adder.

4.5.2 Dual Source MEFET Device

4.5.2.1 Multiplexer

The circuit schematic and transient simulation of the dual source MEFET multiplexer referred to as the spin-MUXer is shown in Figure 4.17. Two NMOS transistors are shown at the input to control the spin current injected into the device though MEFET inputs can also be used.

As previously described, there are effectively two stages of the device that create a low resistance path between the output and only one of the inputs. The spin-MUXer selects either the ‘up’ spins or ‘down’ spins depending the polarity of applied gate voltage. The operation is shown here in two steps: In Figure 4.17, only ‘up’ spins injected is enabled and the output goes low when the polarity of gate voltage is positive.

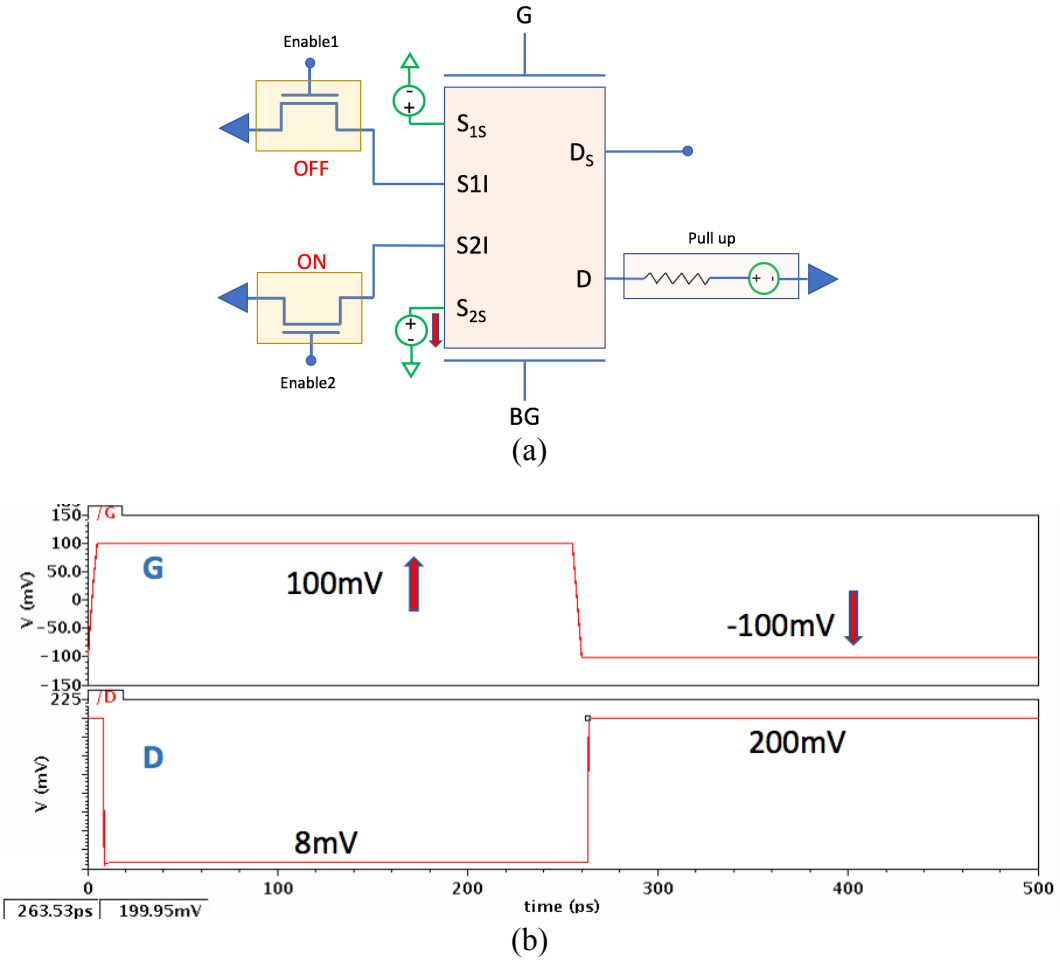
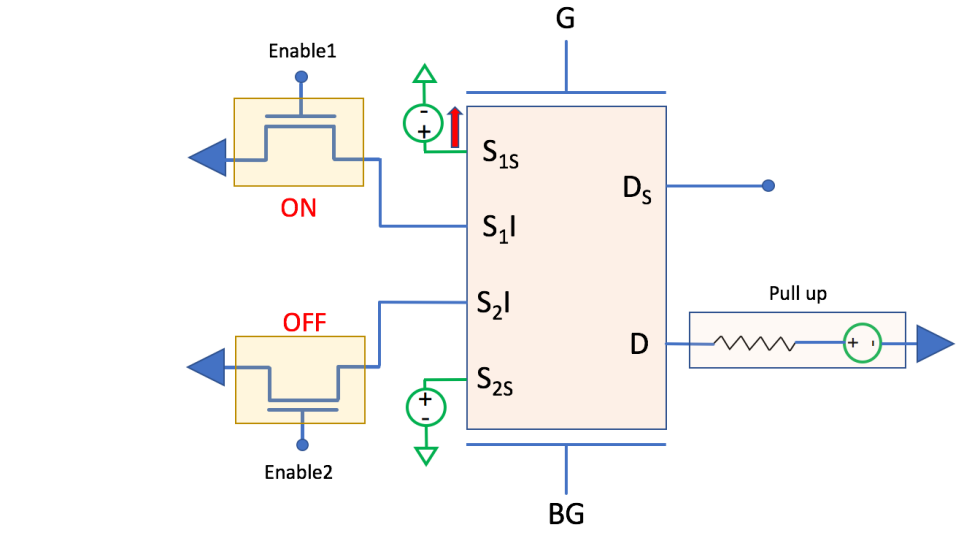
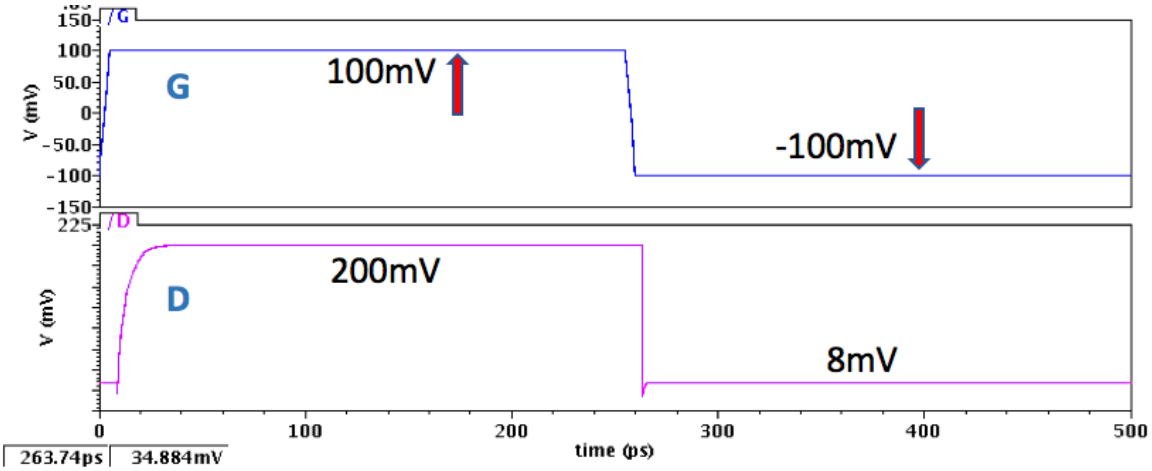


Figure 4.17: (a) Circuit schematic and (b) transient simulations of the dual source MEFET based spin-MUXer for ‘up’ spin injection.

When only ‘down’ spin is injected, the output goes low (8 mV) when positive gate voltage (100 mV) is applied as shown in Figure 4.18(b).



(a)



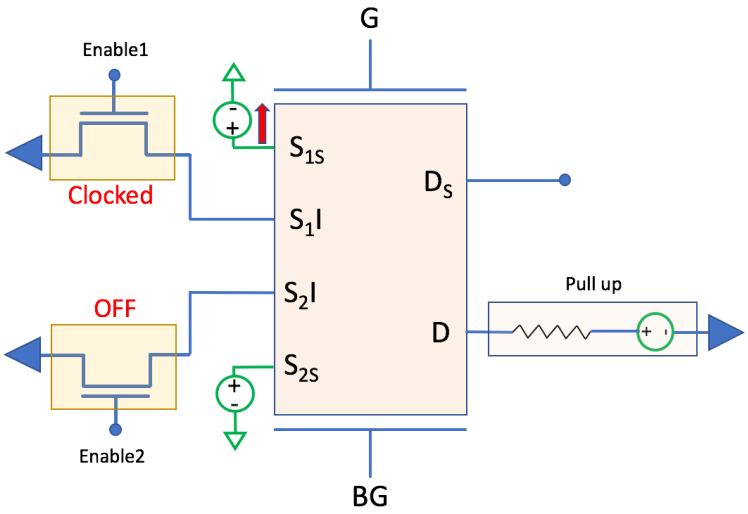
(b)

Figure 4.18: Circuit schematic and transient simulations of the dual source MEFET based MUX for “down” spin injection.

This happens due to the non-conduction of the channel. Conversely, when low gate voltage (-100 mV) is applied to the MEFET, the output goes high (200 mV) due to channel conduction. Inverter/buffer like functionality can also be derived from the MUXer. It is observed that the circuit shown in Figure 4.17(a) behaves like an inverter. Similarly, a buffer like operation can be obtained using the circuit in Figure 4.18(a).

4.5.2.2 NAND gate

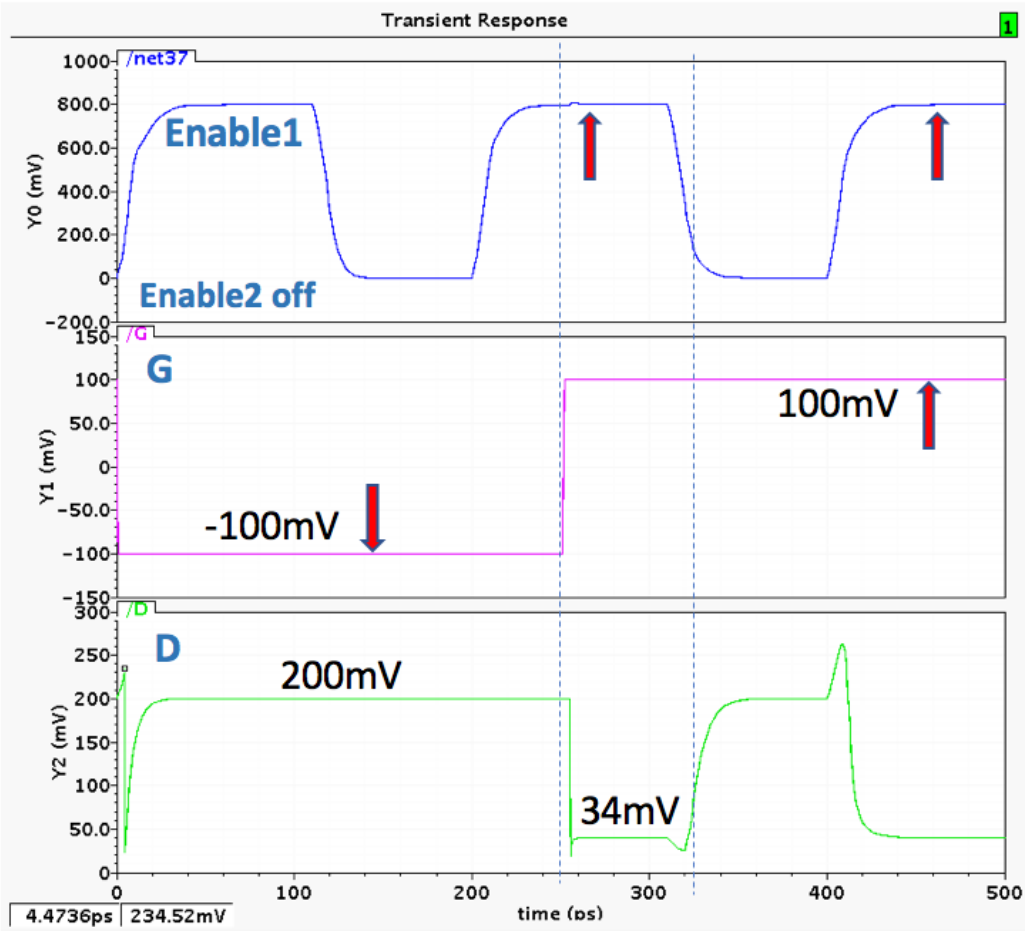
Figure 4.17 shows the circuit schematic, logic truth table and transient simulation results of the dual source MEFET based NAND gate. The function can be obtained using a single device compared to two components required in the single source version shown in Figure 4.12(a).



(a)

G	Enable1	Enable2	D
↓	↑	No 'down' spin	No spin (200mV)
↓	No spin	No 'down' spin	No spin (200mV)
↑	↑	No 'down' spin	↑ (34mV)
↑	No spin	No 'down' spin	No spin (200mV)

(b)



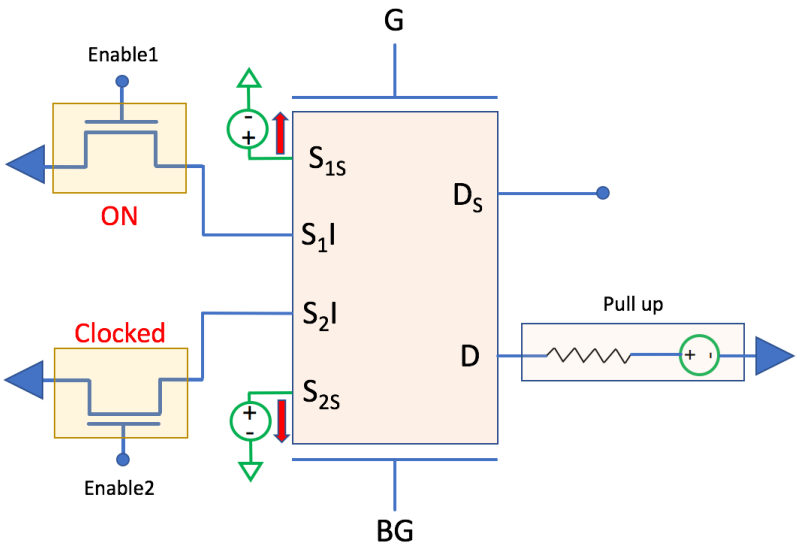
(c)

Figure 4.19: (a) Circuit schematic (b) truth table and (c) transient simulation results of the dual source MEFET based NAND gate.

The ‘up’ spin injected is clocked whereas the ‘down’ spin injection is disabled. Depending on the gate voltage applied across ‘G’ and ‘BG’, the drain voltage varies. When gate voltage is low indicating that the chromia spin vectors are aligned in ‘down’ direction, the output voltage goes high since the channel is non-conducting. When the gate voltage is high, i.e., ‘up’ spin orientation of chromia spin vectors, then the output voltage goes low (34 mV), since the channel is conducting.

4.5.2.3 NOR gate

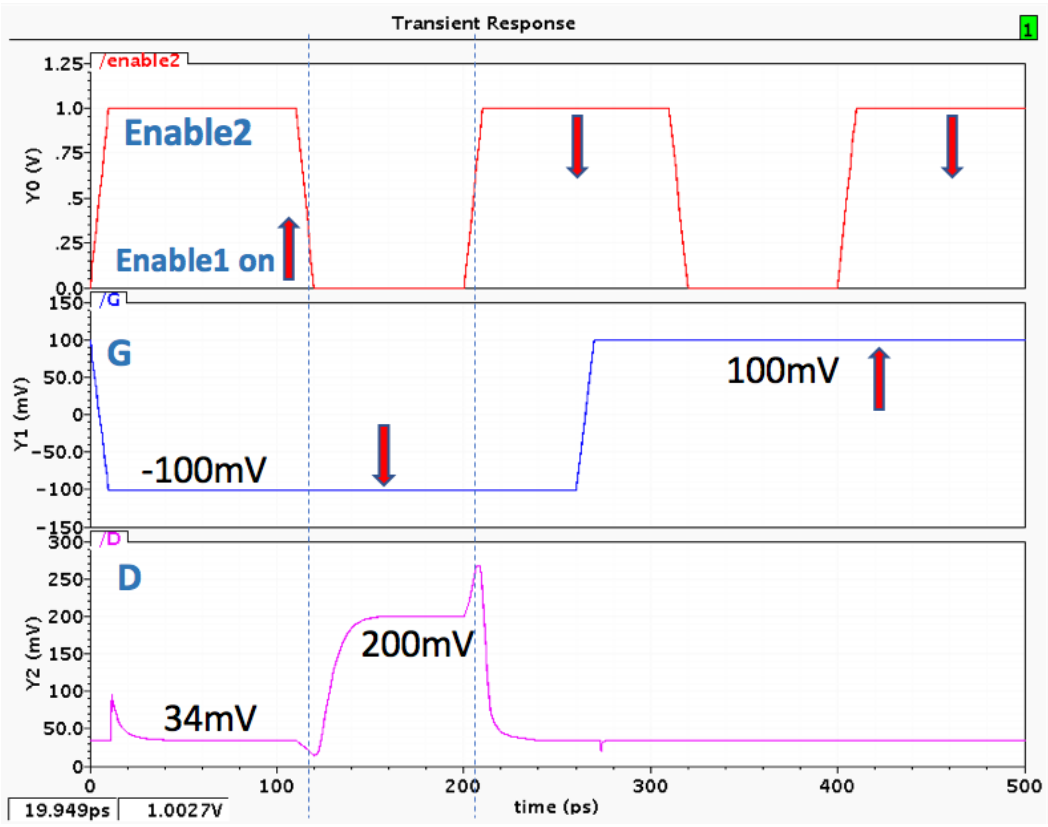
The circuit schematic and transient simulation results of the dual source MEFET based NOR gate is shown in Figure 4.20. The ‘up’ spin injected is enabled whereas the ‘down’ spin injected is clocked throughout the cycle.



(a)

G	Enable1	Enable2	D
↓	↑	No spin	No spin (200mV)
↓	↑	↓	↓ (34mV)
↑	↑	No spin	↑ (34mV)
↑	↑	↓	↓ (34mV)

(b)



(c)

Figure 4.20: (a) Circuit schematic (b) truth table and (c) transient simulation results of the dual source MEFET based NOR gate.

Depending on the gate voltage applied across ‘G’ and ‘BG’, the drain voltage varies. As shown in Figure 4.20(b), when gate voltage is low indicating that the chromia spin vectors are aligned in ‘down’ direction, the output voltage goes high since the channel is non-conducting. When the gate voltage is high, i.e., ‘up’ spin orientation of chromia spin vectors, then the output voltage goes low (34 mV), since the channel is conducting.

A variety of logic function derived from the MEFET devices have been verified for functionality using the custom designed Verilog-A models. These devices offer non-volatility, compact circuit footprint, faster write speeds (~3 ps) at lower cost in energy (~aJ) making the MEFET transistors of considerable interest for post-CMOS technology.

CHAPTER 5

CIRCUIT BENCHMARKING[11]

Benchmarking is the study and comparison of the relative performance of emerging technologies and Complementary Metal Oxide Semiconductor (CMOS). The comparison is at the circuit level and used to identify the strengths and weaknesses between technologies. Using Verilog-A models and transient simulations, energy and delay of various circuits have been estimated for Magneto-electric Magnetic Tunnel Junction (ME-MTJ) and Magneto-electric Field Effect Transistor (MEFET) devices, low-power (LP) and high-performance (HP) CMOS at the 15 nm node and benchmarked with respect to the equivalent CMOS devices. HP CMOS uses a 0.73 V supply voltage, providing the benefit of faster switching at the cost of increased energy consumption [7]. In contrast, LP CMOS uses a lower supply voltage (0.3 V) [7], providing the benefit of lower-power operation that comes at the cost of increased switching delay.

5.1 ME-MTJ Benchmarking

All of the ME-MTJ devices display a similar delay of 200 ps as shown in Figure 5.1. Contrast this with the delay of the CMOS equivalents where significant increases in the delay is observed as computation complexity (inverter → Majority logic → XNOR) increases. The CMOS behavior reflects the need for increasing numbers of Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) to implement these logic operations; a CMOS XNOR/XOR gate, for

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example, requires some 12 MOSFETs, whereas the ME-MTJ version of each of these gates can be implemented with just a single device.

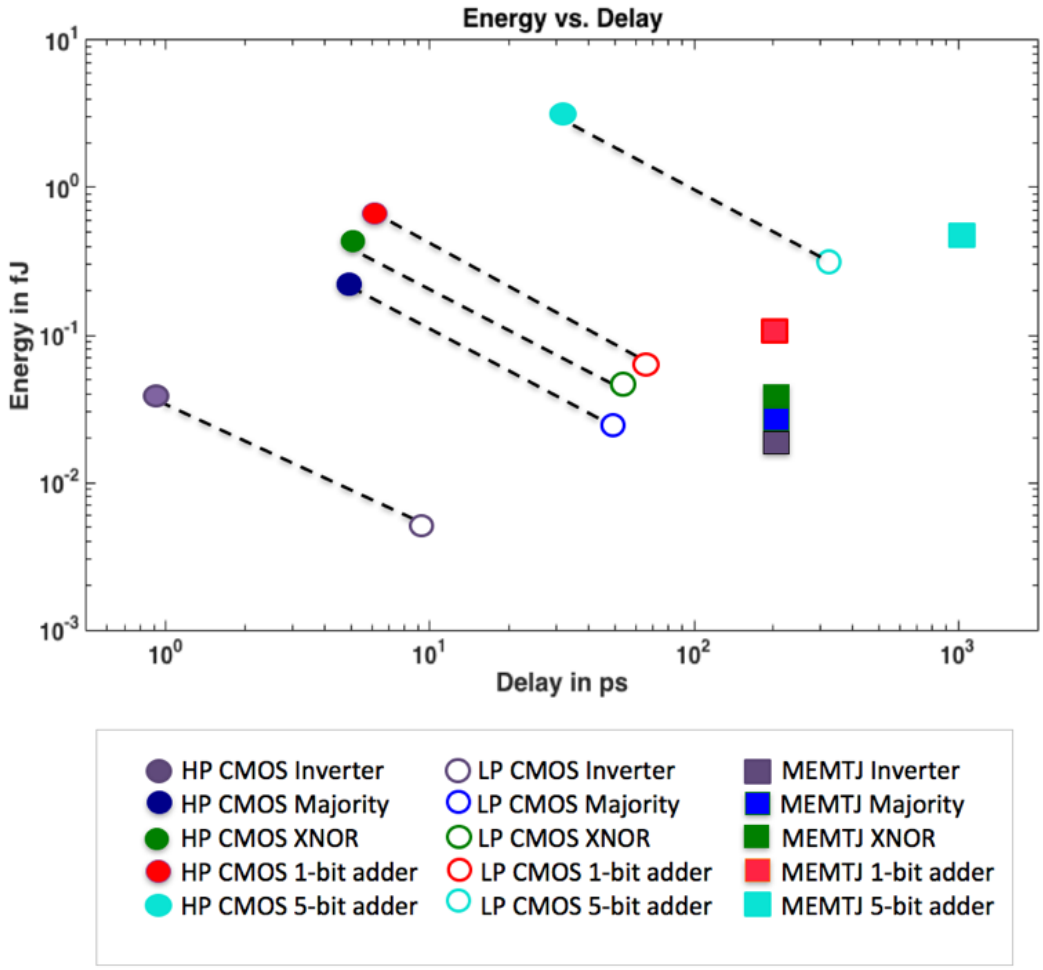


Figure 5.1: Benchmarking of the ME-MTJ device with the CMOS equivalents. © 2017 IEEE

In contrast to CMOS, the small Tunneling Magnetoresistance (TMR) values of typical magnetic tunnel junction (MTJ) mean that they continue to pass significant current, even in the 'off' state. The ME-MTJ majority gate consumes the most energy since it is driven by a higher supply voltage which increases leakage.

The ME-MTJ inverter and XNOR/XOR gate are identical in terms of energy, since both devices are driven by the same voltage. The XNOR/XOR gate is particularly attractive since the device permits the smallest possible gate, and formation of multiple magneto-electric (ME) domain formation is not an issue. Thus, as complexity of the logic increases, ME-MTJ devices improves with respect to CMOS in terms of energy. Due to the large coupling delay of 200 ps between chromia and 'fixed' ferromagnetic layer, the delay for these devices is higher compared to CMOS equivalents.

5.2 MEFET Benchmarking

The MEFET devices described in chapter 4 are here benchmarked with respect to CMOS devices in terms of energy and delay as shown in Figure 5.2. The switching speed for the standalone MEFET device is between 3 ps and 20 ps, giving a range of possible energy and delays. The delay for the MEFET devices can be attributed to the boundary magnetization time-constant between the chromia layer and the narrow channel semiconductor, and is incorporated in the Verilog-A model. The energy can be attributed to the leakage components due to the CMOS pull-up device which is required to read the output state of the device.

For inverter operation, CMOS has better performance than the MEFET. However, for more complex circuits, such as the CMOS 1-bit full adder which requires up to 36 MOS components the MEFET based adder has better energy-delay performance, as it requires only 15 components including the read and reset circuitry (Figure 5.2).

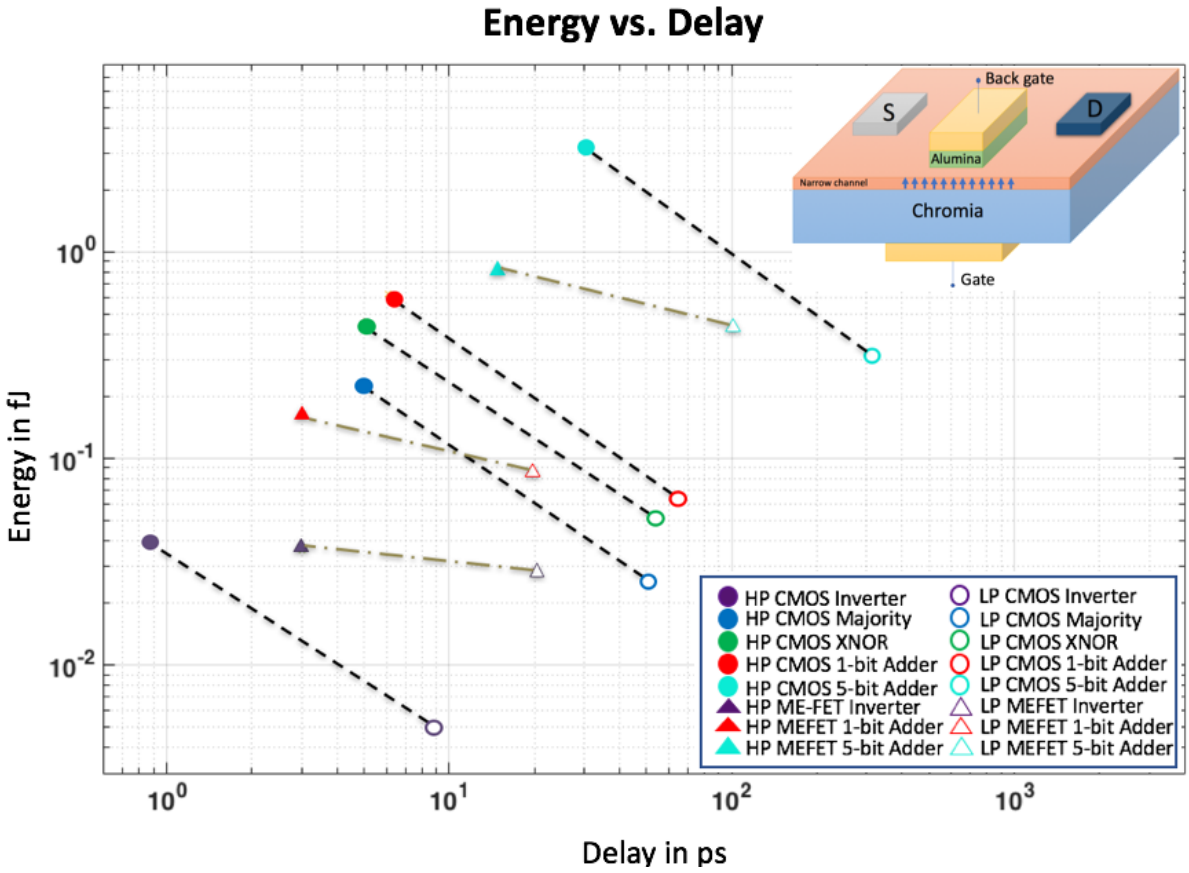


Figure 5.2: The single magneto-electric spin transistor (triangles) is compared to high-performance (filled circles) and low performance (open circles) CMOS. The switching speed is estimated to lie between 3 ps (filled triangles) and 20 ps (open triangles) for an individual magneto-electric spin transistor, giving a range of possible energy versus delay estimates (dashed-dot lines).

5.3 Center for NanoFerroic Devices (CNFD) Memory Benchmarking

A variety of magneto-electric and ferroelectric (nanoferroic) logic devices are benchmarked with respect to CMOS for performance and power. The technologies compared have been studied previously for their logic capabilities [34,35,37,38,40,42]. Models for switching mechanisms use MATLAB decks, and are aligned with those used in [44] to obtain switching delay and energy for intrinsic elements (transistors or nanomagnets). The devices can be fabricated

at BEOL of the CMOS process. The power associated with these devices can be estimated using Table 5.1. Please note that the column select may be of CMOS or a tunnel FET, and may therefore contribute leakage.

Table 5.1: Method for estimating power.

Power/bit	**Formula**
Write power	Write voltage * write current, plus leakage
Read power	Read voltage * read current
Standby power	~Negligible

5.3.1 Memory Cells for Comparison

The list of parameters for comparison may be found in the 2014 ITRS report on Emerging Research Devices (ERD) [90]. The memory can be split into the basic cell, the selector that allows write and read, and the array, where much of the cell read and write delay occurs. At the edges of the array additional circuitry for read and write is needed. The read is generally analog circuitry, and here it is assumed the read circuit is available that is compatible with the array. This is illustrated in Figure 5.3. DRAM and flash are the baseline reference, as found in typical standalone memory arrays.

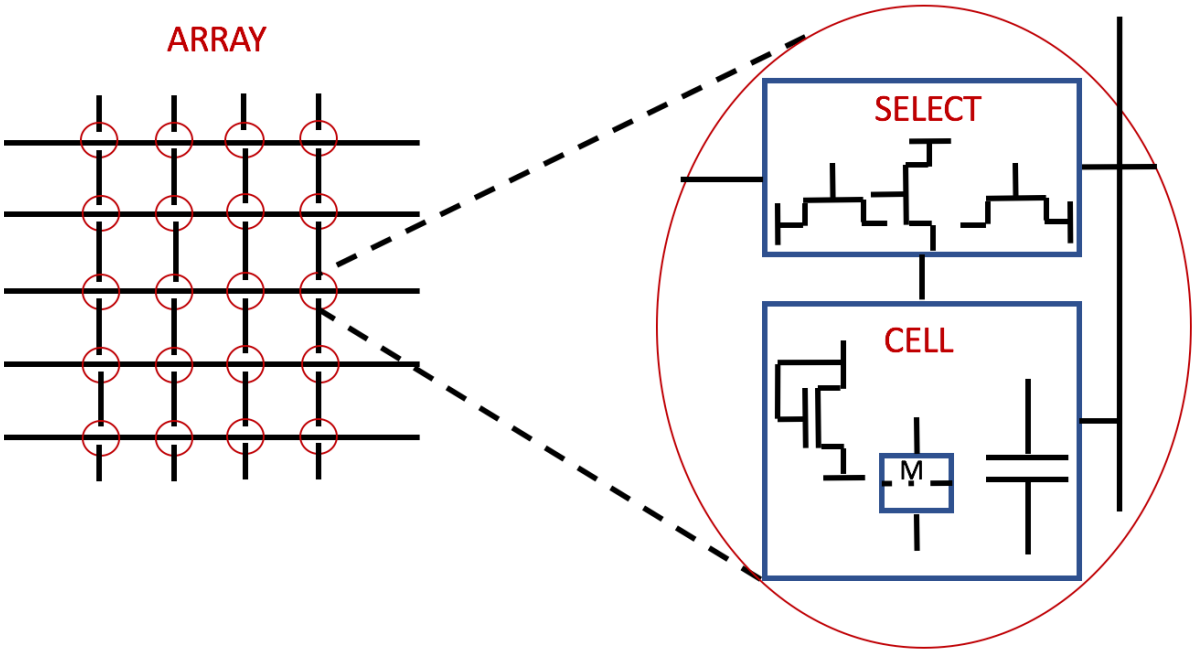


Figure 5.3: Cell, Select and Array depictions for various memory arrays.

5.3.2 Dynamic Random-Access Memory (DRAM) Cell

Dynamic RAM (DRAM) is where periodic refreshes are necessary or non-volatile memory devices where no power needs to be supplied for data retention, as for example flash memory. The DRAM cell size is: 4 x 5.3 or 21 F^2 (Figure 5.4), though diagonal packing reduces this to close to about 16 F^2 value.

5.3.3 NAND Flash Cell

The current NAND flash structure is around the smallest available for a non-volatile cell. While DRAM and SRAM type cells have benefits in some applications, a non-volatile cell with

retention when power is not being supplied has many advantages. Figure 5.5(a) shows an individual floating gate device.

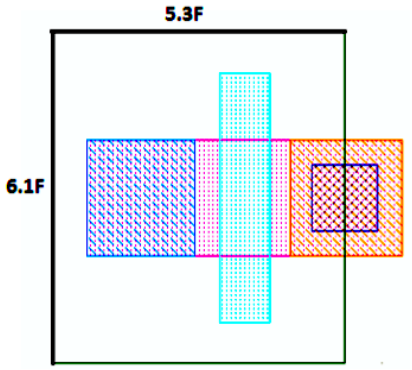
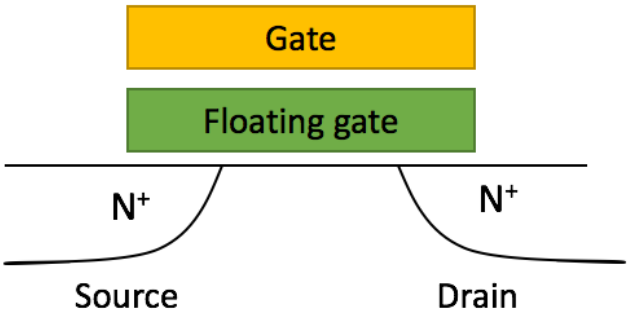
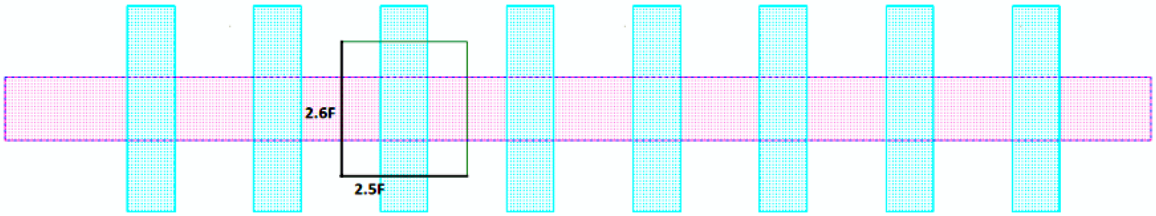


Figure 5.4: Circuit layout of a CMOS DRAM cell. In terms of F, the area is 32.3 F^2.

Typical actual size of this type of cell is 4 F^2 (based on technology node half wordline pitch). Using the non-optimized layout rules scheme used here, the device is: 6.5 F^2 (Figure 5.5(b)). The NAND flash is a relatively slow memory, but is non-volatile, a huge advantage for power consumption. It is, however, known to suffer wear-out after many state-cycles.



(a)



(b)

Figure 5.5: Diagram showing an individual NAND floating gate transistor. In terms of F, the area is 6.5 F². © 2015 IEEE

5.3.4 Magneto-electric Magnetic Tunnel Junction (ME-MTJ) Device

The ME-MTJ is a device in which the conventional spin-dependent functionality of the MTJ is greatly enhanced through the integration of novel magneto-electric materials as discussed in chapter 2. This device can be configured in a manner similar to NAND flash, though because of a relatively low I_{on}/I_{off} ratio it is unlikely that the devices can be stacked to the same level as a conventional NAND flash.

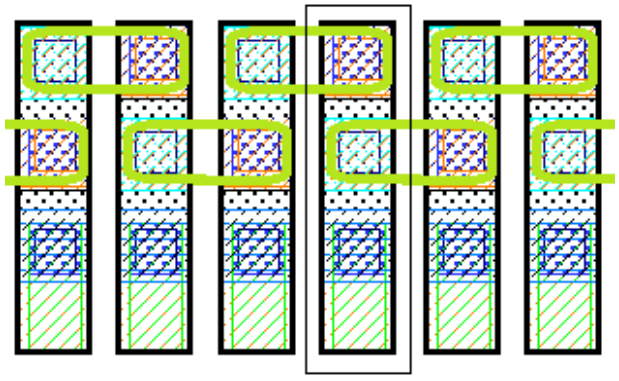


Figure 5.6: Layout indicating unit cell of ME-MTJ stacked memory, using design rules of [7]. The area of a single ME-MTJ device is 24 F^2. © 2015 IEEE

Nevertheless, it is potentially a useful memory type as it can be integrated onto conventional silicon CMOS, without significant CMOS area requirements, so the basic cell size at 24 F^2 (Figure 5.6) is larger than the flash cell, but can be placed over the top of CMOS logic. The clocking and reset don't necessarily consume extra area as CMOS can fit underneath the ME-MTJ. Write and read voltage for this device is 0.1 V.

5.3.5 Ferroelectric Tunnel Junction (FTJ) Cell

The FTJ device uses programmable electric polarization to strongly modulate the tunnel probability through a thin barrier [28,118-120]. The non-volatility of the spin state makes the FTJ device attractive for memory applications. FTJ devices are two-terminal memory devices that also have an invert or buffer capability. Adapted from early designs by Zhuravlev et al. [118] an example of the basic FTJ device structure is shown in Figure 5.7. By integrating the FTJ into the backend or interconnect processing of silicon CMOS, it should be possible to create a low voltage non-volatile memory. The device is expected to operate normally up to 400 K.

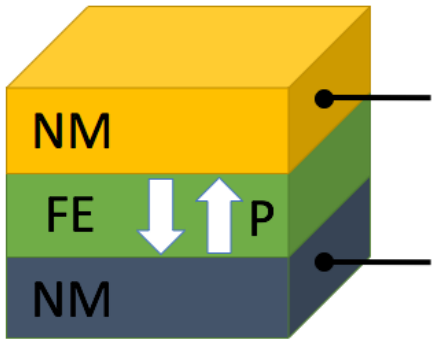


Figure 5.7: The basic FTJ device structure.

5.3.6 Ferroelectric Field Effect Transistor (FE-FET) Cell

The FE-FET device, on the other hand, uses programmable electric polarization at a tunnel barrier device [121,122]. Here, a ferroelectric polarization induced metal-insulator transition in a correlated oxide (CO) material controls a current in a channel, providing a three-terminal non-volatile gate. The basic FE-FET device structure is shown in Figure 5.8.

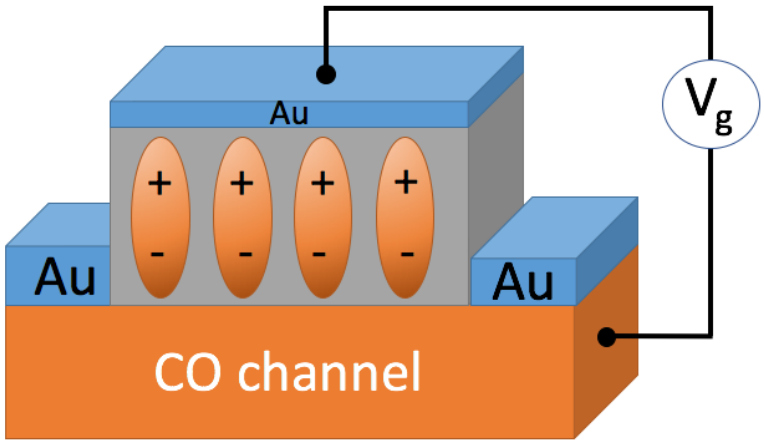


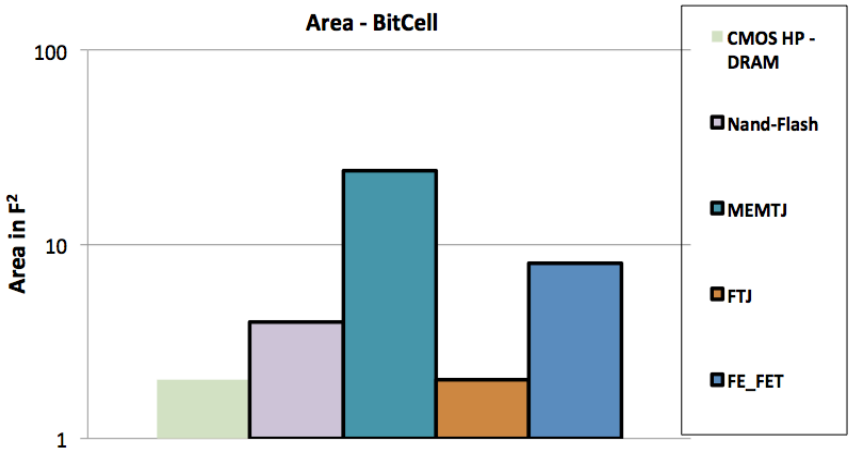
Figure 5.8: The basic FE-FET device structure.

The FE-FET uses voltage controlled switching, but unlike the ME-MTJ though, it has a higher I_{on}/I_{off} ratio (probably between about 200x and 10000x). The device still has not demonstrated to as high stacking possibilities as a conventional NAND flash. It is potentially a useful memory type as it can be integrated onto conventional silicon CMOS, without significant additional CMOS area requirements, so the basic cell size at 6.5 F^2 makes it of the same order of size as the flash cell, but can be placed over the top of CMOS logic, for a stacked CMOS/memory (though this may be slightly larger if the 'source' and 'drain' regions have to be isolated from each

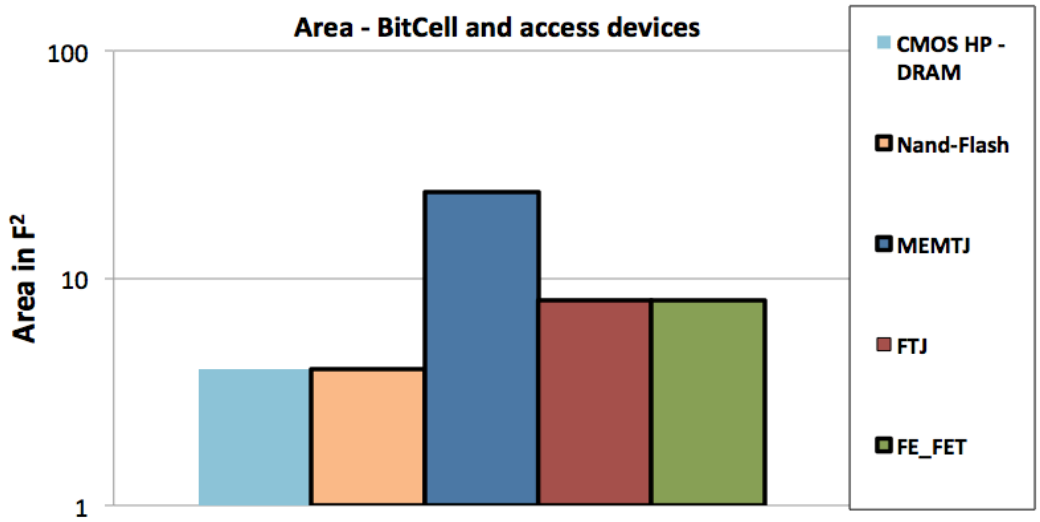
other). Regarding the effect of temperature on device operation, it is expected to operate normally up to 400 K.

5.3.7 Performance Comparison Results

We have analyzed several of the NanoFerroic devices, i.e., ME-MTJ, FTJ and the FE-FET device and compared their performance, as unit cells for memory applications, with conventional DRAM and flash memory, including for write energy, memory area and quiescent leakage. Figure 5.9(a) shows the bitcell area benchmarking for these devices. The ferroelectric tunnel junction is competitive in this comparison. After the basic bitcell has been defined, the access devices are added. The access devices are determined based on the most performance-efficient method to access and program the bitcell. Figure 5.9(b) illustrates the range of 'bitcell and access device' areas from the memory cells studied. As with the bitcell graph, the cells with the bold edging are non-volatile.



(a)



(b)

Figure 5.9: (a) Area of the bitcell only and (b) area of the bitcell and access devices in F^2. The bold-edged cells are non-volatile. © 2015 IEEE

Energy vs. delay time for the write operation of the bitcell plus access device is shown in Figure 5.10. The charge-based devices tend to fall in the lower left (desirable) corner of the graph while the spin based devices group at a relatively higher energy and delay, though, write time is also dependent upon the time it takes to write the stable state into the bit cell, thus causing deviation from a linear correlation for some devices.

Figure 5.11(a) compares the bitcells configured into a larger (1024 x 1024) array. The energy-time graphs for the write includes proportional interconnect capacitance. This comparison suggests that the energy and delay terms of the ferroelectric tunnel junction is large compared to NAND flash and CMOS.

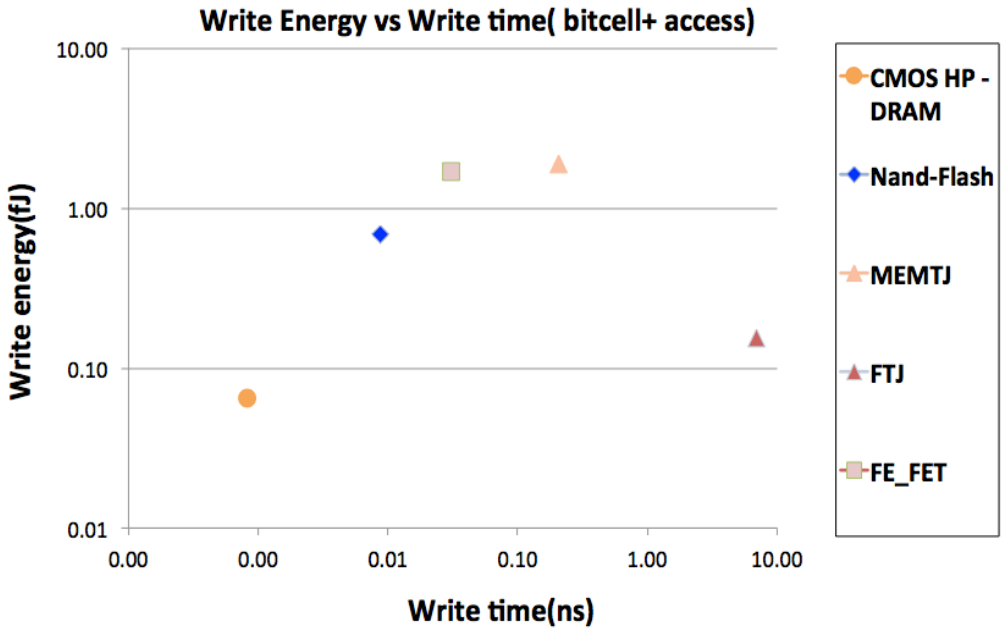
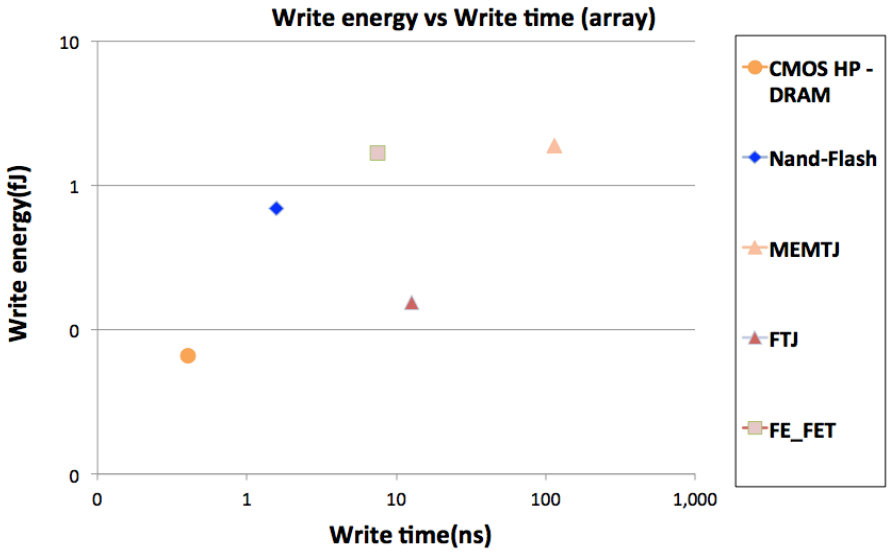


Figure 5.10: Write energy versus write time for the bitcell plus access transistors. © 2015 IEEE

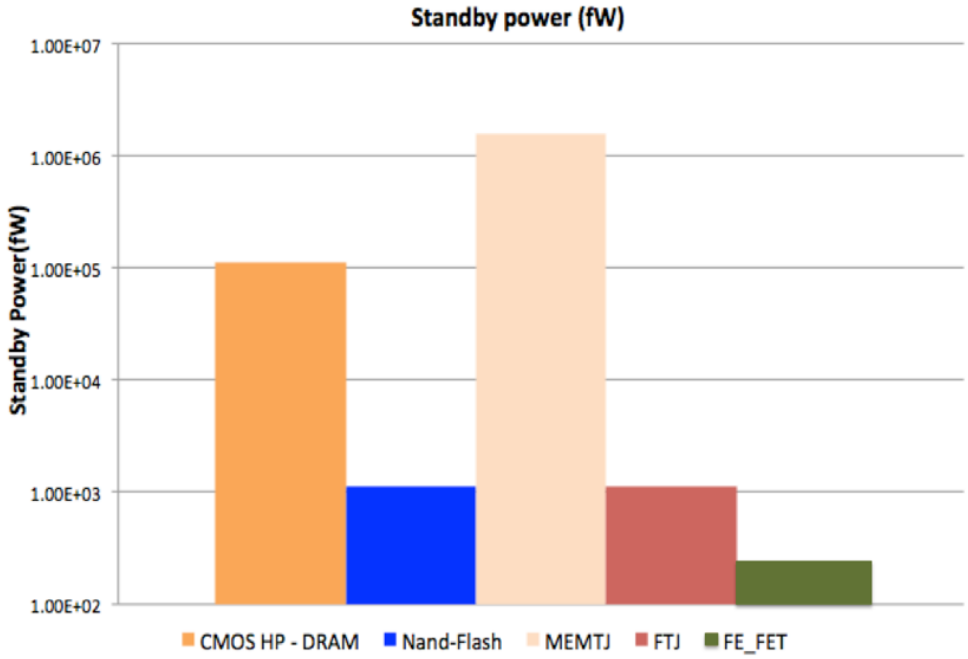
Figure 5.11(b) shows standby power in fW per bit. Some technologies do not require a sustained voltage to maintain the memory state, and such devices may have a lower standby power, but here, for clarity, all bit cells are limited at 200 fW minimum. The ferroelectric tunnel junction is again competitive in this comparison.

5.3.8 Summary

The magneto-electric and ferroelectric family of memory devices described are competitive to conventional CMOS in terms of area and quiescent (or standby) power, but are expected to have longer write times, and possibly longer write energies, making them very suitable for infrequent write and non-volatile applications.



(a)



(b)

Figure 5.11: (a) Write energy versus write time for the bitcells with access devices in a larger array (1024*1024) configuration. (b) Standby power for the bitcells with access devices. © 2015 IEEE

CHAPTER 6

OTHER RESEARCH WORK

A variety of charge-based logic devices are being investigated as possible technologies options for the beyond-CMOS era. The tunneling devices such as the Bilayer Pseudo-Spin Field-Effect transistor (BiSFET), the Bilayer Pseudo-Spin Junction Transistor (BiSJT) and the Interlayer Tunnel Field-Effect Transistor (ITFET) have previously been studied for their logic capabilities. These have an intrinsic memory capability, making them an interesting candidate for standalone memory applications. The performance of these devices with respect to CMOS for memory applications is presented.

6.1 South West Academy of Nanoelectronics (SWAN) Memory Benchmarking

Here we use the same basic methodology described in [7], and updated in [9], and explore devices exhibiting negative differential resistance (NDR) [123-129] using the same physical models developed therein. We consider the performance of a BiSFET, BiSJT and ITFET as standalone memory devices, and compare those to conventional CMOS memory cells. Models for switching mechanisms use MATLAB [130] decks, and are aligned with those in [9] to obtain the switching delay and energy for the intrinsic elements (transistors or nanomagnets).

6.1.1 Memory Cells for Comparison

Memory can be split into the basic cell, the selector which allows write and read, and the array, where much of the cell read and write delay occurs. At the edges of the array, additional circuitry for read and write is needed. The read is generally analog in nature, and here it is assumed

the read circuit is available that is compatible with the array. Parameters such as delay times, cell area, write voltage, write energy per bit, read energy per bit and fabrication techniques have been analyzed for CMOS SRAM, BiSFET, BiSJT and ITFET devices. Write energy per bit is defined as the total energy required to switch the state of the cell. It includes the energy to charge the device and the leakage energy associated with it. Read energy per bit is defined as the total energy required to read the state of the cell.

6.1.2 Static Random-Access Memory (SRAM) Cell

SRAM high-performance (HP) and low-power (LP) are the baseline reference cells, as found in typical standalone memory arrays. Like the memory elements considered here, SRAM cell can retain its stored information as long as the power is supplied. This behavior is in contrast to non-volatile memory where no power needs to be supplied for data retention, as, for example, in flash memory. The write voltages for the SRAM HP and LP device is 0.73 V and 0.3 V respectively. Write energy per bit is defined as the total energy required to switch the state of the SRAM cell. It includes the energy to charge the cell and the leakage energy associated with it. Read energy per bit is defined as the total energy required to read the state of the memory cell.

6.1.3 Bilayer Pseudo-Spin Memory

The Bilayer Pseudo-spin Memory is designed using the BiSFET devices. The BiSFET is based on the electrical properties of two layers of semiconductor in close proximity. The physics of this system can be addressed by treating one of the layers (top or bottom) as having degrees of freedom much as a PseudoSpin, like the spin (up or down) in a Ferromagnet (FM) [123,131]. Figure 6.1 shows the output can be pulled high or low, into one of two stable states [131].

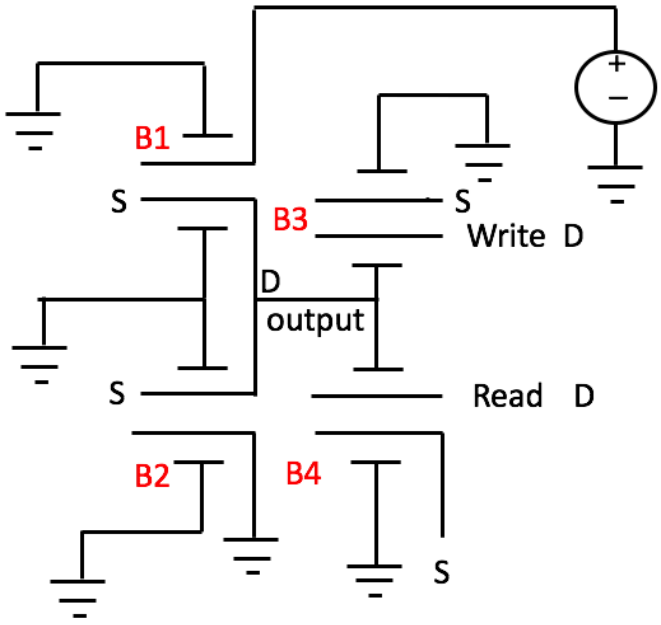


Figure 6.1: BiSFET/BiSDiodes memory cell with BiSFET/MOS pass gate and BiSFET sensing device.

Figure 6.2 shows the I-V characteristics of the BiSFET devices. The operating voltage for this device is very low. Leakage may be high if CMOS access transistors are used, but can be very low if a BiSFET is used. BiSFET can also be used to access the memory cell and is likely to have a lower leakage current. The single ended output shown allows direct interfacing with components at higher voltages whereas, if a BiSJT buffer is used, a supply voltage similar to the diode must be used. The supply voltage is 25 mV to match with [3] and the input is voltage-based. The output is voltage-based but is then made accessible as a current at the read node.

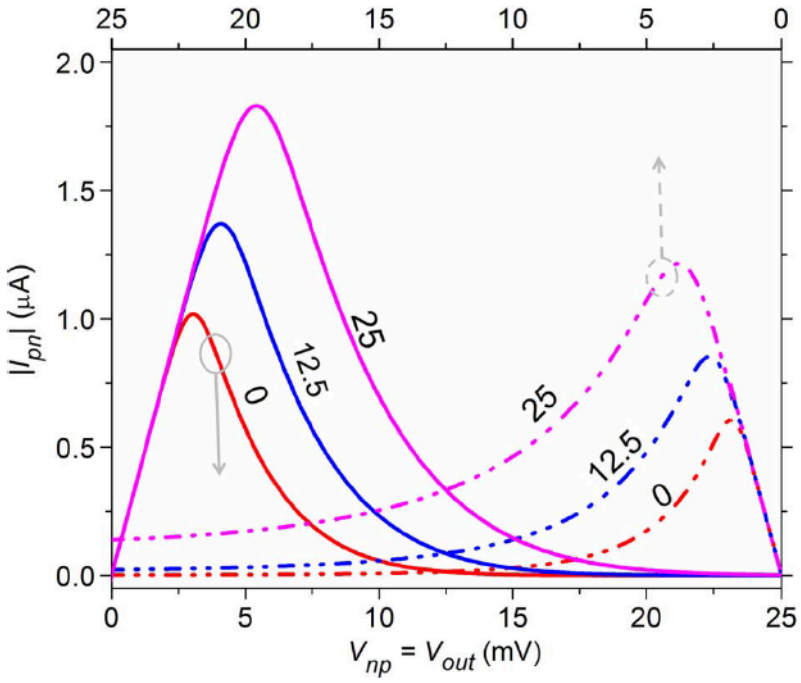
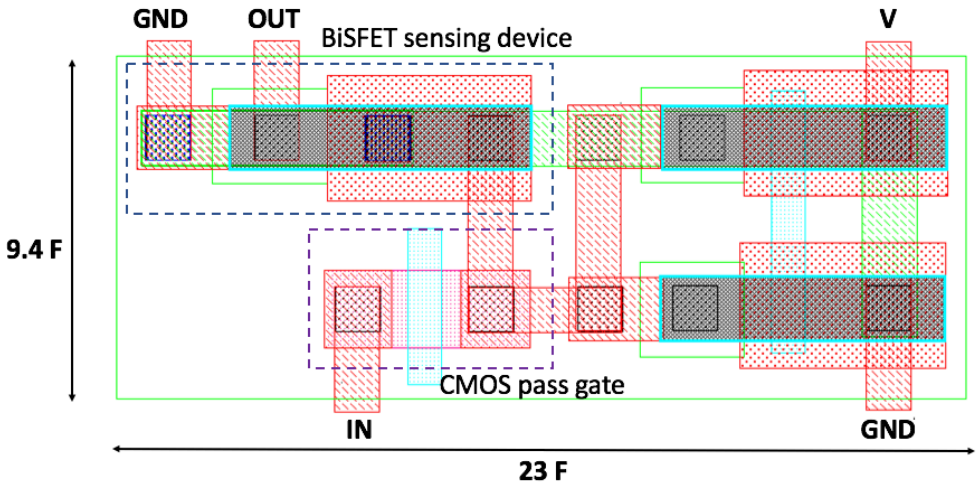


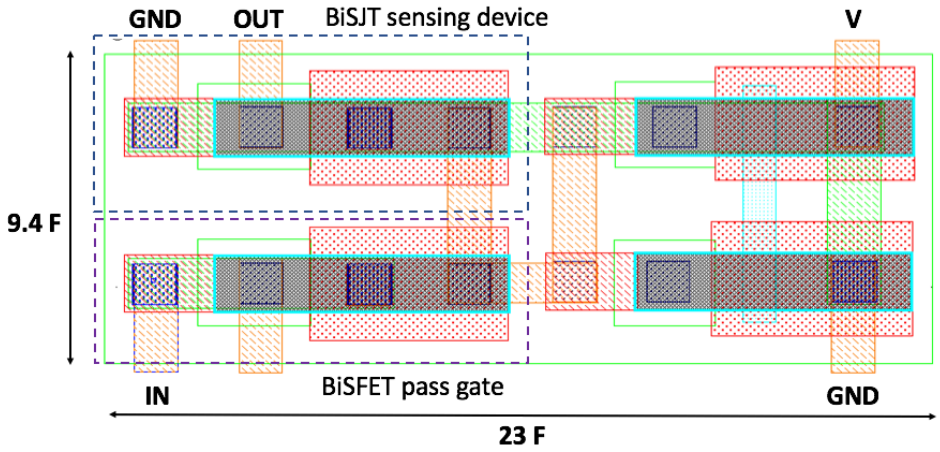
Figure 6.2: I-V characteristics of the BiSFET device, showing an inverter configuration can be stable in two states [131]. © 2010 IEEE

The memory cell is made from a BiSDiode 'inverter', an NMOS pass gate and a BiSJT sensing device [128]. The area of the layout for this configuration is 23x9.4 F^2 or 216 F^2 (Figure 6.3(a)). The alternative version uses a BiSFET pass gate and the area is the same in either version shown in Figure 6.3(b). A memory cell very similar to that of Figure 6.1 has been proposed previously in [123,131], we can save some space on the chip by using BiSDiodes. The original version assumed two pass gates in series, measuring the voltage of the memory cell state. Here, the output is in the form of a current source, which enables direct coupling to a sense circuit that monitors the memory state with current. This is potentially useful if the sense amplifier must be built-in CMOS. In the case of BiSFET and other thermal budget devices, such as those that use

graphene and other 2-D materials, the assumption is these devices can be integrated within the BEOL, or interconnect layers of standard silicon or III-V integrated chip (IC) processes.



(a)



(b)

Figure 6.3: (a) BiSFET layout, showing the two BiSDiode devices and a CMOS or Tunneling Field-Effect Transistor (TFET) pass gate with BiSJT as the sensing device. (b) BiSFET layout, showing the two BiSDiode devices and a BiSFET pass gate with BiSJT as the sensing device.

The write energy per bit in this case is the energy to switch a transmission gate (approximates to half a minimum inverter), plus the energy required to switch a BiSFET inverter. Read energy per bit is the energy to read the state of the BiSFET memory cell through the transmission gate. BiSFET write time is the time it takes to write to the cell, assuming the bitline (BL) and bitline complement (BLB) are preset, is from the time the WL is switched high, following the path through the cell, until the entire cell is stable in its new state. The time for this to occur can be approximated at half a minimum inverter switching plus a BiSFET inverter switching. There is an additional delay if interconnect is included.

6.1.4 Bilayer Pseudo-Spin Junction Transistor (BiSJT)

The BiSJT device is based on the ideal room temperature interlayer electron-hole exciton condensation in bilayer two-dimensional material systems, and could provide switching energies in the order of 10's of zJ, orders of magnitude below end-of-the-roadmap CMOS [128]. Also, the BiSJT is current-controlled and may allow for a simpler device design, smaller device area, and more flexible gate design. The layout of the BiSJT device along with the transport mechanism is shown in Figure 6.4.

Like its voltage controlled sibling, the previously proposed BiSFET [123,124], this current-controlled device concept is spawned by the transport physics of interlayer exciton condensates. (For both devices, 'pseudospin' refers to the two-level 'top' and 'bottom' layer degree of freedom and not to actual spin). However, the BiSJT may allow for simpler devices and circuits.

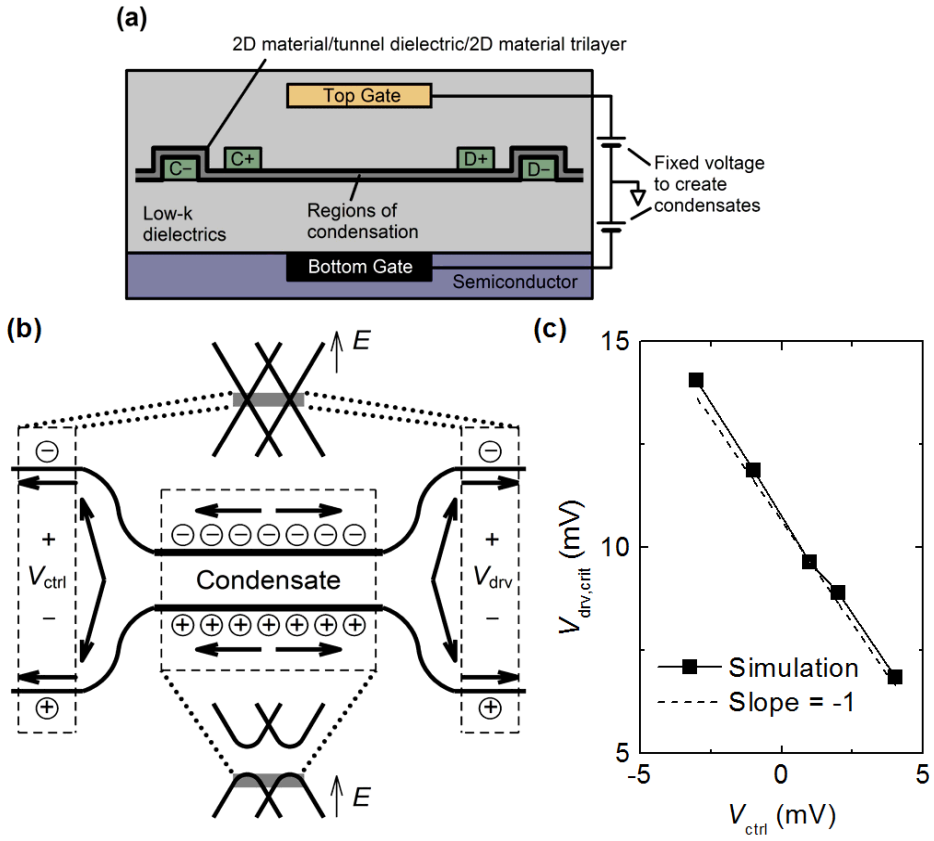


Figure 6.4: Schematic illustration of possible BiSJT layout. (b) Structure for quantum transport simulation, and (c) Obtained 'effective' interlayer critical voltage seen on the 'drive' end versus the interlayer voltage on the 'control' end. Original source [128]. © 2017 IEEE

Input and output are both charge-based - Input voltage is the supply voltage (V_{dd}), here = 25 mV to match with [9]. The cell consists of a BiSJT 'inverter' and two NMOS gates, and will be similar to the layouts for BiSFET (Figure 6.3(a) and 6.3(b)). As with the BiSFET, the assumption is we can integrate with the BEOL, or interconnect layers of standard silicon or III-V IC processes. The circuit schematic for the BiSJT inverter is shown in Figure 6.5.

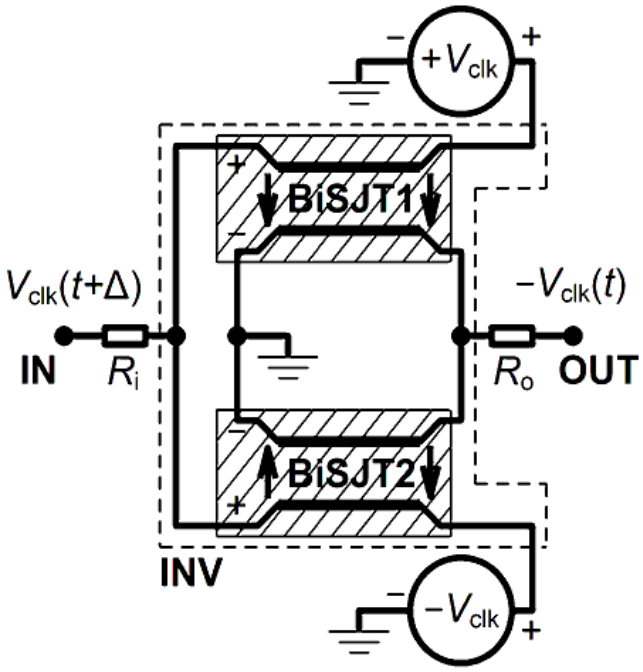
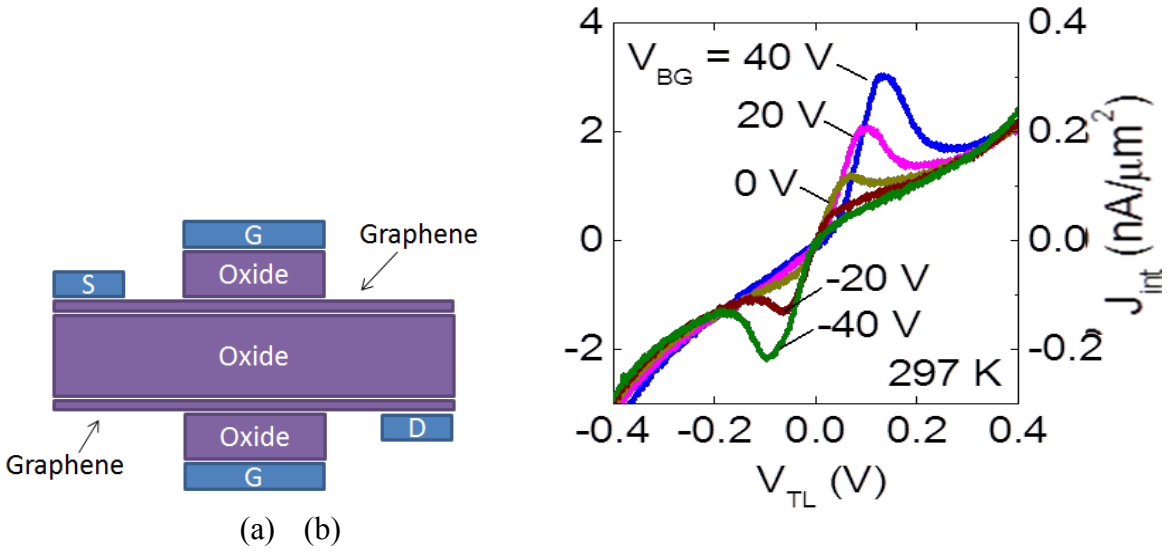


Figure 6.5: Circuit schematic of a BiSJT inverter [128]. © 2017 IEEE

Write energy per bit is defined as the total energy required to switch the state of the cell. This is the energy to switch a transmission gate (approximates to half a minimum inverter), plus the energy required to switch a BiSJT inverter. Read energy per bit is the energy required to read the state of the cell, and is the energy to switch a transmission gate based on using a CMOS transmission gate. BiSJT write time is the time it takes to write to the cell, assuming the BL and BLB are preset, is from the time the WL is switched high, following the path through the cell, until the entire cell is stable in its new state. The time for this to occur can be approximated as half a minimum inverter switching plus a BiSJT inverter switching. There is additional delay if interconnect is included.

6.1.5 Interlayer Tunnel Field-Effect Transistor (ITFET)

The ITFET device is shown in Figure 6.6(a). It is a charge-based device, which relies on resonant tunneling between two graphene layers. As a result, it has a highly non-linear I-V curve (Figure 6.6(b)) [129]. This means a circuit for an ITFET based volatile memory is expected to look similar to the one for BiSFET, shown in Figure 6.1.



(a) (b)

Figure 6.6: (a) Cross-section and (b) I/V characteristic of the Interlayer Tunneling FET [132]. © 2012 IEEE

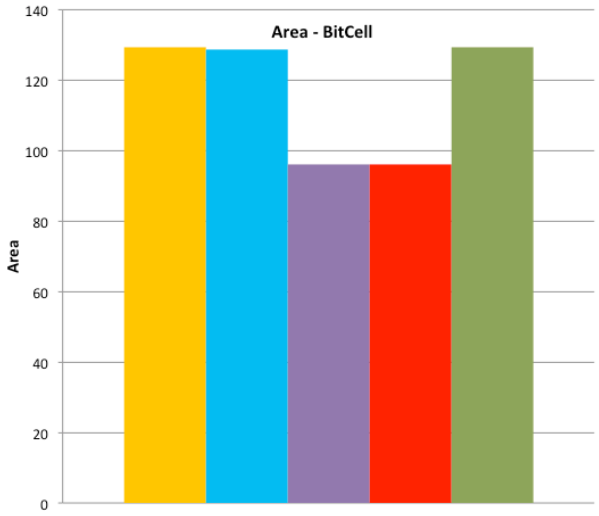
The cell is made from an ITFET 'inverter' and two NMOS gates, and will be similar to the layouts for BiSFET (Figure 6.3(a) and 6.3(b)). It may also be possible with the ITFET to replace one of the devices in the inverter latch with either a resistor or CMOS current source. Input and output are both charge-based - Input voltage is the supply voltage (V_{DD}). Depending on the resonant peak, the memory storage voltage will vary. The read and write voltage used is 75 mV and output voltage will reach V_{DD}.

The write energy per bit is the energy to switch a transmission gate plus the energy required to switch an ITFET inverter. The write time for ITFET is the time it takes to write to the cell, assuming the BL and BLB are preset, and is from the time the WL is switched high, following the path through the cell, until the entire cell is stable in its new state. The time for this to occur can be approximated as half a minimum inverter switching plus an ITFET inverter switching. There is additional delay if interconnect is included. The standby power per bit is through the primary leakage mechanism of the cell from V_{DD}-gnd, which is through the ITFET inverter. This standby power simplifies to the leakage of the 1x inverter cell.

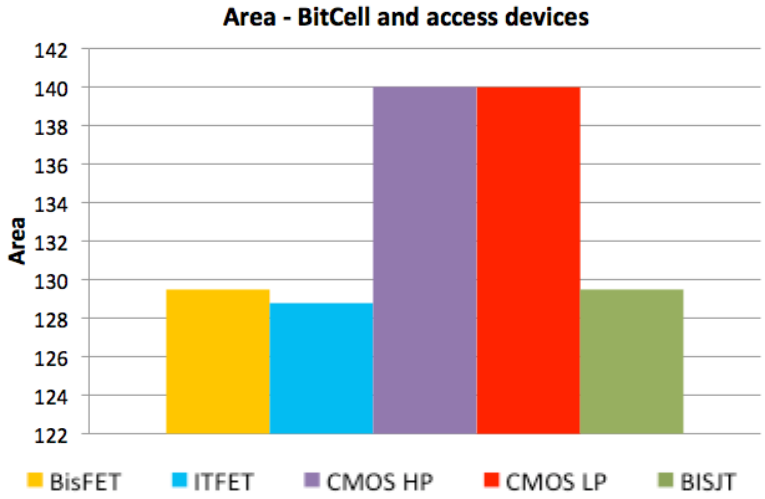
6.2 Performance Comparison Results

Once the performance characteristics, such as read and write time and operational characteristics, are determined to be acceptable, one of the most significant items in the decision for which memory cell to use is the bitcell area. Figure 6.7 illustrates the range of bitcell areas from the memory cells studied.

After the basic bitcell has been defined, the access devices are added. The access devices are determined based on the most performance-efficient method to access and program the bitcell. Figure 6.8 illustrates the range of 'bitcell and access device' areas from the memory cells studied. It can be concluded from Figures 6.7 and 6.8 that for bitcell area without access device, the area numbers for the beyond-CMOS devices are higher than their CMOS counterpart. However, if area for the bitcell and the access devices is considered, beyond-CMOS devices are more competitive.



(a)



(b)

Figure 6.7: (a) Bitcell only area and (b) area of the bitcell and access devices in F^2.

Write energy vs. read energy of the bitcell plus access device is shown in Figure 6.8. The BiSJT and BiSFET are at an extremely low write and read energy. The ITFET energy is 10x that of to the BiSJT and BiSFET in terms of write energy due to differences in the write voltages. The voltage for ITFET is 75mV whereas for BiSFET, it is 25mV. The ITFET and BiSJT based cells have comparable read energy.

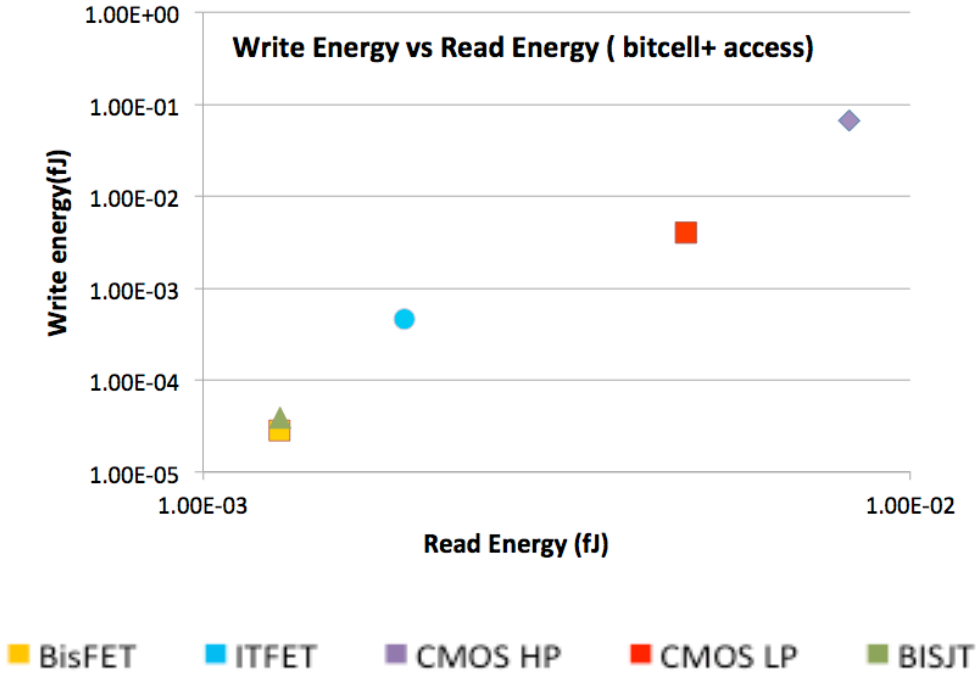


Figure 6.8: Write energy versus read energy for the bitcell plus access transistors.

6.3 Summary

The memory cell performance of the ITFET, BiSFET and the BiSJT devices is compared with conventional SRAM memory, including for read and write energy, memory area and quiescent leakage. The beyond-CMOS devices analyzed here are competitive to conventional CMOS in terms of area and quiescent (standby) power, but are expected to have longer write times with lower write energies in reality, making them suitable for infrequent write, low-power applications.

CHAPTER 7

CONCLUSIONS/FUTURE WORK

This chapter summaries the dissertation, discusses the findings and contributions, points out the limitation of this work and outlines the possible future research directions. In this dissertation, we introduced several ME based devices, presented the models for these in Verilog-A platform and verified the functionality of logic functions obtained from these devices.

7.1 Conclusions

A beneficial feature of the Magneto-electric Magnetic Tunnel Junction (ME-MTJ) and Magneto-electric Field Effect Transistor (MEFET) devices is that they are switched at low voltages, in the range of 0.1 - 0.2 V reducing power consumption and improving operating frequency. These devices may also be configured to achieve minimal quiescent-power requirements due to their inherent non-volatility which also allows integration of the memory functionality. ME devices also show the advantage of CMOS process-compatibility.

The MEFET devices have about 10x better performance than the ME-MTJ due to the 10x improvement in the delay component (Figure 7.1). They also have a better on-off ratio (~10^7) compared to the ME-MTJ devices with ratio of just 10x. On the other hand, the MEFET devices do not have quite the circuit density of ME-MTJ devices.

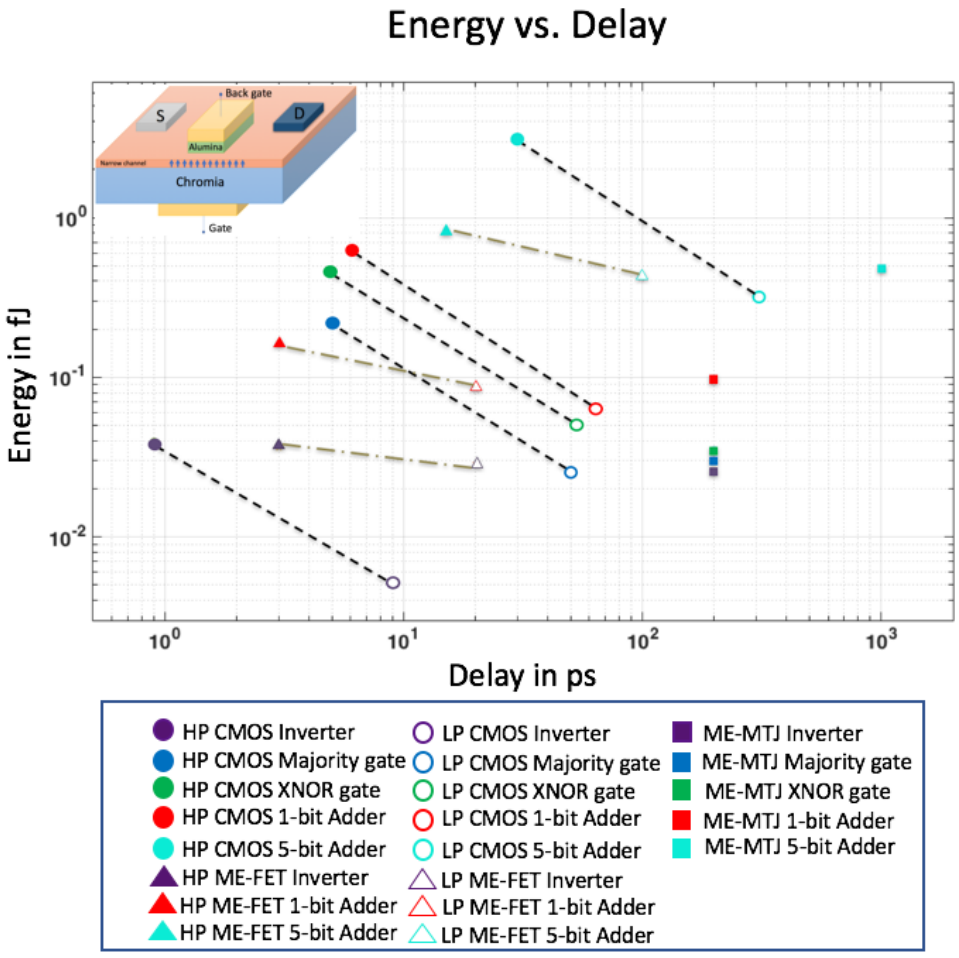


Figure 7.1: Benchmarking of the MEFET and ME-MTJ devices with respect to CMOS equivalents.

7.2 Contribution of this Dissertation

One of the main contributions of this work is the platform it provides to the circuit designers to perform early stage analysis for the ME devices. The contributions of this research are as follows:

- The first compact model of the ME-MTJ device in MATLAB has been developed. Energy and delay terms for the ME-MTJ have been derived from the model and the results are benchmarked with respect to CMOS devices [37].

- The first compact model of the ME-MTJ and its derived devices in Verilog-A has been developed. This model has been used to design and test ME-MTJ based analog and digital circuits for operation. The digital circuits include inverter, buffer, NAND, NOR, XNOR, 1-bit and 5-bit full adder etc. and the analog circuits include comparator, flash and serial analog to digital converter (ADC) [35,38,40-43].

- Novel designs for the ME-MTJ based SRAM cell have been proposed where the ME-MTJ introduces non-volatility in the volatile CMOS memory cell. This reduces the power consumption since the bit is retrieved from the ME-MTJ cell when the circuit is powered up [33].

- To reduce the number of CMOS components required for the ME-MTJ operation, a new device concept, i.e., Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) has been proposed which only requires a unipolar power supply for operation unlike ME-MTJ devices which require bipolar supply [39].

- The Verilog-A model developed for the ME-MTJ devices has been modified to model the UMMTJ based circuits and transient simulations have been performed for the UMMTJ based devices [39,94].

- Compact modeling of the single source and dual source MEFETs and their derived devices in Verilog-A has been developed. The model includes physical models to outline the behavior

the device accurately. This model has been used to design and test MEFET circuits for ex-inverter, NAND, majority gate and full adder [43].

- The benchmarking results obtained from the simulations for the ME-MTJ and the MEFET circuits have been compared with the CMOS equivalents.
- The benchmarking results have been incorporated in the Semiconductor Research Corporation (SRC) - Center for NanoFerroic Devices (CNFD) reports.
- Benchmarking for other beyond-CMOS devices has been performed with respect to CMOS memory devices to broaden the spectrum of analysis [36].

7.3 Discussion

7.3.1 Limitations of the ME-MTJ Device

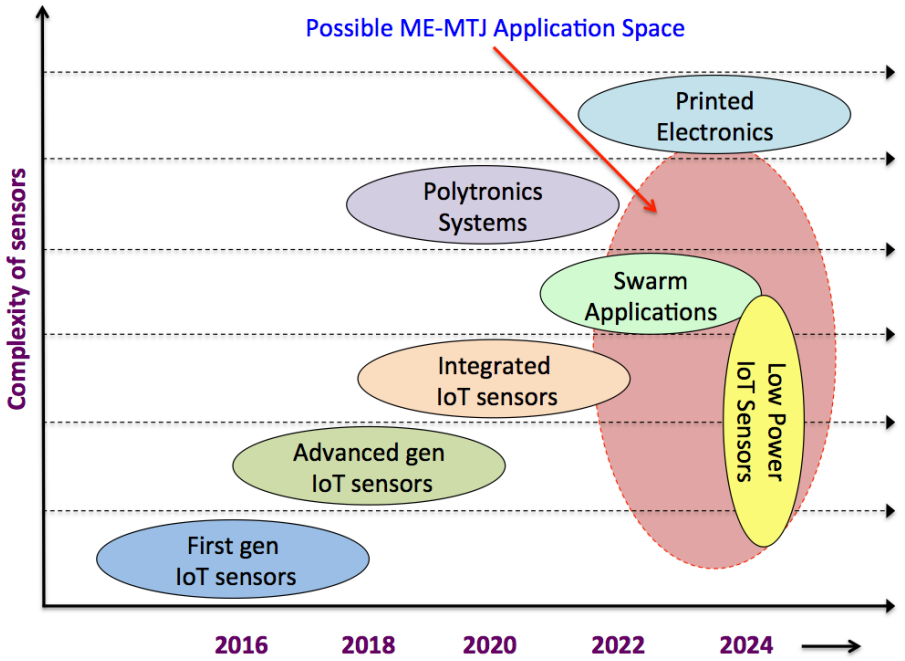
As noted already, the delay of the ME devices is essentially set by the slow process of magnetization transfer, in which the boundary magnetism of the ME reverses the bulk magnetization of the free FM.

7.3.2 Limitations of the MEFET Device

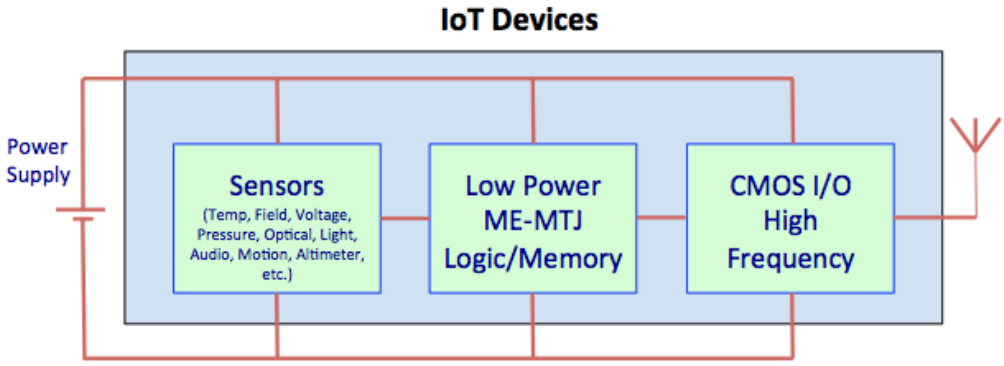
The model for the MEFET device has been presented to simulate the logic functions derived from this device. One of the major limitation of this work is that the theoretical models for the spin injection are not included. The assumption was made that the current injected into the system is capable of switching the magnetization of the FM assuming spin transfer torque effect and the spin injection efficiency is 100%.

7.4 Suggestions for Future Direction

- Once the ME-MTJ device is available, the comparison of the simulation results with the experimental results could be the primary task at hand. This would increase the confidence in the developed Verilog-A models.
- The ME-MTJ device uses a combination of magnetic and electric fields to enable switching of the magneto-electric chromia layer. Recently, our team has found a way to switch this layer just by applying electric field. The models can be upgraded to include this feature [133].
- The enhanced version of the ME-MTJ, i.e., the UMMTJ device can be used for designing analog circuits just like the ME-MTJ device but with enhanced performance. It can also be used to introduce non-volatility in the CMOS SRAM cell. These circuits can be simulated in the Cadence environment.
- The MEFET device can be made unipolar by introducing a floating gate or an ionic conductor as in the UMMTJ device. This unipolar magneto-electric FET can be modeled in Verilog-A and simulated in Cadence.
- The MEFET devices can be tuned for various analog and memory applications. These circuits can be modeled, designed and simulated in Cadence similar to the ME-MTJ device.
- The ME-MTJ device can be used as a sensor in the area of the Internet of Things (IoT). There is an evolving market segment where alternate technologies are becoming viable (Figure 7.2).



(a)



(b)

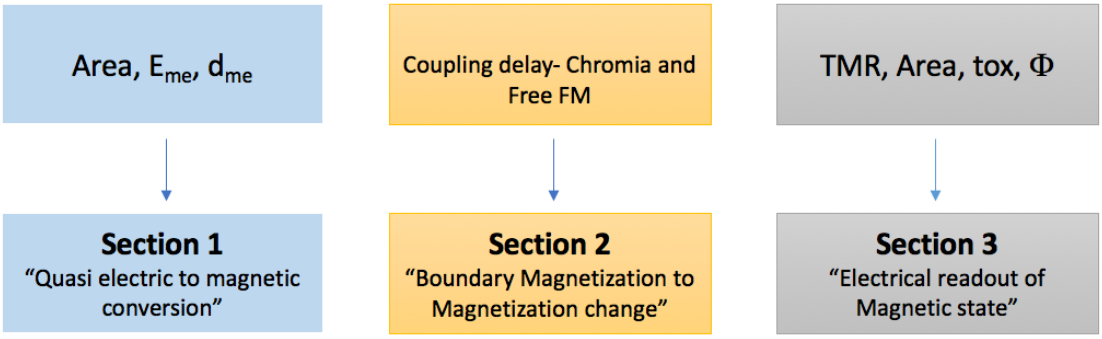
Figure 7.2: (a) Types of sensors based on emerging technologies for Internet of things (IoT). (b) One of the possible applications of the ME-MTJ device in IoT applications.

- The ME-MTJ device can be used directly for magnetic sensing applications. Since the ME-MTJ works on the principle of exchange biasing, the switching depends on the product of electric and magnetic field. With a fixed voltage input, once the magnetic field exceeds the nominal value, the output of the ME-MTJ device goes high or low depending on the

polarity of input applied. Thus, ME-MTJ can be used as a magnetic switch in applications where magnetic field detection is necessary for operation. This might include magnetic sensors in security as motion sensitivity applications.

APPENDIX

The code below describes the Verilog-A modeling of the ME-MTJ inverter, the ME-MTJ majority gate and the ME-MTJ based XNOR gate.



ME-MTJ Inverter

Section-1

```
// Verilog-A for MEMTJ_inverter, Verilog-A, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall
`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/
module MEMTJ_inverter_section1(G,S,Spin_FM1);
// Fixed source terminal
inout S;
electrical S;
// Input gate terminal
inout G;
electrical G;
// Terminal for the spin orientation in FM layer
inout Spin_FM1;
electrical Spin_FM1;

/*************************************************************
Parameter Declaration
*************************************************************/
```

```
/*----------Threshold of Chromia state inversion in volts----------*/
parameter real Vtmax= 0.055 from [0:inf] ;
/*----------Area of input capacitor----------*/
parameter real A= 900e-18 from [0:inf] ;
/*----------Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------Width of Chromia layer in meter----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Dielectric constant of Chromia ----------*/
parameter real k=12;
/*----------Input resistance----------*/
parameter real R=1100;

real Vgs; // Input gate voltage
real Tau1; // Switching time for chromia
real vm; // Voltage node defined to represent the memory
real C1; // Input capacitance

/*************************************************************
Body definition
*************************************************************/
analog
begin @(initial_step)
  begin
  C1=(k*E0*A)/w;
  end

I(G,S) <+ C1* ddt(V(G,S)); // Current in section 1
Vgs=V(G,S); // applied gate voltage

if (V(G,S) >= Vtmax)
  vm=1; // chromia spin are oriented up.
else if (V(G,S) <= -Vtmax)
                                                    vm=-1; // chromia spin are oriented down.
else if (V(G,S)> -Vtmax && V(G,S) < Vtmax) // chromia spin switching condition not met
  begin
  if (vm == -1)
  begin
  vm=-1;
  end
  else if (vm==1)
  begin
  vm=1;
  end
  else vm =5;
  end
else vm = 5;

// memory state variable is assignment
V(Spin_FM1) <+ transition(vm,0,0,0);
// Chromia switches instantaneously

end
```

```
endmodule
```

Section-2

```
// Verilog-A for MEMTJ_inverter, Verilog-As
// Authors: Nishtha Sharma, Andrew Marshall

`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/

module MEMTJ_inverter_section2(Spin_FM1, Spin_FM2);
// Spin state in chromia
inout Spin_FM1;
electrical Spin_FM1;

// Spin state in free FM layer
inout Spin_FM2;
electrical Spin_FM2;

/*************************************************************
Body definition
*************************************************************/
analog
begin
  @(initial_step)
  begin
  end

// Switching delay of 200ps between chromia and free FM layer
V(Spin_FM2) <+transition(V(Spin_FM1),200p,0,0);
end
endmodule
```

Section-3

```
// Verilog-A for MEMTJ_inverter, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE
```

```
/************************************************************
Module definition
/************************************************************/
module MEMTJ_inverter_section3(D,Spin_FM2,S);

// Output drain terminal
inout D;
electrical D;
// Fixed source terminal
inout S;
electrical S;
// Spin state of free FM layer
inout Spin_FM2;
electrical Spin_FM2;

/************************************************************
Parameter Declaration
/************************************************************/

/*----------Threshold of chromia state inversion in volts----------*/
parameter real Vtmax= 0.05 from [0:inf];
/*----------Area of input capacitor in m2----------*/
parameter real A= 900e-18 from [0:inf];
/*----------Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------Width of chromia layer in m----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Average barrier potential height of MgO in electron-volt----------*/
parameter real Phi=0.4 from [0:inf];
/*----------Dielectric constant of chromia----------*/
parameter real k=12 from[0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real RA=10 from [5:15];
/*----------TMR(0) with zero Volt bias voltage; value expected to 1000%----------*/
parameter real TMR=10 from [0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real FA=332.5 from [0:inf];
/*----------Switching delay in section 2----------*/
parameter real Tau2= 200E-12;
/*----------Oxide barrier thickness in meter----------*/
parameter real tox=2e-9 from [1e-9:4e-9];
/*----------Voltage for calculating real TMR in volts ----------*/
parameter real Vh=0.11 from [0:inf];
/*----------Bias voltage in volts----------*/
parameter real Vb=0.11 from [0:inf];

real Rap; // Anti-parallel resistance
real Rp; // Parallel resistance
real id; // Current at the output node
real vout; // Voltage across the output
real TMRR; // Real tunneling Magnetoresistance
real vmem; // Variable for representing the memory state
```

```
/*************************************************************
Body definition
*************************************************************/

analog
  begin
  @(initial_step)

begin
  TMRR=TMR/(1+Vb*Vb/(Vh*Vh));                          // MTJ resistance using brinkman model
  Rp = (tox*exp(1.025*tox*sqrt(Phi)))/(FA*sqrt(Phi)*A); // Parallel resistance
  Rap= Rp*(1+TMR) ; // Anti-parallel resistance
end

id=I(D,S); // Current across the output(drain-source)
if (V(Spin_FM2) ==1 )
  begin
  vout=id*Rp;
  vmem=0;
  end
else if (V(Spin_FM2) ==-1 )
  begin
  vout=id*Rap;
  vmem=1;
  end
else begin if (vmem==0)
  begin
  vmem=0;
  vout=id*Rp;
  end
else if (vmem==1)
  begin
  vmem=1;
  vout=id*Rap;
  end
else vout=0;
end

// Voltage at the drain terminal**************************
V(D,S)<+ vout;

end
endmodule
```

ME-MTJ Majority gate

Section-1

```
// Verilog-A for MEMTJ_Majority_gate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall
```

```
/*************************************************************
Module definition
*************************************************************/
`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

module MEMTJ_Majoritygate_section1(G1,G2,G3,S,Spin_FM1);

// Fixed source terminal
inout S;
electrical S;
// Input gate terminal
inout G1,G2,G3;
electrical G1,G2,G3;
// Terminal for the spin orientation in FM layer
inout Spin_FM1;
electrical Spin_FM1;

/*************************************************************
Parameter Declaration
*************************************************************/

/*----------Threshold of Chromia state inversion in volts----------*/
parameter real Vtmax= 0.055 from [0:inf] ;
/*----------Area of input capacitor----------*/
parameter real A= 900e-18 from [0:inf] ;
/*----------Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------Width of Chromia layer in meter----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Dielectric constant of Chromia ----------*/
parameter real k=12;
/*----------Input resistance----------*/
parameter real R=1100;

real Vgs1; // Input gate G1 voltage
real Vgs2; // Input gate G2 voltage
real Vgs3; // Input gate G3 voltage
real Tau1; // Switching time for chromia
real vm; // Voltage node defined to represent the memory
real C1; // Input capacitance

/*************************************************************
Body definition
*************************************************************/
analog
  begin
```

```
  @(initial_step)
  begin
C1=(k*E0*A)/w;
end

Vgs1=V(G1,S); // Voltage at G1
Vgs2=V(G2,S); // Voltage at G2
Vgs3=V(G3,S); // Voltage at G3

I(G1,S) <+ (C1/3)* ddt(V(G1,S)); // Current through gate 1
I(G2,S) <+ (C1/3)* ddt(V(G2,S)); // Current through gate 2
I(G3,S) <+ (C1/3)* ddt(V(G3,S)); // Current through gate 3

if (((Vgs1+Vgs2+Vgs3)/3) >= Vtmax) // Majority gate works on averaging
  vm=1; // Chromia spin vectors are oriented up

if (((Vgs1+Vgs2+Vgs3)/3) <= -Vtmax)
  vm=-1; // Chromia spin vectors are oriented down
else
  begin // chromia spin switching condition not met
  if (vm ==-1)
  begin
  vm=-1;
  end
  else if (vm==1)
  begin
  vm=1;
  end
  else vm =5;
  end

// memory state variable is assignment .
V(Spin_FM1)<+ transition(vm,0,0,0);
// Chromia switches instantaneously

end
endmodule
```

Section-2

```
// Verilog-A for MEMTJ_inverter, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall
`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/

module MEMTJ_Majoritygate_section2(Spin_FM1,Spin_FM2 );
inout Spin_FM1,Spin_FM2;
electrical Spin_FM1,Spin_FM2;
```

```
/*************************************************************
Body definition
*************************************************************/
 analog
  begin
  @(initial_step)
  begin
  end
// Switching delay of 200ps between chromia and free FM layer
V(Spin_FM2)<+transition(V(Spin_FM1),200p,0,0);

end
endmodule
```

Section-3

```
// Verilog-A for MEMTJ_Majoritygate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/
module MEMTJ_Majoritygate_section3(D,Spin_FM2,S);

// Output drain terminal
inout D;
electrical D;
// Fixed source terminal
inout S;
electrical S;
// Spin state of free FM layer
inout Spin_FM2;
electrical Spin_FM2;

/*************************************************************
Parameter Declaration
*************************************************************/

/*----------Threshold of chromia state inversion in volts----------*/
parameter real Vtmax= 0.055 from [0:inf] ;
/*----------Area of input capacitor in m2----------*/
parameter real A= 900e-18 from [0:inf] ;
/*----------Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
```

```
/*----------Width of chromia layer in m----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Average barrier potential height of MgO in electron-volt----------*/
parameter real Phi=0.4 from [0:inf];
/*----------Dielectric constant of chromia----------*/
parameter real k=12 from[0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real RA=10 from [5:15];
/*----------TMR(0) with zero Volt bias voltage; value expected to 1000%----------*/
parameter real TMR=10 from [0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real FA=332.5 from [0:inf];
/*----------Switching delay in section 2----------*/
parameter real Tau2= 200E-12;
/*----------Oxide barrier thickness in meter----------*/
parameter real tox=2e-9 from [1e-9:4e-9];
/*----------Voltage for calculating real TMR in volts ----------*/
parameter real Vh=0.11 from [0:inf];
/*----------Bias voltage in volts----------*/
parameter real Vb=0.11 from [0:inf];

real Rap ; // Anti-parallel resistance
real Rp; // Parallel resistance
real id; // Current across the output
real vout; // Voltage across the output
real TMRR; // Real tunneling Magnetoresistance
real vmem; // Variable for representing the memory state

/*************************************************************
Body definition
*************************************************************/

            analog
            begin
              @(initial_step)
            begin
  TMRR=TMR/(1+Vb*Vb/(Vh*Vh));                    // MTJ resistance calculation using brinkman model
  Rp = (tox*exp(1.025*tox*sqrt(Phi)))/(FA*sqrt(Phi)*A); // Parallel resistance
               Rap= Rp*(1+TMR) ; // Anti-parallel resistance
            end
id=I(D,S); // Current across the output(drain-source)
if (V(Spin_FM2) ==1 )
  begin
  vout=id*Rp;
               vmem=0;
            end
else if (V(Spin_FM2) ==-1 )
  begin
  vout=id*Rap;
  vmem=1;
  end
else begin
  if (vmem==0)
```

```
 begin
 vmem=0;
 vout=id*Rp;
 end
 else if(vmem==1)
 begin
 vmem=1;
 vout=id*Rap;
 end
 else vout=0;
 end

// Voltage at the drain terminal**********************
V(D,S)<+ vout;

end
endmodule
```

ME-MTJ XNOR gate:

Section-0

```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/
module MEMTJ_XNOR_section0(G1,S1,G1S1);
// Input terminals
inout G1,S1;
electrical G1,S1;

// Difference terminal
inout G1S1;
electrical G1S1;

/*************************************************************
Parameter Declaration
*************************************************************/
/*----------Threshold of Chromia state inversion in volts----------*/
parameter real Vtmax= 0.050 from [0:inf] ;
/*----------Area of input capacitor----------*/
parameter real A= 900e-18 from [0:inf] ;
/*---------- Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------width of Chromia layer in meter----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Dielectric constant of Chromia ----------*/
```

```
parameter real k=12;

real vg1;
real vs1;

/*************************************************************
Body definition
*************************************************************/
analog
  begin
  @(initial_step)
  begin
end

vg1= V(G1); // input gate voltage
vs1= V(S1); // fixed source voltage

V(G1S1)<+transition(vg1-vs1); // Difference signal

end
endmodule
```

Section-1

```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/

module MEMTJ_XNOR_section1(G1S1,Spin_FM1);

// Difference of inputs terminals
inout G1S1;
electrical G1S1;

// Terminal for the spin orientation in FM layer
inout Spin_FM1;
electrical Spin_FM1;

/*************************************************************
Parameter Declaration
*************************************************************/
```

```
/*----------Threshold of Chromia state inversion in volts----------*/
parameter real Vtmax= 0.055 from [0:inf] ;
/*----------Area of input capacitor----------*/
parameter real A= 900e-18 from [0:inf] ;
/*---------- Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------width of Chromia layer in meter----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Dielectric constant of Chromia ----------*/
parameter real k=12;

real Vgs; // Input gate voltage
real Tau1; // Switching time for chromia
real vm; // Voltage node defined to represent the memory
real C1; // Input capacitance

/*************************************************************
Body definition
*************************************************************/
analog
begin
  @(initial_step)
  begin
  vm=-1;
  C1=(k*E0*A)/w;
  end
vgs=V(G1S1); // difference voltage from section0

if (V(G1S1) >= Vtmax)
  vm=1; // chromia spin are oriented up.
else if (V(G1S1)<= -Vtmax)
  vm=-1; // chromia spin are oriented down.
else
  begin // chromia spin switching condition not met
  if (vm == -1)
  begin
                                  vm=-1;
                                end
  else if (vm==1)
  begin
  vm=1;
  end
  else vm =5;
  end

// memory state variable is assignment
V(Spin_FM1)<+ transition(vm,10p,0,0);
// Chromia switches after a delay of 10 picoseconds

end
endmodule
```

Section-2

```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`include "constants.vams"
`include "disciplines.vams"
/*************************************************************
Module definition
*************************************************************/
module MEMTJ_XNOR_section2(Spin1,Spin_FM1);

// Spin state in chromia
inout Spin_FM1;
electrical Spin_FM1;

// Spin state in top free FM layer
inout Spin1;
electrical Spin1;

/*************************************************************
Body definition
*************************************************************/
 analog
  begin
  @(initial_step)
  begin
  end
// Switching delay of 190ps between chromia and top free FM layer
V(Spin1)<+transition(V(Spin_FM1),190p,0,0);

end
endmodule
```

Section-3

```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/
module MEMTJ_XNOR_section3(S1,Spin1,Spin2,S2);
```

```
// output terminal
inout S1;
electrical S1;

// fixed source terminal
inout S2;
electrical S2;

/*************************************************************
Parameter Declaration
*************************************************************/

/*----------Threshold of Chromia state inversion in volts----------*/
parameter real Vtmax= 0.055 from [0:inf] ;
/*----------Area of input capacitor----------*/
parameter real A= 900e-18 from [0:inf] ;
/*---------- Coulomb constant, C^2/(m*J)----------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------width of Chromia layer in meter----------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------The average barrier potential height of MgO in electron-volt----------*/
parameter real Phi=0.4 from [0:inf];
/*----------Dielectric constant of chromia----------*/
parameter real k=12 from[0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real RA=10 from [5:15];
/*----------TMR(0) with Zero Volt Bias Voltage ; value expected to 1000%----------*/
parameter real TMR=10 from [0:inf];
/*----------Resistance-area product in ohmum2----------*/
parameter real FA=332.5 from [0:inf];
/*----------switching delay in section 2----------*/
parameter real Tau2= 200E-12;
/*----------Oxide barrier thickness in meter----------*/
parameter real tox=2e-9 from [1e-9:4e-9];
parameter real Vh=0.11 from [0:inf];
parameter real Vb=0.11 from [0:inf];
/*-----------------------------------------
Variables
-----------------------------------------*/

real Rap ; // Anti-parallel resistance
real Rp; // Parallel resistance
real id; // Current across the output. This is provided by a pull-up device
real vout; // Voltage across the output
real TMRR; // Real tunneling Magnetoresistance
real vm; // Variable for representing the memory state in top chromia
real vp; // Variable for representing the memory state in bottom chromia
real vmem; // output memory state

/*************************************************************
Body definition
*************************************************************/
```

```
  analog
  begin
  @(initial_step)
  begin
  TMRR=TMR/(1+Vb*Vb/(Vh*Vh));                                    //MTJ resistance using brinkman model
  Rp = (tox*exp(1.025*tox*sqrt(Phi)))/(FA*sqrt(Phi)*A); //Parallel resistance
  Rap= Rp*(1+TMRR); //Anti-parallel resistance
  vmem=1;
  spin_fixedFM=1;
  end

id=I(S1,S2); // Current across the output(drain-source).
vm=V(Spin1);
vp=V(Spin2);

if (vm == -1 && vp== -1 )
  begin
  vout=id*Rp;
  vmem=0;
  end

else if (vm == -1 && vp == 1 )
  begin
  vout=id*Rap;
  vmem=1;
  end

else if (vm == 1 && vp== -1 )
  begin
  vout=id*Rap;
  vmem=1;
  end

else if (vm == 1 && vp== 1 )
  begin
  vout=id*Rp;
  vmem=0;
  end
else
  begin
  if (vmem==0) // switching condition not met
  begin
  vout=id*Rp;
  vmem=0;
            else if (vmem==1)
              begin
  vout=id*Rap;
  vmem=1;
  end
  else vmem=5;
  end
```

```
// Voltage at the drain terminal************************

V(S1,S2)<+ vout;

end
endmodule
```

Section-4

```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/
module MEMTJ_XNOR_section4(Spin2,Spin_FM2);

// Spin state in chromia
inout Spin_FM2;
electrical Spin_FM2;

// Spin state in bottom free FM layer
inout Spin2;
electrical Spin2;

/*************************************************************
Body definition
*************************************************************/
 analog
  begin
  @(initial_step)
  begin
  end
// Switching delay of 200ps between chromia and bottom free FM layer
V(Spin2)<+transition(V(Spin_FM2),190p,0,0);

  end
endmodule
```

Section-5

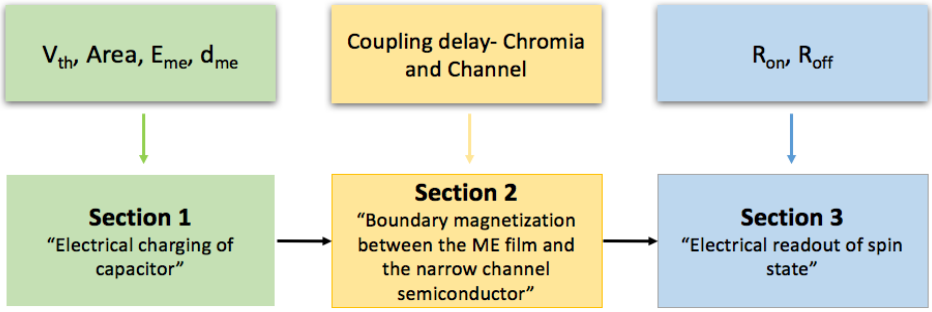
```
// Verilog-A for MEMTJ_XNOR, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
```

```
 `define INITIAL_MODEL @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/

module MEMTJ_XNOR_section5(G2,S2,Spin_FM2);

// inputs terminals
inout G2,S2;
electrical G2,S2;

// Terminal for the spin orientation in FM layer
inout Spin_FM2;
electrical Spin_FM2;

/*************************************************************
Parameter Declaration
*************************************************************/
/*----------Threshold of Chromia state inversion in volts---------------*/
parameter real Vtmax=0.055 from [0:inf] ;
/*----------Area of input capacitor-----------------------------------*/
parameter real A= 900e-18 from [0:inf];
/*---------- Coulomb constant, C^2/(m*J)-------------------------------*/
parameter real E0 = 8.854e-12 from [0:inf];
/*----------width of Chromia layer in meter---------------------------*/
parameter real w=10e-9 from [1e-9:100e-9];
/*----------Dielectric constant of Chromia ---------------------------*/
parameter real k=12;

real Vgs; // Input gate voltage
real Tau1; // Switching time for chromia
real vp; // Voltage node defined to represent the memory
real C1; // Input capacitance

/*************************************************************
Body definition
*************************************************************/
analog
begin
  @(initial_step)
  begin
  vp=1;
  C1=(k*E0*A)/w;
  end

if (V(G2,S2) >= Vtmax)
  vp=-1; // chromia spin are oriented down.
else if (V(G2,S2) <= -Vtmax)
  vp=1; // chromia spin are oriented up.
else
        begin                   // chromia spin switching condition not met
```

```
        if (vp ==-1)
                begin
                    vp=-1;
                end

        else if (vp==1)
                begin
                    vp=1;
                end
        else vp =5;
    end

// memory state variable is assignment
V(Spin_FM2)<+ transition(vp,10p,0,0);
// Chromia switches after a delay of 10 picoseconds

end
endmodule
```

MEFET

The code below describes the Verilog-A modeling of the single and dual source MEFET device.



Section-1

```
// Verilog-A for MEFET_1input_spinstate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
`define INITIAL_MODEL
@(initial_step or initial_step("static"))
`define INITIAL_INSTANCE
```

```
/*********************************************************
Module definition
/*********************************************************/

module MEFET_singlesource_section1(G,BG,spin_cr);

// terminal definition of spin vector orientation in chromia
inout spin_cr;
electrical spin_cr;
// input gate terminal
inout G;
electrical G;
// Fixed back gate terminal
inout BG;
electrical BG;
//channel terminal
electrical channel;

/*********************************************************
Parameter Declaration
/*********************************************************/
// threshold voltage for chromia vector switching
parameter real vt= 0.1 from [0:inf];
// MEFET Device dimensions
parameter real A= 900e-18 from [0:inf];
parameter real e0 = 8.854e-12 from [0:inf];
parameter real w = 30E-9 from [0:inf];
parameter real l = 30E-9 from [0:inf];
// top and bottom gate capacitors
branch (G,channel) cap_cr;
branch (BG,channel) cap_al;
// dielectric constants
parameter real k_al = 4 from [0:inf];
parameter real k_cr =12 from [0:inf];
// thickness of the top and bottom gate insulators
parameter real t_al = 30e-9 from [0:inf];
parameter real t_cr = 30E-9 from [0:inf];
// resistor to define boundary condition for switching
parameter real r_int = 1 from [0:inf);

real vm;  // variable for storing the spin state in chromia
real c_al; // capacitance with Alumina as the dielectric
real c_cr; // capacitance with Chromia as the dielectric

/*********************************************************
Body definition
/*********************************************************/
 analog
   begin
```

```
        @(initial_step)
                        begin
                              c_al=(k_al*e0*A)/t_al;
                              c_cr= (k_cr*e0*A)/t_cr;
                             vm=1;
                        end

if ( V(G,BG) >= vt)
              vm=1;         // up
else if (V(G,BG) <= -vt)
              vm=-1;     // down
else if  (V(G,BG)> -vt && V(G,BG) < vt ) begin
                                                    if (vm == -1)   begin
                                                                        vm=-1;
                                                                  end
                                                    else if (vm==1) begin
                                                                        vm=1;
                                                                   end
                                                    else vm =5;
                                                    end
else   vm = 5;

// memory state variable is assigned to the spin_cr terminal.
V(spin_cr)<+ vm;
// Chromia is assumed to switch instantaneously
end
endmodule
```

Section 2

```
`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/
module MEFET_singlesource_section2(spin_cr,spin_channel);

/*************************************************************
Parameter declaration
*************************************************************/
// terminal for spin state of chromia from section 1
inout spin_cr;
electrical spin_cr;
// terminal for spin state in channel induced by the ME chromia through proximity effect
inout spin_channel;
electrical spin_channel;

/*************************************************************
Body
*************************************************************/
```

```
 analog
   begin
       @(initial_step)
      begin
      end
// delay of 3 ps introduced for the spin polarization in chromia due to proximity effect


V(spin_channel)<+ transition(V(spin_cr),3p,0,0);

end
endmodule
```

Section-3

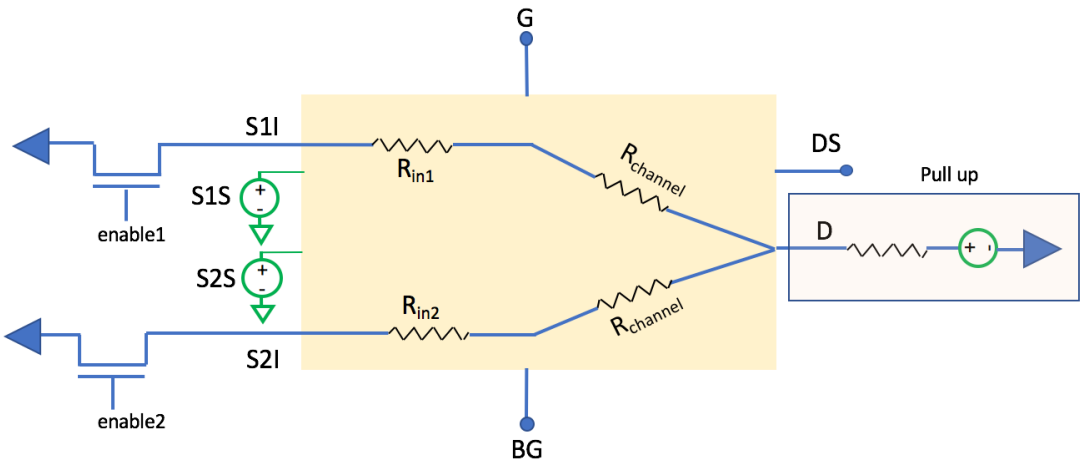
```
`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
`define INITIAL_MODEL @(initial_step or initial_step("static"))
`define INITIAL_INSTANCE

/*********************************************************
Module definition
*********************************************************/

module MEFET_singlesource_section3(spin_channel,D,DS,SI,SS,BG);
// output drain terminal
inout D;
electrical D;
// fixed back gate terminal
inout BG;
electrical BG;
// terminal for injected/detected spin current states at the source/drain terminal
inout SS,DS;
electrical SS,DS;
// terminal for injected current
inout SI;
electrical SI;
// terminal for spin state in the channel
inout spin_channel;
electrical spin_channel;
// channel
electrical channel;
// introduced for branching since there are two resistors in series
electrical SI_int;
// branch definitions
branch (D,SI_int) S_res_on;
branch (D,SI_int) S_res_off;
branch (SI_int,SI) S_res_int;
```

```
/*************************************************************
Parameter Declaration
/*************************************************************/

// on-off resistances in ohms for the WSe2 channel
parameter real roff= 100000k from [0:inf];
parameter real ron= 1k from [0:inf];

// threshold voltage in volts for chromia vector switching
parameter real vt= 0.1 from [0:inf];

// resistance value in ohms of the internal resistor introduced for boundary condition for switching

parameter real r_int = 1 from [0:inf);
real vm;
real V_Dspin;
real gm_on; // conductance in on-state
real gm_off; // conductance in off-state
real vres;
real gm_int;

/*************************************************************
Body definition
/*************************************************************/

 analog
  begin
     @(initial_step) // initialization
    begin
          vm=1;
          gm_on=(1/ron);
          gm_off= (1/roff);
          gm_int=(1/r_int);
    end

vss=V(SS); // voltage at the spin injection terminal defined as +1V or -1V in the simulation.

I(S_res_int)  <+ V(S_res_int)* gm_int;    // current across the internal resistor
vres= V(S_res_int);                       // voltage across the internal resistor

// if spin injection is enabled
if (vres <= vt)
          begin
               if (V(spin_channel)==1)    // if chromia spin are oriented up.
                         begin
                              vm=1;
                                   begin
                                        if (vss ==1)  // if up spin is injected into the source
                                          begin
                                               I(S_res_on) <+ (gm_on) * V(S_res_on);  // current in on-state
                                               V_Dspin= vm;
                                          end
```

```
                    else if (vss ==-1 ) // if down spin is injected into the source
                        begin
                            I(S_res_off) <+  (gm_off) * V(S_res_off); // current in off-state
                            V_Dspin= vm; // memory state comes from the chromia spin vectors
                        end
                    else V_Dspin= 0 ;
                end
        end
else if (V(spin_channel)==-1) // if chromia spin are oriented down.
        begin
            vm=-1;
                begin
                    if (vss ==1)   // if up spin is injected into the source
                        begin
                            I(S_res_off) <+  (gm_off) * V(S_res_off);
                            V_Dspin= vm ;
                        end
                    else if (vss ==-1) // if down spin is injected into the source
                        begin
                            I(S_res_on) <+ (gm_on) * V(S_res_on);
                            V_Dspin= vm ;
                        end
                    else V_Dspin= 0 ;
                end
        end
else
    begin     // if the chromia spin vector switching condition isn't met.
        if (vm==1)  // up spin in chromia due to inherent memory
            begin
                vm=1;  // no state change
                    begin
                        if (vss ==1) // if up spin is injected into the source
                            begin
                                I(S_res_on) <+(gm_on) * V(S_res_on);
                                V_Dspin= vm ;
                            end
                        else if (vss ==-1) // if down spin is injected into the source
                            begin
                                I(S_res_off) <+  (gm_off) * V(S_res_off);
                                V_Dspin= vm ;
                            end
                        else V_Dspin= 0 ;
                    end
            end
        else if (vm==-1)  // down spin in chromia due to inherent memory
            begin
                vm=-1; // no state change
                    begin
                        if (vss ==1) // if up spin is injected into the source
                            begin
                                I(S_res_off) <+ (gm_off) * V(S_res_off);
                                V_Dspin= vm;
                            end
```

```
                                        else if (vss ==1) // if down spin is injected into the source
                                            begin
                                                I(S_res_on) <+(gm_on) * V(S_res_on);
                                                V_Dspin= vm;
                                            end
                                        else V_Dspin= 0 ;
                                    end
                                end
                            else   V_Dspin= 0 ;
                        end
                end
else V_Dspin= 0 ;

// the drain spin state comes from the memory state in the device
V(DS) <+transition(V_Dspin,0,0,0);

end
endmodule
```

MEFET- DUAL SOURCE



Section -1

```
// Verilog-A for MEFET_2input_spinstate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall


`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
```

```
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
`define INITIAL_MODEL @(initial_step or initial_step("static"))
`define INITIAL_INSTANCE

/*************************************************************
Module definition
*************************************************************/
module MEFET_dualsource_section1(G,BG,spin_cr);

// terminal definition of spin vector orientation in chromia
inout spin_cr;
electrical spin_cr;
// input gate terminal
inout G;
electrical G;
// Fixed back gate terminal
inout BG;
electrical BG;
//channel terminal
electrical channel;

/*************************************************************
Parameter Declaration
*************************************************************/
// threshold voltage for chromia vector switching
parameter real vt= 0.1 from [0:inf] ;
// MEFET Device dimensions
parameter real A= 900e-18 from [0:inf] ;
parameter real e0 = 8.854e-12 from [0:inf];
parameter real w = 30E-9 from [0:inf];
parameter real l = 30E-9 from [0:inf];
// top and bottom gate capacitors
branch (G,channel) cap_cr;
branch (BG,channel) cap_al;
// dielectric constants
parameter real k_al = 4 from [0:inf];
parameter real k_cr = 12 from [0:inf];
// thickness of the top and bottom gate insulators
parameter real t_al = 30e-9 from [0:inf];
parameter real t_cr =30E-9 from [0:inf];
// resistor to define boundary condition for switching
parameter real r_int = 1 from [0:inf);
// variable for storing the spin state in chromia
real vm;
real c_al;
real c_cr;
/*************************************************************
Body definition
*************************************************************/
 analog
   begin
```

```
        @(initial_step)
                        begin
                            c_al=(k_al*e0*A)/t_al;
                            c_cr= (k_cr*e0*A)/t_cr;
                            vm=1;
                        end
if (V(G,BG) >= vt)
                    vm=1;        // up
else if (V(G,BG) <= -vt)
                    vm=-1;     // down
else if  (V(G,BG)> -vt && V(G,BG) < vt )
                                                    begin
                                                      if (vm == -1)
                                                                begin
                                                                    vm=-1;
                                                                end
                                                      else if (vm==1)
                                                                begin
                                                                    vm=1;
                                                                end
                                                      else vm =5;
                                                    end
else   vm = 5;

// memory state variable is assigned to the spin_cr terminal.
V(spin_cr)<+ vm;
// Chromia switches instantaneously

end
endmodule
```

Section -2

```
// Verilog-A for MEFET_2input_spinstate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`include "constants.vams"
`include "disciplines.vams"

/*************************************************************
Module definition
*************************************************************/
module MEFET_dualsource_section2(spin_cr,spin_channel);

/*************************************************************
Parameter declaration
*************************************************************/
// terminal for spin state of chromia from section 1
inout spin_cr;
electrical spin_cr;
// terminal for spin state in channel induced by the ME chromia through proximity effect
```

```
inout spin_channel;
electrical spin_channel;

/*********************************************************
Body definition
*********************************************************/
 analog
   begin
       @(initial_step)
      begin
      end
// Delay of 3 ps introduced for the spin polarization in chromia due to proximity effect
V(spin_channel)<+ transition(V(spin_cr),3p,0,0);

end
endmodule
```

Section -3

```
// Verilog-A for MEFET_2input_spinstate, Verilog-A
// Authors: Nishtha Sharma, Andrew Marshall

`resetall
`include "constants.vams"
`include "disciplines.vams"
`define explimit 85.0
`define exp(x) exp(min(max((x),-`explimit),`explimit))
`define sqrt(x) pow( (x), 0.5)
 `define INITIAL_MODEL  @(initial_step or initial_step("static"))
 `define INITIAL_INSTANCE

/*********************************************************
Module definition
*********************************************************/

module MEFET_dualsource_section3(spin_channel,D,DS,S1I,S1S,S2S,S2I,BG);
// output drain terminal
inout D;
electrical D;
// terminal for spin state in the channel
inout spin_channel;
electrical spin_channel;
// terminal for injected/detected spin current states at the source (S1,S2)/drain (D) terminal
inout S1S,S2S,DS;
electrical S1S,S2S,DS;
// terminal for injected current
inout S1I,S2I;
electrical S1I,S2I;
// fixed back gate terminal
inout BG;
electrical BG;
```

```
// channel
electrical channel;
// introduced for branching since there are two resistors in series
electrical S1I_int, S2I_int;
// branch definitions
branch (D,S1I_int) S1_res_on;
branch (D,S1I_int) S1_res_off;
branch (D,S2I_int) S2_res_on;
branch (D,S2I_int) S2_res_off;
branch (S1I_int,S1I) S1_res_int;
branch (S2I_int,S2I) S2_res_int;

/*************************************************************
Parameter Declaration
*************************************************************/

// on-off resistances in ohms for the WSe2 channel
parameter real roff= 10000000k from [0:inf];
parameter real ron= 1k from [0:inf];

// threshold voltage in volts for chromia vector switching
parameter real vt= 0.1 from [0:inf];
parameter real vtm= 0.05 from [0:inf];
parameter real r1_int = 1 from [0:inf);
parameter real r2_int = 1 from [0:inf);

real vm;
real V_Dspin;
real gm_on;
real gm_off;
real vgbg;
real gm1_int;
real gm2_int;
real vs1s;
real vs2s;

/*************************************************************
Body definition
*************************************************************/
 analog
  begin
     @(initial_step)
                  begin
                        vm=-1;
                        gm_on=(1/ron);
                        gm_off= (1/roff);
                        gm1_int=(1/r1_int);
                        gm2_int=(1/r2_int);
                  end

// Voltage at the spin injection terminals defined in the simulation as +1V or -1V.
vs1s=V(S1S);
vs2s=V(S2S);
```

```
 // Current across the internal resistor
I(S1_res_int)  <+ V(S1_res_int)* gm1_int;
I(S2_res_int) <+ V(S2_res_int)* gm2_int;

// 'Up' spin is injected ********************************************************
                    // down spins are injected**********
if (V(S1_res_int) <= vtm)
                begin
                   if (V(S2_res_int) <= vtm)
                      begin
                           if (V(spin_channel)==1)  // if chromia spin are oriented up.
                              begin
                                   vm=1;
                                        begin
// The conditions make the spin injection terminal flexible for injecting up or down spins.
                                             if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                   I(S1_res_on) <+ (gm_on) * V(S1_res_on);   // current in on-state
                                                   I(S2_res_off) <+ (gm_off) * V(S2_res_off); // current in off-state
                                                   V_Dspin= vm;
                                                end
                                             else if (vs1s ==-1 && vs2s ==1)
                                                begin
                                                   I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                   I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                                                   V_Dspin= vm;
                                                end
                                            else V_Dspin= 0 ;
                                         end
                              end
                           else if (V(spin_channel)==-1)  // if chromia spin are oriented down.
                              begin
                                   vm=-1;
                                        begin
                                           if (vs1s ==1 && vs2s ==-1)
                                              begin
                                                 I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                 I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                                                 V_Dspin=vm;
                                              end
                                           else if (vs1s ==-1 && vs2s ==1)
                                              begin
                                                 I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                                 I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                 V_Dspin= vm ;
                                              end
                                           else V_Dspin= 0 ;
                                        end
                              end
                           else
                              begin     // if the chromia spin vector switching condition isn't met.
                                   if  (vm==1)
```

```
                                    begin
                                      vm=1;
                                          begin
                                              if (vs1s ==1 && vs2s ==-1)
                                                  begin
                                                    I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                                    I(S2_res_off) <+ (gm_on) * V(S2_res_off);
                                                    V_Dspin= vm ;
                                                  end
                                             else if (vs1s ==-1 && vs2s ==1)
                                                  begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                                                   V_Dspin= vm ;
                                                  end
                                             else V_Dspin= 0 ;
                                          end
                                      end
                                 else if (vm==-1)
                                          begin
                                           vm=-1;
                                          begin
                                              if (vs1s ==1 && vs2s ==-1)
                                                  begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                                                    V_Dspin= vm;
                                                  end
                                              else if (vs1s ==1 && vs2s ==-1)
                                                  begin
                                                    I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                    V_Dspin= vm;
                                                  end
                                             else V_Dspin= 0 ;
                                          end
                                      end
                                  else   V_Dspin= 0 ;
                               end
                        end

// down spin injection is disabled**********
                    else if (V(S2_res_int) > vtm)
                            begin
                                if (V(spin_channel)==1)
                                        begin
                                            vm=1;
                                                begin
                                                    if (vs1s ==1 && vs2s ==-1)
                                                                begin
                                                                    I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                                    V_Dspin=vm;
```

```
                                    end
                                else if (vs1s ==-1 && vs2s ==1)
                                    begin
                                        I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                        I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                        V_Dspin=vm;
                                    end
                                else V_Dspin= 0 ;
                            end
                    end
        else if (V(spin_channel)==-1)
                    begin
                        vm=-1;
                            begin
                                if (vs1s ==1 && vs2s ==-1)
                                    begin
                                        I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                        I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                        V_Dspin=vm;
                                    end
                                else if (vs1s ==-1 && vs2s ==1)
                                    begin
                                        I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                        I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                        V_Dspin=vm;
                                    end
                                else  V_Dspin= 0 ;
                            end
                    end
        else
            begin
                if (vm==1)
                        begin
                            vm=1;
                               begin
                                if (vs1s ==1 && vs2s ==-1)
                                        begin
                                            I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                            I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                            V_Dspin=vm;
                                        end
                                else if (vs1s ==-1 && vs2s ==1)
                                        begin
                                            I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                            I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                            V_Dspin=vm;
                                        end
                                else V_Dspin= 0 ;
                                end
                        end
                else if (vm==-1)
                        begin
                            vm=-1;
```

```
                                                    begin
                                                      if (vs1s ==1 && vs2s ==-1)
                                                                begin
                                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                                    V_Dspin=vm;
                                                                end
                                                      else if (vs1s ==-1 && vs2s ==1)
                                                                begin
                                                                    I(S1_res_on) <+ (gm_on) * V(S1_res_on);
                                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                                    V_Dspin=vm;
                                                                end
                                                      else V_Dspin= 0 ;
                                                    end
                                                end
                                        else   V_Dspin= 0 ;
                                    end
                                end
else   V_Dspin= 0 ;

end
// up spin injection is disabled ************************************************************
// down spins are injected**********

else if (V(S1_res_int) > vtm)
                begin
                  if (V(S2_res_int) <= vtm)
                      begin
                        if (V(spin_channel)==1)
                            begin
                                vm=1;
                                    begin
                                      if (vs1s ==1 && vs2s ==-1)
                                                    begin
                                                        I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                        I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                        V_Dspin=vm;
                                        else if (vs1s ==-1 && vs2s ==1)
                                                    begin
                                                       I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                       I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                                                       V_Dspin=vm;
                                                    end
                                        else V_Dspin= 0 ;
                                    end

                             end
                        else if (V(spin_channel)==-1)
                            begin
                                vm=-1;
                                    begin
                                      if (vs1s ==1 && vs2s ==-1)
```

```
                    begin
                        I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                        I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                        V_Dspin=vm;
                     end
            else if (vs1s ==-1 && vs2s ==1)
                    begin
                        I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                        I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                        V_Dspin=vm;
                    end
          else  V_Dspin= 0 ;
        end
    end
else
    begin
        if (vm==1)
            begin
              vm=1;
                begin
                  if (vs1s ==1 && vs2s ==-1)
                      begin
                          I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                          I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                         V_Dspin=vm;
                      end
                  else if (vs1s ==-1 && vs2s ==1)
                      begin
                          I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                          I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                          V_Dspin=vm;
                      end
                  else V_Dspin= 0 ;
                end
            end
        else if (vm==-1)
            begin
              vm=-1;
                begin
                  if (vs1s ==1 && vs2s ==-1)
                      begin
                          I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                          I(S2_res_on) <+ (gm_on) * V(S2_res_on);
                          V_Dspin=vm;
                      end
                  else if (vs1s ==-1 && vs2s ==1)
                      begin
                          I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                          I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                          V_Dspin=vm;
                      end
                  else V_Dspin= 0 ;
                end
```

```
                                end
                            else   V_Dspin= 0 ;
                        end
end
// down spin injection is disabled**********
else
                if (V(S2_res_int) > vtm)
                    begin
                        if (V(spin_channel)==1)
                            begin
                                vm=1;
                                    begin
                                     if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                    V_Dspin= vm ;
                                                end
                                      else if  (vs1s ==-1 && vs2s ==1)
                                                begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                    V_Dspin= vm ;
                                                end
                                            else V_Dspin= 0 ;
                            end
                    end
                        else if (V(spin_channel)==-1)
                            begin
                                vm=-1;
                                    begin
                                      if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                    V_Dspin=vm;
                                                end

                                      else if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                    I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                    I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                    V_Dspin= vm;
                                                end
                                      else V_Dspin= 0 ;
                                    end
                            end
                        else
                             begin
                                if (vm==1)
                                      begin
                                                vm=1;
                                                  begin
```

```
                                        if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                   I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                   I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                   V_Dspin= vm;
                                                end
                                        else if (vs1s ==-1 && vs2s ==1)
                                                begin
                                                   I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                   I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                   V_Dspin= vm;
                                                end
                                        else V_Dspin= 0; end
                                    end
                            else
                              if (vm==-1)
                                  begin
                                    vm=-1;
                                      begin
                                        if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                   I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                   I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                   V_Dspin= vm ;
                                                end
                                         else if (vs1s ==1 && vs2s ==-1)
                                                begin
                                                   I(S1_res_off) <+ (gm_off) * V(S1_res_off);
                                                   I(S2_res_off) <+ (gm_off) * V(S2_res_off);
                                                   V_Dspin= vm;
                                                end
                                       else V_Dspin= 0;
                                    end
                                  end
                    else   V_Dspin= 0;
                              end
else   V_Dspin= 0;
end
else    V_Dspin= 0;
// the drain spin state comes from the memory state in the device
V(DS) <+ transition(V_Dspin,0);

end
endmodule
```

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BIOGRAPHICAL SKETCH

Nishtha Sharma is a Ph.D. candidate and research assistant in the Department of Electrical Engineering (EE) at The University of Texas at Dallas (UTD). She has previously interned at ARM and GlobalFoundries. She completed her master's degree in electrical engineering from The University of Texas at Dallas in 2015. Her areas of interest are beyond-CMOS logic and memory devices, including development of SPICE models for low-power, voltage controlled Magnetic Tunnel Junctions (MTJ) that utilize novel magneto-electric materials as their switching components, and ferroelectric memory devices. She has worked on the layout of memory array cells for the Nanoelectronics Research Initiative (NRI) and some STARNET devices. She has also worked on the development of a MATLAB decks for the Magneto-electric Magnetic Tunnel Junction (ME-MTJ) devices. Her latest achievements include the development of Verilog-A based compact models for the ME-MTJ based devices and circuit design. In addition, she has also worked on the simulation of ME-MTJ based complex circuits and their benchmarking with respect to CMOS based circuits. Her latest research efforts include the compact model development for the Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) device and the Magneto-electric Spin Field-Effect Transistor (MEFET). She is also working on exploration of the performance of circuits (non-volatile SRAM, majority gate logic and full adder, etc.) that utilize these devices as their core elements.

CURRICULUM VITAE

Nishtha Sharma

PROFESSIONAL EXPERIENCE

ARM Inc., Austin, TX Feb-May 2017
Research Intern
Supervisor: Dr. Brian Cline

- Spin based device landscape study & presentation
- Detailed analysis of the Magneto-electric Magnetic Tunnel Junction (ME-MTJ) electrical and physical characteristics, including compact modeling enhancements and layout
- LVS decks modification and parasitic extraction of the ME-MTJ based devices
- HSPICE simulations of the ME-MTJ based circuits

GlobalFoundries, Malta, NY June-Aug 2016
SRCEA Intern Scholar
Supervisor: Dr. Ajey Jacob

- Study of the spin based devices and in-depth analysis of the switching mechanisms
- Power-performance-area (PPA) analysis of novel Spin Transfer Torque Magneto-resistive Random-Access Memory (STT-MRAM) devices

EDUCATION

University of Texas at Dallas, Richardson, TX May 2015-Dec 2017 (expected)

- **Ph.D.** in Electrical Engineering
- Dissertation title: "Circuit level modeling of spintronic devices"
- Faculty Advisor: Dr. Andrew Marshall

University of Texas at Dallas, Richardson, TX Jan 2014- Dec 2015

- **M.S.** in Electrical Engineering
- Faculty Advisor: Dr. Andrew Marshall

Amity University, Uttar Pradesh, India Aug 2007- May 2011

- **B.Tech** in Electronics and Communication Engineering

PATENTS

- N. Sharma, A. Marshall, P. Dowben, UMMTJ (Unipolar Magneto-electric Magnetic Tunnel Junction), disclosed 9/26/16, Provisional patent pending; USPTO issued January 23, 2017; application Serial Number 62/449,199; SRC IP1586N
- N. Sharma, A. Marshall, F. Register, R. Deng, B. Ghosh, S. Banerjee "RKKY (Ruderman-Kittel-Kasuya-Yosida) Ultra-compact circuit designs for magneto-electric device applications" (Pending).

RESEARCH EXPERIENCE

University of Texas at Dallas, Richardson, TX Jan 2015- Present
Research Assistant

- Compact modeling of the Magneto-electric Field Effect Transistor (MEFET) device
- Verilog-A modeling of the Unipolar Magneto-electric Magnetic Tunnel Junction (UMMTJ) device
- Verilog-A modeling of analog variations of ME-MTJ device and its derived structures
- MATLAB modeling of the ME-MTJ device and derived structures
- Verilog-A modeling of the ME-MTJ device and its derived structures
- MATLAB modeling of the Ferroelectric Tunnel Junction (FTJ)
- Analyzed the device structure derived from the basic ME-MTJ device, i.e., Inverter/Buffer, XOR/XNOR gate, Majority gate and NAND/NOR gate
- Comparison between current-controlled and voltage controlled beyond-CMOS devices
- Energy-delay analysis of the ME-MTJ derived devices w.r.t. high-performance and low-power CMOS
- Area estimation of beyond-CMOS devices using Cadence Virtuoso layout editor
- Performance and area comparison between CMOS and ME-MTJ based one-bit full adder
- Dual gate InAs Tunnel Field-Effect Transistor (TFET) and single gate AlGaSb-InAs TFET logic gate HSPICE simulations
- Performance comparison of CMOS and TFET ring oscillators
- Analysis of leakage power vs. voltage supply for various CMOS based level shifters
- Analysis of ME-MTJ device logic operation

PUBLICATIONS

- **Sharma, Nishtha**, et. al. "Memory Circuits using Resonant Charge-based Devices" IEEE Des. Test (submitted).
- **Sharma, Nishtha**, et. al. "Compact Modeling and Design of Magneto-electric Transistor Devices and Circuits " IEEE Des. Test (submitted).
- **Sharma Nishtha,** et al. "VerilogA based Compact model of a ME-SpinFET device." Energy Efficient Electronic Systems (E3S), 2017 Fifth Berkeley Symposium on. IEEE, 2017 (Accepted).
- **Sharma, Nishtha,** et. al. "Novel Ring Oscillator Design using ME-MTJ Based Devices " Energy Efficient Electronic Systems (E3S), 2017 Fifth Berkeley Symposium on. IEEE, 2017 (Accepted).
- Guanhua Hao, Nicholas Noviasky, Shi Cao, Ildar Sabirianov, Yuewei Yin, Carolina C. Ilie, Eugene Kirianov, **Nishtha Sharma,** et. al. "Some Device Implications of Voltage Controlled Magnetic Anisotropy in Co/Gd2O3 Thin Films Through REDOX Chemistry", Journal of Magnetism and Magnetic Materials 87.3 (2017) (Accepted).
- **Sharma, Nishtha,** et. al. "Magneto-Electric Magnetic Tunnel Junction based Analog Circuit options" System-on-Chip Conference (SOCC), 2017 30th IEEE International. IEEE, 2017 (Accepted).
- **Sharma, Nishtha,** et. al. "VerilogA Compact Model of a ME-MTJ Based XNOR/NOR Gate". Nanoscale Architectures, 2017. NANOARCH 2017. IEEE International Symposium on. IEEE, 2017 (Accepted).
- L. F. Register II, et al. "Resonant Interlayer Tunneling in 2D Van Der Waals-Materials-Based Channel-Dielectric-Channel Systems and Possible Device and Circuit Applications" Electrochemical and Solid-State Letters 7.7 (2017) (in press).
- **Sharma, Nishtha**, et. al. " Unipolar Magnetoelectric Magnetic Tunnel Junction (UMMTJ) Devices and Circuits." Nanotechnology (IEEE-NANO), 2017 IEEE 17th International Conference on. IEEE, 2017 (Accepted).
- **Sharma, Nishtha,** et. al. "Multi-bit Adder Design using the Compact Model of the ME-MTJ device and its Derived Structures." The 11th International Conference on Advanced Semiconductor Devices and Microsystems 2016, IEEE, 2016.

- A. Marshall, **N. Sharma**, J.P. Bird " Memory Circuits using NanoFerroic Devices." Circuits and Systems Conference (DCAS), 2016 IEEE Dallas. IEEE, 2016.
- **Sharma Nishtha,** et al. "VerilogA based Compact model of a three-terminal ME-MTJ device." 2016 16th IEEE Conference on Nanotechnology, IEEE NANO 2016.
- **Sharma, Nishtha**, et al. "Compact-device model development for the energy-delay analysis of magneto-electric magnetic tunnel junction structures." Semiconductor Science and Technology 31.6 (2016): 065022.
- **Sharma, Nishtha**, et al. "Magneto-electric magnetic tunnel junction logic devices." Energy Efficient Electronic Systems (E3S), 2015 Fourth Berkeley Symposium on. IEEE, 2015.
- **Sharma, Nishtha**, et al. "Magneto-electric magnetic tunnel junction as process adder for non-volatile memory applications." Circuits and Systems Conference (DCAS), 2015 IEEE Dallas. IEEE, 2015.

PRESENTATIONS

- TECHCON, Austin, TX "Compact modeling of Magneto-electric Spin Field Effect Transistor Device"- Poster and Oral presentation, 2017, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- IEEE NANO, Pittsburgh, PA "Unipolar Magneto-electric Magnetic Tunnel Junction Devices and Circuits"- Oral presentation, 2017, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- TECHCON, Austin, TX "Compact Model of the ME-MTJ Device and its Derived structures for Logic and Memory"- Poster and Oral presentation, 2016, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- TxACE Symposium, Dallas, TX, "Spice Compatible Compact Model of the ME-MTJ device and its Derived Structures."- Poster presentation, 2016, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- CNFD annual meeting, Lincoln, NE, Sep 30-31 2016 "Spice Compatible Compact Model of the ME-MTJ device and its Derived Structures" poster presentation, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- GlobalFoundries internal conference "Benchmarking e-MRAM". Oral presentation, **Nishtha Sharma**, Karthik Chandrasekharan, Ajey Jacob, George Gomba.
- 2015 Fourth Berkeley Symposium on. IEEE, Berkeley, CA, Oct 1-2 2015 "Magneto-electric Magnetic Tunnel Junction logic devices." poster presentation, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- CNFD annual meeting, Lincoln, NE, Sep 9-10 2015 "Circuit, Layout and Performance of ME-MTJ logic" poster presentation, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- TECHCON, Austin, TX "Compact, Non-Volatile Logic Gates Based on Magneto-Electric Magnetic Tunnel Junctions"- Poster and Oral presentation, 2015, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- Circuits and Systems Conference (DCAS), Dallas, TX, Oct 12-13, 2015 "Magneto-electric Magnetic Tunnel Junction as process adder for non-volatile memory applications."- Poster presentation, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- Circuits and Systems Conference (DCAS), Dallas, TX, Oct 12-13, 2015 "TFET Performance of Logic Circuits using Tunneling FETs." "- Poster presentation, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.
- TxACE Symposium, Dallas, TX, "Magneto-electric Magnetic Tunnel Junction Devices and Circuits."- Poster presentation, 2015, **Nishtha Sharma**, Andrew Marshall, Jonathan Bird and Peter Dowben.

AWARDS/HONORS

- Best poster award at the SRC-CNFD review — Aug 2017
- SRC-CNFD scholarship — Jan 2015-Present
- Erik Jonsson school of engineering scholarship — Jan 2015-Present

SKILLS

- Circuit design tools: HSPICE, Cadence suite, Synopsys IC validator and StarRC
- Mathematical software: MATLAB
- Programming languages: Verilog-A, C, C++, and Verilog
- Operating systems: MAC, LINUX, Win32 variants (XP/Vista/Windows 7/8)

SELECTED COURSES AND PROJECTS

Electronic, Magnetic and Optical Materials, VLSI design, Advanced VLSI design, Analog IC design, Semiconductor Device Characterization, Active Semiconductor Devices, Advanced Digital Logic, Energy Harvesting, Storage and Powering for Microsystems.

Design of low- power fully- differential operational amplifier and verify the performance using HSPICE. Tools used: Virtuoso schematic editor, virtuoso analog design environment, Spectre circuit simulator, and SPICE simulator, HSPICE.

Design of high speed and low-power 21b*21b multiplier using Booth-2 method. Tools used: Virtuoso schematic editor, virtuoso analog design environment, Spectre circuit simulator, and SPICE simulator, Silicon smart, Primetime. The design was divided into Booth-2 Partial Products, Partial Product Compressor, and a 42b Carry look ahead adder. A maximum delay path of 4.47ns and .0106w power with a majority from switching was calculated by primetime.

Design and layout of 128 word SRAM (word size is 10bits) using the IBM 130nm process. Designed a full custom 128 word SRAM with memory cell size, total area and speed constraints. Tools used: Virtuoso schematic editor, Virtuoso layout editor, virtuoso analog design environment, Spectre circuit simulator, and SPICE simulator. Successfully designed SRAM with minimum area.

OTHER WORK EXPERIENCE

Student worker at Information Resources, UT Dallas, Texas, US June'14-Jan'15

- Helpdesk staff at Information Resources, University of Texas at Dallas, providing end-user technical, network, and computer account support

Software engineering analyst, Accenture Services Private ltd, Gurgaon, India June '11-Dec'13

- Responsibilities included analysis of the business requirement, writing high and low level test cases and capturing the associated defects in defect management tool
- End-to-end knowledge of functional testing
- Experience in setting up test data environment & preparing test cases, reviewing, executing, reporting and tracking the defects
- Recognition and awards from project manager and supervisor on the quality of work delivered

Electrical Engineer Intern, **NTPC, Noida, India** May'10-June'10

- Worked on project 'Automation of ICS Using Visual Basic 6.0' wherein I developed a code to automate a certain process
- Exposed to functions of a thermal power plant and a demineralization (DM) plant
- Developed MS Visio drawings for the actual flow, inlets, and outlets in a DM plant.