DEVELOPMENT OF INDIUM GALLIUM ZINC OXIDE THIN FILM TRANSISTORS ON A SOFTENING SHAPE MEMORY POLYMER FOR IMPLANTABLE NEURAL INTERFACE DEVICES

by

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by

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The continuous improvement in electronic active devices has led to several innovations in semiconductor materials, novel deposition methods, and improved microfabrication techniques. In the same way, the implementation of thin-film technology has revolutionized the semiconductor industry. For instance, the field of flexible electronics has utilized novel thin-film electronics components for the fabrication flexible displays, radio frequency identification (RF-ID) tags, and solar cells. Moreover, flexible electronics have sparked a great interest in the field of bioelectronics, for the fabrication of high-spatial-resolution implantable devices for neural interfaces. This incorporation of thin-film technology can potentially enable stimulation and recording the nervous system activity by utilizing novel, minimally invasive, conformal devices. To achieve this, flexible electronics circuits must possess high performance, reliability, and stability, as well as be resilient to mechanical stress and human body conditions, are some of the requirements that flexible electronics must meet for the realization of these devices. Furthermore, the choice of substrates is also critical since it directly affects final properties of the active devices.

Substrates, which are mechanically and biologically compliant, are preferred. For this reason, novel, softening materials like thiol-ene polymers are considered in this research. This work centers on the development of Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistors (TFT) using the thiol-ene softening polymer as substrate. Functional IGZO-TFTs were fabricated on top of 50 µm of a thiol-ene/acrylate shape memory polymer (SMP) and electrically characterized. Hafnium oxide (HfO_2) deposited at 100°C by atomic layer deposition was used as gate dielectric, and gold (Au) as contacts. The devices were exposed to oxygen, vacuum and forming gas (FG) environments at 250°C to analyze the effects of these atmospheres on the IGZO-TFTs. Improvement in the electrical performance was noticed after the exposure to FG with a significant change in mobility from 0.01 to 30 cm2 V-1s-1, and a reduction in the threshold voltage shift (ΔV_{th}), which it is translated into an increase on stability. Vacuum and oxygen effects were, also analyzed and compared. Furthermore, a time-dependent dielectric breakdown (TDDB) analysis was performed to define the lifetime of the transistors, where a prediction of 10 years at an operational range below 5 V was obtained. Additionally, the TFTs were encapsulated with 5 µm of SMP and exposed to simulated *in vivo* conditions. Up to 10^4 bending cycles were performed to the IGZO-TFTs with a bending radius of 5 mm and then, soaked into PBS solution at 37°C for one week to determine the resilience and reliability of the devices. The encapsulated IGZO-TFTs survived to the PBS environment and demonstrated resilience to mechanical deformation with small changes in the electronic properties. The results provided in this research contribute to the development of complex circuitry based on thin-film devices using mechanically adaptive polymers as a flexible substrate and enable the production of multichannel implantable bioelectronics devices.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

The advance in technology has enabled the development of wearable and implantable bioelectronics capable of monitoring, recording and tracking vital signals to improve the health and quality of life of people. Commercial and research wearable devices have been fabricated to measure heart rate, blood pressure, oxygen levels, and respiration rate [1]. In the same way, implantable devices have been used to control and treat neurological disorders as well as enhance the function of human organs [2]. In order to achieve this function, neural interfaces connect the nerve system with the electronic device in charge of processing the recorded signal or stimulate the nerve tissue. This technology is designed to be implanted in the central (CNS) or peripheral (PNS) nervous system. Where some of them, surround the nerve [3], others are inserted into the brain for deep brain stimulation [4] and others remain on the surface of the nerve tissue [5]. In any case, the implantable neural interface should have the same mechanical properties as the body tissue for chronical implantation. However, the long-term interconnection between the nervous system and the electronic device remains limited principally for the immune and inflammatory response of the body against a foreign body. This response stimulates the formation of scar tissue over the neural interface, which degraded the mechanical stability and performance of the device [6-8]. Another limitation relapse in the performance of the neural interface. In this case, the spatial resolution and stimulation selectivity are limited by the size and density of the electrodes. As the number of electrodes increase, the number of electrical connections also increase. This relation made the volume of the device increase, which creates a bigger tissue damage during the

implantation. Due to these issues among other limitations, a better approach to fabricated high-spatial resolution and chronical neural interface implant is needed.

Flexible electronics is a branch of the electronic field that has migrated from heavy bulk and rigid silicon substrates to flexible, transparent and low weight substrates. The introduction of this technology into the electronic field enabled the development of flexible applications like NFC tags [9], flexible sensors [10], active-matrix flexible displays [11, 12] and bioelectronics [13]. The realization of these applications is mainly based on thin-film electronic components such as capacitors, diodes or transistors. In fact, thin-film transistors (TFTs) are the more common electronic component required for the fabrication of complex circuits that allows the controlling, addressing or amplifying electrical signals. Neural interfaces can take advantage of this technology by integrating TFTs into their electronic design for the fabrication of active electronic circuits capable of increasing the density of electrodes, address specific areas and amplify the bioelectrical signal. However, additional requirements of the neural substrate must be considered.

In order to integrate the flexible electronic technology with neural interface implants, we need to consider certain properties required to address the lifetime and performance limitations of the previous neural interface devices. These requirements are divided into substrate properties and electrical design. In order to address the inflammatory response of the body, we need to choose a flexible and soft material with a low storage modulus. This property will reduce the mechanical mismatch of the device with the body [14]. Additional, compliant behavior will increase the conformability of the device and improve the quality of the electrical signal [15]. In the same way, a substrate compatible with microfabrication process and resilience to high temperatures will help for the fabrication of high-performance TFT [16]. In order to improve the functionality of the

neural interfaces, we need to consider the increase of the number of electrodes without increasing the volume and size of the device, and at the same time keep a low power consumption. One way to achieve these points is by the fabrication of high-performance TFTs that require high mobility and frequency response to keep a low power consumption. In addition, these transistors must show stable behavior and resilience to the body environment to achieve chronic implantation.

1.2 Flexible electronics

Flexible electronics consist in the development of active electronic circuits on a flexible substrate. The idea of having active electronic circuits on a stretchable, lightweight, transparent, conformable and flexible substrate generates great interest due to the broad spectrum of applications such as flexible displays [17], radio frequency identification (RF-ID) [18], and wearable biomedical devices [19-21]. In the same way, the biomedical field has applied the biocompatibility of a certain group of polymers for the fabrication of implantable bioelectronics [22-24]. However, for the realization of any type of implantable bioelectronics, the selection of an appropriate flexible substrate is of significant importance. Besides, of biocompatibility and bio-stability of the substrate, some key requirements must be considered for the fabrication of high-performance TFTs. The substrate must be compatible with micro-fabrication and photolithography processes that include high temperature, chemical and plasma exposure. Additionally, mechanical stability and low deformation are required for the manufacturing process as well as surface roughness in the order of nanometers (10^{-9}) to avoid the generation of stress, delamination, and misalignment between layers and patterns [16]. Within the broad spectrum of flexible substrates that have been used in flexible electronics and bioelectronics, polyamides (PI), polyethylene naphthalate (PEN), polyethylene terephthalate (PET), parylene-C and polydimethylsiloxane (PDMS) have been used

for the fabrication of flexible electronics devices and bioelectronics. However, PEN and PET present thermal instability with temperatures above 150°C that degrades the substrate or creates antistrophic mechanical deformation due to their high coefficient of thermal expansion (CTE). On the other hand, PI (Kapton) and parylene-C have shown compatibility with microfabrication process and high temperatures above 250°C, but these films present surfaces stress that affects the final properties of the active device and in some cases delamination from the substrate. In the same way, PDMS has been used as flexible substrate for TFTs fabrication, but it is hard to process using standard microfabrication techniques. Another flexible material that has been used for biomedical applications and shown compatibility with microfabrication techniques is the shape memory polymers.

1.3 Shape memory polymer (SMP)

The shape memory polymers (SMPs) are stimuli-responsive materials that can actively change from one shape to another and return to their original shape when an external stimulus is applied [25]. The shape memory polymers consist of covalent net-points and switching segments arranged in a network. When the material is thermally heat and reaches its thermal transition temperature (T_{trans}), the molecules switches become active and the polymer enters the soft/rubbery state. This enables the deformation of the network, which is defined by the net-points. This process is better known as shape memory effect (SME), the combination of the molecular network structure and the polymer morphology generates this effect, and its mechanical properties are determined by the variation of the molecular parameter, such as the type of monomers or comonomer ratio [25, 26]. In essence, the SMP is processed into the initial permanent shape, then it is mechanically deformed and fixed into a temporary shape (programming). By the application of an external stimulus such

as heat, light or a change of pH in the solution, among others [27-29], the recovery response effect is triggered and the polymer returns to its original (permanent) shape [26]. In the same way, the SMP has the ability to decrease its Young's modulus 2 orders of magnitude or more [30, 31]. Due to these properties, the shape memory polymers have been integrated into different areas and applications, for example, smart fabrics, mobile phones, and medical devices, among others. In fact, the biomedical field has been taking advantage of their characteristics for the development of medical applications such as suturing, drug delivery and implantable electrodes [32-34]. The use of polymeric substrates like polyamide, Parylene-C, and SU-8 has been used for the micro-fabrication of bioelectronics devices. However, these polymers generate an inflammatory and immune response due to a mechanical mismatch between the polymer and the tissue [35-37]. On the other hand, elastomers such as polydimethylsiloxane (PDMS) or silicones are soft enough to avoid a mechanical mismatch with the tissue, but because of their low Young's modulus (MPa), these materials present complication during the micro-fabrication and implantation of the device [14, 35]. Therefore, in order to address these issues, the design of a biocompatible polymer substrate, capable of being stiff enough for insertion during the implantation and get soft *in vivo* condition is required. *Ware et al.* have reported the synthesis of a thiol-ene/acrylate-based SMP. This type of SMP is synthesized via the simultaneous reaction of the alkene and thiol functionality in a step-growth mechanism, giving a stoichiometric reaction between these two functional groups, often described as a "click" chemistry. This reaction generates a low cure stress final polymer which is not inhibited by oxygen molecules [35]. In addition, the introduction of multifunctional acrylates into the synthesis of the polymer generates an increase in the crosslink density which rises the rubbery modulus, increases the glass transition of the network and generates a strong

interaction between the thiols and metal atoms such as gold and platinum, improving the adhesion between the polymer and metals film [14]. Beyond the SME and network characteristics, the thiol-ene/acrylate SMP has the ability to reduce its young's modulus 3 order of magnitude (10^3), from GPa to MPa when the glass transition temperature is reached [38]. This softening mechanism can be very helpful in implantable applications since the material will be stiff form the implantation and became complaint once it is implanted into the body. Furthermore, this polymer has proven mechanical and thermal stability against degradation with the capability of withstanding temperatures up to 250°C without a significant mass loss [39]. Additionally, it has been used for the fabrication of neural interface devices, showing compatibility with microfabrication and photolithography processes [3, 33, 37].

1.4 Thin-film transistor (TFT)

The introduction of thin-film transistors (TFTs) into the electronic field became a fascinating evolution in the semiconductor industry that advanced from the heavy bulk and rigid silicon substrate to transparent, flexible, soft and lower weight substrates. Since the fabrication of the first TFT by Weimer *et al.* at the RCA laboratory, the TFT has been constituted of three basics elements, a thin semiconductor film, a dielectric (insulator) layer, and three electrodes [40]. As is illustrated in Figure 1.1, two electrodes (source and drain) are placed at a short distance from each other and in contact with the semiconductor film. Then, the dielectric film (gate dielectric) insulates the semiconductor layer from the third electrode (gate). Due to this simple architecture, the TFT can be fabricated in a different configuration. As is shown in Figure 1.2, the main four configurations are bottom-gate staggered (Figure 1.2a), bottom-gate coplanar (Figure 1.2b), top-gate staggered (Figure 1.2c), and top-gate coplanar (Figure 1.2d). The bottom or top gate describes if the gate

electrode is deposited below or above the semiconductor film. In the same way, the staggered or coplanar structure defines if the source/drain contacts are on top of the active layer or in the same plane as the semiconductor/dielectric interface. These configurations are related to the metal-oxide-semiconductor field-effect transistor (MOSFET) structure and share the same FET working principles. However, the current modulation within the TFT channel is due to the accumulation of carriers (electrons or holes) in the semiconductor/dielectric interface rather than the creation of an inversion layer as in the MOSFET technology. When a voltage is applied to the gate contact, an electric field is formed within the gate dielectric. This field creates a capacitive injection of carriers in the active layer (semiconductor) and attracts either electrons for an n-type or holes for p-type semiconductor. When the gate voltage (V_{GS}) reaches a certain value, the carriers gather in the semiconductor/dielectric interface to form an accumulation layer that allows the current flow between the source and drain contacts. This voltage is known as the threshold voltage (V_{th}), and it defines the minimum voltage required to form a conductive channel in the semiconductor. The value of this parameter can be affected by defects and charge traps in the semiconductor/dielectric interface and dielectric bulk, which also affects the performance stability of the TFT [41-43].

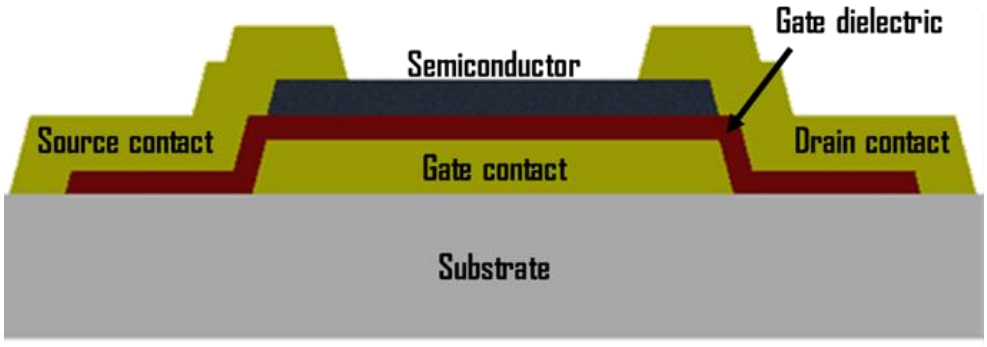

Figure 1.1. Transversal view and schematic structure of a generalized thin-film transistor

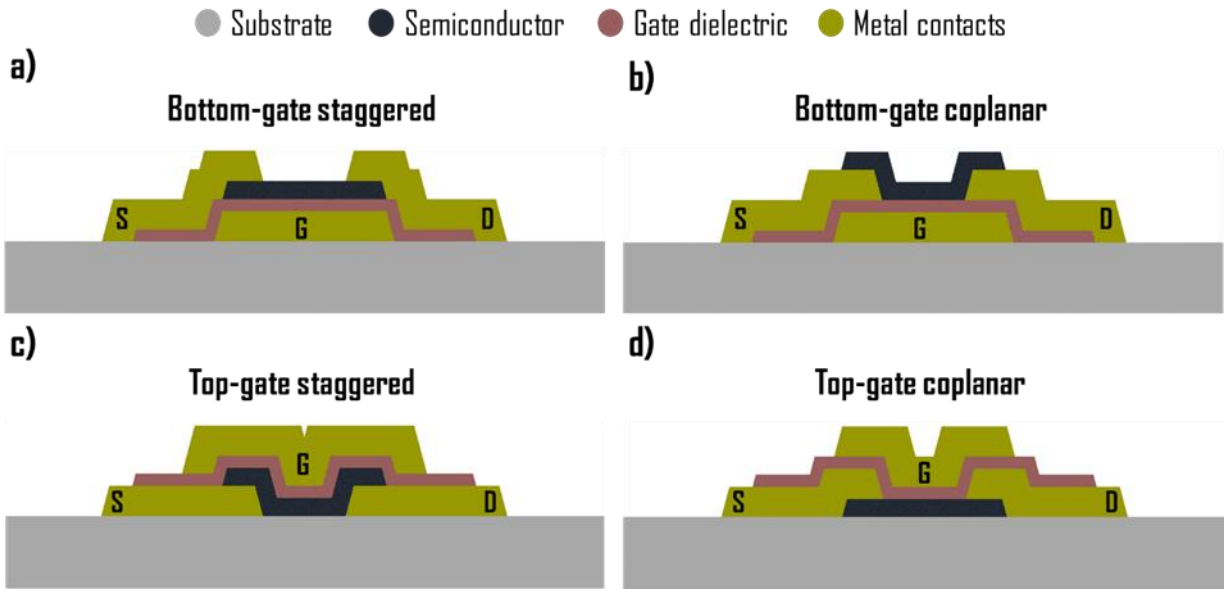

Figure 1.2. Schematics view of the most conventional TFT configurations according with the position of the gate, source and drain contacts. Bottom-gate a) staggered and b) coplanar. Top-gate c) staggered and d) coplanar

Another parameter that describes the performance of the TFT is the carrier or saturation mobility (μ_{sat}). This parameter describes how efficient the charge carriers (electrons or holes) move through the semiconductor and depends on the number of impurities or defects in the semiconductor film [44]. The mobility influences the maximum current that flows through the active channel. If the mobility increase, the drain current also increases. In the same way, the subthreshold swing (SS) determines the switching frequency of the transistor between the on and off state. This parameter is related to the quality of the semiconductor/dielectric interface and it is affected by the trap density in this region [44]. Besides these three parameters, the contact resistance (R_C) between the source/drain contacts and the semiconductor is another important characteristic that determines the electrical performance of the TFT. A high R_C can limit the TFT's performance and degrades the μ_{sat} and the frequency response [45, 46]. In order to fabricate high-performance transistors, we

need to control these parameters by decreasing the R_C and the SS, increasing the μ_{sat} and tuning the V_{th} value between 0 and 1 V.

1.5 Semiconductors for flexible electronics

The TFT has been a fundamental building block for the development of flexible electronic devices. The constant research in flexible circuits has generated great advances in the fabrication of low-temperature TFTs for flexible polymeric substrates. Studies in semiconductors such as hydrogenated amorphous silicon (a-Si:H), low-temperature polycrystalline silicon (LTPS), organic semiconductors and oxide semiconductors have been done extensively [47-51]. However, Nomura *et al.* achieved a major breakthrough, when he reported a transparent TFT on a flexible polyethylene terephthalate (PET) foil using an amorphous oxide semiconductor (AOS) [52]. This demonstration paved the way for several studies in low-temperature processing amorphous oxide semiconductors TFTs. Additionally, in comparison with the different available semiconductor materials, AOSs have demonstrated several advantages in cost, microfabrication and scalability among others [16, 53, 54] (Table 1.1). AOSs became a promising class of TFTs due to their high carrier concentration (10^{16}-10^{21} cm^{-3}), transparency ($E_g > 3eV$), amorphous structure that yields to $\mu_{sat} > 10$ cm^2 $V^{-1}s^{-1}$ and ability to be deposit at low temperatures [55-57]. These properties are attributed to the electronic orbital structure of the oxide semiconductors. The direct overlap of the metal s orbitals creates a conductive path where free electrons can move. This characteristic permits the deposition of AOS in an amorphous state without significant degradation of the electrical parameters. Zinc oxide (ZnO) is one of the binary AOS used for the development of TFTs on flexible substrates, because of its low-temperature processing and mobility values that range between 0.2 to 40 $cm^2V^{-1}s^{-1}$ [58]. However, this material tends to form a polycrystalline

structure that leads to the generation of grain boundary defects. This characteristic induces a non-uniform layer that affects the TFT performance over larger areas [53, 58]. The addition of indium (In) to the ZnO semiconductor generates a semiconductor with a stable amorphous phase that suppresses the formation of grain boundary defects. Indium zinc oxide (IZO) presents uniformity on a large scale and high mobility. Nevertheless, the addition of indium increase the carrier concentration ($N>10^{17}$ cm^{-3}) that leads to a high I_{off} and low On/Off current ratio (I_{on}/I_{off}) [16], [53]. In order to control the increase of carrier concentration, gallium (Ga) atoms were incorporated into IZO. The strong bond of Ga with oxygen atoms decrease the carrier concertation and shit the V_{th} towards positive values [52, 59].

Table 1.1. Comparison between the different semiconductors technologies used in the fabrication of TFTs for flexible electronics: oxide, amorphous silicon, low-temperature polysilicon and organics semiconductors [16, 53, 54].

Properties	**Semiconductors**			
	Oxide	**a-Si:H**	**LTPS**	**Organic**
Mobility ($cm^2V^{-1}s^{-1}$)	1-100	≤ 1	50-100	0.1-10
Operation frequency (MHz)	> 1	≈ 0.1	> 1	≈ 1
Manufacturing cost	Low	Low	High	Low
Microfabrication complexity	Low	Low	High	Low
Process temperatures (°C)	RT-350	150-300	350-500	RT-250
Scalability	High	High	Low	High
Long-term stability	High	Low	High	Low

The indium gallium zinc oxide (IGZO) semiconductor allows the fabrication of TFTs with μ_{sat} > 10 $cm^2V^{-1}s^{-1}$ and I_{on}/I_{off} $>10^6$ [60-62]. Additionally, the amorphous deposition of IGZO at low temperatures and large-scale uniformity permit the fabrication of TFTs on flexible polymeric

substrates. These characteristics made the IGZO the most widely used material for the development of flexible electronic devices.

1.6 Conclusions

The constant research in flexible electronics has enabled new technologies that assist in the development of biomedical devices. An area of this field is dedicated to the development of neural interfaces for long-term implantation, which has been limited by the physiological response of the body and the actual microfabrication technology. In order to overcome these limitations, we need to consider smart materials that can adapt to the body environment and become compliant once they are inserted into the body. Therefore, due to the softening mechanism and microfabrication compatibility, the thiol-ene/acrylate SMP can be used as a substrate for neural interfaces to address these problems. In addition, this type of SMP can assist in the integration of flexible electronics with neural interfaces. The development of high-performance TFT is required to achieve active electronic circuits capable of amplifying, addressing and modulating the neural signals. In order to accomplish this challenge, we opted to use a-IGZO as semiconductor due to its high mobility, high I_{on}/I_{off}, large area scalability, and low-temperature processing. However, further research is required for the complete development of active electronic circuits for neural interfaces. Even though we are using state-of-the-art materials, the fabrication of high-performance TFTs remains challenging. Additionally, the electrical stability, lifetime and resilience to the body environment of the TFTs must be considered. In chapter 3, we conducted a thermal annealing study in order to improve the electrical performance of the fabricated IGZO-TFTs on SMP. Chapters 4 and 5 address the lifetime of the TFTs under constant electrical stress and the electrical stability and resilience of the TFT under *in vivo* conditions.

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CHAPTER 2

MATERIALS AND METHODS

2.1 Materials

The fabrication of the indium gallium zinc oxide thin-film transistors (IGZO-TFTs) on a thiol-ene/acrylate shape memory polymer (SMP) was carried out in a Class 10,000 Cleanroom, except for the polymer substrate, which was synthesized in a standard fume hood. The flexible substrate was synthesized using the following monomers purchased from Sigma-Aldrich: Tricyclo [5.2.1.02,6]decanedimethanol-diacrylate (TCMDA), 1,3,5-Triallyl-1,3,5-triazine-2,4,6 (1H,3H,5H)-trione (TATATO), Tris [2-(mercaptopropionyloxy)ethyl] isocyanurate (TMICN), and 2,2-Dimethoxy-2-phenyl-acetophenone (DMPA) as the photo-initiator. For the fabrication of the TFTs, gold was used for the metal contacts, Indium Gallium Zinc Oxide (In:Ga:Zn:O = 1:1:1:4) target was purchased from Kurt J. Leaker for the semiconductor and for the HfO_2 gate dielectric a tetrakis(dimethylamido)hafnium(IV) precursor from Aldrich for atomic layer deposition (ALD).

2.2 Shape memory polymer synthesis and substrate fabrication

The thiol-ene/acrylate shape memory polymer substrate was synthesized in a standard fume hood, using the following monomers and photo-initiator: 31 mol% of TCMDA, 34.5 mol% of TATATO, 34.5 mol% of TMICN and 0.1 wt% DMPA. The mixture of the monomers was performed in a 20 mL glass vial and mixed using a dual symmetric centrifuge speed mixer. During the preparation, the mixture was cover with aluminum foil and protected from light to avoid premature polymerization. Once the polymer solution was prepared, it was spin-coated on a 5 x 7.5 cm glass slide, at 650 rpm with an acceleration of 100 rpm/s for 60 seconds to form a 50 µm layer. The glass slide surface was previously cleaned with isopropanol (IPA) and sprayed with air to eliminate

any residue. Finally, the spin-coated polymer was exposed to 254 nm UV-light for 120 seconds to start the polymerization and then to 354 nm UV-light for 60 minutes. The substrate was transferred into a vacuum oven at 120°C for a day for curing the polymer, reduce moisture, and remove residue monomers.

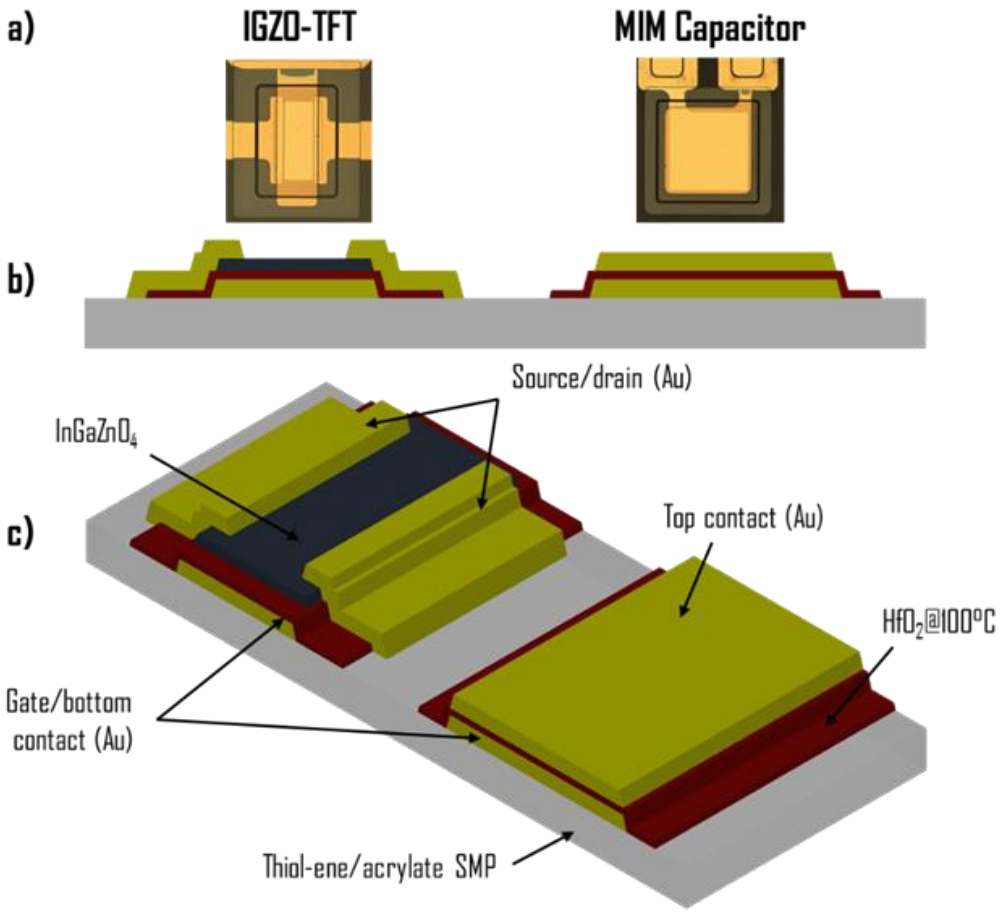

Figure 2.1. a) Top, b) transversal and c) isometric view of the IGZO thin film transistor and MIM HfO_2 capacitor ($4x10^{-4}$ cm^2) fabricated on SMP

2.3 In-Ga-Zn-O_4 thin-film transistor fabrication

The micro-fabrication of the indium gallium zinc oxide thin-film transistors (IGZO-TFTs) was performed using positive photoresist S1318 and standard photolithography process. The photoresist was spun at 2000 rpm with an acceleration of 1000 rpm/s giving a ~2 µm thickness layer. The samples were baked at 85°C for 10 minutes and then exposed to G-line with a dose of 150 mJ/cm^2 and MF-319 was used as a developer. The IGZO-TFTs were fabricated in a bottom-*gate* staggered configuration, as is shown in Figure 2.1. First, 200 nm of gold (Au) is deposited by E-beam evaporation to form the gate contact on top of the 50 µm SMP substrate. Then, a layer of hafnium oxide (HfO_2) was deposited by atomic layer deposition (ALD) at 100°C to pattern the gate dielectric. The IGZO semiconductor was deposited by RF sputtering at room temperature. Finally, another 200 nm Au layer was deposited and patterned to form the source and drain contacts. All the layers were patterned by wet etching: the gold layers were etched by Potassium Iodide, HfO_2 by BOE 7:1 and the IGZO layer with HCl diluted 20:1. At the same time, HfO_2 metal-insulator-metal (MIM) capacitors were fabricated next to the TFT using Au as top/bottom contacts as is shown in Figure 2.1. TFTs with different channel dimensions (W=10, 20, 40, 80 µm /L=5, 10, 20, 30, 40, 50 µm) and MIM capacitors with different areas ($1x10^{-4}$, $2x10^{-4}$ and $4x10^{-4}$ cm^2) were fabricated. A schematic representation of the fabrication process is illustrated in Figure 2.2.

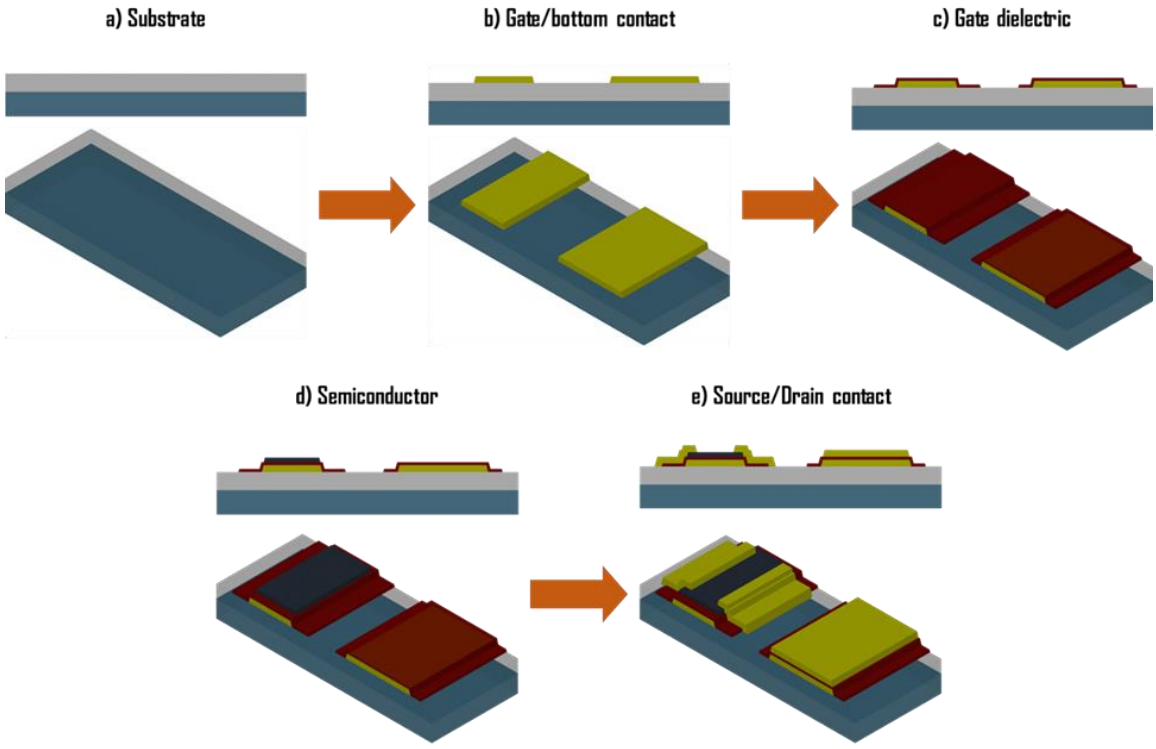

Figure 2.2. Baseline full micro-fabrication process of the IGZO thin film transistors on a thiol-ene/acrylate SMP. Transversal and isometric view of the IGZO-TFT and HfO_2 MIM capacitors. a) SMP substrate on top of a glass slide, b) Au gate and bottom contacts patterns of the TFT and MIM capacitors, c) HfO_2 as gate dielectric, d) IGZO patterning for the active channel, e) Au top contacts to pattern the source, drain and top contacts of the TFT and MIM capacitors.

2.4 Electrical characterization of the IGZO-TFTs

The electrical characterization of the IGZO-TFT was carried out under regular ambient conditions using a Keithley 4200-SCS semiconductor characterization system and a Cascade Microtech probe station. The electrical performance of the TFTs was characterized by plotting the transfer and output curves (Figure 2.3), which are divided into linear and saturation regimes or regions. The linear regime is defined by Equation 2.1 when $V_{DS} << V_{GS} - V_{th}$. Where W and L represent the width and length of the channel, μ the carrier mobility of the active layer, C_{ox} the capacitance density of the gate dielectric, V_{th} the threshold voltage, $V_{DS,}$ and V_{GS} the drain and gate voltage,

respectively. Then, if $V_{DS} \geq V_{GS} - V_{th}$ the transistor operates in the saturation regime and the drain current (I_{DS}) is given by Equation 2.2

$$I_{D,lin} = \frac{W\mu C_{ox}}{L}(V_{GS} - V_{th})V_{DS} \quad \text{Eq (2.1)}$$

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{th})^2 \quad \text{Eq (2.2)}$$

The output curve is obtained by measuring the I_{DS} while the V_{DS} sweeps from zero to a selected voltage (0 to 5 V). At the same time, the V_{GS} is held constant until the sweep ends. Then, the V_{GS} changes to another pre-set voltage and the measurement start over. The loop continues until the V_{GS} have gone through all the pre-set voltages. Figure 2.3a shows a representation of the output curve. The transfer curve (Figure 2.3b) is plotted by holding the V_{DS} constant (5 V) and the V_{GS} sweeps between a certain range (-5 to 5 V), while the I_{DS} is measured. The measurements in the linear regime ($V_{DS} << V_{GS} - V_{th}$) were used to obtain the contact resistance (R_C) that is determined by the junction between the source/drain contacts and the semiconductor. In order to obtain this parameter, it is necessary to measure the total resistance between the source and drain contacts (R_T or R_{SD}) with different channel lengths (L) and different V_{GS}. Where R_T consists of the channel resistance (R_{CH}) and the contact resistance (R_C) as is shown in Equation 2.3. Then, the plot R_T-L gives the R_C by the intersection at the y-axis of the linear fit where L = 0.

$$R_T = R_{CH} + 2R_C \quad \text{Eq (2.3)}$$

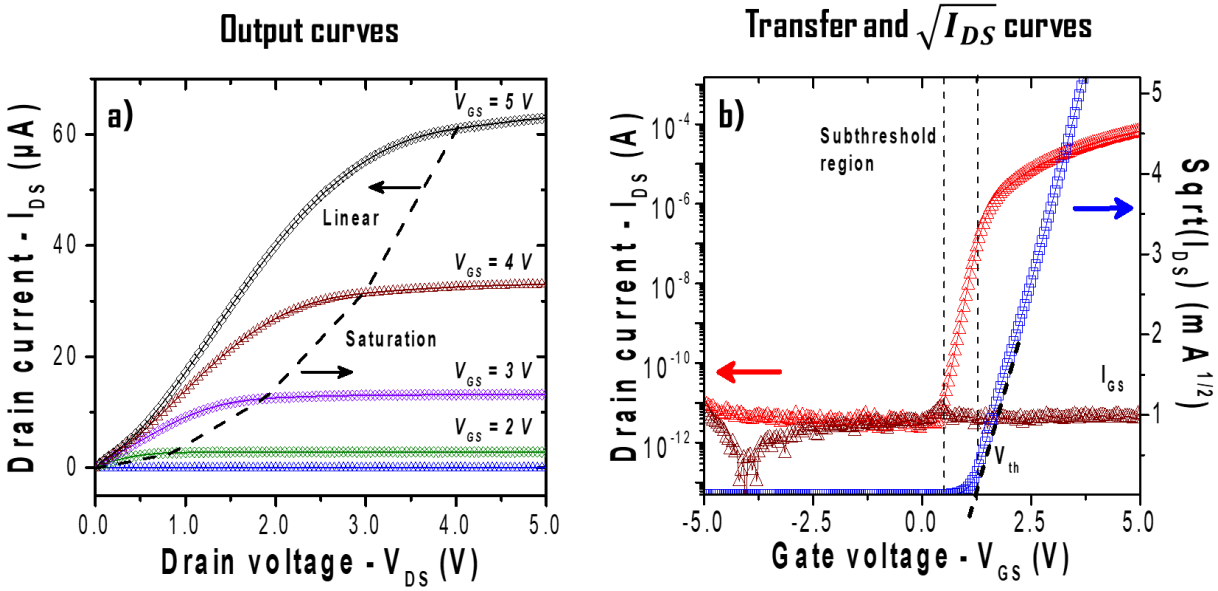

Figure 2.3. I-V curves a) the output curves display the I_{DS} while the V_{DS} sweeps from 0 to 5V and the V_{GS} increase in steps from 0 to 5 V. The two main operating regimes, linear and saturation are shown in this plot. The transfer and $I_{DS}^{1/2}$ curves are displayed in b). The I_{DS} is shown in red and the leakage current (I_{GS}) in dark red both in logarithmic scale. The subthreshold region is demonstrated between the dash lines. The $I_{DS}^{1/2}$ is displayed in blue with the extraction of the V_{th}.

On the other hand, the threshold voltage (V_{th}), saturation mobility (μ_{sat}) and subthreshold swing (SS) were calculated in the saturation regime ($V_{DS} \geq V_{GS} - V_{th}$). The SS is obtained from Equation 2.4, which defines the SS as the inverse of the maximum slope of the $\log_{10}(I_{DS})$ curve in the subthreshold region (Figure 2.3b).

$$SS = \frac{dV_{GS}}{d\log_{10}(I_{DS})} \qquad \text{Eq (2.4)}$$

Then, the V_{th} was extracted from the intercept of the linear fit of the $I_{DS}^{1/2}$ vs V_{GS} curve with the x-axis as is shown in Figure 2.3b. Similarly, the mobility is calculated from the slope of the $I_{DS}^{1/2}$ curve and Equation 2.5, where L and W are the length and width of the active channel and C_{ox} is the capacitance density of the HfO_2 layer.

$$\mu_{sat} = \frac{2L}{WC_{ox}}\left(\frac{d\sqrt{I_{DS}}}{dV_{GS}}\right)^2 \qquad \text{Eq (2.5)}$$

2.5 Electrical characterization of the HfO_2 MIM capacitors

The HfO_2 MIM capacitors were characterized using a Cascade Microtech probe station with a Keithley 4200-SCS semiconductor characterization system and HP/Agilent 4284A Precision LCR Meter under regular ambient conditions. The capacitance density (C_{ox}) and dielectric constant (k) were calculated from the capacitance-voltage (C-V) curve, using Equation 2.6**,** where ε_0 the vacuum permittivity, *t* is the thickness and A is the area of the dielectric layer. In addition, a capacitance vs frequency (C-F) measured was done to determine the frequency response of the dielectric layer. This measurement was obtained by applying a constant voltage (5 V) and measuring the capacitance while a sweep in frequency from 10 kHz to 10MHz is done. The breakdown voltage (V_B) was obtained from the abrupt increase of the leakage current against the increase in the voltage. In the same way, the time-to-breakdown was extracted by applying constant voltage stress, slightly lower than the $V_{B,}$ while the leakage current is being monitored. The time the dielectric layer takes to break is called the time-to-breakdown. This test was repeated several times to create an accurate time-dependent dielectric breakdown (TDDB) analysis.

$$C = \frac{\varepsilon_0 kA}{t} \qquad \text{Eq (2.6)}$$

CHAPTER 3

EFFECT OF ANNEALING ATMOSPHERE ON IGZO THIN FILM TRANSISTORS ON A DEFORMABLE SOFTENING POLYMER SUBSTRATE[1]

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[1]Adapted from *Semiconductor Science and Technology*, G. Gutierrez-Heredia, J. Maeng, J. Conde, O. Rodriguez-Lopez, and W. E. Voit, "Effect of annealing atmosphere on IGZO thin film transistors on a deformable softening polymer substrate," *Semicond. Sci. Technol.*, vol. 33, no. 9, p. 095001, Sep. 2018.

3.1 Introduction

Low-temperature electronics based on oxide semiconductors have been extensively studied due to their mobility higher than that of amorphous silicon (Si) semiconductor (~1cm^2 V^{-1} s^{-1}) and comparable to that of polycrystalline Si TFTs (10–100 cm^2 V^{-1} s^{-1}) for temperatures <300°C, as well as their process compatibility with flexible materials [1–3]. Recently, indium–gallium–zinc-oxide (IGZO) semiconductor has gained increasing attention as promising candidate for the active layer of thin-film transistors (TFTs) and active matrix circuit displays [4–7]. Besides the favorable characteristics including high mobility and performance stability, the wide band gap of IGZO has enabled this material to be exploited in transparent electronics [8–11]. Also, the implementation of transparent semiconductors on bendable substrates has been demonstrated for flexible electronics applications [12–16]. This kind of approach could be extended into more complex applications, such as implantable bioelectronics if the oxide semiconductor technology is applied on biocompatible materials and can achieve increased performance over acute and chronic time points.

Shape memory polymers (SMPs) are smart materials that can be deformed into a meta-stable shape and when triggered by an external stimulus (e.g., temperature, light, and fluid) can soften in modulus and return to their original shape [17–20]. Previously, a thiol-ene/acrylate based SMP was presented as a softening substrate for implantable applications [21–23]. This polymer can be engineered to have an onset of its glass transition temperature (T_g) when dry just above body temperature (37.5°C), so that it softens in the body upon exposure to fluids in vivo. This same class of SMPs has also been proposed as a platform substrate for semiconductor processing on which IGZO TFTs were fabricated with processing temperatures up to 250°C [24].

In this work, we systematically investigate the effect of annealing treatments on IGZO TFTs implemented on a thiol-ene/acrylate substrate and achieve record mobility up to 30 $cm^2 V^{-1} s^{-1}$ on SMPs. Different annealing atmospheres including oxygen, vacuum and forming gas are compared during annealing at 250°C. Conventional polymers used for flexible electronics may undergo irreversible deformation due to the thermal expansion and the associated thermal stress imposed by high-temperature fabrication processes. However, SMP utilized herein relaxes the thermal stress while cooling down to room temperature by returning to its original form owing to its memory properties. The electrical characteristics of the TFTs including mobility, threshold voltage (V_{th}), contact resistance (R_C) and channel conductivity associated with those annealing conditions are examined. In particular, the changes in contact resistance are correlated with other electrical parameters. This study provides a deeper insight into the impact of annealing on the junction contacts in IGZO-based TFTs implemented on a softening polymer using hafnium oxide as a dielectric and Au as the gate, source and drain metal.

3.2 Experimental

TFTs with a bottom-gate/top-contact configuration were fabricated on a glass slide (7.5 cm × 5cm), using the photolithographic processes schematically represented in Figure 3.1a. First, a thiol-ene/acrylate based SMP was synthesized and an SMP layer of 50 μm was coated on the glass slide, following established literature protocols [21–24]. Then, a 100 nm thick Au layer was deposited by e-beam evaporation and patterned as gate contact (Figure 3.1a-i). A hafnium oxide (HfO_2) layer of 30 nm was deposited as the gate dielectric by atomic layer deposition (ALD) at 100 °C, followed by a 40 nm thick IGZO layer deposited by an RF sputtering system at room temperature (Figure 3.1a-ii). The process conditions used for the IGZO deposition include a pre-vacuum of 10^{-8} Torr,

an O_2 flow rate of 12 sccm, a deposition pressure of 5 mTorr, and a sputtering power of 50 Watts. The distance from the target to the substrate was approximately 15 cm. Next, the semiconductor and dielectric films were patterned (Figure 3.1a-iii). Another 100 nm thick Au layer was deposited and patterned as the source–drain contacts (Figure 3.1a-iv). All metals layers were defined by a wet etch process in a dilute etchant such that the soak time was approximately 45 s. Afterwards, annealing treatments were conducted on different samples at 250°C under vacuum, oxygen or forming gas atmospheres. Forming gas atmosphere with 5% of Hydrogen is used to facilitate oxygen reduction in the exposed semiconductor as previously reported for oxide- semiconductor TFTs [25]. A schematic three-dimensional device structure and an optical image of a typical device as fabricated are shown in Figures 3.1b and c, respectively. Finally, the SMP substrate was released from the glass carrier (Figure 3.1d). TFTs with different dimensions (W = 10, 20, 40, 80/L = 5, 10, 20, 40 μm) were fabricated and characterized using a Keithley 4200 semiconductor characterization system under dark and regular ambient conditions. Metal-insulator-metal (MIM) capacitors with different dimensions (100×100, 100×200 and 200×200 μm^2) were also fabricated for dielectric constant characterization of the IGZO film.

3.3 Results and discussion

Figure 3.2a shows the electrical performance of the IGZO TFTs on SMP after an annealing treatment under forming gas at 250°C for 1 h. Drain-to-source current (I_{DS}), gate-to-source current (I_{GS}) and square-root-I_{DS} are plotted against gate-to-source voltage sweep (V_{GS}). I_{GS} appears in the range of $\sim 10^{-13}$ A, and similar behaviors are observed for all other IGZO TFTs on SMP (not shown). The I_{DS}–V_{GS} transfer curves of the as-fabricated IGZO TFTs (labeled as 'Original') without posterior annealing, along with the annealed devices under oxygen (O_2), vacuum (Vac)

and forming gas (FG) are shown in Figure 3.2b. In all cases, V_{GS} from −6 to +6 V was applied while keeping V_{DS} at +6 V. The maximum on-current (I_{ON}) decreases from ~10^{-7} (as-fabricated) to ~10^{-8} A after an annealing treatment under oxygen, while I_{ON} increases to 10^{-5} and 10^{-3} A under vacuum and forming gas, respectively. V_{th} of the TFTs was extracted from the intersection of the linear fit of the $I_{DS}^{1/2}$ versus V_{GS} curves as shown in Figure 3.2c. The field effect mobility (μ_{FE}) is extracted using the slope from the same fit using Equation (3.1) where C_{OX} is the capacitance density of the HfO_2 film whose dielectric constant is measured as 12 from the MIM capacitors. The extracted μ_{FE} and V_{th} for the as-fabricated devices are 10^{-2} $cm^2\,V^{-1}s^{-1}$ and 1.2 V, respectively. It is observed that the oxygen annealing reduces μ_{FE} to 10^{-3} $cm^2\,V^{-1}\,s^{-1}$ and increases V_{th} to 3 V. On the other hand, the forming gas annealing increases μ_{FE} to 30 $cm^2\,V^{-1}s^{-1}$ and decreases V_{th} to −0.6 V. These changes are attributed to the incorporation or reduction of oxygen in the IGZO film during the annealing treatments under oxygen or forming gas, respectively. Interestingly, the vacuum annealing also presents a significant improvement in electrical performance, resulting in μ_{FE} of 2 $cm^2V^{-1}s^{-1}$ and V_{th} of 0.4 V.

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{th})^2 \qquad \text{Eq (3.1)}$$

In addition, transfer curves of the IGZO TFTs on SMP with an applied voltage of V_{DS} = 0.1 V are obtained (Figure 3.2d). The I_{OFF} remains at ~10^{-13} A, as was the case for the forming gas annealing in Figure 3.2a, yet I_{ON} drops by about two orders of magnitude. In the case of oxygen annealing, there is a more significant drop in I_{ON} by approximately four orders of magnitude. This is likely due to the increase in IGZO film resistivity as previously reported [26–28].

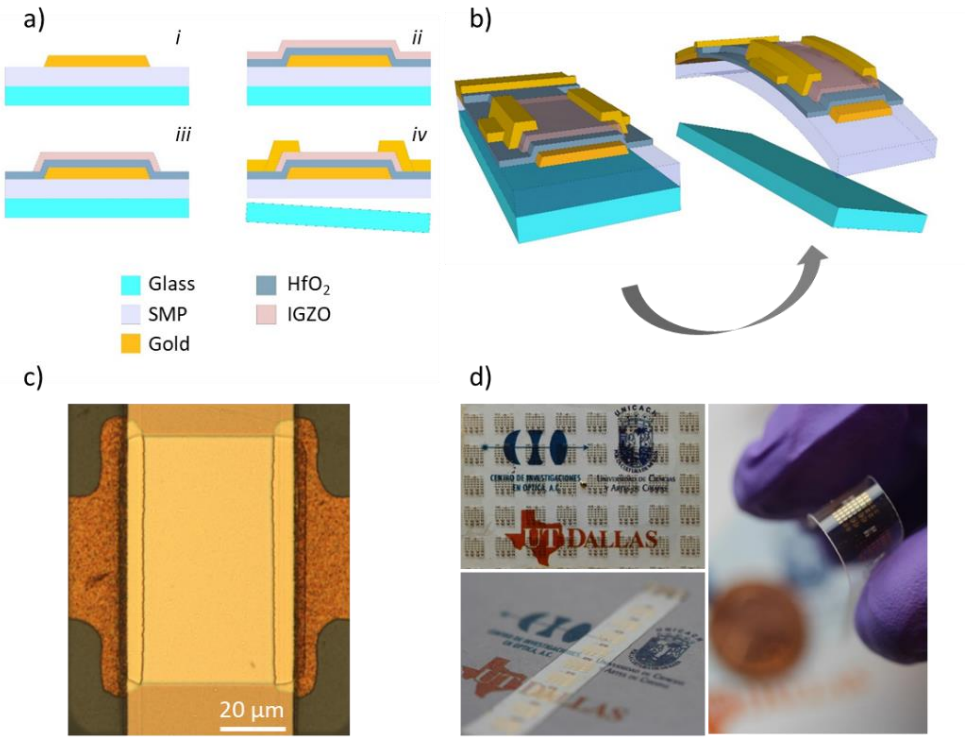

Figure 3.1. Fabrication of IGZO TFTs on SMP as a deformable softening substrate: a) fabrication process, b) 3D schematic images of the device before and after releasing, c) an optical microscopic image of a single IGZO TFT and d) optical images of the released devices on SMP in both flat and bent configurations.

Figure 3.3a presents the total resistance or the resistance between source and drain ($R_{SD} = R_C + R_{CH}$) obtained for the IGZO TFTs on SMP with vacuum annealing at different V_{GS}. Knowing I_{DS} values from each TFT, R_{SD} values can be extracted at different V_{GS}. In order to extract the contact resistance (R_C) at the IGZO-Au junction, an extrapolated linear fit is used where $2 \cdot R_C$ is extracted from the intersection at the y-axis of the R_{SD} versus channel length. R_C tends to decrease due to the carrier accumulation while V_{GS} increases. The changes in R_C are compared with their respective TFTs channel resistance (R_{CH}) in Figure 3.3b where $R_{CH} = R_{SD} - 2 \cdot R_C$. Here, the results from annealing in all various conditions are included. The as-fabricated devices notably

exhibit higher resistances than the devices processed with vacuum or forming gas annealing, by at least one and up to four orders of magnitude. In the case of TFTs with oxygen annealing, we were not able to obtain R_C due to the large resistance values and the noise in the measurements likely due to oxygen incorporation into the IGZO. These trends, i.e., improvement in the contact resistance under vacuum or forming gas annealing, yet deterioration under oxygen annealing, coincide with those observed from the changes in the device mobility. This suggests that the mobility can be strongly limited or influenced by the contact resistance as well as the annealing atmospheres. Another important point to note is that R_{CH} is higher than R_C for the untreated and the vacuum-treated devices. This indicates that the electrical performance of those TFTs is mainly limited by the semi- conductor resistance rather than by the junction resistance. On the other hand, R_{CH} appears to be lower than R_C for the forming gas treated devices. Similarly, this suggests that the forming gas annealing decreases the semiconductor resistance below the contact resistance and further improves the electrical performance of TFTs.

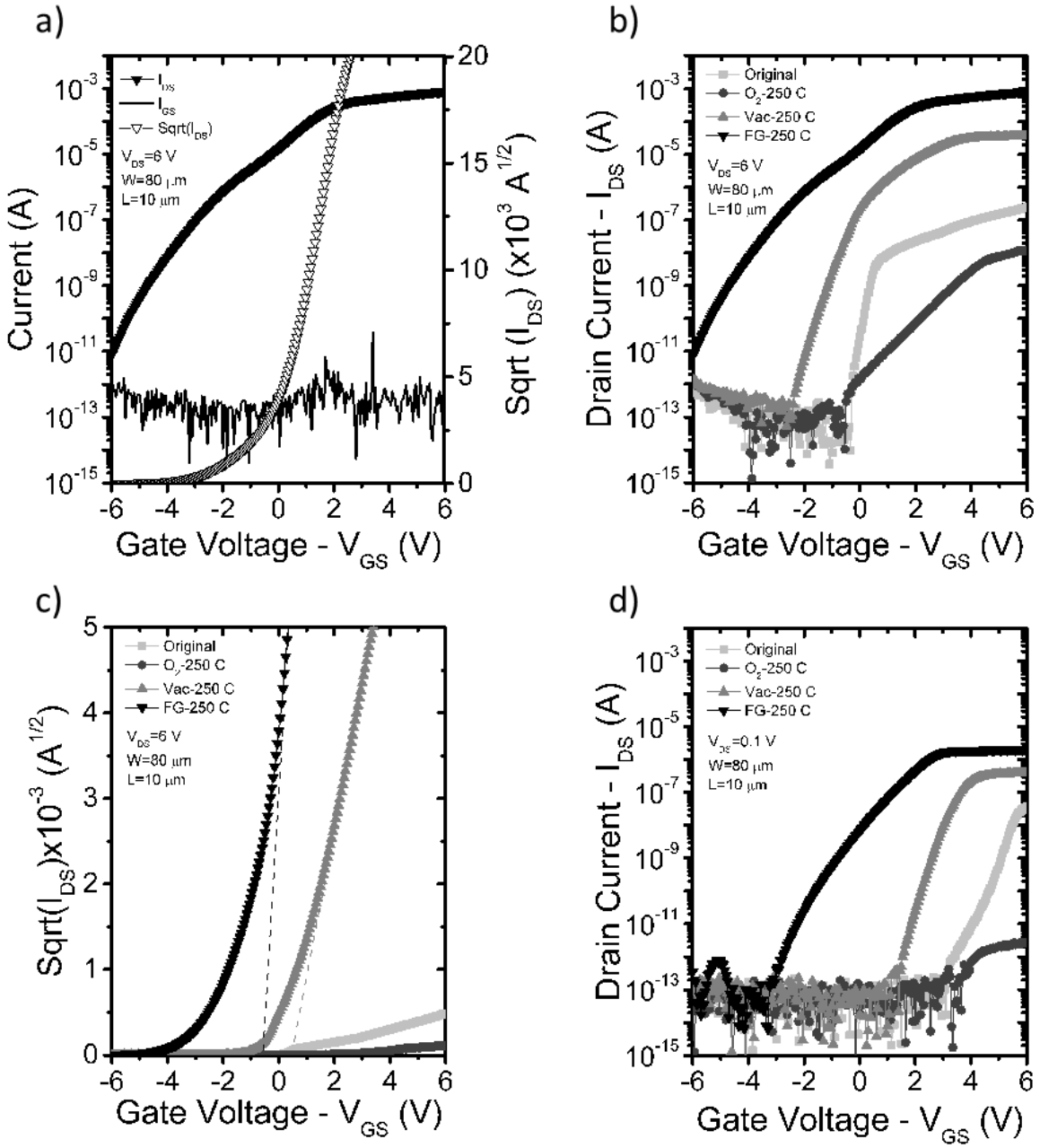

Figure 3.2. a) Transfer curves of IGZO TFTs on SMP after an annealing treatment under forming gas at 250°C where drain (I_{DS}) and gate current (I_{GS}) are shown. The square root (Sqrt) of the drain current was used for the extraction of mobility and threshold voltage (V_{th}). b) Transfer curves in saturation regime, c) Sqrt (I_{DS}) and d) transfer curves in linear regime for the TFTs as fabricated and after annealing treatments under oxygen (O_2), vacuum (Vac) and forming gas (FG) at 250°C.

The electrical performance of the TFTs with different channel lengths is also characterized with regard to different post-annealing treatments. The average mobility and V_{th} obtained for these devices are presented in Figures 3.4a and b, respectively. The TFTs with the forming gas treatment achieve the highest mobility with average values ranging from 20 to 40 $cm^2\ V^{-1}\ s^{-1}$. Lower mobility values of 1–5, 1–7 × 10^{-2} and 4–13 × 10^{-4} $cm^2\ V^{-1}\ s^{-1}$ are obtained for the vacuum-treated, untreated and oxygen-treated devices, respectively. In each group of samples, the mobility values exhibit relatively small variations along the different channel lengths within the same order of magnitude, indicating the smaller influence of the channel dimension than that of the annealing atmosphere. The small variations can be related with the properties of R_C and R_{CH}. For example, the FG condition which is the only case where the $R_C > R_{CH}$ (Figure 3.3b) shows the trend of slight increase in mobility with the channel length reduction (Figure 3.4a). Similarly, the variations in V_{th} along the different channel lengths appear insignificant in each group of samples with different annealing treatments. On the other hand, relatively large variations in V_{th}, up to ~5 V, are observed among the devices with different annealing treatments. This can be attributed to the defects or traps formed in the film bulk and at the semiconductor-dielectric interface as previously reported [29–32]. Despite the significant improvement in mobility and maximum I_{DS} achieved by forming gas annealing, other changes such as negative shift in V_{th} and increase in subthreshold swing also occur during the same treatment. Therefore, care must be taken in choosing the annealing condition based on one's necessity. Also, the annealing treatment using FG added a kink in the subthreshold region of the I_{DS}. A similar behavior was previously reported due to water absorption at the gate dielectric and reduced by using treatments above 600°C [33]. Future work will be required to reduce this unfavorable effect.

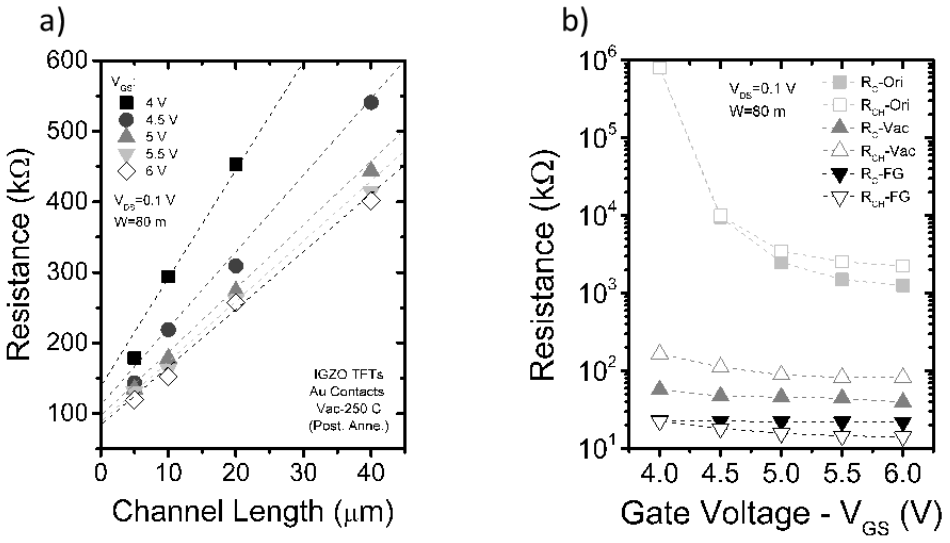

Figure 3.3. a) Linear fit of the total resistance for the vacuum-annealed (250°C) IGZO TFTs (W = 80 μm and V_{GS} = 0.1 V) with different channel length dimensions and voltages for the extraction of contact (R_C) and channel resistance (R_{CH}). b) Comparison of R_C and R_{CH} for the IGZO TFTs on SMP.

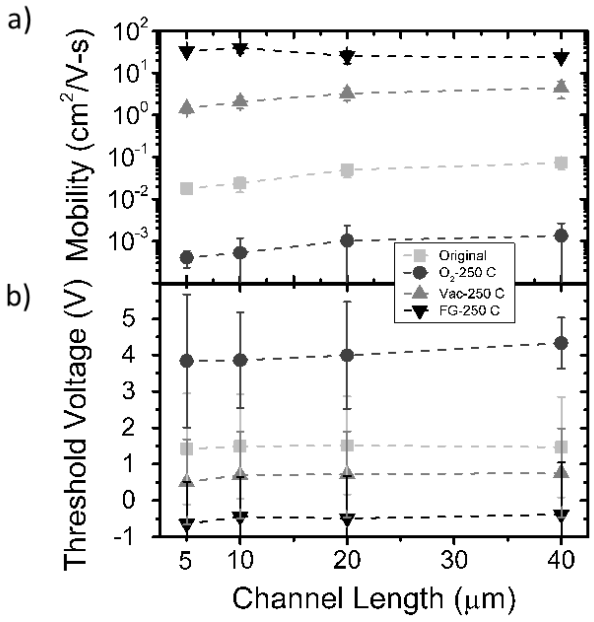

Figure 3.4. Average a) mobility and b) V_{th} of the IGZO TFTs on SMP as fabricated and after annealing treatments under oxygen (O_2), vacuum (Vac) and forming gas (FG) at 250°C.

3.4 Conclusions

A systematic study on the effect of annealing atmosphere on TFTs with unconventional IGZO-Au junction contacts fabricated on a deformable softening polymer has been carried out. Annealing treatments under different conditions including ambient air, oxygen, vacuum, and forming gas, are employed and the changes in the electrical characteristics of these TFTs are examined. The device mobility varies in the range of 10^{-3}–10^{1} cm^2 V^{-1} s^{-1} depending on the annealing atmosphere. With a forming gas treatment at 250°C, a maximum μ_{FE} of 30 cm^2 V^{-1} s^{-1} is achieved which is an improvement by nearly 300 times from that of the untreated devices. The threshold voltage of these devices vary within −0.5 to 3.9 V depending on the annealing atmosphere. The analyses on the R_{CH} and R_C show the interplay between the semiconductor resistance and the semiconductor–metal con- tact resistance in determining the electrical performance of the TFTs. These results provide myriad possibilities for achieving various designs of electronic circuitries with different electrical behaviors on biocompatible substrates such as the softening SMP demonstrated herein. The annealing methods used for the IGZO-Au junction herein can also be applied to different metals and the respective metal–semiconductor interfaces. As these TFT technologies scale to complex flexible and bioelectronic applications, chronic electrical and mechanical stability and packaging must be carefully considered for an emerging generation of smart devices to serve as useful research tools, medical devices and functional consumer products.

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CHAPTER 4

LIFETIME OF HAFNIUM OXIDE DIELECTRIC IN THIN-FILM DEVICES FABRICATED ON DEFORMABLE SOFTENING POLYMER SUBSTRATE[2]

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[2]Adapted from *Materials Science in Semiconductors Process*, G. Gutierrez-Heredia *et al.*, "Lifetime of hafnium oxide dielectric in thin-film devices fabricated on deformable softening polymer substrate," *Mater. Sci. Semicond. Process.*, vol. 88, no. July, pp. 273–277, Dec. 2018.

4.1 Introduction

The technology of low-temperature processing semiconductors has enabled the development of electronic devices on top of flexible substrates such as plastics and polymers [1–4]. This has received much attention in recent years due to the huge potential applications in medical devices, flexible displays and self-powered circuits among others [5–9]. However, the electrical instability of flexible electronic devices has become an issue for the development of reliable applications. There are different studies which focus on thin-film transistors (TFTs) as the basic unit for future complex circuits and on the improvement of its threshold voltage (V_{th}) stability [10–12]. On the other hand, time-dependent dielectric breakdown (TDDB) technique is a well- known characterization method to predict dielectric lifetime by applying different voltage ranges (or electric fields) to a dielectric layer (or capacitor). This characterization is also used to define the operation ranges for electronic circuits, and it is commonly used for single-crystalline silicon (Si) technology, which is incompatible with flexible substrates [13–15]. In this work, we present the electrical stability and lifetime of hafnium oxide (HfO_2) dielectric on top of softening thiol-ene/acrylate- based shape memory polymer (SMP) as flexible substrate, which has the ability to remember a programmed shape after deformation and then to return to its original form when an external stimulus is applied [16–19]. As previously reported, this activation by stimulus, such as temperature, humidity, light or a combination of these can drop the polymer storage modulus from the order of GPa to MPa [20–22]. Because of the change in the storage modulus, this softening polymer is compatible with the paradigm “stiff for insertion and soft chronically,” useful for a broad class of implantable bioelectronic applications.

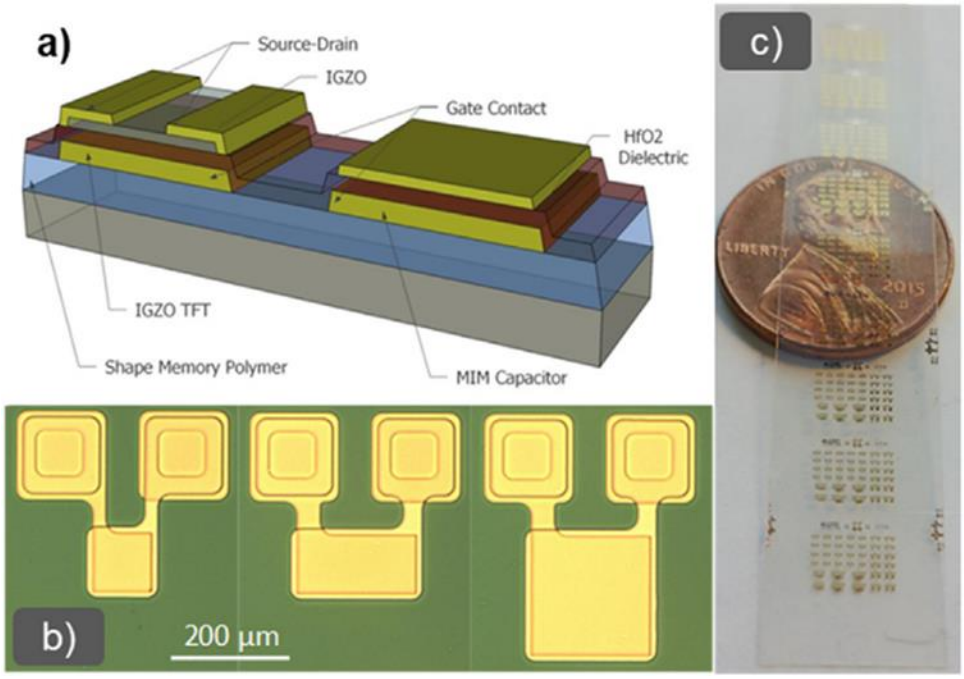

Figure 4.1. a) 3D diagram of Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistors (TFTs) and metal-insulator-metal (MIM) capacitors. b) Optical micrographs of the fabricated MIM capacitors (100×100, 100×200 and 200×200 µm) using 50 nm of hafnium oxide as insulator. c) Optical image of the thin-film devices on top of the shape memory polymer (SMP) based on thiol-ene/acrylate, as softening substrate, after being cut and released from the glass carrier.

To our knowledge, this is the first time an electrical reliability analysis of de- vices based on High-K dielectric, more specifically HfO_2, have been reported on a softening polymer as substrate. Also, this SMP has shown resilience through photolithography and aggressive fabrication processes reaching temperatures up to 250°C without significant mass loss [23]. The HfO_2 was deposited by atomic layer deposition (ALD) to fabricate metal-insulator-metal (MIM) capacitors and indium-gallium- zinc oxide (IGZO) TFTs on top of SMP as shown with the 3D structure in Figure 4.1a. The lifetime of the HfO_2 was obtained by analyzing the TDDB of the fabricated capacitors with different dimensions (Figure 4.1b).

4.2 Experimental

All the steps for SMP synthesis were performed in a fume hood using, as previously reported: 1, 3, 5 Triallyl 1, 3, 5-triazine-2, 4, 6(1 H, 3 H, 5 H)-trione (TATATO), Tricyclo [5.2.1.02, 6] decanedimethanol-diacrylate (TCMDA), Tris [2-(mercaptopropionyloxy)ethyl]isocyanurate (TMICN) and 2, 2-Dimethoxy-2-phenyl-acetophenone (DMPA) [22]. The obtained polymer on a glass slide (5×7.5 cm) was 50 µm thick. The SMP roughness obtained by an atomic force microscopy (AFM) Veeco (Dimension 5000) was of R_a = 0.19 nm (Figure 4.2a). Then, the MIM capacitors and IGZO TFTs were fabricated on top of the SMP substrate without any posterior treatment or passivation layer as previously reported [23]. The device fabrication was carried out using photolithographic processes, as well as wet and dry etch. A gold layer, deposited by thermal evaporator, of 100 nm was used for bottom contact (Gate) and another as top contact (Drain/Source). For both devices 50 nm of HfO_2 by ALD at 100°C was deposited, sharing the same gate dielectric. A tetrakis(dimethylamido) precursor was used for hafnium and DIW for the oxidation. The HfO_2 thickness was measured by ellipsometry and cross-section SEM (Figure 4.2b). An RF sputtering and a In:Ga:Zn:O=1:1:1:4 target were used for the semiconductor deposition at room temperature. During the entire fabrication process, the devices were exposed to a maximum temperature of 100°C with a posterior annealing of 200°C for one hour (in forming gas, 5% H_2) after fabrication. Posteriorly, the SMP substrate was cut and released as shown in Figure 4.1c. A cascade probe-station with a Keithley 4200 and HP/Agilent 4284A Precision LCR Meter instrument were used for the electrical characterization of the capacitors and TFTs.

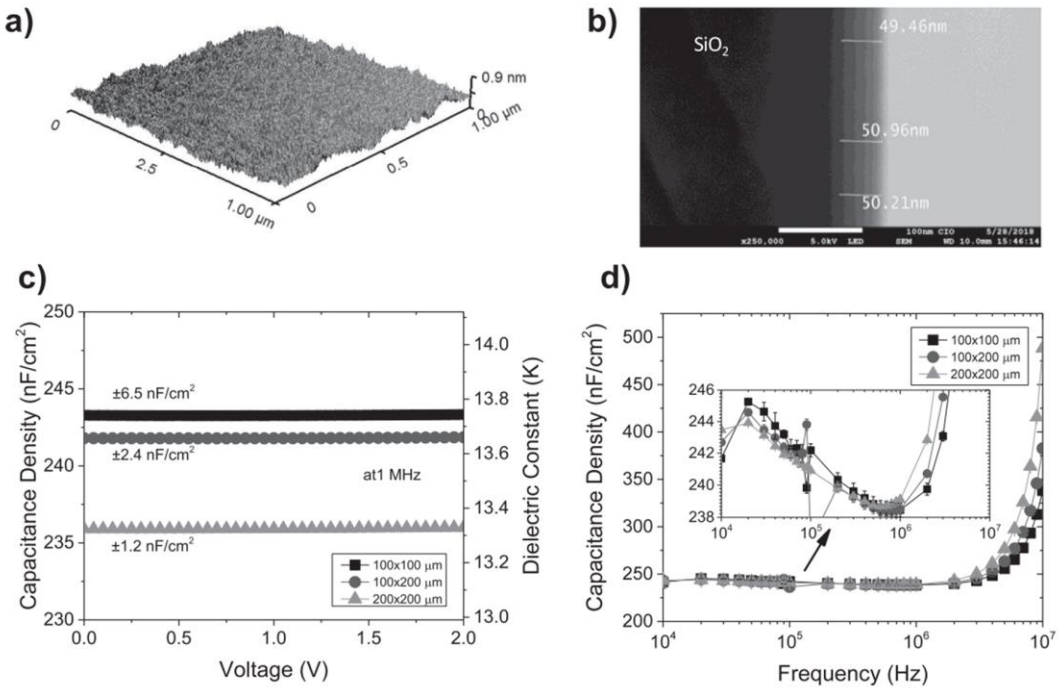

Figure 4.2. a) Atomic force microscopy (AFM) used to measure the SMP roughness (R_a = 0.19 nm). b) Cross-section scanning electron microscopy (SEM) of HfO_2 (50 nm) on Si/SiO_2 wafer. Analysis of the average capacitance density analysis using c) voltage sweep @1MHz and d) frequency sweep at 5 V, using twelve MIM capacitors with 50 nm HfO_2 on top of SMP substrate.

4.3 Results and discussion

Electrical characterization of the metal-insulator-metal (MIM) capacitors with dimensions of 100×100, 100×200 and 200×200 µm was performed before the TFTs analysis. From the capacitance-voltage (C-V) characterization and using Equation (4.1) where ε_0 is the vacuum permittivity, k the dielectric constant, A and t are the area and thickness of the capacitor, a dielectric constant of around 13.6 was obtained (Figure 4.2c).

$$C = \varepsilon_0 kA/t \qquad \text{Eq (4.1)}$$

Besides the closeness of the capacitance density/dielectric constant (k) values among the different dimensions, a clear downward trend in capacitance density was observed for larger capacitor dimensions, going from 243 ± 6.5–241 ± 2.4 and 236 ± 1.2 nF/cm^2 (k value of 13.74, 13.66 and 13.34, respectively). Similarly, during the C-V characterization, it was observed by sweeping the frequency (Figure 4.2d) that there is a dependence between electrical responses and capacitor dimensions. The variation between the capacitance density/dielectric constant can be related to insignificant changes in the dielectric thickness or quality. This effect was observed despite the good uniformity presented of the HfO_2 by ALD (inset of Figure 4.2a). However, this effect will be discussed later in this work. This behavior was observed in different regions across the sample by measuring 12 capacitors. A brief analysis of the IGZO TFTs also presents a trend with different channel width (W) and length (L) dimensions (W = 40, L = 20, 30, 40, 50 µm) is presented in Figure 3a. The electrical characterization of the IGZO TFTs with field effect mobility (μ_{FE}) and V_{th} values, was obtained using electrical measurements from transfer curves (Figure 4.3d) and Equation (4.2) where I_{DS} is the drain current, C_{OX} the capacitance density and V_{GS} the voltage applied between gate and source electrodes.

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{th})^2 \qquad \text{Eq (4.2)}$$

A stable behavior was observed for the V_{th} in all cases at around 0.8 V. On the other hand, the mobility values decrease as the channel dimensions increase from 18.26 to 17.72, 17.19 and 17.17 cm2 V-1s-1, for TFTs channel L of 20, 30, 40, 50 µm, respectively (Figure 4.3b). We cannot assume that the change in mobility is due to the obtained capacitance variation, which is inversely proportional (Equation (4.2)), without a more complete study about TFTs. However, by comparing

the performance between the TFTs, with normalized channel current in Figure 4.3c, the difference be- tween the current obtained could be due to a slight improvement of the IGZO-HfO_2 stack. In the same way, this mobility variation presented a similar trend of improving the device characteristics with the reduction of device dimensions. The average leakage current density of another 12 capacitors was also extracted, 4 for each different dimension as shown in Fig. 4a. A voltage sweeps from 0 to 35 V exhibits how the leakage current started to increase and continued into the breakdown region from 22.5, 25 and 27.5 V for the capacitor dimensions of 200×200, 100×200 and 100×100 µm, respectively. Also, stress tests by applying and keeping different voltages (26, 28, 30 and 32 V) vs. time was extracted. Figure 4.4b presents the current density vs. time of three fabricated capacitors, where the devices with an applied voltage of 26 V lasted around 400, 100 and 70 s, respectively for smaller to larger dimensions. The inset presents a broken capacitor during the current vs. time test. A time dependent dielectric breakdown (TDDB) analysis was obtained from 48 capacitors with different dimensions and applied voltages (4 devices for each condition). The results also show a slight trend to increase the device lifetime by decreasing its dimensions. Fig. 4c shows the trend of the HfO_2 dielectric or the capacitors to last a predicted 10 years by using an operational range below 5 V. Therefore, the lifetime of TFTs dielectric should be subject to the same voltage operational range. However, TFTs are also subject to different defect generation, especially from the semiconductor. A clear dependence is observed by analyzing the same devices vs. the dimensional area in Figure 4.4d. A similar dependence of the lifetime and area of the capacitors was previously reported by Kim et al. for HfO_2 on silicon substrate, correlating this effect with the Weibull distribution [13]. On the other hand, in 2002 Park et al. reported the fabrication of MIM capacitors using Ta_2O_5 on top of a flexible polymer with an

estimation of 10 years of lifetime by using below 3.2 MV/cm (< 24 V for 75 nm) [24]. However, it is difficult to make a direct comparison of the present work with others due to the differences of dielectric material, deposition technique, temperatures used, among others. Nevertheless, HfO_2 on silicon substrate by CVD (chemical vapor deposition) has been reported with the same lifetime for higher electric field ranges up to 17 MV/cm (1.88 V and 1.06 nm) when using 500°C [14]. Contrasting to single-crystal silicon technologies where the roughness is a very controlled parameter and plays an important role in the device's electrical performance, large area and flexible electronics technologies are more prone to be affected by any defect on the substrate surface. Besides the roughness previously reported by the SMP of 0.18 nm and the uniformity presented by ALD films, the processes used posteriorly to the fabrication such as adding an encapsulation layer, substrate releasing (or bending processes during the releasing) and thermal annealing, which deforms the polymer due to it thermal expansion coefficient; can deform the mechanical structure of the SMP and change the gate dielectric characteristics.

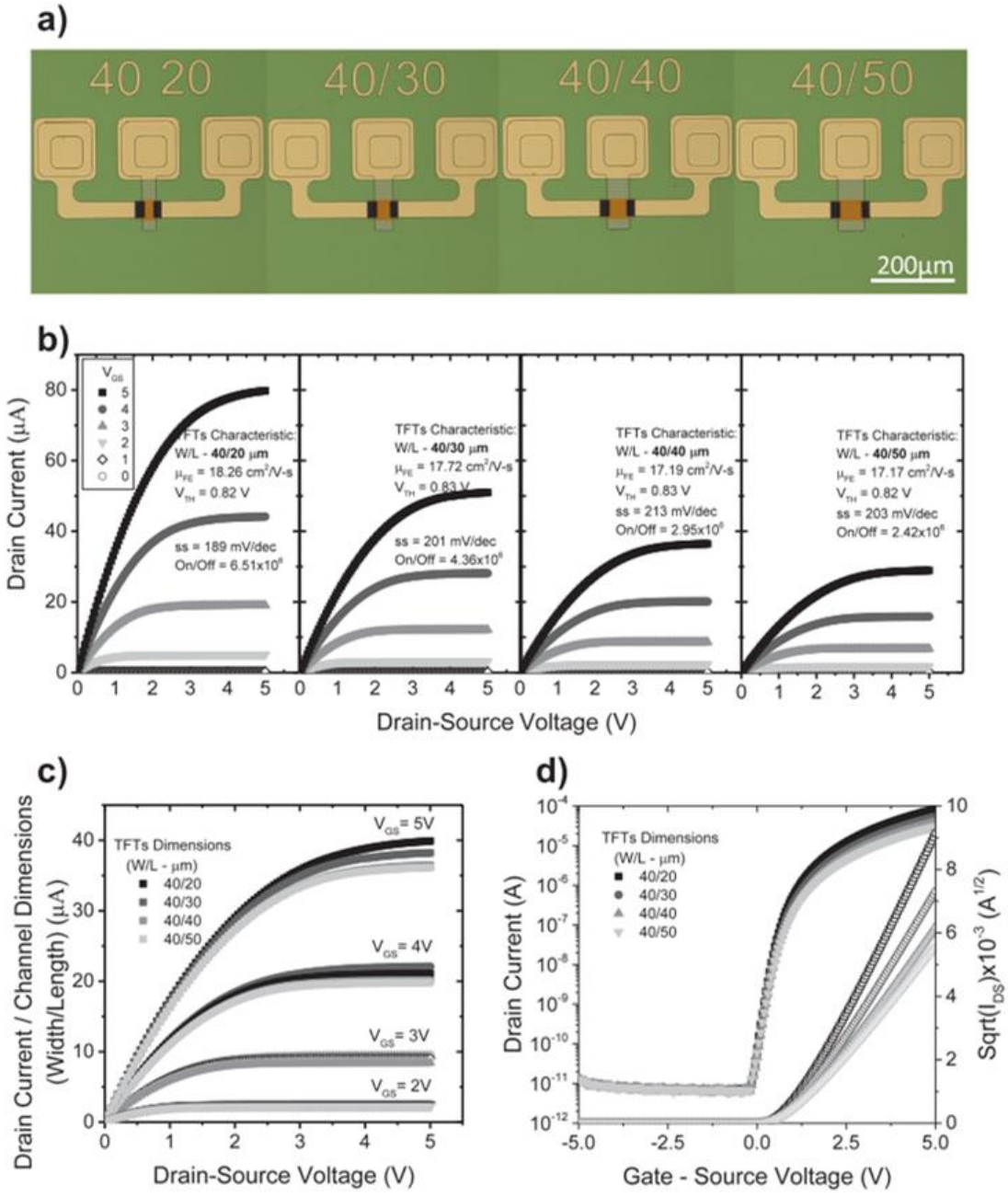

Figure 4.3. a) Optical micrographs of the fabricated IGZO TFTs using 50 nm of HfO_2 as gate dielectric. Electrical comparison of four IGZO TFTs with 50 nm of HfO_2 as gate dielectric and fabricated on SMP substrate. b) Output curves these devices with different channel dimensions (W = 40/L = 20, 30, 40, 50 µm), c) Normalized output curves and d) transfer curves of the same devices.

Unlike other polymers that can be deformed by their thermal expansion and keep that new form, the SMP is constantly deformed during the fabrication process since returns to its original form due to its memory properties. This effect also gives the advantage of being a deformable-free substrate. Therefore, the electrical performance of a device has more possibilities to be affected by any defect with larger area dimensions. Another factor which can affects the performance in these technologies is the quality growth of the HfO_2, and possibly other high-k dielectrics, on top of polymer substrates. In the same way, this study can pave the way for future research of flexible electronics using the combination of electrical and mechanical stresses.

4.4 Conclusions

As we presented in this work, a dependence between devices dimensions using HfO_2 dielectric on top of softening polymer substrate was analyzed. The observed trends suggest a variation in the dielectric thickness or quality on top of this polymer. Both thin-film devices (capacitors and transistors) were fabricated using 50 nm of HfO_2 on top of 200 nm of Au as bottom gate contact. The instability shown by the TFTs mobility in other reports, as well as this one (17.43 ± 0.55 cm^2/Vs), fits with the instability also found in work by the MIM capacitors dielectric constant (13.6 ± 0.2). Unlike crystalline-silicon technology where the HfO_2 is deposited on top of SiO_2 surface, here we are fabricating thin-film devices with high-k dielectric on top of polymer which can influence the film deposition. This electrical variation of these devices should be considered for posterior circuit designs to decrease instability for electronic applications using HfO_2 films on top of polymer substrates. In the same way, this can help to improve the performance in complex applications combining the electrical stability and flexible electronics technologies.

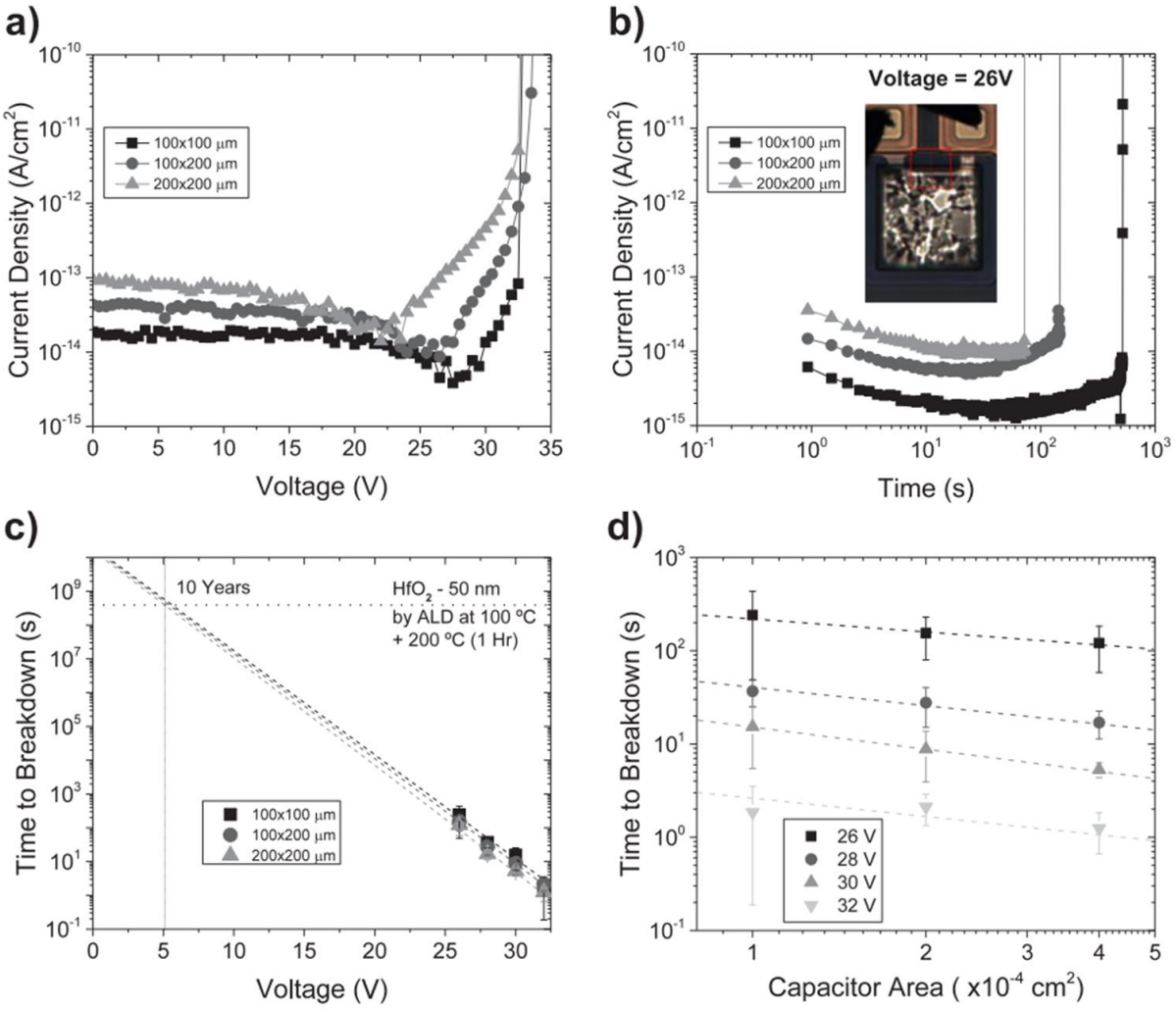

Figure 4.4. a) Average current density using twelve MIM capacitors with 50 nm of HfO_2. b) Current density analysis with fixed voltage at 26 V vs time until dielectric breakdown and optical micrograph of a 200×200 µm MIM capacitor after breakdown (inset). c) Time dependent dielectric breakdown (TDDB) analysis of HfO_2 layer by using 48 MIM capacitors. An estimated dielectric lifetime of 10 years by using a maximum voltage of 5 V. d) Time to breakdown of the same devices vs. capacitor area which shows a clear trend to decrease for larger dimensions.

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CHAPTER 5

HIGHLY STABLE INDIUM-GALLIUM-ZINC-OXIDE THIN-FILM TRANSISTORS ON DEFORMABLE SOFTENING POLYMER SUBSTRATES[3]

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5.1 Introduction

High performance, reliability, and stable behavior are important requirements for flexible electronics in order to meet the rigorous demands of technologies such as solar cells, flexible displays, radio frequency identification (RF-ID) tags, and more recently a host of emerging biomedical applications [1–5]. Biomedical applications such as neural interfaces can take advantage of flexible electronic devices, such as thin film transistors (TFTs) fabricated on biocompatible and flexible substrates, for in vivo multichannel stimulation and recording nervous system activity [6–8]. Such devices can lead the way for soft and more complex applications that more closely mimic the behavior and size scale of biology. To these ends, bioelectronic devices must demonstrate several critical features: be manufacturable via a repeatable fabrication processes; exhibit resistance to mechanical deformation; and demonstrate electrical reliability. Technologies based on TFTs allowed the microfabrication of large-area applications such as flat-panel displays, which were difficult to develop on flexible substrates due to their high temperature processing requirements and were difficult to develop on silicon due to the cost associated with using such a large area of silicon. After Nomura et al. presented TFTs based on indium-gallium-zinc-oxide (IGZO) semiconductors, these became the key component for the fabrication of system-on-glass applications [9]. The electrical performance of IGZO TFTs exhibited high-mobility values (>10 cm2 $V^{-1}s^{-1}$) compared with organic semiconductors (<0.1 cm^2 $V^{-1}s^{-1}$) or amorphous silicon (≈1 cm^2 $V^{-1}s^{-1}$) [9–11]. More recently, IGZO has been reported with mobility values of 29 cm^2 $V^{-1}s^{-1}$ by Jeon et al. to develop a voltage compensation circuit [12]. A transparent circuit based on IGZO TFTs with mobility of 70 cm^2 V^{-1} s^{-1} was presented by Liu et al. with frequency response on the order of megahertz [13]. In addition, Liu et al. incorporated silver nanowires into IGZO to

achieve a mobility of 174 $cm^2\ V^{-1}\ s^{-1}$ [14] but with limits on processing and scalability. Due to their relative low processing temperature requirements (compared with silicon technologies) and high mobility, semiconductor devices made from IGZO allow for the development of emerging technologies such as flexible and wearable electronics: active-matrix phosphorescent organic light emitting diodes displays by O'Brien et al. [15] an amplifier by Münzenrieder et al. [16] and a full color organic light-emitting diodes (OLED)-based display [4] among others. There is a tradeoff among the various processing temperatures used during TFT fabrication, which affects electrical performance and the thermal compatibility with flexible substrates. Important performance characteristics of the electronic components include field effect mobility (μ_{FE}), threshold voltage (V_{th}), changes in V_{th} (ΔV_{th}), and subthreshold swing (SS). The use of elevated temperature during device processing can help improve the quality of amorphous IGZO, as well as its interface with a dielectric. According to Nomura, TFT device simulations revealed that deep acceptor-type traps govern ΔV_{th} for annealed TFTs, while an increase in shallow trap states causes the deterioration of the SS [17]. The use of high temperatures and annealing treatments to increase the TFTs' mobility values have been well studied both by leading device companies and electronics research groups [17–21]. More importantly, annealing treatments can increase the device reliability in terms of stability and lifetime by decreasing the interfacial defects (e.g., deep and shallow trap states, and dangling bonds), which is one of the major requirements for achieving chronically implantable biomedical devices. In the past, TFTs have been fabricated on flexible substrates such as poly(ethylene naphthalate) (PEN), poly(ethylene terephthalate) (PET), or various polyimides presenting mobilities above 10 $cm^2\ V^{-1}s^{-1}$.[15,16,22,23] The major concern regarding PEN and PET substrates is the lack of compatibility with temperatures above 150°C, which tends to degrade

these materials or to cause anisotropic mechanical deformation due to coefficient of thermal expansion mismatches. Studies have demonstrated annealing of IGZO on polyimide materials such as Kapton at temperatures above 250°C [24–26]. However, thermal expansion, large strain mismatch at the interface, and anisotropic polymerization stresses that are relieved as a function of thermal cycling often lead to delamination and the inability to build large area devices [27]. We present flexible substrates that can withstand temperatures up to 250°C without substrate degradation and with limited thermally induced, anisotropic mechanical deformation: traits necessary for the next generation of flexible electronics applications. Beyond their mechanical and thermal stability against degradation, deformation and breakdown, thermoset thiol-ene/acrylate shape memory polymers (SMPs) have the capacity to return to their original shape after deformation into a metastable shape, by taking them to temperatures above their glass transition [28–30]. Substrates based on SMPs self-adjust and soften to enable applications that require engineered materials in very specific temperature ranges [28–32]. Also, SMPs have been previously used in biomedical applications wherein they present a high stiffness at room temperature, while having the ability to soften in vivo upon heating and absorption of small amounts of water [30, 33]. Similarly, microfabrication of TFTs on SMPs has been demonstrated, with minor degradation of electrical performance after multiple mechanical bending cycles [7, 34]. The electrical performance of IGZO TFTs on SMP substrates with processing temperatures up to 250°C is presented in this work. These results demonstrate operation at low voltages and high currents, exhibiting electrical stability, as well as dimensional permanency, which allows microfabrication of larger circuits, mechanical bending resilience, and stable operation in aqueous environments. A statistical analysis of several TFTs' performance helped investigate the reduction

of traps at the interface and dielectric bulk due to annealing treatment after fabrication. Also, multiple bending cycles (up to 104 cycles in 4 h) were carried out to track the electrical behavior of the fabricated devices subjected to such fatigue via accelerated mechanical deformation. Other SMP substrates containing IGZO TFTs were soaked in phosphate-buffered saline (PBS) solution at 37°C for 1 week, in order to track changes in their electrical behavior. Devices that did not shunt due to fabrication defects, exhibited excellent dimensional stability, and low voltage operation. In this paradigm, we fabricated logic inverter circuits using IGZO TFTs on SMPs and characterized them in bent and aqueous conditions. The TFT fabrication was carried out using IGZO as the semiconductor, hafnium oxide (HfO_2) as a thin film dielectric and gold (Au) as electrodes, in a bottom gate/top contact configuration as shown in the 3D model/cross-section and top view (Figure 5.1a, b). Logic inverter circuits were also included in the design using two TFTs in an active load configuration (Figure 5.1c). Since the primary goal of this work is the stability and reliability analysis of the fabricated TFTs on SMPs compatible with high temperature annealing processes, one device of each combination varying the TFT's channel width (W) (80, 40, 20, and 10 µm) and length (L) (40, 20, 10, and 5 µm) was used to achieve statistical significance. A 50 µm thick SMP film (on top of a glass slide as carrier substrate) enables the TFT fabrication before release from the carrier glass substrate, as shown in Figure 5.1d. The shape memory properties of the substrate enable fixing into temporary metastable shapes. After a thermal ramp to a temperature above the glass transition temperature (T_g) of the substrate, the polymer softens and can be molded into a 3D shape. The polymer will maintain its deformed shape after the temperature is subsequently decreased below its T_g.

5.2 Experimental

Prior to the device fabrication, the synthesis of SMP as substrate was performed. Tricyclodecane dimethanol diacrylate (TCMDA), 1,3,5-triallyl- 1,3,5-triazine-2,4,6(1H,3H,5H)-trione (TATATO), and 2,2-dimethoxy- 2-phenyl acetophenone (DMPA) were purchased from Sigma-Aldrich. Tris[2-(3-mercaptopropionyloxy)ethyl] isocyanurate (TMICN) was purchased from Wako Chemicals. All chemicals were used as received. Composition of SMP consisted of 34.5 mol% TATATO and TMICN, 31 mol% TCMDA and 0.1 mol% DMPA. Monomer solution was spun at 650 rpm for 1 min on a glass slide (7.5×5 cm^2) to form a 50 μm thick layer of SMP. For the polymerization process, SMP samples were treated in a 254 nm UV-light chamber for 2 min, followed by a crosslinking chamber with five overhead 365 nm UV bulbs (UVP via Cole-Parmer) for 60 min. Finally, a post-curing process at 110°C in a vacuum oven was used for 18 h.

Dynamic mechanical analysis (DMA) was performed using a TA Instrument RSA-G2. Samples were cut with a CO_2 laser into rectangular shapes with dimensions of 4.5×45 mm for width and height, respectively. Deformation mode was uniaxial in tension by using a strain of 0.275% and 0.05 N as load. Samples were tested both in dry and wet conditions at 37°C (isothermal). Test in wet conditions was possible by using an immersion bath full of PBS with a pH of 7.2, simulating in vivo conditions. Samples were presoaked in PBS for 24 h prior to test. The frequency of deformation was 1 Hz. Glass transition temperature (T_g) is denoted by the peak of tan delta. TGA was performed using a Mettler Toledo TGA/DSC1 in alumina crucibles. Samples were ≈7 mg and were heated from 25 to 70°C, using a heating rate of 20 °C min^{-1}.

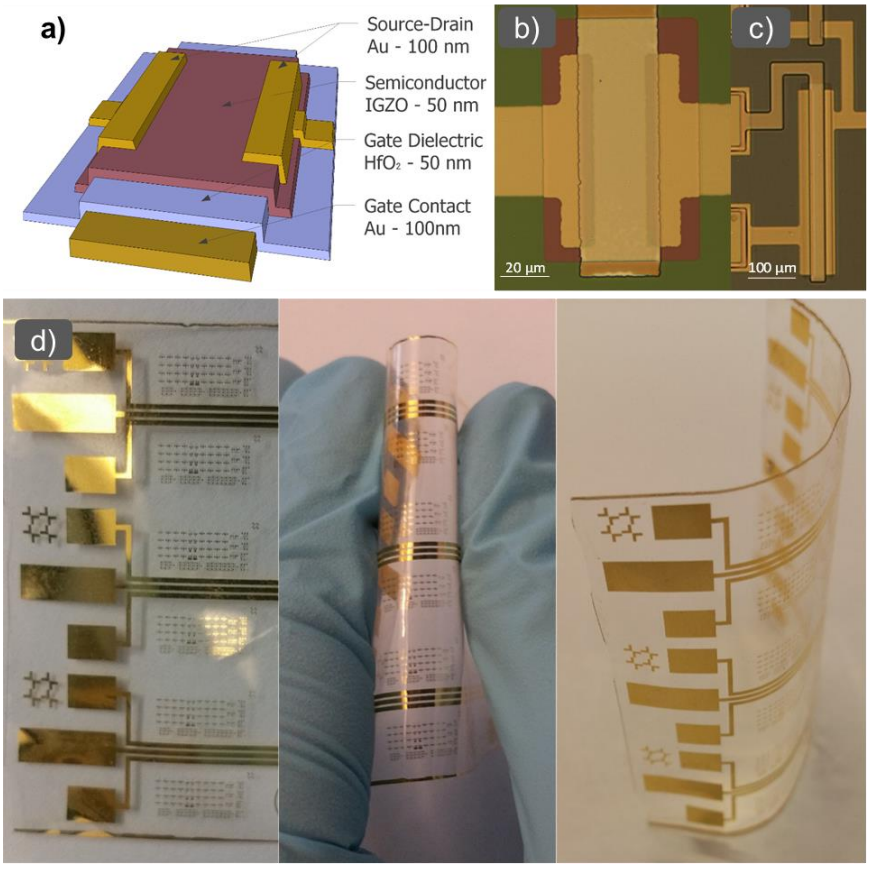

Figure 5.1. Indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) shown as a) a 3D diagram and in optical microscopy images of b) a single IGZO TFT and c) a logic inverter circuit using two IGZO TFTs. d) Optical images highlight the thiol-ene-based shape memory polymer (SMP) substrate as it is fixed into a meta-stable shape by applying mechanical deformation and temperature cycle.

For TFT fabrication, a bottom gate/top contact configuration was used. First, an Au layer of 100 nm was deposited and patterned on the SMP/glass substrate as a gate electrode, using photolithographic and wet etch processes. Then, a 50 nm thick HfO_2 was deposited as gate dielectric by atomic layer deposition at 100°C. After the dielectric deposition and without patterning, an IGZO film of 40 nm was deposited by RF sputtering at room temperature as a semiconductor layer. The sputtering was carried out using an In:Ga:Zn:O = 1:1:1:4 target from

Kurt J. Lesker Co. Wet etching was used for the IGZO and HfO_2 patterning. Another layer of Au (100 nm) was also deposited and patterned as source and drain contacts. After the fabrication and cleaning of the sample, a soft bake of 100°C for 15 min was used. Several TFTs were characterized with different W and L (combinations of W = 10, 20, 40, and 80/L = 5, 10, 20, and 40 μm). MIM capacitors were also fabricated on the same design with different dimensions (1, 2, 4, and 8×10^{-4} cm^2). Similarly, logic inverters with active load configuration were added, using dimensions of 40 × 20 and 400 × 20 μm (W/L) for the active and control TFTs. The electrical characterization was carried out under dark and regular ambient conditions. For the dielectric constant and capacitance density measurements, an Agilent 4284A LCR Metter was used. Next, a Keithley 4200-SCS semiconductor characterization system and a Cascade Microtech probe station were used for the TFTs current–voltage measurement, as well as the inverters performance. For each test, a total of 16 TFTs were electrically characterized and analyzed. All TFTs were measured from −5 to +5 V (at the gate and using +5 V at the drain) ten times in order to extract variations on the behavior and V_{th} stability. Finally, another annealing treatment of 250°C for 1 h was used to improve the TFTs performance, followed of another electrical characterization for their subsequent analysis and comparison.

5.3 Results and Discussion

The SMP substrate used in this work follows the same synthesis processes previously reported by our group in Simon et al. for the fabrication of intracortical microelectrode arrays which exhibit stiffness at room temperature and subsequently soften after implantation into the body [33]. Dynamic mechanical analysis confirmed that the thermomechanical behavior of the materials used herein were similar to previously published properties. Figure 5.2a shows how the SMP's storage

modulus (E′) drops as function of the temperature from ≈2 GPa to ≈10 MPa (black-solid line). The peak of the tan delta curve denotes the dry T_g at 74.2°C. The network already begins to exhibit viscoelastic behavior in a dry state as low as 60°C (black-dotted line). When the SMP is soaked in PBS solution at 37°C for 1 week, properties shift predictably, as indicated by the storage modulus represented as the gray-solid line and a corresponding T_g shift to 50.1°C with viscoelastic behavior above 30°C. This T_g shift can be attributed to diffusion of water into the polymer network which reduces steric hindrance among polymer side chains and was previously extensively analyzed by Ware et al. as part of a study of the in vivo softening of shape memory polymers for flexible electronics [30]. Thermogravimetric analysis (TGA) verified the thermal degradation of the SMP. TGA of the polymer used in this work demonstrated a weight loss of ≈1.5% at 250°C and 5% at ≈375°C as observed in Figure 5.2b. The thermal stability, as well as their recovery-shape capability, are properties that make SMP substrates an ideal candidate for flexible electronics applications. We hypothesize that during the first thermal ramp, it is just the unreacted parts of the substrate, not the polymer network itself that are removed, which corresponds to little or no effect on the performance of the neat polymers or the annealed devices at 250°C. However, by 375°C significant mass loss driven by oxidative degradation begins to have profound effects on the properties of the substrates and the resulting devices. The SMP film of 50 μm was spin-coated on top of a glass slide as mechanical carrier. An average roughness of 3.6 nm was obtained by atomic force microscope at the SMP surface. Then, the device fabrication was carried out directly onto the SMP layer, without any additional layer or surface treatment, using standard photolithography processes as well as wet and dry etching. After the device fabrication, annealing treatments, and electrical characterizations, the devices were encapsulated with another 5 μm SMP layer and

released from the glass slide. Devices underwent robust electrical characterization. Metal-insulator-metal (MIM) capacitors were fabricated to help in the analysis of TFTs performance, such that a dielectric constant (k) of 12 could be calculated, using a capacitance-voltage analysis and Equation (5.1) where C is the capacitance, ε_0 is the permittivity, A is the area of the capacitor, and t is the dielectric thickness. Figure 5.3a shows IGZO TFTs on SMPs without an annealing treatment are unstable between the first and tenth measurements, even before bending or soaking. Drain current (I_{DS}) is measured with a fixed drain–source voltage (V_{DS}) at 5 V, relative to a sweeping gate-source voltage (V_{GS}) from −5 to 5 V. The On/Off current ratio ($I_{ON/OFF}$) was extracted from the transfer curve (I_{DS}–V_{GS}), showing an $I_{ON/OFF}$ ratio of 3×10^5 for the first measurement. The SS of 870 mV dec^{-1} was calculated using Equation (5.2) to get the Off/On transition. Also, the threshold voltage (V_{th}) of −3.7 V was extracted from the intersection of the linear fit of $I_{DS}^{1/2}$ versus V_{GS} curves. Previously, a variation of TFTs V_{th} had been reported during subsequent measurements due to traps at the interface semiconductor-dielectric and dielectric bulk [35–37]. Similarly, the V_{th} of the IGZO TFTs extracted after ten measurements was −1.2 V. During this test, the V_{th} kept shifting with the subsequent measurements toward positive values.

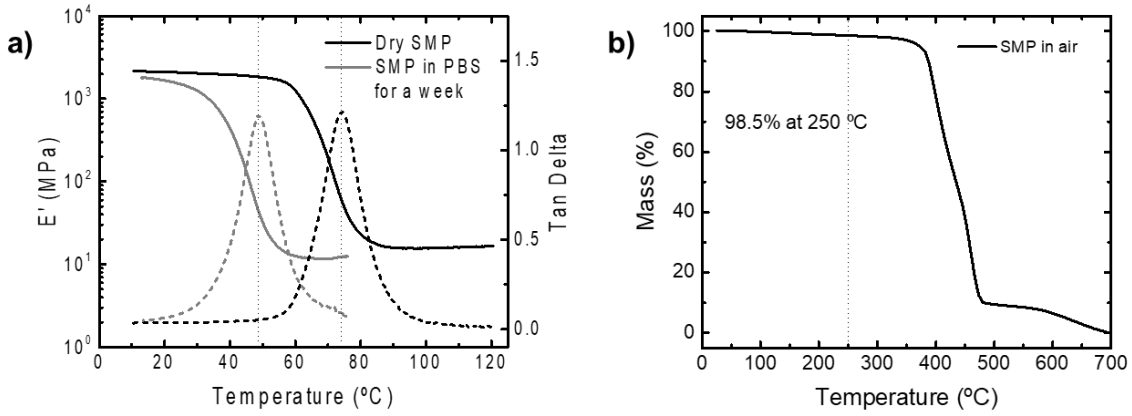

Figure 5.2. a) Dynamic mechanical analysis (DMA) of dry SMP (as synthetized) and after soaked in phosphate buffered saline (PBS) solution at 37°C for 1 week. DMA shows a shift in glass transition temperature (T_g) from 74.2 to 50.1°C, from dry to aqueous conditions. The SMP substrates soften from a storage modulus (E′) of 2 GPa below T_g to 2 MPa above T_g. b) Thermogravimetric analysis of an SMP substrate shows minor degradation of 1.5% at 250°C and the onset of degradation above 350°C.

However, the shift tends to decrease and become negligible by the tenth measurement. The variation in V_{th} (ΔV_{th}) is presented as the difference of V_{th} from the first to the tenth measurement from each TFT, yielding a ΔV_{th} of 2.5 V. Each sweep measurement (from −5 to +5 V at the gate contact) took around 30 s. Therefore, each IGZO TFT characterization last 5 min. The values of $I_{ON/OFF}$ and SS also change to 1.5×10^6 and 228 mV dec^{-1}, respectively. The gate current remains below nA range during the ten measurements. Similarly, the fit slopes used to extract the V_{th} were used to obtain each TFT field effect mobility (μ_{FE}) of 6.4 and 9.3 $cm^2\ V^{-1}\ s^{-1}$, for the first and tenth measurement, respectively, using Equation (5.3), where C_{OX} is the capacitance density of the HfO_2. Figure 5.3b presents the performance of the same IGZO TFTs on SMPs after an annealing treatment of 250°C in air for 1 h.

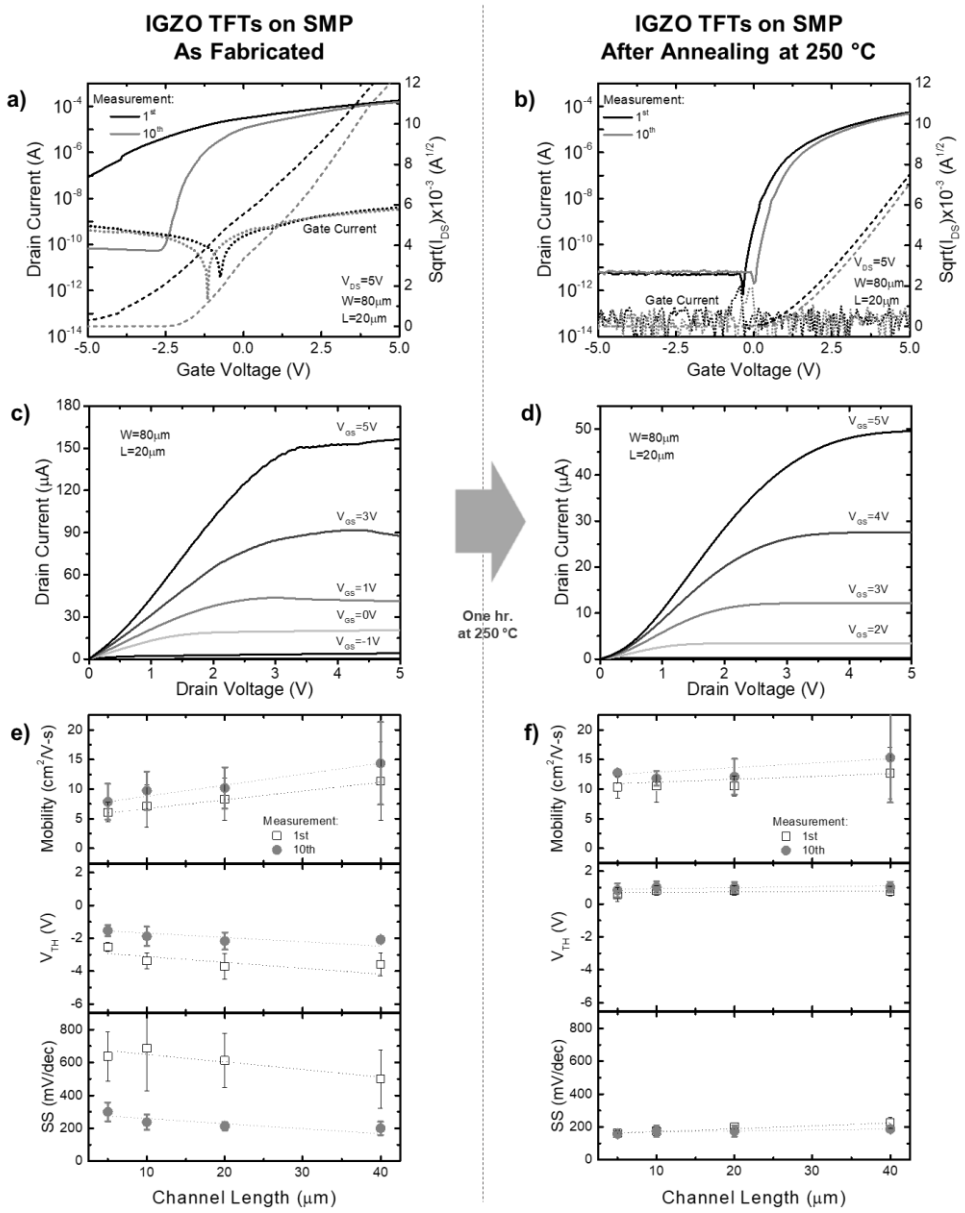

Figure 5.3. Electrical performance of IGZO-TFTs on SMPs before and after annealing treatment at 250°C in Forming gas (FG), using a voltage bias between the source and drain (V_{DS}) of 5 V. The drain current (I_{DS}) for each TFT was continuously measured across 10 gate (to source) voltage (V_{GS}) sweeps between −5 and 5 V for stability comparison, shown as the characteristic transfer curves a) as fabricated and b) after annealing. Solid lines represent I_{DS} on a log scale, while dotted lines the gate current. Dashed lines represent the square root of I_{DS}, commonly used to extract mobility and threshold voltage (V_{th}). Output curves were extracted after the transfer curve measurements c) as fabricated and d) after annealing. Mobility, V_{th} and subthreshold swings (SS) are averaged from sixteen IGZO TFTs on SMPs e) as fabricated and f) after annealing by modifying the channel length (L) at a various channel widths (W) of 10, 20, 40, and 80 μm.

The values of $I_{ON/OFF}$ not only show baseline improvements, but also statistically insignificant changes in the ratio between the first (8.9×10^6) and tenth (9.3×10^6) measurements. The gate current improved by decreasing to the pA range. Similarly, the SS was reduced from 810 mV dec^{-1} to the range of 146–133 mV dec^{-1} during the ten measurements. Additionally, a drastic improvement in the ΔV_{th} behavior was observed, which changes from 1.0 to 1.2 V after the cycled measurement. Mobility values were 17.8 and 15.1 $cm^2\ V^{-1}s^{-1}$, respectively after the first and tenth cycles. Output curves of each IGZO TFT were extracted after the transfer curve measurements. A channel modulation was observed at $V_{GS} = -1$ V before annealing (Figure 5.3c) due to the negative V_{th} value. On the other hand, the TFT after annealing (Figure 5.3d) shows a channel modulation for $V_{GS} = 2$ V due to its V_{th} value of 1.2 V. Different dimensions of characterized IGZO TFTs allowed calculation of the statistical behavior of device electrical properties. In Figure 5.3e, f, a statistical analysis between TFTs before and after the annealing treatment is presented, using 16 devices for each. Figure 5.3e shows the mobility, V_{th} and SS of IGZO TFTs on SMP without the annealing treatment, where the electrical characteristics present unstable behavior between the first and tenth measurements. Extracted mobility of the TFTs varies between 6 and 11.5 $cm^2\ V^{-1}s^{-1}$ for the first measurement alone, as a function of channel length for non-annealed samples. Then, these mobility values shift to between 7.5 and 14.5 $cm^2\ V^{-1}s^{-1}$ by the tenth measurement. The change in mobility between measurements is also observed in Figure 5.3a with a slight increase in current. However, the shift of the threshold voltage is more apparent since the value of the first measurement is ≈−3.5 V and shifts to −2 V for the tenth. Similarly, this change occurs to the SS which shifts from around 850 to 250 mV dec^{-1}. Figure 5.3f also presents the statistical analysis (mobility, V_{th} and SS) of the IGZO TFTs after the annealing treatment. Mobility is uniform relative

to the different dimensions of the TFTs. Also, there is an increase in mobility toward 12.5 ± 2.5 and 15 ± 2 $cm^2\ V^{-1}s^{-1}$, for the first and tenth measurement. The V_{th} values increase to ≈0.9 and 1.1 V and SS values decrease to 145 ± 15 mV dec^{-1} for all measurements.

$$C = \varepsilon_0 kA/t \quad \text{Eq (5.1)}$$

$$SS = \frac{dV_{GS}}{\mathrm{d}\log_{10}(I_{DS})} \quad \text{Eq (5.2)}$$

$$I_{D,sat} = \frac{W\mu C_{ox}}{2L}(V_{GS} - V_{th})^2 \quad \text{Eq (5.3)}$$

After the electrical measurement of the IGZO TFTs on the SMP/glass-carrier, devices were encapsulated with another layer 5 μm thick of SMP, cut and released. These devices on SMP were electrically tested again with no considerable change due to the encapsulation, vias opening and releasing from mechanical carrier processes. Then, the IGZO TFTs were subjected to several bending cycles as shown in Figure 5.4a. A bending-induced strain of ≈0.54% on the devices, parallel to the drain–source channel, was calculated as previously reported methods [38, 39]. Again, the 16 devices with different channel dimensions were electrically characterized and they showed similar behavior after each bending test with the flattened SMP (Figure 5.4b). The electrical performance of the same TFTs (80/20 μm, W/L) were extracted after 10^2, 10^3, and 10^4 bending cycles using a radius of curvature of 5 mm (Figure 5.4c). Statistically, mobility and V_{th} values remain the same after the bending test with similar behaviors as presented in Figure 5.3f. However, a significant change on the subthreshold region between each bending set was observed. SS values increased from 195 mV dec^{-1} to 615, 665, and 750 mV dec^{-1} for 10^2, 10^3, and 10^4 bending cycles, respectively. In order to frame potential biomedical applications, as well observe possible degradation mechanisms of these IGZO TFTs, an SMP sample with these devices was

soaked in PBS solution at 37°C for 1 week (Figure 5.4d). The PBS, which is commonly used to model in vivo conditions, was purchased from Fisher–BioReagents and has a pH level of 7.4. The SMP sample was removed from the PBS solution and then was dried for another week in a desiccator.

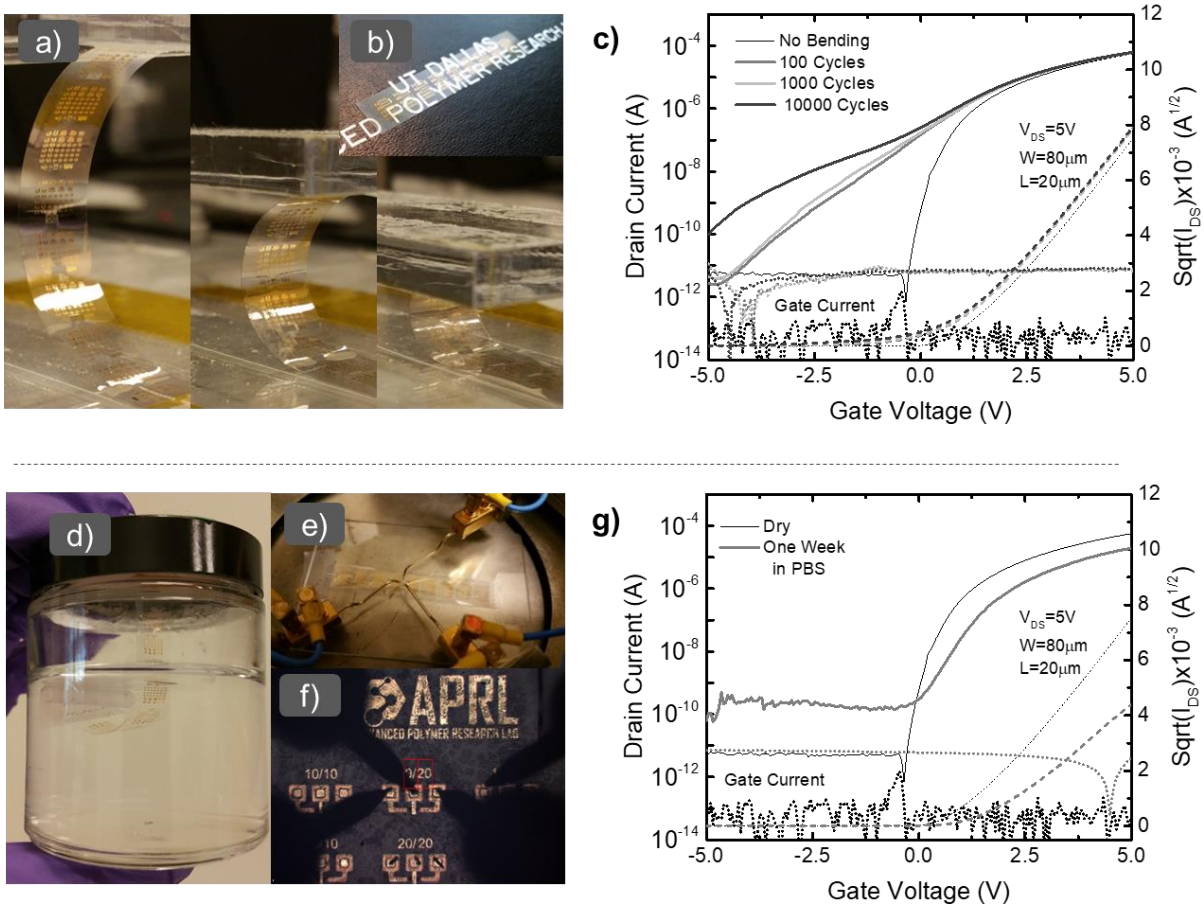

Figure 5.4. a) IGZO-TFTs on SMPs are bent to 5 mm radii of curvature. b) Flattened SMP substrates with devices shown prior to electrical characterization. c) Transfer curves show annealed IGZO-TFTs after 0, 100, 1000, and 10 000 bending cycles. d) IGZO-TFTs on SMPs were soaked in PBS for 1 week at 37°C. Dried samples are electrically characterized at e) small and f) large magnification. g) Transfer curves of IGZO-TFTs on SMPs compare dry samples to samples soaked in PBS for 1 week.

After the drying process, 16 devices were electrically characterized again (Figure 5.4e). PBS residues were observed along the sample (Figure 5.4f). Electrical degradation was observed in TFT transfer curves (Figure 5.4g), compared with its original performance (sample after annealing), showing a decrease of I_{ON} and an increase of I_{OFF}. However, three IGZO TFT evaluated devices maintained their original performance and mobility values of 15 $cm^2\ V^{-1}s^{-1}$. Out of the remaining devices, nine showed mobility drops to 1 $cm^2\ V^{-1}s^{-1}$, while the other four dropped to ≈0.1 $cm^2\ V^{-1}s^{-1}$. Specific V_{th} values shift between 0.5 and 1.5 V through the 16 devices. The ΔV_{th} remains unchanged in all cases between the first and tenth measurements. There are several agents that can be involved in the performance deterioration of only some of the soaked devices. Trapped dust particles (1–10 μm) during packaging can generate pinholes in the encapsulation layer (5 μm) supporting the isolation breakdown. Another possibility is the oxygen incorporation into the IGZO channel which could explain the TFTs performance deterioration as previously reported [40, 41]. The SMP encapsulation plays an important role to calculate the device lifetime in PBS or another solution. Other published studies have tracked swelling and water uptake of SMP in PBS for bioelectronic devices [33]. Previous studies on similar thiol-ene/acrylate substrate indicate around 2% swelling in PBS at 37°C over 30 d. A possible solution to this effect could be the integration of an isolation layer acting as a bio-fluid barrier without compromising the device flexibility as the presented by Fang et al [42]. Despite the meager 18.75% yield of working transistors after soaking for a week in PBS at 37 °C, our results prove that a well-packaged device can endure harsh in vivo environments and deliver reliable performance if packaged appropriately. Other nuances exist in the electrical performance data. Mobility variations among the different dimensions of the TFTs channels (as the observed in Figure 5.3f) could be due to the channel length effect, which is

commonly attributed when the channel resistance is dominated by the drain–source contact resistance as previously reported [43–45]. The TFT stability is commonly associated with the variation in the V_{th}, which has been one of the major foci of research into low-temperature TFT technologies, a problem that can be solved with the increasing of processing temperatures [17, 18, 46–49].

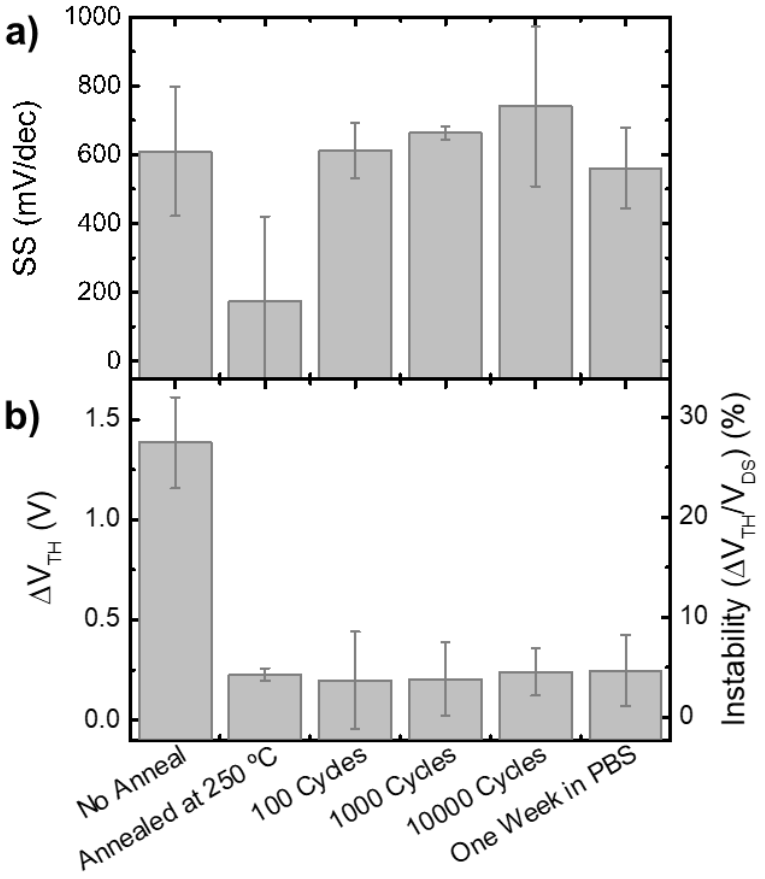

Figure 5.5. a) SS and b) V_{th} shift (ΔV_{th}) of the IGZO TFTs on SMPs are compared as a function of various post-processing treatments. Moisture and bending had an adverse effect on the SS of the annealed samples while ΔV_{th} remained stable. Across treatments, V_{DS} was constant at 5 V so device instability can be mapped as a percentage based on ΔV_{th}. No annealing leads to 27.5% instability, while all forms of post-processing after annealing maintain instability of ≈5%.

In the same way, lowering the SS values means a reduction of trap density at the interface dielectric-semiconductor (D_{it}). A low SS is desired to improve electrical performance of the device since TFTs will require less voltage to change the channel current. By using Equation (5.4), where q is the electron charge, k is the Boltzmann constant, and T is temperature, a D_{it} of 2.2×10^{13} and 2.7×10^{11} cm^{-2} eV^{-1} were calculated for the TFTs without and with the annealing treatment. However, as indicated in Figure 5.5a, SS tends to increase with bending and after being soaked in PBS solution, suggesting that defects are being generated at the bulk of the semiconductor and dielectrics films. The annealing treatment also helped to reduce the oxide trap charges at the dielectric bulk (N_{ot}) which is directly proportional to the ΔV_{th} and calculated by Equation (5.5). After the annealing treatments, the TFTs ΔV_{th} is reduced to 0.25 ± 0.05 V (Figure 5.5b). It is also important to notice that the ΔV_{th} varies little during the bending and soaking in PBS tests. Therefore, it is possible to compare both TFTs N_{OT} values and see the reduction of defects on the dielectric bulk from 1.71×10^{12} to 3.12×10^{11} cm^{-2} after the annealing treatment. As shown here and throughout literature, much research focused on fabricating IGZO TFTs to improve the stability, agree on the use of annealing treatment to improve the quality of the films and interfaces [19–21, 50]. However, it is difficult to directly compare these results with other TFTs' electrical performance since there are large differences in materials, thicknesses, structures, and important operating ranges, which can vary depending on the circuit application. For this reason, in this work, the ΔV_{th} was also compared with V_{DS} (and V_{GS} at 5 V as the maximum operation voltage) showing variations of 27.6 ± 5.3% before and 4.5 ± 0.6% after the annealing treatment (Figure 5.5b). Finally, logic inverter circuits using IGZO on SMP TFTs are demonstrated in order to establish a credible pathway to move toward more complex circuits as previously reported on different

substrates [51–53]. An active load configuration for a logic inverter is presented in this work. The *W/L* dimensions used for the load TFT were 40/20 and 400/20 μm for the drive TFT. In addition to the TFTs alone, the inverters' electrical performance before and after the annealing treatment are also exhibited. Figure 5.6a shows the electrical performance of the logic inverter before the 250°C annealing treatment, where a large variation is observed in the On/Off voltage transition curve between the first and tenth measurements, beginning at negative voltages. Inverter gains were calculated to be ≈0.5 using Equation (5.6). After the 250°C annealing treatment, the voltage transition and gain curves in Figure 5.6b show a reduction in the variation between the first and tenth cycles, gain increases and movement of the functional operational range toward positive voltages.

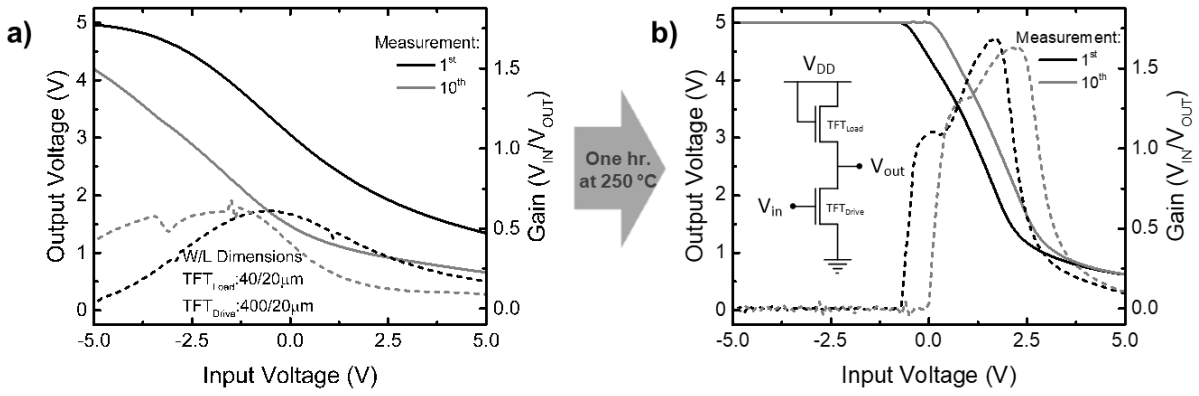

Figure 5.6. Output voltage (V_{out}) of logic inverters is measured using an active load configuration using two IGZO TFTs on SMPs a) as fabricated and b) after annealing treatment in air at 250°C. Each inverter was continuously measured across 10 input voltage (V_{in}) sweeps between −5 and 5 V for stability comparison. Solid lines represent voltage transfer curves (V_{out} vs V_{in}) and dotted lines the gain (ratio of V_{in} to V_{out}) versus V_{in}. V_{IN} at a device level is equivalent to V_{GS} at a transistor level.

The unstable shift behavior of the inverter On/Off transition curve is attributed to the TFTs V_{th}. As for the TFTs, the variations between the consecutive measurements are reduced with the annealing treatment. Also, the logic circuit shows a slight improvement on the gain as TFT mobility increases.

$$D_{it} = \frac{C_{ox}(\Delta SS - 1)}{\ln(10) q k T} \quad \text{Eq (5.4)}$$

$$N_{ot} = \frac{C_{ox} \Delta V_{th}}{q} \quad \text{Eq (5.5)}$$

$$Gain = -\partial V_{out} / \partial V_{in} \quad \text{Eq (5.6)}$$

5.4 Conclusions

In summary, this work presents the fabrication of IGZO TFTs with high temperature processing on a thermoset SMP as a flexible substrate. The analysis of the electrical performance before and after an annealing treatment shows a considerable improvement on the stability behavior as well as an increase in mobility. Average TFTs mobility, V_{th}, ΔV_{th}, and SS of 15 ± 2.5 $cm^2\ V^{-1}s^{-1}$, 1 ± 0.1 V, 0.25 ± 0.05 V, and 145 ± 15 mV dec^{-1}, were obtained from 16 devices after annealing at 250°C. Also, this work proves that SMPs can be used as substrate for the fabrication of TFT technologies using high temperature ranges without significant mass loss or conductor cracking or layer misalignment from anisotropic mechanical deformation during thermal cycling. Taking advantage of the dimensional stability, as well as the shape-memory capability, logic inverters were fabricated, analyzed, and discussed, resulting in enhanced performance after the annealing treatment. A mechanical deformation resilience was also observed from the IGZO TFTs performance. Well-packaged devices survived soaking PBS environments at 37°C for 1 week with little effect on electrical properties of the encapsulated transistors. All told, well-packaged,

fabricated IGZO TFTs on SMPs are promising candidates for flexible electronics applications such as RF-ID tags, displays, and sensors and could help launch a new generation of multichannel and implantable bioelectronics.

5.5 References

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BIOGRAPHICAL SKETCH

Ovidio Rodriguez Lopez was born in Sabinas, Coahuila, Mexico. He is the son of Ovidio Rodriguez Jimenez and Rosa Guadalupe Lopez Ramos. He finished his BE in Mechatronic Engineering at the Saltillo Technological Institute in 2015. During his studies, he made an internship at Delphi Diesel Systems as a process engineering and with other fellow students, he represented his institute in the contest Daimler challenge 2014. Additionally, he was named president of the Mechatronic student chapter and worked towards improving the reputation of the institute. In 2015, he joined the Advanced Polymer Research Lab (APRL) at The University of Texas at Dallas (UTD) under the supervision of Dr. Walter Voit and Dr. Gerardo Gutierrez Heredia. Finally, he started his graduate studies in Electrical Engineering at UTD in 2017 to continue with his research in the development thin film transistors (TFTs) on shape memory polymers for implantable neural interface devices.

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Ovidio Rodriguez Lopez

Relevant Professional Experience

The University of Texas at Dallas – Advanced Polymer Research Lab

Research Assistant, August 2017 – present

- Focus on the development of flexible electronics for biomedical implantable devices. Micro-fabrication, electrical characterization and performance analysis of IGZO thin-film transistors using a softening, bendable polymer as substrate.

Student Chapter of Mechatronic Engineering at the Technological Institute of Saltillo

President, Period 2013 – 2014

- Development of CAD software and programming courses for the students' development.
- Donation of computer equipment and robotic kits to the Mechanic-Mechatronic engineering department of the Technological Institute of Saltillo.

Reto DAIMLER 2014

Team member, Spring 2014

- Automated manufacturing process development
- Integration of ABB robots and a PLC Allen Bradley as Human Machine Interface (HMI) for handling and welding of aluminum sheets.

Delphi Diesel Systems

Process Engineering, Internship 2012-2013

- Standardization of the manufacturing process for diesel injectors.
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Ph.D. in Electrical Engineering - Solid-State Devices Concentration, Aug. 2019 – present GPA: 3.54/4.00

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Papers and Presentation

Papers

- Gutierrez-Heredia, G., Pineda-Leon, H. A., Carrillo-Castillo, A., **Rodriguez-Lopez, O**., Tishechkin, M., Ong, K. M., … Voit, W. E. (2018). Lifetime of hafnium oxide dielectric in thin-film devices fabricated on deformable softening polymer substrate. *Materials Science in Semiconductor Processing*, *88*(July), 273–277. https://doi.org/10.1016/j.mssp.2018.08.010
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- Gutierrez-Heredia, G., Meang, J., **Rodriguez-Lopez, O**., Voit, W. E (2018). Effect of Annealing Atmosphere on IGZO Thin Film Transistors on a Deformable Softening Polymer Substrate. *Semiconductor Science and Technology*, 0–15. https://doi.org/10.1088/1361- 6641/aad293
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Presentations

- 2018 MRS – Fall Meeting & Exhibit Poster presentation, *Electrical Performance after Mechanical Stress of Hafnium Oxide Capacitors on a Deformable Softening Polymer Substrate*
- XXVI International Materials Research Congress 2017 Poster presentation., *Hafnium Oxide Thin-Film Capacitors on Shape Memory Polymer*

Organizations

IntelliChoice – Free Math Tutoring

Carrollton Branch Manager, April 2017 - present

Red de Talentos Mexicanos (Mexican Talent Network)

Dallas Branch Volunteer, November 2016 - present