HIGH-DENSITY ON-CHIP DC-DC POWER CONVERSION:

ARCHITECTURE, CONTROL SCHEME, AND CIRCUIT DESIGN

by

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To my wife, Eunjeong Kim, sons and dear family

Thank you for all the love and support

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Modern mobile devices have been developed with the trend towards improving performance, integrating further multiple functions in limited form factor, and providing long runtime. Therefore, high-density power converters are required to facilitate this trend, while maintaining fundamental features, such as high efficiency over the wide-load-range, fixed switching frequency, low EMI noise, high reliability, low latency, low-quiescent power consumption, and wide input-voltage (V_{IN}) for direct usage of the varied battery voltage. This dissertation describes advanced system architectures, control schemes, and circuit designs, which can overcome the design challenges to enhance power density of the DC-DC converters.

First, the dissertation discusses achieving system-level miniaturization by improving the power distribution plan in the battery-operated mobile applications. To mitigate the design challenges, a 3-level converter is essential due to its half V_{IN} swing, which allows direct supply connection with the varied battery voltage while using the thin-oxide devices, enabling power converter integration with another functional device on the same chip. Although the half V_{IN} swing in the 3-level converter allows operating at high switching frequency, which induces small passives and fast

response, the efficiency as well as V_{IN} range reported in the published works was limited. To further improve the efficiency, a 20MHz all-NMOS 3-level converter is presented. To handle all-NMOS power switches even with varied V_{IN} supply, such as battery, the isolated bootstrap circuit is proposed to mitigate the voltage charging issue in the 3-level high-side gate driving. Also, proposed is a precise sub-ns dead-time controller, which is integrated in the gate buffer stage, minimizing the dead-time power loss without sacrificing reliability.

To deliver high power with tremendous current slew rate required in the mobile application processors, a 25 MHz, 4-phase power converter is presented. The converter employs a synchronized adaptive window hysteretic control to facilitate ultra-fast transient response and minimize output voltage (V_O) undershoot and overshoot. Its inherent clock synchronization ability ensures current balancing among the phase sub-converters. The control is also capable of providing a wide range of programmable V_O for dynamic voltage scaling, thereby efficiently saving system power. As the all-phase operation degrades the light-load efficiency, a 1-Cycle active phase count scheme is introduced to maintain high efficiency over a wide load range without degrading transient speed.

To further integrate required design features for mobile applications, the hybrid digital-assisted double adaptive bound (DAB) converter is developed. The analog DAB controller achieves fast transient response, fixed switching frequency, high output regulation, and wide V_{IN} supply in a compact structure. Combining the DAB control with a digital mode manager, the proposed hybrid converter provides four operation modes to further improve transient performance and wide-load-range efficiency. Due to the single control loop assisted by the digital mode manager, the converter successfully utilizes fast and seamless mode transitions without any supply glitch.

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CHAPTER 1

RESEARCH BACKGROUND AND MOTIVATION

This chapter provides a brief discussion of the background, motivation, and major contributions of this research development. Section 1.1 provides a general overview of the development trends in the mobile application. Subsequently, Section 1.2 discusses three major challenges that need to be considered to design the high-density power converter in the mobile system: power train and converter architectures for achieving system-level miniaturization, control design for compact and robust converters, and circuit design techniques for resolving the demerits of using the simple and high-performing hysteretic control. Then, briefly introduced in Section 1.3 is the main focus of this research, which is the goal to overcome the aforementioned challenges. Finally, Section 1.4 discusses the organization of this dissertation.

1.1 Development Trends of the Mobile Application

Over the last 20 years, mobile usage across the globe has grown tremendously. Users of mobile devices in 2017 numbered more than 5 billion people, which is two-thirds of the global population [George-17]. As the number of users and their needs have increased, so have the mobile device innovations and new products from the earliest days of feature phones, to smartphones, and now tablets and Internet-of-Things (IoTs). These innovations have come in the form of new technology and functionality together, integrating multiple functions in one device, such as display, camera, communication, sensor, application processor etc. Even with employing multiple functions together, the device has to be lightweight and handy for portability. In addition, these individual functions have been constantly improved in performance [Arm-14 and Girardin-16]. For example, consumers demand thinner form factors, bigger display, faster connectivity, and

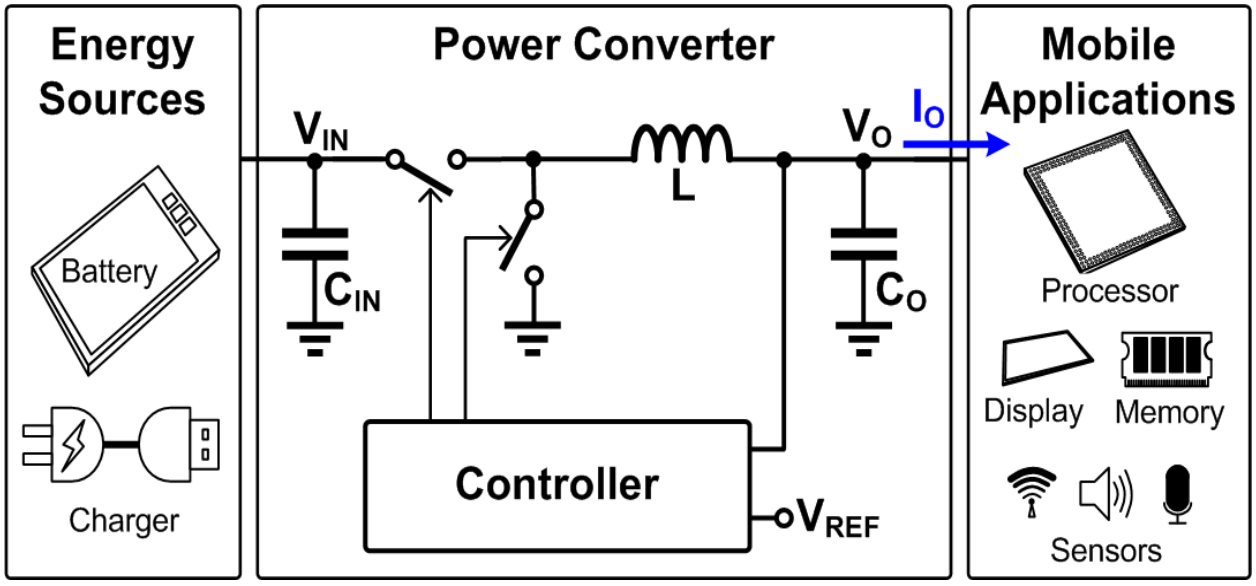
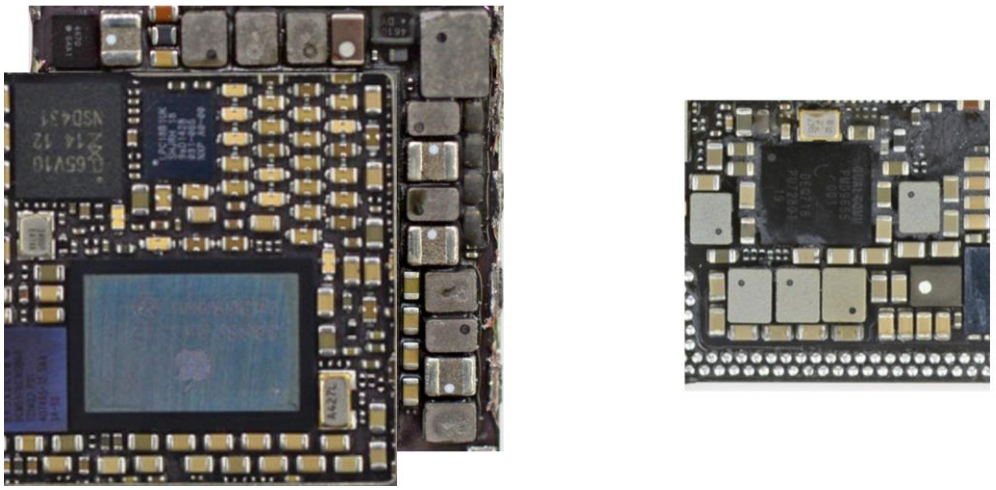


Figure 1.1. System diagram of the mobile application.

better multimedia capabilities. In this case, the device requires much more processing capability and demands more power. Despite the advancements in device capabilities, the long operating time remains the most desired feature by consumers [Kumar-12 and Qualcomm-13]. In order to increase the operating time, the energy storage sources, e.g., the battery, should be improved in energy density. However, unlike the other functional devices that have been improved in their density, which, according to Moore's law, doubles every two years, battery technology has not improved due to the physics limitation [Schlachter-13]. In fact, it takes a decade to double the battery energy density.

In order to operate these advanced mobile applications, power converters are required to bride battery (or charger) with individual functional devices as shown in Figure 1.1. Along with the improvement in performance as mentioned before, such a power converter is required to deliver higher power demanded by advanced applications. Furthermore, the form factor of the power system has to be miniaturized for portability and cost reduction. For example, Figure 1.2 shows



(a) (b)

Figure 1.2. Application boards: (a) iPhone 6 [Djuric-14] and (b) iPhone X [Lionheart-17].

the power converters in the application boards of the iPhone 6, developed in 2014, and the iPhone X, developed in 2017 [Djuric-14 and Lionheart-17]. As can be seen, with the three-year difference, the footprint of the iPhone X was significantly reduced, compared to the iPhone6, even though the iPhone X embodies more functions. Moreover, to support the long operating time of the portable application, the power system must have a high efficient design but with low cost and compact structure. For these reasons, the high-density power converter is required.

1.2 Challenges of the Mobile System Design

As discussed in the previous section, the perpetual demands for improved processing performance and high levels of transistor integration have led to innovations in new portable applications. However, with the increased complexity of theses advanced systems, new design challenges related to the power converter arise. First, in order to increase the density of the power converter, increasing switching frequency allows much smaller passive components (inductor L and output capacitor C_O as shown in Figure 1.1), which account for the major portion of the powertrain and cost, resulting in small form factor and compact packaging. However, as shown in

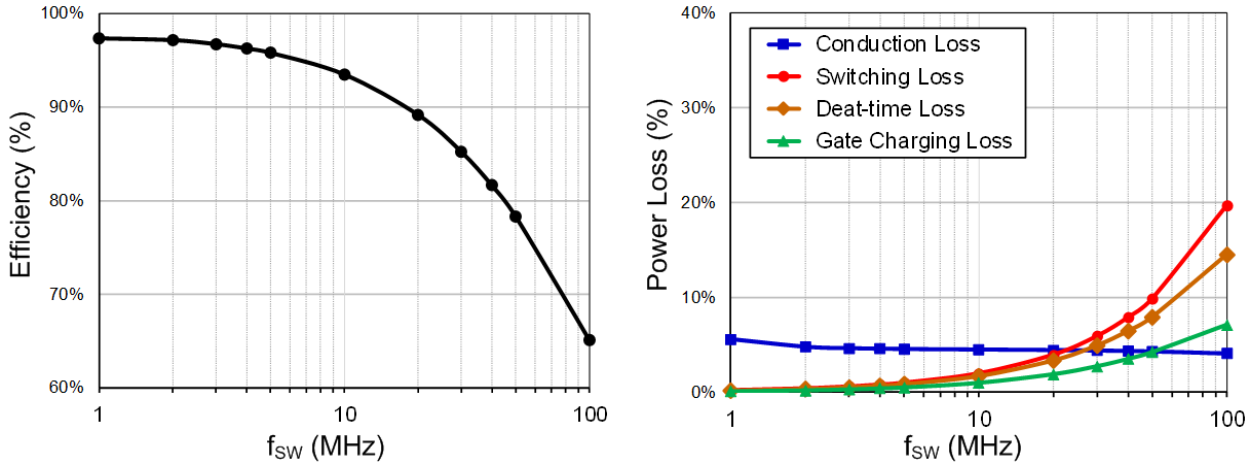


Figure 1.3. Power efficiency and power losses versus switching frequency for 3.3 V to 1.6 V conversion at the load current of 0.5 A in 0.35 μm CMOS process.

Figure 1.3, the system power efficiency is degraded significantly. Here, detailed power losses can be classified into four categories: 1) conduction loss ($R_{ON}I_O^2$), 2) switching loss ($0.5V_{IN}\times I_O\times t_r\times f_{SW}$), 3) dead-time loss ($V_f\times I_O\times t_D\times f_{SW}$), and 4) gate charging loss ($Q_{GG}\times V_{DRV}\times f_{SW}$), where R_{ON} is the total on-resistance in the converter including power switches and inductor, I_O is load current, t_r is the sum of the rising/falling time on V_{LX}, and f_{SW} is the switching frequency. Also, V_f is the diode forward voltage, t_D is the sum of the power switches' non-overlap time (=dead-time) at V_{LX} rising/falling, V_{DRV} is the gate driving voltage for the power switches, and Q_{GG} is the overall electrical charge in the power switches [Rohm-16]. Here, all power losses, except the conduction loss, are related to f_{SW}. Thus, when the load is decreased, despite the reduced conduction loss, the other losses are increased.; i.e., the dominant power at light load is all f_{SW}-related power losses, challenging mobile devices to increase f_{SW} [Jauregui-11]. In addition, at high frequency level, speed requirements on controller and gate driver designs are extremely high. The electrical magnetic interference (EMI) and radio frequency interference noises also require special attention. Hence, to understand detailed issues in power management for state-of-the-art portable systems,

this section addresses design challenges with three different aspects: architecture, circuit, and design.

1.2.1 Challenges on Architecture

In modern portable devices, a rechargeable Lithium-ion battery is commonly used due to high energy density and low price [Crabtree-15 and Curry-17], and its operating voltage varied from 3V to 4.2V. Also, in order to recharge the battery, the system needs a charger, which has higher charging voltage than battery voltage, commonly using 5V. However, with aggressive CMOS technology scaling, the transistor ratings in the digital modules have been scaled around 1 V or even lower. Therefore, the converter cannot directly connect with the energy sources for

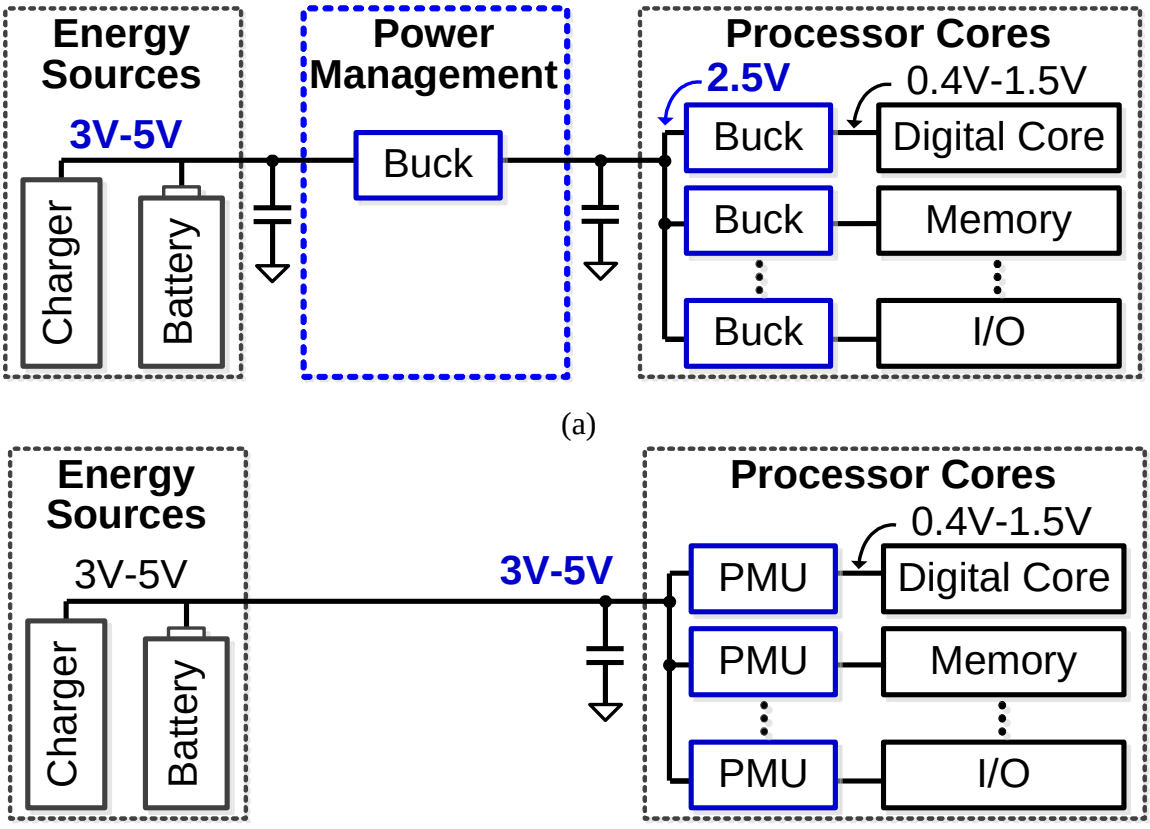


Figure 1.4. Power distribution plan for mobile application

supplying power. Furthermore, to extend the operating time of the digital modules, especially the processors, and to maximize the energy efficiency, the supply voltage (V_O) is reduced to the near-threshold voltage and the operating frequency is reduced as well, known as dynamic voltage/frequency scaling (DVFS) [Borker-11, Dreslinski-10, and Zhai-04], requiring a large output voltage range and fast voltage scaling.

Figure 1.4 illustrates the power distribution plan for the mobile system. In a conventional system, as shown in Figure. 1.4(a), the power converters are located on the processor cores. Although this approach can reduce the number of power paths, parasitics, and components, the input voltage of the traditional buck converter should be the same as the device breakdown voltage. In order to bridge the voltage gap between the energy sources and input voltage of the converter, an external power converter is also required, consuming the extra footprint and cost. In this case, the total power efficiency (η) is degraded due to the number of the converting stages ($\eta_{total} = \eta_1 \times \eta_2$), degrading the efficiency. Moreover, to further improve the power density, the external power management unit (PMU) has to be removed and the energy source should be directly used for the input supply. Therefore, the new wide-input power converter has to be developed to overcome the

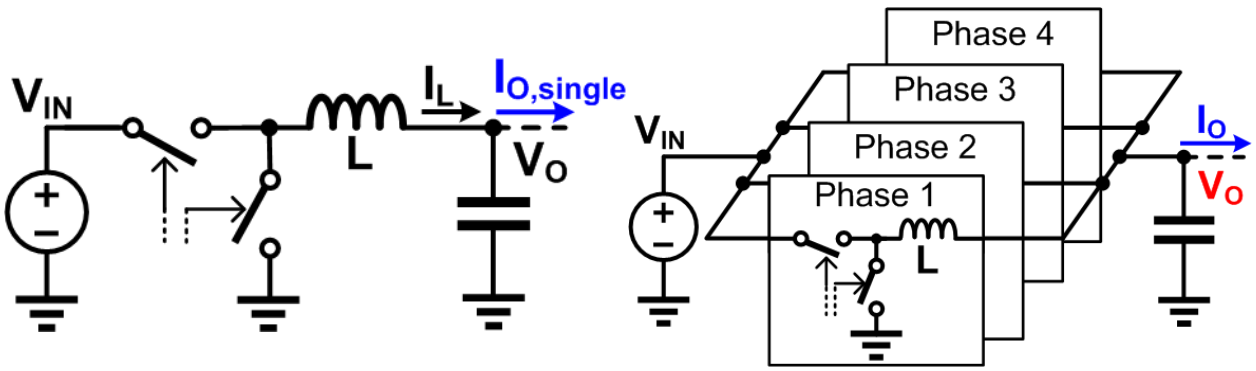


Figure 1.5. Power converter architecture: (a) single-phase and (b) multiphase.

breakdown voltage limit of the power switches, as shown in Figure 1.4(b). This solution has the benefit of improving the efficiency due to the single-stage power conversion, compared to the previous power plan.

On the other hand, the power converter requires handling large current along with the advanced application demand. In order to increase the amount of the supplying power, two converter architectures can be considered as shown in Figure 1.5. Compared to the single-phase architecture as shown in Figure 1.5(a), the multiphase architecture in Figure 1.5(b) has many benefits [Baba-12, Tim-07 and Wong-15]. Instead of using a single inductor in the single-phase architecture, the multiphase architecture uses multiple inductors and each phase turns-on in a time-interleaved manner. When all the inductor currents are added together, it supplies much higher power. Also, due to time interleaved operation, the steady state voltage ripple at V_O is also reduced

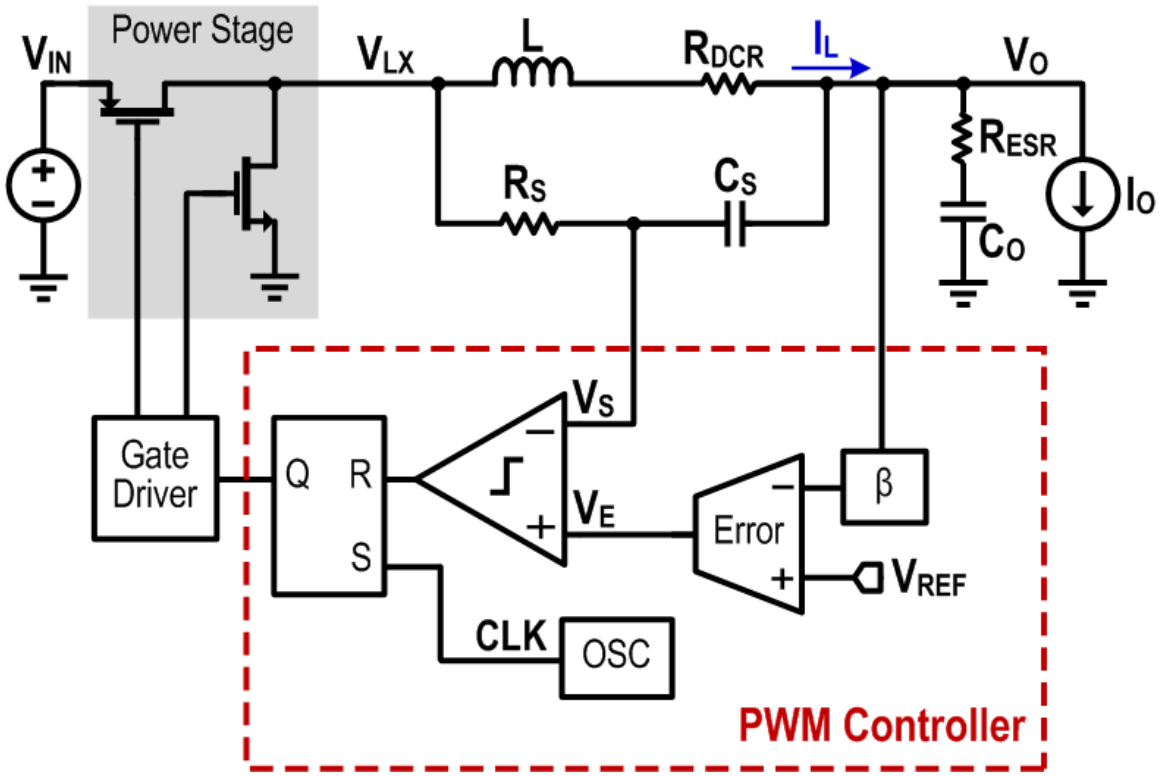


Figure 1.6. Conventional current-mode PWM controller.

due to ripple cancellation in the multiphase converter, helping to reduce the input and output capacitor size and form factor. Furthermore, compared with the single-phase converter, the multiphase converter improves transient response performance due to equivalently extended loop-gain bandwidth. However, at light load, the all-phase operation degrades the power efficiency significantly due to higher switching loss. Also, to ensure time interleaved operation, a fixed frequency operation is essential.

1.2.2 Challenges on Control Scheme

The other view in the power converter is the control scheme, which produces the duty cycle and maintains regulation. Generally, the control schemes can be classified into two categories such as pulse width modulation (PWM) and hysteretic controller. Figure 1.6 demonstrates the block diagram of the PWM control scheme. In this scheme, the leading edge of each switching cycle is synchronized by the clock pulse input, CLK, while the falling edge of the switching cycle is determined by the control bandwidth, which is set by the error amplifier as depicted in Figure 1.6. Due to this fixed f_{SW} and clock synchronization, the PWM control scheme has been widely adopted in the interleaved multiphase implementation. Moreover, to regulate the output, this control scheme is based on the linear control theory; thus, the speed of the converter is determined by the control bandwidth, which is limited to five to ten times below f_{SW}, leading to slow transient response and bulky passives in the power stage. In order to improve transient response, the PWM control are implemented to run at tens or even hundreds of MHz of f_{SW} with small inductors and output capacitors. However, when switching converter operates in high frequency range, efficiency is greatly compromised as switching loss becomes significant, increasing the design

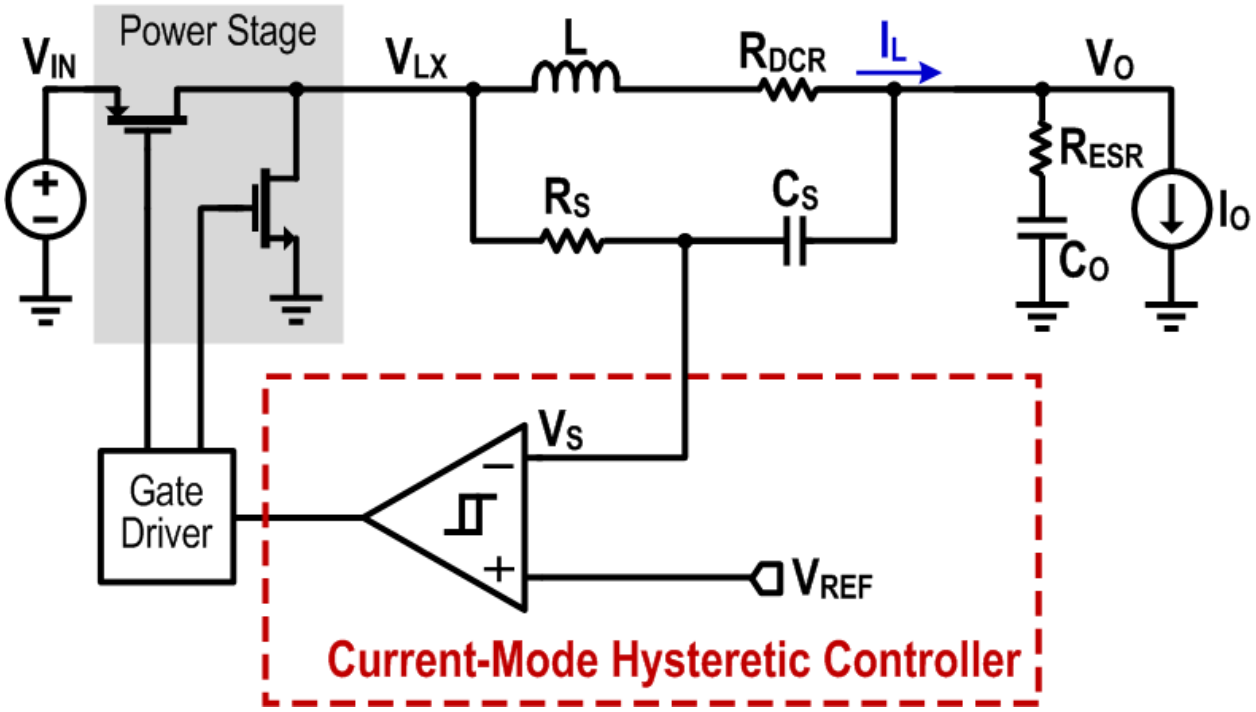


Figure 1.7. Conventional current-mode hysteretic controller.

complexity of the power switch control. Cleary, those challenges are against the power demand trends of the modern portable applications.

Figure 1.7 illustrates the current-mode hysteretic controller. which consists of a hysteretic comparator and an RC matching filter (R_S and C_S). In this control scheme, only the hysteretic comparator is needed to compare inductor current I_L with fixed hysteresis window, ΔV_H. In other words, the peak and valley of the I_L is obviously controlled, making stable system for all duty cycle without the error amplifier and compensation circuit. Furthermore, owing to the direct controlled by I_L and ΔV_H, the hysteretic control can respond within one switching cycle [Keskar-07]. Thus, the speed for the output transient is determined by f_{SW} performing fast transient response is determined by f_{SW}. However, this control scheme has an inherent delay due to realistic hysteretic window size ΔV_H and the limit in physical I_L slew rate, $(V_{IN}-V_O)/L$ or $(V_O)/L$. Another drawback

is that the conventional hysteretic controller operates by variable f_{SW} due to the lack of clock synchronization. Thus, varying f_{SW} requires the design of an input EMI filter and causes current imbalance and hot spot issues in the multiphase converter architecture. Also, when the f_{SW} is changed to be frequency range, the switching noise becomes audible. However, the hysteretic controller still has the benefit of reducing the size due to the simple structure. Thus, this research aims to overcome the disadvantages of the hysteretic control in order to develop the high-density converter.

1.2.3 Challenges on Circuit Design

As mentioned before, for V_O regulation, the conventional current-mode hysteretic control ordinarily compares current I_L with ΔV_H during the whole switching cycle; i.e., the continuous I_L sensor is essential. Instead of using the series resistor sensing [Forghani-zadeh-07], which incurs a power loss in the sensing resistor, the emulated RC matching filter is popularly used as shown in Figure 1.8. By inserting the RC low-pass filter, R_S and C_S, this technique filters the voltage

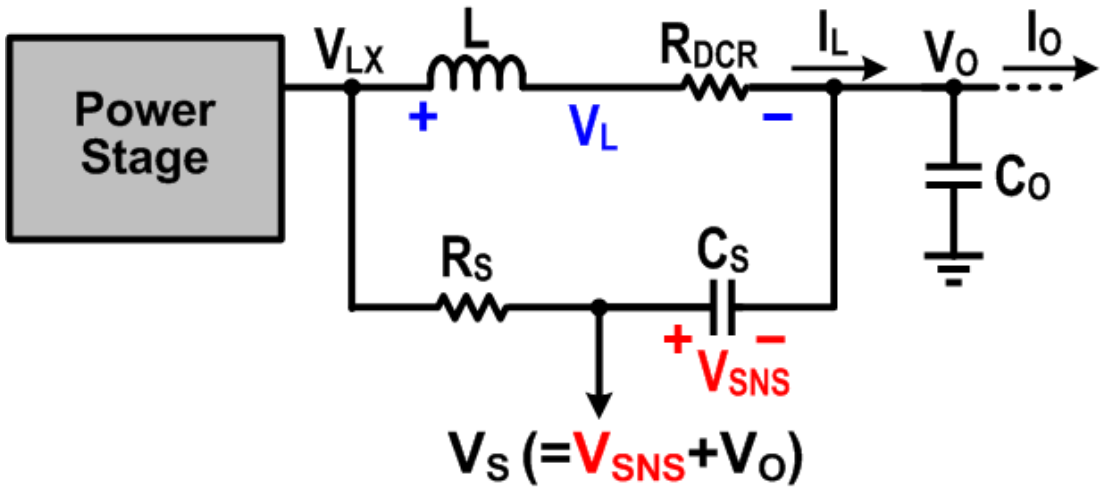


Figure 1.8. The emulated RC matching filter.

across the inductor L and emulates I_L through the DC resistance (R_{DCR}) of L. First, the voltage across L, V_L, is

$$V_L = (sL + R_{DCR})I_L, \tag{1.1}$$

where s is the frequency variable in the Laplace domain. The voltage across C_S, V_{SNS}, is

$$V_{SNS} = \frac{V_L(1/sC_S)}{(R_S + 1/sC_S)} = \frac{(1 + sL/R_{DCR})}{(1 + sR_SC_S)} R_{DCR} I_L . \tag{1.2}$$

Matching $L/R_{DCR} = R_SC_S$ yields

$$V_{SNS} = R_{DCR} I_L . \tag{1.3}$$

where I_L is the DC current of the inductor current, i.e., I_O, and, hence, V_{SNS} emulates I_L as shown in Figure 1.9. The benefits of this technique are not only the continuous I_L sensing, but also no

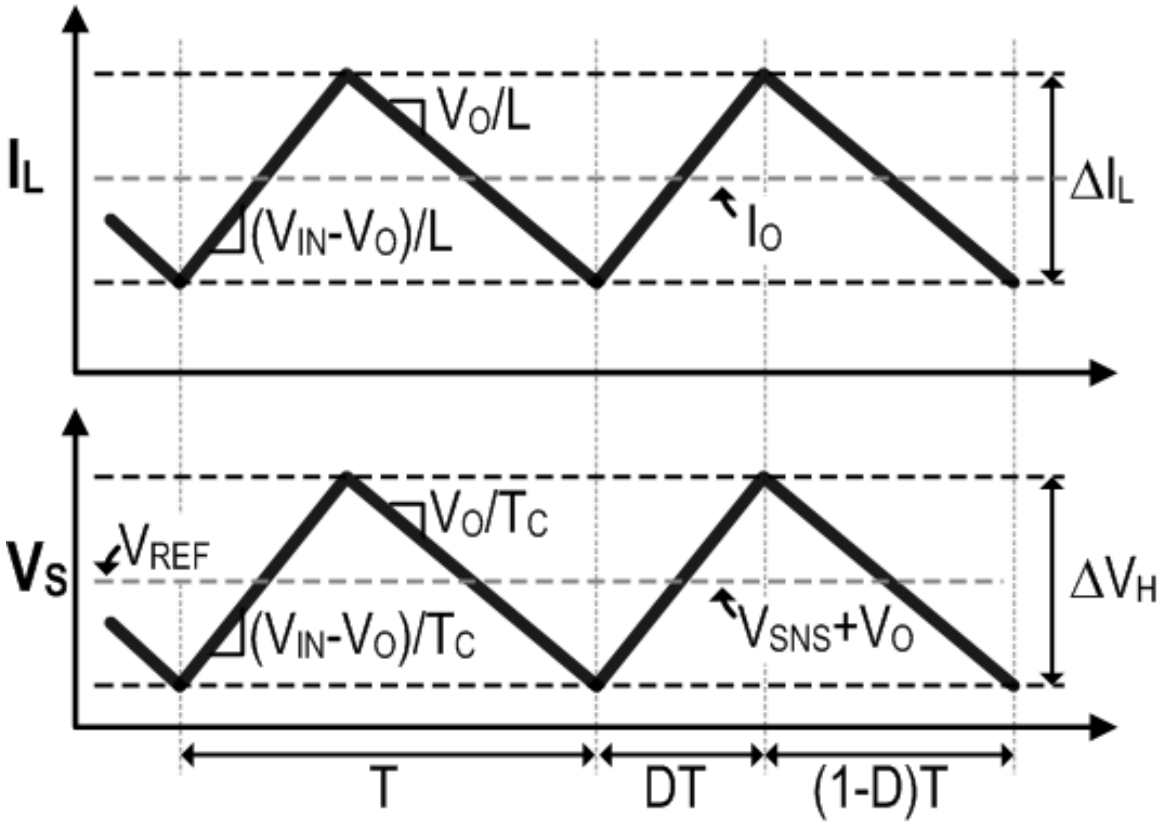


Figure 1.9. Timing diagram of the I_L and V_S in the current-mode hysteretic controller.

power loss. Using this matching filter, the switching frequency in the current-mode hysteretic controller is calculated by

$$f_{SW} = \frac{1}{T} = \frac{V_O\left(1 - V_O/V_{IN}\right)}{L \times \Delta I_L} = \frac{V_O\left(1 - V_O/V_{IN}\right)}{T_C \times \Delta V_H}. \quad (1.4)$$

where T_C is the time constant value of the RC filter, i.e., T_C=$R_S C_S$. However, in the portable application, as battery voltage is varied by stored energy, V_{IN} is not constant. Also, to save the system power, the dynamic voltage scaling (DVS) [Zhai-04] and near-threshold voltage technique [Dreslinski-10] can be implemented by reducing V_O. In this case, f_{SW} is varied with different V_{IN} and V_O in Equation (1.4), making it difficult to employ the simple structure hysteretic controller.

Another challenge to design the hysteretic control is its poor load regulation. In the current-mode hysteretic controller (Figure 1.7), the feedback loop is connected to V_S, which is in the middle of the RC matching filter, rather than V_O, which is given as

$$V_S = V_{SNS} + V_O. \quad (1.5)$$

As the hysteretic controller directly controls V_S within the hysteretic boundary, the average of V_S equals V_{REF}, i.e., V_O=V_{REF} as shown in Figure 1.9. This connection enables the controller to receive the V_O transient simply and directly by C_S, achieving fast response in the hysteretic controller. However, as the sensing signal V_{SNS} is proportional to I_O and R_{DCR} in Equation (1.3), the DCR mismatch is induced, degrading V_O load regulation. Although the converter can eliminate the DCR mismatch by an error amplifier in the control loop [Song-14], this consumes a large silicon area, thus losing the merit of the simple structure of the hysteretic controller.

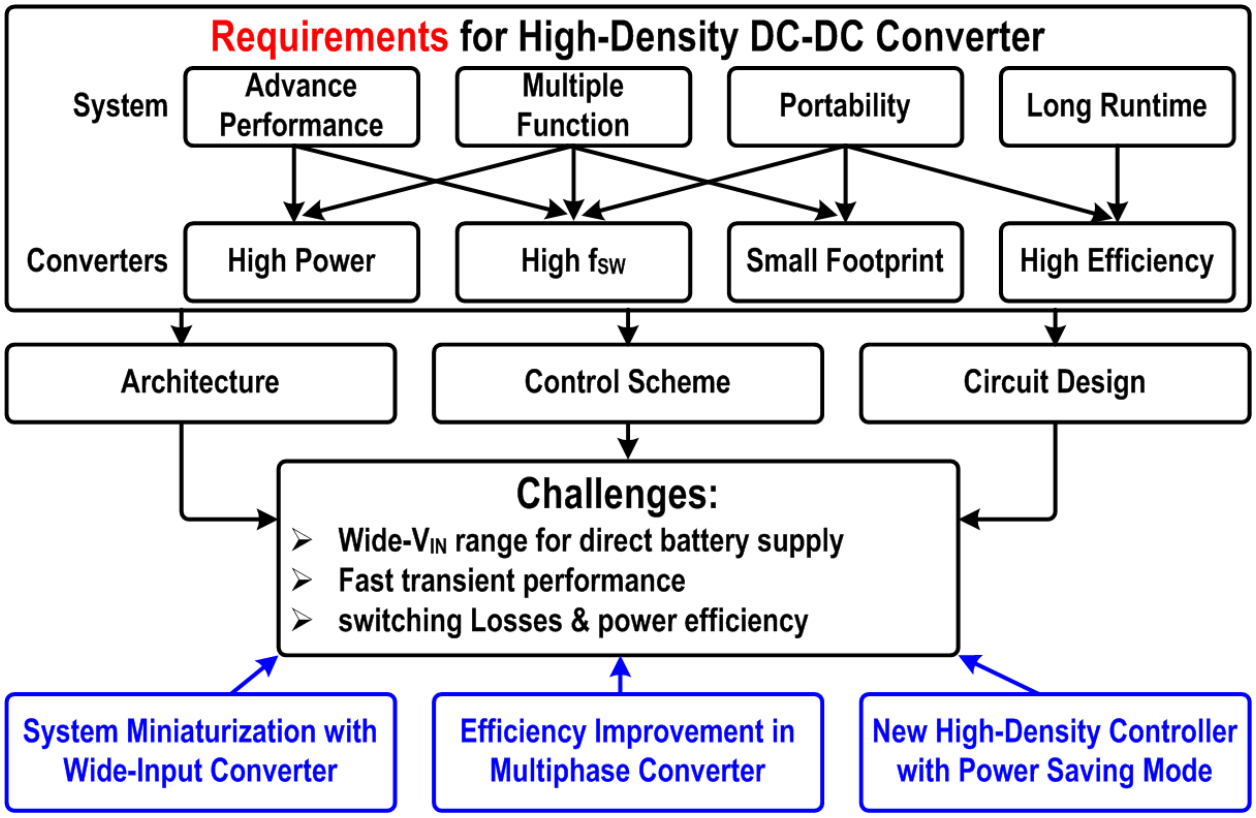


Figure 1.10. Scope of the dissertation.

1.3 Research Goals and Contributions

Figure 1.10 illustrates the scope of the dissertation, which includes the design challenges as discussed in the previous section and research contributions. The high-density power converter is required to achieve a small footprint and deliver higher power, without degrading the efficiency. To develop the high-density power convertor, three aspects were considered: architecture, control scheme, and circuit design. First, to minimize the power distribution area and supply wide-input range, the 3-level converter is proposed by implementing all-NMOS power switches, which is needed to overcome the bootstrap (BST) charging issue under the wide-input range operation. Also, a precise dead-time controller has to be developed not only to minimize the dead-time power loss especially at high switching frequency, but also to prevent shoot-through current of the power

switches for reliable operation. Second, to deliver higher power, the multiphase converter is proposed with the clock synchronized hysteretic controller. In addition, as the all-phase operation degrades the light-load efficiency, the active phase count, which controls the operating phase number, is required without degrading the transient performance. Finally, to achieve the high output regulation and clock synchronization together without degrading the benefit of the simple structure, the double adaptive bound (DAB) controller is proposed. Moreover, to accelerate the transient and light load performance, the hybrid digital-assisted DAB converter is developed. The main outcomes and contributions of this work are described in the following:

(1) Minimized System-Level Power Distribution Plan

(1.1) Developed a high-speed all-NMOS 3-level converter architecture, which reduces the switching power loss by half and enables the use of thin-oxide devices for power switches: This power converter can be directly integrated with the featured chips, such as application processors, reducing the power delivering paths and its parasitics and thus improving system efficiency due to the single power converter stage. In addition, as the figure of merit of NMOS is higher than PMOS, using all-NMOS power switches minimizes the gate driving loss. Consequently, the proposed converter with precise dead-time control jointly accomplishes up to 21.5% power efficiency improvement over the current state-of-the-art.

(1.2) Developed an isolated bootstrap gate driver, which can handle the high-side NMOS power switch in the 3-level converter with a wide V_{IN} supply range: This scheme not only enables the all-NMOS 3-level converter design, but also supports a reliable gate driver even with a varied battery supply. Due to the half voltage swing range in the 3-level converter, the conventional bootstrap gate driver cannot sufficiently charge the gate driving voltage, V_{DRV},

which increases the on-resistance of the power switch, thereby degrading the conduction loss. With the proposed bootstrap scheme, the source of the high-side power switch is isolated to charge the bootstrap capacitor up to V_{DRV}. Thus, the proposed scheme can operate from 3 V to 6 V of V_{IN} without on-resistance variation, enabling the use of the varied battery voltage for V_{IN}. Moreover, the proposed converter can regulate V_O as low as 0.4 V, converted from 6 V of V_{IN}, achieving a minimum duty ratio of only 6.7% at 20 MHz f_{SW}, which is 50% less than the best level in the prior schemes.

(1.3) Developed an interception coupling dead-time (ICDT) controller, which achieves a sub-ns dead-time: The proposed dead-time controller is directly employed in gate driver, eliminating the level-shifter for bootstrap circuits. By reducing the required number of level-shifters, the proposed gate driver not only decreases silicon area and power, but also facilitates a sub-ns delay in the dead-time control loop. In addition, sensing the opposite-side of the gate voltage directly, the dead-time is adaptively and precisely controlled, allowing the aggressive design of the dead-time, which eliminates the dead-time loss, but still provides reliable and secure gate driving. Hence, the proposed design provides 0.5 ns dead-time over a load range of 500 mA at 20 MHz of switching frequency. This also achieves 85.5% of the maximum power efficiency over a 0.8 W power range, which is 21.5% higher than that of the published 3-level DC-DC converter.

(2) Improving Delivering Power with Wide-Load-Range Efficiency

(2.1) Developed a synchronized adaptive window (SAW) hysteretic control to achieve fast transient response and fixed switching frequency, which can upgrade the converter design with multiple operation: This SAW hysteretic control evolved from the concept of the

adaptive window (AW) hysteretic control, which fundamentally elevates the function of the hysteretic window and largely improves the load transient performance of the hysteretic control. Without degrading the fast transient response, the SAW hysteretic control employs the clock synchronization technique, which can be easily applied to the multiphase architecture to facilitate the current balancing among phases. Therefore, the proposed SAW hysteretic controller provides smaller undershoot voltage than the conventional hysteretic controller at load step-up, which is reduced from 80 mV to 42 mV, leading to 47.5% reduction. Meanwhile, 1% settling time t_{settle} drops significantly from 2 μs to 112 ns, thanks to the immediately extended turn-on period in the SAW control. During load step-down, the overshoot voltage is also reduced from 92 mV to 43 mV, a 53% reduction compared to the conventional hysteretic controller. In addition, the proposed design provides a wide programmable range of V_O to accommodate the dynamic voltage scaling (DVS), which is an essential feature to save system power in the application processor. Thus, the proposed controller can regulate the V_O from 0.3 V to 2.6 V with fixed switching frequency of 25 MHz [Lee-17].

(2.2) Developed a 20MHz, four-phase switching power converter with a proposed 1-Cycle active phase count (APC) scheme, which helps the converter maintain high efficiency over a wide output power range without degrading transient response performance: With the proposed 1-Cycle APC, the number of active phases is adaptively adjusted with load current to retain high efficiency. As a result, the efficiency stays above 80% over 96.7% of the full power range, with a peak value of 88.1%, which retains higher efficiency over one

of the widest power ranges than the state-of-the-art. Area-efficient circuit design leads to a very competitive power density of 3.98W/mm^2 even at a higher technology node [Lee-17].

(3) Improving Control Design with Fixed Frequency and High V_O Regulation

(3.1) Developed a double adaptive bound (DAB) control, which integrates all features for high-density mobile applications, such as fixed switching frequency, fast transient performance, high load regulation, and compact design area: This control scheme employs a duty generator with an additional RC filter to achieve the real-time current-slope tracking reference, achieving fast transient and fixed switching frequency together. Moreover, by employing the reset cancellation scheme, the offsets in the RC filters can be eliminated without compensation circuits, enabling 5mV/A of the load regulation and attaining less than 0.3% V_O variation. Furthermore, a wide V_{IN} operation in the converter allows direct connection with the battery, which has varied voltage depending on its stored energy, eliminating the need for another power converter stage and thus enhancing system efficiency. All these features are integrated in the single control scheme, facilitating compact size.

(3.2) Developed a hybrid digital-assisted DAB converter with an autonomous mode manager (AMM), which implements four modes for operating at different load conditions, further improving transient response and wide-load-range efficiency: Combining the DAB controller with the AMM, the proposed converter further enhances fast transient response, achieving 31 mV of V_O droop with fast settling time of 200 ns when load step-up occurs from zero to maximum in 3 ns. Moreover, by employing discontinuous conduction mode and pulse skipping mode in the single controller, wide-load-range efficiency can be

utilized. In addition, all-digital implementation in the mode manager avoids the power- and silicon-hungry analog circuits. The proposed techniques have been combined and realized by compact designed circuits, facilitating seamless mode transition owing to the single control loop. Thanks to the digital implementation, all design features have been integrated into a small silicon area, achieving the highest reported chip power density of 14 W/mm^2 with traditional technology node. The design achieves above 80% efficiency over 99.9% of the full power range with a peak value of 91%. Accordingly, this work is appropriate for further integration in compact and low-power portable applications for system-on-chip designs.

1.4 Dissertation Organization

The rest of the dissertation is organized as follows. In Chapter 2, the benefits of the 3-level converter to overcome the limitation of the system-level power distribution plan are first introduced, including half of the switching loss and thinner oxide device usage due to the converter's half-voltage switching, which allows operating at high switching frequency, thereby inducing small passives. Also addressed are the design limitations for applying the battery-operated system in published 3-level converters, including low power efficiency and constant V_{IN} operation. The system architecture of the proposed 3-level converter is introduced, and three key operation schemes are illustrated. Instead of using PMOS devices for high-side power switches, using all-NMOS devices in the proposed design overcomes the power efficiency limitation in the previous studies. The isolated bootstrap gate driver is essential to handle these all-NMOS power switches even with varied supply voltage. In addition, the sub-ns dead-time control scheme is presented, which eliminates level-shifters and further dead-time loss without debasing reliability.

The proposed 3-level converter is implemented using only thin-oxide NMOS devices for all four power switches with a 0.35 μm low-voltage BCD process. Finally, the measurement results of the proposed design are provided to successfully verify the functionality.

Chapter 3 first reviews the design challenges of the multiphase DC-DC converter, which especially requires fast transient response and wide-load-range efficiency for mobile application processors. The principle of the proposed adaptive window hysteretic control is then addressed, which fundamentally elevates the function of the hysteretic window and largely improves load transient performance of the hysteretic control. To facilitate the adaptive window hysteretic control in multiphase converters, a synchronized adaptive window (SAW) hysteretic control is introduced with fixed frequency, which evolved from the adaptive window control. To realize an extended power saving feature, dynamic voltage scaling, in the application processors, a wide range of the programmable V_O in the SAW control is presented. The system architecture of the proposed multiphase DC-DC converter is addressed with the principle and implementation of 1-Cycle APC, accomplishing adaptive phase count within one switching cycle. The proposed converter is fabricated in a 0.35 μm CMOS process. Finally, the experimental results of the proposed design are provided to verify the functionality.

In Chapter 4, the system requirements of the compact low-power mobile devices are firstly reviewed. Next, the control design challenges for these mobile applications are then introduced, including a fixed switching frequency, high V_O regulation, fast transient, and wide-V_{IN} operation. In addition, to support the mode transition, active/sleep, in the mobile application, the low f_{SW} mode has to be implemented to save power. A wide V_{IN} supply is also essential for the battery-operated system. Integrating all these features together is thoroughly challenging without

increasing the design complexity and degrading the system performance. The principle of the double adaptive bound (DAB) control is presented, which fundamentally elevates the function of the hysteretic window with real-time slope-tracking reference and thus achieves a fixed switching frequency. To further improve the power density, the proposed controller upgrades the V_O load regulation without using of the compensation network. The proposed converter with the autonomous mode manager (AMM) is introduced, accomplishing further improved transient performance and light-load efficiency through installing four modes. Next, each mode operation is described in detail. Finally, the converter is designed and fabricated with a 0.18 μm CMOS process, and the measurement results successfully verify the functionality and performance of the design.

Finally, Chapter 5 concludes this dissertation with a summary of the research contributions and a discussion of the future research directions.

CHAPTER 2

WIDE-INPUT 3-LEVEL GATE DRIVER WITH BOOTSTRAP AND DEAD-TIME CONTROL FOR ALL-NMOS POWER SWITCHES

In this chapter, the wide-input 3-level converter is addressed to minimized system-level power distribution plan in the battery-operated mobile applications. The benefits of the 3-level converter are first reviewed in Section 2.1, followed by the design challenge of the 3-level converter to improve power efficiency under varied input supply. In Section 2.2, the proposed gate driver architecture for all-NMOS 3-level converter is introduced. In addition, the precise sub-ns dead-time control strategy is proposed, which is integrated in the gate buffer stage, minimizing the dead-time power loss without sacrificing reliability. In Section 2.3, the circuit level implementation of the proposed 3-level converter is described. Isolated bootstrap scheme for high-side NMOS power switch and an interception coupling dead-time (ICDT) technique is also addressed. Finally, experimental results of the proposed design are provided in Section 2.4 to successfully verify the functionality and performance.

2.1 Overview of the Design Challenges in the 3-level DC-DC Converter

Recently, the 3-level DC-DC converter has been reported with inherent merits to integrate the voltage regulator on-chip [Godycki-14, Kim-11, Liu-15, Shi-13, Villar-08, and Yousefzadeh-06]. Figure. 2.1 illustrates the power system comparison between the conventional buck and 3-level buck converters. First, the voltage swing of the 3-level converter is half that of the buck converter, reducing the switching power loss by half. Furthermore, this half voltage swing facilitates the V_{IN} to be twice that of the device breakdown voltage, allowing the energy sources to

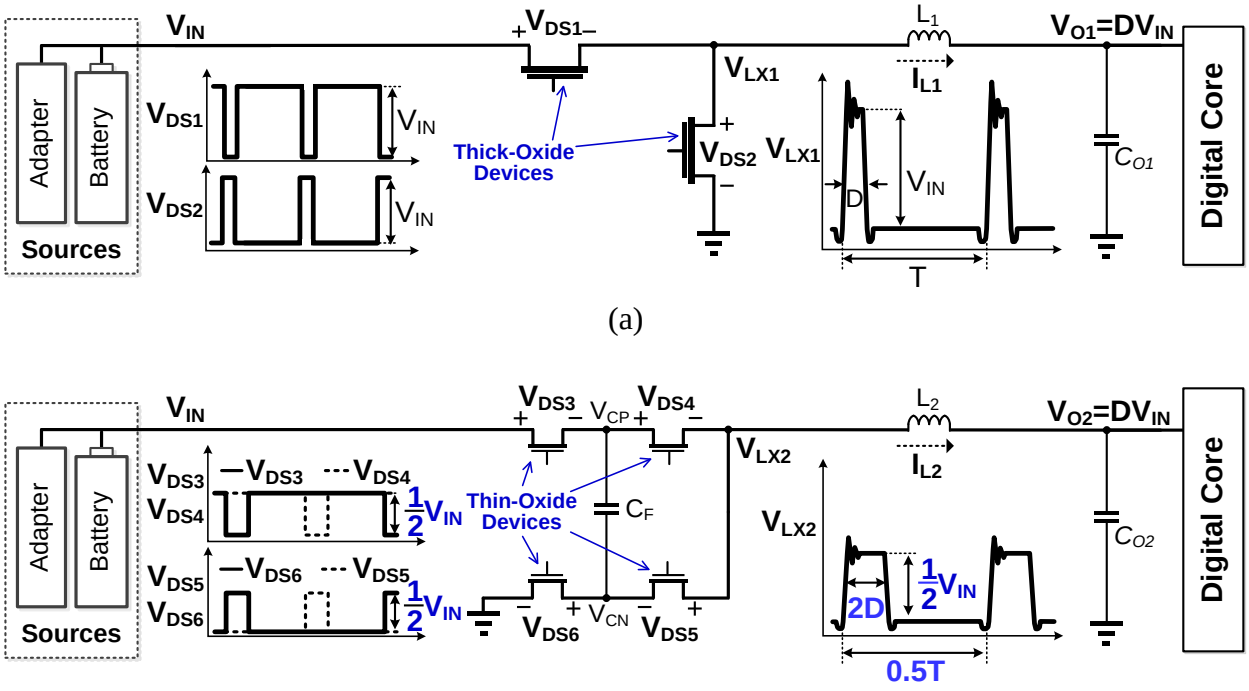


Figure 2.1. System architecture comparison: (a) conventional buck and (b) 3-level converter.

connect directly while using a thin-oxide device. Comparing the thick-oxide device with the same on-resistance (R_{ON}), the thin-oxide device has merits of the higher carrier mobility and lower gate-oxide capacitance, reducing chip area and gate-driving loss. If employing the thick-oxide device which has high breakdown is employed, the system loses inherent benefits of modern technologies with small gate capacitance and silicon area. Furthermore, the passive components can be reduced due to the half inductor current (I_L) swing.

However, despite these advantages, the reported 3-level converters do not have enough power efficiency [Godycki-14, Kim-11, and Liu-15]. In these state-of-the-art converters, 77% of the power efficiency is the best result with above 10 MHz of f_{SW}. Regarding the power stage design, the previous 3-level converters implemented stacked P-type MOSFETs for high-side switches and

stacked N-type MOSFETs for the low-side switches. With the same R_{ON}, the P-type switches consume more than four times the silicon area, gate capacitance, and switching power loss, compared to the corresponding N-type switches because the majority carriers of the N-type device have a higher mobility than that of the P-type device. If the high-side switches are replaced by the stacked N-type devices, all of the power switches are employed by the N-type devices and the topology improves power and silicon efficiency. Moreover, another bottleneck to implementing the power stage is using the varying voltage of the energy sources. As the previous studies implemented the power stage by using a fixed supply voltage, another power converter was mandatory, degrading the system efficiency. Developing the 3-level converter with the all N-type switches and high switching operation requires special cares to design a robust bootstrap gate driver because: 1) the operating range of the source node of the highest switch is from half V_{IN} to V_{IN}, 2) the R_{ON} of the power switches increases when the gate driving voltage is not sufficient [Streetman-00], and 3) increased f_{SW} imposes stringent stress on achieving reasonable propagation delay and dead-time control in the gate drivers. Due to the reduced V_O near the diode forward voltage, the converter increases the dead-time loss and diode reverse recovery loss [Mappus-03]. For example, when designing the power converter that operates in 0.4 V of V_O and 5 V of V_{IN} at 20 MHz, the on-time must be extremely narrowed down to 2ns. Therefore, the non-overlapped time should be controlled under the sub-ns range. However, the conventional dead-time controller has delay variation, which can be larger than nanosecond level, and thus suffers from extra power loss or the shoot-through issue.

Hence, to enhance the efficiency benefit of the 3-level converter, the all-NMOS 3-level converter with thin-oxide devices for power switches is proposed, which can optimize the power

loss even when operating at high f_{SW}. To handle the converter from varied V_{IN} directly, the proposed converter employs bootstrapped gate drivers with constant driving voltage (V_{DRV}), which can sustain the low R_{ON} and conduction loss. In addition, to control dead-time under sub-ns range without sacrificing reliability, the interception coupling dead-time (ICDT) technique is proposed, which can reduce both gate-driving and dead-time power losses.

2.2 Proposed Gate Driver

2.2.1 Gate Driver Strategy

Prior to presenting the proposed all-NMOS 3-level gate driver, the detail operation of the conventional 3-level buck converter will be discussed to provide a better understanding of the requirements and challenges to design the gate driver with varying V_{IN}. The power stage for the converter and its detailed operating waveforms are shown in Figure 2.2. The 3-level converter consists of four power switches ($M_{1\text{-}4}$) and their corresponding gate drivers, a flying capacitor C_F, and the output filter (L, C_O). The 3-level converter can generate three different output voltages

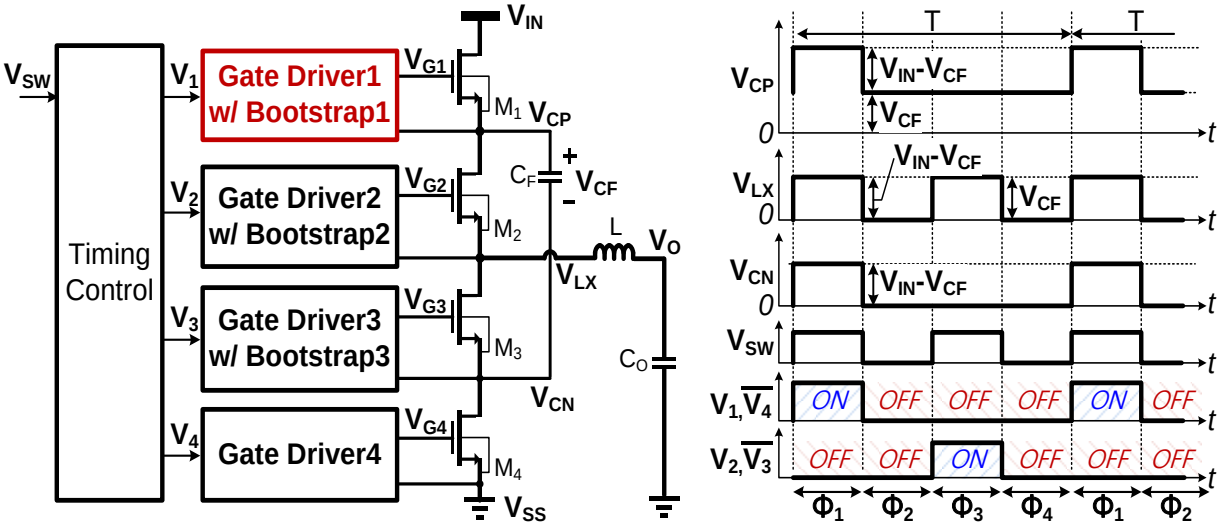


Figure 2.2. Block diagram of the power stage for the all-NMOS 3-level converter and its operating waveforms.

(V_{IN}, $0.5V_{IN}$, and V_{SS}) and has two different operating modes depending on the duty cycle ($D = V_O/V_{IN}$) [Kim-11]. The D is always lower than 0.5; thus, we only considered one operating mode, in which the output voltage switches from $0.5V_{IN}$ to V_{SS}. In this mode, the 3-level converter operates 4 phases ($Ø_{1\text{-}4}$) in one switching cycle (T), and the power switches turn on/off properly by the gate driver inputs ($V_{1\text{-}4}$) in each phase. At $Ø_1$, M_1 and M_3 turn on; thus, the switching node (V_{LX}) is connected to the negative node of the C_F (V_{CN}), i.e., $V_{LX} = V_{IN}–V_{CF}$. At $Ø_3$, M_2 and M_4 turn on and the V_{LX} is connected to the positive node of the C_F (V_{CP}) (i.e., $V_{LX} = V_{CF}$). Assuming the ideal case where V_{CF} is the same as $0.5V_{IN}$, V_{LX} remains $0.5V_{IN}$ in $Ø_1$ and $Ø_3$. Unlike the conventional buck converter, which has one switching node and swings from V_{IN} to ground, the 3-

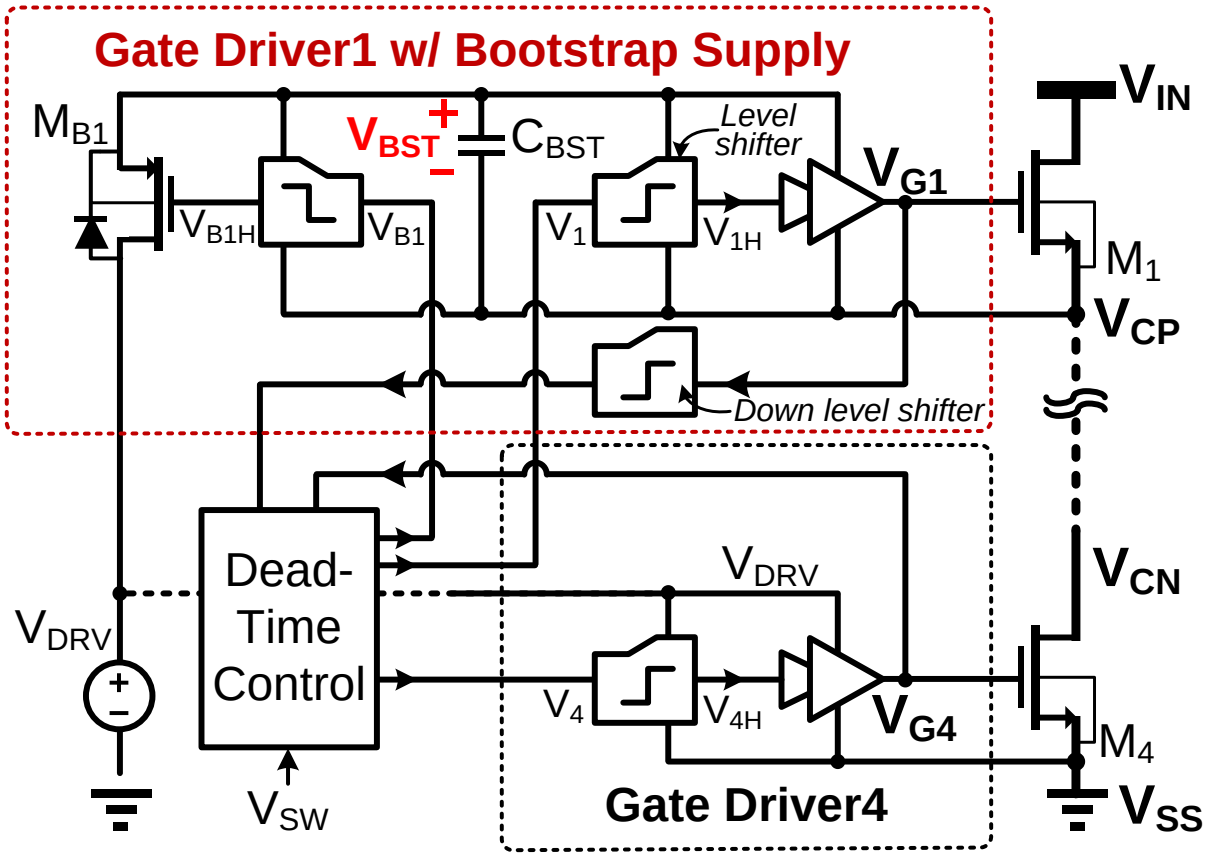


Figure 2.3. Conventional gate driver with the bootstrap power supply.

level converter has three switching nodes, each of which has a different swing range, as shown in Figure 2.2. The V_{CP} and V_{CN} switching depends on the converter's operating phase: the swing range of V_{CP} is from V_{IN} to $0.5V_{IN}$, and that of V_{CN} is from $0.5V_{IN}$ to ground. With this different swing range and varied supply V_{IN}, the driving voltage (V_{DRV}) of the power switch needs to be considered when designing the gate driver to prevent increasing R_{ON}, which in turn increases conduction loss.

Conventionally, to operate the N-type high-side device, the bootstrap power supply technique is applied to the gate driver due to the benefits of the simple and low cost. The bootstrap circuit includes a bootstrap capacitor (C_{BST}), a switch (M_{B1}), and a level shifter to control the M_{B1}, as illustrated in Figure 2.3. Instead of using a bootstrap diode, the M_{B1} is utilized to eliminate the diode voltage drop in V_{BST}. This scheme requires a time interval between the M_{B1} and power switches $M_{1\text{-}4}$ to prevent the shoot-through current. When the source node of the M_1, V_{CP}, goes below V_{IN} or is pulled down to low voltage, the C_{BST} charges through the M_{B1} from the gate driving voltage, V_{DRV}, providing the bootstrap supply voltage V_{BST}, i.e.,

$$V_{BST} = V_{DRV} - V_{CP} . \tag{2.1}$$

Then, when the high-side switch turns on and pulls to a higher voltage, the V_{BST} floats, and the M_{B1} turns off and blocks the rail voltage from V_{DRV}.

To develop the gate drivers for M_2 and M_3, this bootstrap technique can be applied because their source nodes (V_{LX} and V_{CN}, respectively) can go down to V_{SS}, as in the buck converter, enabling the V_{BST} to charge as much as V_{DRV}. However, the bootstrap technique requires additional consideration to drive the M_1 due to the V_{CP} swing range from V_{IN} to $0.5V_{IN}$, which is always higher than half V_{IN}, as shown in Figure 2.2. As mentioned before, the 3-level converter generally uses

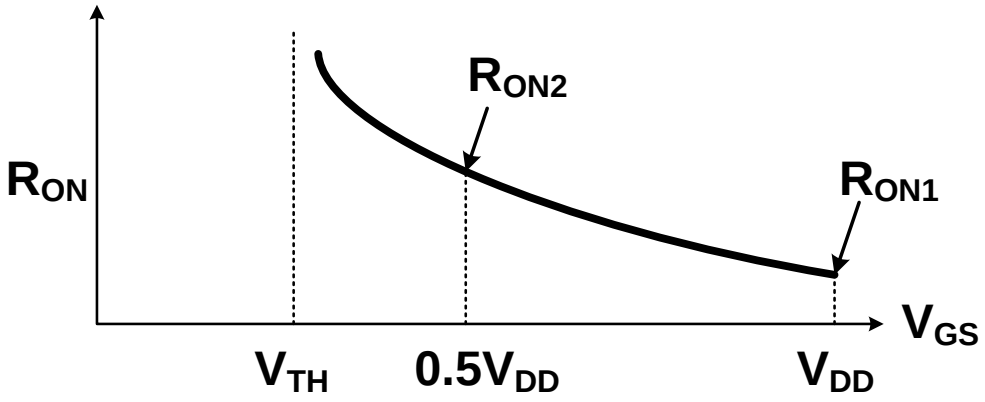


Figure 2.4. The MOSFET R_{ON} versus V_{GS}.

the thin-oxide device for the power switches, and the switch breakdown and the V_{DRV} are half of the maximum V_{IN}. Accordingly, V_{BST} for the M_1 gate driver cannot be fully charged as much as V_{DRV}, expressed as Equation (2.1). Furthermore, if we consider the lower V_{IN} condition, this charging problem is more obvious. For example, let's assume the maximum V_{IN} is 6 V and V_{DRV} is 3 V. Since the low voltage of the V_{CP} (=0.5V_{IN}) equals the V_{DRV}, the V_{BST} cannot charge and turn on the M_1 due to V_{BST} = 0 V. One feasible approach is applying the different driving voltage source, such as V_{IN}, for the M_1 gate driver [Kim-11]. However, under the varied V_{IN}, V_{BST} has an insufficient driving voltage issue. If V_{IN} is reduced to 3V, the V_{CP} swings from 3 V to 1.5 V; thus, the V_{BST} is only 1.5 V, expressed as Equation (2.1). As shown in Figure 2.4, the R_{ON} of the power switch is related with the V_{GS}, and the equation is demonstrated as:

$$R_{ON} = \frac{1}{\mu C_{OX} \frac{W}{L}\left(V_{GS} - V_{TH}\right)}. \tag{2.2}$$

Assuming that V_{TH} is 0.7 V and V_{GS} is the same as the V_{BST}, the R_{ON} at 3 V of V_{IN} (R_{ON2}) is 2.9 times larger than that at 6 V of V_{IN} (R_{ON1}), i.e., R_{ON2} = 2.9×R_{ON1}, as shown in Figure 2.4. Hence, while the V_{IN} is reduced in the portable device, the conduction loss is increased, accelerating the

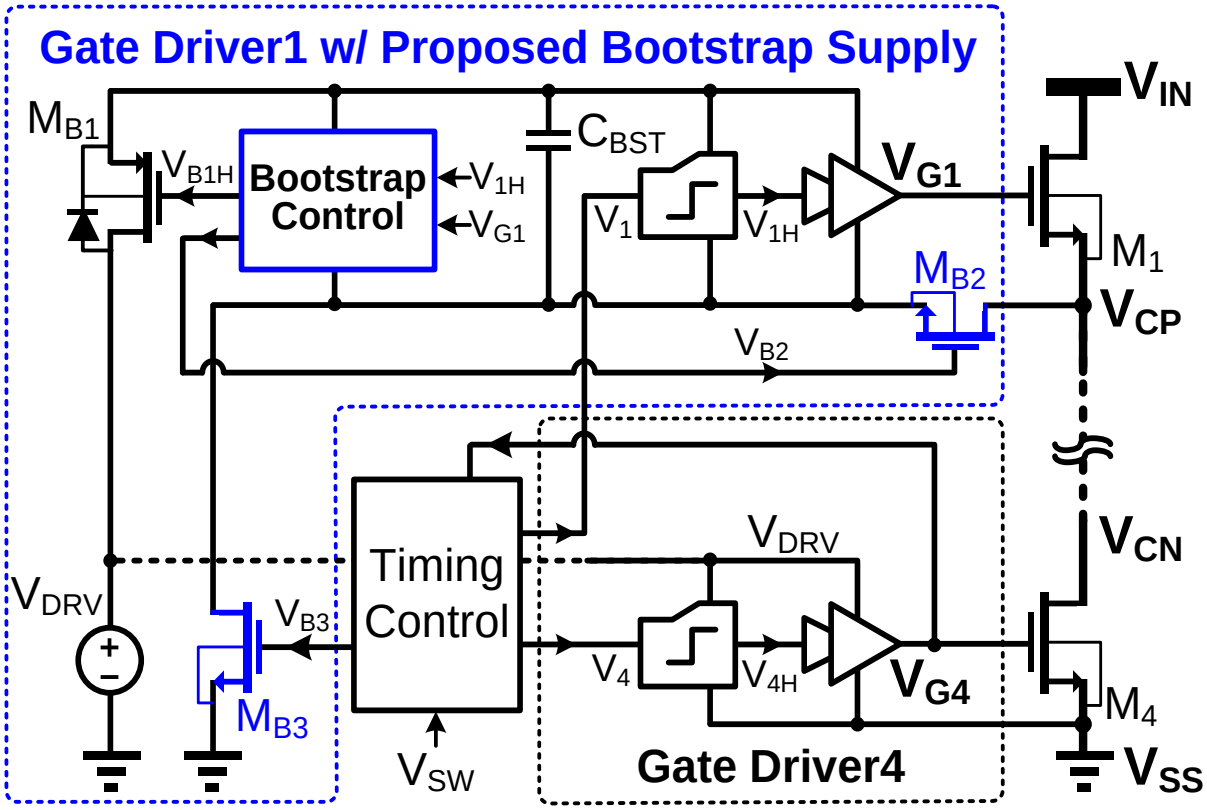


Figure 2.5. Proposed system architecture for All-NMOS 3-level gate driver.

power consumption. Moreover, this R_{ON} variation occurs only for the M_1 gate driver, creating the R_{ON} mismatch with other power switches ($M_{2\text{-}4}$). Since maintaining the V_{CF} at half V_{IN} is important in the 3-level converter, this mismatch has to be minimized.

To overcome these issues, a gate driver for the high-side power switch M_1 is implemented with the proposed isolated bootstrap power supply circuit as shown in Figure 2.5, which is not affected by V_{IN} variation. The proposed bootstrap circuit includes three switches ($M_{B1\text{-}3}$), and a bootstrap control. As in the traditional bootstrap supply circuits, the M_{B1} is utilized to remove the diode voltage drop. However, instead of using a level shifter to control the bootstrap circuit with the non-overlap time, the bootstrap control signal can be generated by sharing the gate driver

control signal V_{1H} due to the proposed dead-time controller. As fewer level shifters are utilized, the proposed gate driver helps to reduce the C_{BST} and the total power consumption. The detailed operation will be described later with the proposed dead-time control method. To ensure that V_{BST} can be fully charged to V_{DRV}, the proposed bootstrap circuit employs M_{B2} and M_{B3} to isolate the

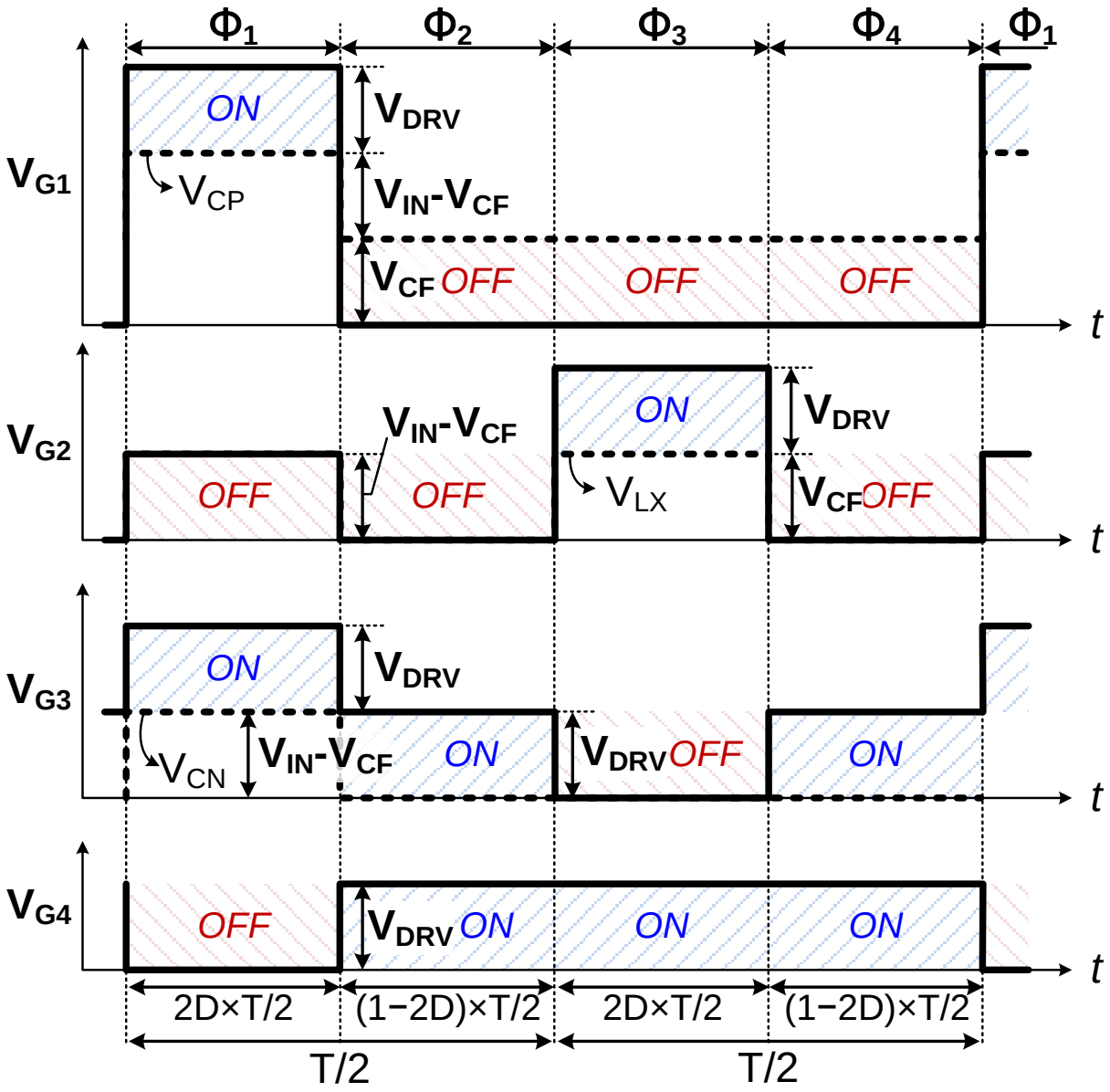
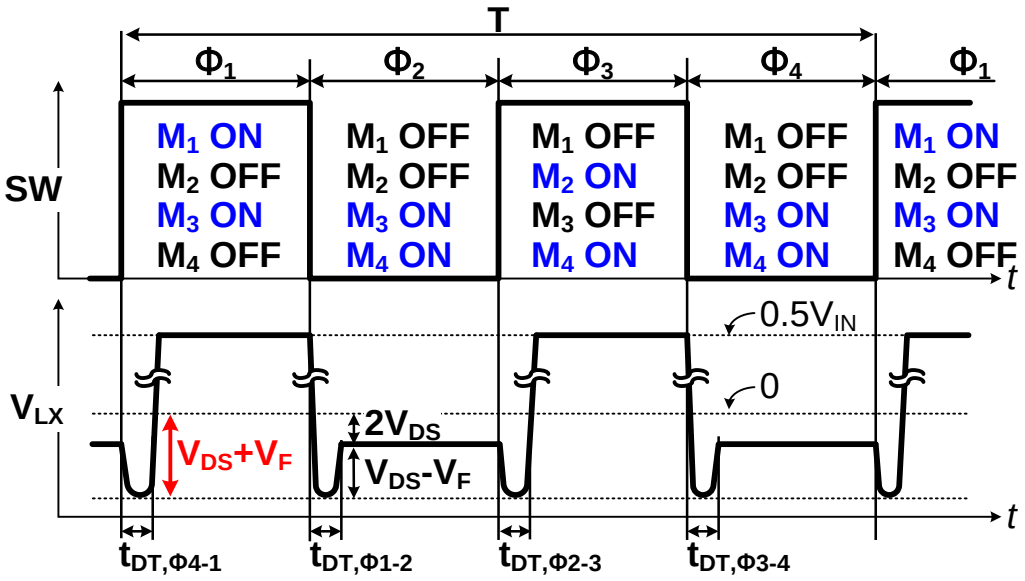
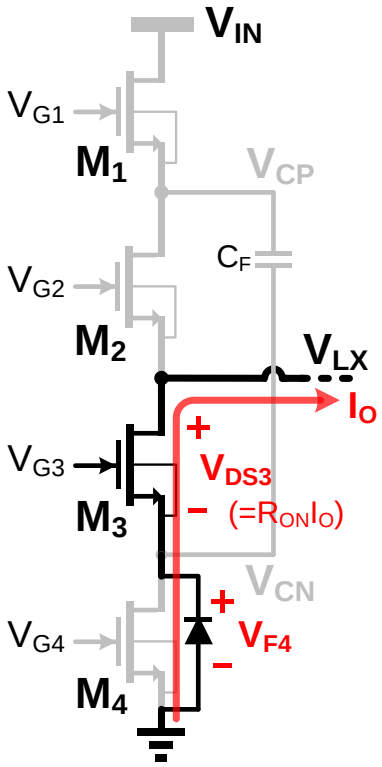


Figure 2.6. Operation waveforms of the gate nodes for each driver.



(a)



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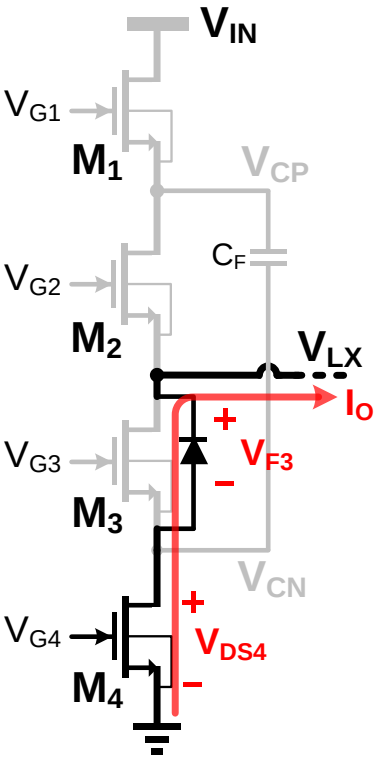


(c)

Figure 2.7. The switching and dead-time operation in the 3-level converter: (a) operating waveforms, (b) switches operation during $t_{DT,\Phi4\text{-}1}$ and $t_{DT,\Phi1\text{-}2}$, and (c) switches operation during $t_{DT,\Phi2\text{-}3}$ and $t_{DT,\Phi3\text{-}4}$.

negative node of the C_{BST} (V_{BS}) from V_{CP} during the charging period. The detailed operating voltage of each gate driver is shown in Figure 2.6.

2.2.2 Dead-time Control Strategy

A precise dead-time controller with minimized delay is mandatory to improve efficiency and robustness, especially for the 3-level converter. The operating waveforms and the switch operation during the non-overlap period are shown in Figure 2.7. Unlike the conventional buck converter, which has two phases (turn-on/-off) in one T, the 3-level converter has four phases, facilitating a smaller output ripple and filter size. However, due to this double switching, power loss has to be considered: Although the switching power loss (P_{SW}) of the 3-level converter equals that of the buck converter due to the half voltage swing, (i.e., $P_{SW} = 1/2 \times 0.5 V_{IN} \times I_O \times 2 f_{SW}$), the dead-

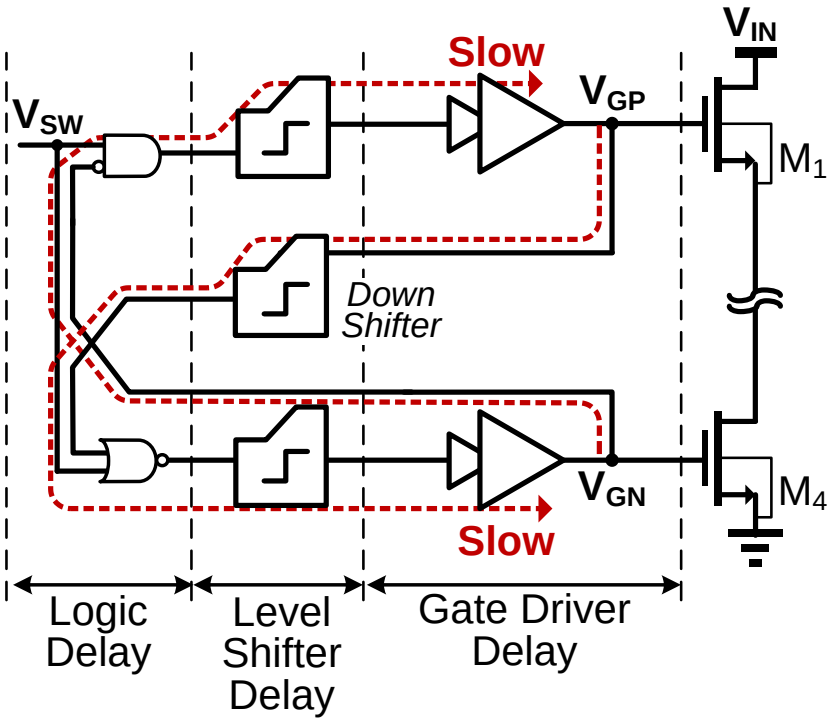


Figure 2.8. Block diagram of the previous dead-time controller.

time conduction loss (P_{DT}) is increased. Moreover, since the output supplying current always passes two switches, the conduction loss during the dead-time is increased as:

$$P_{DT} = (V_F + R_{ON} I_O) \times I_O \times f_{SW} \times \left(t_{DT1} + t_{DT2} + t_{DT3} + t_{DT4}\right). \tag{2.3}$$

Besides, due to the V_O scaling trend, P_{DT} in the total power loss is increased [Mappus-03]. Therefore, the dead-time must be reduced under the sub-ns range. In [Song-15], an active dead-time control scheme was designed for narrow dead-time generation to detect the voltage of the switching node and adapt accordingly, as shown in Figure 2.8. This approach, however, inherently suffers from the propagation delays of the level shifter and logic gates. The predictive dead-time control is one possible solution to achieve the sub-ns range of the dead-time due to the feedback and timing control scheme [Mappus-03]; however, this approach requires

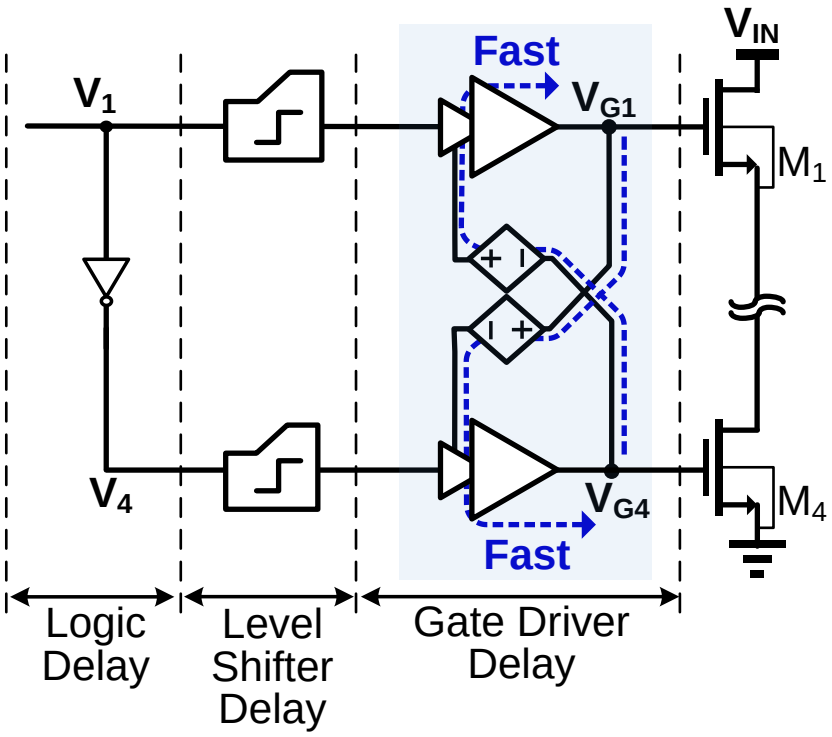


Figure 2.9. Block diagram of the proposed ICDT controller.

many trimming bits for precise control, consuming a large area and additional power. Also, since the speed of this scheme is limited by the loop bandwidth, the scheme cannot be employed for applications that require fast load transient.

To reduce the dead-time further, the interception coupling dead-time (ICDT) controller with a pseudo-voltage source is proposed in Figure 2.9. Instead of sensing and inserting the interval time in the timing control block (before the level shifter block), the proposed scheme propagates the control signal to the two gate drivers, which need to switch to the converter phase. Unlike the conventional dead-time control scheme, this control signal is simultaneously transmitted to the gate drivers through level shifters. While the gate driver that receives the off-signal directly turns off the power switches, the gate driver that receives the on-signal turns on when it senses the gate off-signal from the opposite side. Meanwhile, the proposed ICDT scheme intercepts the gate off-signal from the opposite side of the power switch directly by using the pseudo-voltage source, conveys the captured signal to the gate driver, and finally turns on the power switch. Following this process, any delay in digital logic and the level shifter This course thereby eliminates any delay in the digital logic and level shifter is eliminated in the dead-time control path, achieving the dead-time within the sub-ns delay adaptively and increasing the power efficiency without any reliability issue. In addition, since the ICDT scheme creates an inherent time interval between the gate on and off signals after the level shifter stage, the bootstrap control signal for the proposed bootstrap supply circuit (Figure 2.5) can be utilized by using the gate on/off signals in the high-voltage domain without additional level shifters.

2.3 Circuit Implementation

2.3.2 Gate Drivers with the Bootstrap Power Supply

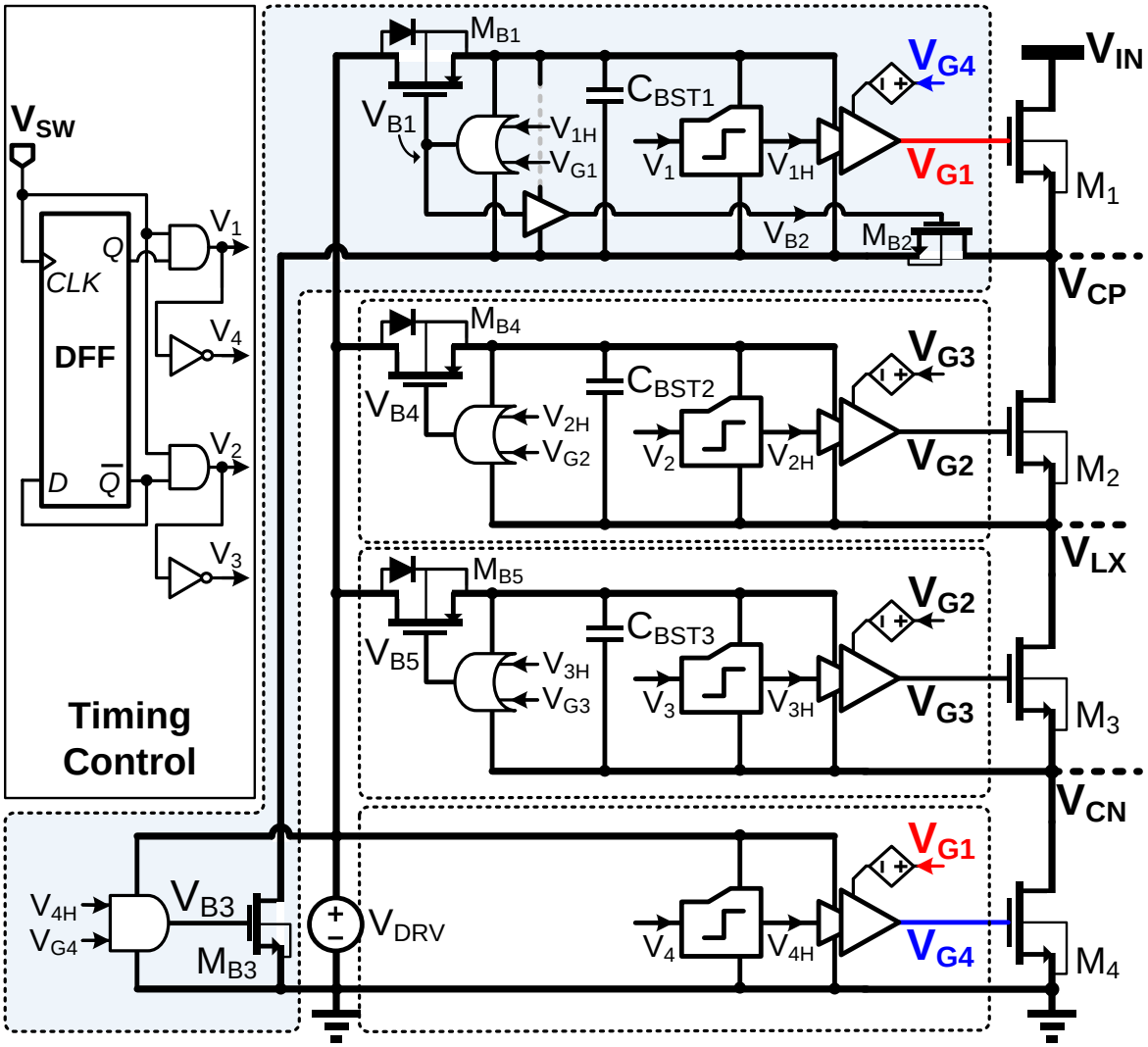


Figure 2.10. The circuit implementation of the proposed All-NMOS 3-level gate driver with bootstrap supply.

The circuit implementation of the all-NMOS 3-level gate drivers is proposed as illustrated in Figure 2.10, which has the same power stage as Figure 2.2(a). Basically, each gate driver is composed of a level shifter and a buffer stage including the proposed ICDT technique. The gate drivers for driving $M_{1\text{-}3}$ further consists of the bootstrap power supply circuit (C_{BST}, M_{Bx}), and for M_1, in particular, the circuit is comprised of three switches ($M_{B1\text{-}3}$) and their corresponding control logics without additional level shifters. $M_{B1\text{-}3}$ can be controlled by buffer signals located in their

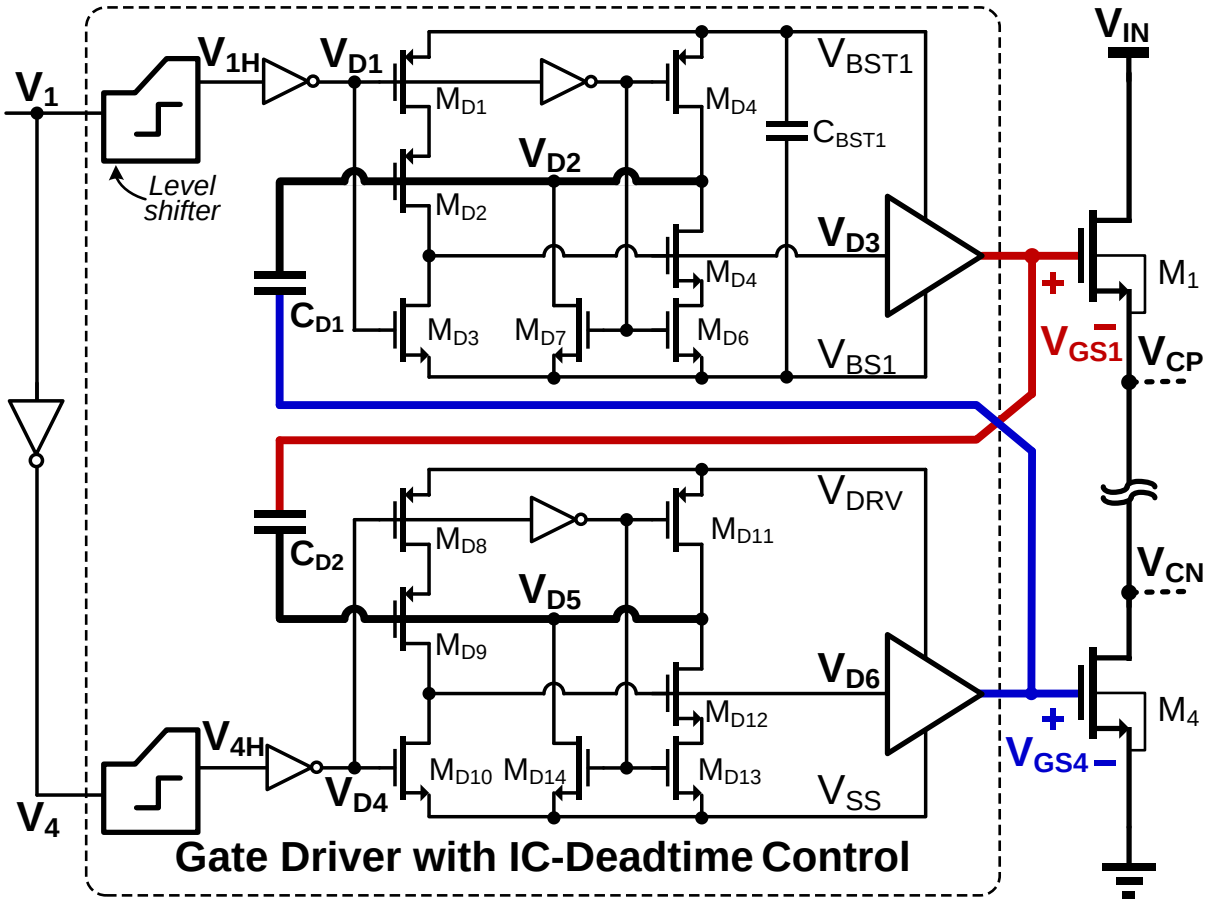


Figure 2.11. The circuit implementation of the gate drivers with ICDT controller.

respective voltage domains. For example, the buffer signals for M_1 can be used to control M_{B1} and M_{B2}, while the buffer signal for M_4 can be used to control M_{B3}. Moreover, to control the power switches, the timing control employed by logic gates (in Figure 2.10) receives a switch on/off signal (V_{SW}) and generates the phase control signal ($V_{1\text{-}4}$) in the low-voltage domain as shown in [Reusch-09].

2.3.2 Gate Driver with the ICDT Controller

The detail circuit implementation of the proposed ICDT controller is illustrated in Figure 2.11. To control the dead-time within the sub-ns range, the proposed dead-time controller,

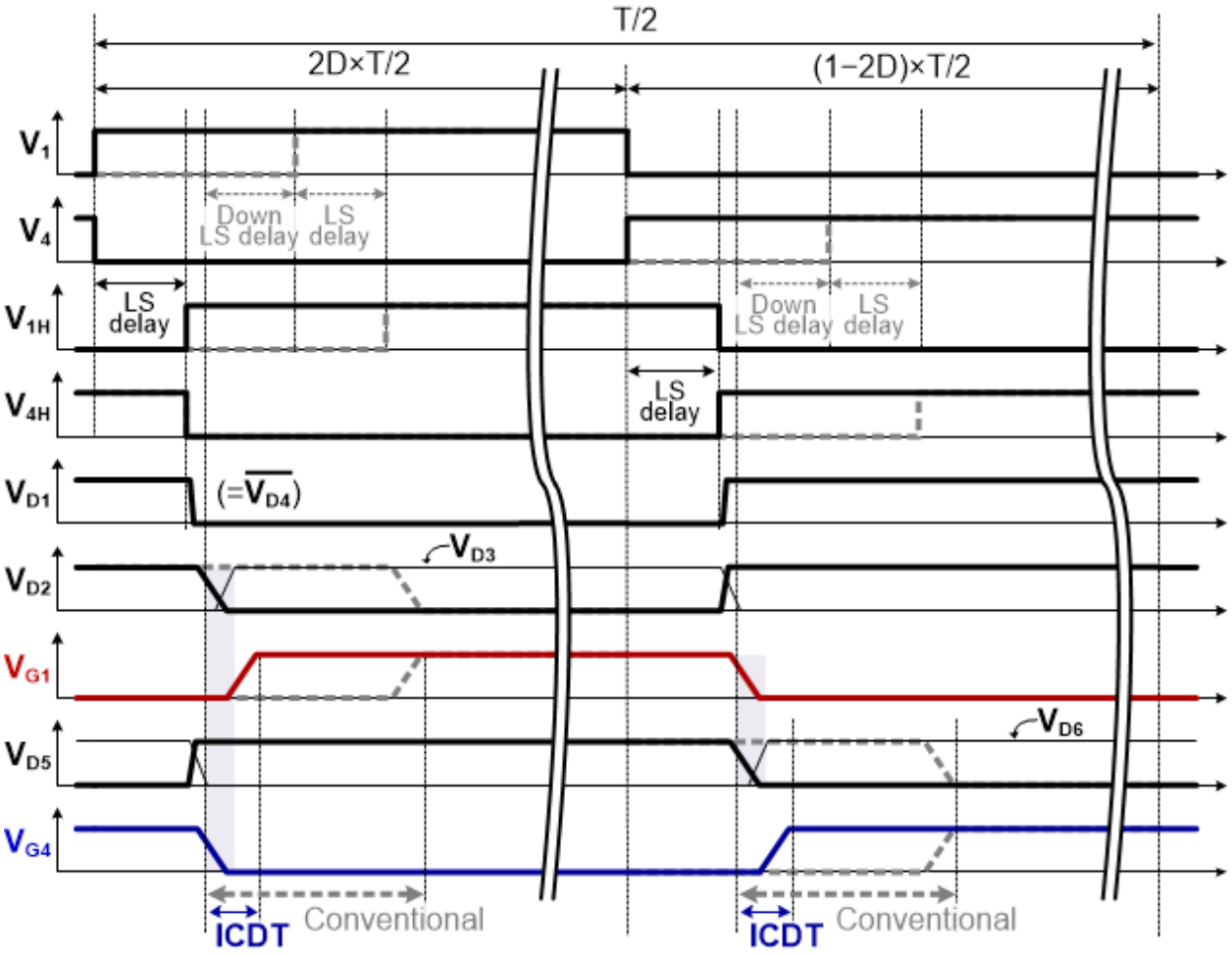


Figure 2.12. Detailed operation waveforms of the ICDT controller.

consisting of a capacitor (C_{D1}) and a latch circuit ($M_{D1\text{-}7}$), is integrated in the beginning of the buffer stage, where a small circuit size is required to reduce the dynamic current. This reduces the propagation delay from level shifters. Then, by using a C_{D1} and a capacitor coupling technique, the turn-off signal from the opposite gate driver is transferred to the latch, eventually turning on the power switch. Thus, the dead-time can be managed by the buffer stage delay, which has the sub-ns range. This latch circuit operates in an asymmetric manner: 1) when it receives the turn-off signal, the V_{D2} goes high and turns off the power switch, and 2) when it receives the turn-on signal,

the V_{D2} and V_{D3} are changed to the floating node, making it easy to receive the coupled voltage from C_{D1}. Thanks to the configuration of the all-NMOS power switches, which has the same high/low signal to turn-on/off the switch, the same ICDT circuit can be implemented for all gate drivers, facilitating less design effort. Since the two pairs of gate drivers in the 3-level converter operate in a complementary manner, alternating every half T as shown in Figure 2.7, this section will explain the dead-time controller with only one pair of gate drivers to provide a basic understanding.

The detailed operation waveforms are shown in Figure 2.12. At the beginning of the switching cycle (transits from $Ø_4$ to $Ø_1$), V_1 transitions to high and V_4 goes low simultaneously. These signals pass through each side of the level shifter with the propagation delay. For the high-side gate driver, which receives the turn-on signal, V_{D1} goes low, turning off the M_{D3} and M_{D4}. Due to the cross-coupled connection, M_{D2} and M_{D4} have been turned off, and V_{D2} and V_{D3} follow the previous states, which are high and low, respectively, latching until C_{D1} detects the falling edge of V_{GS4}. Meanwhile, for the low-side gate driver, which receives the turn-off signal, V_{D4} goes high (opposite from V_{D1}), and M_{D10} and M_{D11} turn on, decreasing V_{D6} and V_{GS4} directly without waiting for the rising edge of V_{GS1}. Once the falling edge of V_{GS4} is detected through C_{D1}, V_{D2} decreases and turns on M_{D2}, pulling high V_{D3} and turning on V_{D4} as well. Due to the feedback loop in the latch, the V_{D3} quickly increases to turn on M_1, minimizing the logic propagation delay. Compared to the conventional dead-time controller, the proposed scheme has much shorter delay as shown in Figure 2.12, helping to reduce the dead-time power loss. In the next phase ($Ø_2$), the ICDT controller operates in a complementary manner. In addition, a small switch M_{D7} is inserted to pull down V_{D2} to trigger the latch reliably when all the power switches ($M_{1\text{-}4}$) are in a turn-off configuration (e.g.,

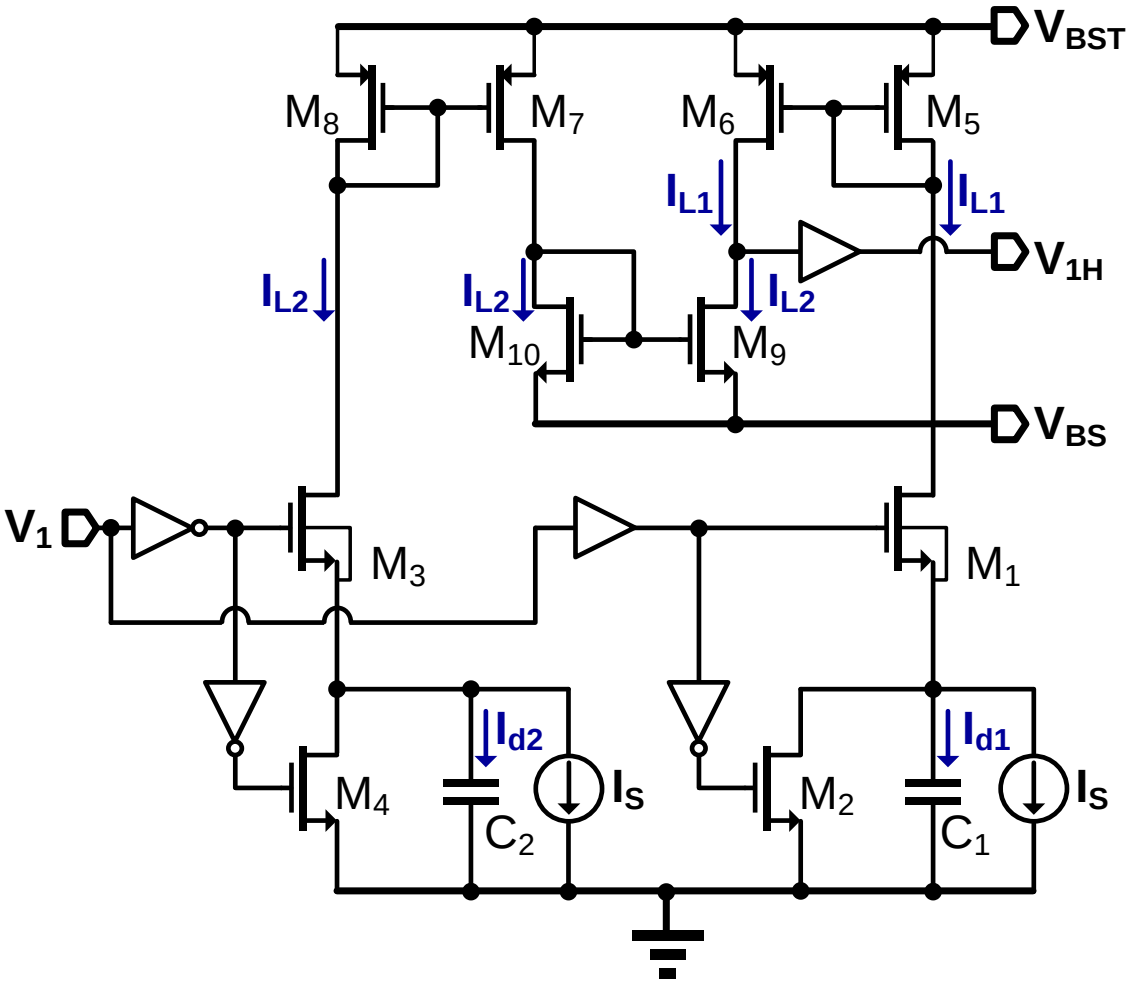


Figure 2.13. The circuit implementation of the high-speed rail-to-rail level shifter.

stand-by mode). The pull-down speed of M_{D7} is more than ten times slower than f_{SW}; thus, it does not affect the normal switching operation.

2.3.3 High-Speed Rail-to-Rail Level Shifter

To implement an all-NMOS 3-level buck converter with low conversion ratio and high f_{SW}, a high-speed level shifter is required. In general, the level shifter is dominant in determining the delay of the gate driver. Nevertheless, the conventional level shifter has a propagation delay up to 10 ns, which is not favorable in a high f_{SW} operation. At the same time, a dynamic level shifter

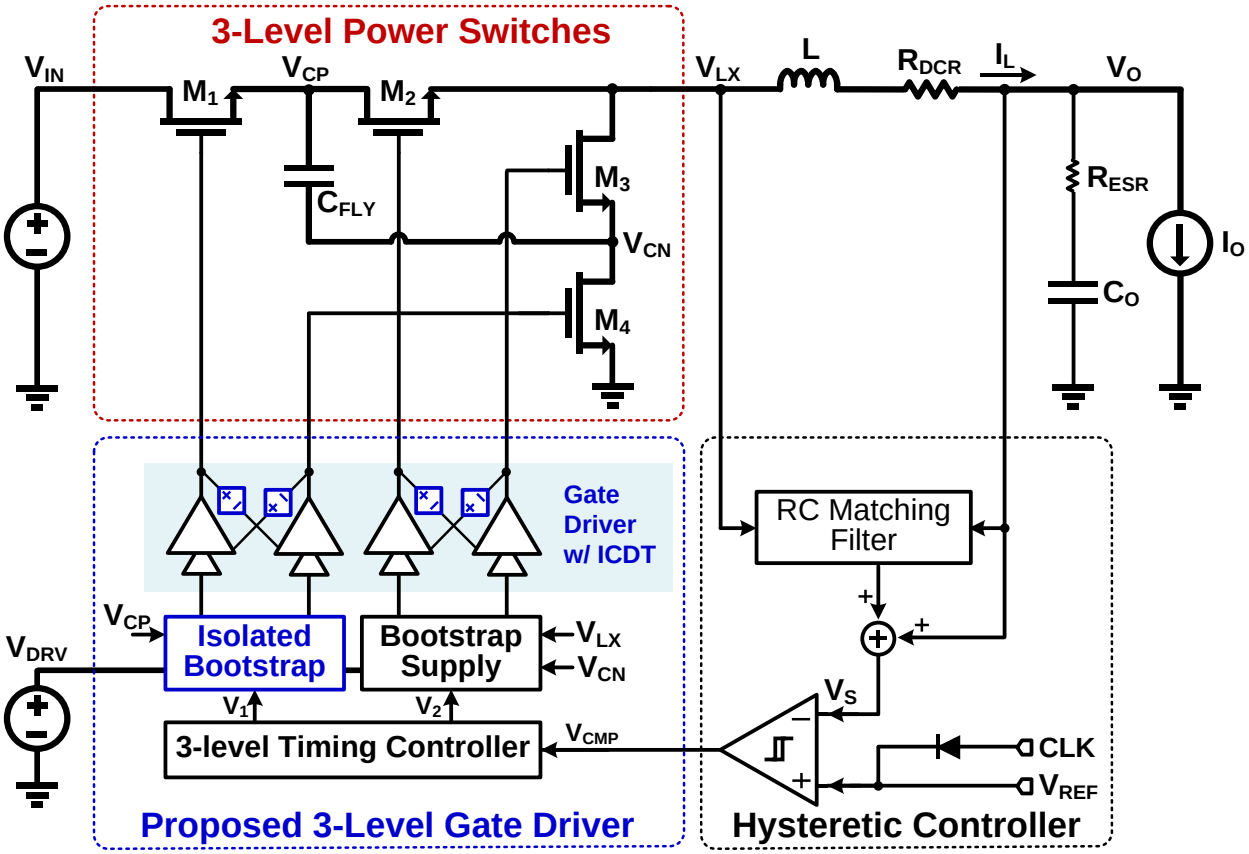


Figure 2.14. Circuit block diagram of the proposed 3-level power converter.

[Song-15] has much faster transient response; however, this application is limited only to a relatively high voltage domain. To mitigate this problem, a high-speed rail-to-rail level shifter is proposed to directly achieve a full-swing output voltage and short delay (Figure 2.13). During the turn-on period ($Ø_1$, $Ø_3$), when V_1 cycles to high, a large dynamic current, I_{d1}, is mirrored in I_{LS1}, which increases the output of the level shifter, V_{1H}, to achieve dramatically fast level shifting. I_{d1} is preserved until V_{GS} of M_1 falls below the threshold voltage by charging up the capacitor, C_1. Considering that I_{d1} only occurs during the transition of the gate driving signal, the average power consumption of the gate driver is minimized. Furthermore, the proposed design replaces the source

follower circuit in [Reusch-09] with a current-mirror structure, releasing maximum output voltage swing to supply voltage.

2.3.4 Full System Implementation

The converter's circuit block implementation is illustrated in Figure 2.14, which contains the 3-level power switches with output filter, a hysteretic controller, and a proposed 3-level gate driver. The driver includes four gate drivers with the proposed ICDT scheme, bootstrap supplies, and a 3-level timing controller. This timing controller distributes the control signal V_{CMP} to corresponding gate drivers. And, the hysteretic controller is employed to regulate the output with clock synchronization scheme for achieving constant f_{SW}.

2.4 Experimental Results

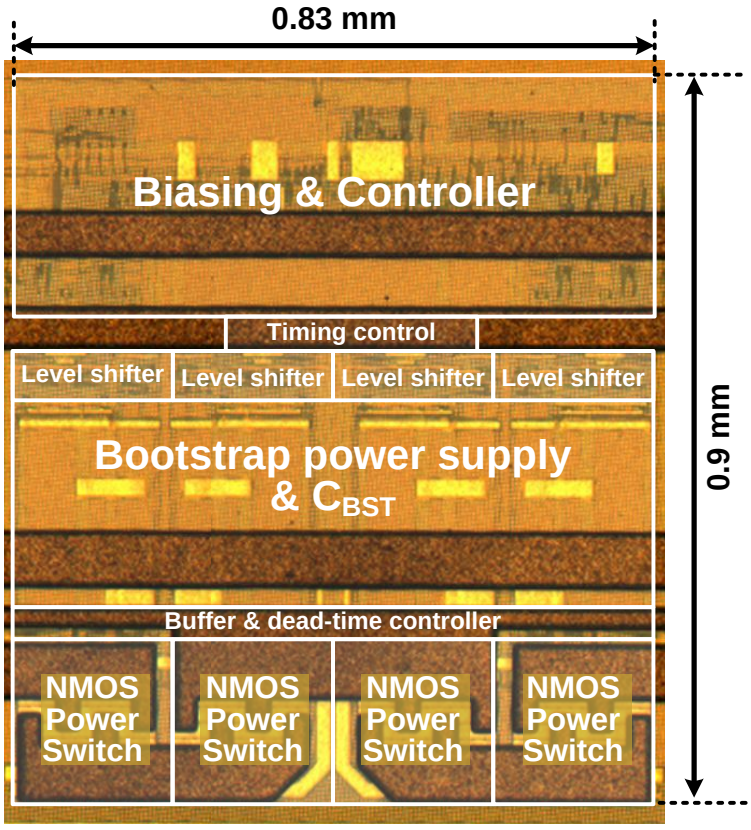


Figure 2.15. Chip micrograph.

The proposed 3-level converter, using only NMOS for all four power switches, is fabricated in a 0.35 µm BCD process with an active area of 0.75 mm^2 as shown in Figure 2.15. The converter is targeted to operate at a switching frequency of 20 MHz with an inductor of L=72 nH. The value of the output capacitor C_O is 2.2 µF, and the flying capacitor (C_F) is 100 nF. For the bootstrap power supply circuits, the bootstrap capacitors ($C_{BST1\text{-}3}$), each with 400 pF, are integrated in the chip. The converter operates under the variable V_{IN} from 3 V to 6 V, and the V_O is programmable from 0.4 V to 1.6 V with a maximum load current of I_O=0.5 A.

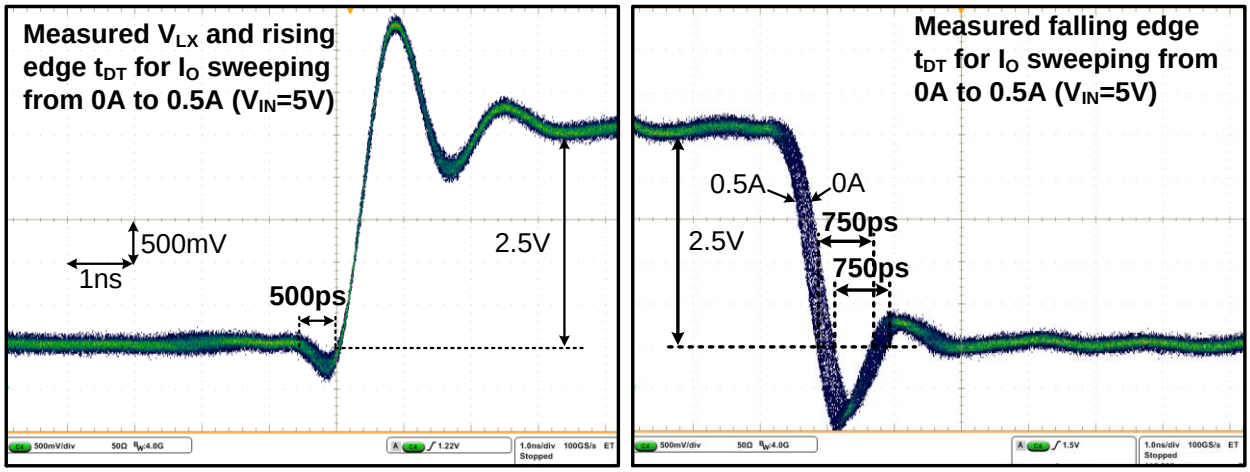


Figure 2.16. Measured switching behavior of the gate driver with ICDT controller.

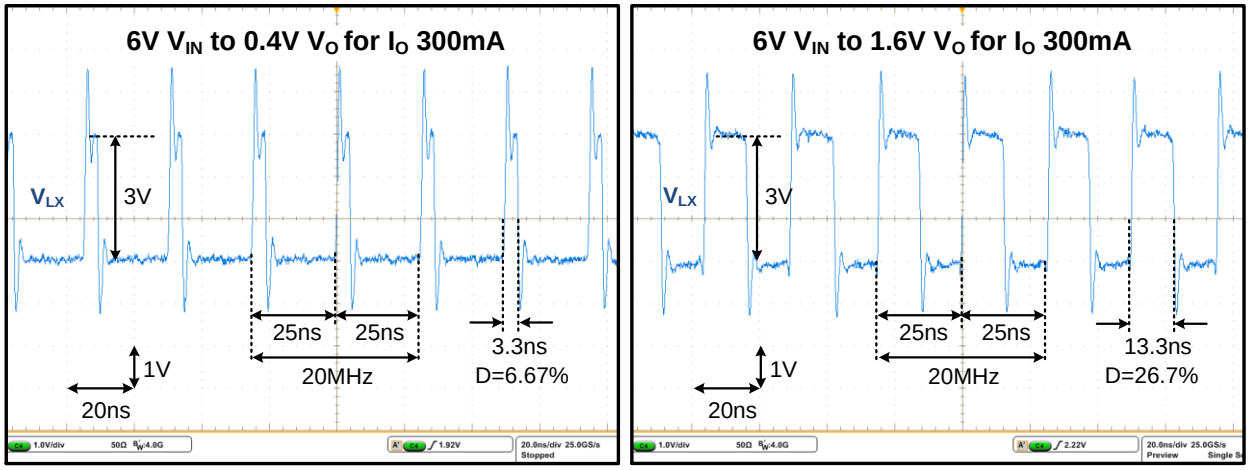


Figure 2.17. Measured switching node to verify range of conversion ratio.

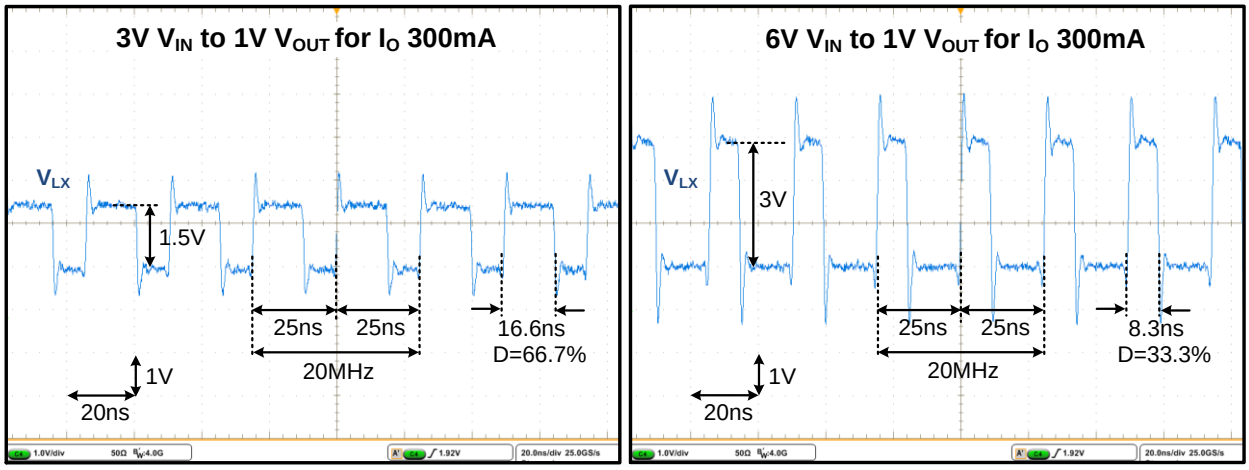


Figure 2.18. Measured switching node to verify V_{IN} operating range.

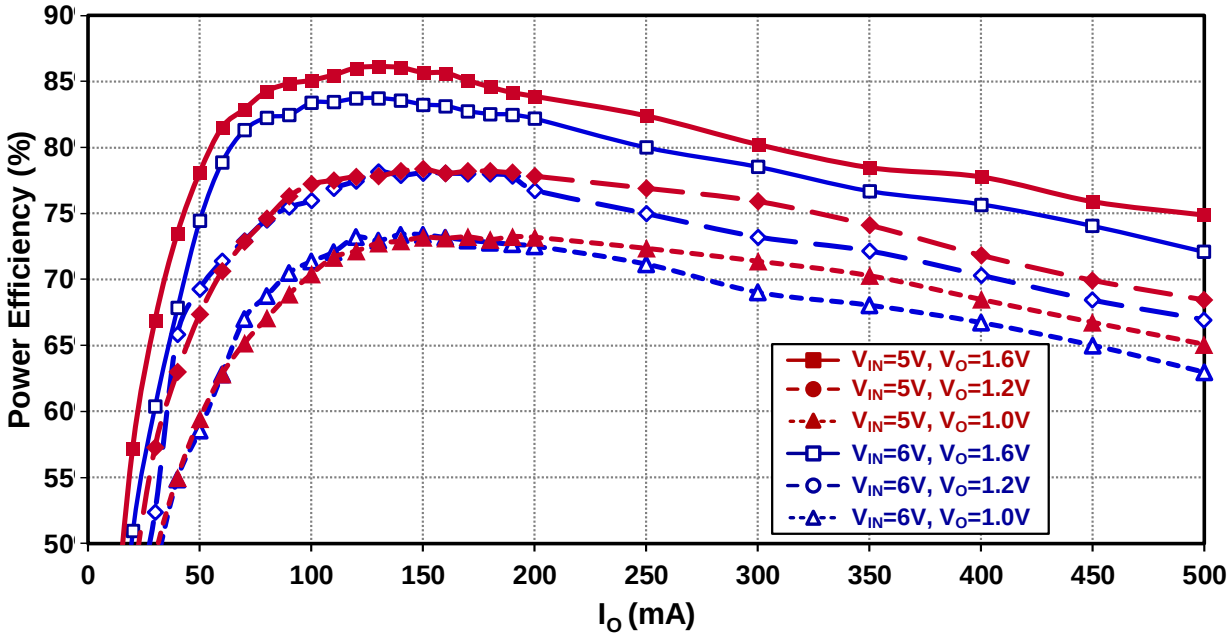


Figure 2.19. Measurement efficiency versus I_O.

Figure 2.16 demonstrates the benefits of using the proposed gate driver for the 3-level converter at 5 V of V_{IN} and 1 V of V_O condition. Thanks to the ICDT controller, the dead-time for the rising edges of the V_{LX} achieves 500 ps, while sweeping the load range from 0 mA to 500 mA. Similarly, the dead-time for the falling edges of the V_{LX} is 750 ps. These fixed dead-times over a full load range are only consumed by the propagation delay of the gate buffer stage, which is

regarded as a significant improvement compared with [Song-15]. Furthermore, the voltage swing on V_{LX} is only 2.5 V (half V_{IN}), verifying the 3-level operation.

Figure 2.17 demonstrates the measured V_{LX} node to verify wide V_O range at 6 V of maximum V_{IN} and 300 mA of I_O. Due to the sub-ns dead-time controller and high-speed level shifter, the converter operates in wide V_O range from 0.4 V to 1.6 V even with 20 MHz of f_{SW}, and the corresponding conversion ratios are 6.7% and 26.7%, respectively. As depicted in Figure 2.18, the measured V_{LX} node verifies the V_{IN} independent bootstrap power supply at 20 MHz of f_{SW}. The converter regulates the V_O of 1 V constantly even with varying V_{IN} range from 3 V to 6 V, allowing the converter to apply battery voltage directly for power supply V_{IN}. In addition, the dead-time on

Table 2.1. Performance comparison with previous 3-level converter designs.

Design	[Villar-08]	[Godycki-14]	[Kim-11]	This Work
Technology (nm)	250	65	130	350
Power Switch Structure	Stacked PMOS /Stacked MOS	Stacked PMOS /Stacked MOS	Stacked PMOS /Stacked MOS	All NMOS
Input Voltage (V)	3.6	1.8	2.4	3-6
Output Voltage (V)	1	0.5-0.75	0.4-1.4	0.4-1.6
Switching Frequency (MHz)	37.3	N/A	50-200	20
Minimum Duty Ratio (%)	27.8	27.8	16.7	6.7
Maximum Output Power (W)	0.1	0.28	1	0.8
Peak Efficiency (%)	69.7	64	77	85.5

V_{LX} shows no change under different V_{IN} conditions. The measured power efficiency is plotted over the output power range in Figure 2.19. The achieved peak efficiency is 85.5% for 5 V to 1.6 V conversion, and the maximum output power is 0.8 W.

A performance comparison with previous 3-level converter designs is shown in Table 2.1. The presented design operates in a wider V_{IN} range to deal with variable battery voltage, whereas the supply voltage of the previous designs is fixed. To achieve the trends of the output voltage scaling, the presented design accomplishes 0.4 V of V_O, resulting in a conversion ratio of 6.7%. This result is half of the conversion ratio than that of the best prior design [Liu-09]. Besides, compared with other designs with similar f_{SW}, this design achieves up to 21.5% higher efficiency even with higher supply voltage due to using all-NMOS power switches and sub-ns range of the dead-time controller.

CHAPTER 3

A MULTIPHASE HYSTERETIC DC-DC CONVERTER WITH WIDE-LOAD-RANGE EFFICIENCY AND FAST TRANSIENT RESPONSE*

In this chapter, the design challenges of the multiphase DC-DC converter in mobile applications are first reviewed in Section 3.1, which especially requires fast transient response and wide-load-range efficiency for application processors. In Section 3.2, the principle of the adaptive window (AW) control is then addressed, which fundamentally elevates the function of the hysteretic window and largely improves load transient performance of the hysteretic control. To facilitate the AW control in multiphase converters, a synchronized adaptive window (SAW) hysteretic control evolves from the AW control. Extended feature of achieving wide range of programmable V_O in SAW control for DVS features is also discussed. In Section 3.3, the principle and implementation of 1-Cycle APC are addressed, accomplishing adaptive phase count within one switching cycle through an internal current sensing mechanism equipped. Then, the implementation of our proposed multiphase converter is elaborated. Finally, the experimental results of the proposed design are provided in Section 3.4 to successfully verify the functionality and performance.

3.1 Design challenges of the multiphase DC-DC converter

Modern application processors (APs) have been continuously advancing with escalated performance and power consumption [Wong-11]. The switch mode DC-DC converter, which is commonly used to power these APs, is crucial, as it ensures a steady power supply, despite

repetitively and drastically changing current drawn by the APs. When an AP flips its operation from deep sleep mode to active mode, the supply's load current slew rate can reach beyond 1A/ns [Wong-11], in order to minimize latency and retain throughput. Accordingly, the power converter is expected to facilitate such a drastic load current change at a comparable, if not larger, slew rate. Otherwise, devastating system blackout could occur. Such a load transient performance is three to four orders higher than state-of-the-art commercial products, imposing an unprecedented challenge to modern power converter design. As possible alternatives, increasing output capacitance of the power converter may reduce voltage overshoot/undershoot during load transients. However, it further increases board real estate, which has already been challenging in portable applications. Alternatively, the inductor in the power stage can be reduced to elevate the inductor current (I_L) slew rate. However, this is usually at the cost of significant switching frequency and noise increases, leading to direct penalties on efficiency and reliability.

From the perspective of control, the fast feedback control method is essential to accommodate large load current slew rate. In addition, to improve system power density and efficiency, simple and compact implementation is highly desirable. Historically, current-mode hysteretic control has been popular owing to its fast load transient performance and simple, robust circuit structure [Nabeshima-04]. However, it still does not suffice due to the delay of the hysteretic feedback loop. In order to achieve the unprecedented current slew rate of 1A/ns, such delay is expected to be significantly shortened. On the other hand, a hysteretic control usually works at variable switching frequency, which causes current imbalance and hot spot issues in multiphase converters [Eirea-08]. It can also complicate the input EMI/EMC filter design. Numerous clock synchronization techniques [Li-09, Lee-09, Su-09, and Kim-15] were reported to achieve fixed

switching frequency operation in the hysteretic control. However, they introduce additional large delays, which contradict the needs for fast transient and large current slew rate.

To enhance a power converter's load current slew rate, multiphase converter structures are highly advantageous over single-phase ones in power converter design [Li-09, Kim-15, Song-14, Huang-13, and Huang-16]. For a N phase converter, its equivalent current slew rate is approximately equal to the current slew rate of a single-phase converter multiplied by N [Perreault-98]. If phase sub-converters operate in an interleaving manner, the output V_O ripples can be greatly attenuated through phase shifting. In this case, smaller output capacitor can be used, leading to extended loop bandwidth and reduced form factor, and making the dynamic voltage scaling (DVS) system operation possible [Zhai-04, Dreslinski-10, and Kaul-12]. However, although the multiphase architecture can extend power range and improve current slew rate, at the light load all-phase operation suffers low efficiency due to excessive switching loss in all phase sub-converters. To mitigate this, active phase count (APC) techniques [Huang-13, Huang-16] were proposed to turn-off some of the active phases judiciously at light to even moderate load conditions. However, the delay time caused by the process of sensing and/or computing average load current can become a speed bottleneck during extreme load transients [Huang-13, Huang-16]. The resulting V_O drooping can exacerbate severely, forfeiting the benefit of adopting multiphase structures.

3.2 SAW Hysteretic Control

3.2.1. Adaptive Window Hysteretic Control

The proposed SAW hysteretic control initially evolved from the concept of the adaptive window (AW) hysteretic control. Hence, the creation of the AW hysteretic control is discussed

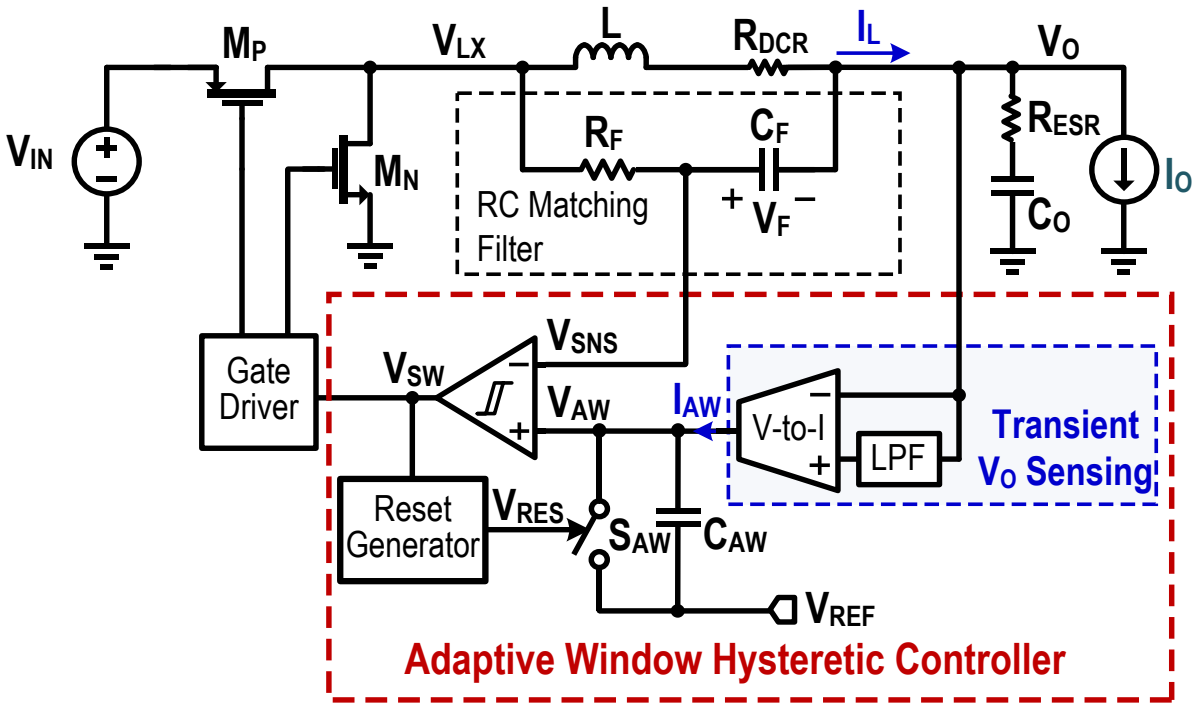


Figure 3.1. Block diagram of the proposed adaptive window hysteretic controller.

first. The block diagram of the proposed AW hysteretic controller is shown in Figure 3.1. Compared to the conventional fixed window hysteretic controller in [Nabeshima-04], which includes a hysteretic comparator, an RC matching filter, and a reference voltage (V_{REF}), the proposed controller requires four additional elements: a transient V_O sensing block, a capacitor C_{AW}, a switch S_{AW}, and a reset generator block.

In order to improve the transient response in the conventional hysteretic controller, the time constant of the RC matching filter can be increased; however, the chip size and cost are sacrificed, and the hysteretic window is narrowed, which can be easily affected by the switching noise. In contrast, the AW hysteretic controller detects the load step-up/down by sensing output voltage droop ΔV_O directly in the transient V_O sensing block, adjusts the V_{HYS} adaptively, and enhances the load transient. By directly altering the hysteretic window, the proposed controller has faster

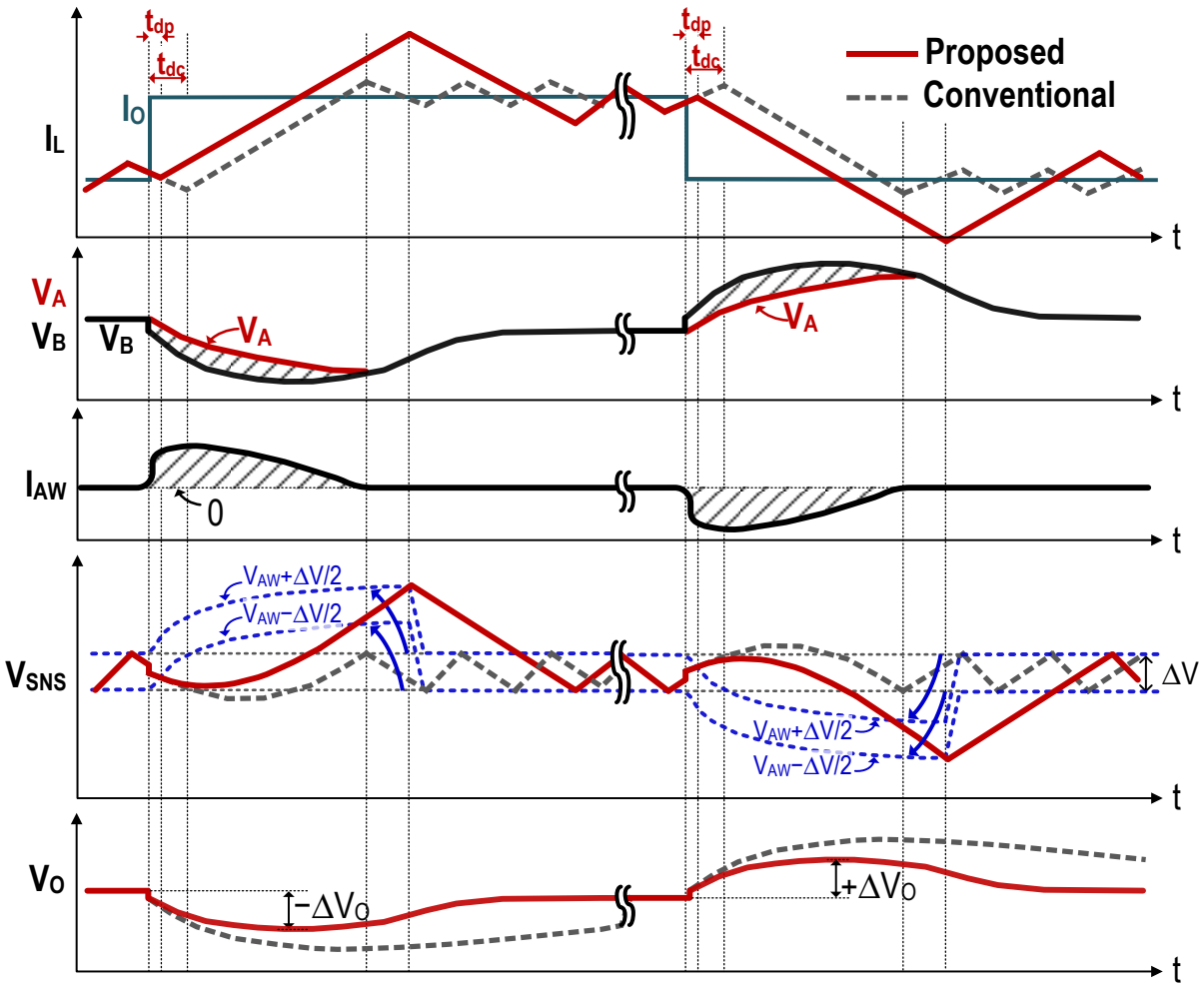


Figure 3.2. Timing diagram of the AW hysteretic control.

transient response than the conventional fixed window hysteretic control. Furthermore, without increasing the time constant in the RC matching filter, the controller can enhance the load transient, saving the area cost.

Figure 3.2 shows the detailed operation waveforms of the AW hysteretic control. At the beginning of the switching cycle, V_{RES} closes the switch S_{AW} to initialize $V_{AW}=V_{REF}$. After that, the S_{AW} becomes open to let the current I_{AW} decide V_{AW}. In steady state, the inputs of the voltage-to-current (V-to-I) converter are equal ($V_A=V_B$), forcing I_{AW} to zero. Hence, $V_{AW}=V_{REF}$. The hysteretic

comparator generates a fixed hysteretic window ΔV centered at V_{REF} similar to any conventional hysteretic control. However, during load transients, the voltage variation at V_O is sensed by the low-pass filter (LPF) creating a momentary voltage difference between V_A and V_B. At load step-up transient, the voltage undershoot at V_O causes $V_A > V_B$. Then the V-to-I converter generates a sourcing current I_{AW}, which charges C_{AW} to create an upward shift of V_{AW}. As a result, the hysteretic window moves adaptively in the upward direction opposite to the voltage undershoot shown in Figure 3.2. Consequently, V_{SNS} hits the lower boundary $V_{AW}-\Delta V/2$ of the adaptive hysteretic window much earlier ($t_{dp}<t_{dc}$) than the conventional fixed window hysteretic control. This leads to an immediate turn-on for the high-side power switch M_P to minimize the response time and the voltage undershoot at V_O. Afterwards, the adaptive window extends the turn-on period, facilitating

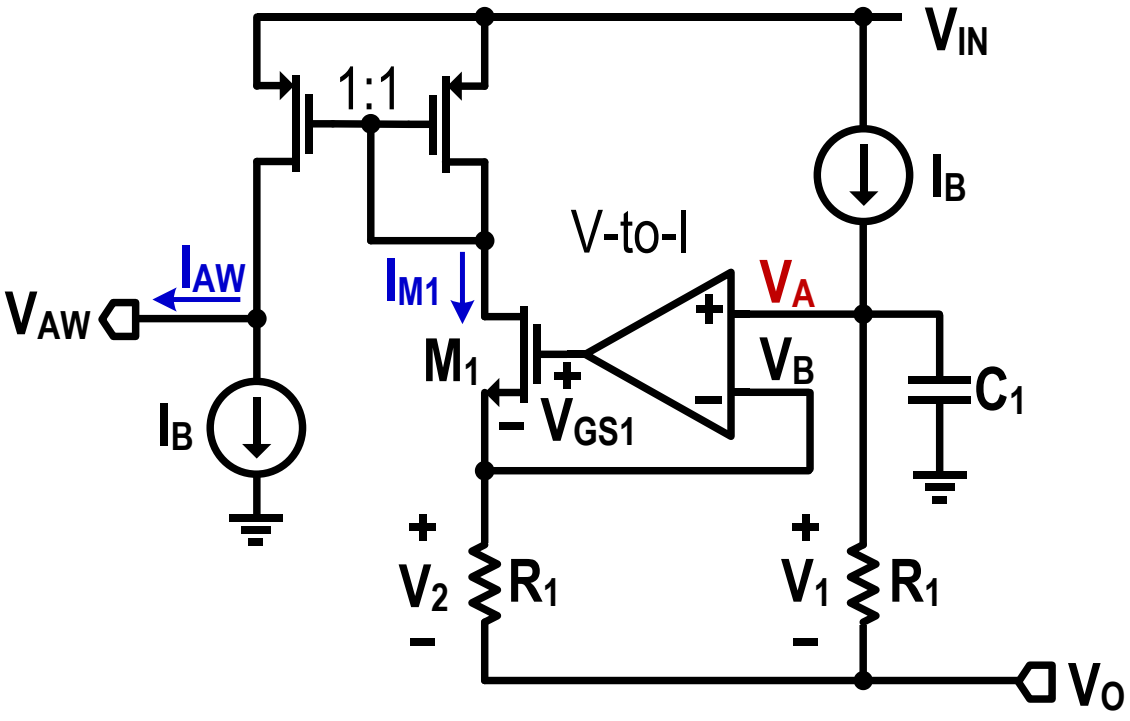
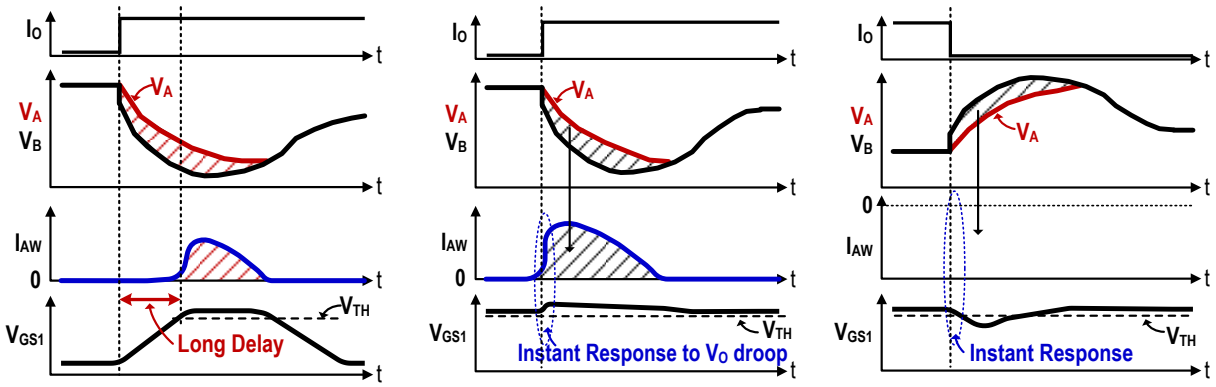


Figure 3.3. Implementation of the transient V_O sensing block.

I_L to charge more than the conventional hysteretic control. This way, the AW hysteretic controller provides a short response time as well as fast V_O settling. Once V_O recovers, M_P turns off and V_{RES} closes S_{AW} again to reset V_{AW} to V_{REF}. Then the hysteretic window returns to steady state. Likewise, at load step-down, the voltage overshoot at V_O makes $V_B>V_A$, and the V-to-I converter discharges C_{AW} with a sinking current, making V_{AW} drop. Thus, the hysteretic window moves to the downward direction, which is opposite to voltage overshoot. In this case, an extended turn-off period with a shorter response time helps achieve a smaller overshoot at V_O.

The transient V_O sensing block consists of a LPF followed by a V-to-I converter. The circuit implementation is shown in Figure 3.3. In the steady state, $V_A=V_B$. The differential input voltage of the V-to-I converter is equal to zero, leading to $I_{AW}=0$. However, if there is any voltage transient at V_O, it propagates to the inputs of the V-to-I converter. The LPF consisting of R_1-C_1 introduces an additional delay to the signal V_A compared to V_B and creates a momentary voltage difference V_A-V_B, which is then translated into a current I_{AW} by the V-to-I converter.

Note that it is necessary to employ the DC bias currents I_B at V_A and V_{AW}. In the absence of



(a) (b) (c)

Figure 3.4. key operation waveforms of the transient V_O sensing block with (a) $I_B=0$ during load step-up, (b) $I_B>0$ during load step-up, and (c) $I_B>0$ during load step-down.

I_B, the V-to-I converter in Figure 3.3 produces a zero current in the steady state, forcing M_1 to enter the cut-off region by lowering its gate-to-source voltage V_{GS1} below the threshold voltage V_{TH} as shown in Figure 3.4(a). When a load step-up transient occurs, the momentary undershoot at V_O makes $V_A > V_B$ and creates the input difference ($V_A - V_B$), which is translated into a sourcing current I_{AW}. As M_1 was initially in the cut-off region, its V_{GS1} has to be charged above V_{TH} to enter the saturation region. This creates a very long delay during critical load transient events. In addition, with I_B=0, the transient V_O sensing block does not have any current sinking capability at V_{AW} as required during load step-down transient when $V_B > V_A$. Hence, in this design, a small DC bias current I_B at V_A is introduced to keep M_1 always awake even in steady state condition. As M_1 is also carrying the same I_B in steady state, the DC offset at V_A introduced by I_B is cancelled by placing a matching resistor R_1 in between V_O and V_B. This ensures a zero-input differential voltage

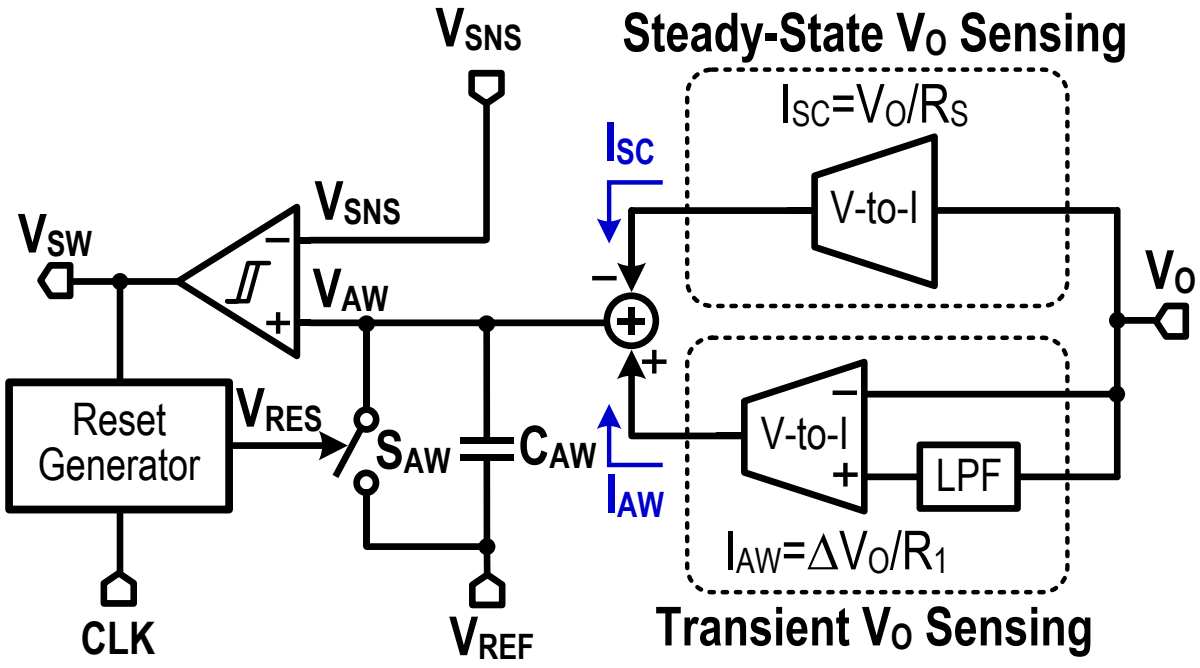


Figure 3.5. Synchronized adaptive window (SAW) hysteretic controller.

by making V_A=V_B. As results, in steady state, M_1 operates in the saturation region. V_{GS1} of M_1 is slightly higher than V_{TH} as shown in Figure 3.4(b). When I_{M1} is mirrored to V_{AW}, it gives a sourcing current of I_B. A sinking current reference with the same value of I_B is placed at V_{AW} to keep I_{AW}=0. When a load step-up transient occurs, as M_1 is always awake, the V-to-I converter detects V_A−V_B, and converts it into I_{AW}=(V_A−V_B)/R_1 at a much faster speed. Similarly, during a load step-down transient, V_B>V_A, resulting in a sinking current at I_{AW} as shown in Figure 3.4(c).

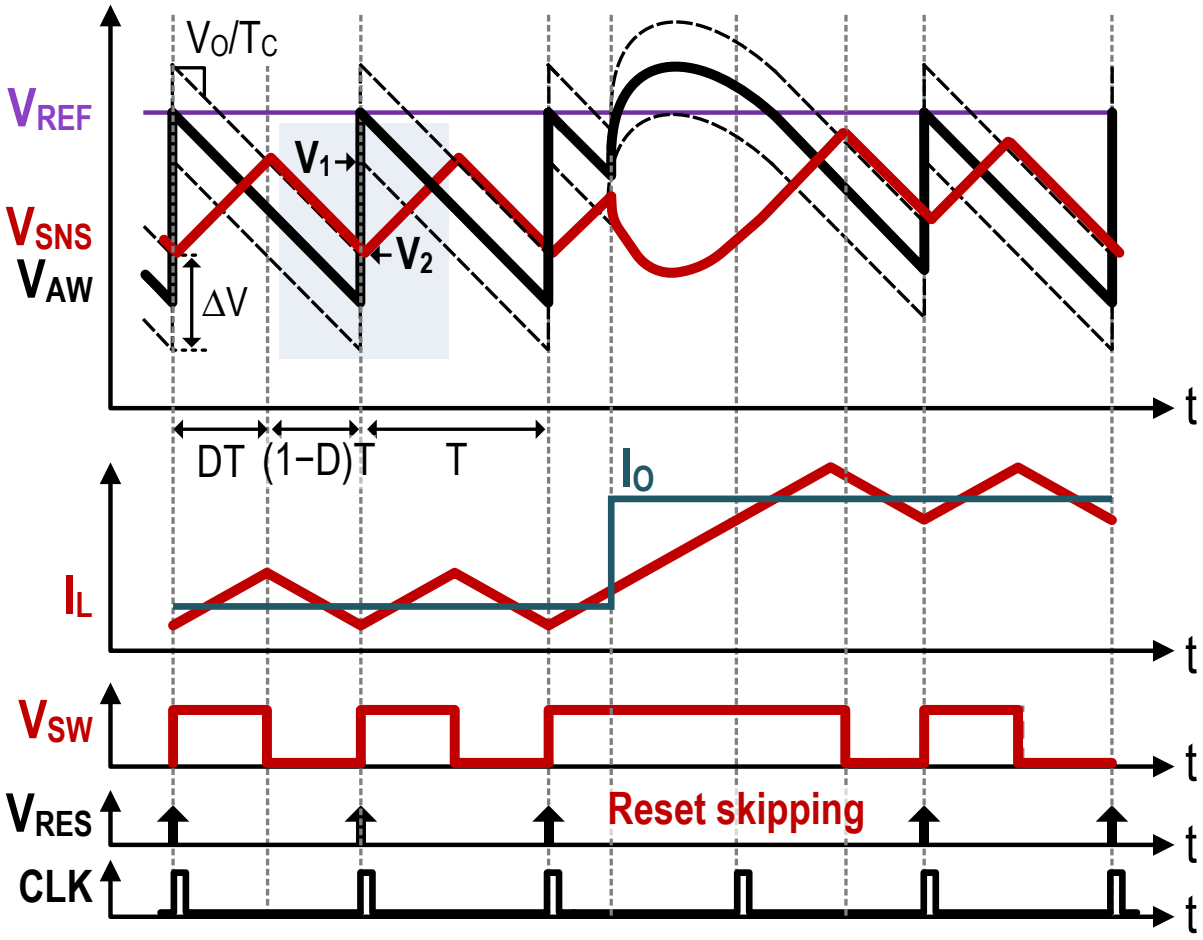


Figure 3.6. Timing diagram of the SAW hysteretic controller.

3.2.2 Synchronized Adaptive Window Hysteretic Control

To enable the AW hysteretic control in multiphase converters, the fixed switching frequency operation is highly desirable in order to avoid current imbalance issues between phase sub-converters. Hence, a synchronized adaptive window hysteretic control is proposed, based on the AW hysteretic control in Section 3.2.1. Figure 3.5 shows a circuit block diagram of the SAW hysteretic controller. A clock signal (*CLK*) and a steady-state V_O sensing block are added. The steady-state V_O sensing block is constructed with a transconductance stage, which converts V_O into the current $I_{SC}=V_O/R_S$, where R_S is the V-to-I gain of the steady-state V_O sensing. Unlike the transient V_O sensing block, the steady-state V_O sensing block operates in the steady state where $I_{AW}=0$, and the current I_{SC} discharges the voltage V_{AW} with a falling slope of I_{SC}/C_{AW} $[=V_O/(R_SC_{AW})]$ across time.

Figure 3.6 illustrates the critical timing operation of the SAW control. In steady state, at the beginning of each switching cycle, *CLK* resets S_{AW} to let $V_{AW}=V_{REF}$ and initialize the charge period *DT*. In the meantime, I_{SC} discharges C_{AW} to cause V_{AW} to drop at a rate of I_{SC}/C_{AW}. On the other hand, the inductor current I_L is sensed using the RC matching filter consisting of R_F and C_F (in Figure 3.1) as a sensing voltage V_{SNS}. During *DT*, as the inductor current rises, V_{SNS} follows the same rising slope of the inductor current $(V_{IN}-V_O)\times R_{DCR}/L=(V_{IN}-V_O)/(R_FC_F)$ by meeting the matching condition

$$L/R_{DCR} = R_F C_F = T_C . \tag{3.1}$$

Here, T_C is the time constant of the R_FC_F matching filter. Once V_{SNS} hits the upper bound of the hysteretic window, V_{SW} flips from "high" to "low." The discharge period $(1-D)T$ then starts. During $(1-D)T$, as I_L decreases, V_{SNS} decreases at the same rate of

$$V_O \times R_{DCR} / L = V_O / (R_F C_F) = V_O / T_C \ . \tag{3.2}$$

In addition, in this design, the falling slope of V_{SNS} matches with that of V_{AW} by maintaining

$$R_S C_{AW} = R_F C_F \ , \tag{3.3}$$

which means V_{SNS} falls at the same slope as V_{AW} and reaches V_2 at the end the switching period of T. The magnitude of V_2 is calculated as

$$V_2 = V_{REF} + \frac{\Delta V}{2} - V_O \times T / T_C \ . \tag{3.4}$$

As the next clock cycle of *CLK* begins, V_{RES} again initializes V_{AW} to V_{REF}, and the lower hysteretic boundary jumps to V_1, defined as

$$V_1 = V_{REF} - \frac{\Delta V}{2} \ . \tag{3.5}$$

If $V_1 > V_2$, *CLK* creates a forceful intersection between V_{SNS} and V_{SW} and starts the next switching cycle. By combining (3.4) and (3.5), the condition for achieving a *CLK*-synchronized operation can be derived as

$$\Delta V = V_O \times T / T_C \ . \tag{3.6}$$

Therefore, in steady state, the falling slope of V_{AW} together with a periodic reset action synchronized by *CLK* creates a sawtooth waveform, which is compared with a triangular V_{SNS} waveform using a hysteretic comparator to guarantee a fixed switching frequency operation.

With the SAW hysteretic control, when a load transient occurs, reset pulses generated by V_{RES} are blocked to allow the inductor to be charged or discharged immediately. For instance, in response to a load step-up transient, a positive I_{AW} from the transient V_O sensing block shifts the adaptive window upward and extends the turn-on time until the inductor is sufficiently charged as

shown in Figure 3.6. Once V_O recovers and I_L reaches its new steady state, the converter is re-synchronized with *CLK* using the same mechanism described earlier. Similar performance is also expected during the I_O step-down transient. In this way, the proposed synchronized operation in the AW controller does not degrade the dynamic performance during load transients.

3.2.3 Wide Programmable Range of V_O

Nowadays modern processors are capable of operating at different power modes to accomplish adaptive power-performance optimization through the techniques such as DVS [Zhai-04, Dreslinski-10 and Kaul-12]. In such case, the power supply is required to cover a wide range of programmable supply voltage to facilitate DVS operation. Translating it to the SAW hysteretic

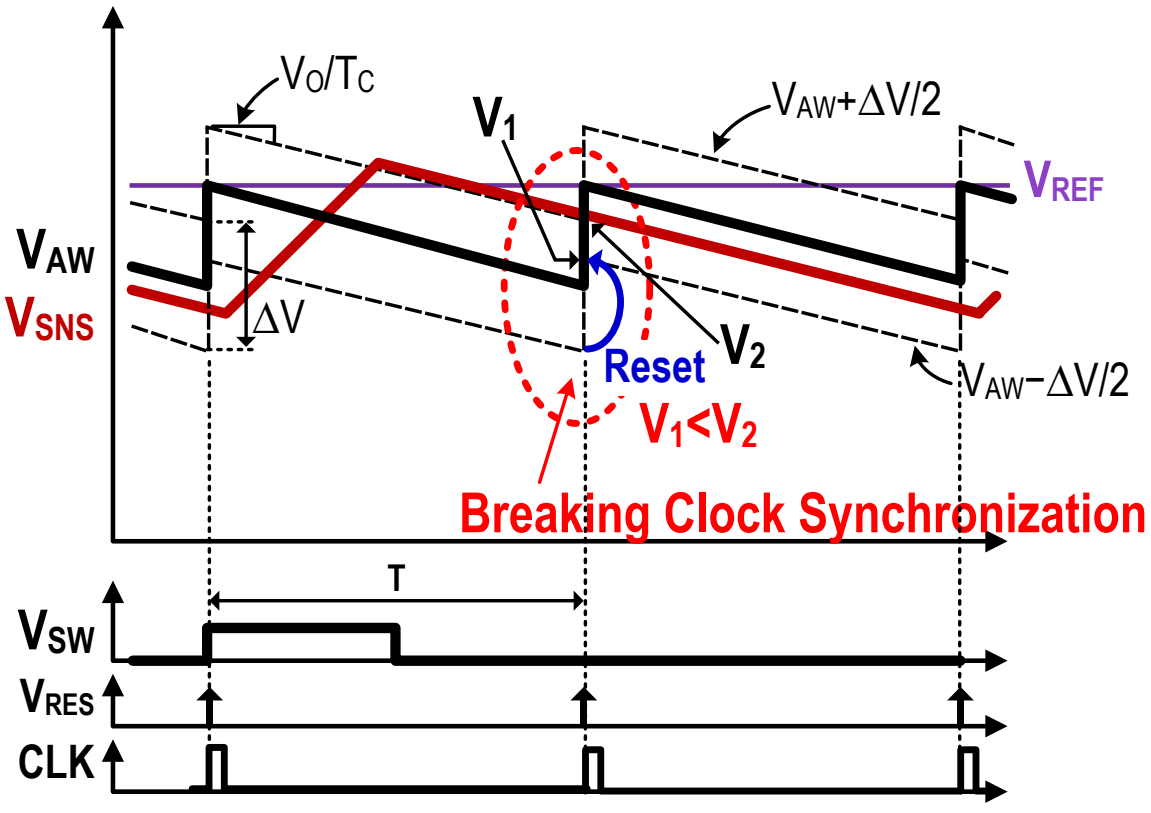


Figure 3.7. Clock synchronization at very low V_O level.

power converter design, this imposes a new challenge when the converter delivers a very low V_O. One fundamental constraint is the condition $V_1>V_2$ addressed in Section 3.2.2, which leads to the relation $\Delta V<V_O\times T/T_C$ in (3.6). If the targeted V_O level is very low, then V_{AW} and V_{SNS} decrease at a much slower rate in the discharge phase, and it may violate the condition. In that case, as $V_1<V_2$, it leads to $\Delta V>V_O\times T/T_C$. Even though V_{RES} resets S_{AW}, the intersection occurs within the hysteretic window. As a result, the output of the hysteretic comparator V_{SW} does not go high, and it breaks the clock synchronization as shown in Figure 3.7. One way to deal with this issue is increasing the switching period T, but this increases output ripples and slows down the speed. Another alternative is to decrease the hysteretic window ΔV or increase the time constant T_C. However, the former makes the converter more sensitive to noise, while the latter demands more silicon area.

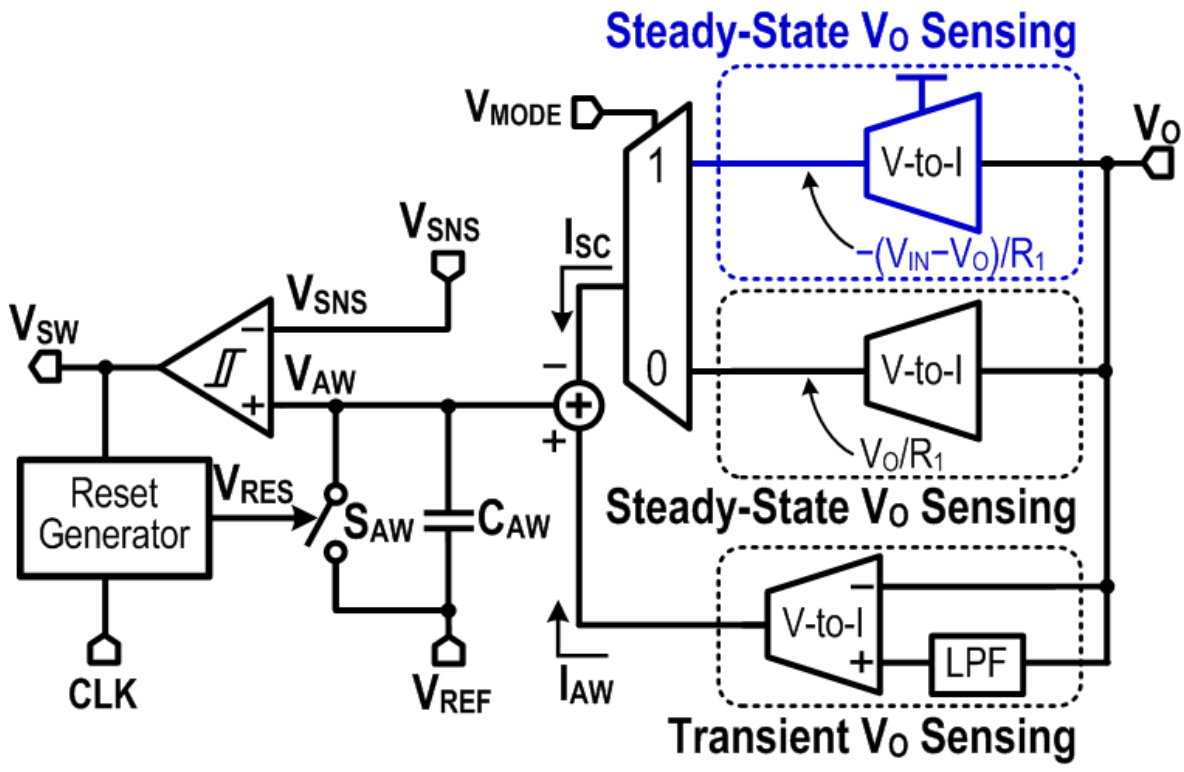


Figure 3.8. Inclusion of the steady-state $V_{IN}-V_O$ sensing to expand programmable range of V_O.

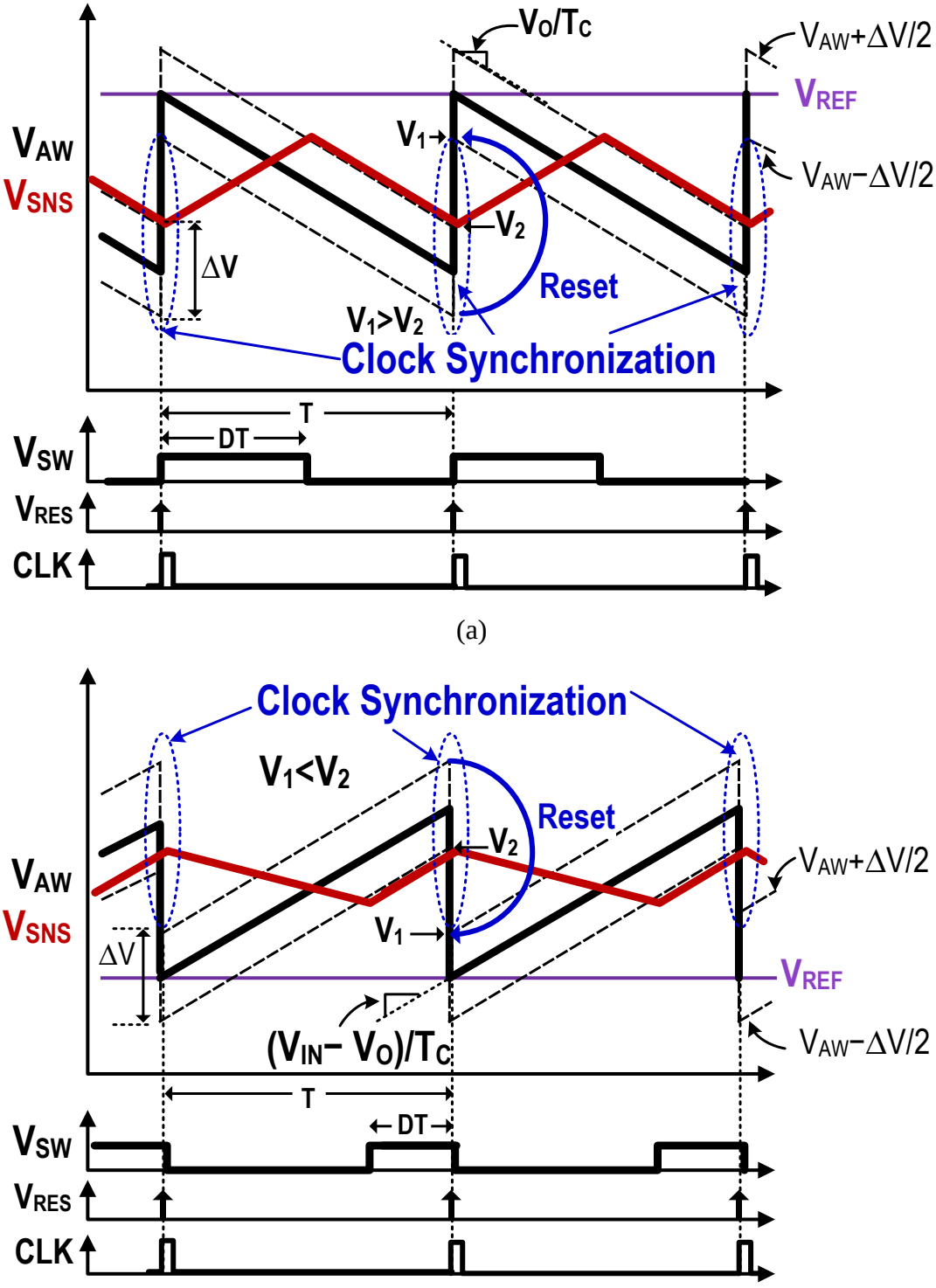


Figure 3.9. Expanding the programmable range of V_O in the SAW hysteretic controller when (a) V_{MODE}=0, and (b) V_{MODE}=1.

To expand the programmable range of V_O, we include a steady-state $V_{IN}-V_O$ sensing block in the SAW hysteretic controller, as shown in Figure 3.8. The steady state V_O sensing block works primarily for the higher side of the V_O operation range, whereas the steady state $V_{IN}-V_O$ sensing block is more helpful to the lower side. With the introduction of two different modes in the controller, a 2:1 multiplexer controlled by the signal V_{MODE} preselects one of them appropriately based on the desired V_O range. Similarly, the steady state $V_{IN}-V_O$ sensing block is a V-to-I converter, which translates the dropout voltage into the current. A negative sign in $V_{IN}-V_O$ indicates that V_{AW} charges with a rising slope of $(V_{IN}-V_O)/(R_SC_{AW})$ in this mode. This leads to change in the modulation scheme from the leading edge (V_{MODE}=0) to the trailing edge (V_{MODE}=1) as discussed next.

As illustrated in Figure 3.9(a), when V_{MODE}=0 (low), the charge period DT is initialized at the beginning of each switching cycle when V_{RES} equalizes $V_{AW}=V_{REF}$. Meanwhile, the discharge period $(1-D)T$ is modulated by the hysteretic controller, and this attribute is a trailing edge modulation. On the other hand, if V_{MODE}=1 (high), as depicted in Figure 3.9(b), the discharge period $(1-D)T$ begins when CLK resets S_{AW} leading to $V_{AW}=V_{REF}$. After that, V_{AW} charges C_{AW} at a rate of $(V_{IN}-V_O)/T_C$ under matched condition, and V_{SNS} falls until it hits the lower boundary of the hysteretic window. Once V_{SW} goes high to start the charge period DT, V_{SNS} rises at the same slope as V_{AW} until it reaches

$$V_2 = V_{REF} - \Delta V/2 + (V_{IN} - V_O) \times T/T_C \,. \tag{3.7}$$

Here, because the start of the charge period is modulated by the controller, this is a leading edge modulation. At the next CLK edge, V_{RES} again initializes V_{AW} to V_{REF}, and the upper hysteretic boundary falls down to

$$V_1 = V_{REF} + \Delta V/2 \,. \tag{3.8}$$

This creates a forceful intersection of V_{SNS} with the higher hysteretic boundary under the condition $V_1<V_2$ as

$$\Delta V < (V_{IN} - V_O) \times T/T_C \,. \tag{3.9}$$

Once V_{SW} goes low, the next switching cycle begins. This ensures a synchronized operation with *CLK* under V_{MODE}=1 (high).

The key benefit of including both modes in the controller is to ensure a synchronized fixed switching frequency operation under a wide programmable range of V_O. The trailing edge modulation scheme generally works well for the higher range of V_O. However, the synchronization may be an issue at a very low voltage level of V_O. On the other hand, the leading edge modulation scheme is suitable for a lower range of V_O, and the synchronization may be lost if a high V_O is targeted. Once, both the modes are incorporated, the controller expands the programmable range of V_O with guaranteed clock synchronization.

3.3 Multiphase SAW Hysteretic Converter

3.3.1. 1-Cycle APC

With the proposed clock synchronization technique in the SAW hysteretic control, we can now upgrade the converter design with multiphase operation, which further improves inductor current slew rate, output ripples and extends loop bandwidth. With the parallel structure, it is apparent that a multiphase converter can cover a much wider power range over its single-phase counterpart. However, this also raises a new problem in retaining high efficiency. Active phase count (APC) has thus been reported recently [Huang-10 and Huang-16]. In such a scheme, the number of active phases is determined by sensing and/or computing averaged inductor currents

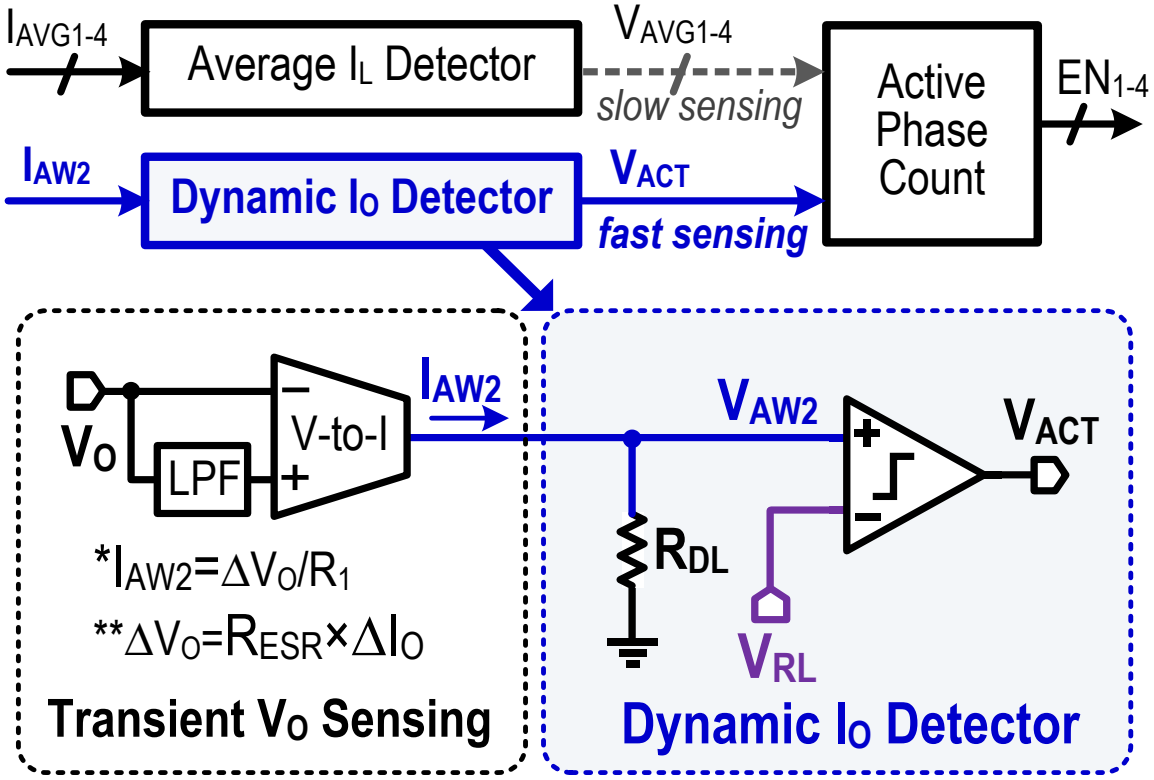


Figure 3.10. Block diagram of the 1-Cycle active phase count (APC) circuitry.

across phase sub-converters. In general, such an averaging process is rather time consuming, resulting in a sluggish dynamic performance. Unfortunately, this might not be acceptable in the APs, where current can be withdrawn from a very low level to a few orders higher within nanoseconds. Accordingly, the APC switching should also be accomplished instantaneously. Hence, the 1-Cycle APC scheme is proposed. Its circuit block diagram is simply illustrated in Figure 3.10.

An average I_L detector generates the phase enabling signals $V_{AVG1\text{-}4}$ and decides the number of active phases with a considerable delay. To mitigate this, by taking advantage of the proposed AW control, a dynamic I_O detector block is used to detect load step-up transient and reinforce 4-phase to all-phase operation within one switching cycle. Note that the dynamic I_O detector is only

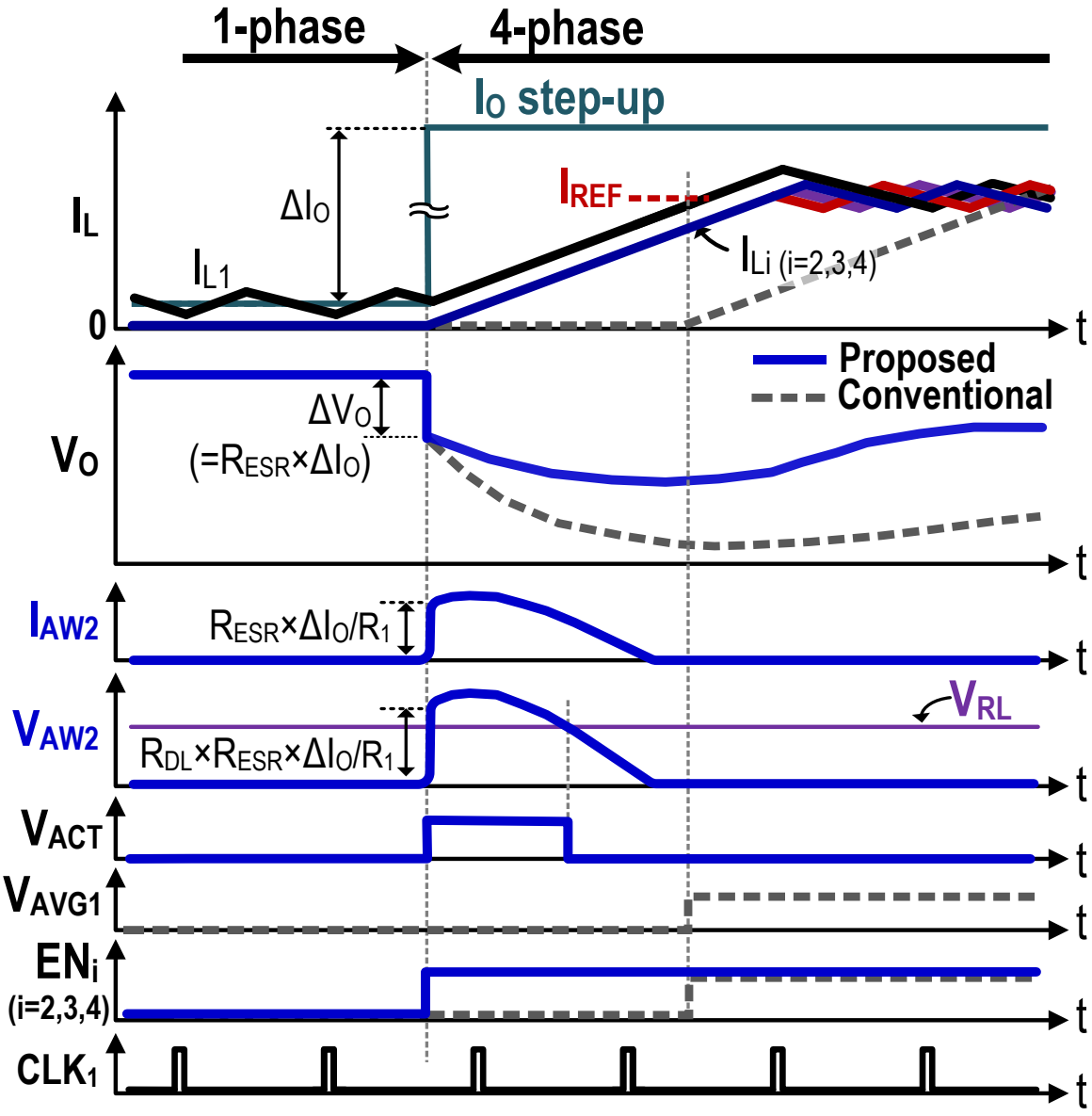


Figure 3.11. Operation of the 1-Cycle APC scheme during load step-up transient.

operational during load step-up transient to minimize voltage undershoot and settling time. As discussed before, the transient V_O sensing block is capable of detecting such voltage transients, and, hence, the same block is reused here. Figure 3.11 describes more detailed operation. For a load step-up of ΔI_O, the voltage drop (ΔV_O) across R_{ESR} is given as

$$\Delta V_O = R_{ESR} \times \Delta I_O . \tag{3.10}$$

The transient V_O sensing block senses ΔV_O and converts into a sourcing current I_{AW2} as

$$I_{AW} = R_{ESR} \times \Delta I_O / R_1 . \tag{3.11}$$

Once I_{AW2} passes through R_{DL} in the dynamic I_O detector block, it produces V_{AW2}, which is given as

$$V_{AW} = R_{DL} \times R_{ESR} \times \Delta I_O / R_1 . \tag{3.12}$$

Then V_{AW2} is compared to a reference voltage (V_{RL}) to produce the all-phase active signal V_{ACT}. Under $V_{AW2}>V_{RL}$, V_{ACT} goes high and the "forced all-phase operation" is enabled. Note that the forced all-phase operation is only desirable for a high load step-up where the V_O undershoot is considerably large. The minimum load step ($\Delta I_{O,ACT}$) to activate V_{ACT} should be judiciously chosen by fixing the value of V_{RL}. Here, $\Delta I_{O,ACT}$ is derived as

$$\Delta I_{O,ACT} = V_{RL} \times \frac{R_1}{R_{DL} \times R_{ESR}} . \tag{3.13}$$

On the other hand, during load step-down transient, if the APC changes the operation from all-phase to single phase momentarily before I_L settles to the steady state, a large overshoot and a long settling time would be observed. Therefore, a quick phase switching from all-phase to single-phase is not desirable during load step-down transient. Instead, the all-phase operation initially discharges the inductor to minimize the overshoot. Afterwards, active phases are gradually turned off one-by-one until reaching the steady state.

In steady state, for efficiency concern, the average I_L detector senses the average inductor current and thus the load current to decide the number of active phases. This happens with a large delay when I_{L1} crosses the I_{REF} limit and V_{AVG1} goes high.

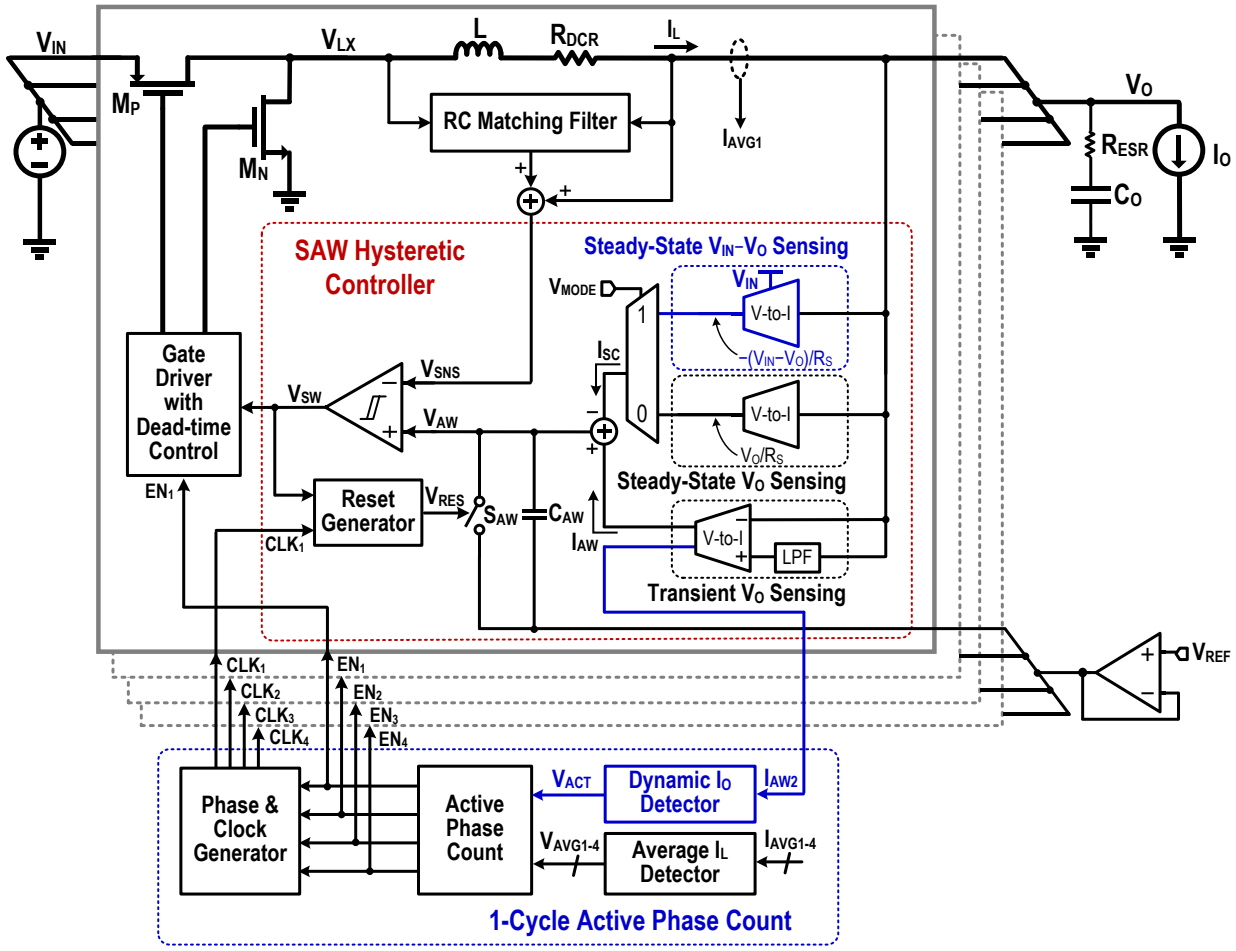


Figure 3.12. Circuit block diagram of the proposed 4-phase SAW hysteretic power converter.

3.3.2 Full System Implementation

The converter's circuit block implementation is illustrated in Figure 3.12, which contains four independently regulated, but clock-synchronized phase sub-converters. Each sub-converter is equipped with a SAW hysteretic controller, a power stage, a gate driver with dead-time control and an RC filter to sense its inductor current. By replicating the output stage of the transient V_O sensing block in the SAW hysteretic controller, I_{AW2} is generated and used in the dynamic I_O detector block. The 1-Cycle APC acts as a control unit for 4 sub-converters. $EN_{1\text{-}4}$ enable the gate

drivers as well as $CLK_{1\text{-}4}$ of the corresponding sub-converters. The phase and clock generator produce 90º phase-shifted, 25 MHz $CLK_{1\text{-}4}$ for the phase sub-converters respectively.

3.4. Experimental Verification

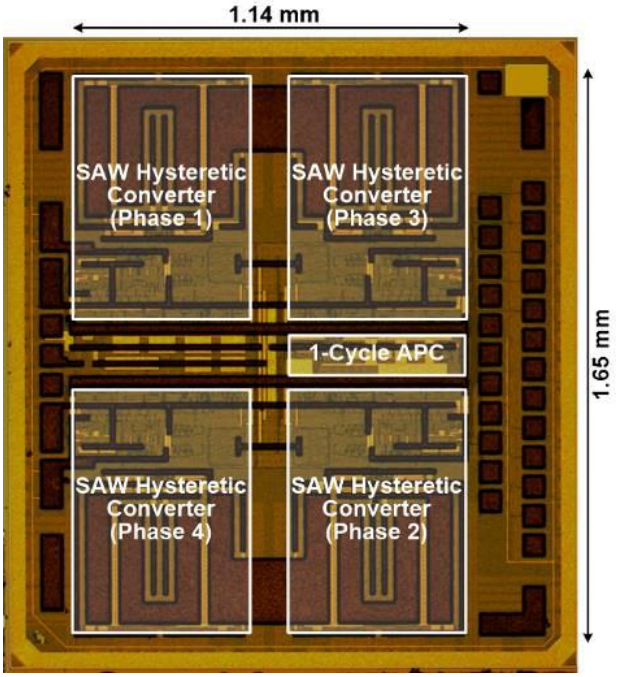
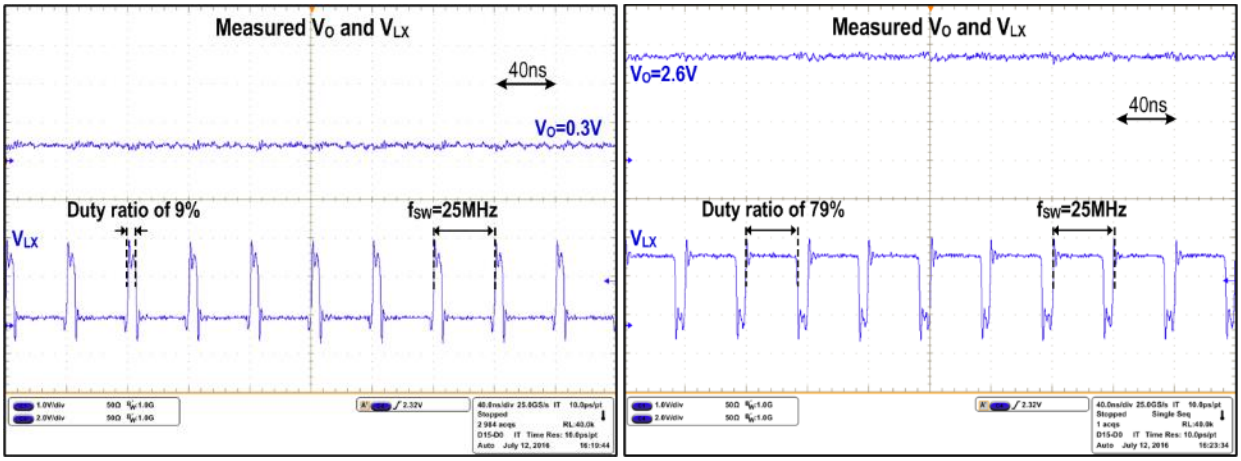


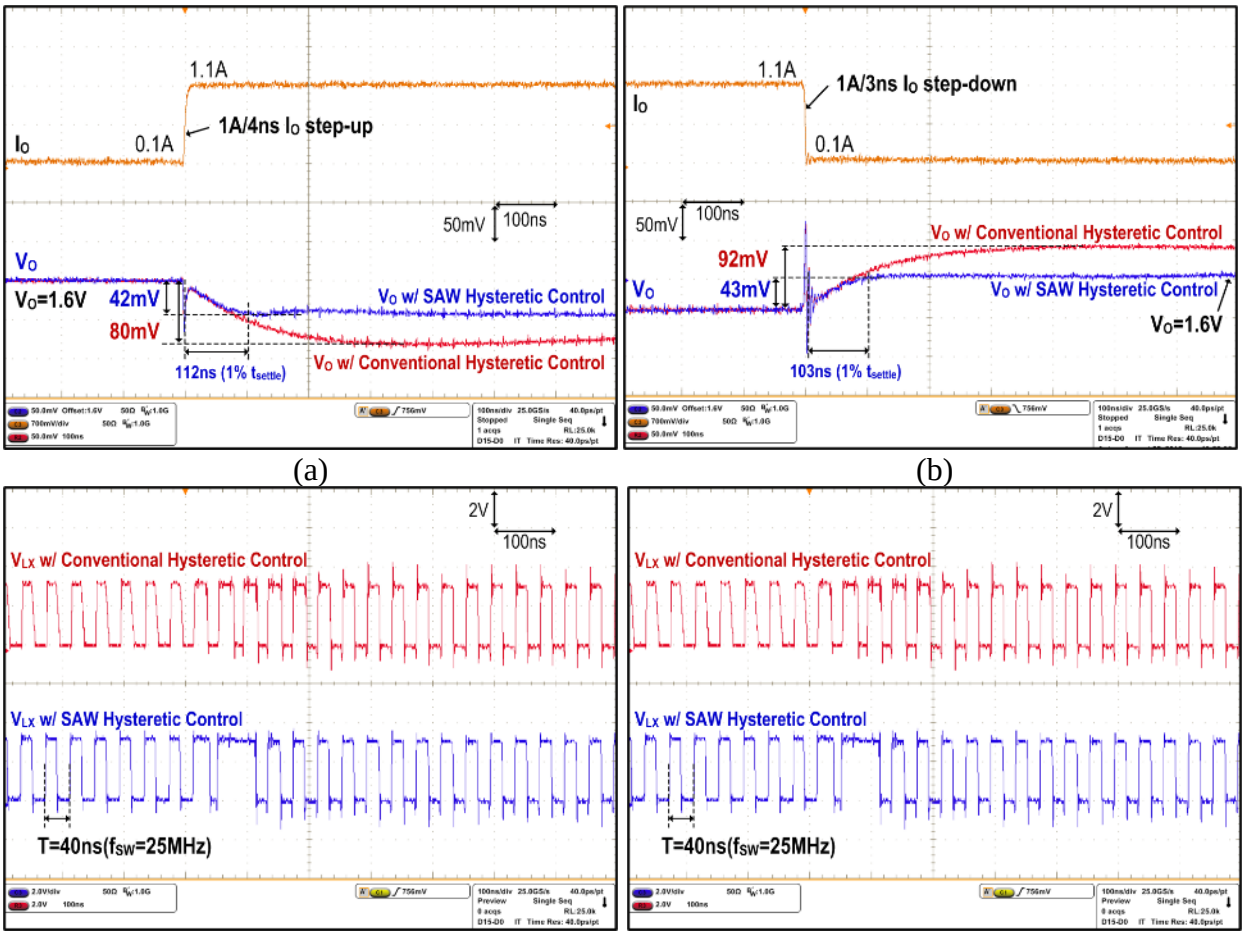
Figure 3.13. Chip micrograph.

A prototype of the converter is designed and fabricated in a 0.35 µm CMOS process. Figure 3.13 shows its chip micrograph. The active die area is measured as 1.88 mm^2. Operating at a nominal switching frequency of 25 MHz, each sub-converter employs a 200 nH inductor and delivers a maximum load current of 1.5 A. Hence, the maximum load current $I_{O,max}$ for the converter is 6 A. Thanks to the features of wide programmable V_O range and fast AW control, the converter offers a wide output V_O seamlessly from 0.3 V to 2.6 V. As verified in Figure 3.14, the measured duty ratio ranges from 9% to 79% when V_O is regulated at 0.3 V and 2.6 V respectively. of both the leading and trailing edge modulation schemes with mode selection expands the V_O range effectively.



(a) (b)

Figure 3.14. Measured results of the V_O and V_{LX} waveforms to verify the wide V_O operating range at V_{IN}=3.3 V.



(a) (b)

(c) (d)

Figure 3.15. Load transient performance comparison between SAW and conventional hysteretic control in single-phase operation.

Figure 3.15 validates the effectiveness of the proposed SAW control within each phase sub-converter. In Figure 3.15(a), in response to 1 A/ 4ns load I_O step-up, the undershoot voltage is reduced from 80 mV to 42 mV, compared to a conventional hysteretic control, leading to 47.5% reduction. Meanwhile, 1% settling time t_{settle} drops significantly from 2 µs to 112 ns, thanks to the immediately extended turn-on period in the SAW control, as observed in V_{LX} of Figure 3.15(c). In response to 1 A/ 3ns load I_O step-down, the overshoot voltage is reduced by 53% (from 92 mV to 43 mV) with 1% t_{settle} of 103 ns as shown in Figure 3.15(b). The corresponding V_{LX} node waveform

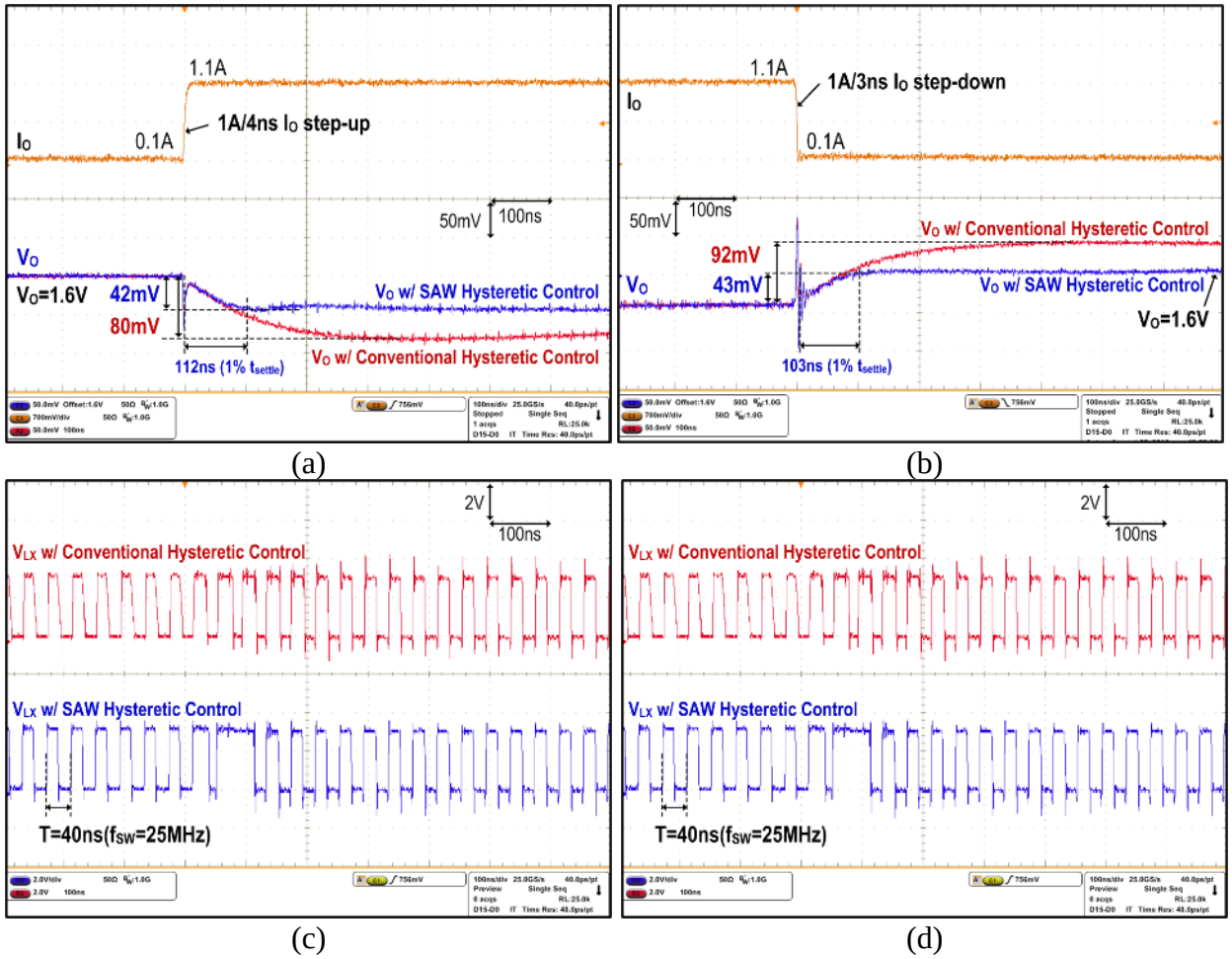


Figure 3.16. Comparison of the 1-Cycle APC with forced 4-phase operation at 0.1 A to 4.1 A load transients.

in Figure 3.15(d) reveals a quickly extended turn-off time in the SAW control to achieve a faster V_O recovery.

For the entire 4-phase operation, in order to verify the performances of load transient and 1-Cycle APC, significant load step changes of 0.1 A to 4.1 A are used in the measurement, which mimic the worst-case scenario for both load transient response and phase adding/dropping for APC in this design. In response to 4 A/ 5ns I_O current step-up, as shown in Figure 3.16(a) and (c), the converter achieves a 1% t_{settle} of 190 ns with an undershoot voltage below 103 mV. During the dynamic transient, it completes the single-phase to all-phase transition immediately with extended turn-on periods seen in V_{LX1-4} waveforms (Figure 3.16(c)) to maximize the effective I_L slew rate. During the period, clock synchronization was temporarily disabled to give the priority to load transient and then resumes after V_O recovery. In response to 4 A/ 3ns I_O load step-down, the measured overshoot is only 123 mV with a 1% t_{settle} of 237 ns as shown in Figure 3.16(b) and (d). Here, the turn-off period is initially extended in all the phases after the load step-down transient, and the average I_L detector gradually turns-off the extra phases as observed in V_{LX1-4} waveforms.

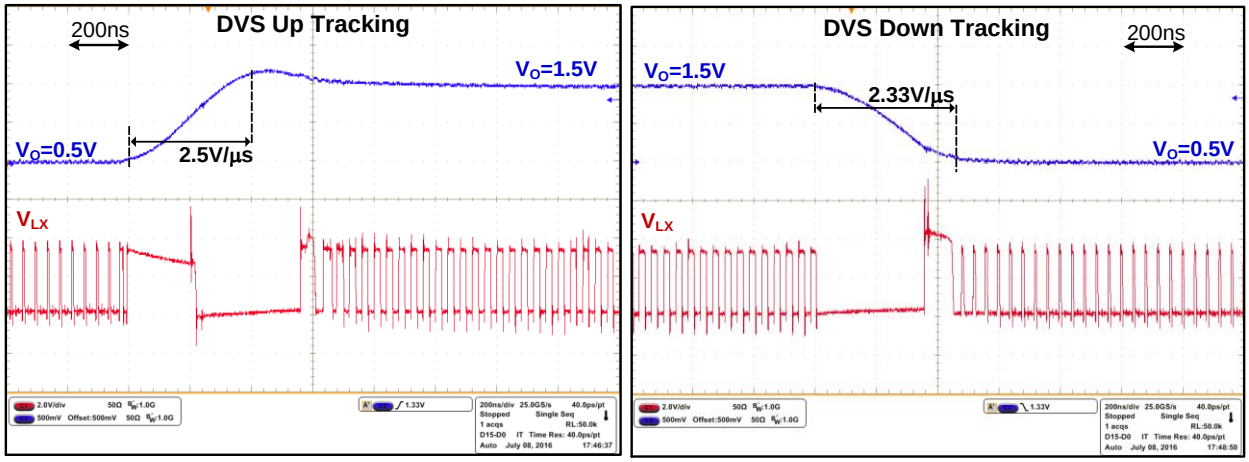


Figure 3.17. Measured results of the DVS operation.

As mentioned in Section 3.3.1, the recovery time in this scenario is usually less harmful to an AP. Hence, the APC focuses on overshoot minimization in load step-down transient.

Figure 3.17 is the measurement result to verify the DVS performance while sweeping the V_O from 0.5 V to 1.5 V. The converter achieves the V_O slew rate of 2.5 V/μs and 2.33 V/μs for up-tracking and down-tracking, respectively. Measured V_{LX} demonstrates that it instantly saturates DT, or $(1–D)T$, at the moment of DVS reference change.

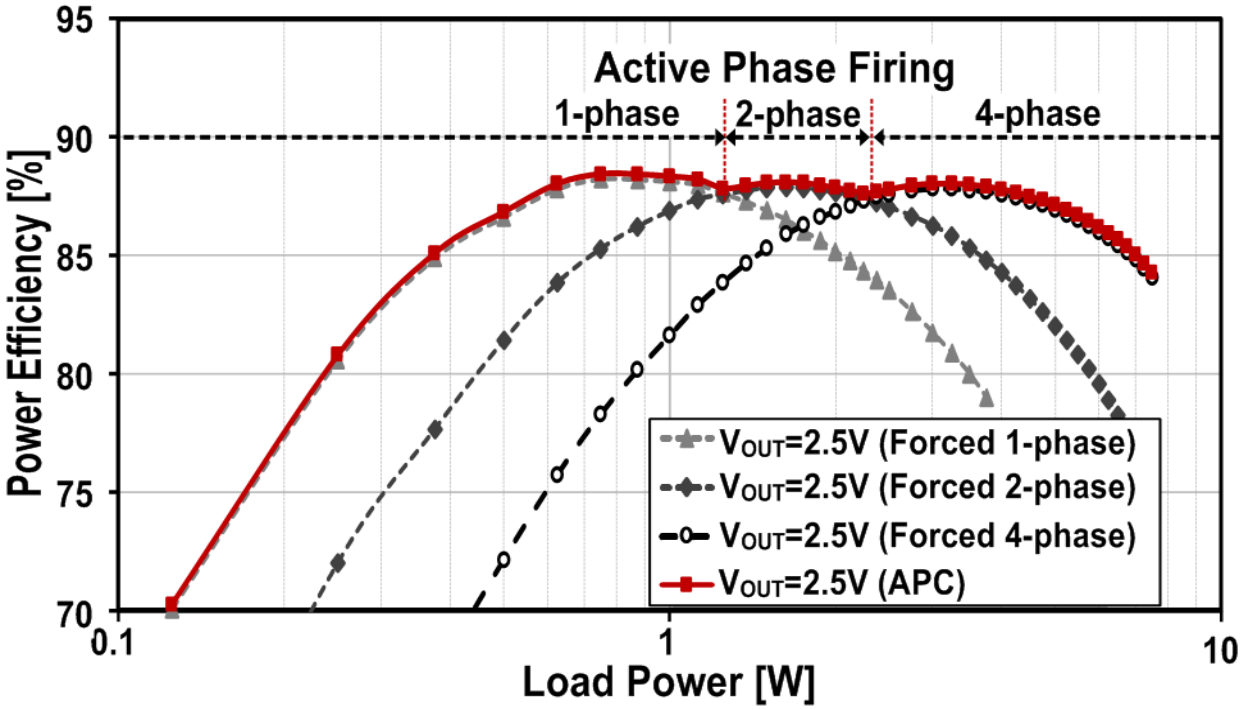


Figure 3.18. Measured power efficiency plots for 3.3 V to 2.5 V conversion.

Measured efficiency in nominal I/O condition is provided in Figure 3.18. In contrast to the proposed APC operation, efficiencies with forced 1-phase, 2-phase and 4-phase are also tested for comparison. As shown in the figure, the forced 1-phase operation is only efficient at low output power whereas the forced 4-phase is highly efficient at high power. In the intermediate level, the forced 2-phase operation provides better efficiency. With the proposed 1-Cycle APC, the number

Table 3.1. Performance Comparison

Design	[Kim-15]	[Song-14]	[Huang-13]	[Huang-16]	This Work
Control Method	T-PID	ZVS Hysteretic	VM PWM	CCS	SAW Hysteretic
Active Phase Count	No	No	Yes	Yes	Yes
Number of Phases	4	4	4	4	4
Switching Frequency (MHz)	30-70	40	100	30	25
Input Voltage (V)	1.8	3.3	1.2	3.3	3.3
Output Voltage (V)	0.6-1.5	0.7–2.5	0.6–1.05	0.7–3.0	0.3–2.6
Inductor (nH)	90	78	8	220	200
Output Capacitor (μF)	0.47	0.94	1.87	0.62	2.47
Technology (μm)	0.65	0.18	0.13	0.18	0.35
Power Density (W/mm^2)	2.5	1.93	0.63	4	3.98
Maximum I_O Current (A)	0.8	6	1.2	2.5	6
I_O Step-up Current (A/ns)	0.4/10	5/5	0.18/800	1.8/5	4/5
Vo Settling Time (ns)	600	230	2000	133	190
Peak Efficiency (%)	87	86.1	82.4	86.5	88.1
Minimum Duty Ratio	33%	21%	50%	21%	9%

[1] Power density calculated by chip area

of active phases is adaptively adjusted with load current and thus power level to retain high efficiency. As a result, the efficiency stays above 80% over 96.7% of the full power range, with a peak value of 88.1%.

Finally, as a summary, Table 3.1 compares this work with the prior art. Owing to the proposed SAW hysteretic control, this design accomplishes the fastest transient response to one

most stringent load transient test condition. The ultra-fast and robust controller design allows the converter to operate at the lowest switching frequency in the comparison group, leading to lower switching loss and thus benefiting the efficiency. Furthermore, the 1-Cycle APC helps the converter retain high efficiency over one of the widest power ranges, without degrading the transient performance. The wide programmable V_O range design delivers the lowest duty ratio achieved and facilitates wide-range DVS operation from near-threshold deep sleep mode to fully active mode. Area-efficient circuit design leads to a very competitive power density even at a higher technology node.

CHAPTER 4

A DOUBLE ADAPTIVE BOUND CONTROL FOR IMPROVING LOAD REGULATION AND POWER DENSITY

Section 4.1 of this chapter reviews the design challenges of the high-density controller, which require fixed switching frequency and high V_O regulation for mobile applications. In addition, to achieve long operating time in the portable application, active/sleep mode transient is addressed. In Section 4.2, the principle of the double adaptive bound control is then addressed, which fundamentally elevates the function of the hysteretic window with real-time slope-tracking reference and thus achieves a fixed switching frequency. To further improve the power density, the proposed control upgrades the V_O load regulation without using of the compensation network. Section 4.3 addresses the implementation of the digital-assisted proposed converter with autonomous mode manager, accomplishing further improved transient performance and light-load efficiency through installing four modes. A detailed explanation of the principle and circuit design for the additional modes is also presented. Finally, the experimental results of the proposed converter are provided in Section 4.4 to successfully verify the functionality and performance.

4.1 Design challenges of the synchronized high-speed controller

Modern mobile applications have been developed for performance improvement and long system runtime, while achieving compact size and low cost. Accordingly, the power converter plays a critical role in the system construction. Along with the performance enhancement, the device activates with sufficient power usage. On the other hand, the mobile system operates in sleep mode, disabling redundant functions and chips; by limiting the operating cycle, the mobile device facilitates long runtime without increasing battery capability and form factor. In addition,

the mobile device flips these active/sleep operations repetitively and drastically. Hence, the power converter is expected to facilitate such a rapid current change for ultra-reliable low-latency power supply. Otherwise, high-latency supply results in not only system failure during power up, but also over-charging energy loss by scaling power down. Moreover, the converter has to be designed with multiple operating modes corresponding to the various load conditions, which achieves decent system performance and provides efficient supply in a wide load range. This mode transition in the converter should be sufficiently fast and smooth to eliminate supply glitches and minimize passive components [Kim-18]. Furthermore, compact design is essential to enhance system density without limiting multi-functional integration.

From the perspective of the control design, the fast feedback control method is essential to accommodate a large load-current. Moreover, the multiple operating modes have to be designed

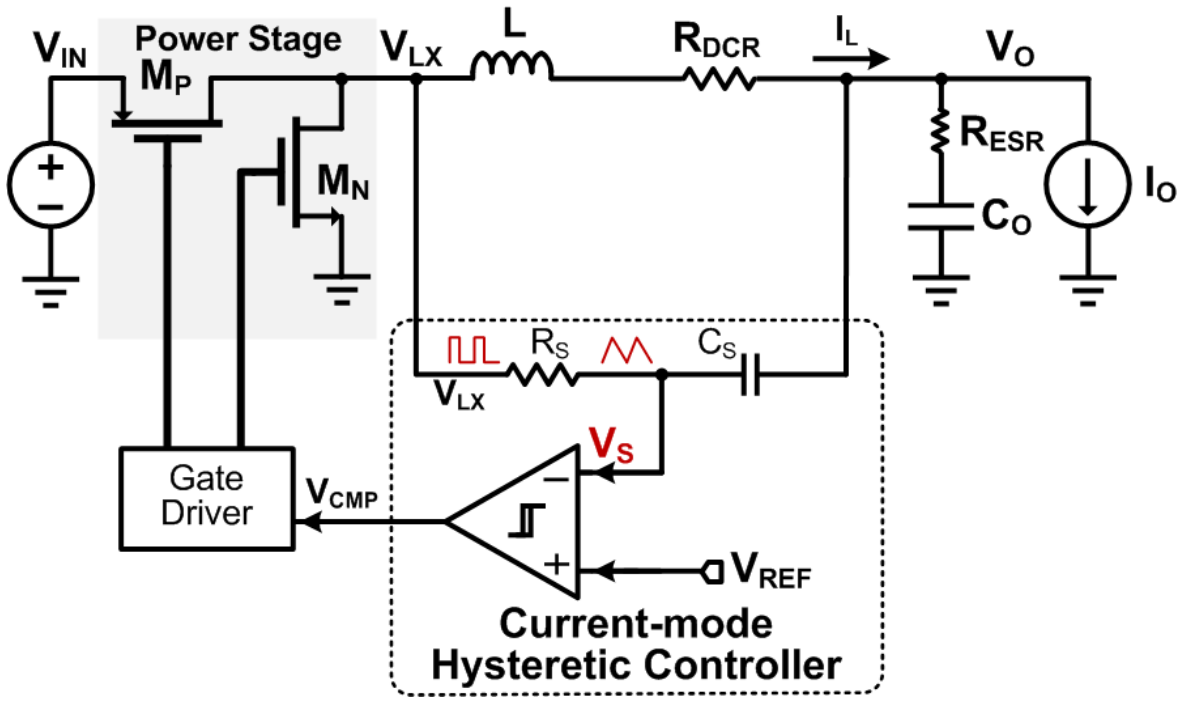


Figure 4.1. Conventional current-mode hysteretic converter.

to achieve decent system performance under various load conditions. It also helps to improve efficiency in a wide load range, especially at light-load condition. Along with these features, simple and area-efficient implementation is highly desirable to improve system power density and efficiency. Conventionally, the PWM control is employed due to its high output gain and fixed f_{SW}. However, it suffers from the low loop bandwidth limited by the bulky compensation network, which is ten times lower than f_{SW}, resulting in complex structure and high latency during power transition. Alternatively, the conventional hysteretic control, which has a double fixed window, can be used for fast response with the simple and robust circuit structure as illustrated in Figure 4.1 [Nabeshima-04]. However, as discussed in Section 1.2, this varying f_{SW} leads to the intricacy of the input EMI filter design in noise-sensitive systems and causes the current/phase imbalance and hot spot issues when designing the multiphase architecture design for high current delivery.

Numerous papers have reported achieving a fixed f_{SW} in the hysteretic control, which can consistently take advantage of the simple structure and fast response. Based on the f_{SW} Equation (1.4), which relates to V_{IN}, V_O, hysteretic window ΔV_H, and T_C of the matching filter, [Lee-15] adjusts ΔV_H with fixed T_C and [Grant-02, Hazucha-05, and Huerta-11] tune T_C with fixed ΔV_H by sensing the V_{IN} and V_O operating conditions. Inserting an adaptive delay within the hysteretic control loop by using digital control as in [Su-08 and Su-09] or by employing a phase-lock loop as in [Li -08 and Li-11] can be another option. However, these approaches require many trimming bits for precise control that necessitate a large area and additional power consumption, which contradicts the needs for a compact and low power-consuming system, resulting in limited power density.

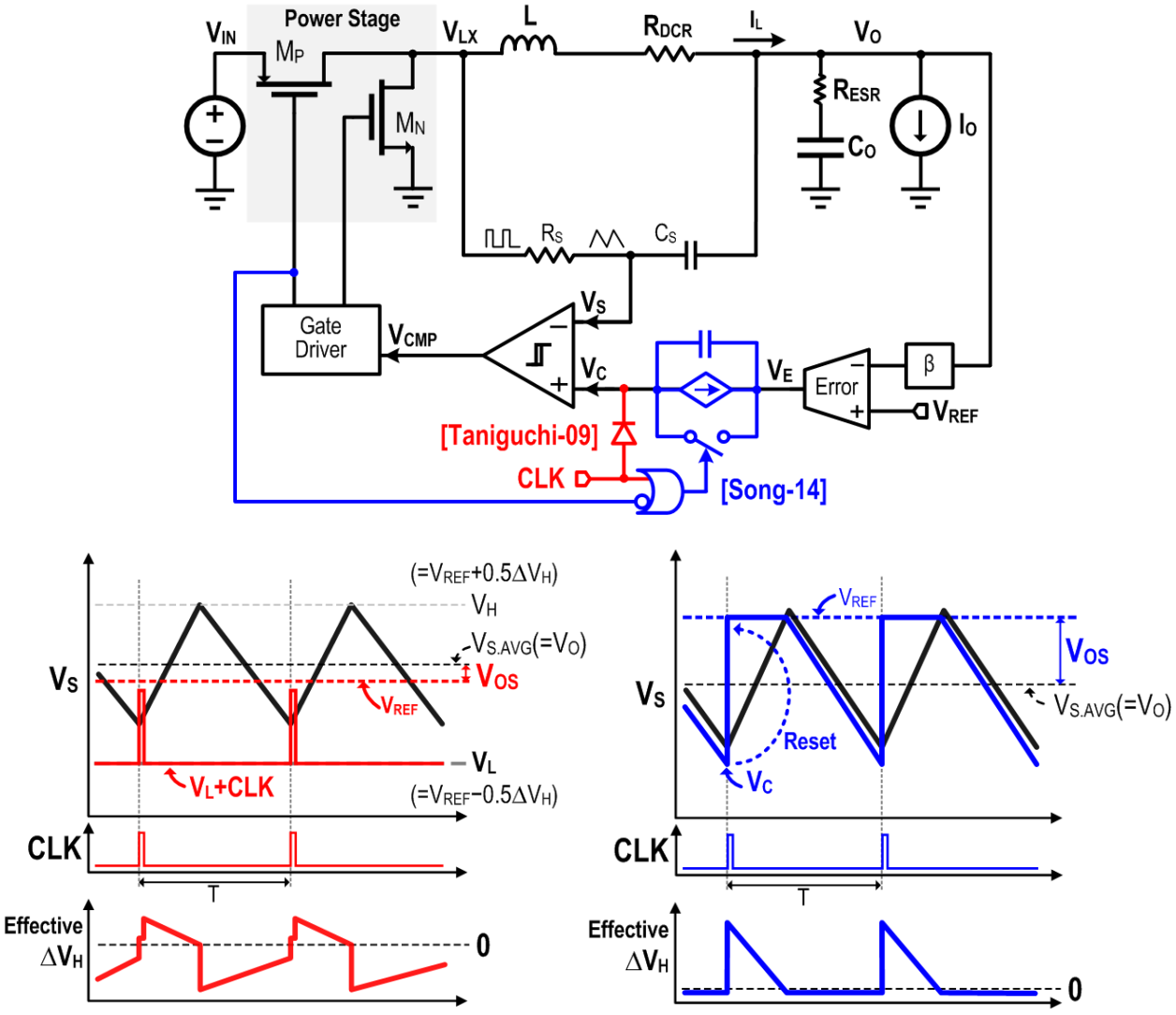


Figure 4.2. Simplified block diagram of the published clock synchronization schemes and corresponding key waveforms.

Alternatively, [Taniguchi-09, Song-14, and Lee-17] effectively reduce ΔV_H by employing a clock in the hysteretic window and forcefully restart the on-period, which result in the constant f_{SW}. Although these approaches can achieve a fixed f_{SW} simply and precisely, they introduce the mismatch between V_{REF} and the average of the I_L-sensed signal V_S, creating V_O offset as illustrated in Figure 4.2. Thus, these approaches need a compensation network with an error amplifier in the

voltage loop, increasing design difficulty, silicon area and further power consumption. In addition, in [Song-14 and Lee-17], as the narrow effective ΔV_H, which enables fast transient response, is employed only during the turn-off period $(1-D)T$, the response time during the turn-on period DT has the same response delay with the conventional hysteretic control. Consequently, this scheme has asymmetric transient response at the on- and off-time.

Moreover, additional features make the power converter the perfect feet for the battery-operated mobile applications. First, as the switching loss is the main power loss at light load, lowering the f_{SW} is essential, especially when the mobile system operates in the sleep mode to save power. Second, further improving transient response and settling time is required for drastic current change in the application processor supply. A wide V_{IN} operation in the converter allows direct connection with the battery, which has varied voltage depending on its stored energy, eliminating the need for another power converter stage and thus enhancing system efficiency.

4.2 Double Adaptive Bound Control

In order to overcome the aforementioned challenges, this section addresses a double adaptive bound (DAB) control. For the first phase, the proposed controller is developed to achieve both constant f_{SW} and fast transient response without degrading the advantage of the simple structure of the hysteretic control. Thus, it fundamentally elevates the function of hysteretic window with real-time current-slope tracking reference. In the next phase, instead of inserting an error amplifier, the DAB control evolves with the digital offset cancellation technique to eliminate the DCR offset, thereby improving V_O regulation. All these features are integrated in the single control scheme, facilitating compact size and utilization of different operation modes as discussed in Section 4.3.

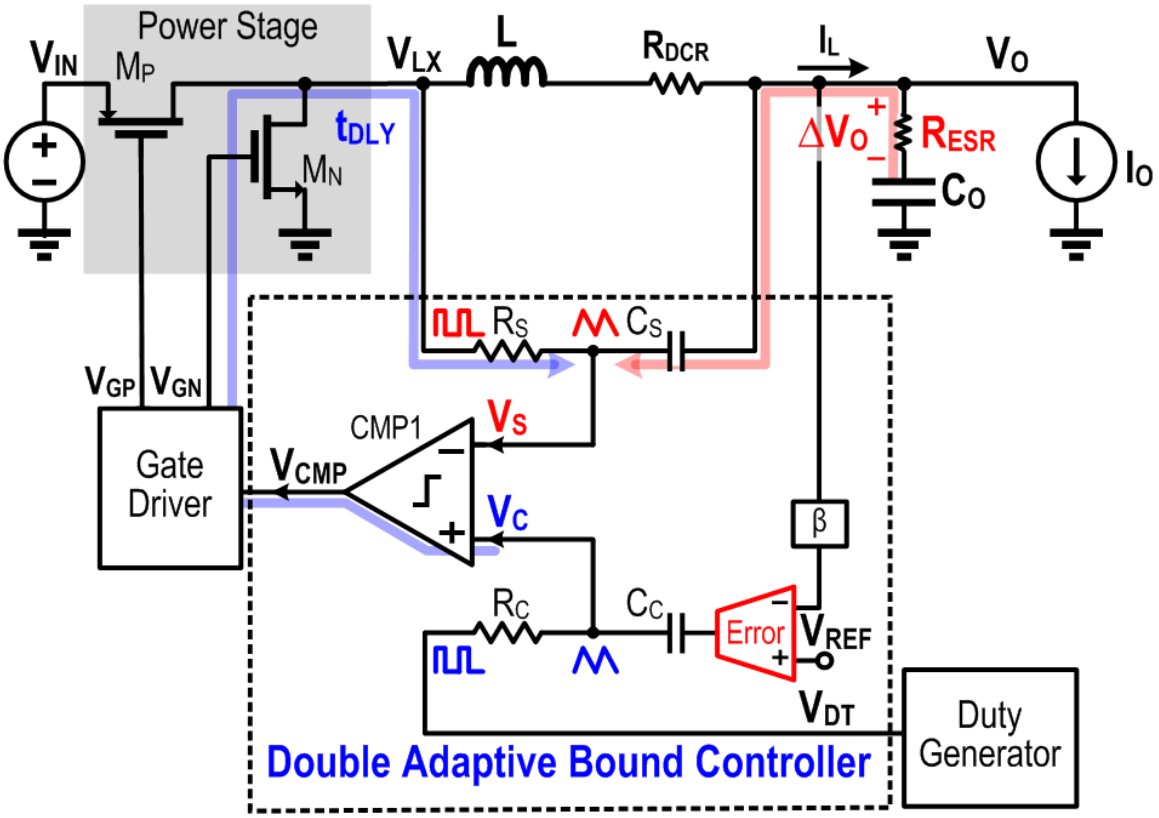


Figure 4.3. The block diagram of the Dual-RC hysteretic controller.

4.2.1 Phase 1: Operation Principle with Achieving Fixed f_{SW} and Fast Transient Response

The block diagram of the proposed DAB hysteretic controller is shown in Figure 4.3. Instead of employing only one RC filter with the hysteretic comparator in the conventional fixed window hysteretic controller (in Figure 4.1), the proposed controller implements two RC filters (R_S and C_S, R_C and C_C) with a comparator CMP1. In addition, the duty generator emulates the V_{LX}, which includes f_{SW} and duty cycle D(=V_O/V_{IN}) information, at V_{DT} according to V_{IN} and V_O. Supplied by V_{DT}, the inserted R_C and C_C modulate the triangular signals V_C as the reference boundary. If the V_O is well regulated at V_{REF} with the same time constant R_CC_C=R_SC_S, V_C can exactly track the slope of V_S owing to the same voltage swings on V_{LX} and V_{DT}, creating a narrow and real-time slope-tracking boundary. On the other hand, the sawtooth signal supplied by the

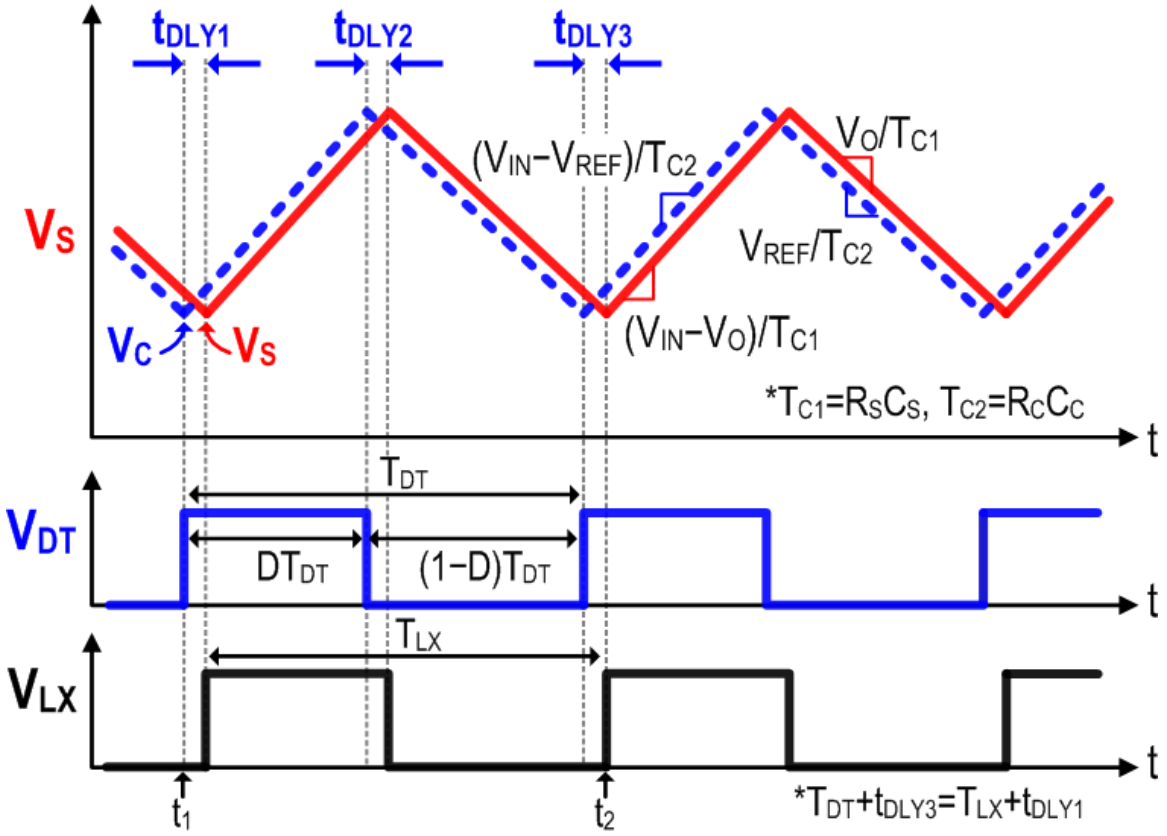


Figure 4.4. Timing diagram of the Dual-RC hysteretic controller in steady-state.

oscillator (OSC) is similar to that of the implementation of the conventional voltage-mode PWM controller. Because of the relationship between the sawtooth signal and V_{IN}, V_O improves the line regulation in the proposed hysteretic controller.

Figure 4.4 illustrates the operating waveforms of the DAB controller in steady state. When V_{DT} goes high first, V_C rises and intersects with V_S; thus, the turn-on period (V_{LX}=H) starts with inherent delay t_{DLY}, forcing V_S to rise with the same slope of V_C. After the turn-on time DT_{DT}, V_{DT} goes low and the turn-off period (V_{LX}=L) is triggered in a complementary manner. V_{DT} goes high again after one cycle T_{DT}, starting the next cycle. The time from t_1 to t_2 can be expressed as

$$T_{DT} + t_{DLY3} = T_{LX} + t_{DLY1}. \tag{4.1}$$

Because the t_{DLY} is the propagation delay created from CMP1 to the power stage, the t_{DLY} variation is negligible such as

$$t_{DLY} = t_{DLY1} = t_{DLY2} = t_{DLY3} \tag{4.2}$$

By combining (4.1) and (4.2), T_{DT} equals T_{LX} and the controller regulates V_O with a fixed f_{SW}. Unlike the previous clock synchronization techniques in [Song-14 and Lee-17], which have a limitation on the V_{IN} and V_O range, the proposed controller inherently and adaptively alters the hysteretic window and slope of V_C and V_S, covering all the operating range.

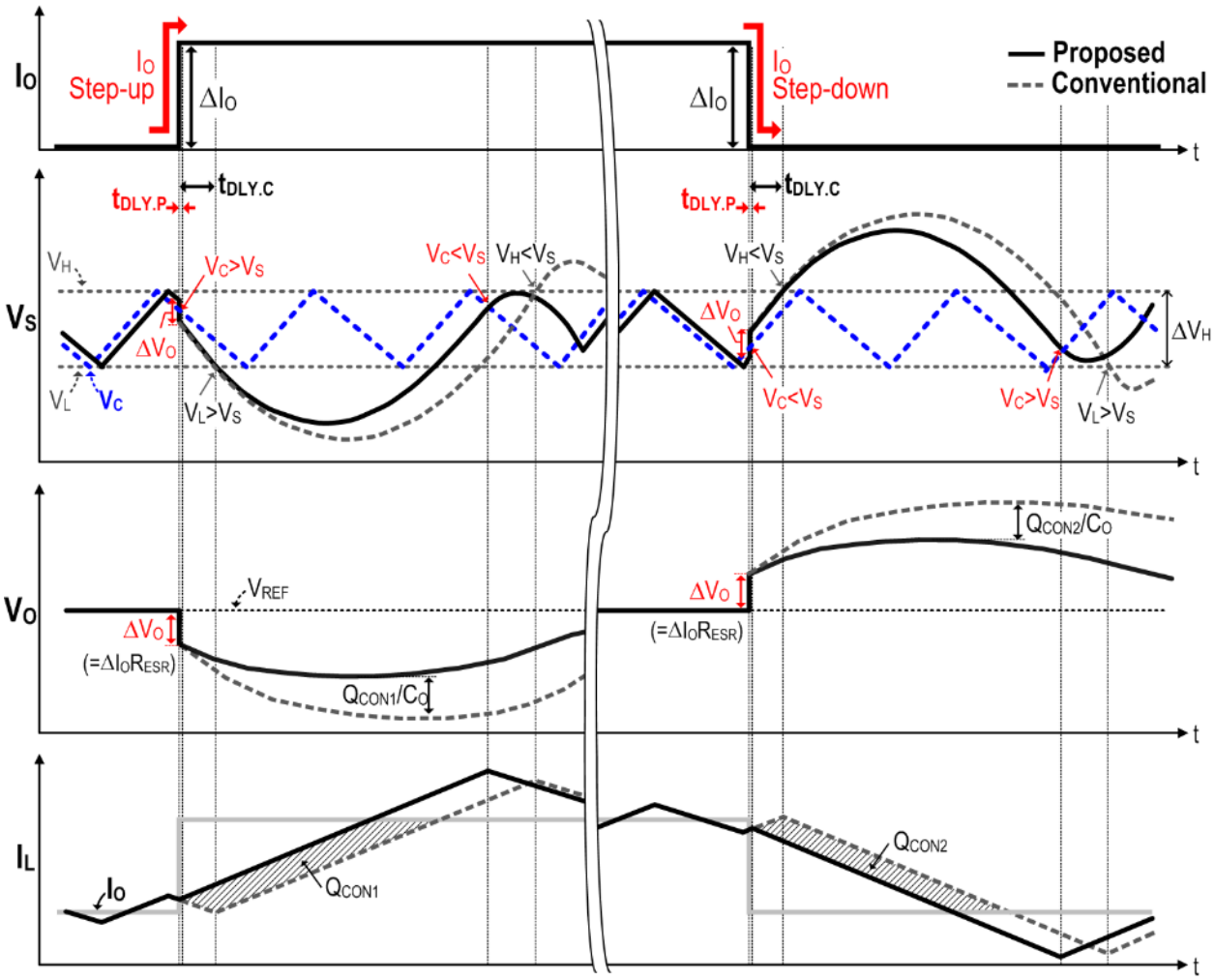


Figure 4.5. Timing diagram of the Dual-RC hysteretic controller at I_O step-up/-down.

Figure 4.5 shows the detailed operation waveforms of the proposed control at load transient. In response to a load step-up of ΔI_O, the voltage drop (ΔV_O) across R_{ESR} is given as

$$\Delta V_O = R_{ESR} \times \Delta I_O . \tag{4.3}$$

Through the feedforward path by C_S, V_S immediately steps down. In the conventional hysteretic control, the V_S has to cross the fixed hysteretic window boundaries, V_H and V_L (in Figure 4.3), triggering the high-side switch M_P and inducing the transient delay $t_{DLY.C}$. On the other hand, the proposed control scheme has a narrow effective hysteretic window due to the real-time slope-tracking reference V_C. This enables instant response in the proposed control, achieving a much shorter delay $t_{DLY.P}$ than the conventional case ($t_{DLY.P} < t_{DLY.C}$) as shown in Figure 4.5. The short delay leads to minimizing the response time and the voltage undershoot at V_O. When I_O steps-down, low latency is attained in the complementary manner. This not only accelerates the load transient response, but also reduces supply voltage variation.

4.2.2 Phase 2: Load Regulation with Reset Control

The proposed DAB controller in Figure 4.3 can achieve fast transient response with fixed f_{SW} by simply employing another RC filter with the duty generator from the hysteretic controller. However, this control suffers from a poor load regulation due to the offset in the RC matching filters. The RC filter is popularly used to detect the inductor current I_L continuously without power consumption [Nabeshima-04, Lee-15, Lee-17, Li-09, and Song-14]. However, as the sensing node V_S equals $I_O R_{DCR}+V_O$, as discussed in Section 1.2.3, this sensing scheme contains the DCR offset, which is proportional to I_O, creating poor load regulation. To overcome this issue, employing an error amplifier on the hysteretic loop (in Figure 4.3) compensates for this V_O variation. However,

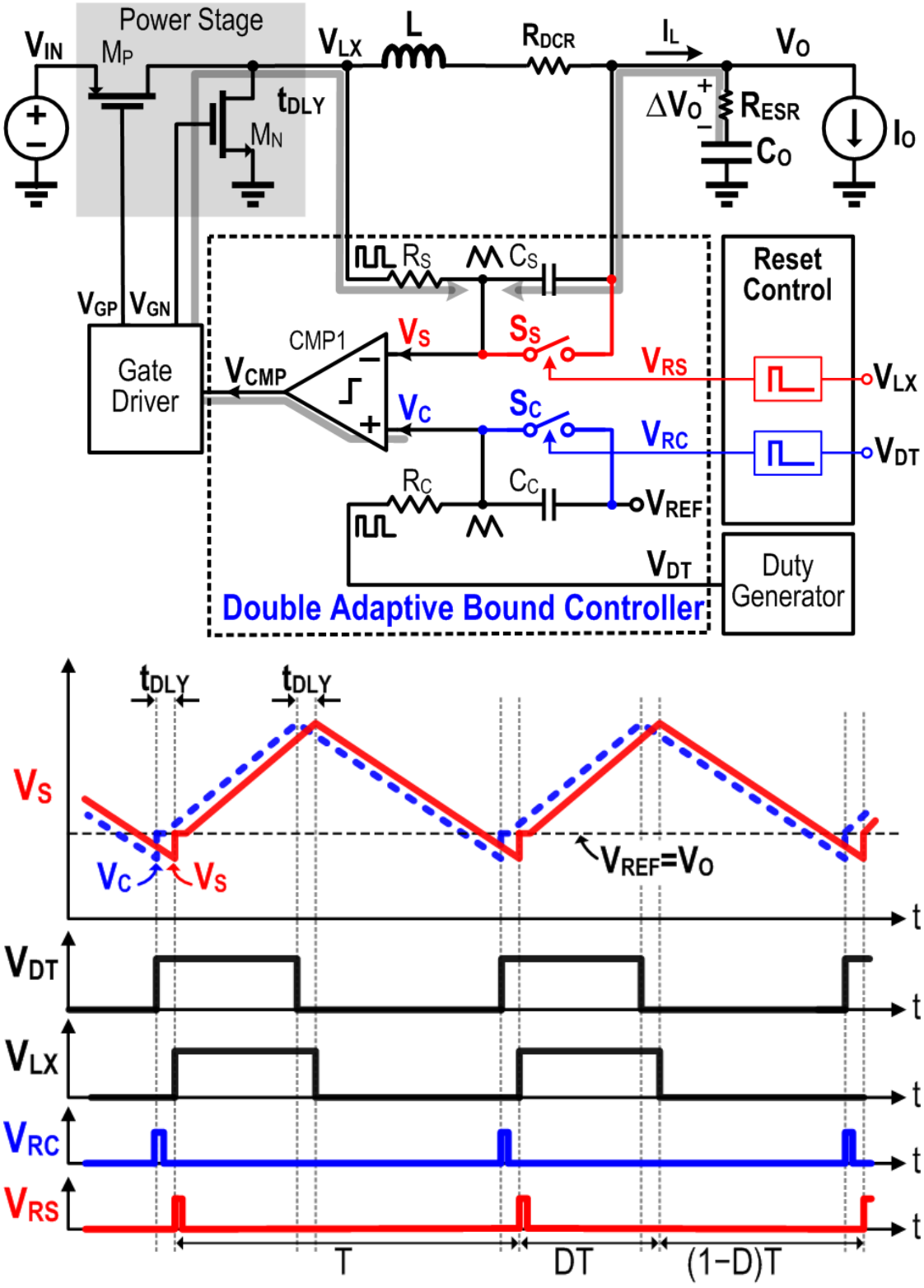


Figure 4.6. Block and timing diagram of the DAB controller with reset control.

this increases the design complexity, silicon area and power consumption, losing the merit of the simple structure of the hysteretic controller.

Instead of that, the DAB controller evolves from the previous concept by employing the reset cancellation technique with two switches (S_S and S_C) across C_S and C_C, respectively, as depicts in Figure 4.6. In every switching cycle, the technique generates the short pulse to turn on the switches S_S and S_C at the rising edge of V_{LX} and V_{DT} to initiate V_S and V_C to V_O and V_{REF}, respectively. Then, any offsets that stored on C_S and C_C are discharged, forcing V_O=V_{REF}, as shown in the waveforms of Figure 4.6. This offset cancellation happens in sequence: at the rising edge of V_{DT}, V_C steps up to V_{REF} and intersects with V_S during high V_{RC}, then V_S resets to V_O during high V_{RS}, with inherent propagation delay t_{DLY}. Consequently, the proposed controller achieves decent V_O load regulation without degrading the transient performance and constant f_{SW}.

4.3 Hybrid Digital-Assisted DAB Converter

As discussed in the design challenges of Section 4.1, the portable applications conventionally implement two modes, active and sleep, to accelerate performance and, at the same time, extend runtime. To support these portable applications, which repetitively and drastically flip operation modes and thus needs steady transient performance and light-load efficiency, the hybrid digital-assisted DAB converter is proposed with a digital autonomous mode manager (AMM), including four operation modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), transient enhance mode (TRAN), and pulse skipping mode (PSM). In this section, an overall system architecture is introduced with the state machine first. Then, three modes, ‘TRAN’, ‘DCM’, and ‘PSM’, are described. The operation principle of ‘CCM’ was explained in the previous DAB control section as a nominal operation. Besides, load transient and light load

sensors are also implemented with only digital circuits, accomplishing the compact and low-power converter. Also, the single control loop with the digital-assisted AMM enables seamless mode transition.

4.3.1 Full System Implementation

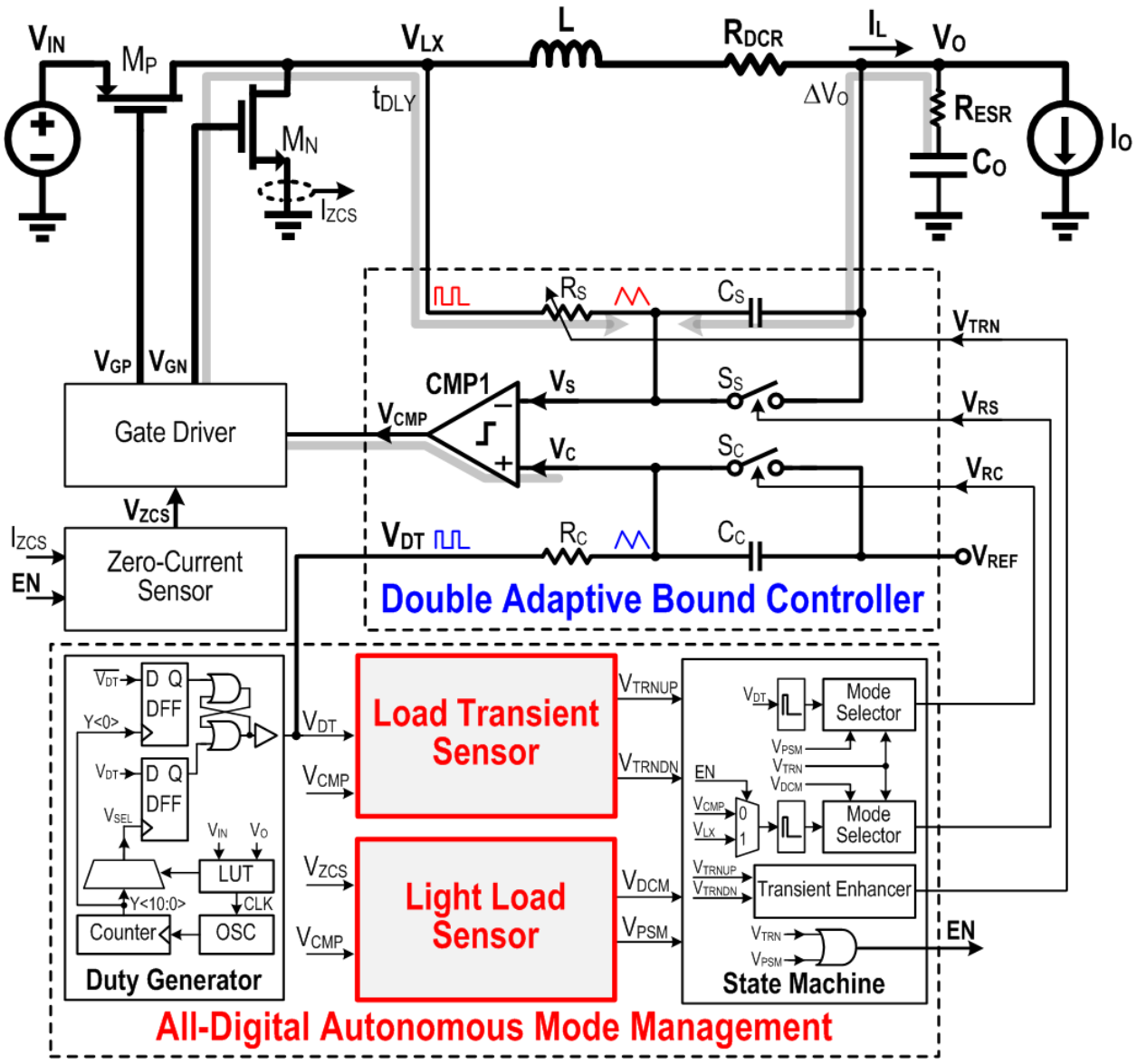


Figure 4.7. Circuit block diagram of the hybrid digital-assisted DAB controlled power converter.

Figure 4.7 shows the overall block diagram of the proposed buck converter, which contains a DAB controller, a power stage, a gate driver, a zero-current sensor (ZCS), and a digital autonomous mode manager (AMM). Assisted by the digital AMM, the DAB controller configures the four modes by controlling two switches S_S and S_C across C_S and C_C, respectively. As the timing information of V_{DT}, V_{LX}, and V_{ZCS} is sensitive to load condition, the load transient and light load

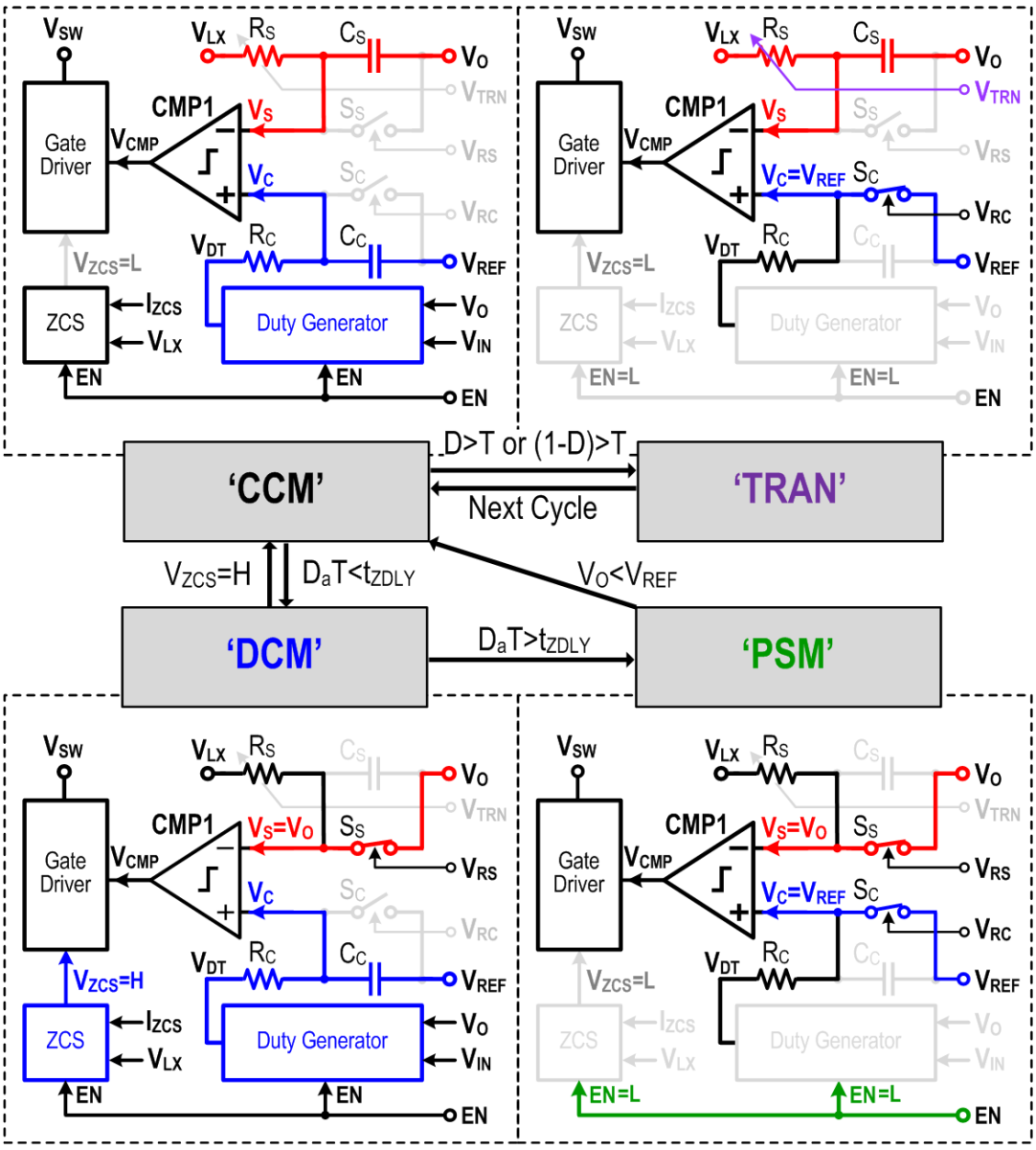


Figure 4.8. State machine with the corresponding operations in the proposed converter.

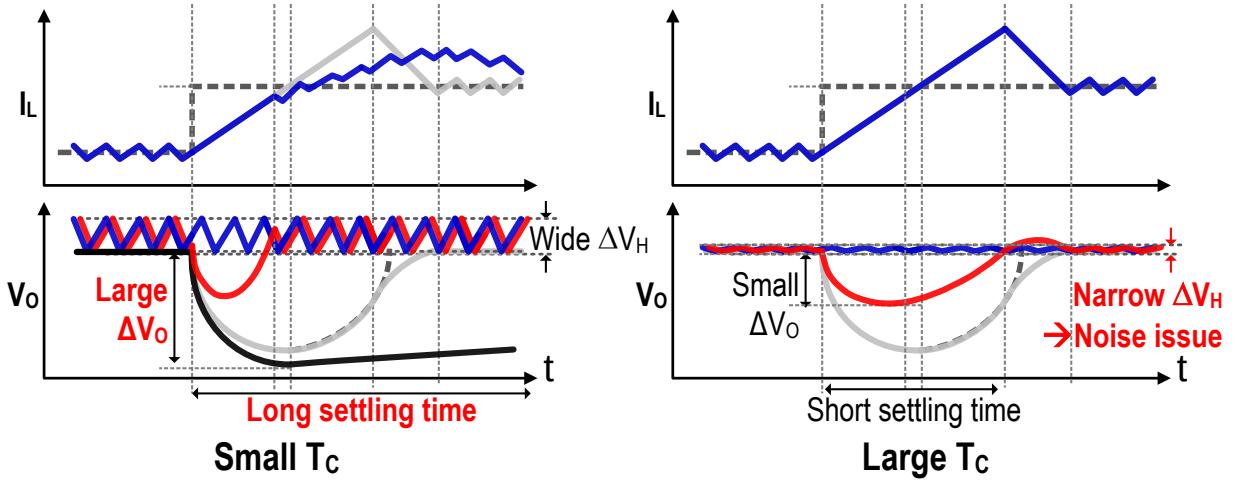


Figure 4.9. Trade-off of the RC matching filter design in the hysteretic control.

sensors in the AMM are digitally implemented to reduce quiescent power and improve density. Also, thanks to the single control scheme, the converter achieves the seamless mode transition with minimum V_O variation. The four modes, 'CCM', 'TRAN', 'DCM', and 'PSM', are controlled by the state machine as illustrated in Figure 4.8.

4.3.2 Transient Enhance Mode (TRAN)

In the current-mode hysteretic controller, the RC filter design is essential for optimizing the load transient, which is important for achieving fast transient and settling time. [Nabeshima-

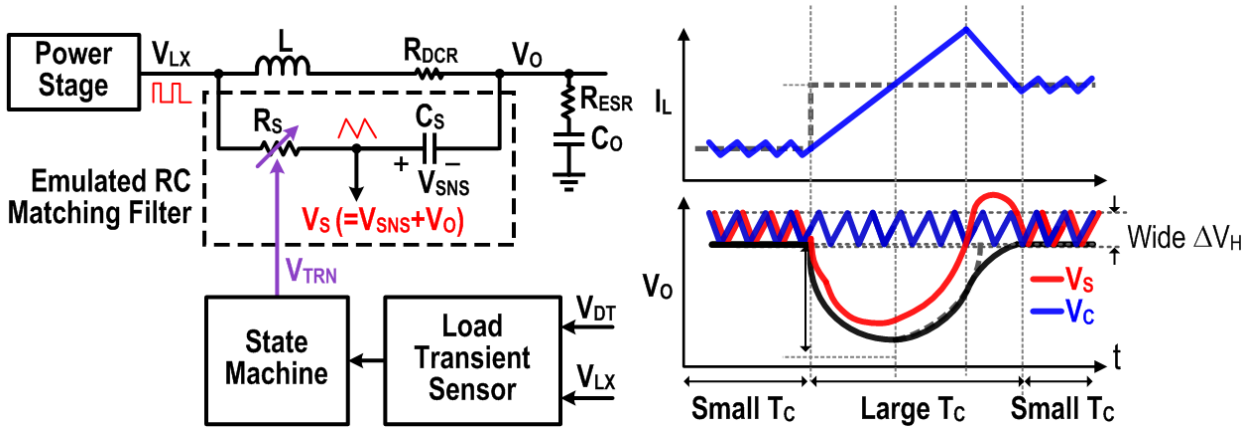


Figure 4.10. Design strategy of the transient enhance mode 'TRAN' and its concept waveforms.

04]. As illustrated in Figure 4.9, with small time constant (T_C) of the RC filter, the transient response is slower than using its larger T_C. However, with large T_C, the sensed node V_S should be narrowed, which degrades the noise immunity in the hysteretic controller.

To overcome this, the proposed controller employs transient enhance mode 'TRAN', which detects the drastic load transient first, adaptively controls T_C by tuning R_S in the R_SC_S matching filter as illustrated in the waveforms of Figure 4.10. For example, during steady state, the controller regulates V_O as the nominal 'CCM', which uses the same small T_C as the two RC filters, i.e., R_SC_S=R_CC_C. This creates a large triangular swing for V_S and V_C, securing the control operation without noise. On the other hand, when the tremendous load step-up/down occurs, the control detects the load transient first and moves into 'TRAN'. Here, the control adjusts R_S to induce large T_C in the R_SC_S filter, slows down the recovery of V_S, and thus expands the turn-on/off time of the

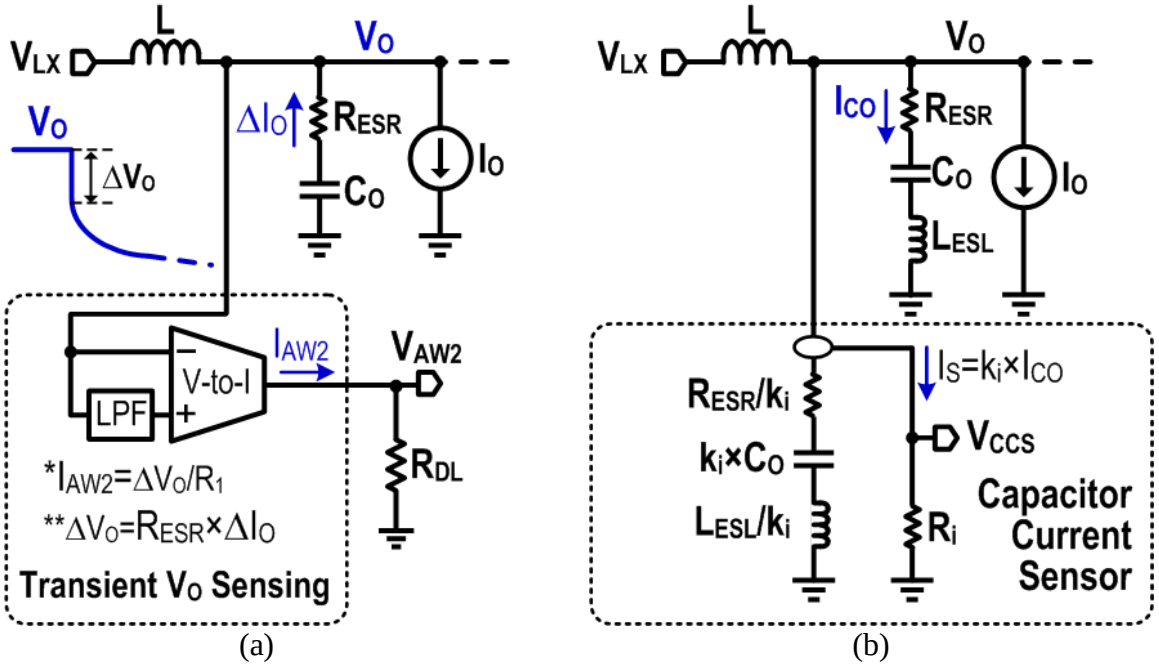


Figure 4.11. Reported analog load transient sensors: (a) transient V_O sensing and (b) capacitor current sensor.

high side switch M_P in the power stage for fast V_O recovery. Once V_O recovers, the control mode changes back to 'CCM'.

To utilize TRAN, the load transient detection is essential. The transient V_O detector method described in [Lee-17] and capacitor current sensing method described in [Chien-15 and Huang-16] , as illustrated in Figure 4.11, can detect the load step directly without a large delay in the average I_L sensor. However, as the transient V_O detector senses the equivalent series resistance (R_{ESR}) in C_O, the sensing resolution is sensitive and is degraded by the mismatch between the reference and R_{ESR}. Also, the capacitor current sensing method detects capacitor charging current I_{CO} by matching the impedance of the internal sensing capacitor C_S with C_O impedance. However, due to the C_O variation and parasitics on the sensing path on C_S, this also affects the sensing resolution.

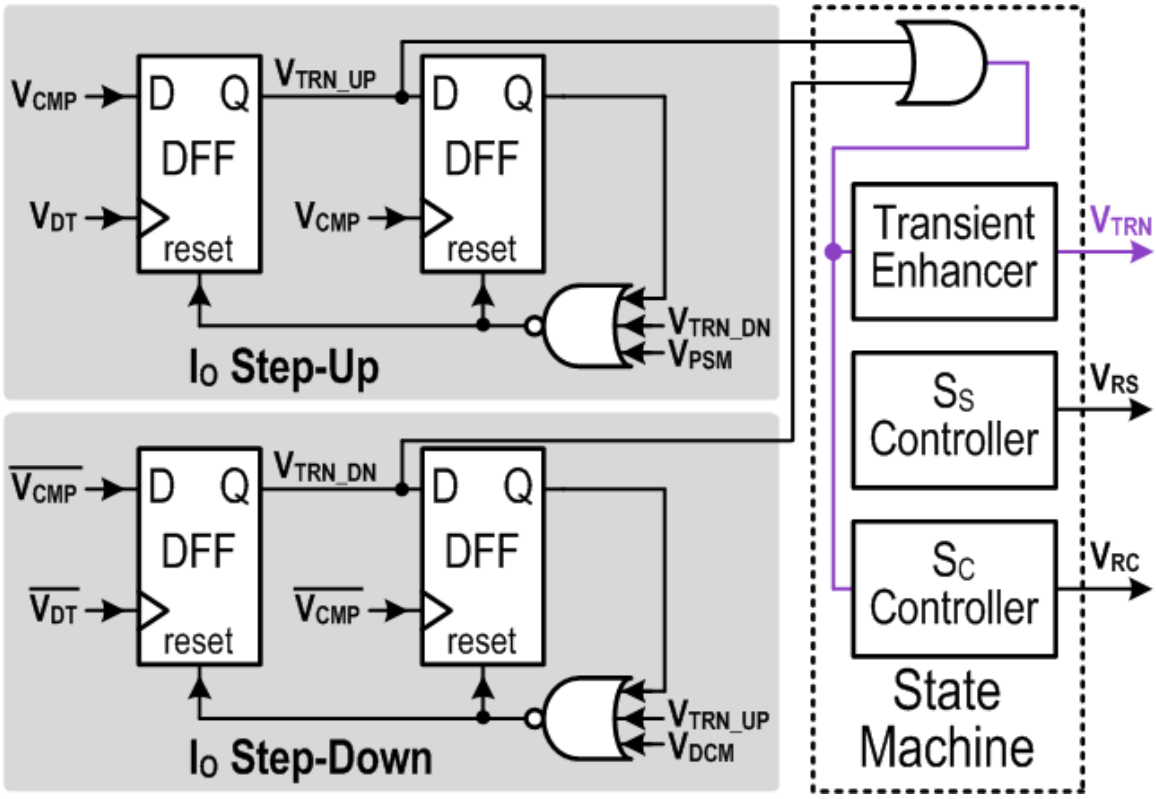


Figure 4.12. Simplified AMM with the proposed digital load transient sensor.

Hence, both techniques require high-resolution analog trimming circuits as well as an additional comparator, which consume extra power and area in the controller.

To avoid using extra analog circuits, the proposed load transient sensor implements only digital circuits by using the inherent hysteretic control operation. Normally, in the conventional switching converter, the switching node V_{LX} goes high and low sequentially in steady state in one switching cycle. When load transient occurs in the hysteretic control, V_{LX} is instantly turned on and stays on for more than one cycle period. Also, when load step-down occurs, V_{LX} goes low immediately and stays off for more than one cycle. By using these fundamental characteristics in the hysteretic control, the load transient sensor can detect the load current change by employing only digital circuits, as depicted in Figure 4.12.

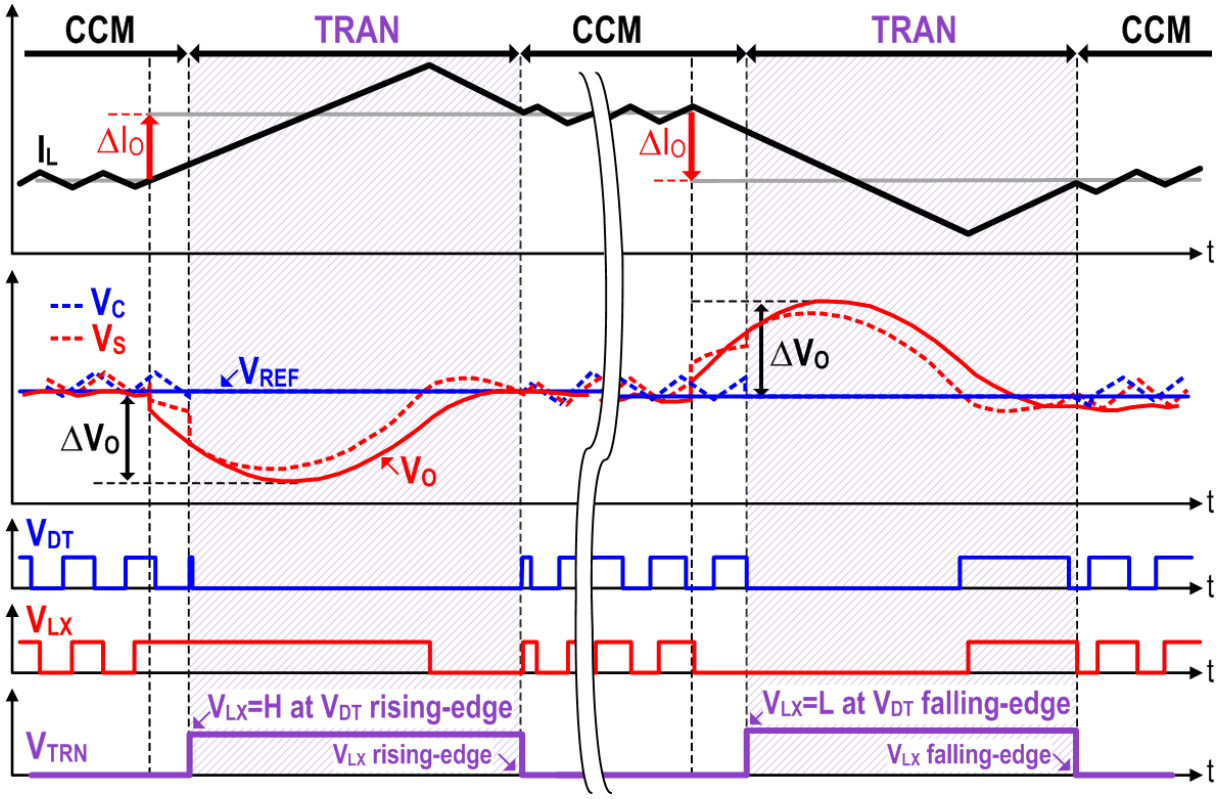


Figure 4.13. Timing diagram of the 'TRAN' mode.

Figure 4.13 illustrates the timing diagram when load transient occurs. At the beginning, the control operates 'CCM' in steady state. When the I_O step-up occurs, V_O steps down due to the voltage drop across R_{ESR} in C_O ($=R_{ESR}\times I_O$) and induces the V_S drop to intersect with V_C instantly, turning on V_{LX} as discussed in the DAB control scheme. As the inductor current I_L continuously rises at the rate of $(V_{IN}-V_O)/L$, the increased current ΔI_L during one cycle period T can be given as

$$\Delta I_L = (V_{IN} - V_O)T/L. \tag{4.4}$$

When ΔI_L is smaller than the transient current ΔI_O, i.e., $\Delta I_L<\Delta I_O$, V_O cannot recover and continuously decreases, and thus stays high more than one cycle period. If V_{LX} remains high at the rising edge of the V_{DT}, the control mode changes to 'TRAN'. Then, the proposed AMM generates

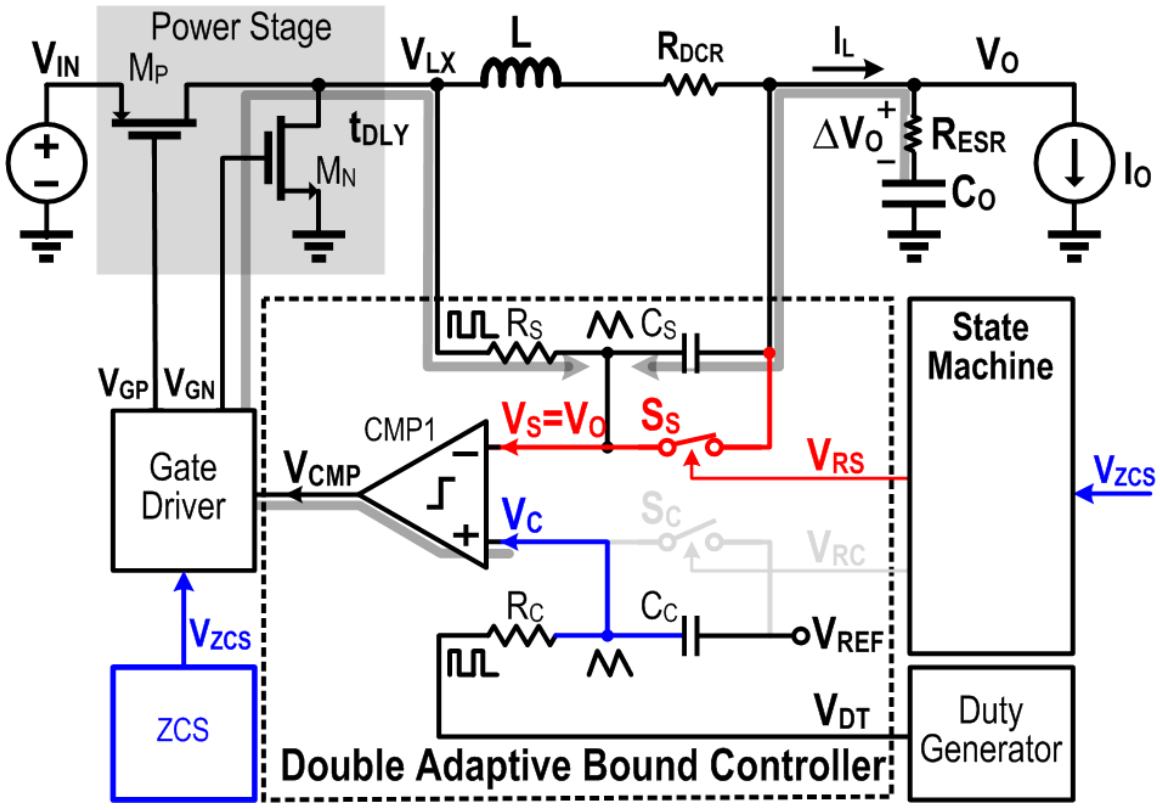


Figure 4.14. Simplified DAB controller at 'DCM'.

V_{TRN} to adjust R_S to a large value to extend the turn-on/off time. Meanwhile, high V_{RC} closes switch S_C and V_C equals V_{REF}, as shown in Figure 4.8, inducing minimized V_O droop and fast V_O settling. The 'TRAN' mode continues for one switching cycle; in other words, after V_{LX} turns high again, the control mode returns to 'CCM'. Likewise, at load step-down, V_O and V_S instantly step up, and V_{LX} turns off and stays off more than one cycle in the complementary manner. Thus, if V_{LX} remains low at the falling edge of the V_{DT}, i.e., one cycle later, the control mode changes to 'TRAN'. During 'TRAN', the AMM not only adjust T_C to extend the turn-on/off time, but also disables the zero current sensor as illustrated in Figure 4.8. This enables the negative I_L to discharge V_O with fast settling, preventing V_O over-charging and energy loss. This process can be employed by only using digital circuits, facilitating simple control and high power density.

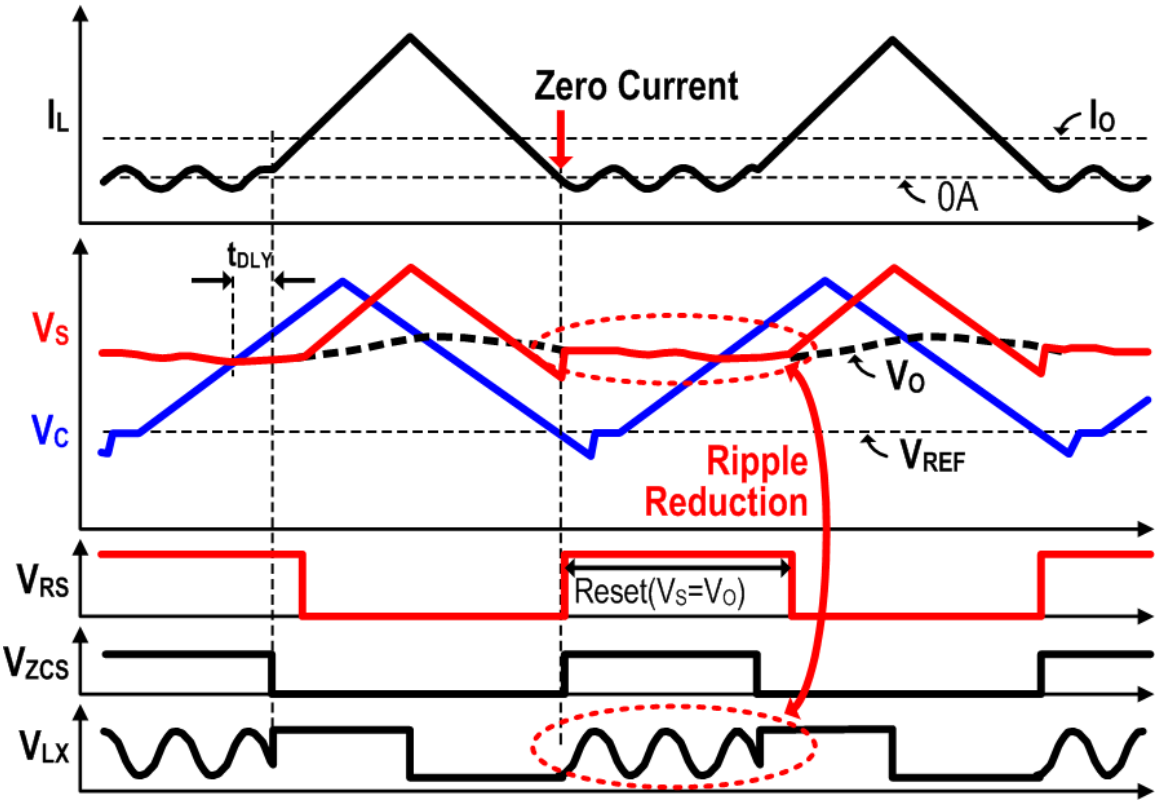


Figure 4.15. Key operating waveforms at 'DCM'

4.3.3 Discontinuous Conduction Mode (DCM)

When the load current is reduced, I_L goes below zero. As this negative current discharges output voltage V_O in the buck converter, it requires more charging current to maintain V_O regulation, increasing conduction loss and degrading overall efficiency. In order to avoid the negative I_L, the discontinuous conduction mode (DCM) is usually implemented in the power converter. 'DCM' can be realized easily by adding a zero current sensor (ZCS) as shown in Figure 4.14. The waveforms of 'DCM' are illustrated in Figure 4.15. V_{ZCS} goes high when I_L goes below zero, triggering 'DCM' directly. Then, the state machine in AMM disables the gate driver, which makes a high impedance node on V_{LX}, creating a resonant ripple which is made by L and the parasitic capacitance on V_{LX}. At the same time, the state machine turns on switch S_S in the DAB controller and connects V_S to V_O as shown in Figure 4.7. Hence, the resonant ripple on V_{LX} does not affect V_S (=V_O). Then, when V_S crosses V_C, the control mode returns to 'CCM'.

4.3.4 Pulse Skipping Mode (PSM)

Normally, the mobile system employs the deep sleep mode, which disables most of the features, inducing zero current consumption and thus saving the limited battery energy. At light

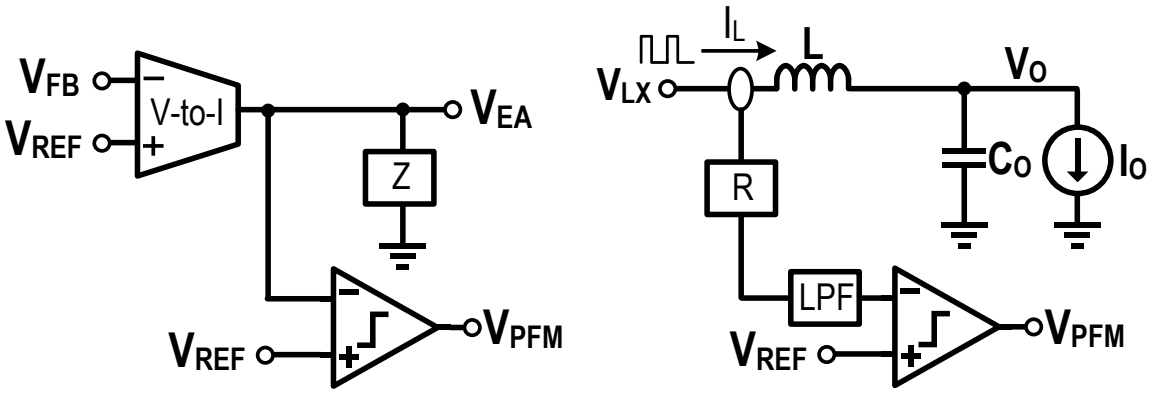


Figure 4.16. Conventional analog light load sensors.

load, the dominant power loss is related to switching frequency. Hence, to improve the efficiency, lowering switching frequency operation, such as pulse skipping mode (PSM), is essential. Conventionally, to implement 'PSM' in the main controller, e.g., the PWM or hysteretic controller, two additional features are required: 1) the light load detector, and 2) the PSM controller.

First, in order to detect the load current in commercial or published converters, the output of the error amplifier or the average I_L with a low pass filter (LPF) are generally used as illustrated in Figure 4.16. However, both techniques limit the sensing speed due to the bandwidth of the compensation network or filter, degrading transient performance especially when load current changes from zero to maximum or from maximum to zero, which requires the fast mode transition between 'PSM' and 'CCM'.

Moreover, the PSM controller is generally implemented as the additional controller as shown in Figure 4.17 [Kim-18]. In this case, another comparator (CMP2) is commonly used to regulate V_O by comparing it with V_{REF} directly. However, the process offset between the two comparators exists, creating an unwanted V_O ripple or even mode transition oscillation. Thus, additional trimming circuits are normally utilized, but this increases silicon area and testg cost.

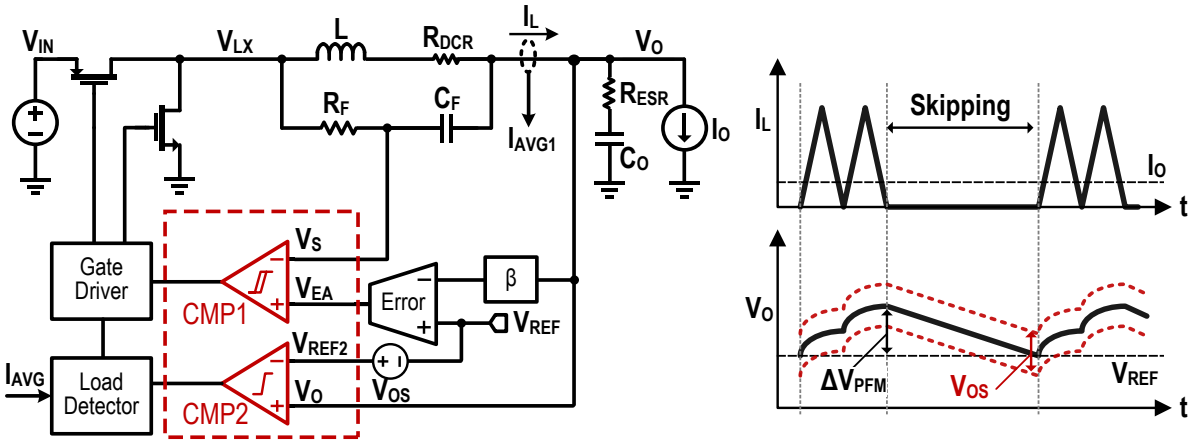


Figure 4.17. Conventional CCM and PWM controller implementation.

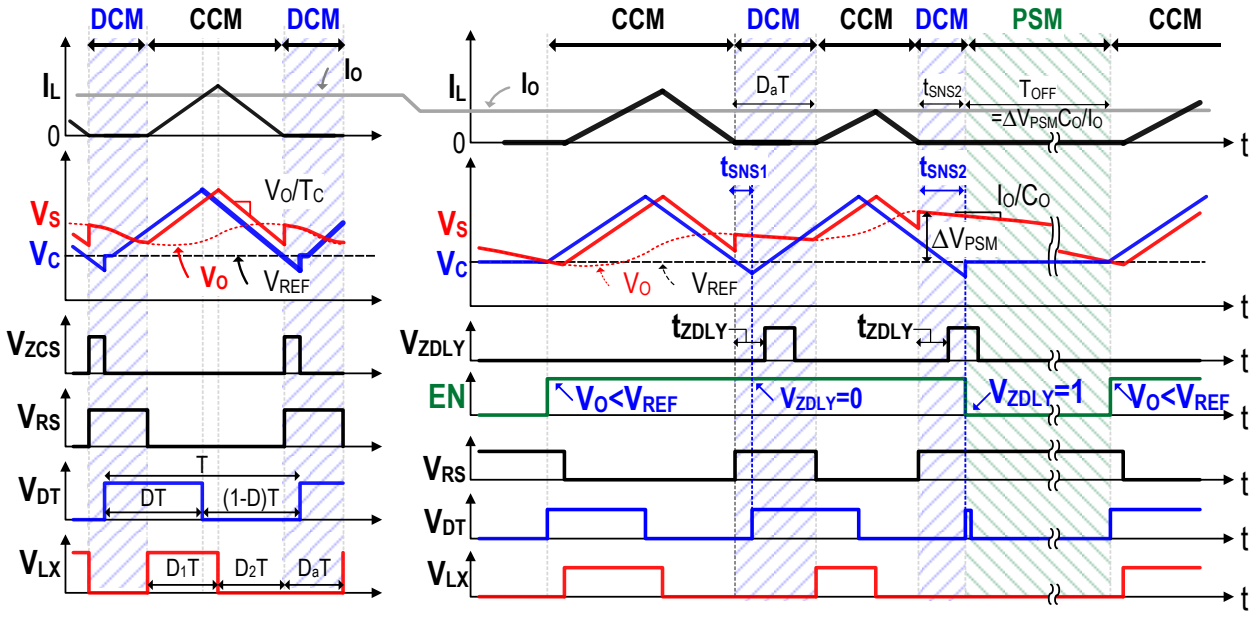


Figure 4.18. Timing diagram at 'DCM and 'PSM' operations.

In the proposed DAB control scheme, the light load sensing can be implemented by only using the timing signals, V_{DT}, V_{LX} and V_{ZCS}. The detailed operating waveforms comparing 'PSM' and 'DCM' are illustrated in Figure 4.18. When I_O further decreases, V_O increases as ΔV_{PSM} and it takes an extended time for V_C to intersect with V_S (=V_O). The extended DCM period D_aT reduces the on-duty of M_P and the peak I_L. Taking advantage of this characteristic, the light load sensor inserts the fixed delay t_{ZDLY} between V_{ZCS} and V_{ZDLY} to compute the load current. When V_{ZDLY} is zero at the rising edge of V_{DT} (t_{SNS1}<t_{ZDLY}), the state machine changes the control operation to 'CCM' at the beginning of the next cycle, followed by 'DCM'. In contrast, if V_{ZDLY} is high at the rising edge of V_{DT} and t_{SNS2}>t_{ZDLY}, the state machine changes the mode to 'PSM'. This disables the duty generator and ZCS to minimize the quiescent current. Meanwhile, V_{RS} and V_{RC} go high to turn on S_S and S_C, respectively, forcing V_S=V_O and V_C=V_{REF}. 'PSM' continues until V_O<V_{REF} (=V_S<V_C) and the operation period (T_{OFF}) is decided by $\Delta V_{PSM}\times C_O/I_O$. Thanks to the simple implementation of 'PSM' in the single DAB controller, seamless mode transition is easily attained for tight load

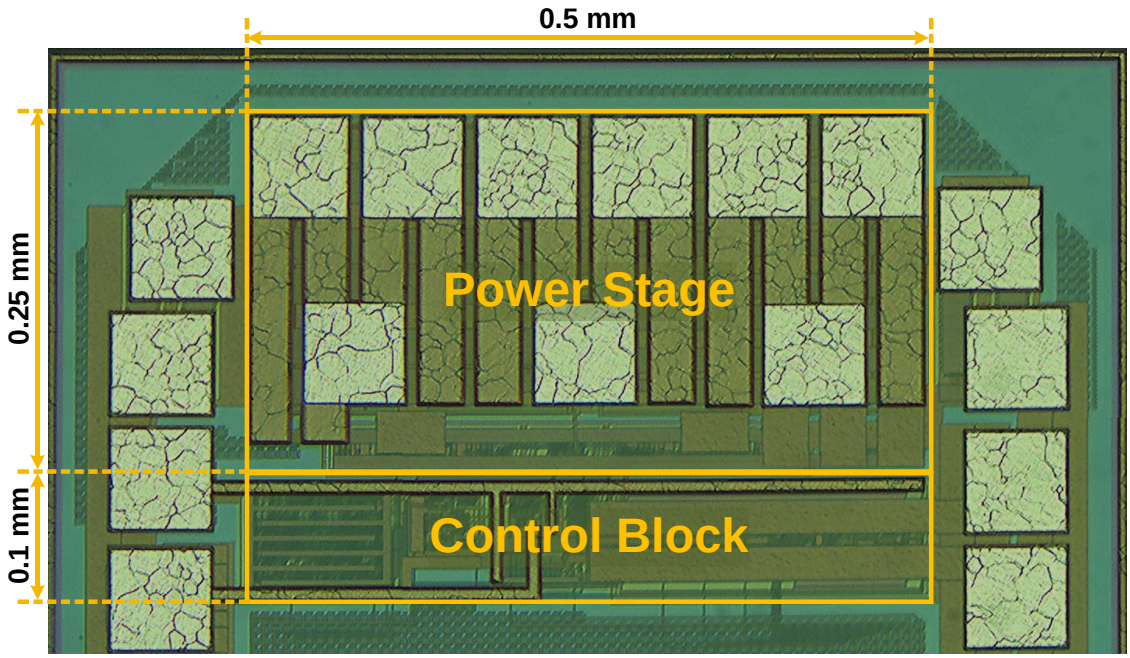


Figure 4.19. Chip micrograph.

regulation. In addition, as only one analog circuit *CMP1* is turned on during 'PSM', the quiescent power consumption is also minimized. Consequently, 'PSM' can be realized by using all-digital sensing and control circuits to obtain high power density and low latency.

4.4. Experimental Verification

A prototype of the converter is designed and fabricated in a 0.18 μm CMOS process. Figure 4.19 shows its chip micrograph. The active die area is measured as 0.175 mm^2. Operating at a nominal switching frequency of 10 MHz, the converter employs a 200 nH inductor and 2.2 μF output capacitor C_O and delivers a maximum load current of 1 A. To be feasible for battery-operated mobile devices, the converter supports a wide range from 3 V to 5 V of V_{IN} and from 0.5 V to 2.5 V of V_O. Unless otherwise specified, the following results are measured under the nominal condition, where V_{IN} = 3.3 V and V_O =1.6 V.

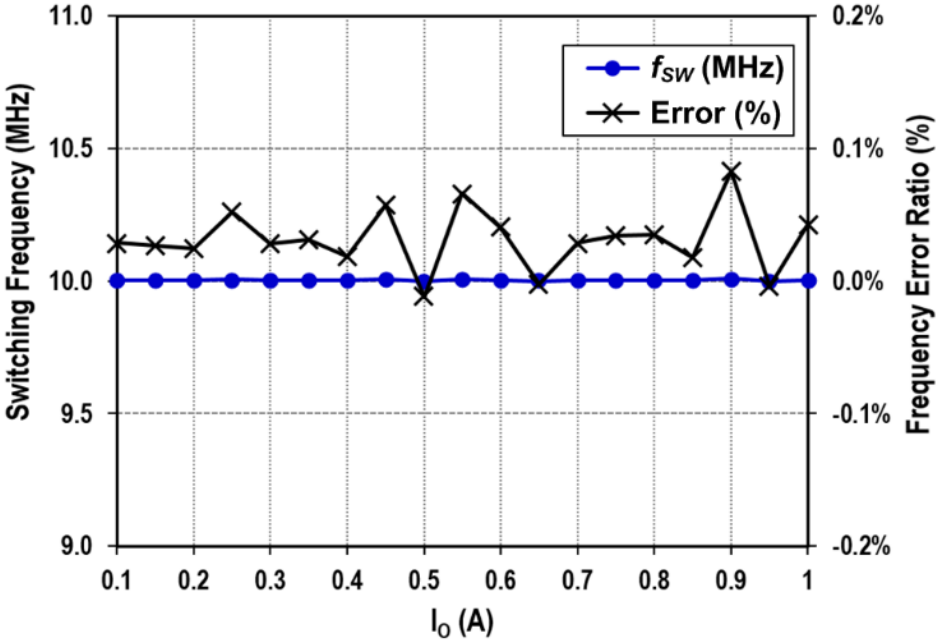


Figure 4.20. Measured switching frequency and frequency error ratio.

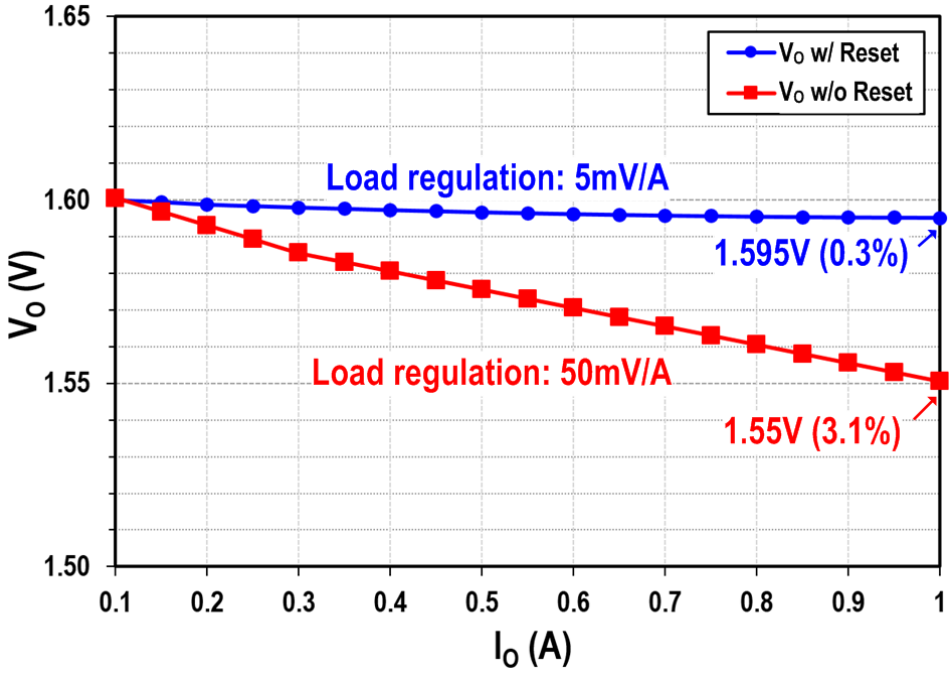
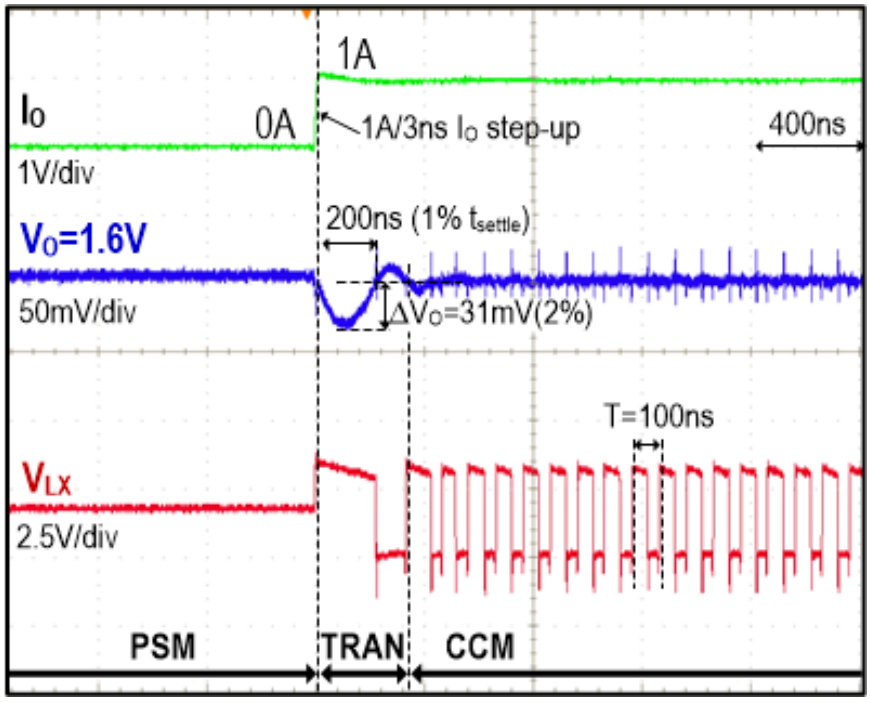
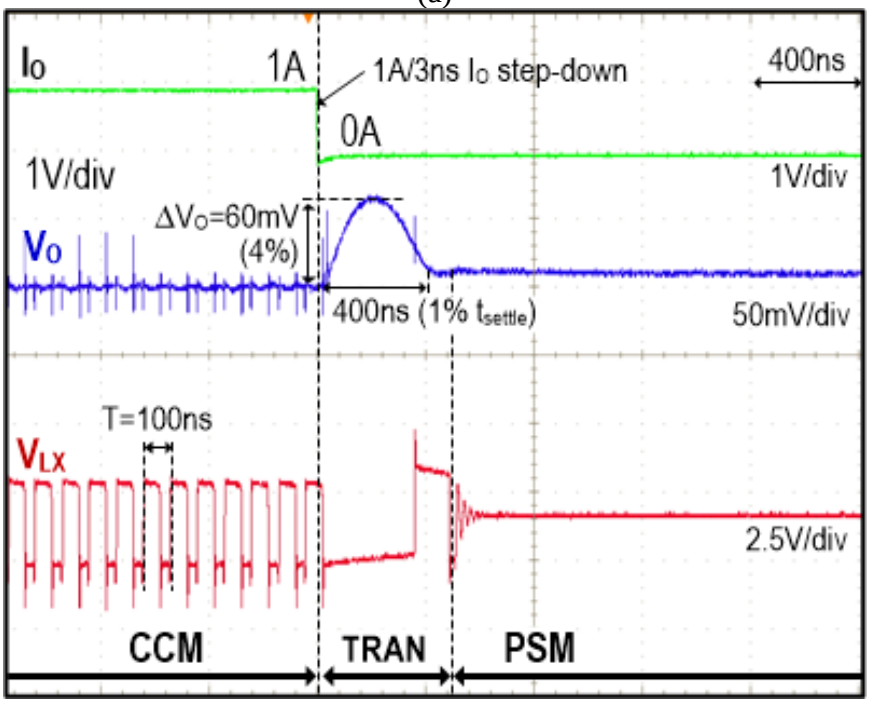


Figure 4.21. Measured load regulation with and without the reset control.



(a)



(b)

Figure 4.22. Measured load transient performance at (a) load step-up, and (b) load step-down.

Figure 4.20 validates the switching frequency variation with different I_O conditions. Thanks to the clock synchronization feature, the proposed DAB control provides 10 MHz switching frequency within ±0.1% of error ratio. Compared to [Lee-15], which has ±0.2% of frequency variation with 6-bit trimming circuits, the proposed design has less frequency variation with simple structure. Figure 4.21 demonstrates the improvements on load regulation using the DAB control with the reset controller. The reset control technique successfully eliminates the offset in the RC matching filters and achieves 5 mV/A load regulation, which is 900% improvement from 50 mV/A load regulation without the reset controller.

Figure 4.22 shows the results of the proposed DAB controller in the worst-case scenario, in which the system power flips between no load (0 A) and full load (1 A). In response to 1 A/3 ns I_O step-up, the proposed design is immediately activated with 100% duty by entering 'TRAN', retaining droop voltage ΔV_O below 31 mV with 1% settling time (t_{settle}) of 200 ns. For I_O step-

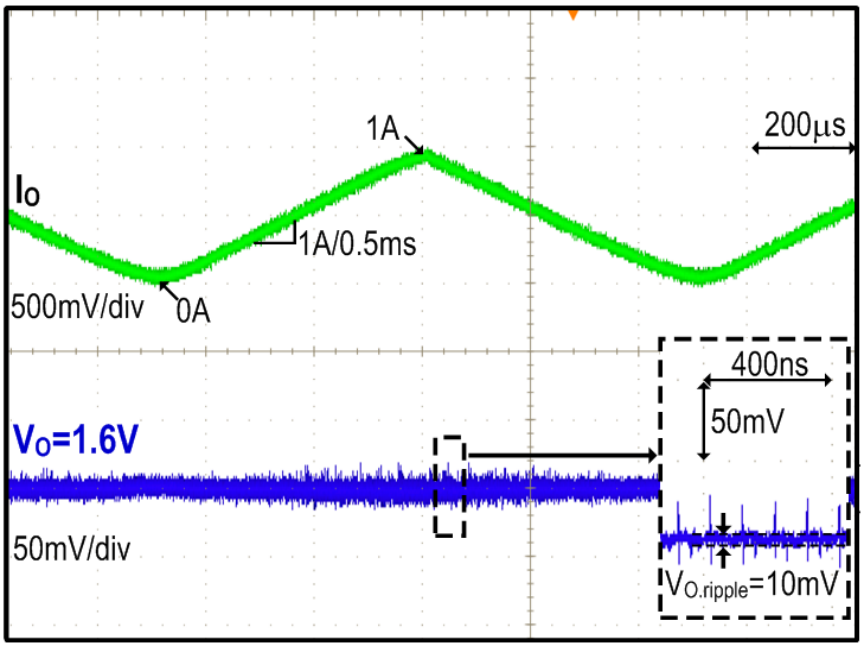
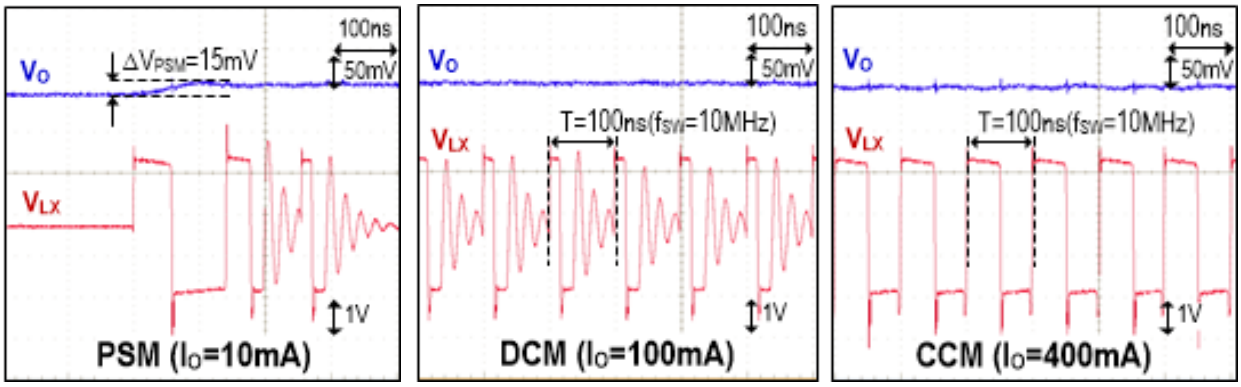


Figure 4.23. Measured mode transient performance with load sweep from 0A to 1A.

down, ΔV_O is 60 mV with 1% t_{settle} of 400 ns. The corresponding V_{LX} node waveforms show the extended turn-on/-off time during the transients in the proposed case. Figure 4.23 measures I_O and V_O to verify the mode transient performance. Sweeping I_O from 0 A to 1 A linearly in 1 ms, the single control loop with the digital AMM achieves the seamless mode transitions among 'CCM', 'DCM', and 'PSM' without any supply glitch and attains less than 0.3% V_O variation.



(a) (b) (c)

Figure 4.24. Measured results of the V_O and V_{LX} waveforms to verify the PSM/DCM/CCM operating modes.

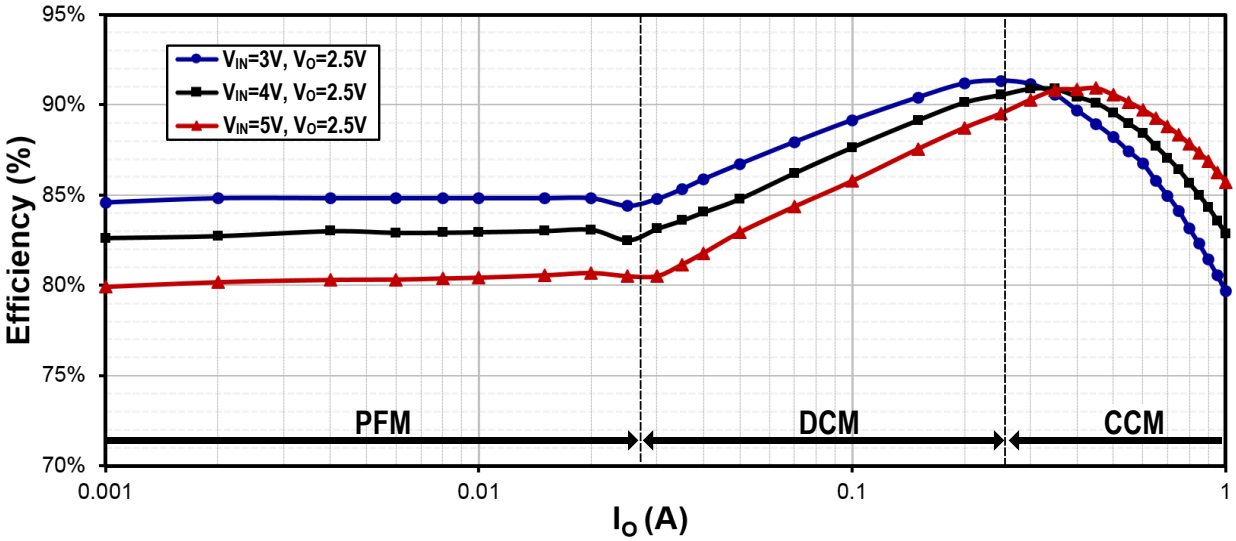


Figure 4.25. Measured power efficiency plots.

Figure 4.24 provides the measured results of V_O and V_{LX} to verify each operation modes, 'PSM', 'DCM', and 'CCM'. The output voltage ripple during 'PSM' is 15mV, which is less than 1% of V_O. Also, at 'CCM' and 'DCM', the switching frequency maintains 10MHz. Measured efficiencies in different I/O conditions are provided in Figure 4.25. As shown in the figure, 'PSM' is efficient at low output power whereas 'CCM' is highly efficient at high power. In the

Table 4.1. Performance Comparison

Control Scheme		[Lee-15]	[Yang-18]	[Kim-18]	This work
Control Scheme		QCIE	P-Hysteretic	T-PID	Hybrid DAB
Input Voltage V_{IN}		2.7-4.5V	4.5-5.5V	1.8V	3-5V
Output Voltage V_O		2V	1.8-3.3V	0.5-1.5V	0.5-2.5V
Conversion Ratio (V_{IN}/V_O)		2.25	3.1	3.6	10
Inductor L_O		4.7μH	-	220nH	200nH
Capacitor C_O		10μF	-	4.7μF	2μF
Load Transient Response	I_O step-up	0 to 400mA	200 to 800mA	20 to 420mA	0 to 1A
	$t_{settling}$	4.8μs	7.3μs	1.8μs	200ns
	ΔV_O	35mV	53mV	40mV	31mV
Frequency f_{SW}		1MHz	1MHz	10MHz	10MHz
Peak Efficiency		95.5%	92.4%	90%	91%
Technology		350nm	55nm	65nm	180nm
Active Chip Area		0.518mm^2	0.85 mm^2	0.14mm^2	0.175 mm^2
Max. Power Density		1.6W/mm^2	3.88W/mm^2	10.7W/mm^2	14W/mm^2

intermediate level, ‘DCM’ provides better efficiency. With the combination of the proposed DAB controller and digital AMM, the mode is automatically managed with load current to retain high efficiency. As a result, the efficiency stays above 80% over 99.9% of the full power range with a peak value of 91%.

Finally, as a summary, Table 4.1 compares this work with the prior art. Owing to the hybrid digital-assisted DAB converter with ‘TRAN’, which is controlled by a digital AMM, this design accomplishes the lowest voltage drop and fastest transient response even with one most stringent and full-range load transition, from no load to maximum, with the smallest C_O test condition. Furthermore, due to implemented DCM and PSM modes, the AMM helps the converter to retain high efficiency over one of the widest power ranges, without a glitch V_O during mode transition. Area-efficient and simple circuit design leads to the highest power density with the traditional technology node. In addition, the simple RC filter with the comparator design enables the highest conversion ratio.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

Modern mobile applications have been developed with the trend towards improving performance, integrating further multiple functions in the limited space, and providing long runtime. Hence, high-density power converters are required to follow this trend. This dissertation proposed advanced system architectures, control schemes, and circuit designs to overcome the design challenges to enhance the power density of the DC-DC converters. The designs presented in this dissertation were developed not only to improve power density, but also to provide the basic features for the mobile applications, such as high efficiency over the wide-load-range, fixed frequency, low EMI noise, fast transient, high load regulation, and wide-input/output operation.

The research began by introducing the all-NMOS 3-level power converter to minimize the system power distribution plan. Due to the half-voltage swing, the 3-level converter allows high switching frequency, which reduces passive components size. Also, as the battery voltage can be used as the supply voltage directly even with the thin-oxide device, an external power converter stage can be eliminated, thus improving system efficiency. Implementing all-NMOS devices also allows minimizing gate driving loss. To handle all-NMOS power switches even with varied supply voltage, the isolated bootstrap circuit was developed to overcome the voltage charging issue for the 3-level high-side gate driving. Moreover, a precise sub-ns dead-time controller was developed, which is integrated in the gate buffer stage, minimizing the dead-time power loss without sacrificing reliability. The proposed 3-level buck converter was fabricated using a 0.35-μm CMOS process. Experimental results verified that the proposed converter can operate from 3 V to 6 V of

V_{IN} without on-resistance variation, enabling the use of the varied battery voltage for V_{IN}. Moreover, the converter can regulate V_O as low as 0.4 V, converted from 6 V of V_{IN}, achieving a minimum duty ratio of only 6.7% at 20 MHz f_{SW}, which is 50% less than the best level in the prior schemes. The converter can also achieve 0.5 ns dead-time over a load range of 500 mA . Operating at 20 MHz switching frequency, the proposed 3-level converter with sub-ns dead-time controller jointly accomplishes up to 21.5% power efficiency improvement over the current state-of-the-art.

The multiphase architecture has the benefit of achieving higher power density than that of the single-phase architecture, while increasing power delivery. Hence, a 25 MHz, 4-phase synchronized adaptive window (SAW) hysteretic converter was presented. A SAW hysteretic control was employed to facilitate ultra-fast transient response and inherent clock synchronization, which ensures current balancing among phase sub-converters. The control also enables a wide range of programmable V_O for dynamic voltage scaling, thereby saving system power efficiently. As the all-phase operation degrades the light-load efficiency, a 1-Cycle active phase count scheme was introduced to maintain high efficiency over a wide load range without degrading transient speed. A design prototype was fabricated in a 0.35-μm CMOS process with an active die of 1.88 mm^2. It operates at 25 MHz with a well-regulated V_O ranging from 0.3 V to 2.5 V. It achieves more than 80 % efficiency over 96.7 % of the output power range, with a peak value of 88.1%. Simple circuit structure leads to a power density of 3.98 W/mm^2, which is comparable to the power density of the current state-of-the-art. In response to 4-A load step-up/down, the converter achieves 103 mV/123 mV of V_O undershoot/overshoot with 1% settling time of 190 ns/237 ns, respectively.

To integrate all design features for mobile applications in the limited area, the hybrid digital-assisted double adaptive bound (DAB) converter was presented. The DAB controller

contributes all required design features for mobile applications, such as fixed switching frequency, high V_O regulation, fast transient, and wide-V_{IN} operation. In addition, to support the mode transition, active/sleep, in the mobile application, the DAB controller was combined with the digital autonomous mode manager, providing four modes to fit with the system. This further enhances transient response and achieves wide-load-range efficiency. All-digital implementation in the mode manager avoids the power- and silicon-hungry analog circuits. The proposed techniques have been combined and realized by compact designed circuits, achieving the highest reported chip power density of 14 W/mm^2 with 0.18-μm CMOS process. The design achieves above 80% efficiency over 99.9% of the full power range with a peak value of 91%. Accordingly, this work is appropriate for further integration in compact and low-power portable applications for system-on-chip designs.

All the presented power converters in this dissertation were fabricated and measured successfully to demonstrate the design performance. The effectiveness of the design is successfully verified in the measurement results and the performance comparisons with the state-of-the-art. Considering all needs and integrating all features to meet those needs, the high-density power converter has been realized for the mobile applications.

5.2 Future Work

This research has provided the groundwork to address various design challenges in high density DC-DC converters for the battery-operated mobile applications. Future research and investigations could be conducted in the following areas: designing high-power supplying multilevel converter for the high-end battery charger or future USB applications, designing the fully-integrated multiphase power converter supported by the compact size of the coupled

inductor, and designing the further reduced quiescent consuming converter for future IoT applications.

Recently, the high-speed battery charger has been developed to meet the customer demands for battery-operated applications, including smartphones, laptops, and electrical automobiles. The main idea for reducing the charging time is to increase charging current. However, if the supply voltage is the same as before, due to parasitic resistance in the power train and rechargeable battery, higher charging current generates heat and power loss, which can be calculated as $P=I^2R$, thereby requiring higher supply voltage, which can reduce current in the power train as $P=IV$. A 3-level converter is one of the candidates for this high-end charger, which has twice as much supply voltage as the device breakdown, instead of employing the thick-oxide device. The research presented in the dissertation helps to operate varied supply voltage for the 3-level converter. In addition, the proposed sub-ns dead-time controller not only reduces dead-time loss, but also eliminates the use of the level-shifter in bootstrap circuits and dead-time control loop, minimizing the usage of the high-voltage devices to save area.

The fully-integrated DC-DC converter, which also integrates passive components, can extremely reduce the form factor by eliminating huge external components, thus drastically increasing power density. However, as the size of the passives is related to the switching frequency, a trade-off between the size and efficiency exists. Here, the coupled-inductor can alleviate the integrating challenges due to 1) a smaller size than the two independent inductors, and 2) a smaller inductor current ripple, which can reduce the output capacitor size. In order to realize that the power converter needs to implement with multiphase. Also, to integrate the chips in one die, the compact controller is essential. By designing the multiphase converter with the DAB controller,

which has fixed frequency operation, high output regulation, and compact size, the monolithic DC-DC converter can be achieved.

Lastly, to develops the power converter for future IoT applications, which requires a sub-nA range of quiescent current, the hybrid digital-assisted DAB converter can be used. Due to the digital power computing and pulse skipping mode, which only needs one analog comparator, the quiescent current can be tremendously reduced during no load condition. To further reduce the power, the dynamic biasing technique can be implemented in the main comparator. In addition, as the hybrid converter provides high power density, this is very suitable for the tiny size of the IoT applications.

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BIOGRAPHICAL SKETCH

Bumkil Lee received the B.S., M.S. degrees in electrical engineering from Hanyang University, South Korea, in 2005 and 2007, respectively. He is currently working toward the Ph.D. degree in Department of Electrical and Computer Engineering at Erik Jonsson School of Engineering and Computer Science, the University of Texas at Dallas, Richardson, TX, USA. He joined the Integrated Power System Laboratory (IPSL) in Fall 2014.

From 2005 to 2007, he worked as a graduate research assistant at the Hanyang University, working on the research of display driver IC for LCD/OLED. From 2007 to 2009, he was with Korea Electronic Corporation, Korea, as a Design Engineer in IC Design Group, working on the design of control ICs for piezo sensor and flyback converter. From 2009 to 2014, he was with Samsung Electronics, Korea, as a Design/Senior Engineer in the System LSI Department, working on the design of power management ICs. He joined the Texas Analog Center of Excellence (TxACE), The University of Texas at Dallas in 2014, working on the research of high-speed, high-density power management ICs. He was also a student design intern at Texas Instruments Inc. in Summer 2017. His research interests include analog/mixed signal circuit, high-speed, high-voltage, high-efficient power converters, and integrated power management system design.

Bumkil Lee was the recipient of State Scholarship (Brain Korea 21, 2006) and Best Engineer Award (System LSI, Samsung Electronics, 2013).

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QUALIFICATIONS

Astute, industrious Ph. D. student uniquely qualified in analog and power management IC design. Seven years of professional work/design experience, developing seven commercial products. Published in IEEE conferences. Proficient in process technology, layout, and testing.

EDUCATION

UNIVERSITY OF TEXAS AT DALLAS, Richardson, Texas
Ph.D. Degree in Electrical Engineering 2018

HANYANG UNIVERSITY, Seoul, Korea
Master's Degree in Electronic & Computer Engineering 2007
Bachelor's Degree in Electronic & Computer Engineering 2005

PROFESSIONAL EXPERIENCE

SYSTEM LSI, SAMSUNG ELECTRONICS, Yong-in, Korea 2009-2014
Senior Engineer

Project: Multi-Output Highly Integrated Power Supply for LCD Backlight Application

- Developed an up to 30V Input Housekeeping Block with a 5V Internal Regulator
  5μA shutdown current; 1.2V±1.5% bandgap reference; up to 30V input to enable controller and Under-voltage lock-out (UVLO) circuit
- Analyzed and Solved the Wireless Areas Noise Problem for Laptop Application
  Found the root cause of the noise source, which was the LC resonant between bonding inductance and parasitic switch capacitance on the switching node in the boost converter and solved the noise problem by moving the resonant frequency.

Project: Multi-Output Highly Integrated Power Supply for Tablet Application

- Developed a Compact 6V Input, Wide Output, 1A Current-Mode Buck Converter
  90% peak efficiency; programmable switching slew-rate controlled gate driver for EMI/WWAN suppression
- Designed a Compact Housekeeping Block for Reducing Area
  One bandgap reference for internal voltage regulator and input UVLO

Project: Advanced PMIC Solution for Mobile Application Processors

- Developed a 5V Input, Variable Output, 1/2/3A Synchronous Buck Converters for Mobile Application Processors
  90% peak efficiency; peak current mode control with pulse skipping mode at light load; fast line and load transient; 3MHz operation frequency; DVS for application processor companion (25mV/1μs); 20μA quiescent current at no load condition

Project: Compact Hysteretic Buck Converter for Mobile Application Processors

- Developed a 5V Input, Variable Output, Synchronous Buck Converters for Mobile Application Processors

  Integrated RC matching filter for inductor current sensing; peak and valley current sensing for over-current protection; fast load transient; DVS for application processor companion (25mV/1μs); 20μA quiescent current at no load condition

IC DESIGN GROUP, KOREA ELECTRONICS CORPORATION, Seoul, Korea 2007-2009
Design Engineer

Project: Control IC with Piezo Sensor for Toner Sensing Application

- Tested and Solved the Problems of the Control IC with Piezo Sensor and Collaborated with Rohm Co. in Japan

Project: Energy Effective Flyback Control IC for Universal Adaptor Application

- Developed A 0.2W Standby Power, 650V, 3A Flyback Control IC for 24W Adaptor Applications

  Universal Input; Integrated 650V Input Primary Biasing Circuit; Integrated 650V DMOS on SiP; 0.2W standby power consumption; 88% power efficiency; collaboration with KISTI, Korea

Project: DMOS Power Switch with Over-Protection Circuits for Pachinko Application

- Developed Integrated Over-Voltage and Current Protection Circuits with 90V DMOS

RESEARCH EXPERIENCE

INTEGRATED POWER SYSTEM LAB, UNIVERSITY OF TEXAS AT DALLAS 2014-2018
Research Assistant (Ph.D. Student)
Advisor: Professor Dongsheng Brian Ma, Ph.D.

A 25-MHz 4-Phase SAW Hysteretic DC-DC Converter with 1-Cycle APC Achieving 190ns t_{settle} to 4A Load Transient and Above 80% Efficiency in 96.7% of the Power Range

- Developed a 25MHz 4-phase buck converter with SAW hysteretic control and 1-cycle APC delivering 7.5W full power. In response to 4A load step-up/down, it retains 103 mV/123 mV VO droop with 1% t_{settle} of 190 ns/237 ns in 0.35μm CMOS. It achieves >80% efficiency over 96.7% power range with a peak value of 88.1%. Simple structure helps to achieve a power density of 3.98W/mm^2.

A 6V, 40MHz All-N-Channel 3-Level DC-DC Converter with 0.5ns/0.75ns Dead Time, 6.7% Minimum Conversion Ratio and 85.5% Peak Efficiency

- Designed A 40MHz, all-N-channel 3-level DC-DC converter to provide as low as 0.4V supply voltage from direct 6V battery voltage. With an interception coupling control dead time controller and full-swing sub-ns level shifting techniques, 0.5ns/0.75ns constant dead-time is accomplished over 500mA full load range. Peak efficiency is 85.5% over 0.8W power range.

INTEGRATED ELECTRONICS LAB, HANYANG UNIVERSITY, Seoul, Korea 2005-2007
Advisor: Professor Oh-Kyong Kwon, Ph.D.

An Area Efficient 8-bit Current DAC for Current Programming AMOLED

- Designed an Area Efficient 8-bit current DAC by 4-bit binary weighted current DAC and 4-bit switched capacitor cyclic DAC. Achieving 25% more area efficiency than typical binary weighted current DAC.

PUBLICATION LIST

- B. Lee, M. K. Song, A. Maity, and D. B. Ma, "A 25MHz 4-Phase SAW hysteretic DC-DC converter with 1-cycle APC achieving 190ns t_{settle} to 4A load transient and above 80% efficiency in 96.7% of the power range," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2017, pp. 190-191.
- B. Lee, M. K. Song, and D. B. Ma, "On-chip inductor DCR self-calibration technique for high frequency integrated multiphase switching converters," in *IEEE Applied Power Electronics Conference & Exposition*, Tampa, FL, Mar. 2017, pp. 2449-2452.
- B. Lee, M. K. Song, and D. B. Ma, "Implementing high-speed inductor current sensing for VHF on-chip voltage regulators," in *17th Annual TECHCON*, Sept. 2015.
- B. K. Lee, J. S. Kang, J. K. Lee, J. U. Han, and O. K. Kwon, "An area efficient 8-bit current DAC for current programming AMOLEDs," in *Int. Meeting on Information Display (IMID)*, Daegu, Korea, 2006.
- B. Lee "Dimming circuit, a light emitting diode driver including the same and a light emitting diode driver," US Patent. No 20120074860 A1
- W. Kim, H.-S. Youn, and B. LEE "Light emitting diode driving apparatus and method for driving the same," US Patent, No 20120280632 A1
- B. Lee, S. Kim, and H. Kim, "Switching mode power supply using frequency modulation type and pulse width modulation type," KR Grant, No 101039992 B1
- B. Lee, S. Kim, and H. Kim, "Switching mode power supply having function of soft start and overload protection," KR Grant, No 101067923 B1
- B. Lee, S. Kim, and H. Kim, "Switching mode power supply having primary bias power," KR Grant, No 101011083 B1

TEACHING EXPERIENCE

ELECTRICAL and COMPUTER ENGINEERING, HANYANG UNIVERSITY, Seoul, Korea 2006
Teaching Assistant
• Taught undergraduate courses in design of electronic circuits.

ELECTRICAL ENGINEERING, UNIVERSITY OF TEXAS AT DALLAS, Richardson, Texas 2015
Teaching Assistant