HIGH EFFICIENCY HIGH POWER DENSITY GAN BASED POWER SUPPLY UNIT (PSU) FOR DATA CENTER APPLICATION

by

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To the Almighty who is absolute possessor of all the five virtues: wealth, strength, fame, beauty and renunciation.

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THESIS

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The ever growing consumption of data and its handling has resulted in huge server stations which cover prime land space and consumes huge amounts of power at low voltages causing high inefficiency. This work attempts to evaluate the design of a GaN based high efficiency and high power density server PSU. A two-stage topology is considered where an active front end rectifier converts 208VAC 3-phase supply to 380VDC. An isolated DC-DC LLC converter employing a planar integrated matrix transformer steps down the 380VDC to 48VDC for further distribution in the server rack. The rectifier switches and the primary switches in the LLC are GaN MOSFETs. The analytical loss and volume model of the converter are derived and a multi-objective design optimization for reduction in loss and volume is performed. Hence, a suitable converter design parameter is selected and a prototype design is considered.

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CHAPTER 1

INTRODUCTION

1.1 Data Center Review

There has been a huge upsurge of internet data consumption in the last decade attributed to the increasing mobile internet usage. The internet traffic has tripled since 2015 and is expected to double by 2022. The power consumption figures of the data centers and server houses around the world in 2018 stands at 198 TWh or 1% of global consumption of power [1]. The data center energy consumption in US alone grew by 90% between 2000-05 followed by 24% increase between 2006-10 and 4% increase from 2010-14. This reduction in growth rate of energy consumption in spite of the surge in data consumption has been a result of enormous efficiency improvements made [2].

To maintain the current power consumption trend the data centers must continue to improve their energy efficiency against the continued increase in Data consumption. Power Usage Effectiveness (PUE) is a popular metric to compare the energy efficiency of data centers is defined as the ratio of the total energy consumed by a data center to the actual energy consumed by the telecom IT equipment. Thus, a higher PUE indicates a higher auxiliary energy required to drive cooling systems, lighting and other utilities and hence lower efficiency. A lower PUE on the other hand refers to a higher efficiency with 1.0 being the perfect. The average Power Usage Effectiveness (PUE) of data centers in 2018 is around 1.58 down from 1.65 in in 2013 and 2.5 in 2007, a decreasing trend which is commendable but still far from the best case performance of 1. However, there are several shortcomings to the PUE definition have emerged with one of them being proper classification or demarcation of IT equipment loads and the auxiliary loads [3]. Currently, the IT

loads capture the energy consumption of the IT loads and the losses caused due to the power delivery network as well. Hence, it can be shown that by replacing the low energy efficiency IT hardware with a higher energy efficiency IT hardware would cause an increase in PUE or apparent reduction in efficiency which is counter-intuitive to the general idea of energy efficiency. Thus, PUE computation should consider the exact figures of IT loads excluding Power electronics to make more sense in our studies. The other concern is the spatial efficiency of the data centers many of which cover well over a few million square feet, puts an additional financial burden. Thus, area occupied could also be used as a metric for comparison.

1.1.1 Data Center Power Supply Distribution and future Trends

Today's data center electrical distribution could be classified as AC or DC. In an AC system [3] the inverter converts the bus voltage to 208V AC to be distributed at the building level to be converted to 12/48 V DC at each server rack. Recent introduction of 48 V DC based server designs used in Google servers has pushed the industry standard towards 48 V [3].

1.1.2 Motivation for the Thesis

The state of the art methodology [4] [5] for a switching power supply design uses a pareto-optimal approach to a given converter architecture. This study suggests a highly efficient and compact architecture of a 3-phase AC server rack level PSU using the pareto-optimal design optimization for a 10kW system. The recent developments in semiconductor has enabled a very fast switching operation without incurring high losses, thus GaN power MOSFETs are employed in this design. The DC-DC converter provides required galvanic isolation by employing a High frequency Matrix transformer (HFMT) to reduce the secondary copper losses due to the high current at the output.

The multi-objective optimization aims to minimize the losses and the volume to depict a Pareto-front to visualize the design trade-offs.

1.2 Introduction to the Two-Step conversion Topology

A two stage converter architecture is proposed for the three phase AC source connected PSU where the first stage is an Active front End (AFE) rectifier feeding an intermediate DC bus using a simple voltage source converter. The second stage is an isolated DC-DC converter (LLC) which transforms Intermediate DC Bus Voltage (IDCB) to Rack Level Bus Voltage (RLB) output. A high frequency integrated planar Matrix transformer provides the necessary isolation and down conversion in this process. A schematic with a 2x2:1:1 Matrix transformer is depicted in Fig. 1.

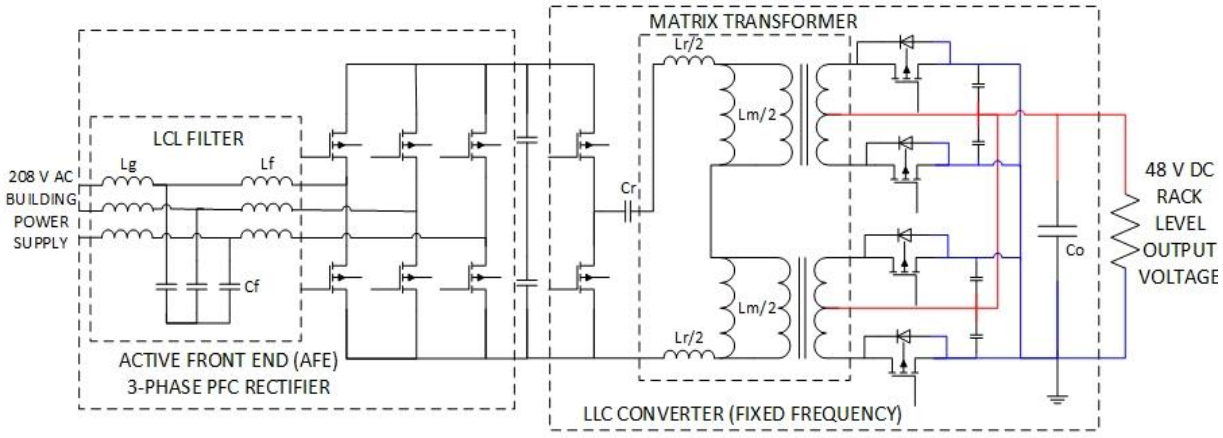

Figure 1: Two stage conversion architecture with 2x2:1:1 matrix transformer

1.3 Introduction to the Active Front End (AFE)

The AFE is realized using 650 V GaN MOSFETs from GaN systems (GS66516T). This highly modular architecture employs three Half Bridge Modules (HBM) corresponding to each phase leg connected in parallel to realize a complete three phase voltage source converter. Each HBM comprises of two GaN switches, and their corresponding isolated Gate driver power supply

(GDPS) and gate drivers in addition to a current feedback Hall effect sensor. The three-phase AFE is interfaced to 208 V AC voltage supply using LCL harmonic filter which ensures that the harmonic performance meets IEEE 1547. The rectified IDCB output is nominally 384 Volts. The LCL filter design is an essential step significantly affecting the overall power density of the circuit. The output DC voltage of AFE is actively controlled to achieve the desired RLB (48 V DC).

1.4 Introduction to LLC Converter

The isolated DC-DC LLC resonant converter forms the second stage and interconnects IDCB (384 V DC) bus with the RLB (48 V DC). The LLC resonant converter is employed because of its ability to achieve both high efficiency and high switching frequency operation due to Zero Voltage Switching (ZVS) resonance operation. The same GaN based HBM has been employed to realize the half bridge side of the LLC to reduce the number of primary turns in the HFMT by half. On the LV side Si MOSFETs are used as Synchronous rectifier which will also exhibit ZVS. An external capacitor is used to realize the resonant tank capacitor element. The efficiency of the resonant converter is compromised when operated at frequencies other than resonant frequency to enable operation over a large input voltage range [6]. Therefore by operating LLC converter at resonance frequency i.e. fixed gain this issue can be resolved. Thus the IDCB is adjusted by controlling the AFE in spite of variation in the 3 phase input AC supply or increase in the load.

1.5 Introduction to Integrated Planar Matrix Transformer

Transformers in a LLC converter fulfil two objectives namely, voltage stepping and isolation. Magnetics are often the bulkiest part of a converter, and increasing switching frequency is a preferred method to reduce the size of the magnetics by reducing the inductance requirement.

However at high frequencies, the transformer losses (copper and core losses) become a significant portion of the total losses in the system. Therefore high frequency magnetics design and optimization is required to achieve high efficiency and compactness simultaneously.

The conventional core transformers (Fig. 2) have been a mainstay for a long time, but planar transformers (Fig. 3) have received a lot of attractions to the recent applications requiring compact form factor. A planar transformer employs the PCB copper layers for primary and secondary windings, thus reduces both system size and weight. The magnetic cores in such power transformers is ferrite (MnZn) based in order to reduce core losses at high switching frequencies.

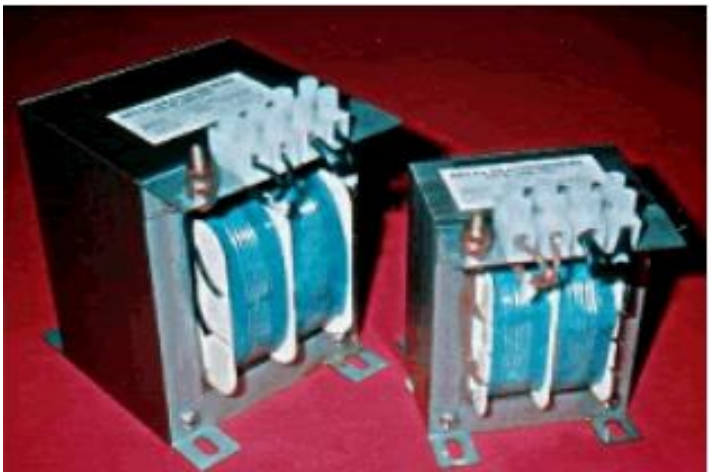

Figure 2: A conventionally wound transformer

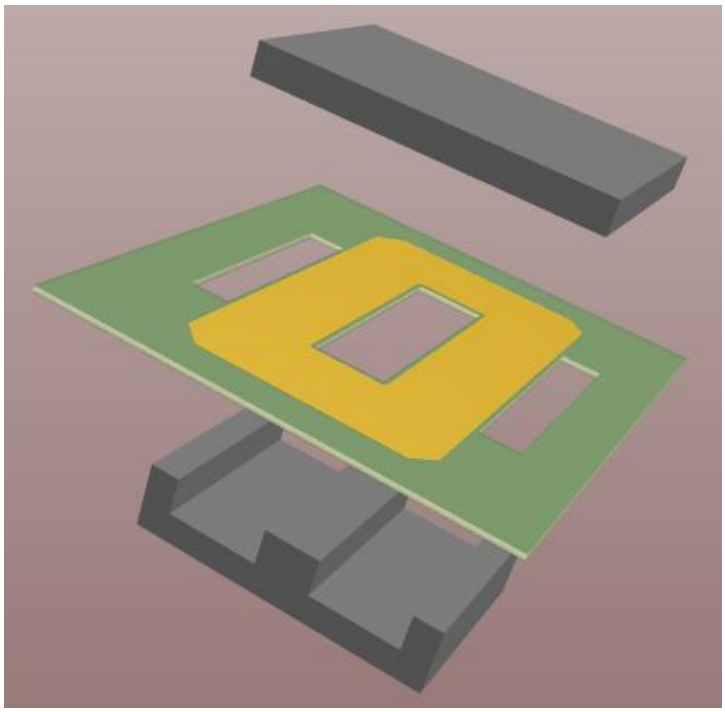

Figure 3: PCB based planar transformer with EE core

1.6 Organization of the Thesis

To optimize the design of the converter system, a multi-objective optimization is considered here. The converter has been optimized for low power loss and low volume, in order to achieve high efficiency and high power density. The following chapters discuss the in depth introduction to the subsystems and their modelling. The final chapter has a discussion on the overall design selection and the resulting efficiency and volume based on the simulation. A prototype based on the following design is being fabricated and the results would be published.

CHAPTER 2

THE ACTIVE FRONT END

The AFE (Fig. 4) is responsible for conversion of 208 V AC available at each server rack to be converted into 384 V DC for further down conversion by a fixed frequency LLC converter. Since the fixed frequency LLC converter provides fixed unity gain, the AFE is actively controlled to maintain the desired voltage at the output of the PSU. It is also responsible for maintaining unity power factor at all loading conditions and meet the power line harmonic performance as per as IEEE 1547 [7]. Below is the schematic of the AFE adopted for this study.

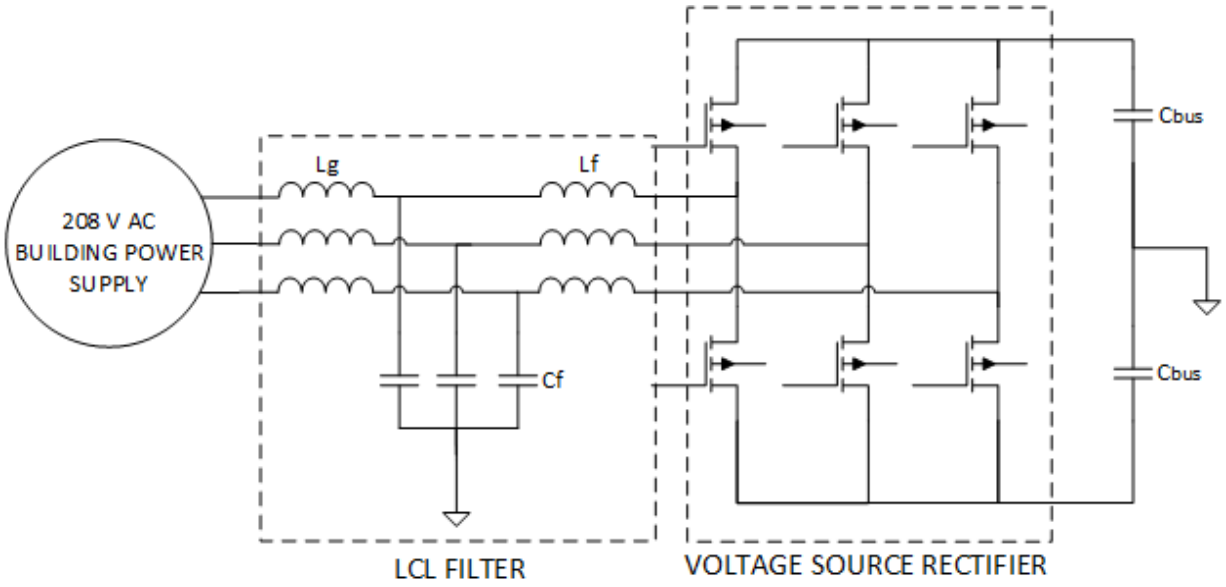

Figure 4: Active front end (3 phase PWM rectifier with LCL filter)

2.1 LCL Filter

The LCL filter has been designed to limit the THD to less than 3% of the fundamental current. Both the converter and grid side inductor model is realized using toroid powder iron cores with

copper windings. The copper loss and core loss have been considered in the loss model. The box volume of the filter components have also been accounted for.

2.2 Voltage Source rectifier

The three phase rectifier is realized using three modular half bridges comprising of two GaN switches. The converter is capable in providing bi-directional power flow both as a rectifier and as an inverter. It is as a hard switched rectifier and hence should be operated at lower frequencies to limit the switching losses. The modulation to be considered employed here is DPWM. Both conduction and switching losses for the considered in the loss model of the AFE. The volume of the rectifiers have been considered fixed since the additional volume occupied by more number of parallel switches is insignificant.

2.3 Half Bridge Realization

Below Fig. 5 shows the top side and the bottom side images of the designed half bridge. The Fig. 6 shows the complete assembly of a modular half bridge with the heat sink fan. Fig. shows three half bridges put together a voltage source rectifier. Sadly, the converter couldn’t be tested because of sudden coronavirus outbreak.

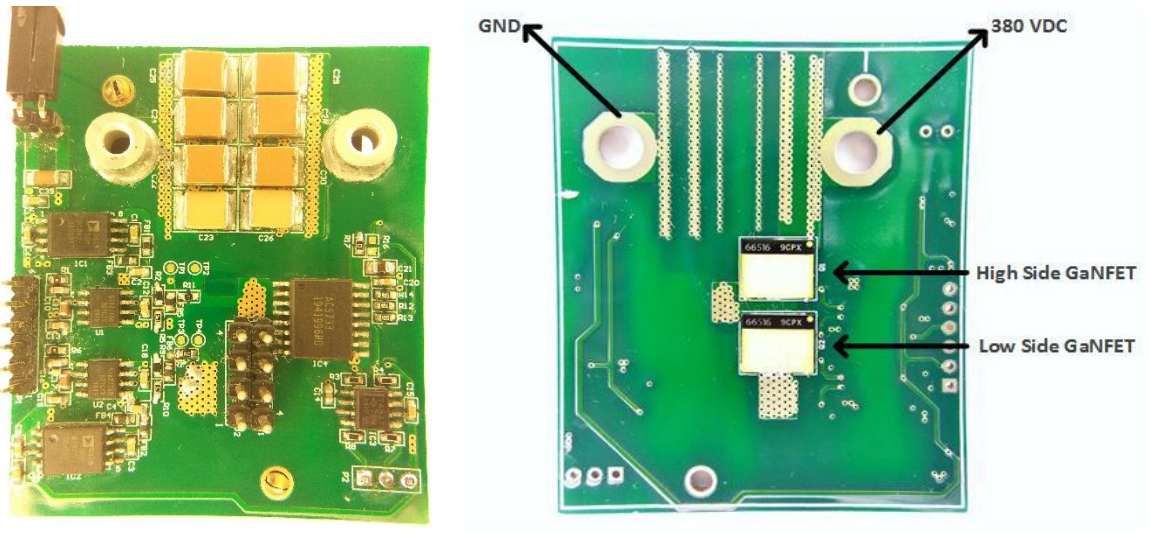

Figure 5: Top view and bottom view of the modular half bridge

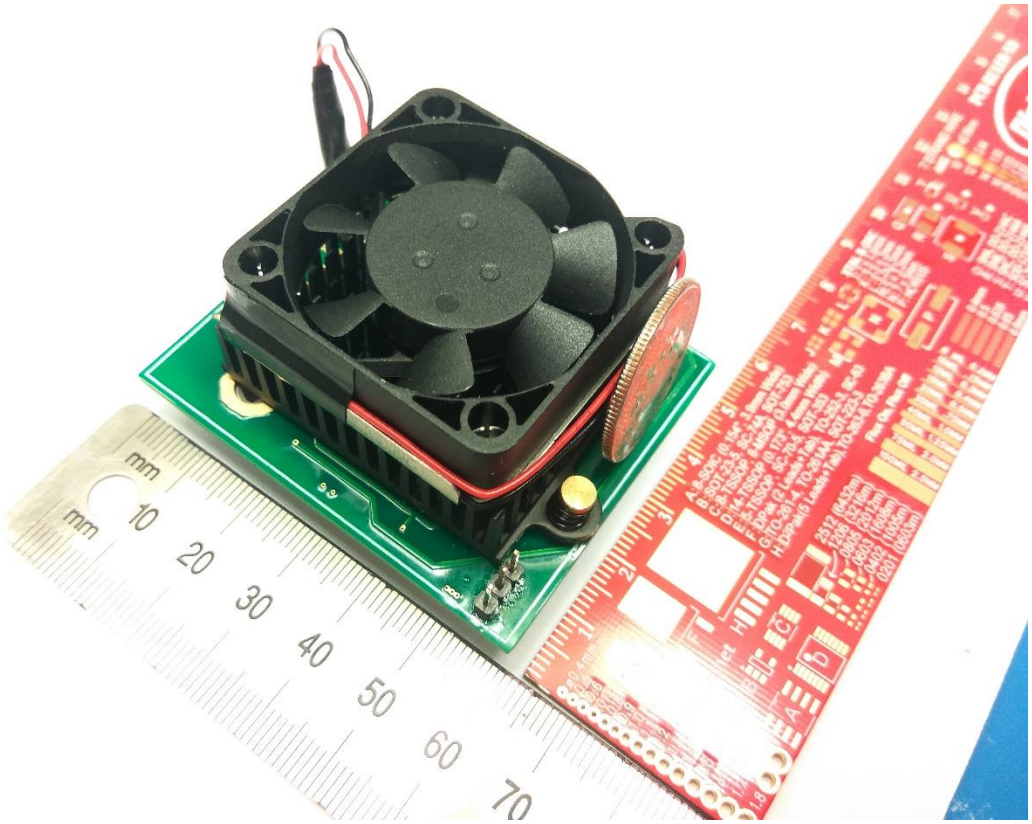

Figure 6: Complete assembly of the modular half bridge

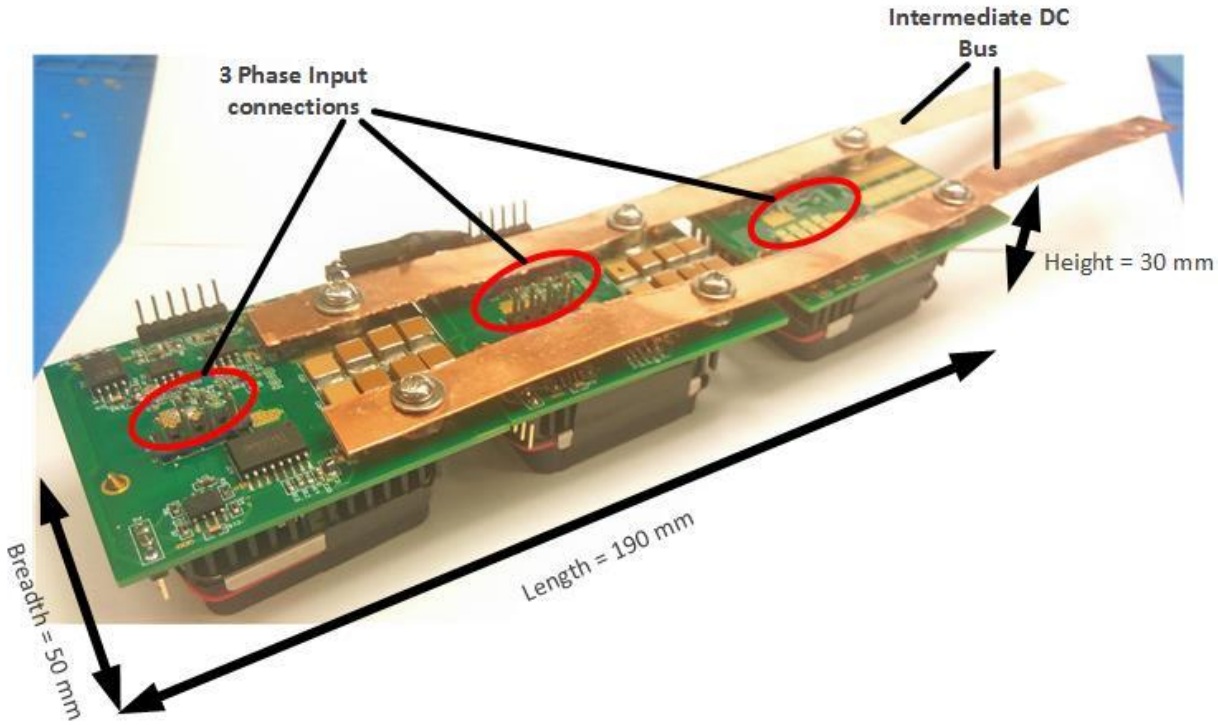

Figure 7: Voltage source rectifier assembly with three half bridges

CHAPTER 3

THE LLC CONVERTER

The LLC resonant converters have gained a lot of popularity [8] [9] among isolated high power density DC-DC converter topologies. The advantages are: (a) ZVS for full load range because of magnetizing current being only dependent on output voltage which is fixed; (b) low turn off current for primary side switches near resonant frequencies; (c) Synchronous rectification for secondary devices to achieve ZVS; (4) voltage-gain without significant efficiency degradation. Being a soft switched converter, high switching frequency allows high power density and efficiency than other hard switched PWM converters.

3.1 Working Principles of LLC Converter

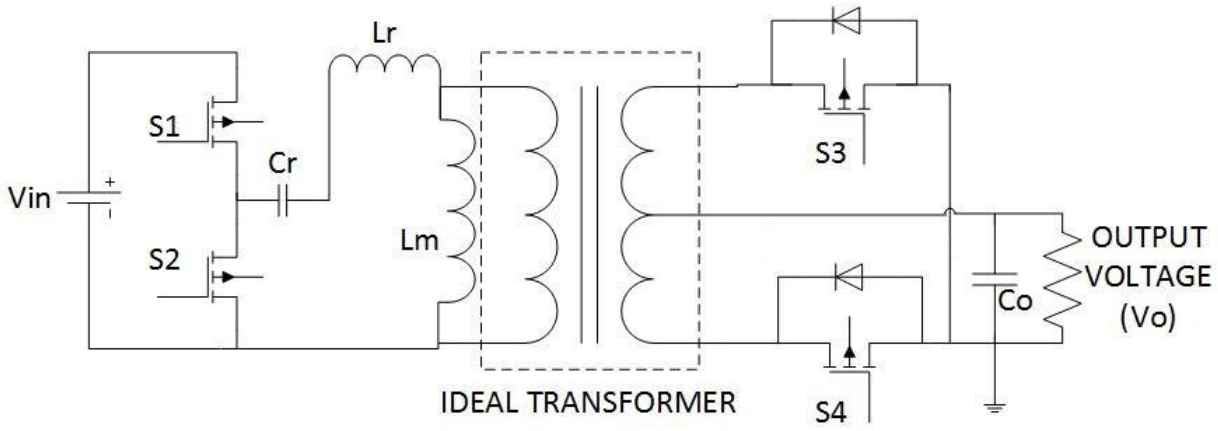

Figure 8: Half bridge LLC converter with secondary synchronous rectification

A typical LLC resonant half bridge converter with synchronous secondary rectification is shown in Fig. 8. However, a full bridge structure at the primary is also common. The converter structure can be expressed as two stages connected in cascade, separated by a transformer for isolation and

voltage step-up or step-down. The switches S1 and S2 are complimentary with a duty cycle of 0.5 and so are S3 and S4. The switch node connects a resonant tank which is hence connected in parallel to the transformer primary windings as in Fig. 8. The secondary side is a center-tapped transformer connected to synchronous rectifier. However, a full bridge structure can also be employed for secondary rectification as well. An output capacitor at the load maintains the output voltage ripple under desired the specification.

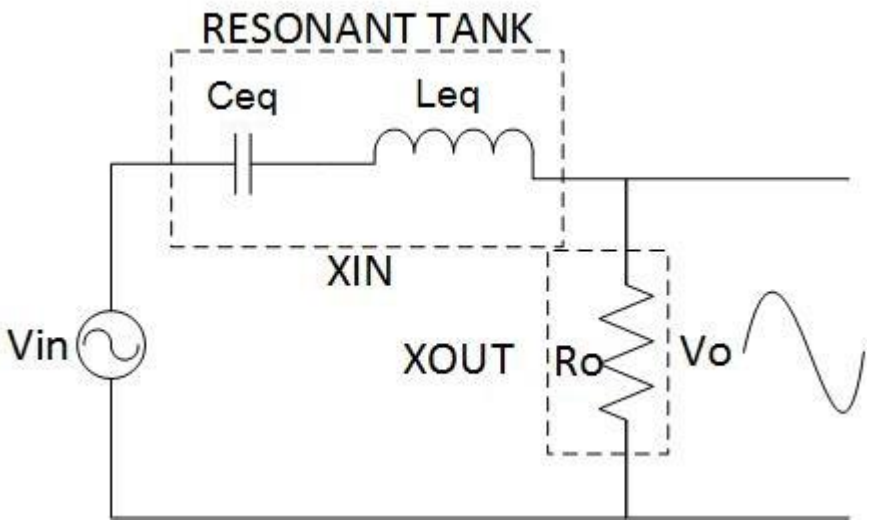

Figure 9: A simple resonant tank network

Since the resonant tank acts like a filter for the high frequency harmonics applied across it due to the square wave input, effectively only the fundamental harmonic component is involved in power transfer to the secondary side. Thus, LLC converter is typically analyzed considering first harmonic approximation (FHA) whereby only the sinusoidal fundamental harmonic component is considered in the analysis. The Thevenin equivalent of the LLC primary can be represented as a resonant tank (Fig. 9) and output load referred to the primary side can be seen as an AC voltage divider [10]. At resonant frequency input voltage appears across the primary side of the ideal

transformer and reflected at the secondary. At any other frequency other than this the voltage across the primary ideal transformer would be lower than that of the input voltage due to voltage drop across the resonant tank. Hence, by varying the switching frequency the impedance of the resonant tank varies which in turn controls the output voltage.

The converter can be operated slightly above or slightly below the resonance frequency enabling ZVS Turn ON and ZCS Turn OFF respectively but not both simultaneously. It is beneficial to operate at a frequency slightly above the resonance frequency because turn ON losses for most devices are much higher than the turn OFF losses. Also, operation slightly above the resonance frequency results in small turn OFF current and thus very small turn OFF losses. The turn OFF losses can be further minimized by optimizing the magnetizing inductance (L_m) such that the magnetizing current is just sufficient for ZVS turn on [11] because a higher magnetizing current causes higher conduction loss and turn off losses in the primary switches.

3.2 Analysis of LLC Converter

The two resonance frequencies "f_o" and "f_p" can be shown [9] [11] [12] to be,

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \quad f_p = \frac{1}{2\pi\sqrt{(L_r+L_m)C_r}} \tag{3.1}$$

Also,

$$k = \frac{L_m}{L_r} \quad Q = \frac{\pi^2}{8N^2 R_L}\sqrt{\frac{L_r}{C_r}} \qquad f_n = \frac{f_s}{f_r} \tag{3.2}$$

Where 'fs' is the operating switching frequency at any instant.

For the converter operation between $f_p < f_s < f_o$, a closed form equation of current is described as,

$$I_{p\_rms} = \sqrt{\frac{N^2(2T_s-T_r)T_r^2V_o^2}{32L_m^2T_s} + \frac{\pi^2T_s^2I_o^2}{8N^2T_r}} \qquad I_{s\_rms} = \sqrt{\frac{N^4(5\pi^2-48)T_r^3V_o^2}{96\pi^2L_m^2T_s} + \frac{\pi^2I_o^2T_s}{8T_r}} \tag{3.3}$$

Where 'N' is the turns ratio of the transformer, T_s is the inverse of f_s (switching frequency), T_r is the resonant period which is decided by L_r and C_r. Thus $T_s=T_r+2t_d$. Also I_o is the DC load current at a given loading condition.

The total conduction loss in the primary and secondary MOSFETs can be given by,

$$P_{Cond} = I_{p\_rms}^2\left(R_{p\_DSON}\right) + I_{s\_rms}^2\left(R_{s\_DSON}\right) \quad (3.4)$$

Where R_{p_DSON} and R_{s_DSON} refers to the primary and secondary on-resistance of the switches.

The switching losses can be ignored in a converter with low switching frequency and in ZVS operation. However, for a high switching frequency operation depending on the ZVS or ZCS operation the losses should be accounted for. In this design the switching losses are not considered since the converter although operating near MHz range, the ZVS ensures zero turn-ON losses in the primary, but finite turn OFF losses at low current. The secondary switches are synchronous rectifiers and a dedicated gate driver ensures ZVS and reverse recovery losses due to diode.

Since the ZVS is insured by selecting value of L_m which can discharge the energy stored in parasitic output capacitance of the MOSFET in the given dead time (t_d) such that the V_{DS} remains negative allowing ZVS turn ON.

$t_d > \frac{2V_{in}C_{OSS}}{I_{pk}}$. While $I_{pk} = \frac{nV_O}{L_m}\frac{T_r}{4}$. (3.5)

Thus,

$$t_d > \frac{8V_{in}C_{OSS}L_m}{nT_rV_O} \quad (3.6)$$

At critical dead time the relation between T_r and L_m is given by,

$$t_d = \frac{1}{4}\times\left\{T_s - \sqrt{T_s^2 - \frac{64V_{in}C_{OSS}L_m}{nV_O}}\right\} \text{ And } T_r = \frac{1}{2}\times\left\{T_s + \sqrt{T_s^2 - \frac{64V_{in}C_{OSS}L_m}{nV_O}}\right\} \quad (3.7)$$

The gain of the LLC converter is given as

$$M = \frac{1}{\sqrt{\left[1+\frac{1}{k}\left\{1-\left(\frac{1}{f_n}\right)^2\right\}\right]^2+\left[\left\{f_n-\frac{1}{f_n}\right\}Q\right]^2}} \tag{3.8}$$

The gain variations with Q and k parameters are depicted in Fig. 10 and Fig. 11. It is very important to remember that Q is a function of L_r, C_r and R_L among them the L_r and C_r are the design parameters which decide the resonant frequency and can't be changed in the hardware. However, the changing loading conditions causes variation in the gain. It is apparent that the gain drops at heavier loads, thus the converter is designed to support the required gain at maximum load. But, since in this study LLC is operated very close to resonant frequency, the gain is fixed at M=1 and hence not a function of loading.

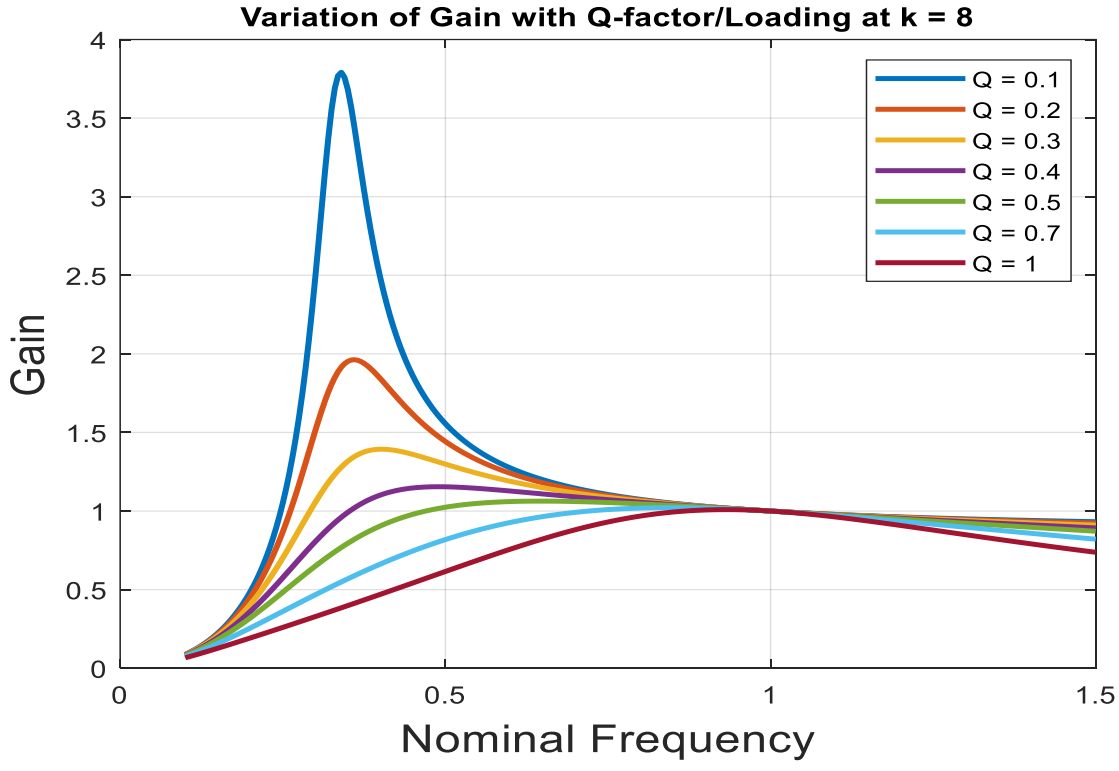

Figure 10: Gain variation with load (Q-factor)

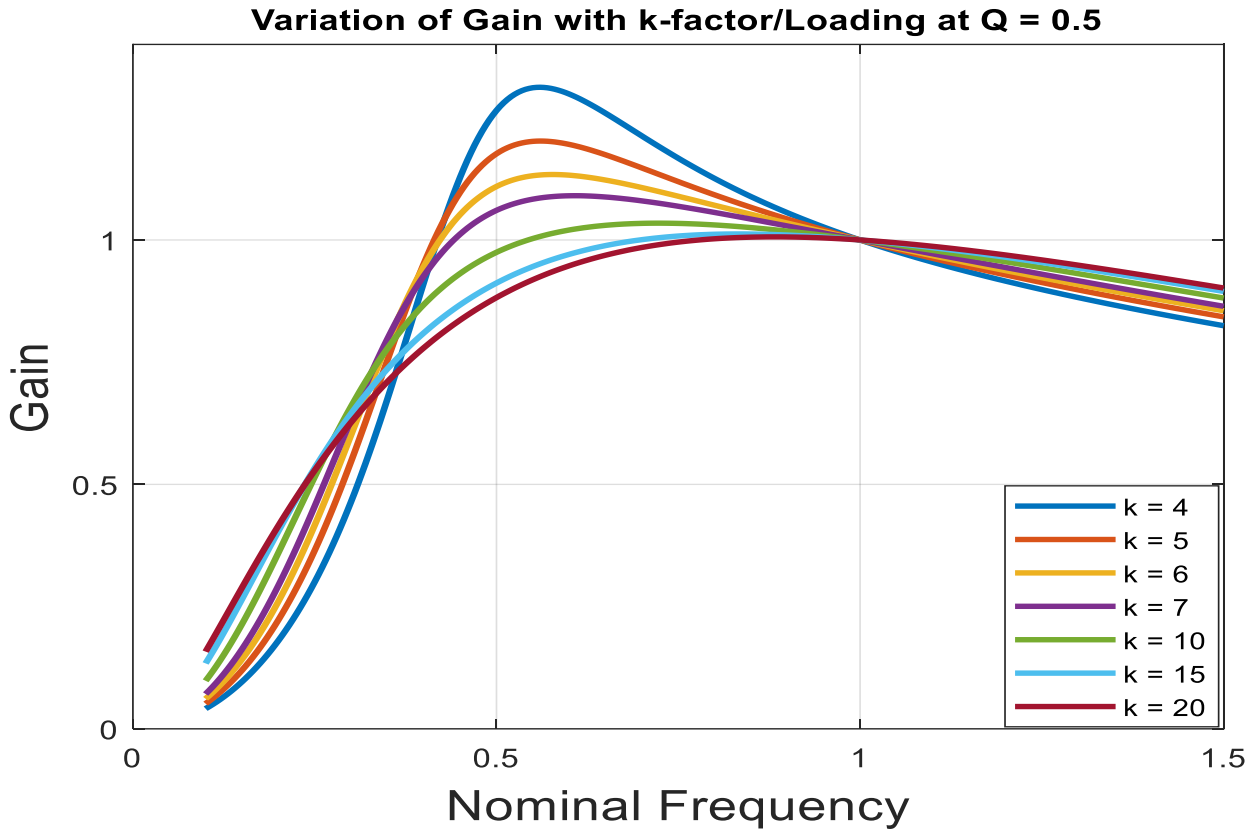

Figure 11: Gain variation with k

3.3 Selection and Characterization of Primary and Secondary Switches

The switches are selected such that the losses due to conduction and switching are minimum and the thermal resistance is low enough for good heat dissipation. The Top cooled devices are preferred for heat dissipation using forced cooling with top mounted heat sinks.

3.3.1 Primary Side GaN Switch

The selected device for the primary side is GS66516T. Table 1 depict some of the relevant nominal characteristics of the selected switch at specific operating conditions.

Table 1: GaN MOSFET (GS66516T) Specifications

Parameter	Value	Unit
V_{DS}	650	V
I_{DS} (T_{case} = 100 ºC)	47	A
R_{DSON} (25 ºC)	25	mOhm
C_{OSS} (V_{DS} = 400 V)	130	pF
C_{ISS}	520	pF
$R_{\theta JC}$ (Junction to Case Top-side)	0.3	ºC/W
E_{ON} (V_{DS} = 400V and I_{DS} = 20 A)	134.1	uJ
E_{OFF} (V_{DS} = 400V and I_{DS} = 20 A)	14.7	uJ

The Double-Pulse-Test for characterizing the switching loss variation with I_{DS} is obtained using the SPICE model of the device and the resulting energy loss was plotted in Fig. 12. Henceforth, a quadratic fit was employed to derive an empirical relationship between switching loss and current.

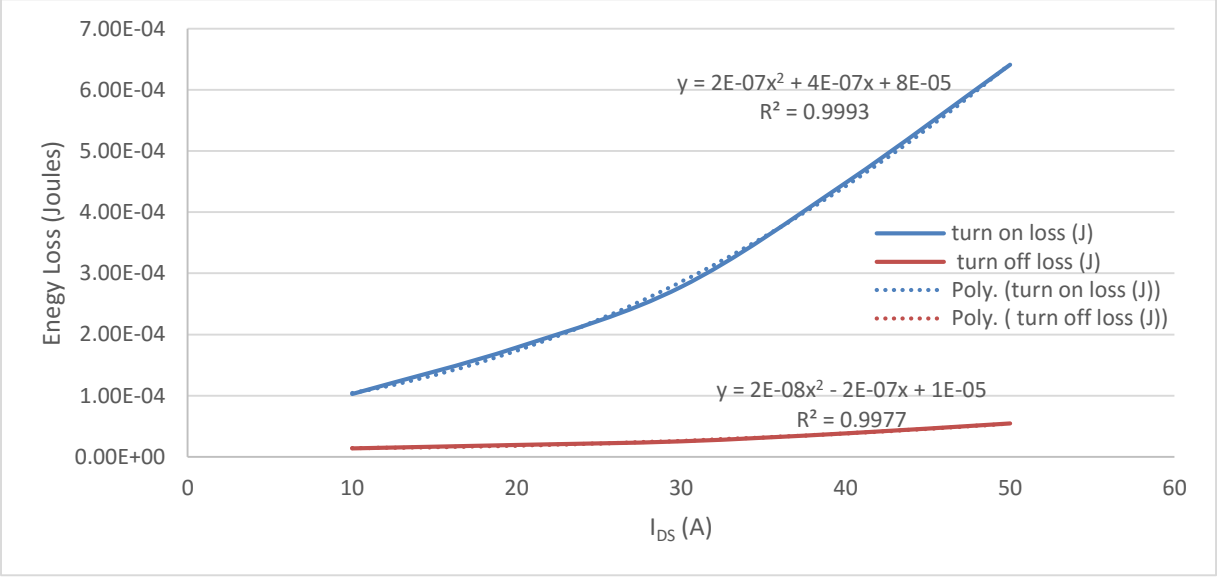

Figure 12: Switching Energy Loss (Joules) vs. I_{DS} (A)

Further, the R_{DSON} variation with the junction temperature was also captured from the datasheet for accurate conduction loss results. The plot is presented in Fig. 13.

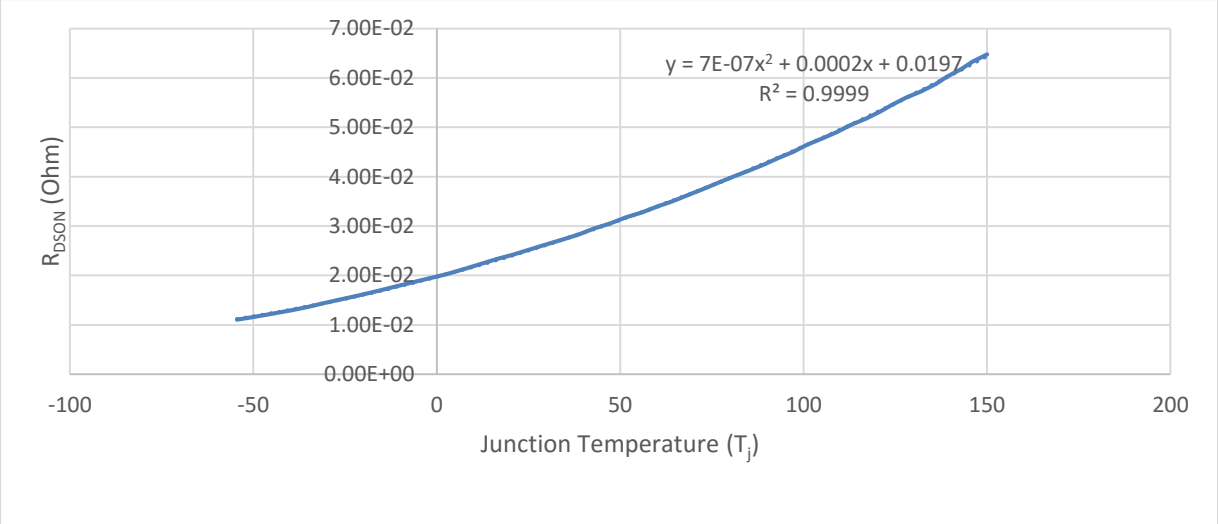

Figure 13: R_{DSON} vs. Junction Temperature (T_j)

The Gate resistance for Turn ON and Turn OFF are selected such that the losses are minimum. The following Fig. 14 and Fig. 15 show Turn ON and Turn OFF losses as a function of $R_{G\text{-}ON}$ and $R_{G\text{-}OFF}$. Thus, $R_{G\text{-}ON} = 0.5\Omega$ and $R_{G\text{-}OFF} = 2\Omega$ are selected for the design.

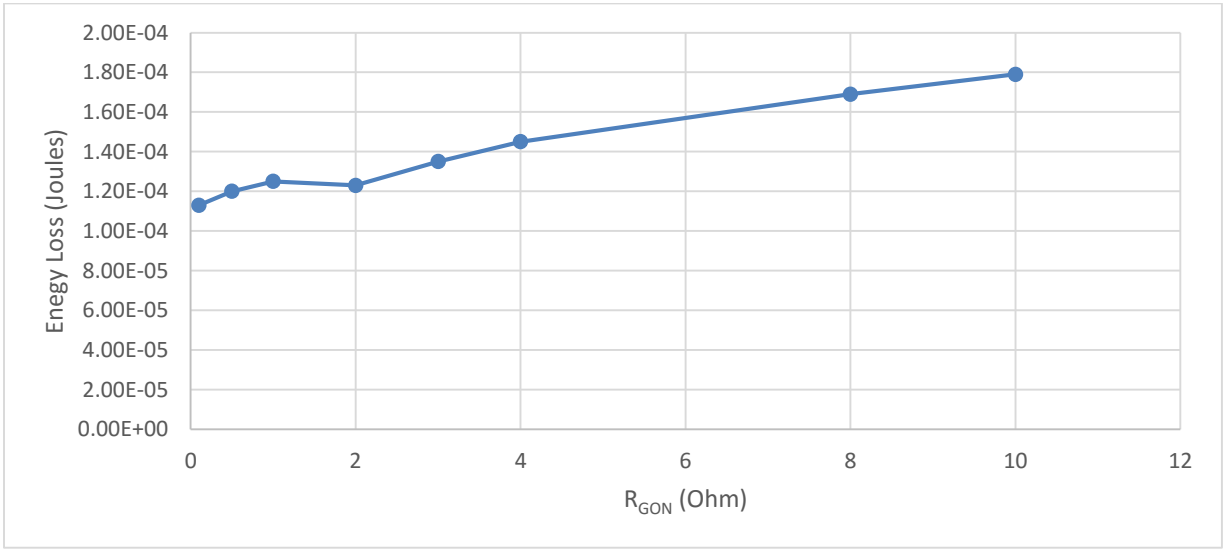

Figure 14: Turn on Loss (J) vs. R_{GON}

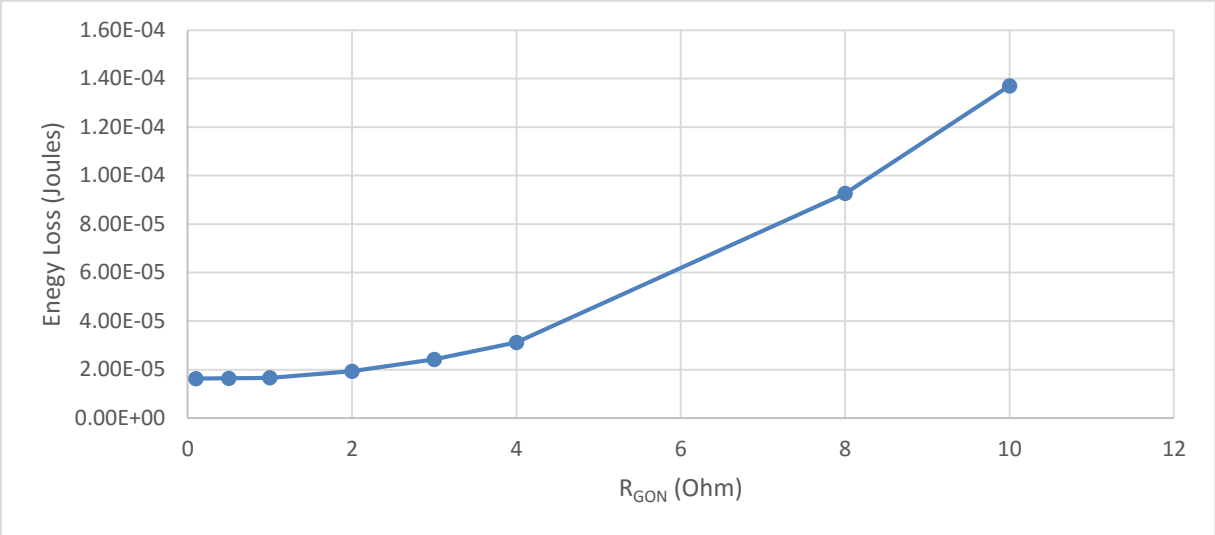

Figure 15: Turn off Loss (J) vs. R_{GOFF}

3.4 Secondary Side Si-based Synchronous Rectifiers

Both GaN and Silicon based devices were considered for the secondary side. However based on the high current requirement and the devices available in the market with low R_{DSON} and good thermal dissipation capabilities, Silicon MOSFETs were finally selected. The selected device for the secondary side are two parallel synchronous rectifiers, IRF7759L2TRPbF operated with a synchronous rectifier standalone controller NCP43080DMNTWG. Table 2 provides some of the relevant nominal characteristics of the switch at specific operating conditions.

Table 2: Synchronous rectifier MOSFET (IRF7759TRPbF) specifications

Parameter	Value	Unit
V_{DS}	75	V
I_{DS} (T_{case} = 100 ºC)	113	A
R_{DSON} (25 ºC)	1.8	mOhm
C_{OSS} (V_{DS} = 400 V)	1465	pF
C_{ISS}	12222	pF
$R_{\theta JC}$ (Junction to Case Top-side)	1.2	ºC/W

The R_{DSON} variation with the junction temperature for the secondary side switch was also captured from the datasheet for accurate conduction loss results. The plot is presented in Fig. 16.

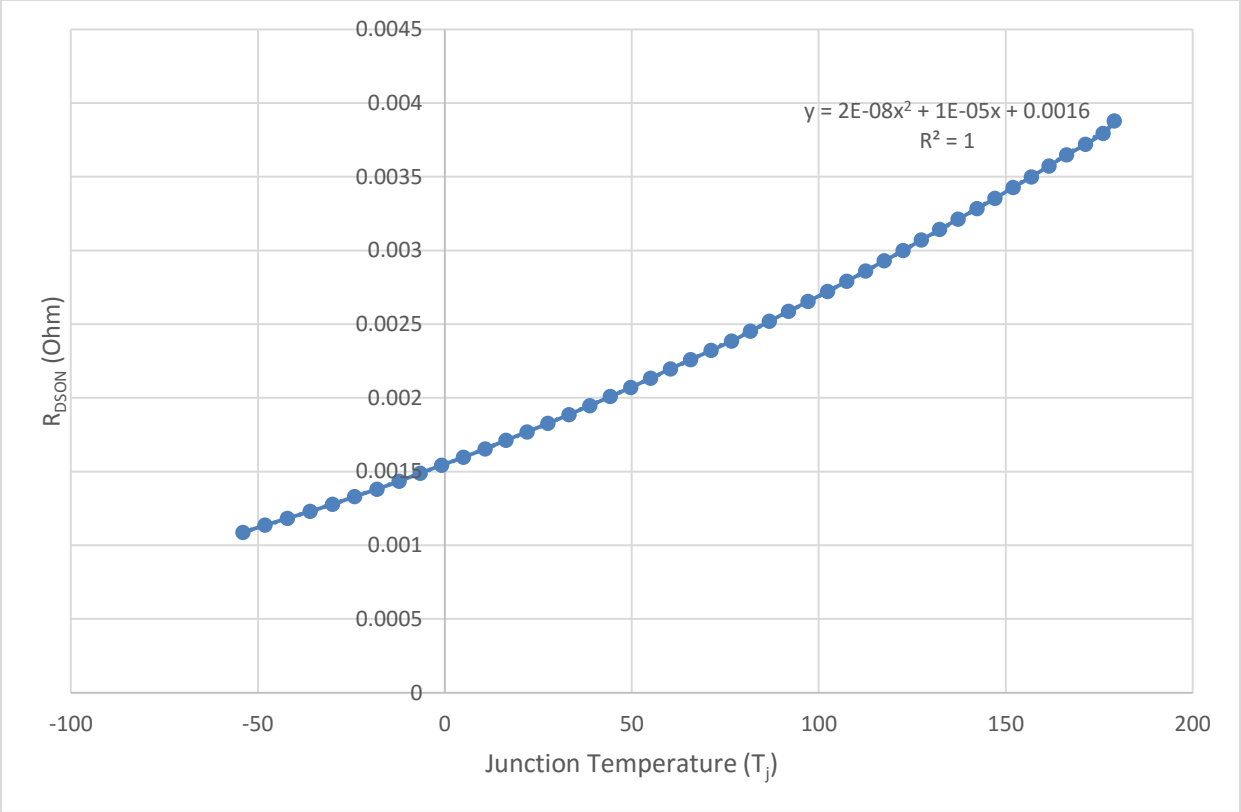

Figure 16: R_{DSON} vs. Junction Temperature (T_j)

CHAPTER 4

MODELLING THE MATRIX TRANSFORMER

The patent for Matrix transformer was issued to E. Herbert in 1985 [13]. However, this new approach to the transformer design has not drawn a lot of attention until now as the transformer design was not considered a significant attention in a power supply design previously. The matrix transformer achieves the desired turns ratio by employing series and parallel combinations of multiple transformers like in a matrix. The Fig. 17 below depicts the implementation of 4:1 ratio transformer using a conventionally wound transformer and a matrix transformer. Here, a matrix transformer aggregates four individual smaller cores of single turn primary and secondary into series and parallel connection of the primary and secondary turns to achieve this [14]. The inherent benefits of this approach: low leakage inductance ($L_{lk} \alpha N^2$) which in turn reduces the eddy current effects in the windings and low copper losses due to distribution of high currents into multiple parallel windings.

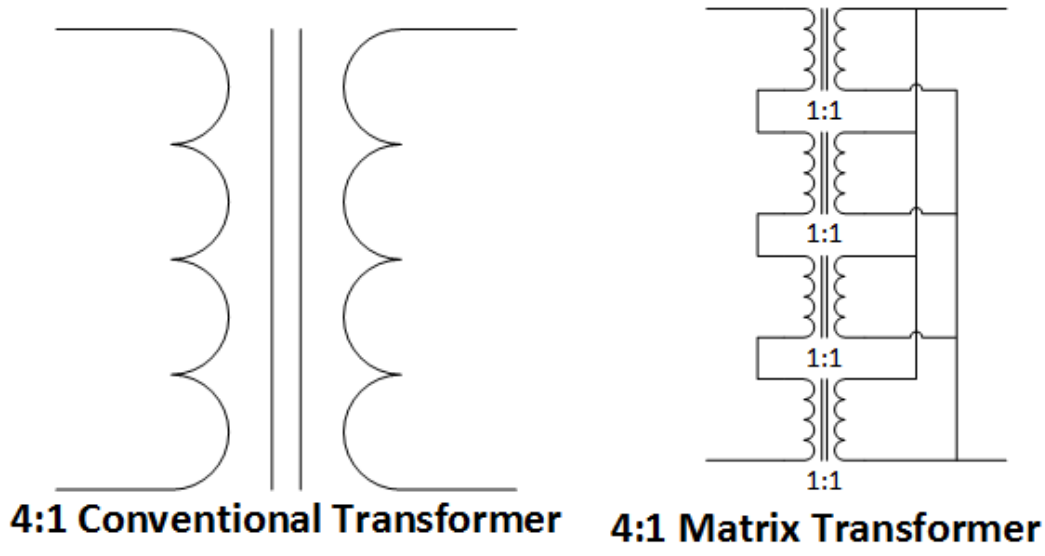

Figure 17: Conventional transformer turns and its matrix transformer equivalent

The Matrix transformer topology is a suitable candidate for the situation where high currents are involved as it would distribute the output current and reduce the secondary side AC resistance, henceforth reducing the transformer copper losses. However, generally there is an increase in the core volume because of usage of multiple cores. Thus this could cause higher core losses. Therefore, a transformer design is a challenging task since it involves selecting multiple parameters and an optimization technique is employed to arrive at a design that involves lower total losses. In this design an integrated planar magnetic design is considered and thus Lr and Lm of the converter is realized using leakage inductance and magnetizing inductance of the HFMT. Thus an external inductor would not be required in the design thereby reducing volume and losses due to an external inductor besides reduction in cost.

4.1 Advantages and Disadvantages of Planar Transformers

In a planar transformers unlike the conventional wound transformers the windings are realized using copper tracks on a Printed Circuit Board (PCB). There could be multiple turns on the same layer as well as on different layers. The principle differences in the geometry in comparison to conventional transformer is a flatter core and rectangular wire cross section instead of a circular.

4.1.1 Advantages of Planar Technology

Some of the advantages of planar transformer over a conventional transformer are [15]:

1. Reduced AC Resistance: A conventional transformer suffers a high AC resistance due to eddy current effects (skin effect and proximity effect) in the winding, causing much higher losses at high frequencies above 100 kHz. However due to its geometry the effect on planar transformer is much lower than a conventional transformer.

2. Tight Control over Leakage Inductance: The common preferred practice in a planar transformer design is dedicating each PCB layer to either primary or secondary winding. Thus varying the separation of these two layers with additional prepeg sheets is a very accurate method of obtaining the desired leakage inductance [14]. Thus, realizing an integrated magnetic structure with sufficiently high tolerance is possible.
3. Manufacturability and Repeatability: Because of mature and proven PCB technology the winding manufacturing is much simpler and accurate than winding a conventional type. Also typically used planar cores E and I cores could be easily be mounted on a PCB using a clip.
4. Light weight and small form factor: High surface area to volume ratio because of the geometry makes it a compact structure with a very high power density with improved heat conduction [15].

4.1.2 Disadvantages of Planar Technology [15]:

1. Higher component Footprint: The price of a flatter geometry is paid by sacrificing crucial PCB area to accommodate the transformer.
2. Unlike conventional power transformers for which many wide varieties of core geometries are available in the market, the same is not true to planar transformers. In fact most of the planar transformer cores available are E-I cores and geared towards low power applications in the range of 1-2 kW. And there are still a very few high frequency magnetic materials in the market for 1 MHz and above transformer designs.

4.2 Planar Transformer Design parameter Overview

Some of the key geometrical and material parameters useful in modelling a planar transformer are as depicted in the figure below and explained henceforth. An E-I core has been considered for explanation.

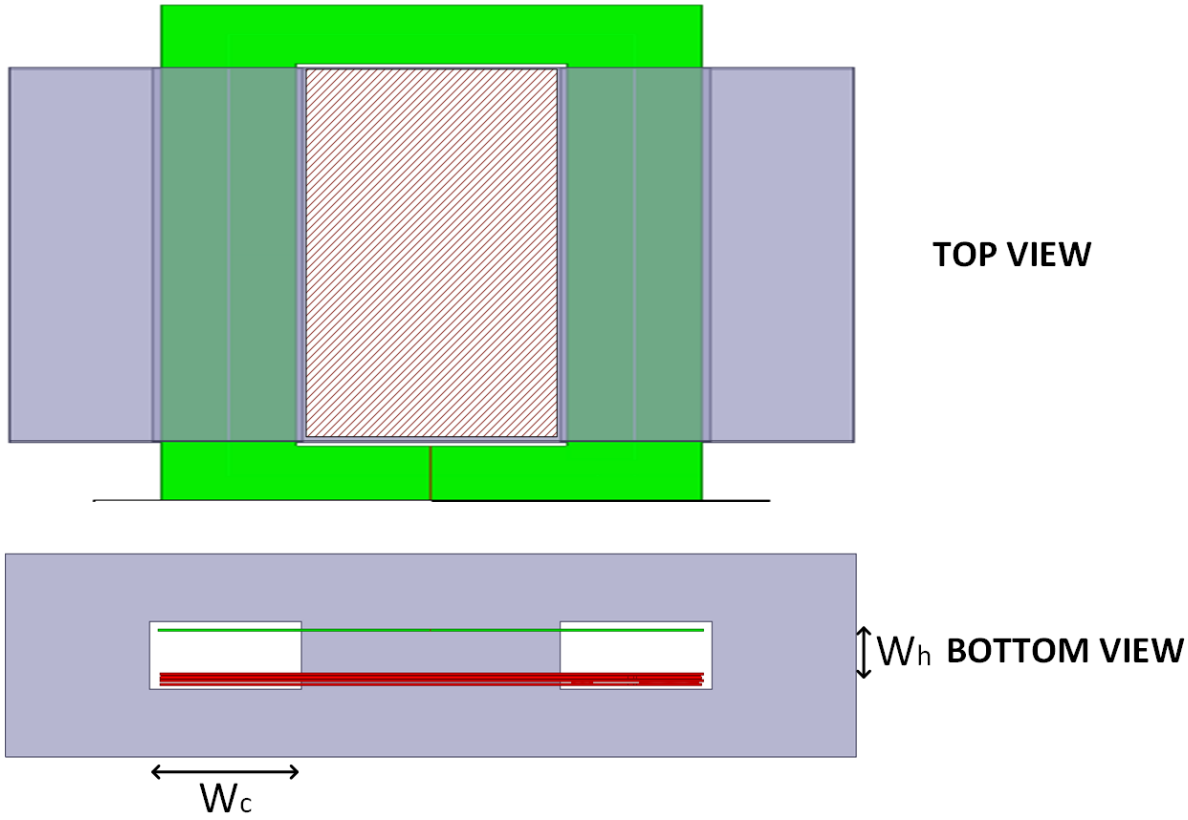

Figure 18: A EI core based planar transformer

1. Core Area (A_c): The shaded area in the Fig. 18 above is the cross sectional area of the central limb of the given core and used as a key parameter in determining the core size. The cross sectional area of the side limbs are approximately half of the area of the central limb. A large core area causes reduction in the magnetic field density and hence the power loss density. However the reduction in power loss density is also accompanied by increase

in core volume and increase in mean turn length of the winding. This could reduce overall core loss in general but it comes with an increase in winding losses.

2. Window width (W_c) : This is the available area for the winding and wider window widths allow wider winding resulting in lower winding resistnace and hence lower winding losses.
3. Window height (W_h) : The window height (Fig. 18) provides a constraint on the number of PCB layers and the seperation between them. Since the leakage inductance is directly proportional to the seperation of primary and secondary windings, a large height could be required to achieve a large leakage inductance. However, the downside to this would be larger volume requirement resulting in low power density of the convcerter.
4. Copper Thickness (t_c) : The thickness of the copper used is dependent on the copper ouncage of the PCB. Although increase in thickness might appear to be a perfect way to reduce the winding resistance and hence the winding losses, but high frequency eddy effects on a thick copper results in higher resistance and hence higher losses.
5. Mean Turn Length (L_T) : Length of each turn around a core is an important parameter affecting the winding resistance.
6. Air Gap Length (g) : Since the permeability of ferrite materials is a non-linear function of the magnetic field intensity (H), the saturation effects start appearing at high currents. Thus, air gap being a high reluctance segment causes the magnetizing inductance to reduce and also reduces the saturation effects. However, in LLC converter a tight regulation of magnetizing inductnace is required and a specific air gap length is maintained to achieve the desired magnetizing inductance.

7. Number of Turns (N_p and N_s) : Number of Primary and secondary turns need to be in a ratio for desired converter operation. However, the absolute number of turns in primary and secondary are crucial factors determining the total winding resistance and leakage inductance. The windings are depicted as copper strips with red and green color in Fig. 18.

4.3 Transformer Geometry

The required overall turns ratio decided for the matrix transformer is 4:1:1 and calculated as,

$$N = \frac{\left\{\frac{V_{in}}{2}\right\}}{V_{out}} = \frac{\left\{\frac{384}{2}\right\}}{48} = 4$$

The two preferred choice of matrix transformer configuration for this design is (a) 2 X (2:1:1) or (b) 4 X (1:1:1) where (a) involves two 2:1:1 transformer and (b) requires four (1:1:1) transformer. The preferred transformer geometry in consideration for (a) is shown in [16] while for (b) is shown in [17] discusses an optimum geometry. The subsequent discussion is based on approach used by the author in [17] and additionally a Pareto optimal approach is also undertaken. In [17] the central limb is circular instead of rectangular, thus reducing the mean turn length. The author in [17] has housed in a primary windings in the two middle layers of a 4-layer PCB. Subsequently the secondary windings are placed in the top and the bottom layer for so that the switches and the capacitor can be the part of the winding. This also results in shorter via-free high secondary current path reducing the secondary resistance and enhances heat dissipation capacity.

In our case due to much higher current, the primary windings could be implemented in a two layer PCB sandwiched between two secondary PCBs representing each secondary half windings.

4.4 Loss Models

The matrix transformer with four cores was selected as an optimum geometry for our application and requiring very low losses was designed in ANSYS as shown in Fig. 19 and Fig. 20. Each of the four sub-transformers comprises of one primary and two center tapped secondary turns.

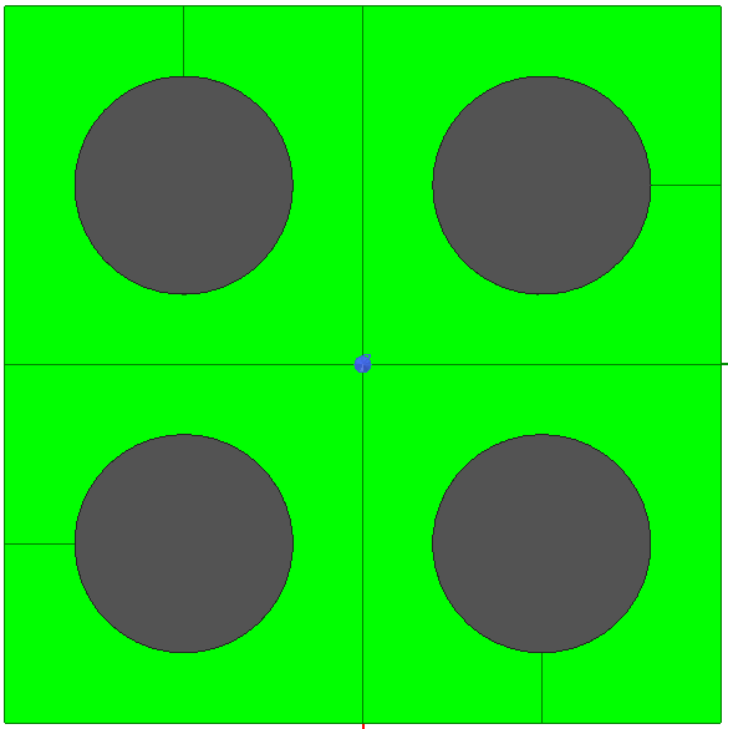

Figure 19: Top view ANSYS model of the four limb geometry

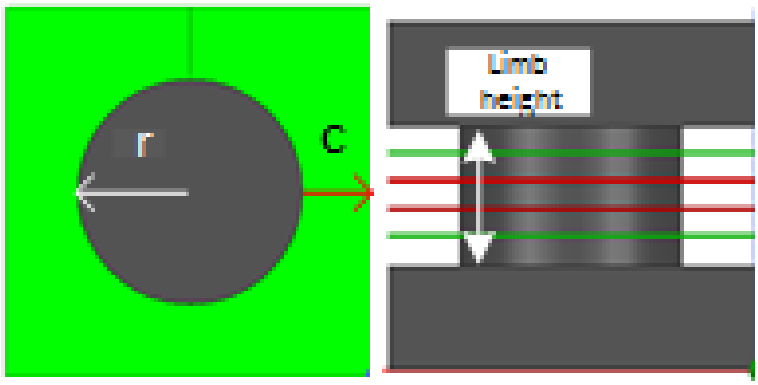

Figure 20: Top view and lateral view of a single limb

4.4.1 Copper Losses Model

The DC resistance of a single turn can be shown to be [17] [18]:

$$R_{Sec\_DC} = \frac{2\pi\rho}{t_c} \times \frac{1}{\ln(R) - \ln r} \tag{4.1}$$

$$R_{Pri\_DC} = \frac{2\pi\rho}{t_c} \times \frac{1}{\ln(R) - \ln r} \tag{4.2}$$

Where R = r + c and ρ is the resistivity of copper. The eddy current effects are very prominent at high frequency operation and thus AC resistance coefficient factor need to be accounted [18].

$$\eta = N_l \frac{a}{b} = N_l = 1$$

Where both 'a' and 'b' are equal to 'c' and 'N_l' is the number of turns per layer. Thus almost entire window width is fully utilized.

$$\alpha = \sqrt{\frac{j\omega\mu_0\eta}{\rho}} \tag{4.3}$$

$$M = \alpha t_c \coth(\alpha t_c) \qquad D = 2\alpha t_c \tanh(\alpha t_c/2) \tag{4.4}$$

$$F_{R\_Sec} = M'_{Sec} + \frac{(m^2_{Sec}-1)}{3} D'_{Sec} \tag{4.5}$$

$$F_{R\_Pri} = M'_{Pri} + \frac{(m^2_{Pri}-1)}{3} D'_{Pri} \tag{4.6}$$

Where 'm' is number of layers in a winding portion which is '1' in the present case.

$$R_{Sec\_AC} = R_{Sec\_DC} \times F_{R\_Sec} \tag{4.7}$$

$$R_{Pri\_AC} = R_{Pri\_DC} \times F_{R\_Pri} \tag{4.8}$$

Thus, the copper loss is given as,

$$P_{Cu} = I^2_{p\_rms}\left(R_{Pri\_AC}\right) + I^2_{s\_rms}\left(R_{Sec\_AC}\right) \tag{4.9}$$

4.4.2 Core Loss Model

The core loss density (P_v) for a given material for a sinusoidal excitation is given by an equation popularly known as Steinmetz equation as follows,

$$P_v = k f^{\alpha} B^{\beta} \tag{4.10}$$

Where 'k', 'α' and 'β' are the curve fit constants for a given core material for a given temperature and frequency range popularly known as Steinmetz parameters while 'f' and 'B' are the frequency and peak magnetic field strength of the sinusoidal excitation respectively.

Although this method predicts core losses very accurately for sinusoidal waveforms, the prediction is not accurate for non-sinusoidal waveforms typical for a switching converter. The Modified Steinmetz Equation (MSE) and Generalized Steinmetz Equation (GSE) were modifications on the original Steinmetz equation to improve the core loss density prediction due to non-sinusoidal waveforms using simple Steinmetz parameters. The Improved Generalized Steinmetz Equation (iGSE) [19] is improved upon the shortcomings of GSE and is able to predict core losses very close to the experimental values. This study employs iGSE for core loss model.

$$P_v = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\, dt \tag{4.11}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha} 2^{\beta-\alpha}\, d\theta} \tag{4.12}$$

Here 'ΔB' is the peak to peak flux density.

4.5 Inductance Modelling

Any given real transformer can be expressed as an ideal transformer and its parasitic elements as shown in Fig. 21. The 'R_c' is the resistance equivalent to the core loss while 'R_s' is the series

winding resistance. Since the copper loss and core loss models are already derived, they are ignored for inductance modelling. In a LLC resonant converter based on an integrated transformer, the leakage inductance (L_{lk}) and the magnetizing inductance (L_m) of the transformer is employed to provide equivalent 'L_r' and 'L_m'. The following sections discuss the methodology to achieve the discussed inductances by modifying transformer geometrical parameters.

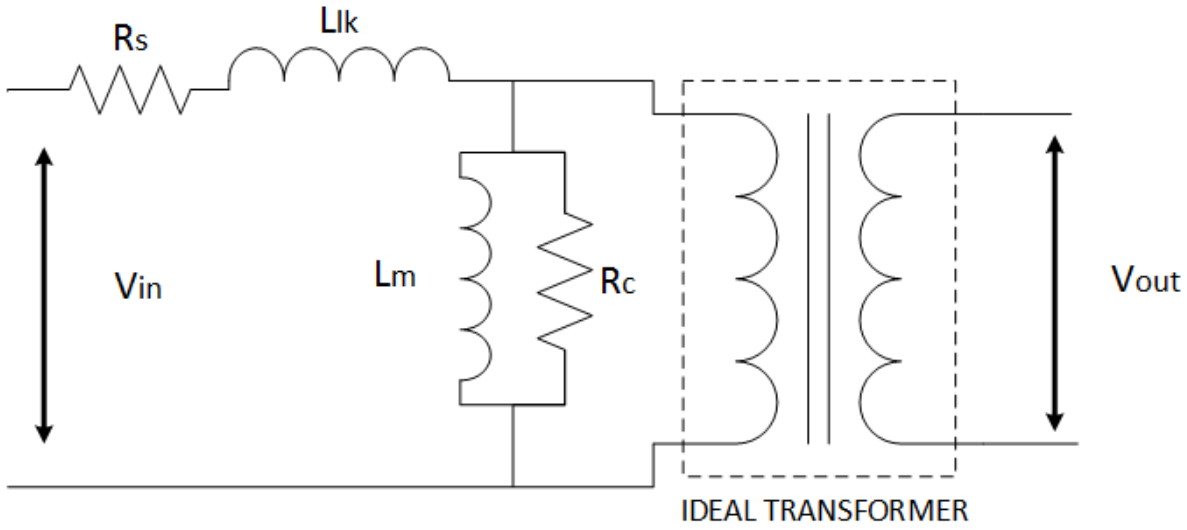

Figure 21: Simple transformer model

4.5.1 Modelling Leakage Inductance

The author in [18] derives frequency independent and frequency dependent components of leakage inductance in a conventional transformer. The frequency independent components are the result of leakage flux passing through interlayer and inter turn gaps of the transformer winding while the frequency dependent component of the leakage corresponds to the leakage flux passing through the copper windings. These fluxes gives rise to eddy currents and hence affects the current density in the winding layer and hence a function of frequency. However in a planar transformer due to the virtue of its geometry, most of the leakage fluxes pass through interlayer gaps instead of the

copper winding because the thickness of copper layer is negligible in comparison to the gaps and the overall window height. Thus, in our discussion the frequency dependency is ignored and only the energy stored in the interlayer gaps is used to calculate the leakage inductance [20]. The MMF distribution of a winding portion for a simple EI core transformer is shown in the Fig. 22 below. The leakage inductance for such a transformer used for LLC converter can be related with the geometrical parameters as,

$$L_{lk} = \mu_0 \frac{l_w}{c} N^2 \left\{ \frac{h_2}{4} + h_1 \right\} \tag{4.13}$$

Where the number of primary windings are 'N' and the secondary is single turn winding, thus a turns ratio is N:1:1.

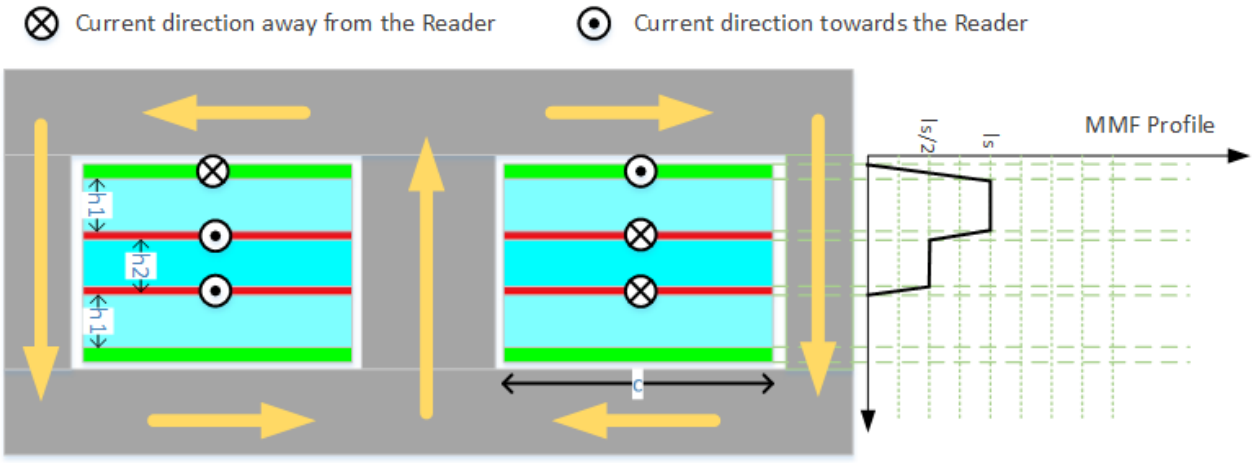

Figure 22: MMF distribution of an EI-core planar transformer

The Fig. 23 shows the MMF distribution of a winding portion of the four limbed geometry considered for the LLC converter in this study. Thus leakage inductance of each N: 1:1 unit sub-transformer of such a geometry can be shown to be,

$$L_{lk} = \mu_0 \frac{l_w}{c} N^2 \left\{ \frac{h_2}{4} + h_1 \right\} \tag{4.14}$$

The resultant leakage inductance of the combined transformer is four times the leakage inductance of a unit transformer since the primary are in series.

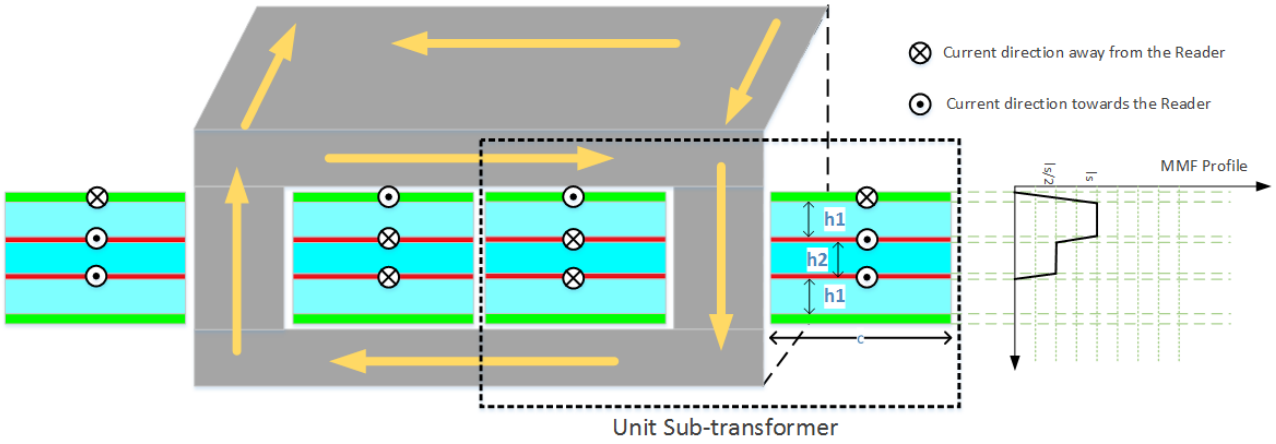

Figure 23: MMF distribution of the four limbed geometry

4.5.2 Modelling Magnetizing Inductance

From the transformer model in Fig. 21, it can also be seen that the magnetizing current depends on the output voltage and the magnetizing inductance. Magnetizing inductance is determined by the common flux path through the core which links both the primary and secondary windings. Any modification in the core flux path would cause variation in the magnetic field. The required magnetizing inductance is achieved by introducing air gap in the central limb of a transformer to adjust the reluctance of the magnetizing flux path. Fig. 24 describes position of the air gap in the E-I core structure. The red and green arrows depict the flux lines due to primary windings and the secondary windings respectively. And as visible the primary flux is stronger than the secondary flux and hence the magnetizing flux direction is determined by the direction of the primary flux. For an E-core geometry the magnetizing inductance referred to the primary windings are given by

$$L_m = \frac{N_p^2}{\left\{\frac{l_g}{\mu_0 A_c}+\frac{l_c}{\mu_0 \mu_r A_c}\right\}} = \frac{N_p^2 \mu_0 \mu_r A_c}{\{\mu_r l_g + l_c\}} = \frac{N_p^2}{\left\{\frac{\mu_r l_g}{l_c}+1\right\}} \times \frac{\mu_0 \mu_r A_c}{l_c} = \frac{N_p^2}{\left\{\frac{\mu_r l_g}{l_c}+1\right\}} A_L \quad (4.15)$$

Where 'N_p' is the number of primary turns, 'μ_r' is the relative permeability of the core material, 'l_c' and 'l_g' are the magnetic length of the core and air gap respectively. 'A_L' is the core parameter available in the core manufacturer datasheet. The above equation is derived from the reluctance model as shown in the magnetic circuit (Fig. 25).

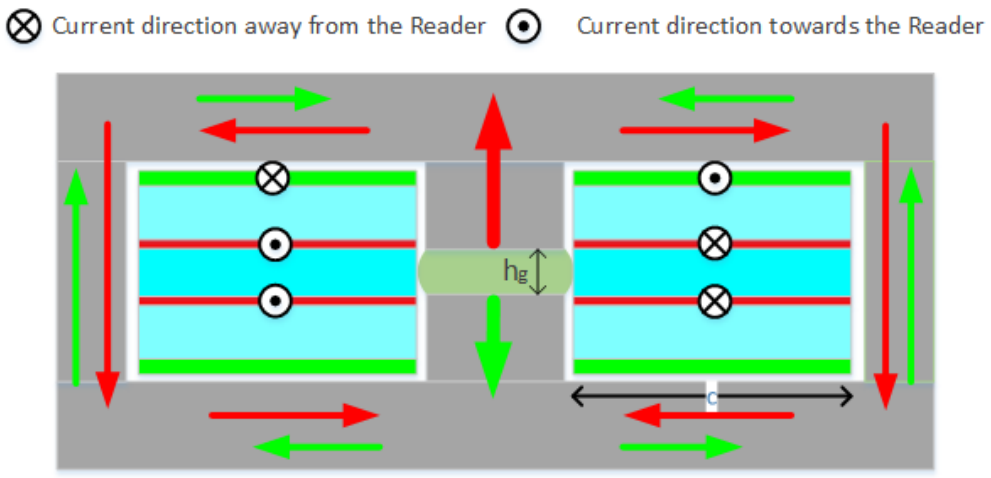

Figure 24: Magnetizing (main) flux path of an EI core transformer with air gap

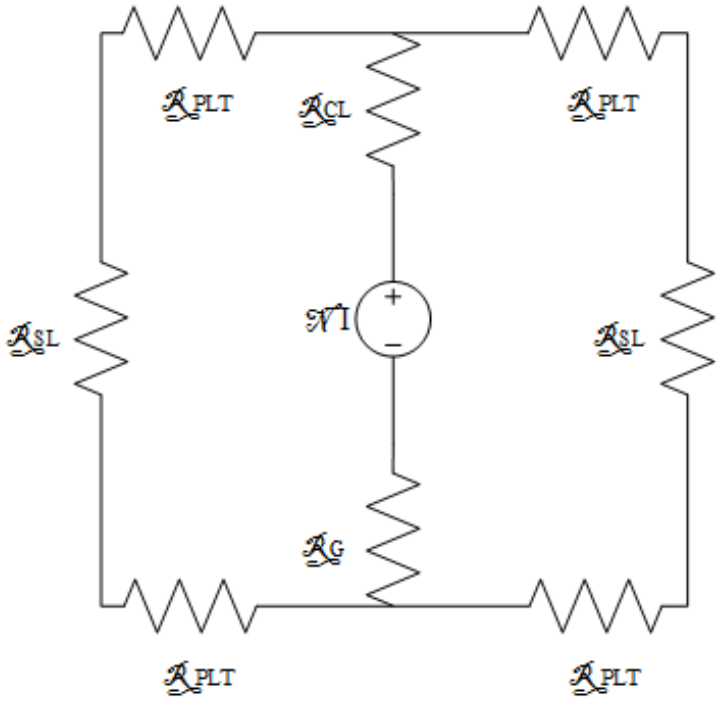

Figure 25: Magnetic circuit model for an EI-core transformer with air gap

The figrure below (Fig. 26) shows the magnetizing field in the considered matrix transformer. The magnetizing inductance of a unit-subtansformer referred to the primary can be given by the expression,

$$L_m = \frac{N_p^2}{\left\{R_L + R_G + \frac{R_{PLT}}{2}\right\}} \tag{4.16}$$

Where 'R_L', 'R_G', and 'R_{PLT}' stand for reluctance of the core limb, air gap and side plate as shown in the reluctance model (Fig. 27).

$$R_x = \frac{l}{\mu_0 \mu_r A_c} \tag{4.17}$$

Above is the reluctance model of each segment where 'l' and 'A_c' are the length and cross section area of the individual segments.

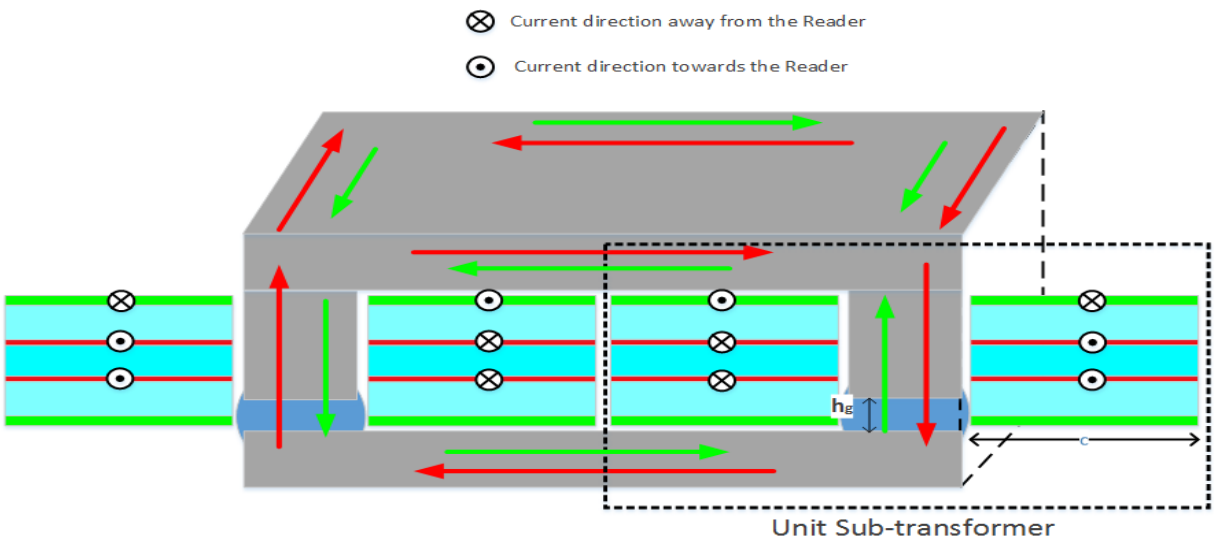

Figure 26: Magnetizing (main) flux path of four limbed transformer with air gap

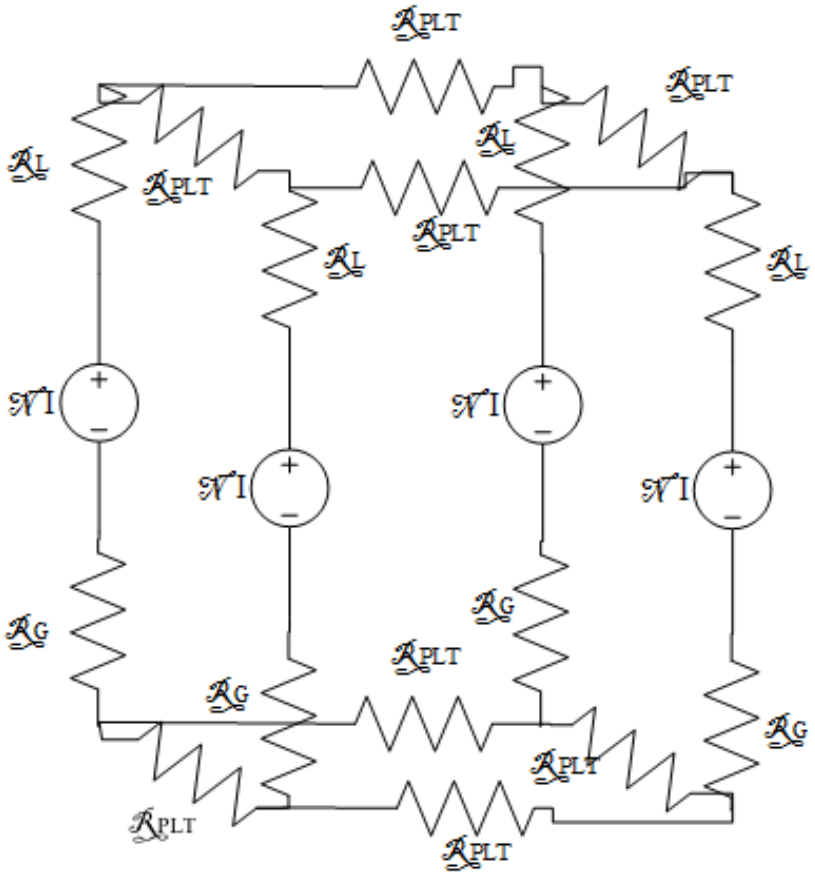

Figure 27: Magnetic circuit model of the four limbed transformer with air gap

CHAPTER 5

OPTIMIZATION RESULTS AND DISCUSSION

5.1 AFE Optimization results

The multi-optimization of the AFE was performed for reduction in energy loss for the following 24 hour load profile and reduction in volume was performed on MATLAB.

Table 3: Intra-day load profile

Power (W)	3000	5000	8000
Time (Hrs)	7	12	5

The Pareto front for the above multi-objective optimization was achieved and a suitable design was selected.

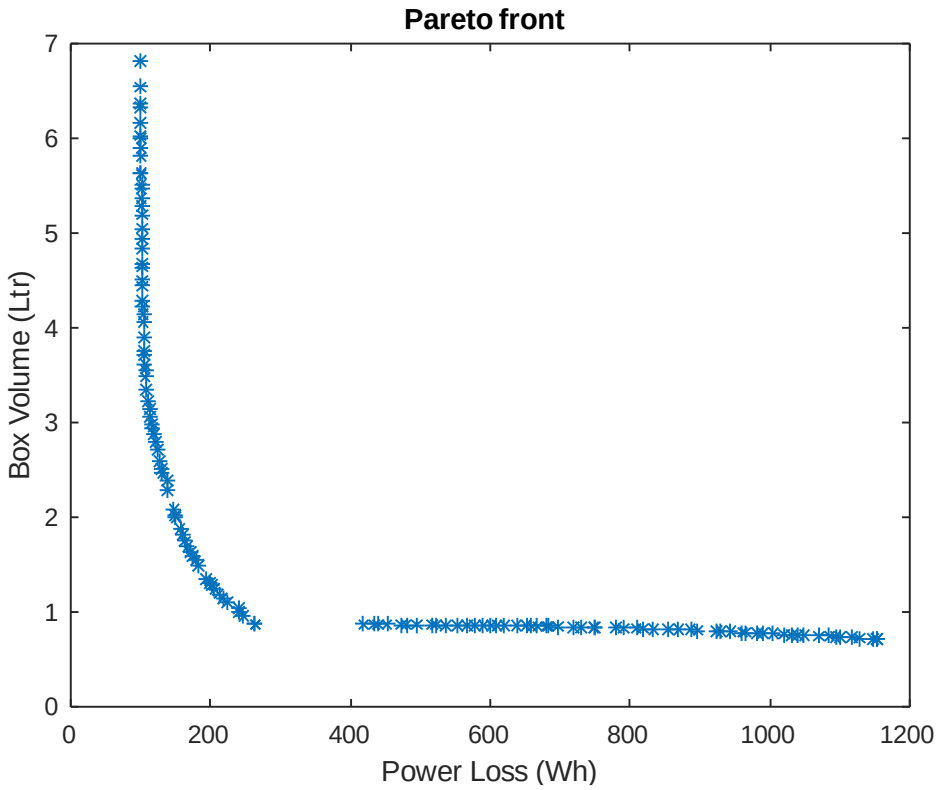

Figure 28: Pareto front for Energy Loss (Wh) vs. Box volume (Ltr)

5.2 LLC Optimization results

The optimization of LLC converter with matrix transformer was performed for reduction in power loss and reduction in volume with seven free variables for a 10kW converter.

$$minimize \quad [P_{Loss}, V_{Box}]$$

$$Free\ Variables\ (X) = \left[f_r, L_r, L_m, r, c, t_{pri}, t_{sec}\right]$$

Where $f_r, L_r, L_m, r, c, t_{pri}\ and\ t_{sec}$ are resonant frequency, resonant inductance, magnetizing inductance, radius of each limb, winding width, primary winding copper ounce and secondary winding copper ounce respectively.

The design were constrained by the following conditions:

- Semiconductor Junction Temperature < 135 ºC
- Magnetic Core Temperature < 125 ºC
- Primary and Secondary Winding Temperature < 115 ºC
- Magnetic Field Saturation < 250 mT
- ZVS Condition: Such that dead time (t_d) < 10% of T_s

5.2.1 Pareto Optimal Solution

The Pareto front for the multi-objective optimization was achieved and is indicated down below in Fig. 29. The marked design achieving 110.2W of power loss and 0.709 liter volume was selected for the converter design. The table 4 below depicts the values of the free variables considered for this design.

Table 4: Selected design parameters

f_r	L_r	L_m	r	c	t_{pri}	t_{sec}
846 kHz	34.8 nH	26.8 uH	10.43 mm	16.45 mm	4	4

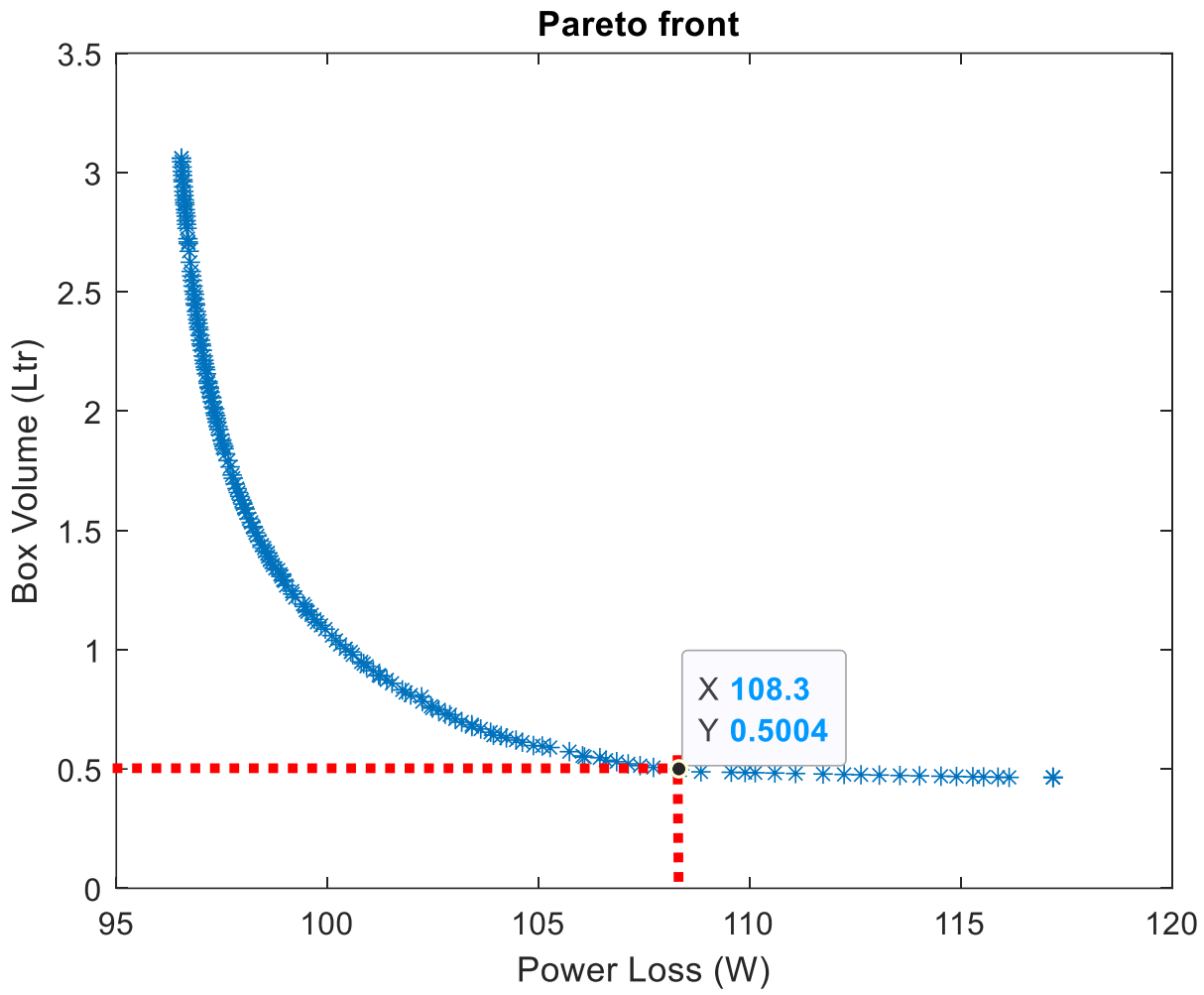

Figure 29: Pareto front for Power Loss (W) vs. Box volume (Ltr)

5.2.2 Loss Distribution

The Resonant capacitor selected was 1uF and dead time adjusted to 94 nanoseconds. The total power loss in the converter is 108.36 W and total volume is 0.5 Liter. This suggests peak efficiency of 98.9% and power density of 20 kW/liter (328 W/inch^3).

Table 5: Loss distribution at full load

Primary Semiconductor Loss (W)	Secondary Semiconductor Loss (W)	Primary Copper Loss (W)	Secondary Copper Loss (W)	Transformer Core Loss (W)
49.88	27.86	5.71	5.70	19.17

The loss distribution can be visualized with the following pie chart as shown below.

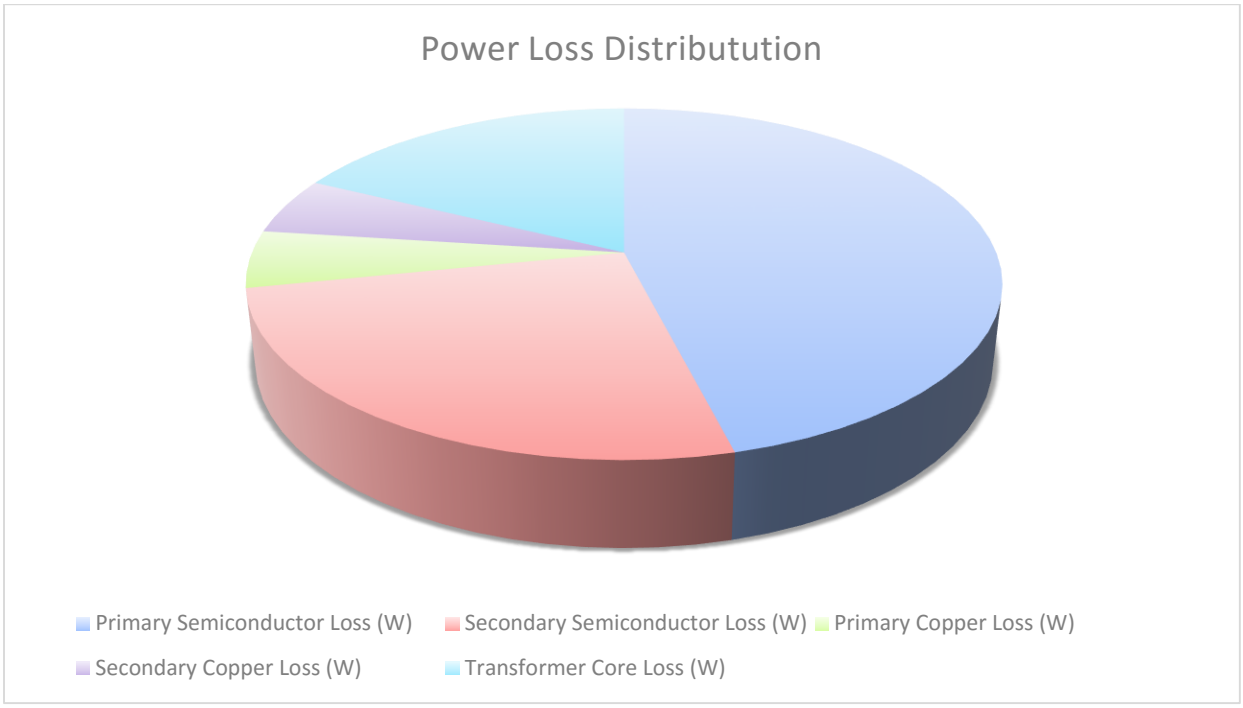

Figure 30: Loss distribution

5.2.3 Matrix transformer realization is ANSYS

Henceforth, the matrix transformer model (Fig. 31) was implemented in ANSYS MAXWELL and the leakage and magnetizing inductance was verified by short circuit test and open circuit test respectively using Eddy current simulation at 846 KHz.

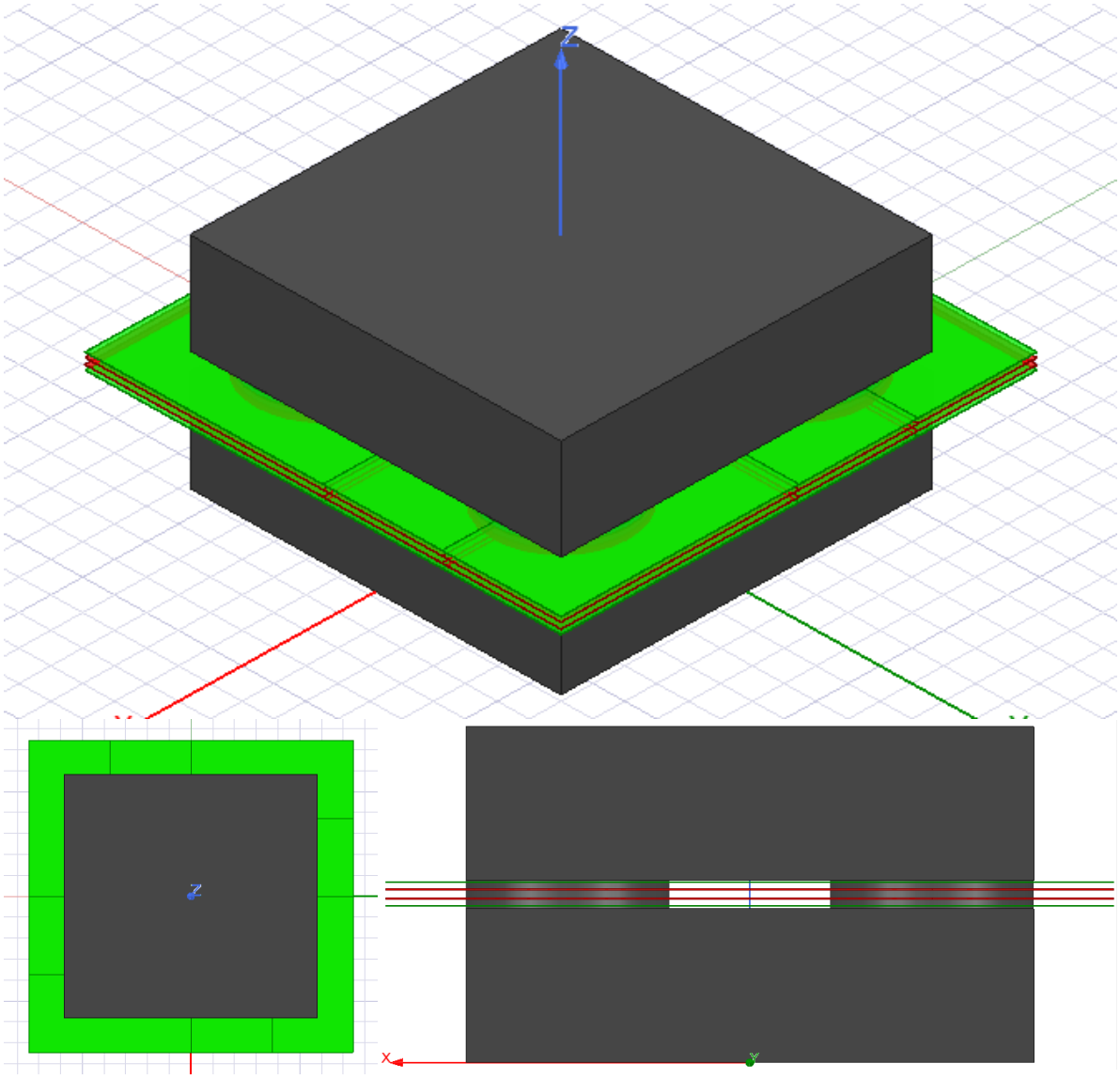

Figure 31: Matrix transformer (Isometric, Top and Side views) constructed in ANSYS

5.2.4 Leakage Inductance Verification

The leakage inductance as discussed above was measured after short circuiting all the bottom secondary windings mimicking either half of the windings conducting at a given time and with voltage excitation provided at the primary windings. The induced current was measured and the short circuit impedance was calculated. The leakage inductance was henceforth inferred from the imaginary component of the impedance. The supporting computation is shown in Table 6. The simulated leakage flux lines are also shown in Fig. 32-34.

Table 6: Leakage inductance computation

Applied Voltage (V)	Induced Current (mA)	Short Circuit Impedance (KΩ)	Leakage (H)
244	77411.6-1377700.12i	9.92E-06+0.000176549i	3.32163E-08

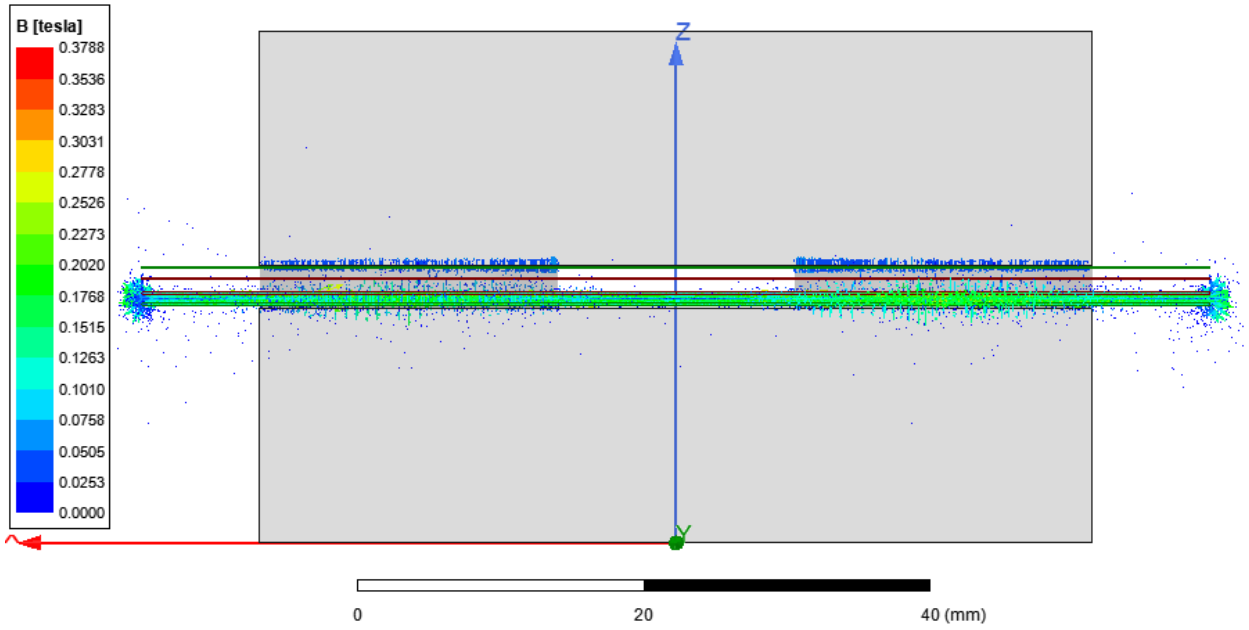

Figure 32: Leakage flux side view

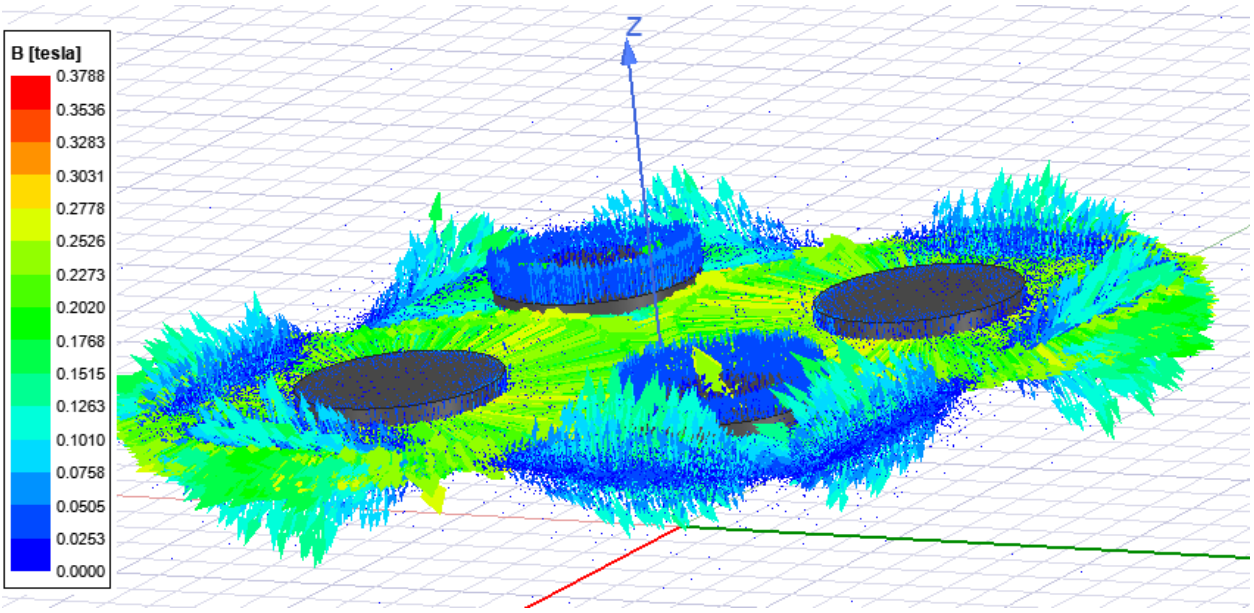

Figure 33: Leakage flux isometric view

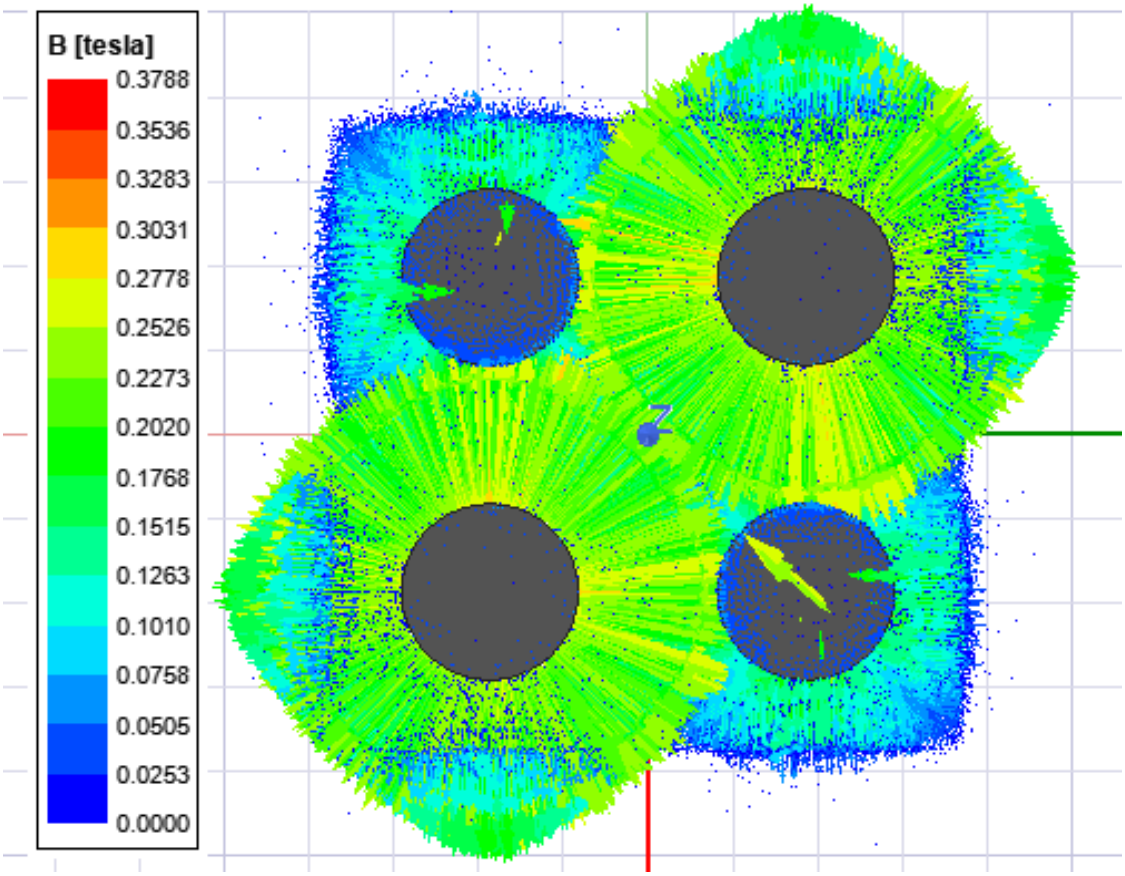

Figure 34: Leakage flux top view

5.2.5 Magnetizing Inductance Verification

The magnetizing inductance was measured after open circuiting all the secondary windings with voltage excitation provided at the primary windings. The induced current was measured and the open circuit impedance was calculated. The magnetizing inductance was henceforth inferred from the imaginary component of the impedance. The supporting computation is shown in Table 7. . The simulated magnetizing flux lines are also shown in Fig. 35-37.

Table 7: Magnetizing inductance computation

Applied Voltage (V)	Induced Current (mA)	Open Circuit Impedance (KΩ)	Leakage (H)
244	4.16122-1757.02i	3.2889E-04+0.13887i	2.613-05

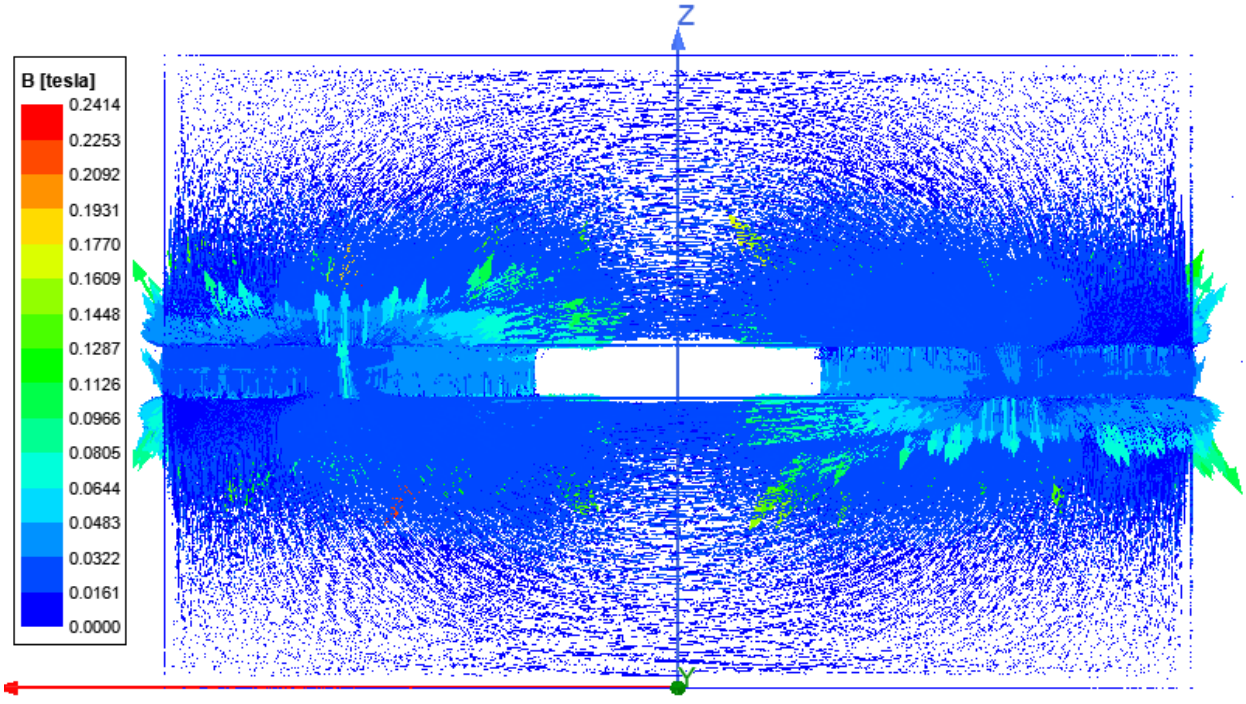

Figure 35: Magnetizing flux side view

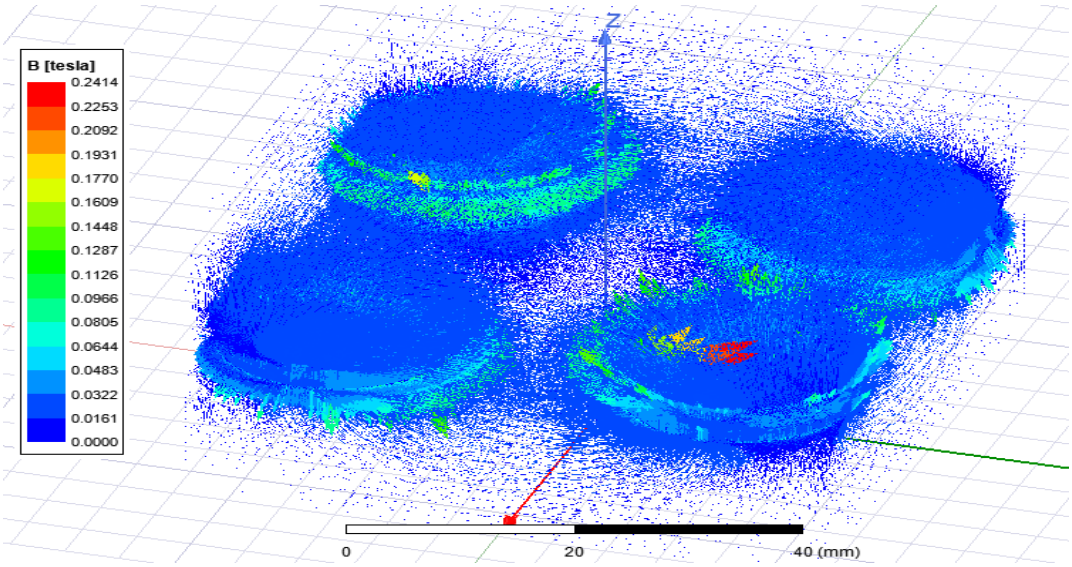

Figure 36: Magnetizing flux isometric view

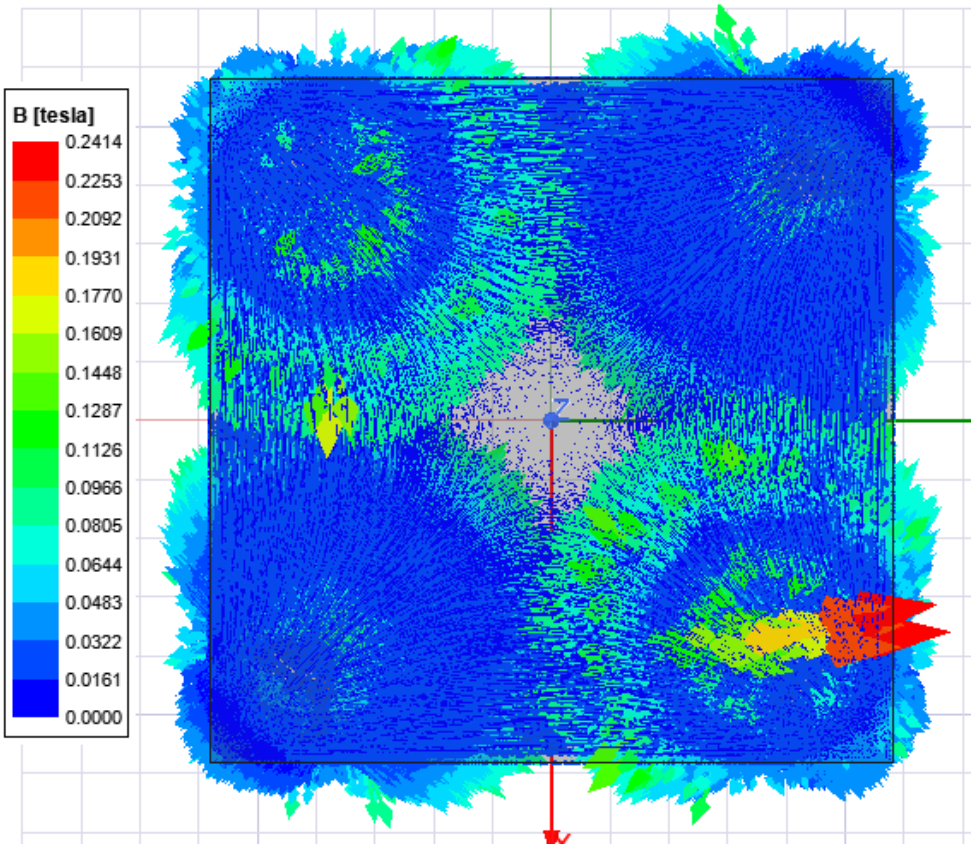

Figure 37: Magnetizing flux top view

CHAPTER 6

CONCLUSION AND FUTURE WORK

The optimization results of the LLC converter promises up to 98.9% efficiency but the box volume requirement for a 10kW prototype is in range of 0.5 liter which needs to be further reduced. Using thinner ferrite core plate for top and bottom to increase the magnetic field density at the cost of reduction in volume could be a possible way to address this issue. To further reduce the primary switch conduction loss, a parallel switch must be connected to reduce the effective R_{DSON}.

Because such unconventional transformer and inductor geometry requires special requests to a core manufacturers, alternate arrangements using regularly available cores in the market was agreed upon to implement the design. Following Fig. 38-41 depict the Altium 3D rendering of the designed converter PCBs.

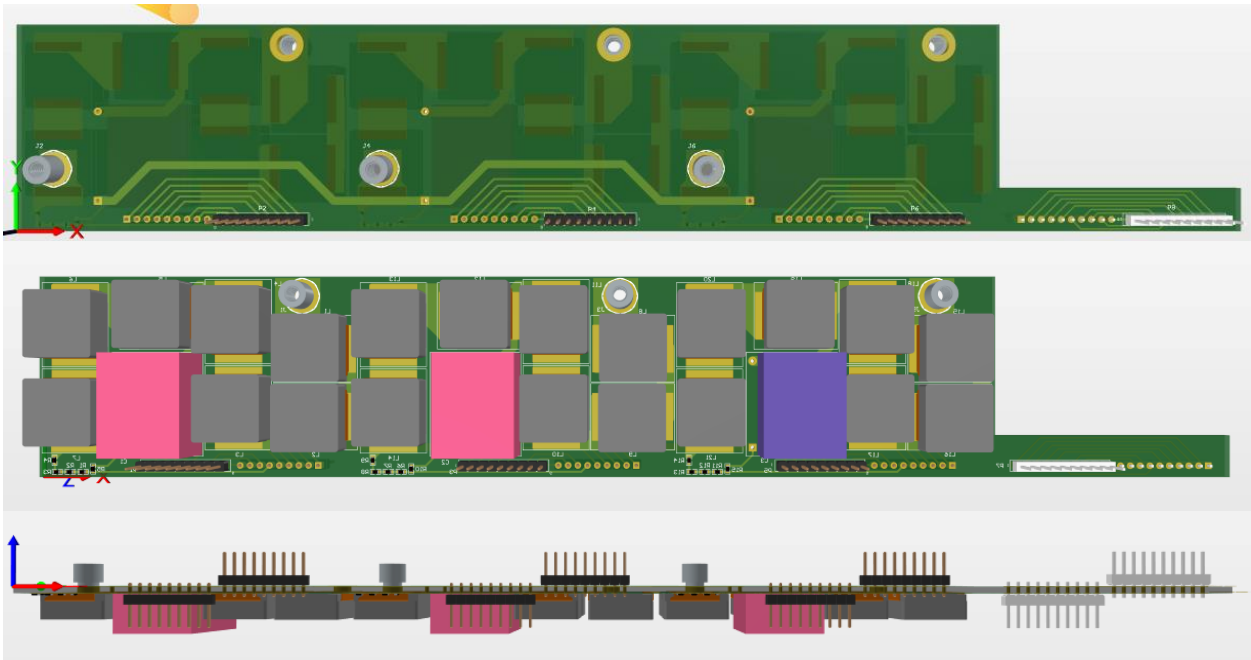

Figure 38: Top, bottom and side view of the LCL filter PCB

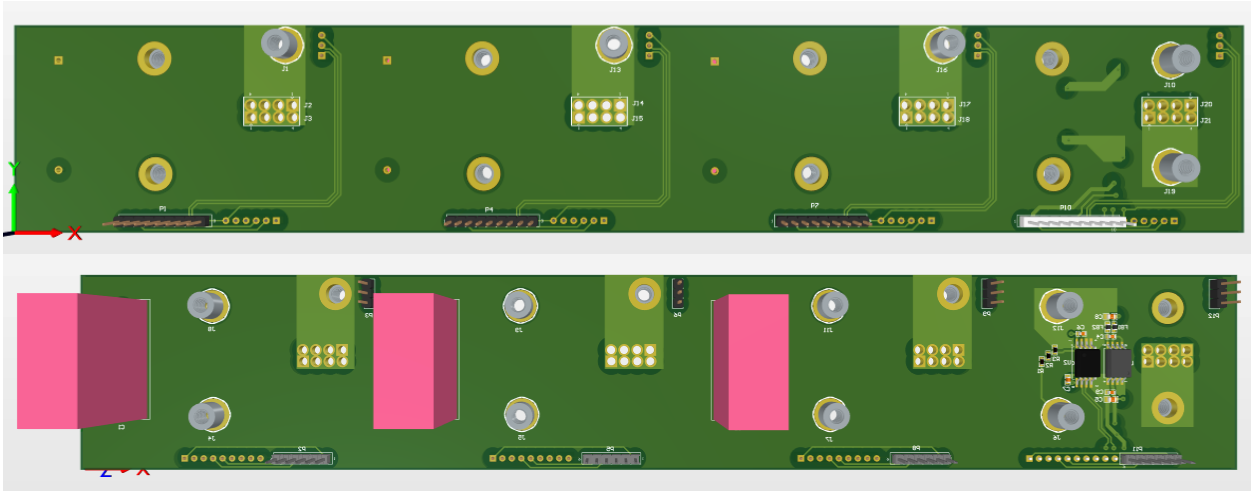

Figure 39: Top and bottom view of the DC bus capacitor PCB

Figure 40: Top and side view of the LLC primary PCB

The final converter bring-up has to be done and the hardware results need to be collected after the university operations resume post the coronavirus pandemic. Some of them haven't been populated yet due to laboratory accessibility while some couldn't be delivered due to closures enforced in place to retard the growth of the coronavirus pandemic.

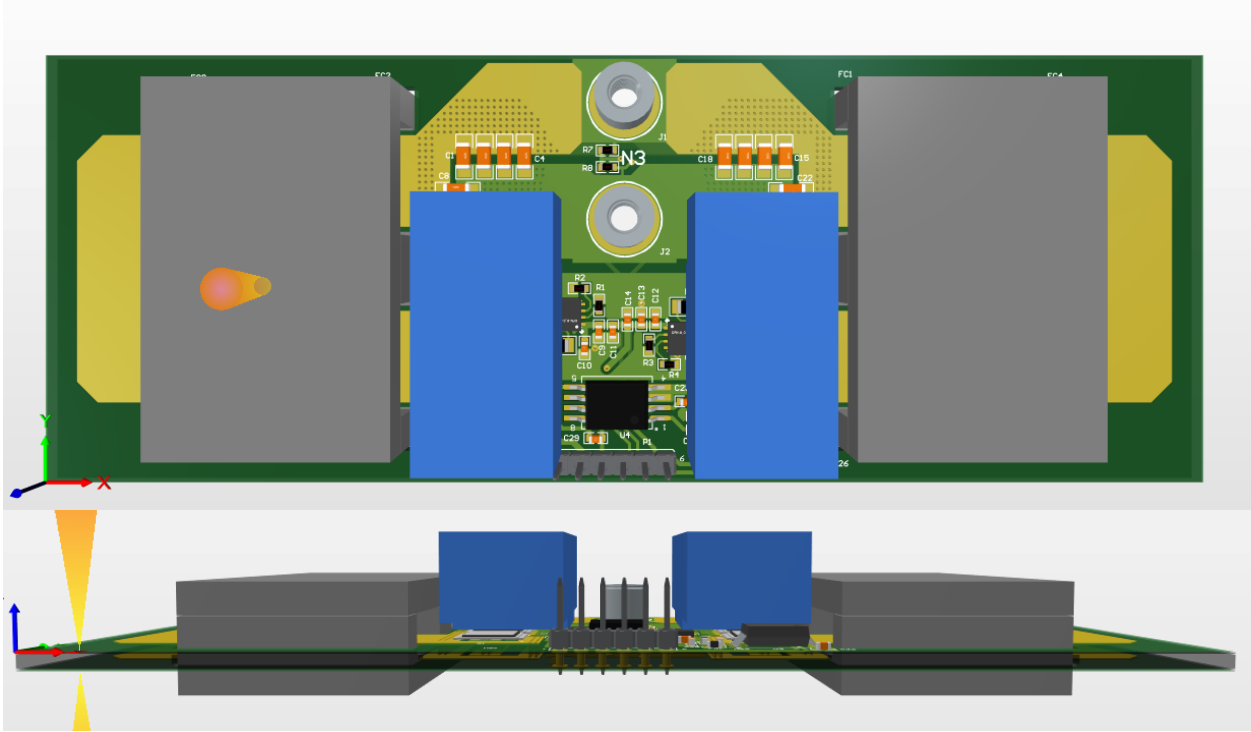

Figure 41: Top and side view of the LLC secondary PCB

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BIOGRAPHICAL SKETCH

Akash Neel Dey was born in Kolkata, West Bengal, India. He received a BE (HONS.) degree in Electronics and Instrumentation Engineering from BITS, Pilani, India in 2016. From 2016 to 2018 he was a full-time Hardware Engineer at GreyOrange Pvt. Ltd, Gurgaon, India, focusing on electrical and electronics hardware development for industrial and warehouse automation products. He started working on a Texas Instruments funded sensor development project with Dr. Andrew Marshall and Dr. Mark Lee in Texas Analog Center of Excellence (TxACE) at UT Dallas from 2018 to 2019. He joined Power Electronics Lab at UT Dallas under the mentorship of Dr. Ghanshyamsinh Gohil in 2019. His research interests include power converter development and optimization and high frequency magnetics design for power converters.

CURRICULUM VITAE

Akash Neel Dey

Education

The University Of Texas at Dallas, Richardson, Texas **Aug 2018-May 2020**
Master of Science in Electrical Engineering, CGPA 3.86/4.0
Birla Institute of Technology & Science, Pilani, India **Aug 2012-May 2016**
Bachelor of Engineering (Honors) in Electronics & Instrumentation, SGPA 3.6/4.0

Research Experience

Power Electronics Lab, Graduate Student Researcher, UT Dallas, TX **Apr 2019-Present**

- Master's thesis (P.I. – Dr. Ghanshyamsinh Gohil) on high efficiency GaN MOSFET based 10 kW LLC converter design for Data Centers.
- Designed Planar (multi-layer) integrated matrix transformer magnetics with flux cancellation and explored novel ways to add leakage layer and increase the power density of the transformer, verified in ANSYS FEM.
- Analytical modelling of converter loss and volume for multi objective optimization with Genetic algorithm (GA) in MATLAB for optimized converter design.

Analog Design Student Worker, TXACE, UT Dallas, TX **Nov 2018-Aug 2019**

- High gain amplifier & optical sensor IC design (PI – Dr. Andrew Marshall, Dr. Mark Lee) for position sensing & control for robotics applications.
- This amplifier and the sensor was designed in 130nm TI SMART power process.
- Implemented a position tracker system based on the above sensor using ADC and UART protocol which directly runs on the PC.

Teaching Assistant, University of Texas at Dallas - Physics **Aug 2019- Present**

- Course– Electricity & Magnetism (Sophomore) and assisted them with lab experimentation.
- Course– Electronics with Laboratory (Junior) and assisted them with lab experimentation.

Professional Experience

Hardware Design Engineer, GreyOrange Ltd., Gurgaon, India **Jun 2016-Aug 2018**

- Designed PCBs for AGV, conveyer based material handling and assisted in system design for automotive warehouse applications.
- Schematic design and layout using Altium Designer and firmware development on TI/NXP/STM microcontrollers.

Publications

Udumbara Wijesinghe, Akash Neel Dey, Andrew Marshall, William Krenik, Can Duan, Hal Edwards and Mark Lee, "**Integrated Circuit Angular Displacement Sensor with On-chip Pinhole Aperture**", *Sensors* **2020**, *20*(6), 1794; doi:10.3390/s20061794

Awards

- Jonsson School Graduate Study and Merit Scholarship **Aug 2018-May 2019**
- Teaching Assistant, University of Texas at Dallas - Physics **Aug 2019- Present**