RELIABILITY ASSESSMENT, CONDITION MONITORING AND LIFETIME ESTIMATION OF SILICON CARBIDE MOSFETS

by

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Dedicated to my family.

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The reliability of power semiconductors is a highly critical topic due to their widespread industrial applications such as aerospace, oil and gas, transportation, and power grid. In recent years, Silicon Carbide (SiC) MOSFET is proofed to be a strong alternative to conventional Silicon-based counterparts. Being a relatively new device type with limited field data and potential uncertainties, SiC MOSFET should be investigated from reliability and ruggedness aspects exhaustively to guarantee the long-term robustness of SiC-based power electronic systems. This dissertation comprehensively evaluates commercial SiC MOSFETs' reliability under various accelerated lifetime tests, develops on-board condition monitoring circuits, and proposes lifetime estimation solutions. An overview of SiC MOSFET aging mechanisms and up-to-date accelerated lifetime tests is first presented as a guideline for accelerated aging and aging assessment tests. By means of various accelerated lifetime tests, SiC MOSFETs are aged under different electrical, thermal, and mechanical stress patterns, and their corresponding aging mechanisms are investigated. Specifically, high electric field tests, active channel gate bias tests, and widely adopted power cycling tests are employed to trigger the device's degradation at both chip and package levels.

Throughout the tests, SiC MOSFETs are characterized by static electrical parameters and switching transients. Further, the device's aging impact on system-level performance is evaluated. Under the light of evaluated aging precursors, on-board condition monitoring methods are proposed, developed, and implemented. In terms of SiC MOSFET lifetime estimation, a MATLAB toolbox is designed and developed based on the system mission profile. By using the device's electro-thermal model and lifetime model, the accumulated damage and estimated consumable lifetime of certain SiC MOSFET is extrapolated. This dissertation intends to comprehensively study reliability issues of SiC MOSFETs from both aspects including test for reliability and design for reliability.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivation

Power semiconductors are the key elements in modern power electronics systems. Conventionally, Silicon (Si) based devices is used as main switches for power conversion. For low voltage (<650V) application, Si power metal oxide semiconductor field effect transistors (MOSFET) has been widely used. It features fast switching with low cost and enables system high power density design. However, a significant drawback of Si is that its energy band gap is low (1.1eV), resulting in low voltage blocking capability. If a Si based power MOSFET is designed to block high drain-source voltage, its drift region is supposed to be thick for standing high electric field (E-field). Consequently, its on-state drain-source resistance ($R_{ds\text{-}on}$) supposed to be high [1]. Hence, this drawback brings serious design considerations to the system from aspects including efficiency, power density, thermal design cost, etc. To overcome this drawback, Si based insulated gate bipolar transistor (IGBT) was invented by Dr. B. Jayant Baliga and has been extensively used in power electronic systems in great varieties so far [1]. IGBT utilizes a high power BJT transistor for high voltage blocking and current conduction. A parasitic MOSFET is only used for controlling the on/off state of the BJT transistor. Other than a thick drift region, the additional P^+ layer enables high voltage blocking with lower on-state voltage drop during on-state conduction. However, such bipolar design makes the minority carrier need to be swept out during turn-off transients in hard switching and causes tail current. Hence, Si based IGBT cannot be used at high switching frequency in high power conversion applications and results in low efficiency and power density.

Another common drawback of both Si based power MOSFET and IGBT is their temperature limitations. In modern industrial applications, power converters are expected to serve in wider range including aerospace, automotive powertrain, and oil field drilling. The requirement of system robustness not only covers normal operation but also harsh environment with high operating temperature.

In recent years, Silicon Carbide (SiC) MOSFET is proofed to be a strong displacement of conventional Si-based IGBT because of its suitability for high voltage, high frequency, and high temperature applications. The wider band gap of SiC enables a thinner drift region for voltage blocking in SiC MOSFET with higher doping concentration and much lower on-state resistance compared with Si devices [1]. In general, it refines the high voltage and power conduction issue of power MOSFET and overcomes the low-efficiency drawback of IGBT. Further, SiC has much higher intrinsic temperature limit and enhance system robustness in high temperature environments.

1.2 Reliability and Ruggedness Concerns

Considering the safety and mission critical applications in aerospace, oil and gas, transportation and power grid, long term reliability and operational stability of power devices are becoming an increasingly important requirement. However, power devices are one of the most vulnerable components in power electronics systems degrading due to electrical, mechanical, and thermal stresses [2]. According to industrial survey on dozens of power electronics companies, power switch is considered as the most fragile component in system because of severe operating environment and heavy loads [2]. Another recent report reveals that more than half of power

converter faults and maintenance issues are caused by power device failures [3]. Therefore, it is critical to conduct comprehensive reliability related studies for power switches.

As previously discussed, among the power devices, SiC MOSFETs are gaining favor over silicon-based counterparts due to their superior electro-thermal properties. They not only offer higher blocking voltage and higher switching frequency capabilities but also exhibit better thermal conductivity, which is crucial for high power density applications [4]-[6]. However, being a relatively new device type with limited field data and potential uncertainties, it is important to investigate the robustness and ruggedness of SiC MOSFETs exhaustively. In the field applications, it may take several years for a slowly growing incipient fault to cause device failure. Therefore, accelerated lifetime tests are used to proactively understand long-term device reliability under different operating conditions. They enable various aspects of reliability studies as shown in Figure 1.1.

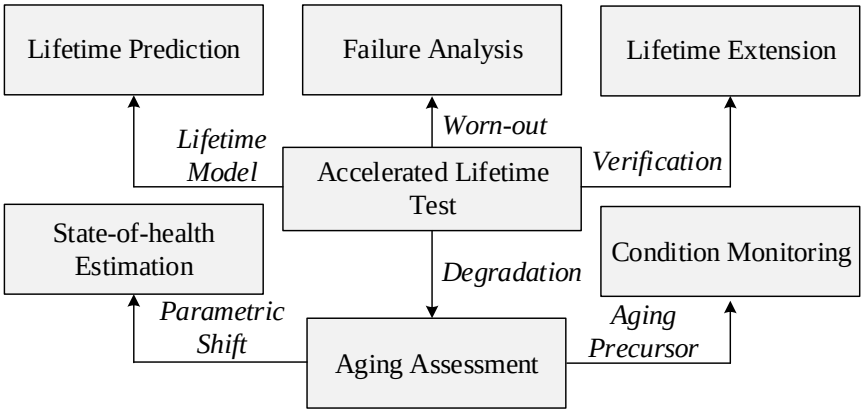


Figure 1.1. Reliability research directions for SiC MOSFET.

Accelerated lifetime tests generally accelerate device degradation by exaggerating the thermal and electrical stresses. There are various types of accelerated lifetime tests which target certain die or package degradation mechanisms using certain stress types. In field applications, depending on

the operating conditions, converter topology, mission-profile and environment, different degradation modes of SiC MOSFET are triggered. To observe and study these, it is essential to conduct accelerated lifetime tests to trigger expected aging mechanisms and mimic field conditions as much as possible. The data from these tests is used to evaluate the impact of aging on both device parameters and system performance. Additionally, these tests are also used to understand end-of-life (EOL) events [7]-[11]. The findings are further used to develop condition monitoring solutions, algorithms for the state-of-health assessment, lifetime estimation and improve the device design [12]-[20].

1.3 Research Objective

The goal of this study is to conduct comprehensive reliability studies on SiC MOSFET. In respect of test for reliability, this study intends to contribute following items:

- Survey and summarize SiC MOSFET aging mechanisms and accelerated lifetime test (ALT).
- Apply various ALTs to SiC MOSFET to trigger failure modes in wide range.
- Conduct failure analysis to investigate failure modes under various stresses.
- Investigate device electrical parameters shift over its lifetime.
- Investigate device's aging impact on its switching performance.
- Investigate device's aging impact on system performance, especially high frequency noise.

Further, in respect of design for reliability, several condition monitoring methods is proposed and developed. The purpose is to develop simple plug-in aging detection circuits which enables on-board aging precursors sensing. On the other hand, a lifetime prediction toolbox based on system

mission profile is developed. The purpose is to estimate accumulated damage on SiC MOSFET during system operation and predict upcoming failure on both device chip and package.

1.4 Dissertation Structure

In Chapter 2, an overview of SiC MOSFET aging mechanisms is carried out. The reliability concerns of commercially available SiC MOSFET comes from both chip and package levels. Aging mechanisms and end-of-life (EOL) failure modes induced by various kinds of electro-thermal and thermal-mechanical stresses are summarized. Further, the expected caused aging modes in various system operating conditions are reviewed and tabulated.

Chapter 3 summarizes existing ALT types for SiC MOSFET. In all summarized ALTs, test bench circuit, operating principle, triggered aging mechanism are introduced. As the outcome of this overview, ALTs are also compared regarding the triggered failure modes and stress severity. Further, an active channel gate bias test is proposed to evaluate SiC MOSFET gate oxide degradation under more realistic patterns compared with conventional high E-field test.

In Chapter 4, aging assessment of SiC MOSFET is carried out throughout various ALTs. Throughout the tests, device electrical parameter shifts are investigated, and potential aging precursors are defined. Aging patterns of both Kelvin-source and common-source packaged SiC MOSFETs are covered. Under the light of static parametric shift, aging impact on device's switching transients is studied by means of double pulse tester. Further, an active PFC is designed and developed using SiC MOSFET, and device's aging impact on system performance especially conductive EMI is analyzed by experimental results.

In Chapter 5, condition monitoring (CM) methods are proposed based on aging impact on device's switching transients. Specifically, Miller plateau voltage and turn-on time are utilized as aging

precursors and plug-in circuits which can be integrated as intelligent gate driver design is designed. A buck converter is constructed for CM circuit implementation and test methods are discussed.

Drain-source based CM method is proposed in Chapter 6. Compared with Chapter 5, the proposed aging detection method can separately detect aging at both chip and package levels. By employing drain-source resistance in both saturation and Ohmic regions, the proposed aging detection method is more practical with low cost and simplicity.

Chapter 7 presents SiC MOSFET lifetime prediction toolbox developed for system operation. The accumulated damage is extrapolated through device electro-thermal model and system mission profile. Through the developed toolbox, SiC MOSFET's consumable lifetime at both chip and package level can be estimated.

Chapter 8 summarizes the contributions and concludes the study.

CHAPTER 2

OVERVIEW OF SIC MOSFET AGING MECHANISMS

2.1 Chip Level Reliability

Failure modes and aging mechanisms at SiC MOSFET die level are summarized in Figure 2.1 at various vulnerable locations.

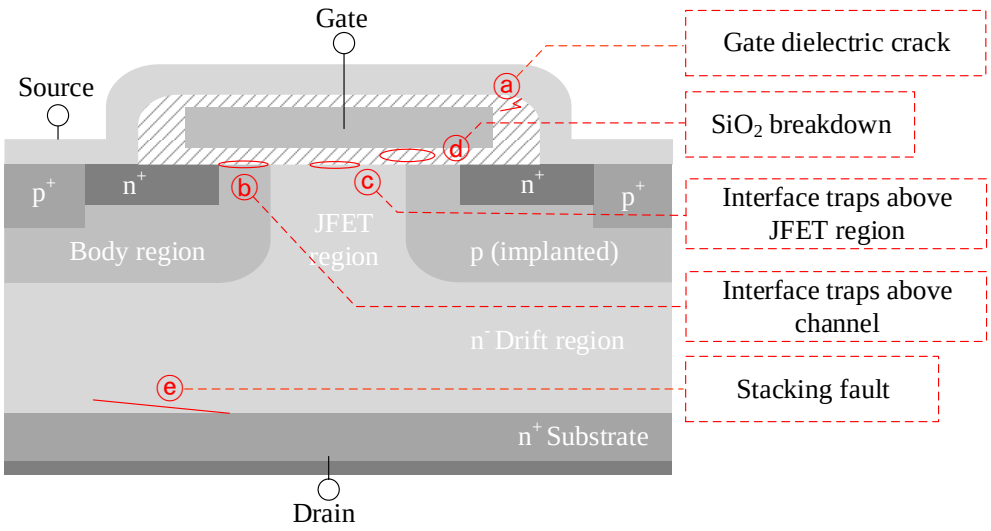


Figure 2.1. Failure modes within SiC MOSFET chip.

2.1.1 Gate Oxide

Gate oxide failure is a major reliability concern in SiC devices mainly due to their thin oxide layer [1]. Due to the larger band gap and higher *p*-based doping concentration, SiC MOSFETs are designed with much thinner gate oxide layer compared with Si-based counter parts to achieve reasonable threshold voltage and transconductance values [21]. Although a typical gate bias of 20V or lower is used to drive SiC MOSFETs, their intrinsic electric field across SiO_2 layer can easily reach 5MV/cm compared to maximum of ~3 MV/cm in Si devices [22]. According to widely

adopted model defined for lifetime estimation with dielectric breakdown, SiC MOSFET gate oxide's consumable lifetime is remarkably lower than Si counterparts [23]. Such aging mechanism is named as time dependent dielectric breakdown (TDDB).

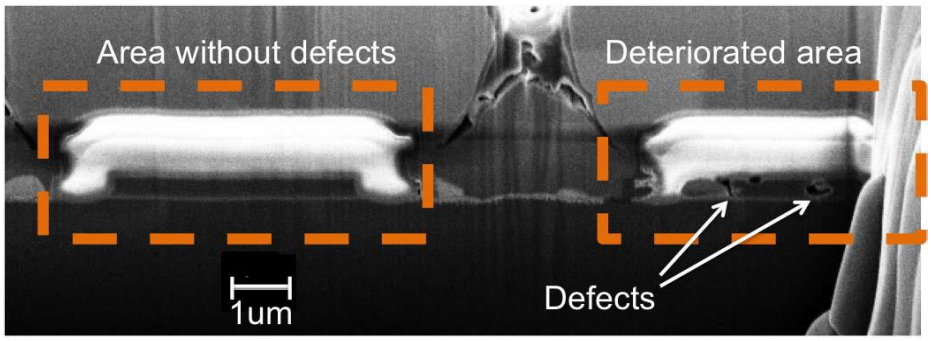


Figure 2.2. Scanning electron microscopy of healthy and degraded gate oxide [24]

Moreover, being a wide-band-gap device, the energy band off-set between SiC and SiO_2 is much lower than Si devices. The tunneling barrier of SiC/SiO_2 is as low as 2.70eV, making it much easier for the electrons to hop from SiC into gate oxide [25]. Electrons with adequate transition energy are directly accelerated by applied gate-source voltage during converter operation to reach anode (SiO_2). Furthermore, under high electric field (E-field) and elevated temperature, Fowler-Nordheim (F-N) tunneling current carrying electrons, flows through the oxide layer, breaking the Si-O bond over time and generating defects [26]. Eventually, these defects may line-up to form a path between the gate and source causing a large gate leakage leading to full breakdown of SiO_2 layer. In Figure 2.2, cross-section scanning electron microscopy (SEM) is used to compare the gate oxide layer of a healthy device with a device degraded under electro-thermal stress [24]. In the degraded device's gate oxide layer, defects can be clearly spotted in deteriorated area [24].

The main extrinsic reliability limiting factor is the relatively poor SiC/SiO_2 interface quality. This is an inherent challenge in device oxidation process during SiC MOSFET fabrication. The

presence of carbon (C) makes SiC/SiO_2 unsuitable for an abrupt oxide surface [27]. The roughness of SiC/SiO_2 interface caused by C-clusters and high C concentration, introduces traps and defects at both interface and near-interface locations [28]. During switching operations when gate biases are applied, these traps are charged by either holes or electrons causing threshold voltage instability and bias temperature instability (BTI) issues. Although a part of the trapped charge can be recovered by applying opposite gate bias or relaxation, the trapped charge can still grow deeper over time when defects gradually expand within oxide layer [29]. These charged traps not only lead to gradual generation of defects within shorten device's lifetime, they also cause serious reliability and performance issues such as decreased channel mobility and inconsistent threshold voltage [30]. Moreover, E-field resulting from the use of negative gate bias (-2V to -5V), which is normally recommended to ensure stable off-state, may also cause negative BTI, unlike conventional IGBT where 0V V_{gs} is normally employed for turn-off. In phase-leg configurations, gate voltage spikes generated by crosstalk effect during the complementary turn on and off transients may further increase the E-field stress on the device [31]. Hence, optimized thermal management and gate driver design are necessary to enhance devices' reliability and ruggedness.

Gate bias at elevated temperature is not the only stress source that devices are exposed to. During switching transients, the high E-field in the device channel caused by large drain-source voltage imparts sufficient kinetic energy to the electrons present in channel to cause hot carrier injection (HCI) effect and leads to device aging [32]. When device conducts under high drain to source E-field, impact ionization effect breaks electron-hole pairs. The generated carriers are injected into gate oxide and get trapped there. Therefore, board layout optimization is important since low

power loop inductance mitigates the transient voltage ringing and limits high drain-source electric field.

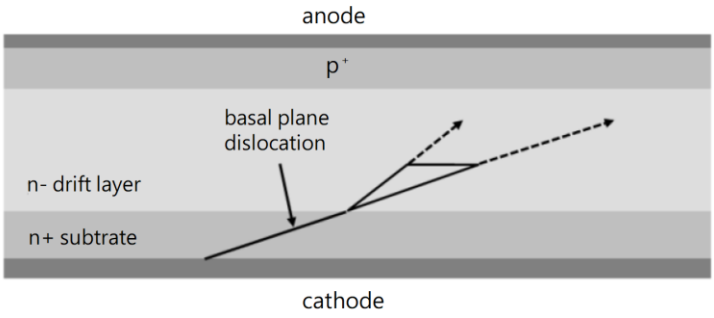
Gate oxide degradation typically results in high gate leakage (I_{gss}) and threshold voltage (V_{th}) instability. If operated with severe gate oxide degradation, a device may not be sufficiently driven due to high I_{gss} which may lead to higher gate driver and converter losses [33]. Further, unstable V_{th} causes extra power loss during switching transients and conduction. Additionally, it also leads to high drain-source leakage (I_{dss}) and negatively impacts device safe operating area (SOA) and surge current tolerance [34]. In high-power converters where multiple SiC chips are typically connected in parallel, V_{th} variations among the chips resulting from non-uniform gate oxide degradation may cause asynchronous switching. Consequently, the system may have an increased risk of thermal runway events.

2.1.2 Body Diode

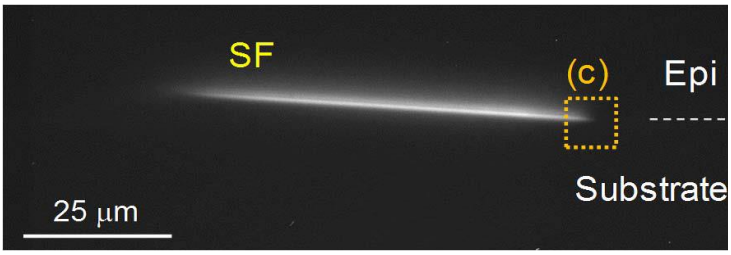
In most converter designs, Schottky diodes are placed in parallel with SiC MOSFETs to minimize the reverse recovery and reverse conduction losses and improve converter performance. Recently, there is an increasing interest in using the internal PiN body diode for cost reduction purposes [35]. Therefore, the reliability of SiC MOSFET's body diode is also critical.

In case of the PiN body diode, bipolar degradation is the primary degradation mechanism caused by off-state third quadrant conduction. During the device manufacturing process, different polytypic crystal structures form the SiC material. This results in lower stacking fault (SF) energy compared to Si devices and increases SiC MOSFETs' susceptibility to bipolar degradation [36]. The root cause of stacking fault under high body diode forward voltage (V_f) is the expansion of basal plane dislocations (BPD) during forward conduction [37]. Recombined electrons and holes

provide energy for BPDs to expand into a triangular shaped stacking fault within the drift region [38]. The expanded BPD travels through the epitaxial layer and creates a barrier for majority carrier conduction which causes carrier mobility reduction [39].



(a)



(b)

Figure 2.3. Exemplary BPD raised SF (a) mechanism and (b) PL image [38], [39].

Figure 2.3 illustrates bipolar degradation resulting from SF mechanism through the help of a degraded device's photoluminescence (PL) image [38], [39]. These SF formations increase both V_f and on-state resistance ($R_{ds\text{-}on}$) [40]. While V_{th} remains constant in post-stress state, gradual increase in I_{dss} can still be observed since the electron states generated by the expanded BPD serve as a charge generation center within drift region [41]. In converter-level applications, although SiC MOSFET body diode's surge current capability has been verified to be comparable to that of anti-parallel Schottky diode, its long-term reliability needs careful evaluation. The reduced carrier

mobility and device conductivity resulting from bipolar degradation causes power loss increase and temperature imbalance between parallel switches [42]. Furthermore, a positive shift in I_{dss} may also result in reduced voltage blocking capability. In this context, a modified safe operating area of SiC MOSFET with bipolar degradation is reported in [43]. Newly developed techniques such as pre-growth surface potassium hydroxide (KOH) etching and lithographic patterning can effectively enhance device ruggedness for third quadrant conduction and minimize BPD density [36]. From reliability assessment perspective, well defined ALTs are crucial if the system design relies on internal PiN diodes.

2.1.3 Gate Dielectric

To ensure system robustness, power converters are required to tolerate possible extreme operational conditions. A short circuit event, for example, causes a sharp rise in temperature inside the SiC chip. Similarly, electric shock induced device avalanche also causes rapid energy dissipation. As shown in Figure 2.4, cracks and cavities are observed through gate dielectric and causes device failure [44].

Such gate dielectric breakdown can be attributed to the extreme heat generated during either short circuit or avalanche conditions. Coefficient of thermal expansion (CTE) mismatch between different materials of SiC chip can provide a solid explanation for this failure mode. Under rapid temperature swings, the shear stress generated in aluminum source, gate electrode and gate dielectric layers due to CTE mismatch results in crack generation at the MOSFET cell corners. Furthermore, the chip temperature may exceed the melting point of surface metallization. In this case, the molten metal may diffuse into the cracks and result in a direct contact between gate electrode and Al-source [45]. Thermo-chemical model is an alternative method to explain

dielectric breakdown that considers weakened Si-O bond at high temperature and provides results consistent with discussion [45]. At elevated temperatures, the Si-O-Si bond strength weakens and linking bond angle can easily exceed 150°. Consequently, traps and defects are generated due to lattice distortion and bond rupture. The accumulation of these traps causes sudden increase in gate leakage and device catastrophic failure.

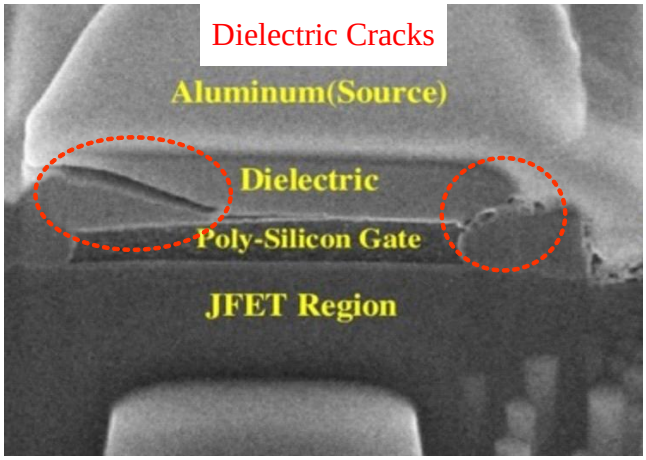


Figure 2.4. Cross-section SEM of gate dielectric as failure site [44].

2.2 Package Level Reliability

Figure 2.5 shows the vulnerable locations and corresponding aging mechanisms within SiC MOSFET's package.

2.2.1 Bond-wire Fatigue

Bond-wire fatigue is one of the most common package related failure mechanisms in power devices [46]. The primary reason for this is the thermo-mechanical stress resulting from CTE mismatch among various elements of the package during device operation [47]. CTE mismatch leads to both shear stress in adjacent layers of different materials and bond-wire flexure. Figure

2.6 depicts bond-wire heel crack and liftoff from cross-sectional SEM analysis of an aged SiC MOSFET. ALTs such as temperature cycling, and thermal shock are used to evaluate CTE based reliability issues. It is well-known that junction temperature (T_j) swing and average temperature in ALTs are the two dominant factors affecting wire-bond lifetime [48]. In addition to temperature induced mechanical stresses, bond-wire aging is also accelerated by active load current [49]. In converter applications with heavy load, the large drain-source current leads to generation of internal voids in the Al bond-wire due to electro-migration effect. Additionally, bond-wire's ohmic self-heating effect also accelerates the aging process.

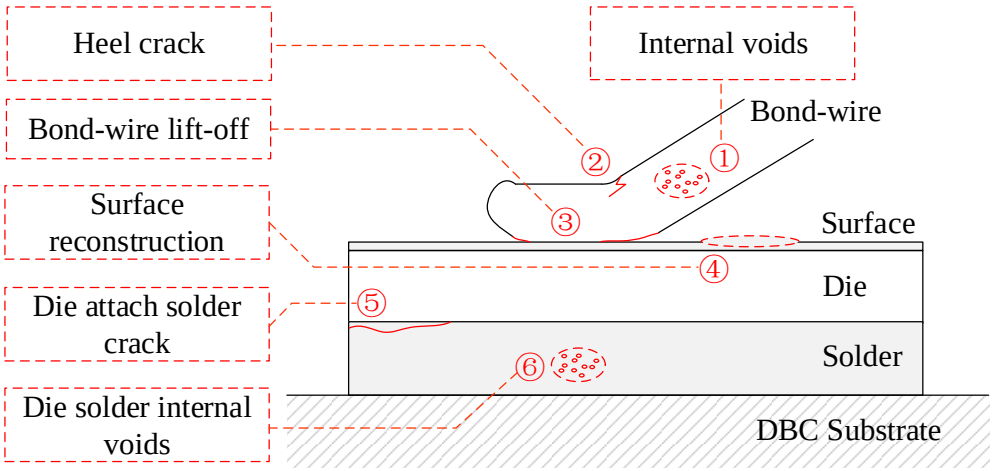


Figure 2.5. Failure modes within SiC MOSFET package.

Bond-wire fatigue mechanisms, namely bond-wire lift-off, heel cracking and internal voids directly result in a positive shift in device $R_{ds\text{-}on}$ [50]. Consequently, in converter applications, SiC MOSFET with severe bond-wire degradation will not only lead to a potential open-circuit fault but also increase the risk of an over temperature scenario.

2.2.2 Surface Metallization Reconstruction

The CTE mismatch between materials including Al and SiC not only causes package fatigue at bond-wire attachment, but also at surface metallization. Al source encounters thermo-mechanical stress owing to a much higher CTE value ($22 \times 10^{-6}/K$) compared to SiC substrate which has a relatively low CTE ($4.3 \times 10^{-6}/K$) [51]. At elevated junction temperatures, the device's Al surface yields to plastic deformation under the generated stress while the SiC substrate remains in elastic state. The pre and post stress scanning electron microscopy images of Al source surface are shown in Figure 2.7 [52].

The plastic deformation of Al source caused by temperature excursions normally results in crack propagation and $R_{ds\text{-}on}$ increment. Consequently, system thermal management is negatively impacted and failure modes such as open-circuit and over temperature are triggered.

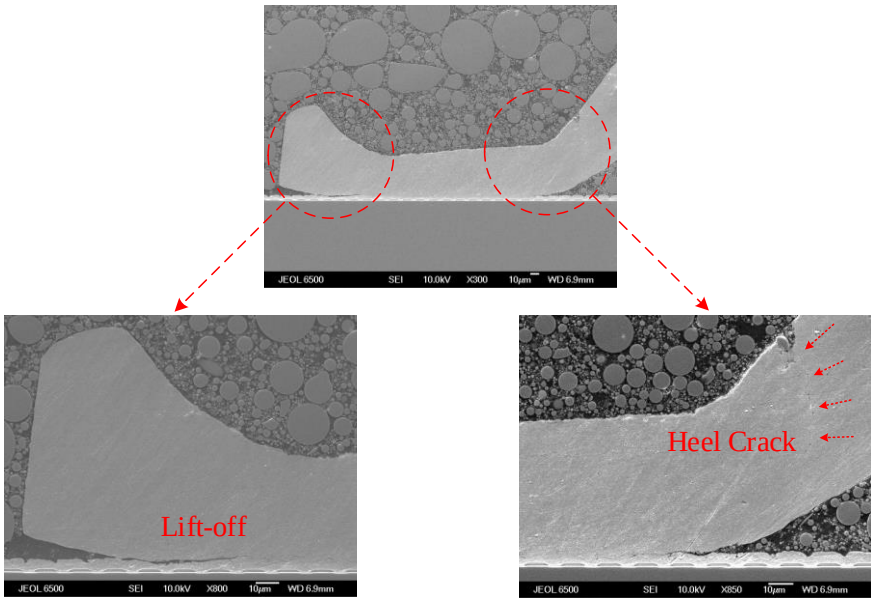
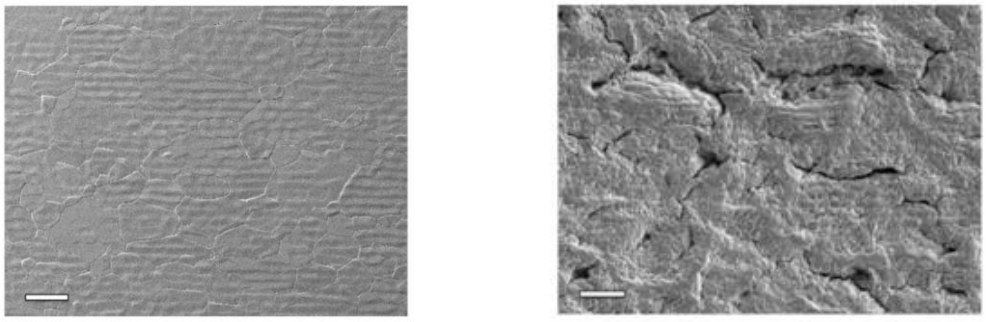
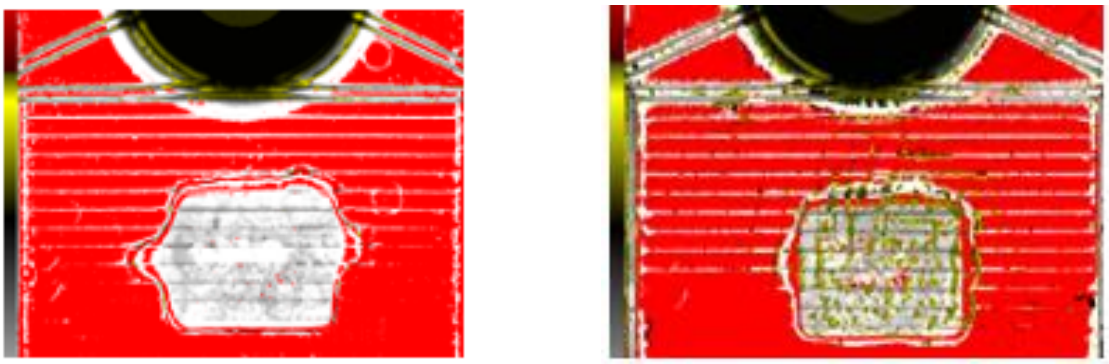


Figure 2.6. Bond-wire liftoff and heel crack detected by cross-section SEM.



(a) (b)

Figure 2.7. SEM image of Al source surface (a) pre-stress and (b) post-stress [52].



(a) (b)

Figure 2.8. (a) healthy and (b) aged die attachment through C-SAM analysis

2.2.3 Die Solder Fatigue

Soldering is typically used for die-attachment, i.e., connecting the SiC MOSFETs drain to the thermal pad in a TO-package device or a direct-bonded copper substrate in a power module. CTE mismatch between the SiC material and the die attachment solder layer can also cause solder fatigue under long-term thermo-mechanical stress. Physics-of-failure based reliability model is one of the tools used to understand the stresses generated at the attachment layer. The attachment cracks are not only a function of T_j swing amplitude, but also the swing frequency [53], [54].

Furthermore, the load current flowing through the solder layer during operation can also cause electro-migration of the solder material and lead to generation of internal voids [49].

Table 2.1. SiC MOSFET Degradation Modes during Converter Operation

System Operating Conditions	Failure Types	Main Degradation Mechanisms	Aging Indicator
Static operation with gate bias at high T_{amb}	Open circuit Short-circuit Over temperature fault	Gate oxide E-field	Gate leakage (I_{gss})
			Turn-on delay ($T_{d,on}$)
			Miller Plateau (V_{mp})
			Threshold voltage (V_{th})
Reverse conduction with body diode	Over temperature fault Short-circuit	Stacking fault	Body diode voltage (V_f)
			Drain leakage (I_{dss})
Wide T_{amb} range and heavy load transients	Open circuit Over temperature fault	Package fatigue (Bond-wire, solder)	On resistance ($R_{ds\text{-}on}$)
			Thermal resistance (R_{th})
			Turn-on Time (T_{on})
Short circuit tolerance	Open circuit Short-circuit	Package fatigue Gate oxide E-field HCI	Gate leakage (I_{gss})
			Threshold voltage (V_{th})
			Transfer curve
			On resistance ($R_{ds\text{-}on}$)
High bus voltage with switching transient	Short-circuit	Gate oxide E-field HCI	Threshold voltage (V_{th})
			On resistance ($R_{ds\text{-}on}$)
			Drain leakage (I_{dss})

In Figure 2.8, the die attachment layer of a TO-247 device before and after power cycling is compared using C-SAM analysis. As can be seen, voids inside solder layer and solder cracks around boarder extensively emerges after power cycling test. The generated defects lead to an increase in the junction-to-case thermal resistance thus causing a deterioration in the cooling performance of the device [54]. The junction-to-case thermal resistance can be used as a failure indicator [54]. Typically, this is done by defining an end-of-life threshold value (20%) [55]. Based on device degradation mechanisms under different stress types, device failure types and aging indicators are summarized in Table I.

As indicated in the first row, even when SiC MOSFETs are operated within their static electro-thermal SOA, the application of gate bias can still cause gate-oxide degradation through mechanisms discussed earlier and potentially lead to gate oxide failure. Moreover, the rate of gate oxide degradation is higher when the converter operates at high ambient temperature (T_{amb}) such as in oil-drilling or aerospace applications. In phase-leg configurations, high dv/dt across the device's Miller capacitance during switching transients can generate crosstalk voltage on the complementary switch [56]. Such crosstalk effect also aggravates the applied E-field stress on device's gate oxide and accelerates its degradation.

The definition and selection criteria of ALTs will be discussed in the next section in the context of the discussed failure mechanisms, device operating conditions and potential target applications.

CHAPTER 3

ACCELERATED LIFETIME TESTS FOR SIC MOSFETS

3.1 Gate Oxide Tests

To evaluate the impact of E-field stress on gate oxide, static voltages are applied at either gate or drain electrodes.

3.1.1 Static HTGB Tests

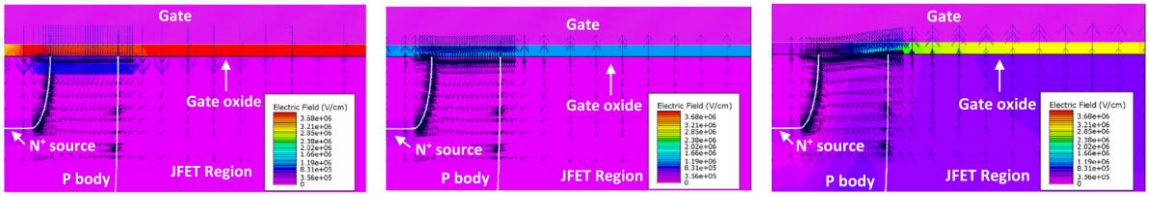
In HTGB test, DUT's drain and source electrodes are shorted to ground in order to set a stable 0V reference on bottom side of the SiO_2 layer [57]. Either positive or negative gate bias is applied across gate-source to generate high E-field in the oxide [58]. TCAD simulations can be used to analyze the E-field effect under various voltage stresses as depicted in Figure 3.1 [59].

Here, gate oxide layer above both JFET and channel regions is exposed to E-field with equal values. As discussed in Section II, both TDDB and BTI are the expected degradation mechanisms during HTGB tests.

3.1.2 Static HTRB Tests

Other than HTGB test, HTRB test is also used to introduce static E-field stress at elevated temperatures. Instead of gate bias, a drain-source voltage (V_{ds}) that typically exceeds the rated blocking voltage is applied to accelerate degradation as shown in Figure 3.1 (c). Additionally, the device gate and source are normally shorted to keep device in blocking state. Therefore, since drift and JFET regions of the chip withstand full applied drain-source voltage and channel is fully blocked, only gate oxide layer above JFET region is exposed to E-field. Because of the thin oxide

layer in SiC MOSFETs, gate oxide layer wear-out is the main failure mode in depletion-mode TDDB [60].



(a) V_{ds}=0V, V_{gs}=+20V (b) V_{ds}=0V, V_{gs}=-5V (c) V_{gs}=0V, V_{ds}=600V

Figure 3.1. TCAD simulation results for devices under static E-field stresses [59].

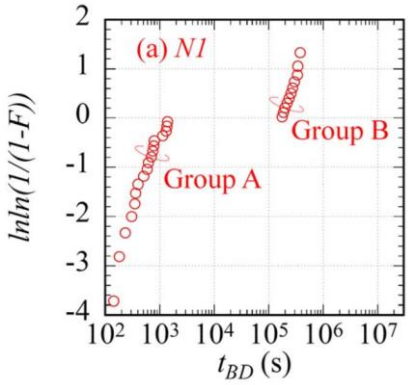


Figure 3.2. Weibull distribution of device's depletion-mode TDDB [61].

In addition to TDDB and BTI caused by high E-field, the leakage current under high drain-source voltage also induces HCI related gate oxide degradations [61]. As a result, at different V_{ds} levels, the extrapolated lifetime models are also different as shown in Figure 3.2 [61]. Here, a reverse bias voltage that significantly exceeds the rated blocking voltage of the device is applied to Group A, whereas a relatively low V_{ds} is applied to Group B. Figure 3.2 shows the Weibull distribution obtained by extrapolating the experimental results of HTRB test. It can be concluded that if the applied V_{ds} significantly exceeds the rated voltage range, the overall consumable device lifetime decreases. HTGB and HTRB are static gate oxide tests and there is no switching action in these

tests. To mimic gate oxide stress in field applications where the devices are switched, other tests can be implemented as summarized in the next part.

3.1.3 High Temperature Gate Switching (HTGS) Test

Unlike static gate oxide ALTs, HTGS tests use dynamic stress testing conditions to mimic real operations with switching transients. HTGS tests can be categorized into three types depending on device's switching conditions.

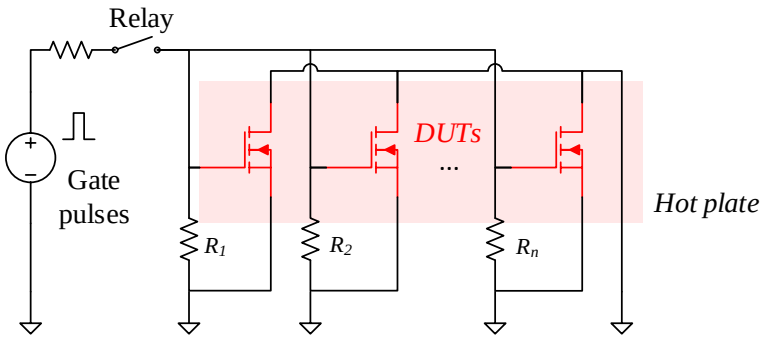


Figure 3.3. Gate oxide ALT under high frequency gate switching [62].

1) Pure Gate Switching

In this test, high frequency voltage pulses are applied across the device gate-source and no additional E-field is applied across drain-source as shown in Figure 3.3 [62]. The switching frequency and gate bias values can be selected based on the converter model and ALT purpose. A hot plate can be used to vary the operating junction temperature of DUTs. Further, a V_{th} sensing circuit can also be integrated in the HTGS setup for online monitoring and evaluation of V_{th} shift during the tests [62]. Generally, BTI induced V_{th} shift is a function of the switching frequency. Moreover, devices' V_{th} is expected to shift significantly as number of switching cycles increase even if equal on-state and off-state durations are used in the test [63].

The choice of applied gate bias value and test duration depends on objectives of the test. The rate of device degradation can be accelerated by using a high E-field stress. However, to mimic conditions during actual converter operation and observe realistic aging patterns, it is recommended to keep V_{gs} within rated range.

2) 0A Gate Switching

To account for the contribution of the system's bus voltage to the total gate oxide stress, 0A gate switching ALTs are proposed which take both V_{gs} and V_{ds} into account.

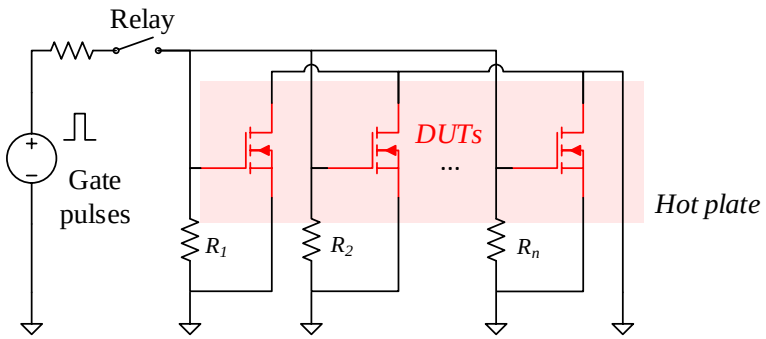


Figure 3.4. Gate oxide ALT under high frequency gate switching [62].

As shown in Figure 3.4, in addition to the periodic V_{gs} signal, system bus voltage is also applied to the DUT. However, there is no load in the system so that no current flows through the DUT's channel. This is done to ensure that there is no temperature difference between device junction and system ambient. The DUTs are arranged in a phase-leg configuration to enable the application of high frequency V_{gs} and V_{ds} voltages while ensuring that they do not conduct any current [59]. To mimic gate oxide degradation in an actual application, the gate pulses for the DUTs are generated using an open-loop SPWM scheme in [59]. This ensures that, the shift in aging precursors such as V_{th}, over DUT's lifetime follows a realistic pattern.

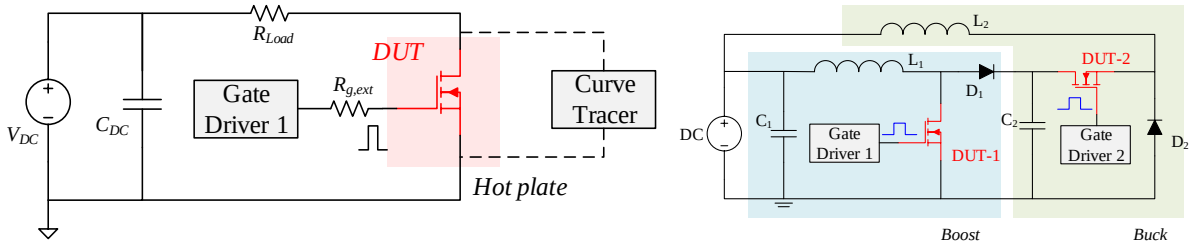
Compared to pure gate switching HTGS, 0A gate switching ALTs subject the DUTs gate oxide to dynamic E-field stress which is closer to real applications. Device V_{th} instability observed in this test is verified to be consistent with known aging mechanisms like TDDB and BTI [59].

3) Hard Switching Under Load

In applications like 3-phase VSI and buck converter, SiC MOSFETs experience hard switching. In addition to drain-source and gate-source voltage stress, device channel also actively conducts. Consequently, switching power loss due to overlap of V_{ds}, I_d and current conduction under high channel E-field cause device aging through impact ionization [64]. In this context, several methods for application of electro-thermal stress caused by switching transients are introduced for device gate oxide aging [26], [65]-[67]. In the first method, repetitive switching transients are directly applied to the DUT. A typical resistive load-based switching transient test circuit is shown in Figure 3.5 (a) [26]. To evaluate gate oxide aging under E-field stress that is equivalent to converter operations, normal gate bias value is selected. A resistive load is used to limit the conducted load current through DUT. Similarly, an inductive load can also be used in place of the resistive load. In this case, however, a free-wheeling diode across the inductor will be necessary to ensure the decay of inductor current in each switching period [65]. To mimic converter operations using hard-switching ALT, the applied bus voltage should not exceed rated blocking voltage. This may result in relatively long device lifetime and therefore long test durations. A hot plate is used to set the operational temperature of the DUTs. Over the device's lifetime, instead of showing a positive shift, V_{th} may decrease under high bus voltage as reported in [65]. It can be speculated that when the channel actively conducts during switching transients, electrons with high kinetic energy cause impact ionization on the device channel. Additionally, the holes generated from impact ionization

are injected into the traps in the gate oxide layer by the high E-field applied across drain-source [64].

In another type of hard-switching HTGS test, the DUTs are integrated into power converters such as pump-back system as shown in Figure 3.5 (b) [66]. Here, the external power supply only provides the DUTs' power loss. Due to the pump-back arrangement, the output power of the boost converter is pumped back by the buck converter into the DC bus. In this kind of ALT, due to switching transients and their effects on gate oxide, the DUTs are exposed to realistic stress conditions.



(a) Resistive load (b) Inductive load

Figure 3.5. HTGS circuits with load [26], [66].

However, it's hard to actively age DUT till failure in a relatively short time unless higher than rated gate bias is applied. Furthermore, the mismatch between junction and ambient temperatures caused by device power loss introduces additional unwanted thermal stresses. Consequently, such T_j offset may cause errors in lifetime estimation models. A common trade-off used to minimize T_j offset is to lower the switching event frequency. However, the use of low switching frequency may increase the total test time necessary to age DUT. Moreover, since multiple aging factors are active simultaenously in the hard-switching HTGS test, it is challenging to decouple their individual impact on DUTs lifetime. Because of several factors involved in selection of suitable HTGS test, depending on the test objective, the right type of gate oxide ALT should be chosen.

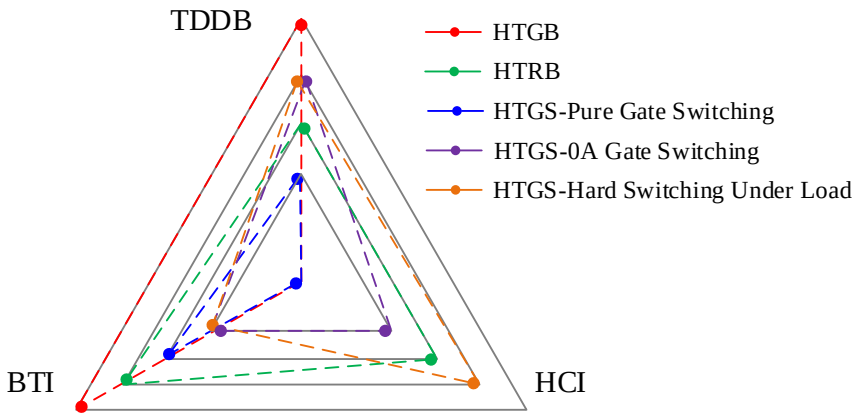


Figure 3.6. Electro-thermal stress applied in gate oxide ALTs.

Based on the preceding discussions, degradation mechanisms and corresponding impacts of various gate-oxide ALTs are summarized through a spider chart in Figure 3.6. In general, during device's forward conduction in power converters, the E-field generated by both V_{gs} and V_{ds} across the device gate-oxide is the primary contributor to gate oxide degradation. For quick reliability verification and lifetime model extrapolation, static tests are preferable while HTGS tests should be conducted for precursor verification and aging impact evaluation. Specific insights on gate-oxide ALT selection are highlighted as follow:

1) In static tests including HTGB and HTRB, the applied electro-thermal stress can be easily adjusted in wide range, without causing unexpected T_j offset and unwanted package fatigues. Hence, DUT's gate-oxide can be aged till failure in a quick manner. However, device's electric parameter shift may be unrealistic due to over-stress, and aging mechanisms caused by high frequency switching is disabled.

2) While HTGS test with either pure gate switching or 0A gate switching may introduce high frequency gate pulses and E-field distributions under realistic values, it's time consuming if DUTs

are required to be aged till failure unless V_{gs}/V_{ds} which largely exceeds rated value is applied. Also, aging mechanisms in real converter operation cannot be fully covered in these tests.

3) HTGS test under hard switching is preferable for precursor evaluation and aging impact study since it mimics real converter operation with aging mechanisms in wide range. However, T_j offset is unavoidable in this test and DUTs can be hardly aged till failure in a decent time.

Further, for all selected tests, total test duration is also an important test parameter and it is determined based on converter model, system requirement and ALT purpose. DUTs can be aged till failure for lifetime evaluation or study of EOL events. Alternatively, shift in the value of a certain aging precursor beyond a predefined threshold can be used to define device failure to reduce HTGS test duration. Specifically, EOL thershold for device parameters can be set to maximum values indicated in device's datasheet. Heuristic failure thresholds for shift in some precursors are recommended by manufacturers or standards committee (e.g. 20% V_{th} shift) [68]. Depending on the system requirements, these criteria can be tuned further. For instance, in high power density designs, V_{th} and $R_{ds\text{-}on}$ changes cause extra power loss and may result in a catastrophic failure. Therefore, in these applications, a lower value can used to define the failure threshold.

3.2 Package Fatigue Tests

3.2.1 Thermal Cycling and Thermal Shock

For ALTs to trigger package degradation caused by CTE mismatch between adjacent layers of the package, DUTs need to be subjected to temperature swings. The tests recommended by JEDEC [69], [70], for this purpose, are temperature cycling and thermal shock. In temperature cycling

tests, devices are subjected to temperature swing with combinations of different soak time, ramp rate and temperature limits. Depending on device package design and reliability requirement, the JEDEC standard recommends multiple test modes with different aging conditions. On the other hand, in thermal shock tests the devices are subjected to rapid temperature excursions and therefore experience higher thermo-mechanical stress within a short time. To do that, it is ensured that in these tests, the total transient time between low to high temperature and vice-versa doesn't exceed 20 seconds [70]. Physics-of-failure based reliability models can be used to quantify thermal-mechanical stress for different temperature ramp rates [53].

Both temperature cycling and thermal shock tests provide alternatives for device package reliability evaluation with relatively low complexity. Without the need to apply any electrical stress, programmable ovens or similar thermal testing platforms can be used to quickly evaluate the ruggedness of the device package. Further, lifetime models such as Coffin-Manson model can be used to extrapolate temperature cycling test results at different T_j swing amplitudes to obtain the expected in-application device lifetime [71]. In temperature cycling tests, average T_j is also a factor influencing device lifetime due to Arrhenius effect [72]. However, some of the more recent lifetime models not only take T_j-swing and mean T_j into account, but also consider device load current [73]. In field applications with high load current, factors like electro-migration effect and bond-wire self-heating also play a role in accelerating device aging. Therefore, for such applications, power cycling tests are preferred over temperature cycling or thermal shock tests for precursor identification, lifetime estimation, aging characterization, etc.

3.2.2 DC Power Cycling Test

In power cycling (PC) tests, device temperature is not forced to follow ambient temperature swing. Instead, a current is actively injected into DUTs and their conduction loss is used to heat them up. This causes thermo-mechanical stress at the various interfaces of the device package. DC PC test is widely adopted in reliability studies due to its low cost, simplicity, and its ability to be used for large-scale data collection. Typically, in a DC PC test, the device is heated up within a short period of time by injecting a current into DUTs channel. Once the device reaches the maximum target temperature, it is turned off and allowed to cool till it reaches the minimum target temperature. The process is repeated till device failure. Forced-air convective cooling or liquid cooling can be used to accelerate the cooling process and shorten the cycle time.

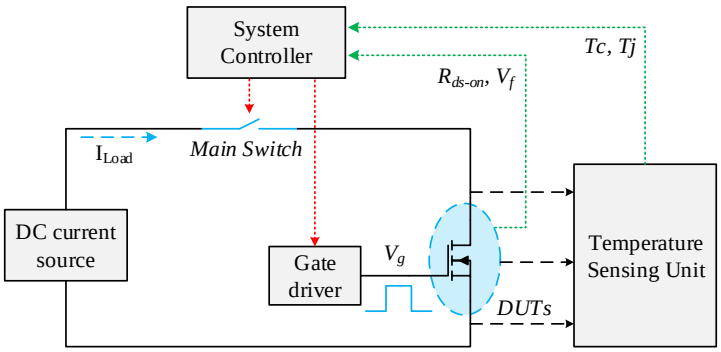


Figure 3.7. Operation principle of power cycling test.

A basic DC PC setup with key components is shown in Figure 3.7. DUT's load current is actively controlled by the main switch. During heating interval, DUT is turned on with positive gate bias. In this interval, the generated heat not only induces thermo-mechanical stresses on package, but also causes gate-oxide degradation due to the high electric field (HEF) generated by the applied gate bias. Typically, device $R_{ds\text{-}on}$, case temperature, and power loss data are collected, and can be

used for device degradation monitoring and online T_j measurement [74]. The choice of DC current source, temperature sensing and control, and precursor monitoring are critical design considerations and will be discussed in the following sections.

1) DC Current Source

Figure 3.8 illustrates two existing approaches to implement a constant current source in PC test for SiC MOSFET [75]-[77]. In Figure 3.8 (a), a buck converter based current source is developed using current feedback. With a high impedance load inductor and high switching frequency, the load current is maintained at the reference value [76].

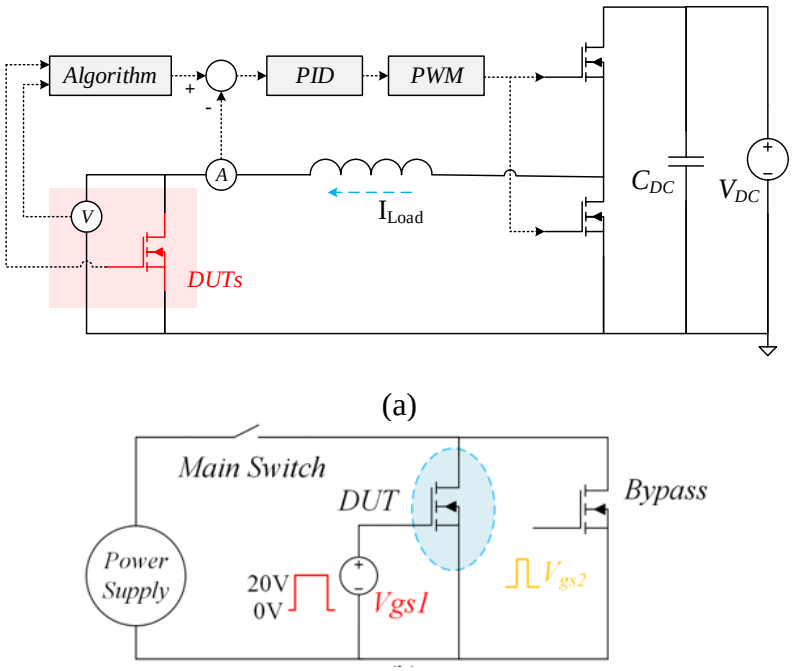


Figure 3.8. DC power cycling circuits with current source [76], [74]

In the second approach depicted in Figure 3.8 (b), the constant current mode of the power supply is utilized [74]. At the beginning of each cycle, DUT is off, and both the main switch and bypass switch are turned on. During this interval, there is a spike in the power supply output current as

the supply shifts from constant voltage mode to constant current mode. Once the current transient settles and load current reaches its steady-state value, gate signal is applied to turn-on the DUT. The parasitics in the circuit, cause another short transient when the DUT turns on. However, this is a relatively short transient, and once the DUT current reaches a steady-state value, the bypass switch is turned off and the load current fully commutates to the DUT. Here, the bypass switch is crucial in reducing commutation noise and ensuring a steady DUT current during DC PC test.

2) Temperature Sensing

The temperature profile throughout the device lifetime is important for lifetime modeling since it is used to calculate the cumulative thermo-mechanical stress applied to DUTs in PC test [78]. Therefore, the device case temperature T_c and junction temperature T_j are critical parameters and need to be accurately measured and controlled in PC tests. Device T_c can be easily monitored by either using a thermocouple or an IR camera [79]. If a heatsink is used in the PC setup, a mechanical solution, such as drilling holes in the heatsink to directly attach temperature sensors to DUT case can be used. T_c can also be estimated by feeding the calculated power loss information into the device case-above-ambient thermal model [80]. However, during DC PC tests, the degradation of die solder and heat-sink attachments may cause a change in the device thermal model thus leading to an estimation error in the long-term. Therefore, it is recommended to use direct temperature sensing techniques if T_c profile is required for temperature control.

Since T_j is the most critical temperature parameter, it needs to be measured accurately in real-time during PC tests. However, in most packages, it is challenging to directly access the MOSFET die for T_j sensing. Therefore, indirect T_j estimation using temperature sensitive electrical parameters (TSEP) is the preferred technique. Several T_j sensing techniques proposed in the context of

converter applications can be used for online estimation of the DUT junction temperature in a PC test as well [81]. Since device conducts continuously during heating interval, device's $R_{ds\text{-}on}$ can be used as a TSEP to calculate T_j at relatively low cost and complexity. However, since $R_{ds\text{-}on}$ is an aging dependent parameter, using it as a TSEP without aging compensation may lead to significant error in T_j measurements. Therefore, to ensure consistency of the applied thermo-mechanical stress, periodic recalibration of $R_{ds\text{-}on}$ with respect to T_j is necessary throughout PC test. The body diode forward voltage drop V_f is another widely used TSEP that is proven to be aging independent at low current and a negative gate bias. For in-circuit measurement of V_f, small current is injected into the device body diode during the cooling interval while the device is kept off using a negative gate bias. Further, a closed loop control strategy is implemented for maintaining the device T_j swing within the set limits. Body diode's electroluminescence is a temperature sensitive optical parameter that can also be used for galvanically isolated T_j sensing during PC tests. However, in this technique, the DUTs need to be decapsulated to expose the chip which may not be possible in certain applications.

3) Monitoring Parameters

Multiple parameters are monitored during PC tests for reliability assessment and aging observations. The most monitored parameters are $R_{ds\text{-}on}$ as a bond-wire fatigue precursor, V_f at low current and negative gate as a TSEP, and device thermal resistance as a die solder fatigue indicator [82]-[84]. Power loss is also monitored through device voltage and current measurements and essential for lifetime estimation calculations. Additionally, device thermal resistance (R_{th}) can be calculated by monitoring both T_c and T_j at thermal steady state.

4) Temperature Control Strategy

In DC power cycling tests, devices can be aged under different temperature profiles and temperature control schemes. Constant on/off time control is the easiest to implement since it is a simple open loop control strategy. In this method, temperature sensing is only needed for either case or junction temperature calibration. However, change in $R_{ds\text{-}on}$ and V_{th} values due device degradation can change device power loss and may cause variations in T_j swing during the test. Therefore, temperature offsets are inevitable and leads to deviation from the pre-set T_j profile [85]. Therefore, to minimize the temperature errors, the on and off times need to be adjusted periodically. Constant power control is another commonly used temperature control strategy in DC power cycling. In this control method, DUT's conductive power loss is maintained at a constant value during the heating interval. An adjustable gate driver is used to change the device's operating point on the I-V curve to actively control the power loss [49]. Further, any thermal deviations that potentially result from aging induced V_{th} and $R_{ds\text{-}on}$ shift can also be compensated by adjusting the gate voltage [85]. However, due to the varying load current and gate bias, electro-thermal stress experienced by the device is inconsistent. Therefore, obtaining a device lifetime model from this test is challenging since that requires fixed aging conditions. One advantage of this control strategy is that it can limit the device power loss to safe levels and thus prevent a potential thermal runway scenario.

Constant ΔT_c control can be implemented to reduce the cost and system complexity [86]. Typically, in this strategy, a thermocouple is used to directly sense device T_c. Further, device T_j can either be monitored by using a TSEP sensing circuit or estimated by using T_c and device thermal model. An exemplary illustration of power cycling bench with T_c based temperature control is shown in

Figure 3.9 [74]. In this circuit, a thermal couple is tightly attached to the back of the device package to obtain real-time T_c measurement. Due to aging related changes in R_{th} over the device lifetime, it is possible to observe higher than set levels of T_j in this method.

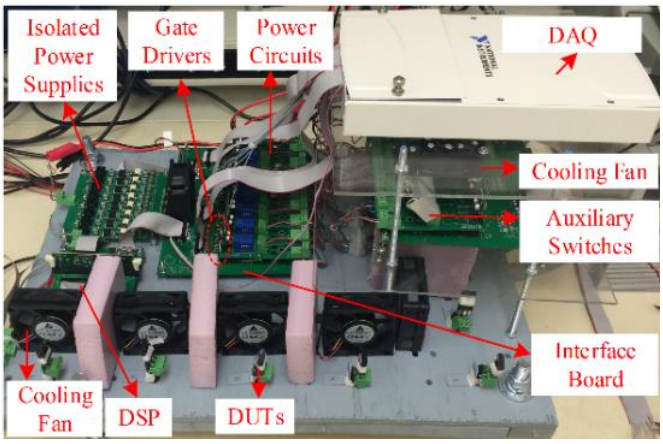


Figure 3.9. DC power cycling bench with T_c control [86].

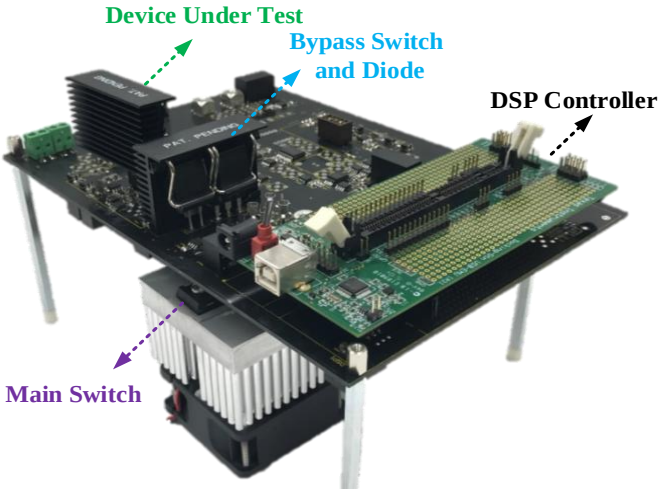


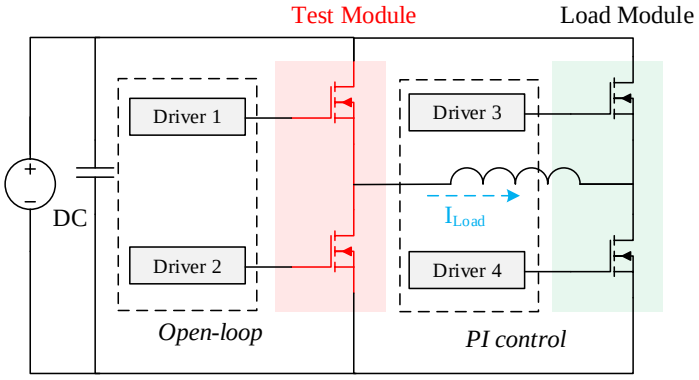
Figure 3.10. DC power cycling bench with T_j control [74].

In constant ΔT_j mode, devices are aged under fixed gate bias, load current and junction temperature swing [74]. This mode is highly useful for studies like aging assessment, precursor identification and lifetime estimation. In the test bench shown in Figure 3.10, DUT is aged under constant T_j

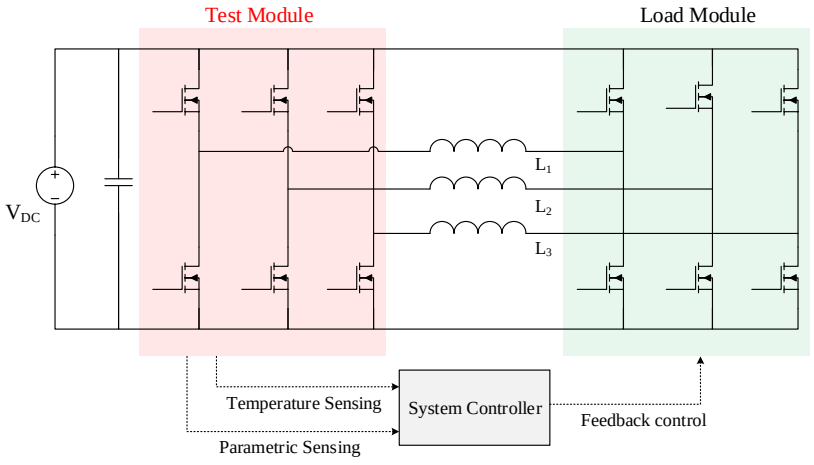
swing. Here, V_f is used as a reliable TSEP for estimating the device T_j and close loop T_j control is implemented to ensure accurate T_j swing.

3.2.3 AC Power Cycling Test

In DC power cycling tests, unlike real converter operation, the DUT is subjected to temperature swings using static conduction and the impact of gate switching is neglected. To address this, AC power cycling tests are used to mimic realistic aging mechanisms.



(a)



(b)

Figure 3.11. AC PC with (a) single-phase and (b) three-phase circuits [87], [88].

In AC power cycling test, DUTs are switched at a relatively high-power level with a time-varying load profile like in actual converter operation. Single phase or three phase back-to-back converters are generally used for AC power cycling as shown in Figure 3.11 [87], [88]. Consequently, the main power supply is used to provide only the power losses of the system. Other than 3-phase load inverter, cogent circuits connected to other types of AC loads are also used for the same purpose such as motors [89].

Unlike DC power cycling tests where a low DC bus voltage is used, in AC PC, the DUTs are operated at realistic bus voltage levels at high switching frequency under inductive load. Therefore, the device gate-oxide is also subjected to electro-thermal stress caused by V_{ds} induced E-field and high frequency gate switching. In Figure 3.11, the load module is closed loop controlled. and DUT's aging conditions including phase angle, load current, T_j swing and line frequency can be actively adjusted.

In another type of AC power cycling test setup, the DUTs are part of a grid connected active front-end PFC converter [90]. Unlike the AC PC test in Figure 3.11 with adjustable phase angle, DUTs can only be forward conducted in the PFC converter due to its fixed power factor. Although this AC PC method reduces the system complexity, it results in higher average temperature during the test because of the fixed grid frequency [90]. When compared to other ALTs which can accelerate only certain degradation mechanisms, both types of AC power cycling tests trigger wider package and die related aging mechanisms like real converter operation.

Figure 3.12 summarizes various temperature/power cycling test types and corresponding degradation mechanisms' severity. As discussed, power cycling tests enable device's degradation in a more realistic way with actively conducted channel while temperature cycling tests only

induce ambient temperature excursion as environmental stress. Hence, package elements including bond-wire and die solder are expected to encounter higher stresses in power cycling tests.

Conventionally, power cycling tests are normally intended to evaluate package level reliability of power switches. For SiC MOSFET, although package degradation is the dominant degradation mechanism in power cycling test, the applied gate bias at elevated temperature also subjects device's gate-oxide to electro-thermal stress. Therefore, gate oxide degradation mechanisms like TDDB and BTI are also observed. In Figure 3.12, HEF stands for E-field induced degradation on gate oxide including TDDB and BTI effects.

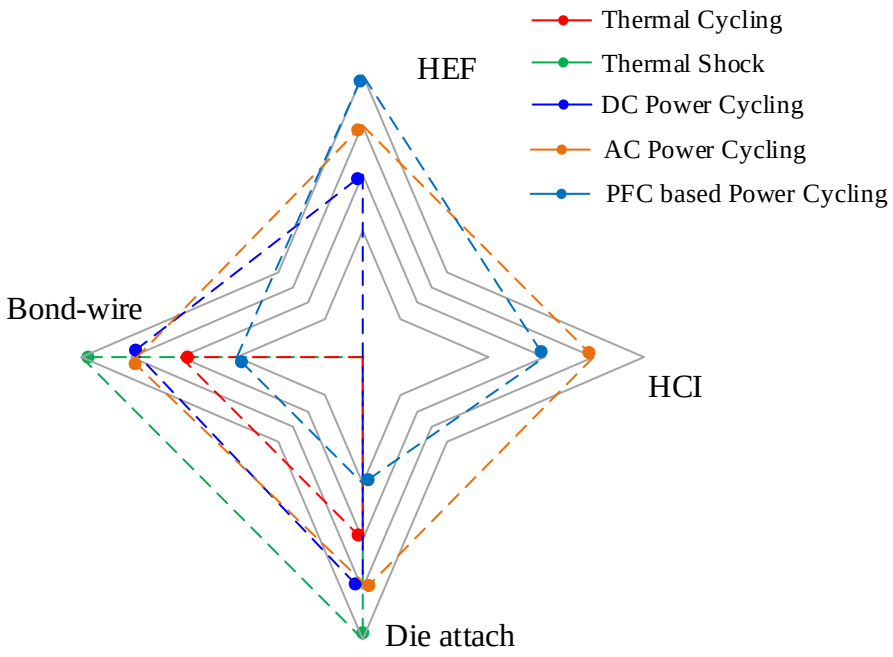


Figure 3.12. Stresses applied in package related ALTs.

By comparison, PFC based test triggers gate oxide degradation with more severity due to its high switching frequency and relatively high average temperature. Moreover, AC power cycling test is expected to create higher impact ionization caused hot hole injection than PFC based power cycling test since HCI effect is reduced in elevated temperature. In DC PC test, since the applied

bus voltage levels are normally low and within device's Ohmic region, HCI is not observed during the test.

3.3 Body Diode Tests

In SiC MOSFET applications, there is a growing trend towards using the SiC MOSFET's internal body diode instead of an anti-parallel diode (diode-less converters) [91]. Regarding SiC MOSFET's third quadrant conduction, understanding the degradation pattern of internal PiN diode is critical for ensuring device ruggedness and converter robustness. The basic principle of 3rd quadrant ALTs is to generate failures in the DUTs by inducing stacking faults through body diode conduction.

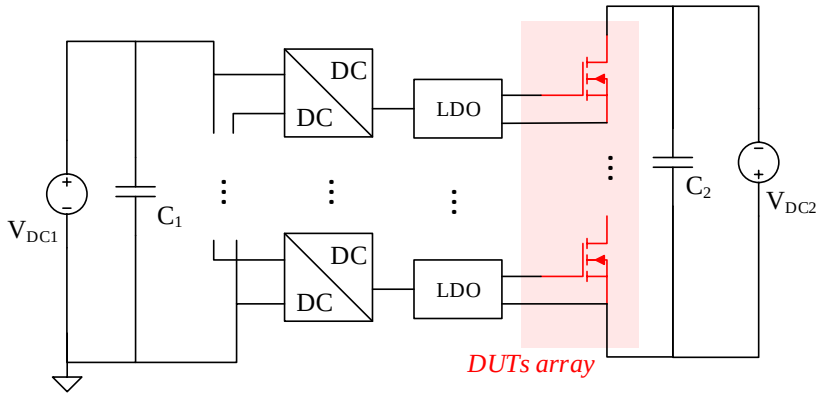


Figure 3.13. Body diode reliability test circuit with 10 DUTs [92].

3.3.1 Inverse Current Injection Test

In DC current injection test (DC-CIT), DUTs are reverse conducted under constant load current. An exemplary circuit used for aging DUTs by accelerating the bipolar degradation mechanism is shown in Figure 3.13 [92]. To ensure that the DUTs' channels are completely off, a negative gate

bias is used in gate driver circuits instead of zero gate bias. Bipolar degradation is accelerated through high current density and elevated temperature. Hence, a hot plate can be used in this test to increase the DUT's aging rate.

3.3.2 Chopper Mode Bias Test

To mimic a high-voltage application where the SiC MOSFET works in switching mode, a chopper mode bias (CMB) test as shown in Figure 3.14 is proposed to stimulate bipolar degradation. A buck converter is used in the setup followed by a boost converter. The load inductor L_1 is shared by both circuits. Specifically, boost converter is used for maintaining load current at desired value and circulating output power back to bus [93], [94].

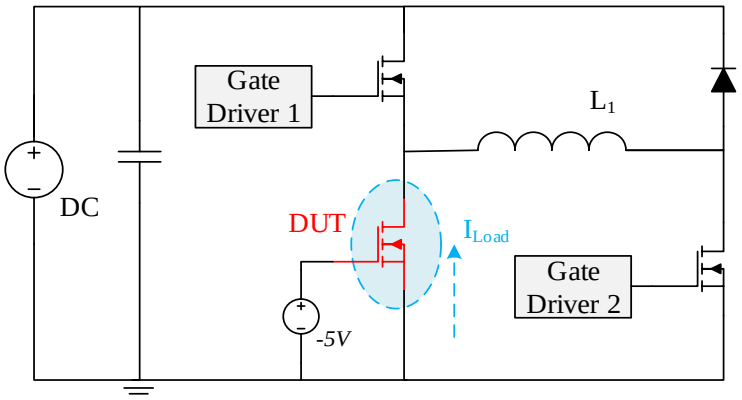


Figure 3.14. 3rd quadrant chopper mode bias test circuit [94].

In both DC-CIT and CMB tests, the DUT is turned off using a negative gate bias at elevated temperatures. Therefore, in addition to bipolar degradation, the induced E-field stress also causes gate oxide degradation and V_{th} instability [94].

In bipolar degradations, the main aging effect is V_f increment. In third quadrant ALTs, the overall V_f shift over DUT lifetime is strongly dependent on the current injection duration and recovery

time. It is discussed in [95] that the inverse conduction in pulsed regime may mitigate DUT's bipolar degradation compared to consistent current injection. Also, the extended BPD may self-recover over time, and the relax time between device aging and characterization is also considered as an impact factor of V_f increment.

3.3.3 Surge Current Test

To evaluate SiC device's robustness in diode-less converter topologies, understanding the surge current capability of SiC body-diode is critical. For this purpose, the surge current capability of an anti-parallel JBS diode is compared to the body diode of SiC MOSFET [96]-[98]. The same test setup is inherited as ALT bench for body diode reliability assessment under repetitive pulses.

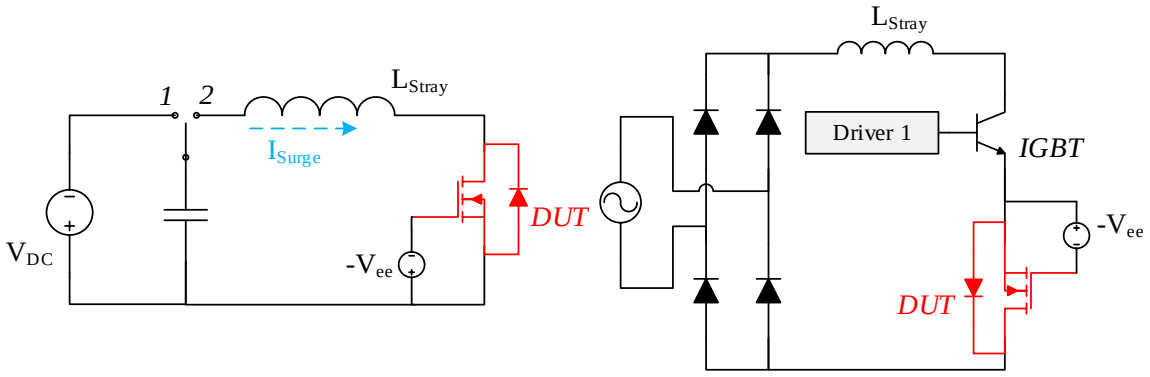


Figure 3.15. Exemplary Circuits for 3rd quadrant surge current test [99], [100].

Figure 3.15 shows the circuit diagrams of the 3rd quadrant surge current test circuits [99], [100]. In test circuit shown in Figure 3.15 (a), the DC link capacitor is pre-charged before device conduction. The resonant tank formed by load inductor and bus capacitor enables half-sinusoidal surge current injection through DUT source-drain [99]. Similarly, diode-bridge circuit can also be

used to generate surge current as shown in Figure 3.15 (b) [100]. In these tests, it is intended for the devices to fail due to bipolar degradation. However, since the devices have significant conduction loss during surge current conduction, they may fail due to thermal runaway if appropriate measures are not taken. Therefore, sufficient delay is ensured between each surge current injection interval, to allow the device to cool down and prevent its T_j from building up during the test. The cool-down duration is chosen based on the junction-above-ambient thermal conductivity and cooling conditions.

Owing to the relatively high body diode voltage drop, SiC devices may experience significant temperature rise during 3rd quadrant conduction. Therefore, the aging mechanisms in 3rd quadrant surge current test are a combination of both gate oxide and body diode degradation. Although an increase in V_f is observed, the failure is generally caused by high I_{gss} and I_{dss} due to gate-oxide degradation [100]. Due to the rapid T_j increase, surge current test induces higher stress on gate oxide compared to CMB test. Therefore, it fails to accelerate bipolar degradation mechanism significantly because of its short conduction interval and long recovery phase.

3.3.4 3rd Quadrant Power Cycling Test

Power cycling tests are also conducted for body diode reliability evaluation. Figure 3.16 depicts a commonly employed circuit for 3rd quadrant DC power cycling. SiC MOSFETs generally have a high V_f due to their high band gap [101], [102]. Therefore, when compared to channel conduction, utilization of body diode conduction enables shorter heating intervals during power cycling test. In this test, both the package and body diode related degradations are observed.

Unlike DC power cycling setups, the low amplitude current injection for V_f sensing in Figure 3.16 is valid for aging precursor measurement instead of T_j measurement. In this power cycling mode,

V_f can no longer be adopted as TSEP for real-time T_j sensing. Further, the V_{th} instability caused by constant applied negative gate bias also results in gradual $R_{ds\text{-}on}$ shift is also expected in this mode. Therefore, when compared to forward-conduction DC power cycling, it is more challenging to obtain accurate real time T_j measurement in 3rd quadrant power cycling tests. Consequently, for DUTs without die-integrated temperature sensing, aging compensation is necessary for TSEP based T_j sensing [102].

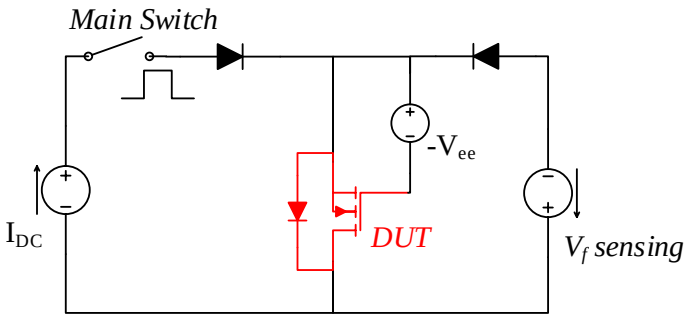


Figure 3.16. Inverse diode mode power cycling circuit [102].

Apart from DC power cycling test, AC power cycling test can also be used to evaluate bipolar degradation for more realistic aging conditions. As shown in Figure 3.11 (b), load inverter is used to actively tune the load current phase. At power factor equals -1, current flows in reverse direction through the DUTs and triggers bipolar degradation [88]. Similarly, PFC topology can also be used for third quadrant focused AC power cycling. In this case, instead of single-phase PFC, totem-pole type PFC is needed to operate SiC MOSFET in 3rd quadrant. Unlike DC power cycling, DUTs in AC power cycling test operate at a high switching frequency under realistic stress scenarios. However, the intrinsic electrical stress experienced by DUT's body diode is lower in AC PC tests. Therefore, longer test times are necessary to trigger SF in DUTs.

The degradation mechanisms for various 3rd quadrant tests are compared in Figure 3.17. As discussed earlier, in compared to other ALTs, DC-CIT induces severe stress on the body diode by continuous current injection. Since the rate of bipolar degradation is inversely proportional to the reverse conduction pulse duration and frequency, it is a less prominent degradation mechanism in surge current tests when compared to power cycling tests. Evaluation of surge current test results reveals that bipolar degradation occurs to a lesser degree than gate oxide degradation which is the dominant failure mechanism in these tests. Further, due to the generation of large temperature swings, repetitive surge current tests trigger package level degradation in SiC MOSFETs whereas DC-CIT and CMB tests can hardly accelerate package related degradation.

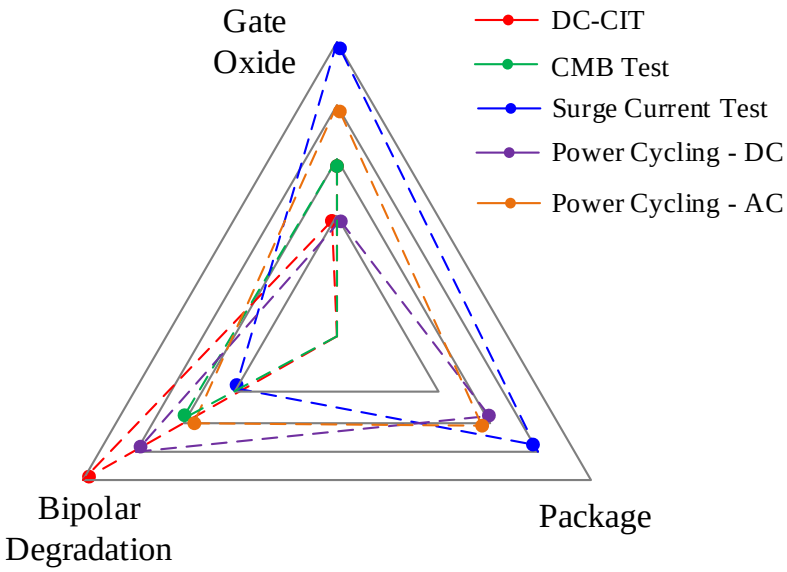


Figure 3.17. Aging locations where stress applies in 3rd quadrant ALTs.

In general, insights are highlighted as follows:

1) DC-CIT should be selected to trigger bipolar degradation since no other aging mechanisms are accelerated with electro-thermal stress.

2) In 3rd quadrant surge current test, gate oxide, instead of body diode is expected to be device's ruggedness limitation.

3) Even though body diode can be used for power cycling test to accelerate T_j swings with lower current, bipolar degradation is also triggered as side-effect. Hence, PC test in 3rd quadrant cannot be used for precursor identification in real system applications.

3.4 Extreme Condition Tests

In addition to normal operating conditions, devices are expected to withstand momentary out-of-SOA operation. For instance, unexpected events such as over temperature, and electromagnetic noise may cause device short circuit (SC). Also, events like electric shock may cause avalanche conduction. To evaluate SiC MOSFET reliability under over voltage or over current conditions, repetitive SC, and repetitive unclamped inductive switching (UIS) tests are generally used.

3.4.1 Repetitive Short-circuit Test

To mimic short-circuit behavior in real applications, the phase-leg configuration used in power converters is also used in SC test as shown in Figure 3.18 [104]. There are two main types of SC faults that may occur in power converters- (a) hard switching fault (HSF) and (b) fault under load (FUL) [104]. A hard-switching fault occurs when the DUT blocks the bus voltage before SC while the complementary switch remains fully conducted. Hence, device's V_{ds} maintains consistently at bus voltage during HSF pulses, and only yields to dv/dt spike caused by short-current transients induced ringing. On the contrary, FUL occurs when DUT conducts load current within Ohmic region and remarkable dv/dt and V_{ds} is expected owning to rapidly rising current when complementary switch encounters false turn-on.

As shown in Figure 3.18, a decoupling capacitor is connected close to the DUT in order to prevent a large dip in the DC bus voltage during the SC interval. A solid-state circuit breaker (SSCB) is also implemented for circuit protection. To mimic real SC event in power converters, the upper main switch is kept at blocking state and the SC power loop is formed by the DUT, SSCB and short circuit inductance in SC test. Therefore, the SSCB used should be able to withstand repetitive SC pulses without failing. The DUT is subjected to repetitive SC pulses till its EOL. Further, since SSCB and DUT are serially connected, SSCB with a high saturation current should be selected. This ensures that the voltage drop across SSCB is low and the full bus voltage is applied to the DUT during SC pulses. A 100kOhm resistor is used to increase RC time constant and prevent over-shoot caused by capacitor charge transients.

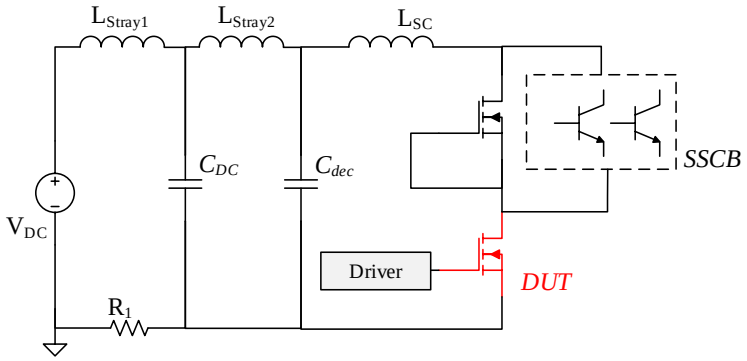


Figure 3.18. Typical short circuit reliability test circuit for SiC MOSFET [103].

In repetitive SC tests, a large amount of energy is dissipated during each SC pulse. Therefore, sufficient time delay is necessary between the SC pulses to prevent device thermal runaway. Typically, multiple seconds of blanking time is ideal [104]. The applied SC pulse length and energy is critical and different testing configurations may result in different degradation types. Figure 3.19 illustrates V_{th} degradation trend under 600V SC pulses [105]. It is observed that at

relatively longer pulses, V_{th} exhibits increasing trend whereas it decreases when the pulse periods are shorter (0.8μs). During repetitive SC tests, both HCI and V_{th} shift caused by gate bias under high temperature are the expected aging mechanisms. It is verified in [106] that high impact ionization takes place at SiC/SiO_2 interface above channel region. Therefore, when SC pulses are applied, generated E-field induces SiO_2 aging and high current causes impact ionization. Long pulses applied at high temperature, accelerate TDDB and BTI mechanisms, whereas HCI is mitigated due to its negative temperature dependent feature [105].

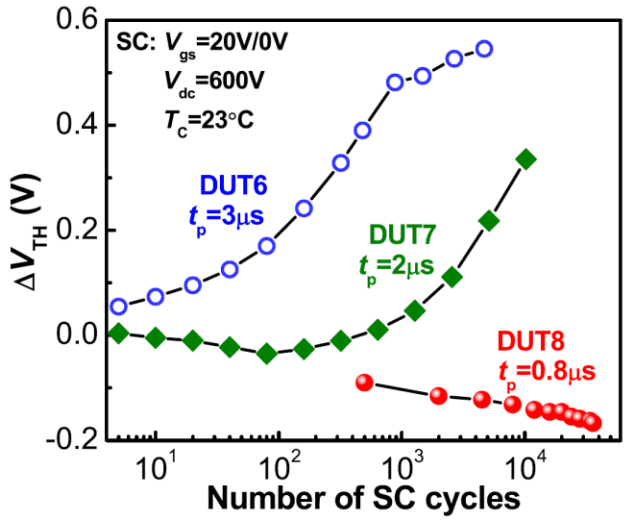


Figure 3.19. V_{th} degradation pattern at different SC pulses [105].

In repetitive SC test, SiC MOSFET results in high I_{gss} or I_{dss} at EOL. Unlike thermal runaway caused by extreme temperature in single-shot SC pulse test, the incremental I_{dss} in repetitive SC test is caused by accumulated oxide traps over repetitive SC cycles [107]. In addition to gate oxide degradation, package fatigue is also possible in repetitive SC test including bond-wire liftoff and surface reconstruction. Moreover, in addition to degradation caused by CTE mismatch within the device package including bond-wire and solder attachment, gate dielectric is also prone to failure

with cracks contributed by the extreme temperature. Therefore, repetitive SC tests are crucial for both die and package ruggedness under surge current conductions.

3.4.2 Unclamped Inductive Switching (UIS) Test

Parasitics such as package stray inductance cannot be fully avoided in converter designs. Due to fast switching transients, SiC MOSFETs are subjected to large voltage ringing during turn-off. Furthermore, unexpected electric shocks also cause large voltage spikes across the device. To analyze over voltage robustness, repetitive UIS test or avalanche test are widely employed. In UIS test, certain amount of load current is forced to flow through the device and trigger its avalanche mode. The three types of typical UIS test circuits are shown in Figure 3.20 [108]-[110]. In Figure 3.20 (a), a load inductor is located in between the DUT and DC voltage supply. When a gate pulse is applied to the DUT, current builds up through load inductor. However, when the DUT is turned off, it is forced into avalanche mode since the inductor current has no free-wheeling path to flow through.

Waveform across the DUT's terminals during UIS is shown in Figure 3.21 [110]. As depicted, in UIS tests, the DUT is stressed during both on-state and off-states. During the on-state, positive gate bias is applied for current conduction. As a result, gate oxide degradation is triggered by HEF under elevated temperature. During off-state, DUT's operates in avalanche mode generating extreme energy and therefore experiences significant electro-thermal stress. By capturing the device drain-source voltage and drain current waveforms during UIS, avalanche energy can be calculated to evaluate devices over voltage robustness. Since avalanche voltage is temperature dependent and the load current is not consistent during UIS, V_{ds} and I_d waveform need to be

integrated to obtain the value of avalanche energy [111]. However, it introduces computational complexity due to the non-linearity of V_{BD}.

To simplify the avalanche energy calculation, the test setup shown in Figure 3.20 (b) is proposed. Specifically, a parallel diode is connected across the load inductor and DUT. During avalanche interval, the main switch is turned off and bus voltage is isolated from avalanche power loop. In this way, avalanche energy can be simply obtained by calculating accumulated energy within load inductance. Moreover, using the circuit depicted in Figure 3.20 (b), a higher bus voltage can be used to build up the avalanche current within a short time thus reducing the electro-thermal stress on the gate oxide. Therefore, degradations in this UIS test are mostly due to avalanche events instead of positive gate bias applied in current accumulation.

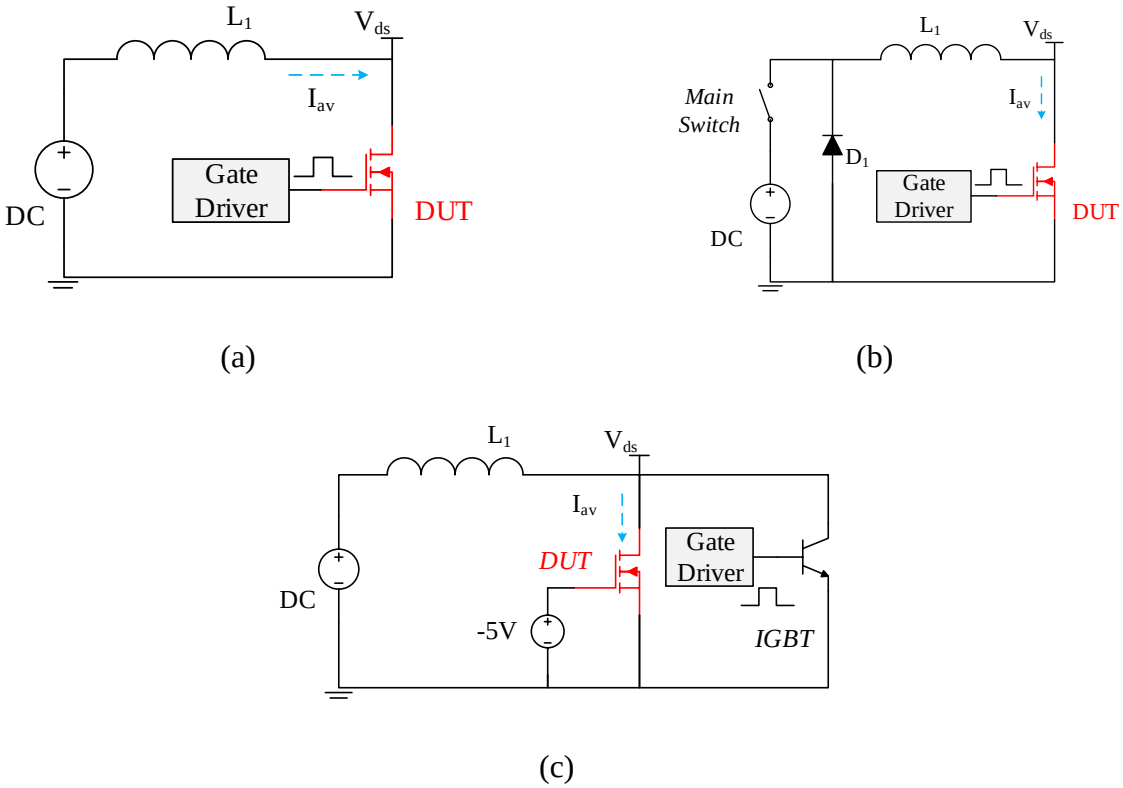


Figure 3.20. Repetitive avalanche test circuits for SiC MOSFETs [108]-[110].

An additional high voltage IGBT is deployed in UIS circuit shown in Figure 3.20 (c). The IGBT has a higher blocking voltage than the DUT so that the DUT can be forced into avalanche conduction at full inductor current. The IGBT is used to build up the avalanche current without any heat dissipation in the DUT. Therefore, in this test setup, the only stress is generated during off-state avalanche event other than the gate bias stress during on-state.

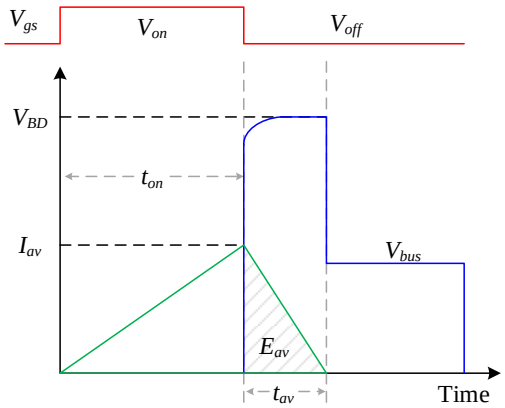


Figure 3.21. V_{ds} and I_d waveform during UIS test.

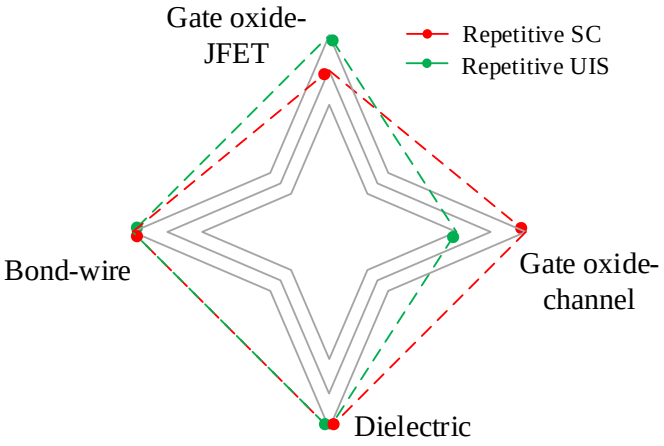


Figure 3.22. Locations prone to degradation in surge power tests

Unlike repetitive SC test, degradation in UIS test takes place at SiC/SiO2 interface above JFET region instead of channel region [112]. Highest current density is expected through internal PiN

diode while only small amount flows through JFET region and channel. According to TCAD assisted analysis, severe impact ionization occurs within JFET region and device degradation is explained by high HCI rate due to the over-voltage V_{ds} during avalanche [112]. As a result, V_{th} shows a decreasing trend over device's lifetime [113]. Moreover, degradation is also reported at the corner of gate dielectric layer because of the severe thermal-mechanical stress generated [113]. Furthermore, the applied repetitive temperature swings also cause package degradation in the DUT. Bond-wire liftoff and surface fatigue is also expected in repetitive UIS tests [114].

3.5 Proposed Active Channel Gate Bias (ACGB) Test

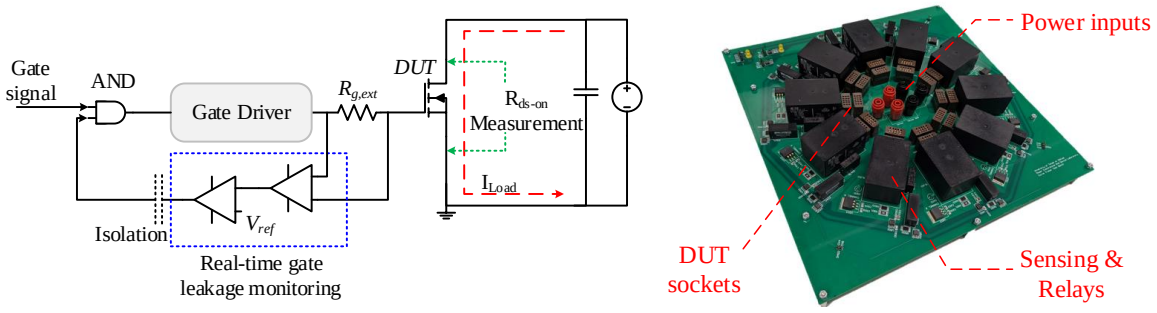
The schematic of the proposed active channel gate bias (ACGB) test is shown in Figure 3.23 (a). Compared to HEF test, DUT channel is conducted under certain amount of load current. As depicted, the voltage drops across $R_{g,ext}$ is monitored in real-time during accelerated aging. Once the measured I_{gss} exhibit rapid increment (>1mA), gate signal is pulled down and DUT lifetime is recorded. The test setup is shown in Figure 3.23 (b). This setup enables both 3-pin and 4-pin device's aging in large scale.

Unlike HEF test, a temperature mismatch between junction to case is expected in ACGB test due to device's conductive power dissipation. Hence, accurate real-time T_j sensing is needed to determine test condition. Another challenge during ACGB test is to maintain DUTs' aging conditions consistent over the whole test procedure including gate bias, temperature, and load current. Both issues are discussed and verified as follow.

1) Accurate Tj Sensing

Since directly decapsulating the device mold compound is costly and may affect the thermal conductivity of device, temperature sensitive electric parameter (TSEP) is preferred in proposed

ACGB test to measure T_j during the test online. Even though TSEPs such as V_{th}, $R_{ds\text{-}on}$ can be used to measure T_j, studies have shown that these parameters are also aging dependent [79]. Considering the load current applied during the test, DUTs' $R_{ds\text{-}on}$ are characterized at different V_{gs} in automated curve tracer over temperature before and after HEF stress in Figure 3.24.



(a) (b)

Figure 3.23. (a) Schematic and (b) setup of proposed ACGB test

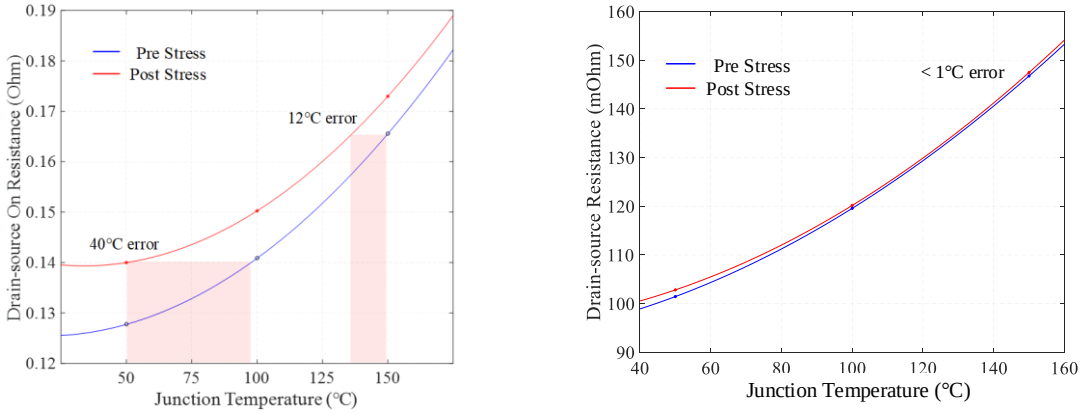
As observed, the shifted $R_{ds\text{-}on}$ caused by increased V_{th} results in more than 10°C temperature measurement error at DUT's rated temperature (150°C). However, if higher V_{gs} (30V) is used for channel conduction, the T_j measurement error can be significantly reduced to no more than 1°C. It can be explained by the correlation between device's channel resistance and threshold voltage in strong-inversion mode under positive gate bias, which is given as follow:

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{ox}(V_{gs} - V_{th})} \tag{1}$$

where L_{CH} is the channel length, Z stand for channel width, μ_{ni} stand for electron mobility and C_{ox} stands for gate oxide capacitance per unit area. Equation (1) reveals that when V_{gs} increases, the impact of a fixed value ΔV_{th} on R_{CH} is gradually decreased. Hence, it can be concluded that the

device channel resistance is slightly impacted by gate oxide degradation when higher gate bias is applied compared to normal V_{gs} in real converters.

Therefore, DUT's drain-source resistance (R_{ds}) at high gate bias is verified to be temperature dependent but aging independent. In the proposed ACGB test setup, it is employed for DUT's T_j monitoring to enable fair comparisons for both 3-pin and 4-pin DUTs.



(a) +15V (b) +30V

Figure 3.24. $R_{ds\text{-}on}$ shift before and after stress at various V_{gs}.

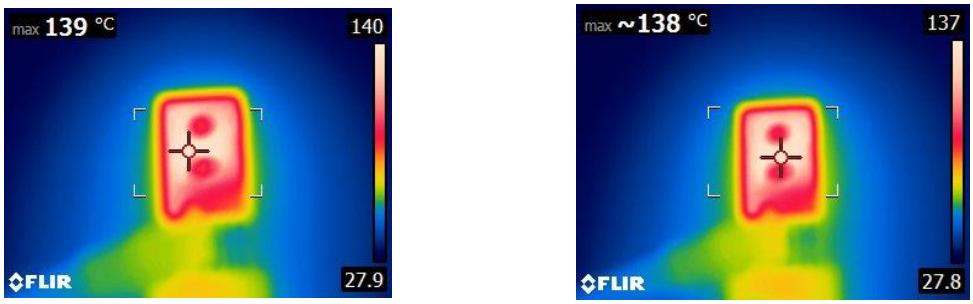
2) Aging Condition Consistency

Another advantage of the verified aging independent R_{ds} at strong E-field is keeping DUT's T_j consistent throughout the ACGB test. To verify both T_j sensing accuracy and aging condition consistency, a preliminary ACGB test is applied at 30V V_{gs} and 5A load current for 50 hours.

Prior to the test, one same part number SiC MOSFET sample is decapsulated by removing mold compound and exposing the die. It is characterized first over wide temperature range (25°C-150°C) using automated curve tracer and oven. A T_j calibration curve is obtained by collecting its R_{ds} values under 30V V_{gs} at various temperatures. During the preliminary ACGB test, its T_j is directly

measured by an IR camera and V_{ds} is measured by oscilloscope in real-time. As shown in Figure 3.25, over 50 hours of continuous aging, device temperature is proved to be consistent.

In ACGB test, DUTs are tightly attached to a hot plate for lifetime acceleration purpose and T_j difference caused by load current are compensated to enable their accelerated aging under the same temperature in both HEF and ACGB tests. Furthermore, to avoid T_j mismatch between samples due to manufacturing caused electrical parameter inconsistency, all DUTs are characterized before aging tests and outliers with different $R_{ds\text{-}on}$ compared to others are excluded from both HEF test and ACGB test.



(a) 0 hour (b) 50 hours

Figure 3.25. Direct T_j measurement at various states of ACGB test

CHAPTER 4

AGING ASSESSMENT AND EVALUATION[1]

4.1 Gate Oxide Aging

In this study, both HTGB and ACGB tests are applied to SiC MOSFETs. SiC MOSFET samples which are used owns 120mΩ $R_{ds\text{-}on}$ and 1kV voltage blocking capability.

4.1.1 Aging over HTGB Test

Figure 4.1 depicts the V_{th} shift patterns over different applied gate-source positive bias.

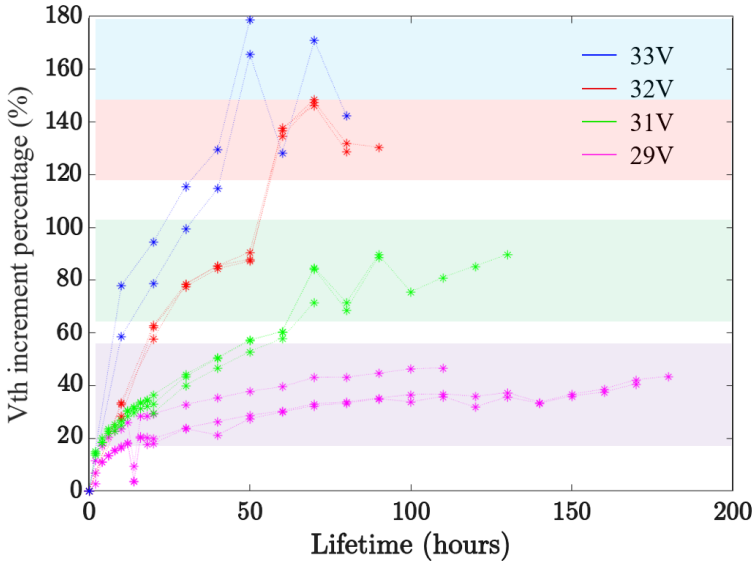


Figure 4.1. V_{th} shift pattern in HTGB test.

From the experimental results, positive threshold shifts are observed for positive gate bias in wide range. The root cause is supposed to be traps and defects trapping and SiO_2 TDDB as

[1] © 2018 IEEE Reprinted with permission from:
S. Pu, E. Ugur, F. Yang, C. Xu and B. Akin, "Thermally Triggered SiC MOSFET Aging Effect on Conducted EMI," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, pp. 51-55.

discussed in former chapters. Further, it is also observed that with higher applied V_{gs}, device instability effect is more severe.

4.1.2 Aging over ACGB test

It is observed that all DUTs in HEF test function well within 700 hours and the first failure case is observed after 760 hours. On the other hand, all devices under 30V V_{gs} ACGB test exhibits early gate oxide failure and reaches high gate leakage within 500 hours. The time-to-breakdown (t_{BD}) Weibull distribution of all DUTs are plotted in Figure 4.2, including 3-pin ACGB, 4-pin ACGB and HEF tests. It can be concluded that device degradations are largely accelerated by conducted load current under high gate bias.

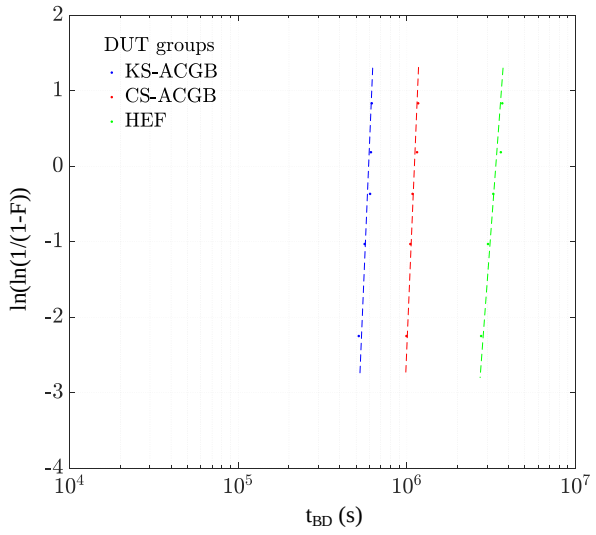
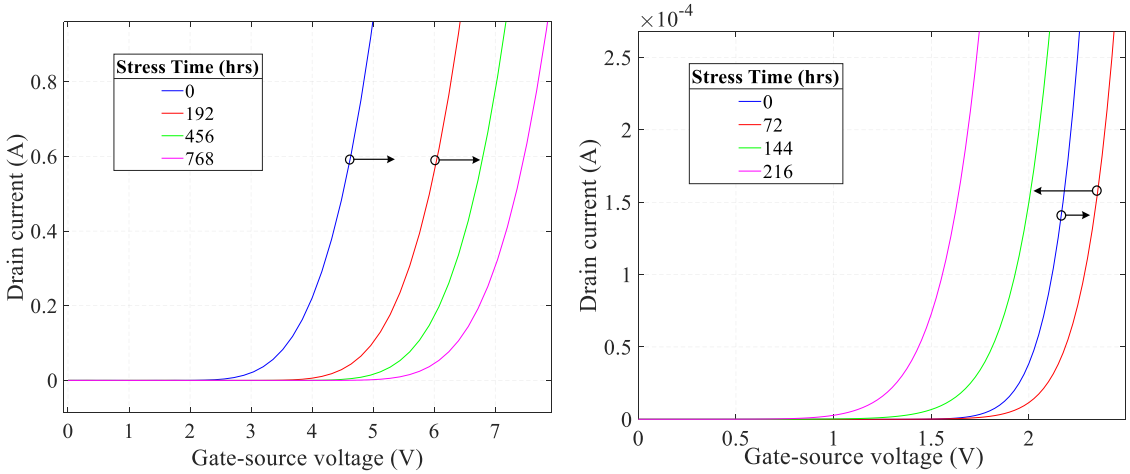


Figure 4.2. Weibull distribution of t_{BD} in both HEF and ACGB tests.

On the other hand, DUTs' end-of-lifetime failure modes after HEF and ACGB tests are quite different. In HEF test, both drain and gate leakage are observed to rise and device short-circuit is verified as the failure event. However, in ACGB test, most DUTs exhibit open-circuit fault with

high gate leakage whereas drain leakage current remains low. From application aspect, DUTs still maintain high voltage blocking capability whereas its gate cannot be effectively charged up. The root cause should be the voltage drop caused by channel resistance. Because of the device's R_{ds} and I_d, the E-field across SiO_2 layer is no longer evenly distributed compared with HEF test. Specifically, the E-field above device's JFET region is mitigated. Consequently, it ends up with a lower electro-thermal stress at gate-drain compared with gate-source side.

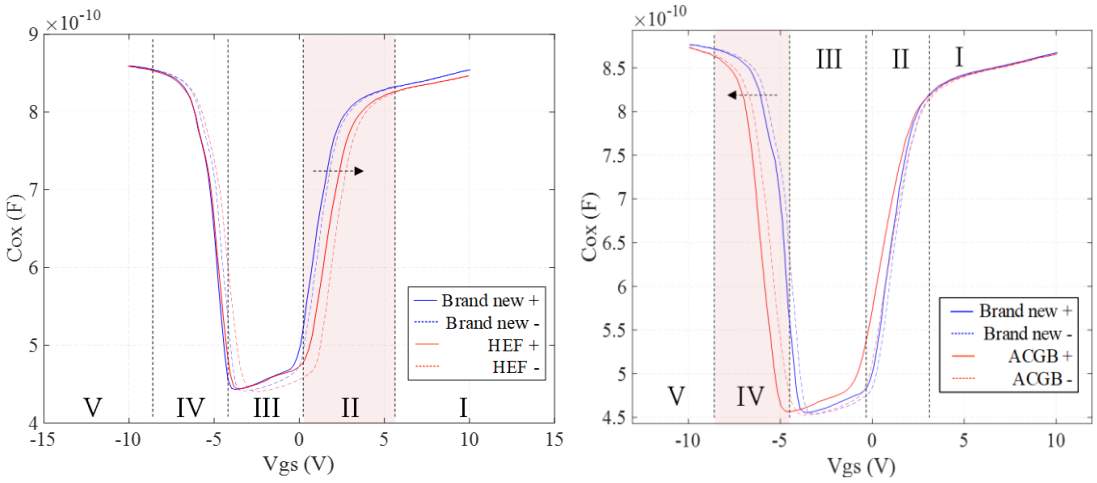


(a) HEF test (b) ACGB test

Figure 4.3. I_d-V_{gs} comparison of (a) HEF and (b) ACGB tests

It is also revealed in Figure 4.3 that in HEF test, device V_{th} increases due to gate oxide degradation with positive-BTI effect. While the additional active channel also introduces strong instability in device V_{th} while the applied stress eventually reduces DUT's V_{th} even below its brand-new state. For aging analysis and degradation mechanism discussion, device gate oxide capacitance (C_{ox}) measurement is obtained over gate bias in wide range. In this measurement, DUTs' drain-source electrodes are shorted, and a high frequency (1MHz) low amplitude AC voltage (100mV) is applied on the gate. The DC gate bias is swept in both positive and negative directions. Figure 4.4

(a) depicts C_{ox} measurement on DUT at healthy and post-HEF stress states, where the solid line represents a positive gate bias sweep, and the dashed line represents a negative sweep. Figure 4.4 (b) depicts C_{ox} measurement on DUT at healthy and post-ACGB stress states.



(a) HEF test (b) ACGB test

Figure 4.4. DUTs' C_{ox} measurement in HEF and ACGB tests.

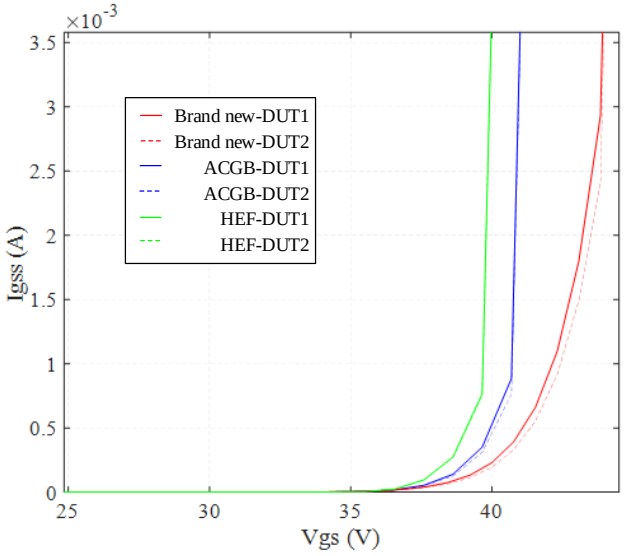


Figure 4.5. Destructive I_{gss} evaluation of brand new and aged samples

First, C_{ox} curve hysteresis effect is enlarged for both HEF and ACGB tests. This is a direct evidence of the interface trap density increase over aging patterns [115]. The increment of interface and near-interface trap is reported as a main contributor of V_{th} instability [116]. When electrons emitted into the interface/near interface, higher V_{gs} is needed to form the conductive channel. Moreover, the gate-source breakdown voltage should also increase because the applied V_{gs} not only need to provide enough charge for dielectric breakdown but also need to compensate the negatively charged traps [116]. However, a decrease in breakdown value is observed for both HEF and ACGB test in this test, as shown in Figure 4.5. Hence, this Q_{it} and Q_{nit} charging effect surely causes V_{th} positive shift in both tests, but it should not be the main contributor of device degradation with shorter lifetime in ACGB test.

Considering C_{ox} evaluation results in Figure 4.4, a positive shift in section II is observed for HEF test and implies negatively charged traps exists within gate oxide [115]. On the contrary, section IV in Figure 4.4 (b) shows an accumulation of positive charge emerges within gate oxide over ACGB test [117]. Since strong E-field (30V V_{gs}) is applied in ACGB test, Fowler-Nordheim (F-N) tunneling current is expected to dominate gate-oxide current flow instead of trap assisted tunneling. Therefore, a possible aging mechanism can be concluded for devices which are operated in high bias with active channel. Specifically, the F-N tunneling which is exaggerated by high gate bias enables electrons trapped at interface/near-interface to tunnel through the gate oxide under strong E-field. While the current flows through the gate-source, electrons within the oxide layer are fully extracted and leave traps and defects in acceptor type, results in device's stronger V_{th} instability and accelerated gate oxide lifetime.

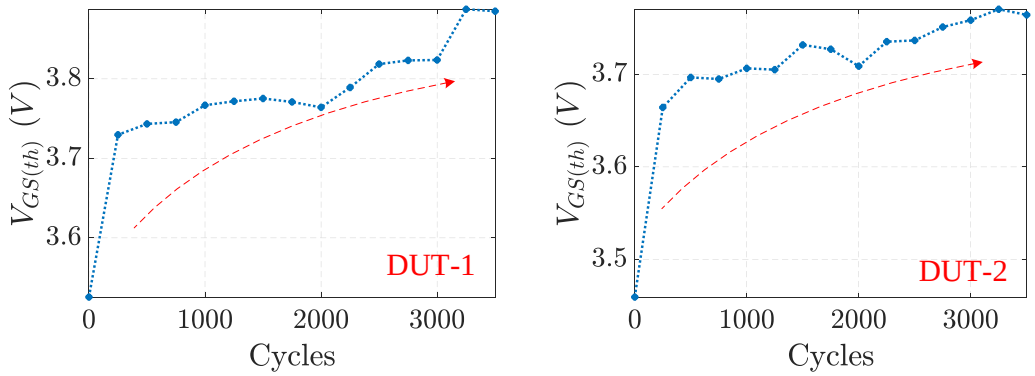
4.2 Degradation Pattern over Power Cycling

In this study, DC power cycling test is conducted to the DUTs. Other than package degradation, die related degradation is also triggered due to the V_{gs} and generated elevated temperature.

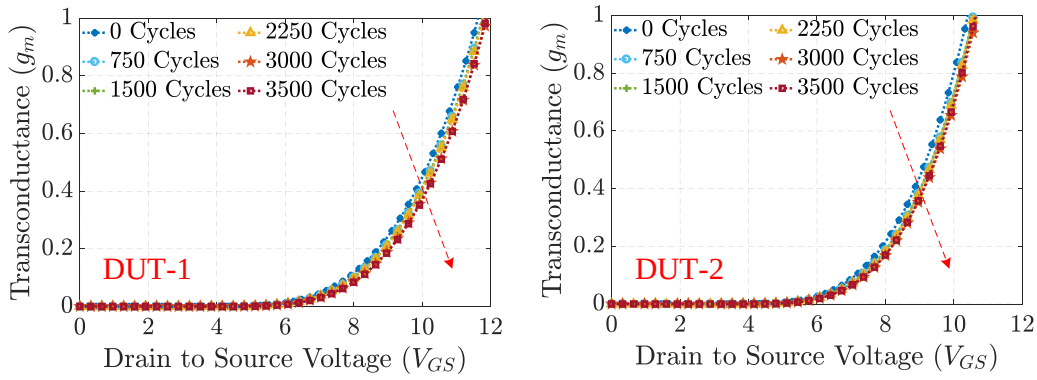
4.2.1 Static Electrical Parametric Shift

1) Threshold Voltage

In this study, the minimum gate-source voltage necessary to conduct 250µA drain current (I_d) is defined as the threshold voltage. Over the aging, the V_{th} change is depicted in Figure 4.6 (a).



(a)



(b)

Figure 4.6. (a) Threshold voltage and (b) transconductance shift over aging

A positive shift in V_{th} is observed and it increases exponentially due to degradation. DUTs' V_{th} shows an increase around 0.4V throughout aging. The reason for this phenomenon is the near interface charge trapping at SiC/SiO_2 interface. Under high junction temperature, tunneling mechanisms like Fowler-Nordheim tunneling current cause the electron trapped at the near interface defects. This causes V_{th} to rise and the channel electron mobility to decrease gradually over the aging process.

2) Transconductance

Another parameter which could be affected by near interface charge trapping related gate oxide degradation is the device transconductance (g_m). Considering the device structure, the relationship between g_m and V_{th} can be described as follow:

$$g_m = \frac{Z\mu_{ni}}{L_{CH}}(V_g - V_{th}) \tag{4.1}$$

where L_{CH} is the channel length, Z is the channel width, μ_{ni} is the inversion layer electrons mobility and C_{ox} is gate oxide capacitance. Hence, theoretically, an increase in V_{th} can result in a decrease in transconductance. Moreover, from equation (4.1), electron mobility is another impact factor for g_m changes over aging. The trapped charges in gate oxide may capture carriers in the conduction channel, decreasing electron mobility and reducing g_m consequently. Figure 4.6 (a) shows experimentally obtained g_m variation at different aging cycles. It is observed that g_m decreases due to device degradation which matches the theoretical analysis result.

3) $R_{ds\text{-}sat}$

Saturation regions drain-source resistance ($R_{ds,sat}$) is characterized over aging and its suitability as a precursor for gate oxide degradation monitoring is studied. The underlying mechanisms behind

the variation of $R_{ds,sat}$ over aging are explained through understanding the effect of aging on V_{th} characteristics. This can be verified from the characterization of V_{th} of the aged devices.

Regarding the channel resistance equation, it is evident that the increase in V_{th} due to device degradation leads to higher channel resistance for a fixed V_{gs}. This is because the formation of the conduction channel is weakened by device aging effect. It is also true for $R_{ds,sat}$ which is expected to increase throughout aging. Hence, with applied electro-thermal stresses, the device drain current is expected to be negatively affected for a fixed positive gate bias. Therefore, $R_{ds,sat}$ change with aging is effectively an indirect indicator of V_{th} drift and hence an effective precursor for gate oxide degradation monitoring. Also, since $R_{ds,sat}$ is several orders of magnitude higher in value than package resistances like lead resistance, bond-wire resistance, solder resistance, etc, use of $R_{ds,sat}$ as a precursor allows isolation of gate oxide degradation monitoring from package degradation which leads to rise in package related resistances.

4) $R_{ds\text{-}on}$

When the device is fully on and conducting within ohmic region, its drain-source resistance is much lower than $R_{ds,sat}$. In this region of operation, the channel resistance is comparable to package resistances. This implies any change in package resistances due to aging will result in a measurable change in the device $R_{ds\text{-}on}$. Therefore, to evaluate package related degradation, device needs to be fully conducted for $R_{ds\text{-}on}$ evaluation over its lifetime.

$R_{ds,on}$ change over aging for the aged SiC devices measured by curve tracer is depicted in Figure 4.7. Theoretically, it is expected that device V_{th} shift would also positively impact $R_{ds,on}$. This is verified in Figure 4.7 where the $R_{ds\text{-}on}$ of the devices increases gradually with aging. However, at 3500 cycles, a jump is observed in the value of $R_{ds\text{-}on}$ of all three devices. A potential root cause

for the observed increment in $R_{ds\text{-}on}$ could be package related degradation rather than gate oxide degradation itself. To verify the above possibility, DUT-1 is decapsulated and device failure analysis is performed by means of SEM. Small cracks are observed in the bond-wire due to applied thermal swings. Also, a partial bond-wire lift-off from die attachment can also be spotted. This explains the sudden rise in the $R_{ds\text{-}on}$ of the device due to a bond wire failing. Hence, Figure 4.7 points out that other than V_{th} induced $R_{ds\text{-}on}$ increase, a sudden positive $R_{ds\text{-}on}$ shift occurs due to the package degradation. Therefore, using $R_{ds\text{-}sat}$ and $R_{ds\text{-}on}$ together as precursors can enable comprehensive degradation monitoring where both die and package related degradation can be tracked over a device's lifetime.

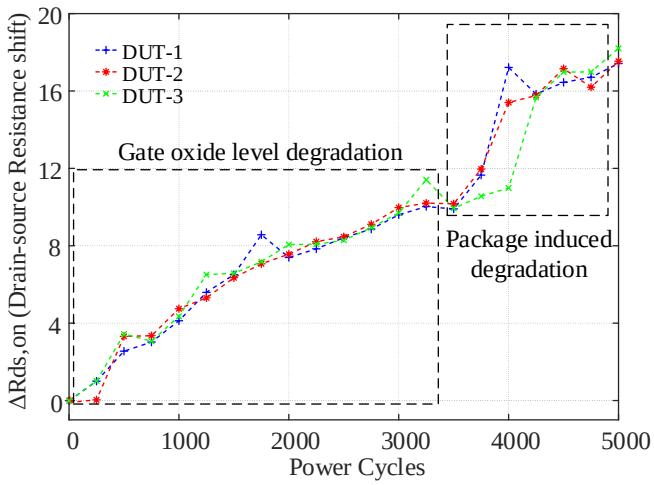


Figure 4.7. $R_{ds,on}$ shift over DUT lifetime

4.2.2 Switching Transient Shift

With the measurement result of device static parameters, DUT switching transient evaluation is conducted by means of double pulse test. For double pulse test rig specs, DC bus voltage is set at

500V, load current is set at 13A. An external 50Ω $R_{g\text{-}ext}$ is applied for the ease of analyzing. The switching transient waveform of DUT-1 is depicted in Figure 4.8.

From t_1 to t_2, gate voltage of the DUT rises to the threshold value and current starts to conduct through the channel. Before the drain current rises to the full load current at t_3, V_g continuously increases. At t_3, a voltage drop of V_g is observed which is caused by the common source coupling effect. Due to the large *di/dt* during turn-on, a voltage drop is induced on the device package stray inductance at the source terminal. For TO-247-3 packaged MOSFET, this stray inductance is shared by both gate loop and power loop. Hence, an extra voltage is induced from gate to source during current rising. After the load current remains stable at t_3-t_4, V_g falls back to the real Miller plateau value. Beyond t_4, the gate is gradually increased to 20V. In this study, the gate voltage change during time interval t_3-t_4 is investigated considering the device aging effects on Miller plateau voltage (V_{mp}) shift.

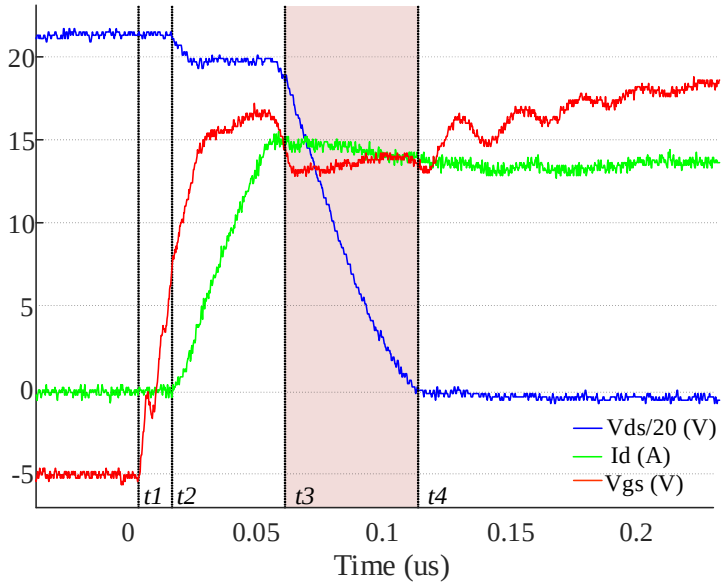


Figure 4.8. Hard-switching transient of DUT-1.

The measured V_g waveforms during turn-on transient after every 3000 power cycles are shown in Figure 4.9. Throughout degradation, a positive change of 0.5V in V_{mp} is observed. Such V_{mp} increment matches the analytical discussions on device static parameters shift over its lifetime. Hence, it can be claimed that both electric and thermal stresses are able to introduce defects to the gate oxide layer and cause V_{mp} increment.

To evaluate the SiC MOSFET switching transient under hard-switching cycles, a DPT is implemented. To obtain smooth transient waveforms with relatively longer time scale and without V_{ds} transient distortion for aging analysis, 20Ω $R_{g,ext}$ and 1nF C_{iss} are used. V_{gs}, I_d and V_{ds} of devices are measured during turn-on transients over aging as illustrated in Figure 4.8. During turn-on, gate-source voltage rises to V_{th} at 20 ns. In this phase, nearly no change is observed in V_{gs} slew rate and turn-on delay time. This small variation matches with the analytical model analysis implying small amount of turn-on delay increase after aging even with large $R_{g,ext}$.

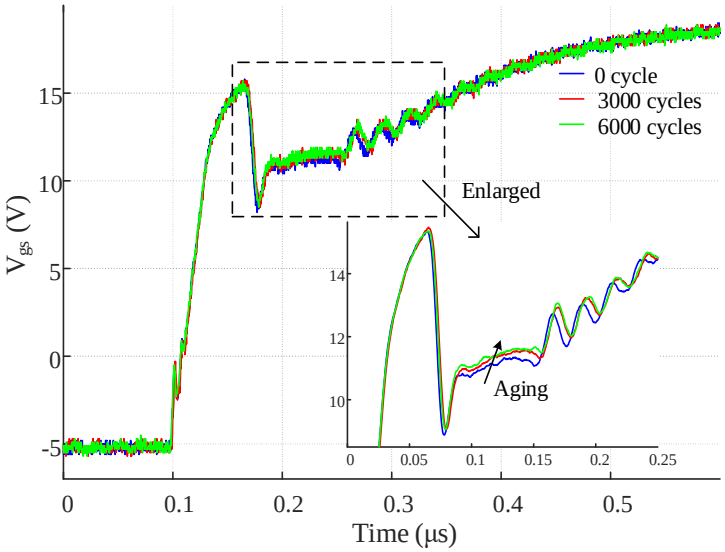


Figure 4.9. Thermally triggered V_{mp} increasing of SiC MOSFET.

During the current rise period, a negative di/dt is observed throughout device aging as shown in Figure 4.10 (b). The variation of V_{gs} during the current rise time interval is shown from 0.02μs to 0.08μs. The figure indicates that the rise of V_{gs} does not vary with aging. Therefore, it can be concluded that a lower g_m causes lower di/dt slope and longer current rise time. This derivation matches with the experimental waveforms in Figure 4.10. From the I_d waveform, the current rise time increases by 1 ns after aging. An increase of 5 ns and 8 ns in the voltage falling time is observed when the device is aged to 1500 cycles and 3000 cycles, respectively. The experimental result is consistent with the parametric measurement results and analytical model-based discussions.

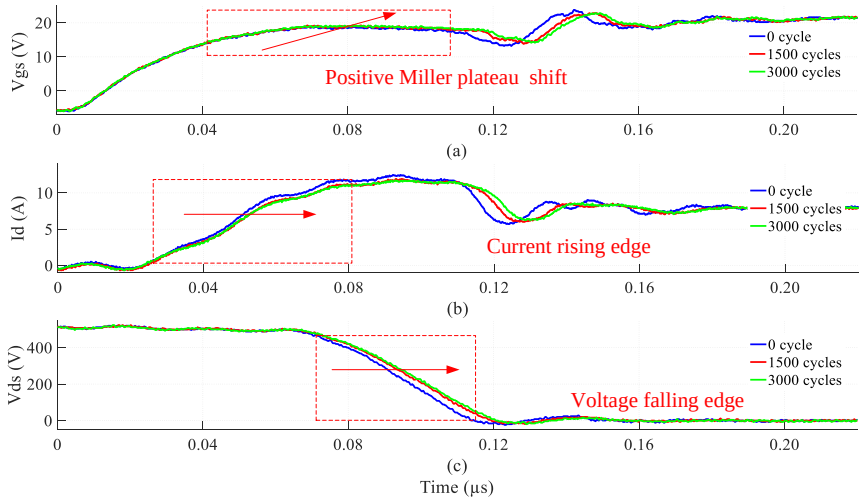


Figure 4.10. Turn-on transients at different device health conditions.

4.2.3 Aging Impact on System Performance-Conductive Noise

1) Analytical Analysis

For high frequency noise propagation, two conduction modes are defined as common mode (CM) and differential mode (DM). Figure 4.11 depicts the noise propagation paths of both modes and

shows EMI evaluation test bench setup with line impedance stabilization networks (LISN). For EMI noise voltage measurement, voltage probes are used in both phase and neutral line LISNs. After time domain signal processing, both CM and DM noises are converted into frequency domain signals according to the algorithmic definition.

In a boost PFC converter with grounded heat-sink, the parasitic capacitance formed by the insulation between SiC MOSFET drain side plate and heat-sink provides a conduction path for CM noise. The CM noise propagation path is shown in Figure 4.12 (a). In the conduction path, LISN network in both phase and neutral power lines has a stable 25Ω impedance by parallel connected. C_i is the insulation parasitic capacitance of the thermal insulation. The switching behavior of SiC MOSFET with high dv/dt introduces noise current to the grounded heat- sink and forms the CM noise source in Figure 4.12 (a).

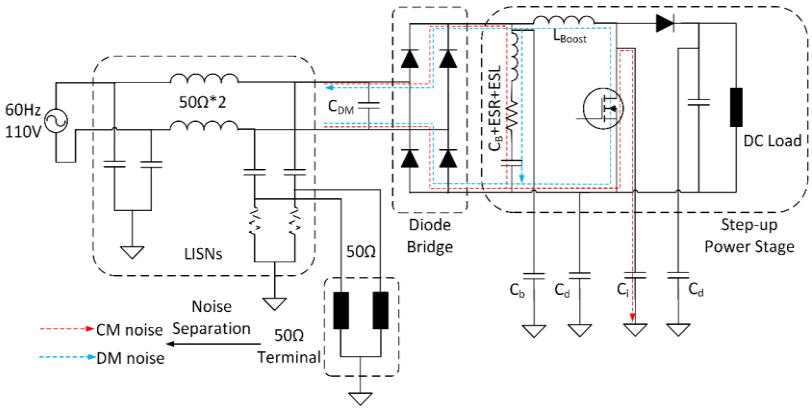


Figure 4.11. Noise conduction path and measurement for CCM Boost PFC.

At lower frequency range, such square wave of V_{ds} can be converted to frequency domain peaks. The common mode noise peaks are related to the k_{th} harmonic of the V_{ds} signal in this range which can be expressed as [118]:

$$V_{DS\_k} = \frac{2V_{out}}{k\pi}\left|sin\left[\sqrt{2}k\pi V_{in}|sin\omega t|/V_{out}\right]\right| \quad (4.2)$$

Where V_{ds_k} is the kth harmonic of drain to source voltage of SiC MOSFET, V_{in} is the converter input voltage and V_{out} is the converter output DC voltage.

Hence, at low frequencies, it is expected that V_{ds} spectra does not depicts too much difference. At higher frequencies, switching transient impacts the CM noise since V_{ds} waveform is not square wave but includes overshoot and ringing. Hence, according to the switching transient analysis above, a low dv/dt during turn on after degradation reduces high frequency noise in conducted EMI.

(a) CM (b) DM

Figure 4.12. Equivalent circuit models of (a) CM and (b) DM noise propagation path.

For CCM boost PFC, the conduction path for DM noise coupling is mainly introduced by the boost inductor. High frequency noise propagates to power line due to the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the bulk capacitor. The DM noise propagation path is shown in Figure 4.12 (b). In DM noise propagation path, LISNs are series connected with a 100Ω impedance and C_B is the balancing capacitor after the diode bridge. SiC MOSFET V_{ds} waveform causes current ripple in the boost inductor. This ripple current is the noise generating current source in DM noise propagation model. Hence, EMI noise peaks are generated at higher order harmonics under 1Mhz frequency range. During operation, this ripple current value is dependent on switching frequency and duty cycle can be calculated as:

$$\Delta I_r = {\sqrt{2}V_{in}|sin\omega t|}\Big/{L_b f_s} \tag{4.3}$$

For SiC MOSFET reliability study, switching frequency f_s is kept constant since such value is controlled by system controller and duty cycle is also determined by circuit control loop. For most EMI filter design, DM noise under 1MHz is a major concern since the noise propagation model path impedance towards the power line increases by frequency and the peak value of DM noise shows up at the first peak in the spectra.

2) Experimental Evaluation

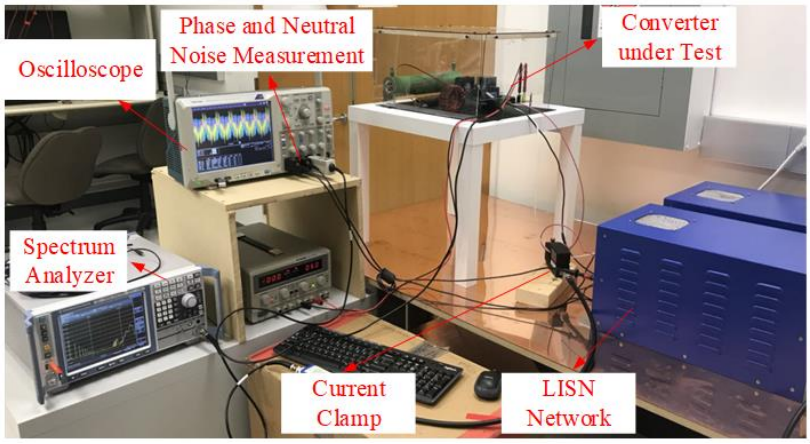


Figure 4.13. Conductive noise evaluation bench of CCM Boost PFC.

An 800W boost PFC converter is built for conducted EMI evaluation over SiC MOSFET aging and its EMI evaluation bench is shown in Figure 4.13. The converter operates in CCM mode and switching frequency is set to 100 kHz. Before starting the accelerated aging, DUTs are soldered to the PFC board and conducted EMI is measured through LISN networks and spectrum analyzer. During the aging process, DUTs are desoldered from PFC and plugged into the accelerated aging bench for power cycling. After each 1500 aging cycles, device electrical parameters are measured, and double pulse test is applied for switching transient evaluation. Subsequently, DUT is

resoldered to the PFC for EMI test. The noise measurement bench impedance is kept constant for both CM and DM noise measurement with EMI testing standard. For CM noise propagation path, V_{ds} spectrum is measured as the common mode noise source in frequency domain from 150kHz to 50MHz. As shown in Figure 4.14, 5 dBμV decrement is observed near 30 MHz within Band B frequency range. According to switching transient evaluation result, this decrement at high frequency matches with the transition changes after device aging. Figure 4.15 shows the measured CM noise for healthy and aged devices. After the device degradation, the peak value in the noise spectra changes slightly. At high frequency range above 10MHz, 10 dBμV decrement is observed. In measured noise spectra, the black envelop curve represents the conducted EMI measurement at healthy state. After aging, the noise spectrum changes by small amount below 1MHz and decreases at high frequency range in between 10MHz to 30MHz.

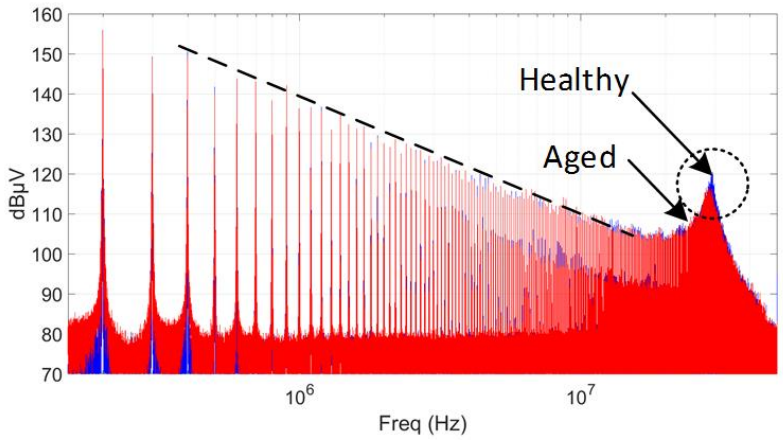


Figure 4.14. SiC MOSFET V_{ds} spectra before and after thermal stress.

To analyze DM noise changes after aging, the boost inductor current is measured in frequency domain, and Figure 4.16 depicts the inductor current spectrum. At the same frequency where V_{ds} shows decreasing trend as shown in Figure 4.14, a 5dBμA decrement is observed in inductor

current spectra at 30MHz. This decrease matches with the switching transient changes since lower switching speed results in less overshoot and ringing at high frequency range.

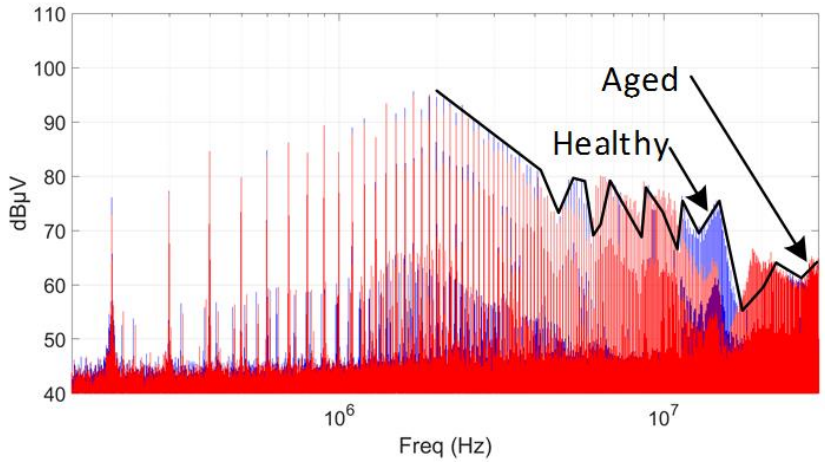


Figure 4.15. CM noise spectra before and after aging.

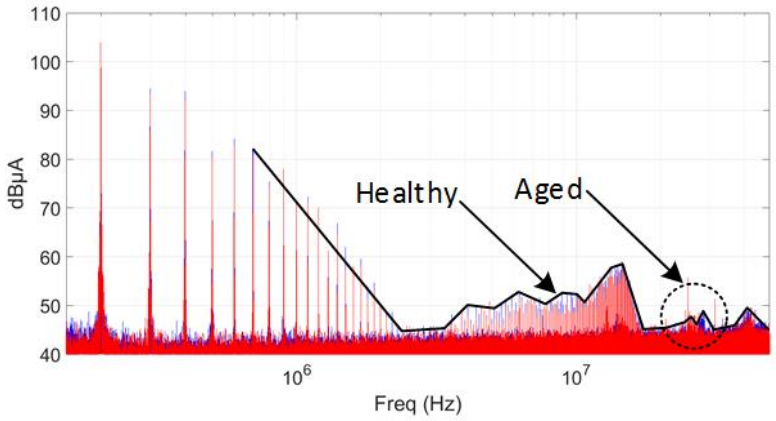
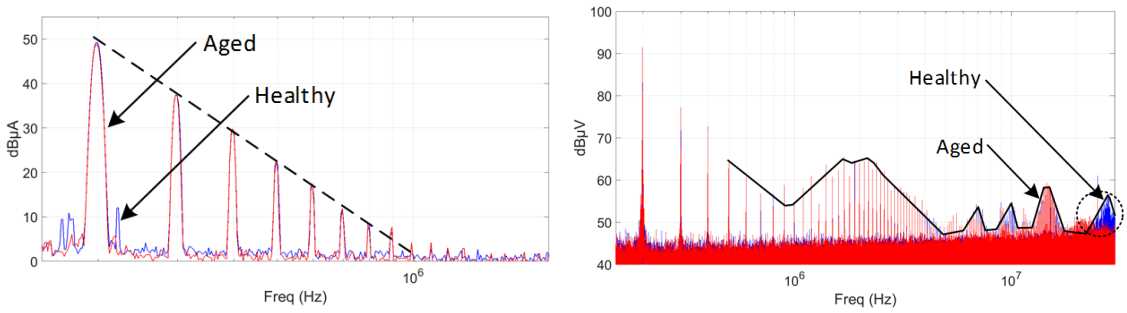


Figure 4.16. Boost inductor current ripple spectra before and after thermal stress.

For DM noise measurement aspect, low frequency range (below 1 MHz) DM current reading is shown in Figure 4.17 (a). Peak measurement shows only small decrease after the device is thermally stressed. Higher order harmonic peak measurement is consistent with the discussions regarding DM noise propagation and matches with the inductor current spectrum. In Figure 4.17

(b), DM noise spectrum in Band B is plotted. At high frequency range where V_{ds} spectra shows decreasing trend, a 8dBμV DM noise decrement is observed as well. The envelope curve represents the DM noise peak values of healthy device. Such decrement happens near 30MHz which is consistent with the previous transient frequency discussions regarding V_{ds} and I_{LB} spectrums.



(a) Below 1MHz (b) Band B (150 kHz ~ 30 MHz)

Figure 4.17. DM noise spectra before and after aging in different frequency ranges.

4.3 Common-source vs. Kelvin-source

4.3.1 Gate Oxide Test

As discussed previously, DUT's gate bias caused E-field stress across SiO_2 layer is consistent throughout the HEF test. Since there is no load current flowing through DUTs, parasitic resistance caused by common source package is not expected to cause any voltage drop on chip gate-source. Therefore, it is expected that devices' gate oxide lifetime is not impacted by package design when channel is not conducted with any load current. Potentially, the existence of the Kelvin source may slightly influence the V_{gs} value because its bond-wire is much thinner compared with the source bonding in common source package. Since this resistance mismatch is small and gate leakage current is also neglectable, there is no lifetime difference observed in the experiment.

As previously discussed, DUTs are characterized over lifetime to evaluate degradation patterns with electrical parameter shifts. V_{th} as the most widely reported aging indicator is depicted in Figure 4.18 for both CS and KS samples. It is observed that the positive shift in V_{th} is equivalent for CS and KS DUTs. Also, DUT's total V_{th} increment throughout aging also matches each other. As depicted in Figure 4.2, unlike HEF test, the existence of Kelvin source greatly impacts device's consumable lifetime. In CS design, R_{cs} causes gate voltage drop on voltage applied on chip due to the applied high load current.

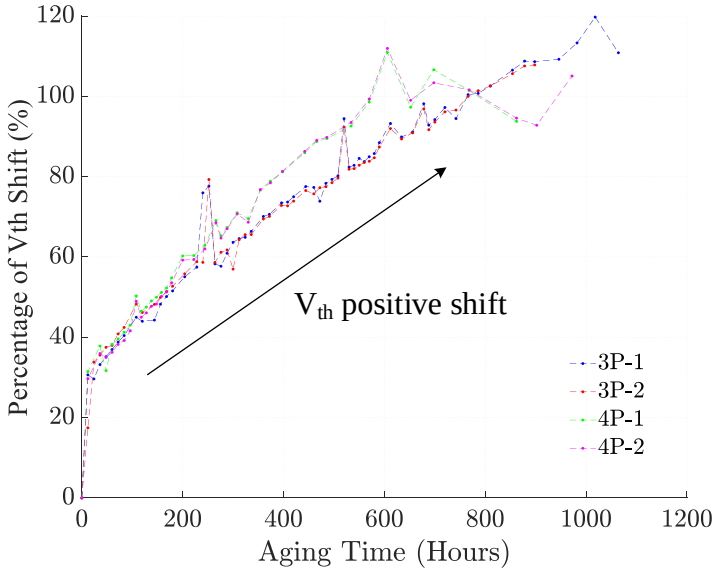


Figure 4.18. V_{th} shift pattern over HEF test.

In comparison, the gate-source voltage in 4-pin device is consistently applied without any mitigation. Hence, it can be concluded that in real converter applications, common-source package enhances SiC MOSFET's gate oxide reliability when device's operating condition is fixed. However, because of the mitigated gate bias, higher $R_{ds\text{-}on}$ is expected for 3-pin device during current conduction, and system efficiency and thermal management design is expected to be

influenced. Hence, system thermal design is more costly if CS device is expected to achieve the same temperature profile with KS devices. Therefore, Kelvin designed SiC MOSFET should not be claimed as "unreliable" considering all converter development aspects, including cost, design complexity, thermal management, etc.

4.3.2 Power Cycling Test

In this part, a constant ΔT_j mode power cycling is conducted to DUTs. Multiple lifetime models are available to estimate device's package lifetime. Among which, the LESIT (Leistungs Elektronik Systemtechnik und Informations Technologie) model is widely adopted with good lifetime estimation accuracy, in which device's ΔTj and average Tj are considered as main lifetime impact factors [48]. In this model, device's expected consumable power cycles are depicted as follow [47]:

$$N_f = \alpha \cdot (\Delta T_j)^{-m} \cdot e^{E_{aa}/(K \cdot T_{j-avg})} \tag{4.4}$$

Where N_f stands for consumable power cycles, and α, m, activation energy (E_{aa}) and Boltzmann constant (K) are constant parameters. In this test, both 3-pin and 4-pin DUTs' T_j are actively swept from 40°C to 180°C, and the load current during heat-up stage is kept consistent at 10A. Therefore, their expected package consumable lifetime is equal. It is verified in the power cycling test that 3-pin and 4-pin samples lost their functionality at approximate same amount of power cycles, and no significant impact from Kelvin-source is observed. To compare the degradation pattern between 3-pin and 4-pin DUTs, device characterization is conducted throughout the test.

As a direct aging indicator, $R_{ds\text{-}on}$ shift patterns of both DUT types are plotted in Figure 4.19. In comparison with 3-pin DUTs, 4-pin devices have much higher $R_{ds\text{-}on}$ shift over its lifetime.

However, both 3-pin and 4-pin DUTs still functions well when rapid $R_{ds\text{-}on}$ shift is observed at around 13k cycles. However, as suggested in industrial applications, 5% of $R_{ds\text{-}on}$ shift is normally employed as end-of-lifetime threshold [55]. Therefore, despite of the equivalent thermal-mechanical stress applied for both device types, 4-pin device is verified to be less reliable than 3-pin in respect of power cycling. The root cause of this aging pattern mismatch between 3-pin and 4-pin DUTs should be the positive-BTI effect introduced by the applied V_{gs} at high temperature.

To investigate aging mechanism difference, transfer characteristics (I_d-V_{gs}) is evaluated by automated curve tracer for both 3-pin and 4-pin DUTs in Figure 4.20. As observed, a much stronger instability is observed for 4-pin device whereas 3-pin device only exhibit 0.051V V_{gs} increment at 2A I_d. This experimental result implies that, because of the conductive load current induced voltage drop on common source resistance, the real voltage stress across the chip gate-source is expected to be higher for KS packaged SiC MOSFET. As a result, 4-pin DUTs show higher BTI effect than 3-pin devices and exhibit severer $R_{ds\text{-}on}$ shift.

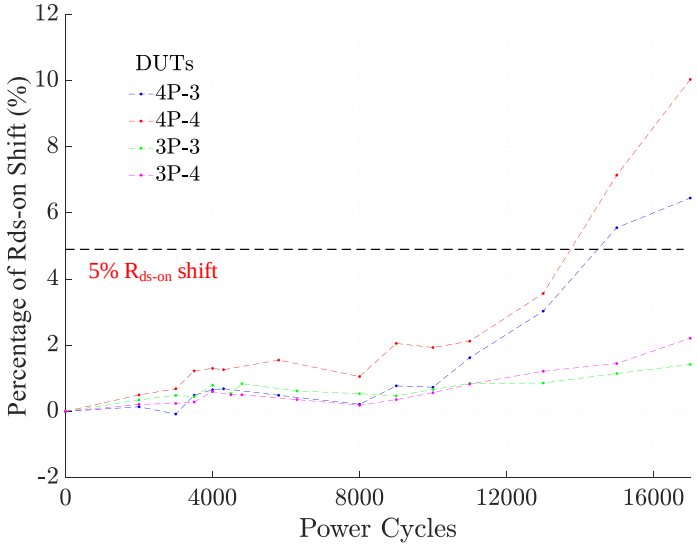
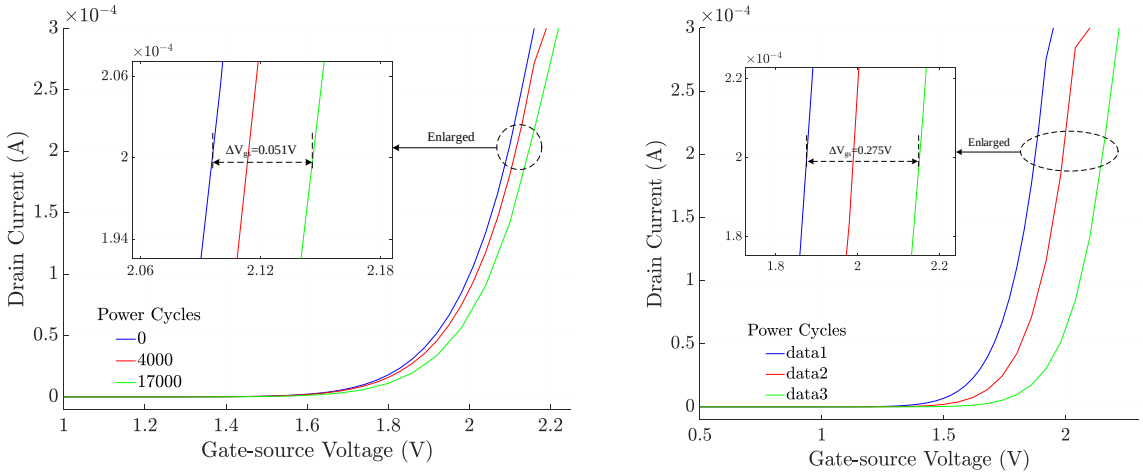


Figure 4.19. $R_{ds\text{-}on}$ shift over power cycling test.

Therefore, even though KS device is expected to own enhanced switching and conduction performance due to its optimized gate loop inductance and driving voltage, such refinement compared to CS devices may be mitigated in long term system operation. Because of its dramatic $R_{ds\text{-}on}$ increment caused by both package and gate oxide degradation, adequate T_j margin in converter thermal design phase should be considered.



(a) 3-pin (b) 4-pin

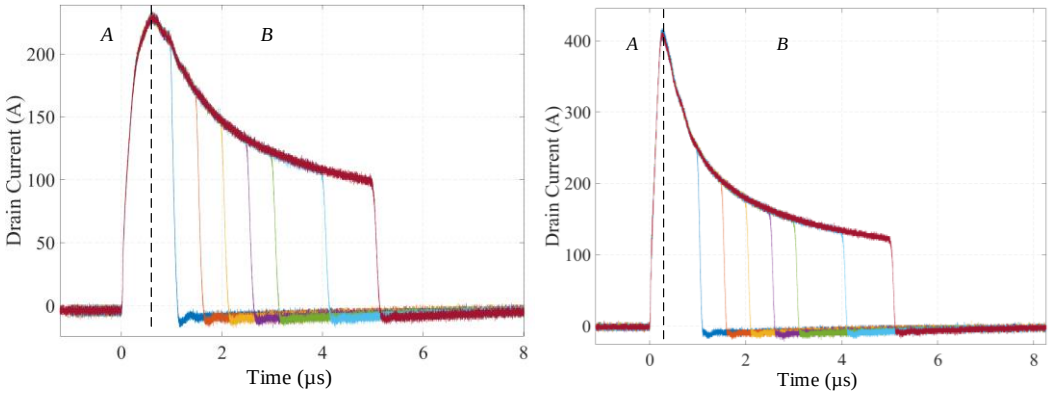
Figure 4.20. Transfer characteristics shift during power cycling test.

4.3.3 Short Circuit Test

The obtained SC pulses at room temperature are plotted in Figure 4.21. It is observed that the Kelvin packaged design has significant impact on di/dt during the current rising transient. For 3-pin DUT with common source, the real applied V_{gs} across the chip gate-source during the turn-on transient (0μs-0.25μs) is largely reduced because of the voltage drop generated on stray inductance L_{CS} and parasitic resistance R_{CS}. Therefore, a retardation on SC current rising can be observed in Figure 4.21 (a), Region *A*. Further, because of the much larger di/dt, the voltage drop generated

across power loop stray inductance is much higher for 4-pin DUT. As a result, a significant V_{ds} dip is observed which is shown in Figure 4.22.

Another critical difference is the saturation current in Region *B*. Because of the high current conduction, the real applied V_{gs} across chip gate-source in 3-pin DUT is expected to be lower than 4-pin. Because the employed CS and KS devices owns the same die technique and configuration, their channel resistance is the same. Therefore, in 4-pin device, higher current is needed to pinch-off its channel and saturation current is expected to be higher. This matches the experimental waveform which is shown in Figure 4.22. It is verified that SC power for 4-pin DUT is much higher than 3-pin DUT.



(a) 3-pin (b) 4-pin

Figure 4.21. Single shot short-circuits experimental pulses.

It is experimentally verified that 4-pin DUT fails at 7µs at 150°C while 3-pin DUT can survive more than 10µs. The failure analysis is conducted through decapsulation and scanning electron microscopy (SEM), which is shown in Figure 4.23. An obvious burn-through mark is observed at gate runner and causes device all three terminals' high leakage as failure mode. Hence, considering

the higher applied V_{gs} and short circuit power, KS device is verified to be much less rugged compared with CS devices.

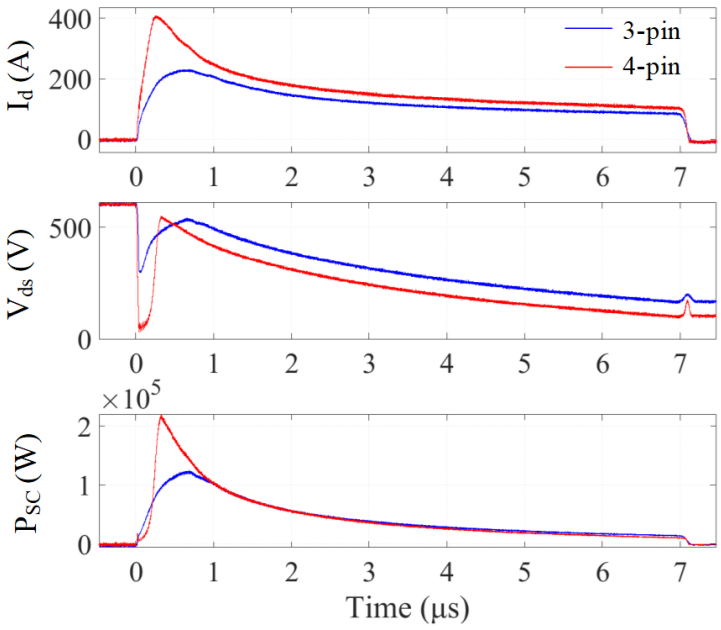


Figure 4.22. Subplot of I_d, V_{ds} and E_{sc} during short circuit pulse.

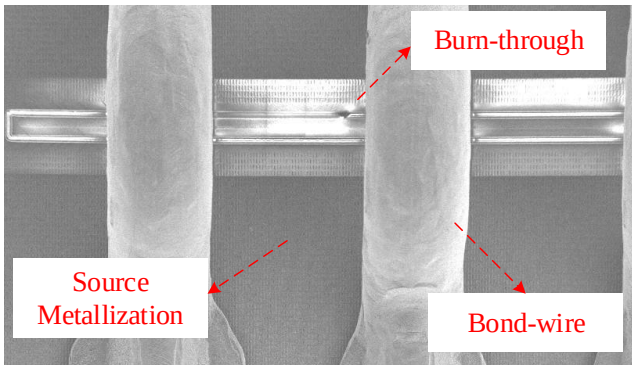


Figure 4.23. Failure analysis of 4-pin DUT under SC stress with SEM.

In respect of converter design, SSCB with faster triggering response is needed for KS devices. On the other hand, for SiC based system which requires strong short-circuit tolerance, CS packaged main switches are suggested.

CHAPTER 5

SWITCHING TRANSIENT BASED CONDITION MONITORING[2]

5.1 Miller Plateau Based Condition Monitoring

As an effective indicator for thermally triggered degradation, V_{mp} can be detected at system start-up to assess DUT state of health without junction temperature effect. Previously, in-situ aging detection circuit for IGBT has been proposed in [119] by means of measuring V_{mp} duration. However, comparing to Si based IGBT, SiC MOSFET owns a unique feature of non-flat Miller platform [120]. Using the existing detection circuit may result in false toggled alarm and unexpected system halt. On the other hand, due to SiC device's fast switching speed, the Miller platform duration in SiC MOSFETs is no more than 50ns. Therefore, a high bandwidth aging detection circuit need to be developed for SiC MOSFET.

In the proposed SiC MOSFET condition monitoring method, the device's V_{ds} signal is used to consistently detect the plateau voltage over aging. Specifically, 50% V_{ds} is selected to trigger gate-source voltage measurement during device turn-on transient. To accurately sense the V_g, a state-of-art sample and hold (S/H) chip with nanoseconds of data acquisition time is used to rapidly capture device's V_{mp} at turn-on.

The proposed aging detection circuit is depicted in Figure 5.1, including V_{mp} detection panel and DUT equivalent model. A resistive voltage divider is used to scale down both drain-source and

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S. Pu, E. Ugur, F. Yang and B. Akin, "In situ Degradation Monitoring of SiC MOSFET Based on Switching Transient Measurement," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5092-5100, June 2020.
S. Pu, F. Yang, E. Ugur, C. Xu and B. Akin, "SiC MOSFET Aging Detection Based on Miller Plateau Voltage Sensing," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1-6.

gate-source voltages to 5V. For V_{ds} signal, if the blocked bus voltage is very high at device off-state, an optional buffer can be applied to isolate the detection circuit input impedance from V_{ds} dividing resistors. The reference voltage (V_{ref}) is set below scaled down V_{ds} to trigger the sample and hold signal. Once scaled V_{ds} reaches V_{ref} during turn-on transient, DUT's V_g is fed to sample and hold (S/H) circuit and measured by system ADC module. Additionally, to validate aging detection functionality for both upper and lower switches, an analog isolator can be placed between the S/H amplifier and system DSP for upper switch monitoring.

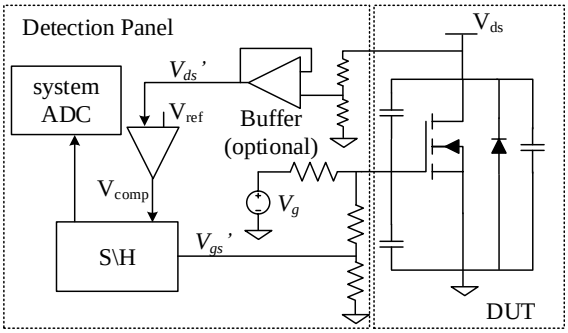


Figure 5.1. Aging detection circuit based on V_{mp} sensing.

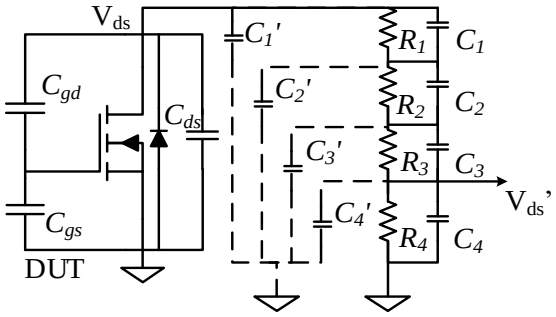


Figure 5.2. High frequency model of resistive V_{ds} divider

To achieve accurate V_{mp} sensing, a design guide is needed, fully considering possible impact factors which may induce measurement error.

1) Voltage Scaling Down

As shown in Figure 5.1, resistors are employed to scale down V_{gs} and V_{ds} under 5V. At static conduction and blocking states, device voltage level can be divided without any distortion. However, during switching transients, circuit parasitic parameters would largely impact detected signals' fidelity. The high frequency V_{ds} detection circuit model is depicted in Figure 5.2. Where R_1-R_4 stands for resistances used to divide V_{ds}, C_1-C_4 stands for equivalent parallel capacitances and C_1'-C_4' are device capacitance to the reference plane (DUT source voltage).

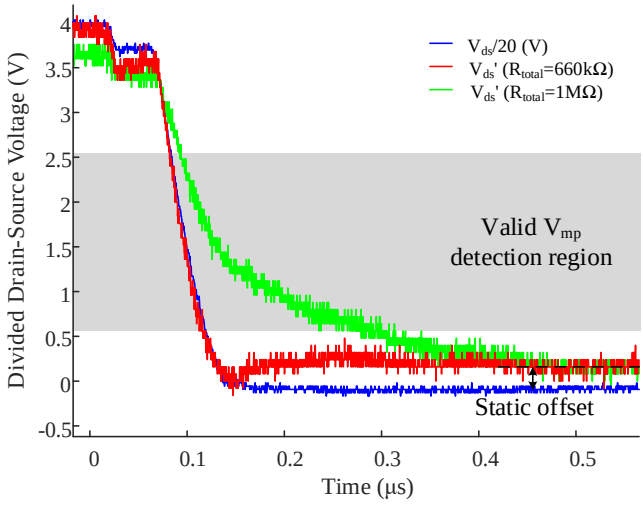


Figure 5.3. Detected V_{ds}' with different voltage divider resistance.

In this study, the resistance value of R_1-R_3 is the same to divide the high voltage at DUT blocking state. By connecting R_1-R_4 in series, the parasitic capacitance caused by resistor package is largely reduced. For PCB layout, the grounded polygon for R1-R_4 is suggested to be removed so that the parasitic capacitance of voltage divider can be further reduced. Furthermore, to optimize the RC charging circuit time constant of V_{ds}', R_1-R_4 need to be carefully selected. Within the boundary of rated power dissipation, the total resistance value R_{total} of R_1-R_4 needs to be as low as possible. In Figure 5.3, op-amp output voltages (V_{ds}') are plotted when different R_{total} applied. As observed,

R_{total} of 660kΩ is a wise option for V_{ds} sensing, without any turn-on transient distortion and signal delay. If 1MΩ R_{total} is selected, a significant delay in introduced in V_{ds} measurement, and can cause significant RC discharging time thus leading to inaccurate V_{mp} measurement. On the other hand, a DC offset of +0.1V can be observed after 0.4μs in Figure 5.3. Based on the load current and DUT $R_{ds\text{-}on}$ value measured by the curve tracer, such offset is mainly caused by device's on-state drain-source voltage drop when conducted. As a result, if a low V_{ref} is used to trigger V_{mp} sensing, a measurement error may occur due to a false triggered enable signal at both V_{ds} falling stage and device fully conducted state. Therefore, to keep the detected V_{ds}' undistorted, low R_{total} (660kΩ) is used in this study and V_{mp} is sensed when V_{ds} reaches near 50% of V_{bus}.

2) Detection Panel

For SiC MOSFET, its Miller plateau only lasts for tens of nanoseconds during turn-on. As tested, only 40ns duration is observed even with external R_g (50Ω) applied. Compared to the switching speed of SiC device, data acquisition speed of system ADC is much slower (80ns). Hence, to achieve fast V_{mp} sensing, a discrete high-speed sample and hold (S/H) amplifier is used.

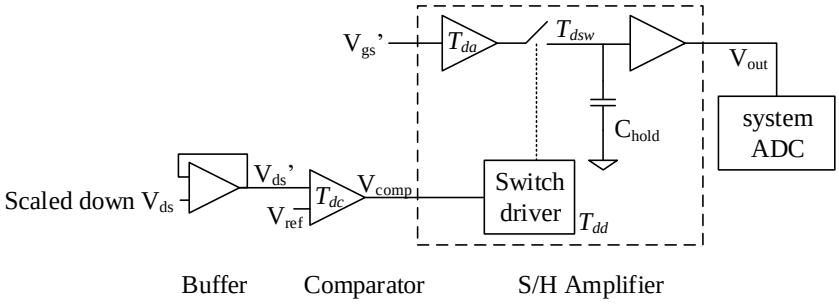


Figure 5.4. Signal delays in proposed V_{mp} detection circuit.

However, the state-of-art S/H IC AD783 with low data acquisition time still requires tens of nanosecond to charge up the output capacitance [121]. Regarding this concern, in proposed circuit,

the S/H amplifier continuously samples V_{gs}' start from the device off state. Hence, when DUT starts to enter saturation region during turn-on, the output capacitance of S/H amplifier is continuously charged. Once V_{ds} reaches V_{ref}, the S/H amplifier is toggled to hold mode. Beyond Miller plateau, the detected V_{mp} is hold by the amplifier and fed to system ADC for measurement. The detection circuit's signal delays are illustrated in Figure 5.4.

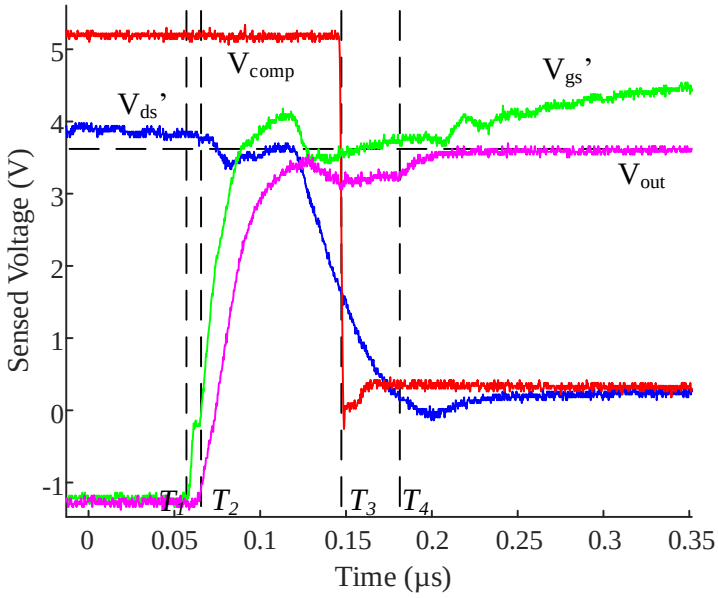


Figure 5.5. Detected signals in V_{mp} detection panel.

As observed in Figure 5.3, the output voltage of the buffer circuit (V_{ds}') perfectly matches the scaled down V_{ds} during DUT turn-on transient. Hence, the added buffer circuit introduce zero signal delay to V_{mp} measurement. As depicted in Figure 5.4, voltage comparator is expected to introduce a propagation delay of T_{dc} to V_{ds}' sensing. Further, S/H amplifier also retard the scaled down V_{gs} signal. Specifically, T_{da} stands for the analog signal delay, T_{dd} stands for switch driver delay and T_{dsw} stands for switch delay. Once the internal switch of S/H is turned off, the voltage

on C_{hold} is clamped at scaled down V_{mp} value (V_{mp}') The aperture delay of S/H amplifier can be expressed as [121]:

$$T_{aperture\_delay} = T_{dd} + T_{dsw} - T_{da} \quad (5.1)$$

In proposed aging detection circuit, total V_{mp} detection delay time (T_{delay}) can be calculated as follow:

$$T_{delay} = T_{dc} + T_{dd} + T_{dsw} - T_{da} \quad (5.2)$$

Therefore, to obtain accurate V_{mp} measurement, V_{ref} and S/H amplifier need to be carefully selected. In Figure 5.5, the switching waveforms of the device's V_{ds} (scaled down one after voltage divider) and V_{gs}, the comparator's output V_{comp}, and the measured V_{mp} (V_{out}) are plotted.

Specifically, V_{bus} is set at 400V, I_d is 12A and V_{ref} is set at 1.75V (toggles when V_{ds} reaches 190V). As shown in Figure 5.5, four intervals can be observed during V_{mp} measurement.

T_1-T_2: From T_1, DUT gate voltage starts to increase while V_{out} still remains 0V due to the positive T_{delay}.

T_2-T_3: The hold capacitor (C_{hold}) in S/H amplifier starts being charged, and V_{out} is tracking V_{gs}'. However, an obvious capacitor charging stage can be observed since the time delay between V_{gs}' and V_{out} gradually increases during this interval. Two factors are contributing to this charging delay, namely the C_{hold} in S/H amplifier and input capacitor (C_{probe}) of oscilloscope probe. Specifically, C_{hold} is around 2pF and C_{probe} is 3.9pF [121]. In comparison, C_{probe} is mainly causing such voltage sensing delay.

T_3-T_4: At T_3, V_{ds}' reaches V_{ref}. The comparator is toggled and trigger the S/H amplifier from sampling to hold mode. According to the V_{ds}' and V_{comp} waveform, no more than 2ns T_{dc} is observed. Within this interval, the S/H amplifier is switched to hold mode and a signal delay can

be observed due to $T_{aperture}$. During T_3-T_4, V_{out} shows slight increment, which means the amplifier is still trying to follow the Miller plateau. This is because even though the internal switch driver is triggered to off state at T_3, the internal switch still needs T_{dsw} to become fully blocked. Within this interval, C_{hold} is expected to be charged up to the mean value of the input voltage (V_{gs}'). The duration of T_3-T_4 is no more than 30ns, matches the delay time provided in datasheet.

Beyond T_4: Starting from T_4, a clean capacitor charging stage is observed. According to the S/H amplifier internal structure shown in Figure 5.4, it can be explained that the internal switch is fully blocked and C_{hold} is fixed at T_4. Hence, beyond this point, C_{hold} can be considered as a voltage source, directly charging up C_{probe}. As earlier discussed, the V_{mp}' detection bandwidth is limited by both C_{hold} and C_{probe}. At this stage, voltage on C_{hold} is fully stabilized and its voltage is charged up to the mean V_{gs}' voltage of T_3-T_4. This measurement result matches the theoretical transient analysis. It can be explained that if C_{hold} fails to capture the gate voltage during Miller plateau, then after T_4, the measured V_{out} has no chance to rise to V_{mp} because the internal switch of S/H has already been fully blocked. Therefore, during T_3-T_4, the C_{hold} is charged up to V_{mp}' and the observed V_{mp}' measurement bias is most likely caused by C_{probe}.

5.2 Turn-on Time Based Condition Monitoring

To measure nanosecond-level turn-on time delay, a high-resolution detection method is required. This is achieved by using high-resolution capture peripheral of C2000 MCUs. The high-resolution capture module (HRCAP) provides 300 ps resolution to detect falling and rising edges. By capturing the rising edge of V_{gs} and the falling edge of V_{ds}, the HRCAP module can measure the time interval between these two edges accurately [122].

A few interface circuits are evaluated to capture SiC MOSFET turn-on time to detect incipient faults and aging related degradations. For monitored voltage edges, the detection circuit downscales the switching pulses and generates voltage pulses with the same time length as device turn-on time without distortion. In this paper, the generated pulses are defined as “turn-on pulses”. The interface circuit shown in Figure 5.6 is developed for exact turn-on delay measurement.

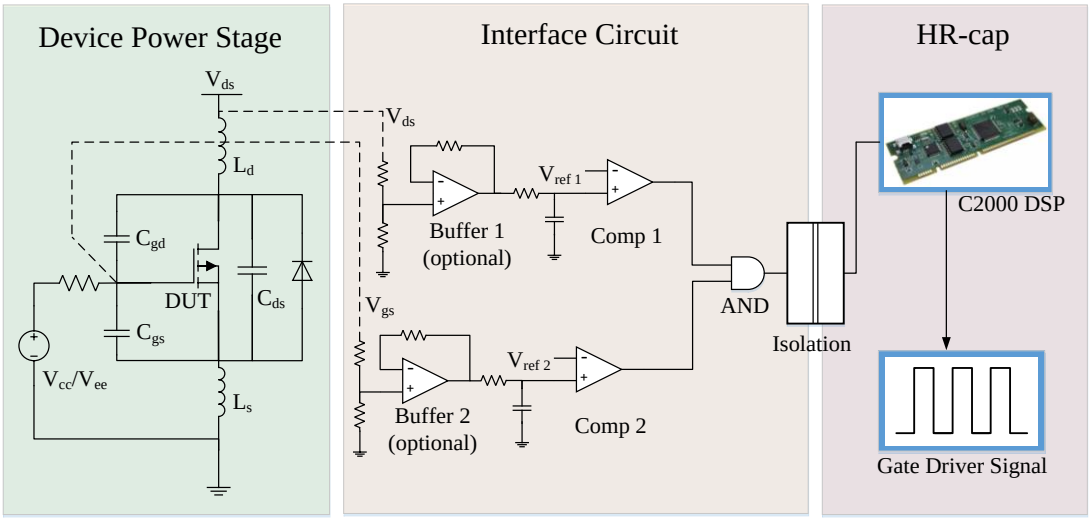
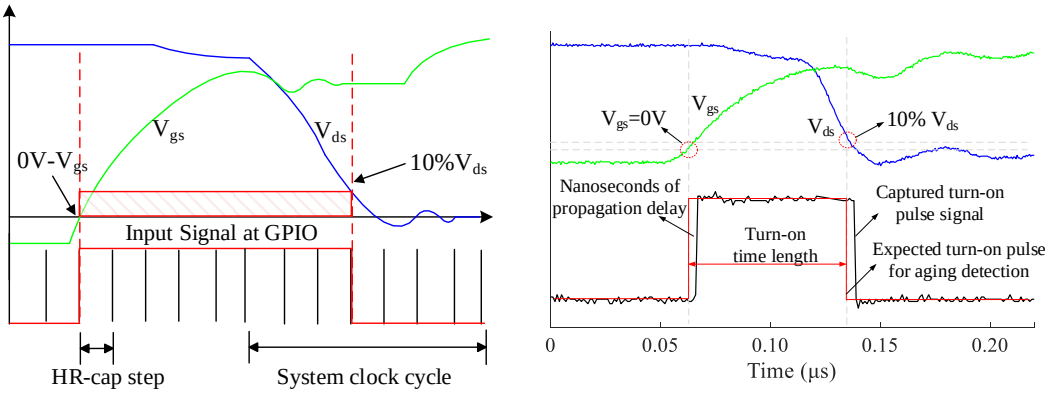


Figure 5.6. Proposed in-situ condition monitoring circuit.

Both V_{ds} and V_{gs} signals are selected as input and voltage dividers are used to scale down the voltages. At high frequencies, the stray inductance of the divider resistors can be remarkable. Hence, possible overshoots and noise can distort the detected signal and affect the measurement accuracy. To eliminate this, parallel capacitors can be used to compensate the impedance at high switching speed. However, additional capacitors may potentially introduce power loss during switching transient. Alternatively, high bandwidth op-amps can be used as buffer circuit to introduce high input impedance. However, if the switching frequency is not too high, these buffers are not needed. In addition to the buffer circuit, an RC filter is utilized to suppress the ringing noise and transmit just detected edges. In this test, the turn-on time is defined when V_{gs} is above 0 V and

V_{ds} drops to 10% of the dc-link voltage. The comparator output signals are fed to the AND logic gate to generate a short pulse width representing the turn-on time as shown in Figure 5.7 (a). To validate aging detection at both upper and lower switches, detection circuit reference plane is set at DUT source voltage and isolation is needed between designed aging detection circuit and system controller ground. Hence, additionally, a digital isolator is used to transmit the turn-on pulse to the MCU beyond the AND gate.



(a) (b)

Figure 5.7. (a) Proposed and (b) tested measurement timing.

Figure 5.7 (b) shows the verification of the proposed method, V_{gs} and V_{ds} voltages during turn-on transient and detection circuit output voltage waveform are illustrated. The red curve depicts the expected voltage pulse output by proposed detection circuit in Figure 5.6. To achieve precise absolute device turn-on time (T_{on}) detection, expected curve starts at 0V V_{gs} and ends at 10% V_{ds} during voltage fall. The black waveform depicts the experimentally detected turn-on pulse in Figure 5.6. As can be seen, the proposed circuit is capable of accurate turn-on pulse time measurement. Though around 3ns measurement delay is observed for the captured turn-on pulse signal which is caused by the propagation delay of the voltage comparison circuits and isolator,

this delay does not impact the measurement precision since the same propagation delay applies to all measurement results before and after aging. In addition, for condition monitoring, instead of absolute time measurement, relative change matters and the decision is made based on this change. To validate the measurement for different operation conditions, several impacts need to be discussed before and after aging. The selected reference voltages for voltage edge capturing in Figure. 5.7 (a) defines the time range of the captured transient during turn-on. V_{ref1} defines the end of captured turn-on pulse end and V_{ref2} defines the starting point of the turn-on pulse. To effectively capture the full turn-on time interval, reference voltages need to be properly selected to assure the captured time intervals keep consistent before and after aging. 10% of V_{ds} is selected as reference voltage for the first comparator (Comp 1). In this way, drain-source voltage fall stage is fully captured by the monitoring circuit. Furthermore, 10% V_{ds} is also officially selected for turn-on transient time range definition per IEC60747-8-4.

Although, negative off-state voltage of -5V is commonly used in SiC MOSFETs to achieve high noise tolerance and fast switching, 0V is selected as V_{ref2} to trigger the turn-on pulse rising edge. This provides consistency for applications with different negative off-state voltage than -5V. In addition, a negative V_{ref2} may result in false triggering of the monitoring circuit due to system noise and V_{gs} ringing. Hence, in the proposed method, when the V_{gs} reaches to 0V during turn-on transient, the voltage comparator (Comp 2) is reliably toggled, and the monitoring circuit can capture the full range device turn-on time. As the starting point of the turn-on pulse is fixed, the turn-on time increment can be precisely observed by only measuring the time shift of V_{ds} falling edge.

At higher junction temperature (T_j), SiC MOSFETs operation exhibit lower V_{th} and higher g_m. Based on the device analytical model, higher T_j implies shorter T_{on}. In Figure 5.8, the drain-source voltage drop is measured at 25ºC, 85ºC and 115ºC by means of DPT. A 20Ω $R_{g,ext}$ is used to compare the temperature dependent switching transient test and T_{on} evaluation result to compare with former discussion. Compared to the room temperature, roughly 7ns T_{on} decrease is observed at 115ºC. Therefore, the temperature effect needs to be considered and decoupled from aging related changes to avoid false alarms. Since the real-time junction temperature estimation and temperature effect decoupling are challenging tasks, the proposed health monitoring method is conducted at system start-up to avoid these challenges. At start-up stage, the device junction temperature is close to the outside ambient temperature and temperature variation during turn-on time measurement is negligible. For a practical system implementation, a calibration curve can be used for condition monitoring. At system start-up, the device junction temperature will be close to ambient temperature and temperature variation during turn-on time measurement is negligible. Hence, onboard ambient temperature sensor can be utilized for T_j estimate. When operating at different environment temperature, a calibration curve can be utilized to correlate the measurement to normal temperature value. Therefore, the junction temperature effect can be fully decoupled from proposed aging detection system.

Theoretically, larger $R_{g,ext}$ implies longer turn-on delay. In addition, both current rise time and voltage fall time are extended. Hence, with higher $R_{g,ext}$, device T_{on} increase caused by aging can be captured relatively easier. The load current affects the switching transient as well since the Miller plateau has a positive shift when load current is high.

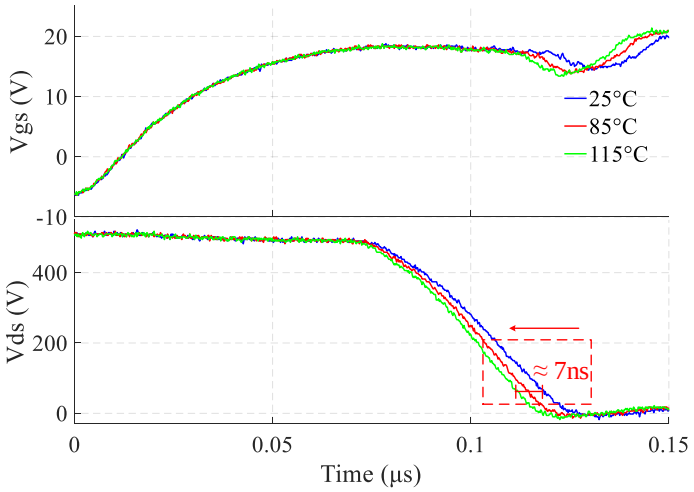
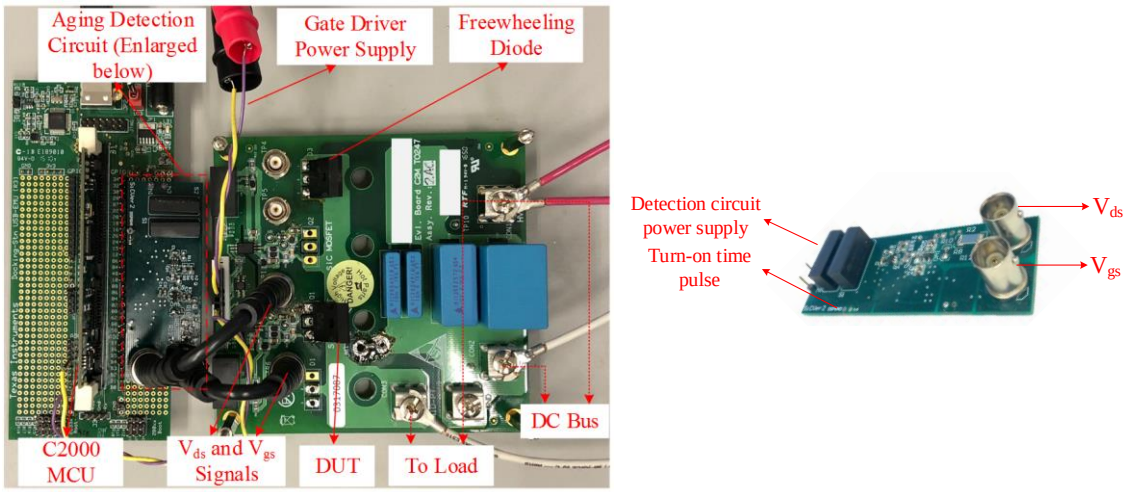


Figure 5.8. Temperature effect on turn-on time



(a) (b)

Figure 5.9. (a) In situ SiC MOSFET degradation monitoring setup and (b) T_{on} detection board

Under the light of above discussions, a higher value of $R_{g,ext}$ is suggested if the measurement resolution is not high enough and require longer delays. This can be achieved by adding a parallel branch. Although it is not needed in our implementation, a relatively high resistance (R_{det}) can be used during the system start up for extended turn on delay, and then paralleled with another resistor

after the first few cycles when measurement process is complete. The condition monitoring setup is shown in Figure 5.9.

5.3 System Implementation

To validate proposed condition monitoring method to practical system operation, a buck converter is used and proposed V_{mp} and T_{on} detection is applied at system start-up. As reported, the observed aging precursors are dependent on device junction temperature. Hence, by conducting monitoring process at start-up, the temperature effect can be fully avoided.

Another impact factor of measurement is the load current. Two applicable methods are proposed in this dissertation.

1) System Current Sensor

In most power converters, shunt resistors as current reading sensor are inherently deployed for system control purpose. At system start-up stage, V_{mp} and load current readings of the first 10 switching cycles can be fully recorded by system DSP. These measured V_{mp} values at certain I_{Load} is compared to the healthy state transient values. A comprehensive lookup table indicating expected V_{mp} value under different load conditions can be used. This lookup table can be exhaustively learned during system operation at the early stage of device's lifetime. By comparing the detected V_{mp} to healthy state value under the same load current, the impact of load can be calibrated.

2) Cycle Control

For system with heavy load condition such as high torque 3-phase motor drives, the starting current could be large enough for aging detection. To avoid I_{Load} impact on V_{mp} measurement precision, system starting current can be actively controlled. At system start-up, since the output voltage

remains 0V and the inductive load value is known, the first cycle duration can be actively adjusted by digital controller to acquire consistent load current.

Table 5.1. Detected Miller Plateau during Start-ups

Load	DUT-1		
	Start-up1	Start-up2	Start-up3
30Ω	3.562V	3.563V	3.557V
50Ω	3.560V	3.563V	3.560V
70Ω	3.559V	3.560V	3.561V
90Ω	3.559V	3.558V	3.560V

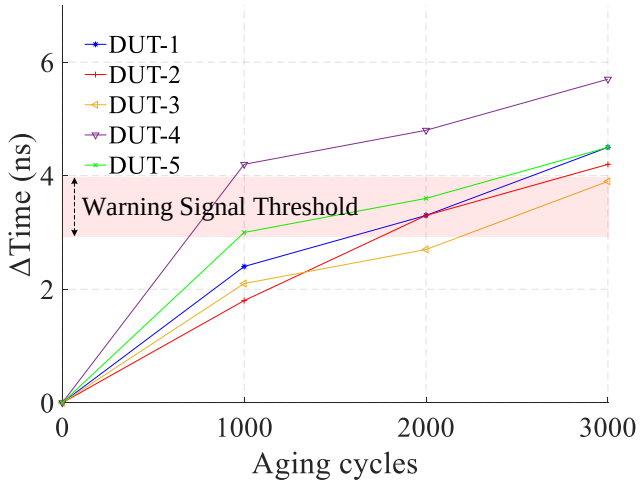


Figure 5.10. ΔT_{on} measurement with proposed aging detection approach.

In this dissertation, the load current is controlled to 10A after the first switching cycle, and the load resistors are set to 30Ω, 50Ω, 70Ω and 90Ω, respectively. Furthermore, to verify the repeatability of proposed current control method, the in-situ condition monitoring is conducted three consecutive times. As shown in Table 5.1, the proposed V_{mp} based aging detection is quite repeatable for multiple start-up tests. Also, at different load conditions, the detected Miller plateau

also matches the theoretical discussion, and no more than 5mV static error is observed. Compared to 0.2V Miller plateau shift throughout device degradation, proposed aging detection method can achieve high resolution on-board SiC MOSFET state of health assessment. Similarly, the same system implementation method can also be adopted for Ton based aging detection. The tested results are shown in Figure 5.10.

CHAPTER 6

DRAIN-SOURCE RESISTANCE BASED CONDITION MONITORING[3]

6.1 Proposed Degradation Monitoring Approach

In the proposed monitoring method, both die and package related aging detection is performed by running an in-situ diagnostic test at system start-up. The test is performed after the input DC voltage is applied and the DC bus capacitors charge up and before the normal converter operation begins. The test itself takes several milliseconds with the exact time taken depending on switch capacitances, power loop inductances and the bandwidth of the measurement circuit. The test is performed in two steps. First, $R_{ds\text{-}sat}$ of the devices is measured and in the next step $R_{ds\text{-}on}$ is calculated.

Figure 6.1 (a) depicts the schematic of the circuit for $R_{ds\text{-}sat}$ measurement which is used to monitor gate oxide degradation in SiC MOSFETs of the converter. V_{det} stands for the low positive bias applied to the gate for saturation mode conduction. -V_{ee} (-5V) is used as the turn-off state V_{gs}, V_{cc} = 20V is used as turn-on state V_{gs} during full turn on. For $R_{ds,sat}$ measurement, the applied DC bus voltage is used to inject current through the MOSFETs in a phase-leg while all the other legs in the converter, if any, are kept off. First, one of the devices in the leg, shown as S1 for illustration, is turned on at the full gate voltage such that the device's channel is fully on and the DUT, shown as S2 for illustration, is turned on for a short duration in saturation mode under low gate voltage V_{det}. During this interval, although the devices are in the leg are on simultaneously, since $R_{ds,sat}$ of

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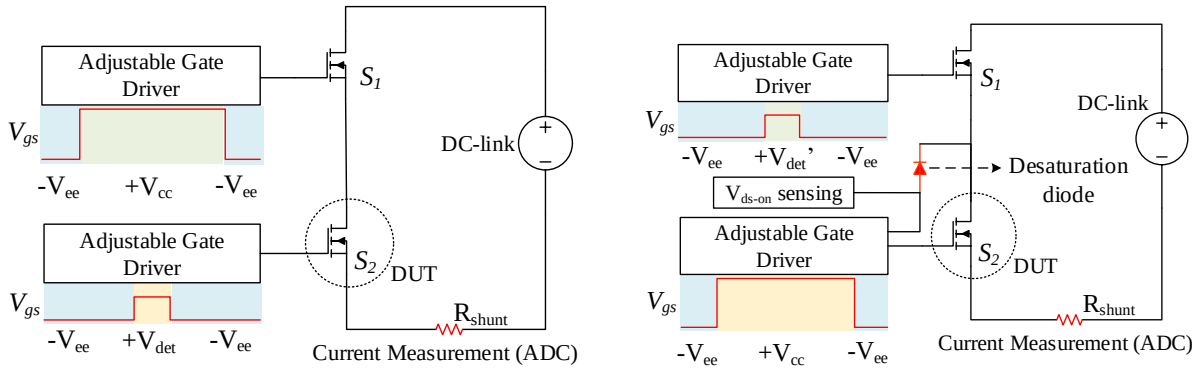
S. Pu, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu and B. Akin, "A Practical On-Board SiC MOSFET Condition Monitoring Technique for Aging Detection," in *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2828-2839, May-June 2020.

the DUT is relatively high, the current in the leg is limited to a safe value. Now, since the on-state resistance of the devices operating in saturation mode is much higher than the fully on device, it can be assumed that the resistance of the leg is almost equal to the $R_{ds,sat}$ of the DUT. The current through the leg can be measured by using the system current sensor, represented by R_{shunt} in Figure 6.1 (a). The voltage across the leg is measured using the system DC link voltage sensor. By dividing the obtained voltage and current values from the same instance, the $R_{ds,sat}$ of the DUT is calculated. The use of system current and DC link voltage sensors, which are readily available in most converter systems, eliminates the need for additional sensors for $R_{ds,sat}$ measurement. The above process is then repeated with S1 acting as the DUT and S2 being turned on at full gate voltage. Further, the process is also repeated for every leg to obtain $R_{ds,sat}$ of each of the switches.



(a) R_{ds-sat} (b) R_{ds-on}

Figure 6.1. Proposed monitoring methods in phase-leg configuration.

Figure 6.1 (b) depicts the schematic of the circuit for $R_{ds,on}$ measurement which is used to monitor package related degradation in the devices. V_{det}' stands for the gate bias applied to the complementary switch during $R_{ds,on}$ detection stage. $-V_{ee}$ and V_{cc} have the same values as previously mentioned. For $R_{ds,on}$ calculation, first, DUT S_2 is turned on at $+V_{cc}$ such that its channel

is fully conducting. Then a gate pulse of V_{det}' is applied to switch S_1 such that it turns on in saturation mode. It is important to turn on S1 in saturation mode to ensure that the current in the phase-leg is limited and both the switches operate within their safe operating area (SOA). The $R_{ds,on}$ of the switch is calculated by sensing the $V_{ds,on}$ across the DUT and dividing it by the current value obtained from the system current sensor. The schematic of the $V_{ds,on}$ sensing circuit is shown in Figure 6.2 [123].

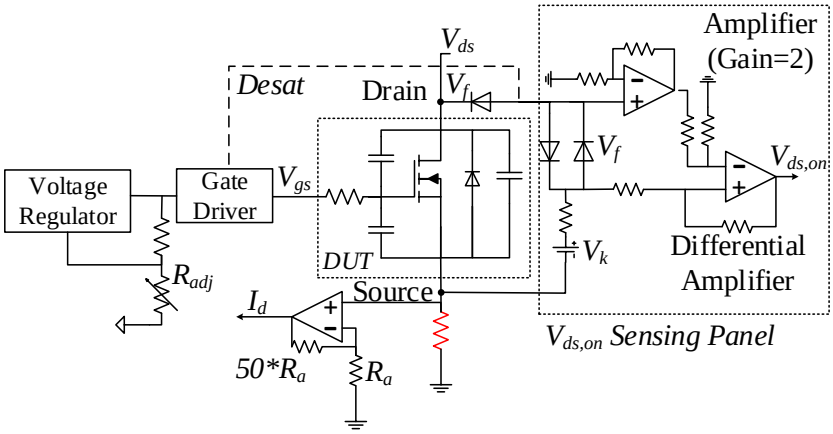


Figure 6.2. Schematic of S_2 with $R_{ds\text{-}on}$ measurement circuit.

The circuit uses a combination of amplifiers to directly output the device $V_{ds,on}$. The desaturation diode used in gate driver short circuit protection circuit itself is used as the high voltage blocking diode when the switch is turned off. From Figure 6.2 it is seen that when the DUT is turned on, the non-inverting input to the differential amplifier is at $2V_f+V_{ds,on}$. The inverting input is fed by a doubling amplifier whose output is equal to $2V_f+2V_{ds,on}$. Hence, the differential amplifier output is equal to the conduction voltage drop across the DUT. It must be noted that DUT (S2) is turned on first and turned off later to ensure that its switch capacitance is completely discharged before current passes through it. This is important to avoid potential high voltage ringing across the switch capacitance due to interaction with parasitic inductances present in the power loop. The process is

repeated with S1 acting as DUT and S2 being turned on in saturation region. Similarly, it is repeated for each leg to obtain the $R_{ds,on}$ value of each of the switches.

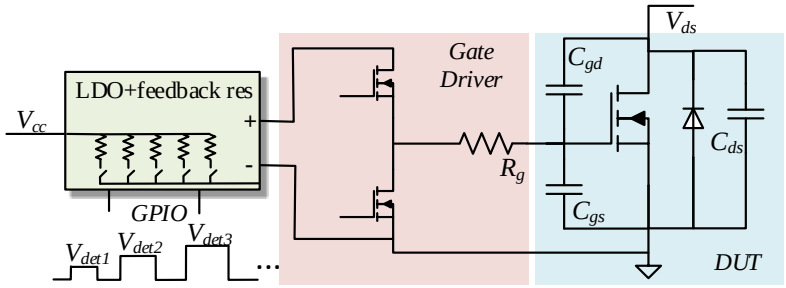


Figure 6.3. Schematic of S2 for single pulse test.

The detailed schematic for on-board adjustable gate driver implementation is shown in Figure 6.3. To vary the applied gate voltage for both aging detection ($V_{det,}$ V_{det}') and normal operation (V_{cc}) on-board, the gate driver is powered up by an adjustable LDO regulator. The output of LDO regulator is actively tuned through a digital potentiometer which is controlled by system DSP's GPIO.

The applied gate voltages, injected current pulse magnitude and duration, gate resistances are the important variables which influence the effectiveness of the proposed degradation monitoring method. Hence, in this study, a systematic discussion on the choice of these variables is presented. The effect of the variables is characterized through a single pulse test setup. The single pulse test is conducted with two switches S1 and S2 serially connected across a 300V DC link in a phase leg configuration like that shown in Figure 6.1. For the test only one of the switches (S2) has an adjustable gate driver and is designated as the DUT. S1 has a normal gate driver with full voltage swing (V_{cc}=+20V and V_{ee}=-5V).

To actively vary the applied gate voltage to S2, an adjustable voltage regulator's output is used as the gate driver power supply. The voltage regulator has a potentiometer feedback to adjust the gate

voltage as depicted in Figure 6.3. A shunt resistor (R_{shunt}) is used for DUT drain current measurement in test setup. For the test, the DUT is turned on at low gate voltage such that it operates in saturation mode and S1 is turned on completely at full gate voltage. The DUT is characterized for various combinations of the test variables like DUT gate voltage level, current magnitude, leg turn on duration and gate resistance. Based on the tests, the factors influencing the choice of these parameters are discussed below.

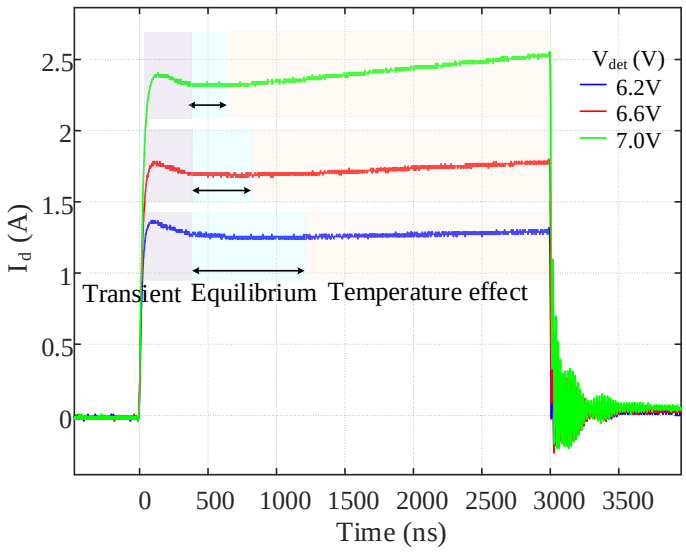


Figure 6.4. Measured $I_{d,sat}$ with different applied V_{det} by SPT.

1) Gate Bias for Aging Detection (V_{det})

Figure 6.4 shows the injected $I_{d,sat}$ waveforms at different V_{det} for a healthy DUT. As expected from the device transfer characteristics, higher drain current is injected at higher V_{det}. In Figure 6.4, three intervals can be observed during device conduction. As soon as V_{det} is applied to the device gate, drain current rises. However, due to resonance between device lead inductance, circuit stray inductances and device capacitances, a current overshoot can be observed which is subsequently damped by the relatively high $R_{ds,sat}$. This transient interval lasts for about 300 ns for different V_{det}

as shown in Figure 6.4. Following this transient interval, DUT reaches equilibrium state. In this interval, I_d remains almost constant. The $I_{ds\text{-}sat}$ through the DUT is measured during this equilibrium interval from which $R_{ds,sat}$ is calculated. However, due to the high V_{ds} across the device and injected $I_{d,sat}$, there is significant device conduction power loss which causes a rise in the DUT junction temperature. Further, the threshold voltage of a SiC MOSFET is inversely proportional to its junction temperature. Hence, with higher T_j, I_d is expected to be higher for the same V_{det}. This positive feedback effect is observed in Figure 6.5 as an increasing $I_{d,sat}$ value in the third interval as the device T_j increases due to heating. It implies that the equilibrium interval gets shorter as V_{det} increases due to early onset of device heating due to increased power loss.

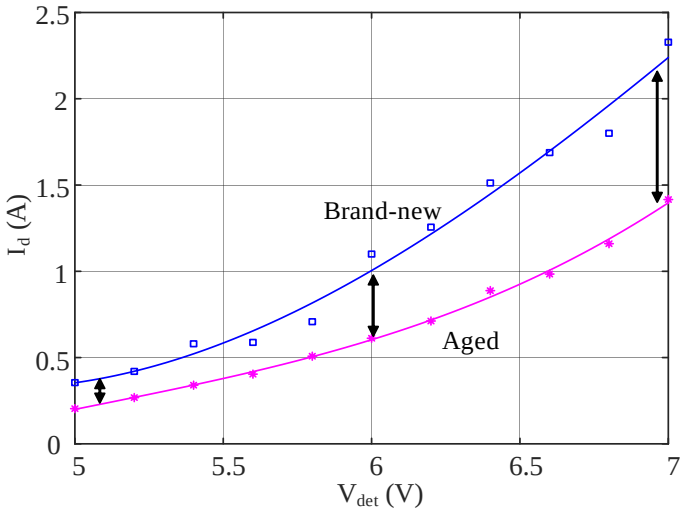


Figure 6.5. Measured $I_{d,sat}$ before and after DUT aging.

As discussed in Section II, with aging, the electro-thermal stresses on the device reduce the ability of the gate to form the inversion layer for on state current conduction. Hence, for the same V_{det}, $I_{d,sat}$ is expected to decrease with device aging. In Figure 6.5, the measured DUT $I_{d,sat}$ is plotted against V_{det} varying from 5V to 7V for a healthy and aged device. It is observed that when higher V_{det} is applied, larger $I_{d,sat}$ difference can be observed. When V_{det}=5V, only 200mA decrement is

reported. Whereas $I_{d,sat}$ decreases by 1A at V_{det}=7V. From the above discussion, it can be concluded that testing at higher V_{det} leads to higher $I_{d,sat}$ which in turn results in greater accuracy in the calculation of $R_{ds,sat}$. Also, for a given measurement resolution, operation at higher $I_{d,sat}$ increases resolution of degradation monitoring due to a larger and observable shift in $I_{d,sat}$ over aging. At the same time, operating at high V_{det} shortens the $I_{d,sat}$ equilibrium interval due to higher power loss hence reducing the available $I_{d,sat}$ measurement window. Therefore, the choice of V_{det} for in-situ monitoring is a tradeoff between measurement accuracy and available measurement window.

2) Applied Detection Pulse Duration (T_p)

Another variable that influences the proposed degradation monitoring method is the duration of the applied V_{det}. An obvious constraint on the in-situ monitoring operation is that the switches must always operate within their safe operating area (SOA). As per the device datasheet, the SiC MOSFET being tested can safely conduct 10A for 10µs with a V_{ds} of 800V. However, the voltage, current and pulse duration must be kept well below these limits to ensure that the degradation monitoring operation itself does not stress the device. Hence the V_{det} pulse duration must be kept as short as possible. The other important constraints are that $I_{d,sat}$ measurement must be made during the equilibrium interval to ensure measurement accuracy and the duration of the available equilibrium interval measurement window must be greater than the setup and hold times of the ADC used for $I_{d,sat}$ measurement.

3) External Gate Resistance (R_g)

As discussed above, a measurement made during the device turn on might not be reliably used for accurate $R_{ds,sat}$ calculation. Hence, it is important to keep the transient interval as short as possible to prevent its impact on detection accuracy and junction temperature of the DUT. To evaluate the

external gate resistance's influence on the transient interval, I_d waveforms are evaluated at turn-on for different values of external gate resistance ($R_{g,ext}$). Figure 6.6 shows $I_{ds\text{-}sat}$ waveforms for different values of gate resistances under same V_{det}.

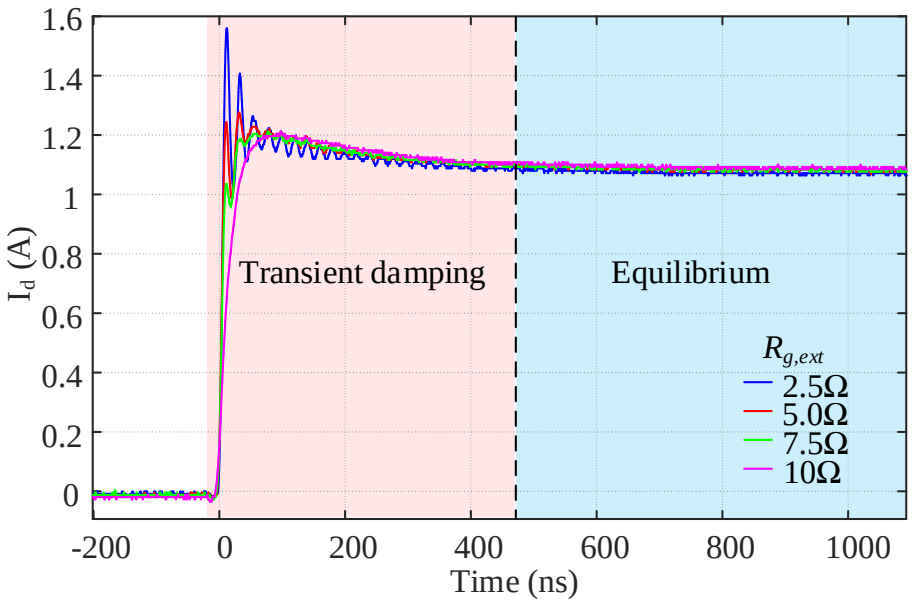


Figure 6.6. Injected I_d transient with different $R_{g,ext.}$

From Figure 6.6, it is evident that there are two transient current components in the drain current waveform at turn on, namely a fast high frequency transient due to parasitics in the gate loop and the much slower power loop transient. The fast transients die out before the slow transient even for a value of $R_{g,ext}$ as low as 2.5Ω. As seen here, higher values of $R_{g,ext}$ lead to faster damping of the fast transients. The slower power loop transient damping duration is largely independent of the value of $R_{g,ext}$. Since the slow transient, which is largely independent of the $R_{g,ext,}$ is the one affecting the measurement delay, the proposed condition monitoring method can be applied effectively even with a low value of $R_{g,ext}$. This implies the device turn on/off speed can be kept high therefore ensuring lower switching losses during the normal converter operation.

4) Applied Current for $R_{ds,on}$ Measurement (I_{det})

The constraints in choosing a suitable I_{det} for $R_{ds,on}$ measurement is the measurement accuracy and SOA operation of switch complementary to the DUT. Since, $R_{ds,on}$ is a relatively small value to measure, it is challenging to accurately measure it at low device currents. Hence, higher I_{det} would ensure greater measurement accuracy for $R_{ds,on}$. However, since the switch complementary to the DUT is operating in saturation region, it has significant power loss. It is important to ensure that this switch always operates within its SOA. To characterize the on-board $R_{ds,on}$ measurement circuit's accuracy, the measured $R_{ds,on}$ value from single pulse test circuit ($R_{ds,circuit}$) is compared to curve tracer measurement ($R_{ds,ref}$) in Table I. As expected from earlier discussion, at low $I_{d,sat}$ (1A), the deviation is around 0.89 mΩ. When larger $I_{d,sat}$ (2.5A) is applied, the measurement error caused by detection circuit further reduces (<0.5mΩ). Hence, if the complementary switch operated within SOA, $R_{ds,on}$ of the DUT can be effectively acquired.

Table 6.1. Drain-source on-resistance measurement of DUT-1

$I_{d,sat}$	$R_{ds,circuit}$	$R_{ds,ref}$	$\lvert R_{ds,circuit}-R_{ds,ref}\rvert$
1A	308.11 mΩ	309 mΩ	0.89 mΩ
1.5A	308.22 mΩ	309 mΩ	0.78 mΩ
2A	308.19 mΩ	309 mΩ	0.81 mΩ
2.5A	308.57 mΩ	309 mΩ	0.43 mΩ

From the discussion in preceding sections, we need to choose a suitable value of V_{det} such that $I_{d,sat}$ at that V_{det} is large enough for accurate $R_{ds,sat}$ measurement and ensure that the available equilibrium interval is long enough for the system ADC sampling. However, existing analytical and behavior device models are not accurate enough to precisely predict the value of injected $I_{d,sat}$

at certain V_{det}. To address this, the V_{det} necessary to achieve target $I_{d,sat}$ is calculated by the system the very first time it is started. The same value is used throughout the life of the converter. During this process, as shown in Figure 6.7, consecutive gate pulses of increasing voltage magnitude are applied to the DUT the very first-time system is started, while the other device in the phase-leg is kept fully on. The DUT current is measured during the application of each of the pulses and the gate voltage setting for which the DUT current first exceeds the target current is used as V_{det} for DUT testing over its lifetime.

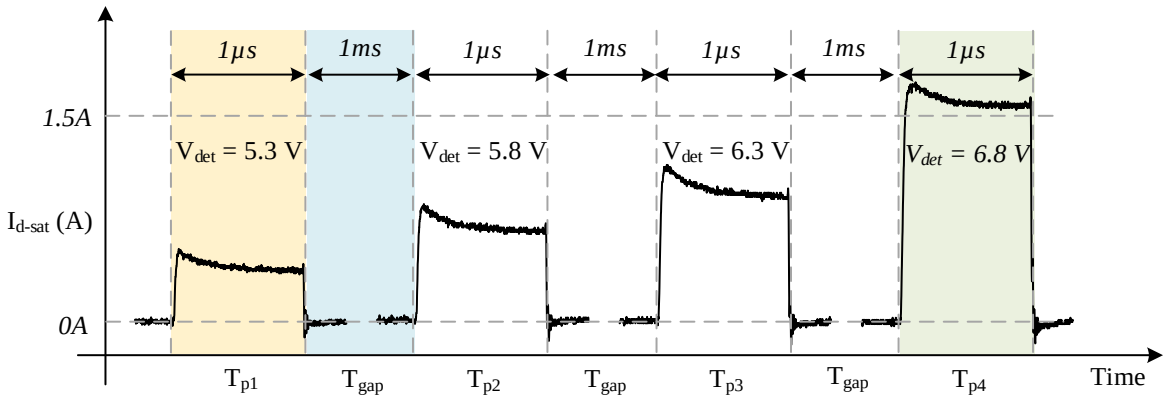


Figure 6.7. Time sequence of applied $I_{ds\text{-}sat}$ pulses to determine V_{det}.

In this study, C2000 series DSP from Texas Instrument is used, the ADC of which needs 80ns to acquire a voltage signal. Hence, an equilibrium interval of at least 100ns is chosen for accurate $I_{d,sat}$ measurement. In Figure 6.4, worst case transient interval of 500 ns is observed for the SiC MOSFET being tested. Therefore, a T_p of $1\ \mu s$ is selected as the optimal pulse duration for accurate $I_{ds\text{-}sat}$ measurement.

Based on single pulse tests of the device before and after aging shown in Figure 6.4 and detected $R_{ds,on}$ data from Table 6.1, a target current of 1.5 A is chosen for $R_{ds,sat}$ measurement as it offers sufficient measurement accuracy, high resolution of $R_{ds,sat}$ variation over aging and sufficiently

long equilibrium interval of around 500ns. As can be seen in Figure 6.7, 1us pulses followed by 1ms rest period are applied to determine the V_{det}. The gate voltage is incremented by 0.5V between pulses. The target current is reached at V_{gs} = 6.8V and it therefore it is picked as the V_{det}. Similarly, 2.5 A is selected to accurately monitor DUT's $R_{ds,on}$ over degradation.

6.2 Case Studies

As discussed above, the proposed method uses the system sensors to obtain current and voltage values. Therefore, to validate the proposed SiC MOSFET degradation monitoring method in various power converter applications, case studies on different circuit current sensing configurations are discussed in this section. For experimental illustration, a three-phase inverter prototype is used for $R_{ds\text{-}sat}$ and $R_{ds,on}$ evaluation over aging, which is shown in Figure 6.8.

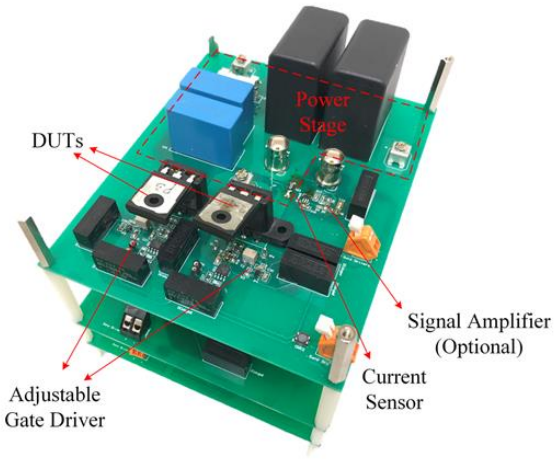


Figure 6.8. A three-phase power converter prototype with aging detection functionality.

6.2.1 Case Study 1: Shunt Resistor in Phase-leg

In phase-leg based power converters, shunt resistors are commonly employed for phase current measurement and are connected in series with power leg. For example, in some of the motor drive

systems, separate shunt resistors are connected in series with the power switches on the low side of each phase-leg. Using the current shunt on the return path of phase leg eliminates need for current sensing isolation. For illustration, DUT-1's current pulses over aging are depicted in Figure 6.8. A dramatic decrease is observed from healthy state to 5000 aging cycles. The observed 0.6A decrement in $I_{d,sat}$ matches with the single pulse test results shown in Figure 6.9. In the test setup, 0.02Ω shunt resistor is employed for current sensing. For the chosen current shunt value, a variation of 0.6A in $I_{d,sat}$ over aging translates to a 12mV change in voltage across the current shunt. This variation can be accurately measured as it is much larger than the 0.8mV resolution of the system ADC used. However, if system's R_{shunt} or ADC sensitivity is low, an optional non-inverting amplifier can be added to improve measurement resolution.

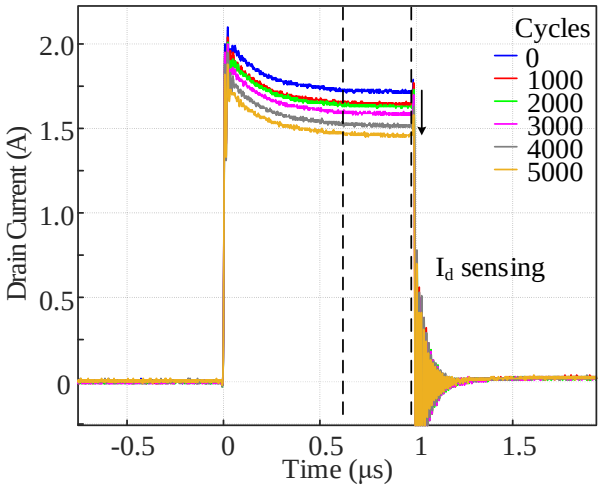
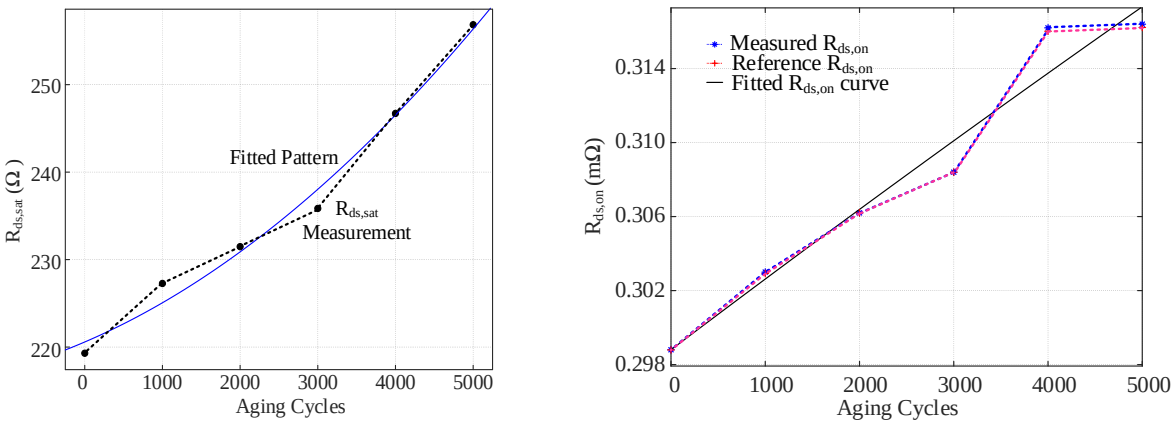


Figure 6.9. On-board measured DUT-1 $I_{d\text{-}sat}$ pulses over aging.

In Figure 6.10 (a) and (b), measured $R_{ds,sat}$ and $R_{ds,on}$ are plotted throughout device's aging process. From 0 to 5000 cycles, $R_{ds\text{-}sat}$ increases by almost than 30Ω. This result matches with the measurement obtained using the curve tracer. The curve fitted to the obtained $R_{ds,sat}$ values over aging is depicted in blue $R_{ds\text{-}sat}$ shows monotonic increment with device aging over its lifetime.

Similarly, measured $R_{ds,on}$ also increases throughout device aging. As shown in Figure 6.10 (b), the values of $R_{ds,on}$ obtained from on-board measurement circuit matches with the curve tracer measured reference values. It is verified that DUT $R_{ds,on}$ change can be accurately monitored by proposed method when the current is sensed through shunt resistors.



(a) (b)

Figure 6.10. Measured DUT-1 (a) $R_{ds,sat}$ and (b) $R_{ds,on}$ increment over aging.

6.2.2 Case Study 2: Current Transducer with Inductive Load

In some cases, the system current sensor is connected in series with the phase outputs as illustrated in Figure 6.11. In this case, the load inductance is in series with the current path and introduce challenges to current sensing. A similar situation is also seen in step-down converter, where the buck inductor exists in current measurement loop. In cases like these, the presence of the inductor impacts the injected drain current during DUT condition monitoring stage.

Due to the presence of load inductance in system current path, power loop current is expected to rise gradually when V_{det} is applied. This added current rise time would make the duration of the transient interval longer. This is illustrated in Figure 6.12 where $I_{d,sat}$ pulses at V_{det} = 5.5V are

shown for different values of load inductance when power loop across S_4-S_5 is selected for current injection and S_4 is picked as DUT. As observed in Figure 6.12, the initial spike in current when gate voltage is applied is due to junction is due capacitance charging current of the anti-parallel diode of the upper switch S_3 as it goes to full blocking state at V_{bus}. After the upper diode is fully charged, current starts to flow through the load inductance. Theoretically, current rise time is positively impacted by load inductance. It is verified in Figure 6.12 that the load inductor induced extra current rise time makes the transient interval longer. For example, for a 170 µH L_{load}, the current settles in 0.8 µs, whereas it takes nearly 3 µs for the current to settle for a 1.5 mH L_{load}. Since a reliable $R_{ds,sat}$ value cannot be obtained during the transient interval, testing should be conducted at a lower V_{det} to avoid temperature induced $I_{d\text{-}sat}$ change during this interval and ensure DUT is accurately monitored at the equilibrium state of injected I_d pulse.

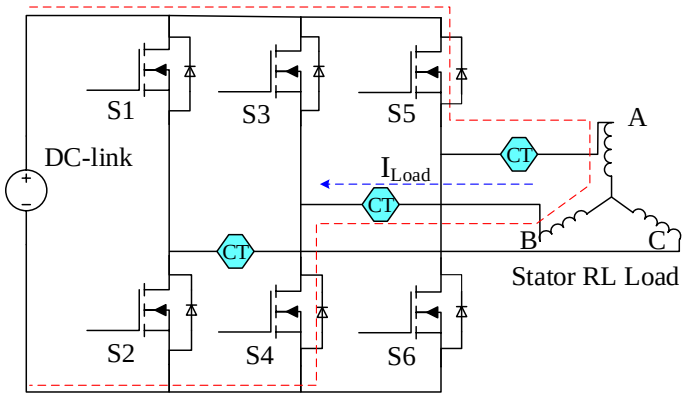


Figure 6.11. Motor drive system with load side planted current sensors.

In Figure 6.13, V_{det} = 5V, 5.5V and 6V are applied to the gate for the same L_{Load} (400 µH). As can be seen from the figure, the transient interval is lower at lower V_{det}. Further, compared to the shunt resistor based current measurement method used in phase-leg configuration, the current transducers' sensing bandwidth is lower (=1MHz). Hence, by applying a low V_{det}, an I_d pulse with

adequate current sensing duration can be acquired, and $I_{d,sat}$ can be effectively captured. For V_{det} = 5V, the transient interval reduces to 1.25 µs from around 2us for V_{det}=6 V. Therefore, instead of choosing the target $I_{d,sat}$ as 1.5A for degradation monitoring, 0.5A $I_{d,sat}$ is picked to determine the applied V_{det} for aging detection. Consequently, T_p for inductive load has be recalculated due to the additional current rise time. During this interval, the slope of the inductor current is described as:

$$L_{Load}\frac{di_L}{dt} = V_{bus} - i_L \times R_{ds,sat} \tag{6.1}$$

$$i_L = \frac{V_{bus}}{R_{ds,sat}}(1 - e^{-\frac{R_{ds,sat}}{L_{Load}}T_p}) \tag{6.2}$$

The $R_{ds,sat}$ is expected to be minimum when the device is brand new. Hence, if minimum $R_{ds,sat}$ is obtained in equation (6.2), the equilibrium state current is expected to reach an upper limit of 0.5A. The applied current pulse duration T_p can be determined by substituting minimum $R_{ds,sat}$ value into equation (6.2), which is equal to V_{bus}/0.5A. Therefore, when $I_{d,sat}$ shifts negatively with the device degradation, the above calculated T_p is more than adequate for $I_{d,sat}$ to stabilize itself for accurate measurement. For illustration, load inductance of 400 µH is substituted into equation (6.2) and a T_p = 3.07 µs is obtained from calculation.

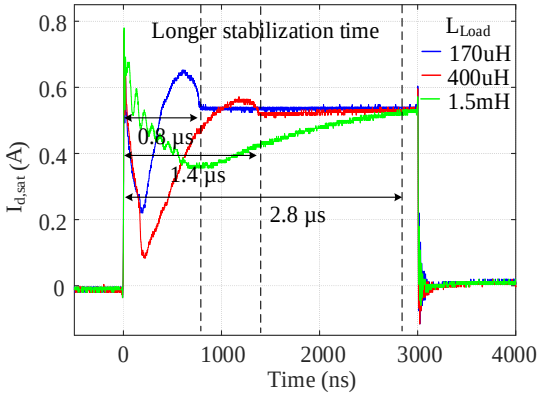


Figure 6.12. Measured $I_{d,sat}$ with different load conditions.

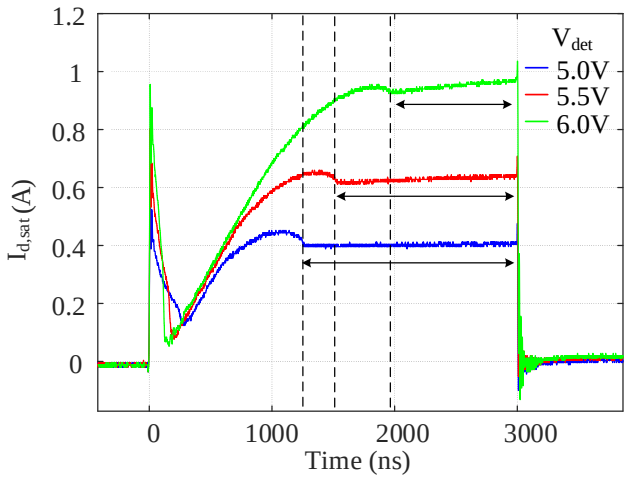


Figure 6.13. Measured $I_{d,sat}$ with different applied V_{det}

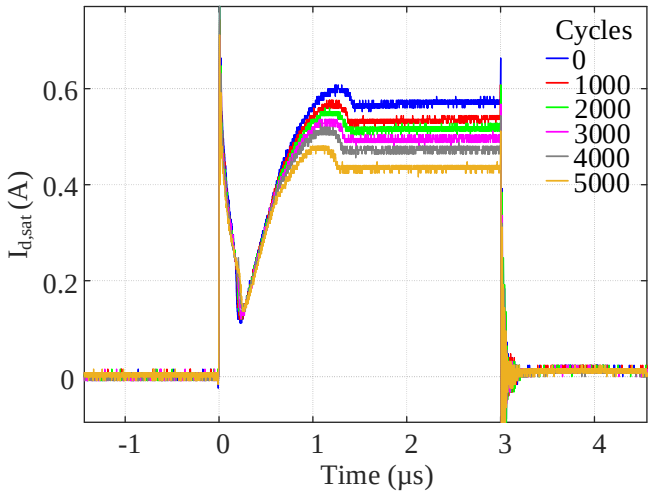
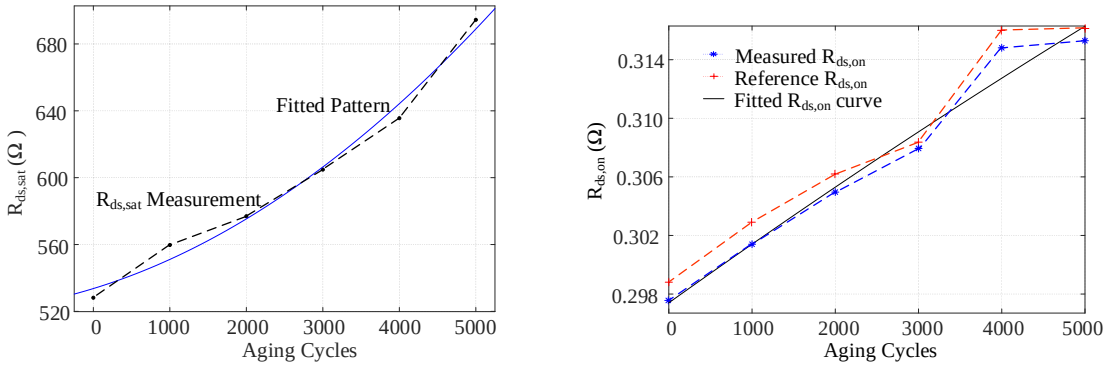


Figure 6.14. Measured $I_{d\text{-}sat}$ shift throughout aging with inductive load.

The experimental result of the measured $I_{d\text{-}sat}$ shift with inductive load is depicted in Figure 6.14. At 5000 cycles, a decrease of 0.3A in the $I_{d,sat}$ is observed which is consistent with the single pulse test result. The 40A hall sensor used in this study could accurately measure the 0.3A shift in $I_{d,sat}$ over aging. For systems, where the sensitivity of current sensor is too low to measure I_d change during aging, an extra high sensitivity current sensor can be used for aging detection. This sensor can operate in saturation mode during system normal operation. As shown in Figure 6.15 (a), the

corresponding DUT's $R_{ds,sat}$ increases by 166.28Ω. Compared to case study I, the detected $R_{ds,sat}$ increment is more remarkable due to operation at lower gate voltage. However, $R_{ds,on}$ sensing accuracy is sacrificed as observed in Figure 6.15 (b) due to lower injected drain current. Compared to an 20mΩ $R_{ds,on}$ shift, the induced $R_{ds,on}$ sensing error is negligible. Hence, as verified, for both the current sensing configurations, the observed $R_{ds,sat}$ and $R_{ds,on}$ shifts match the theoretical analysis results.



(a) (b)

Figure 6.15. Measured (a) $I_{d,sat}$ and (b) $R_{ds,on}$ with inductive load over aging.

CHAPTER 7

LIFETIME ESTIMATION OF SIC MOSFETS CONSIDERING SYSTEM MISSION PROFILE

In this chapter, the operating principle of lifetime estimation toolbox, and workflow of accumulated damage and estimated lifetime calculation is illustrated. The basic operating process and lifetime estimation idea is shown in Figure 7.1. Based on above discussion on device reliability and failure mechanism, device package degradation is induced by junction temperature swing and die related degradation is impacted by junction temperature and gate bias. Therefore, obtaining junction temperature profile during operation is critical for lifetime estimation.

To achieve junction temperature derivation, converter model is used to calculate injected load current and blocking voltage across each device. Once the device operating condition such as V_{ds}, I_d, V_g, R_g are acquired from field or calculated as known values, power loss, as the root cause of junction temperature mismatch from ambient, is calculated. Through thermal network of specific device, the junction temperature rise on top of ambient temperature can be obtained. Once junction temperature profile throughout mission duration is derived, electro-thermal stress calculation algorithm can be implemented, and remaining useful lifetime (RUL) estimation is achieved. In general, the workflow can be concluded as: device power loss calculation, junction temperature calculation, electro-thermal stress calculation, lifetime calculation. Based on the "skeleton" of the toolbox, detailed method and evaluation result is introduced in this chapter.

In subsections, converter modeling and mission profile is discussed firstly. In the second subsection, different methods of power loss modeling and evaluation results are carried out. Thirdly, device lumped thermal model is illustrated with real evaluation data and corresponding

MATLAB sub-model in the toolbox is presented. Finally, the RUL modeling and estimation method is discussed.

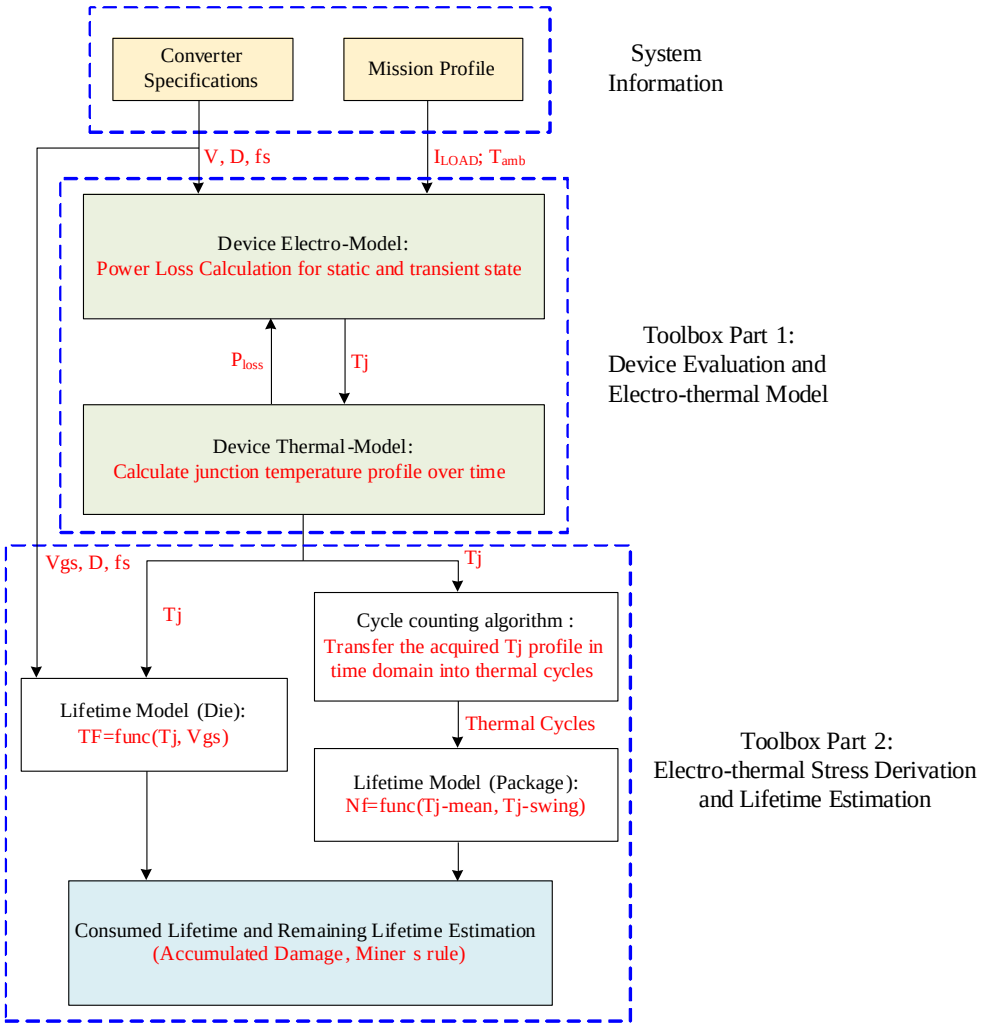


Figure 7.1. Lifetime estimation workflow in health analyzer toolbox

7.1 Device Operating Condition Derivation (System to Device)

Normally during operation, the information of the device operating condition is not directly known value. According to basic system configuration, a temperature sensor is normally implemented to obtain ambient temperature information, to obtain information for robust thermal management

design and over temperature protection. Other available system information is supposed to be bus voltage operation range and output current profile. For constant output voltage type converter, normally a bus voltage sensor is deployed in the system for over voltage protection. Also, load/output current is collected for system control purpose. In conclusion, ambient temperature, bus voltage, load current can be acquired from system mission profile. Based on such information, the operating condition for each device deployed in the system can be calculated. The input/output ratio can be obtained by V_{bus} and I_{Load}, and corresponding duty ratio can be calculated. In Appendix of this report, case study on full bridge dc-dc converter is carried out. Based on converter level profile, device on/off-state duration, injected drain current, blocking drain-source voltage can be calculated as time-series profile.

Furthermore, this information is not enough to obtain device power loss data. During converter design phase, devices are driven by different configuration and conditions. Firstly, when different gate bias is applied to the device, the switching transient speed also varies. For SiC MOSFETs, the turn-on gate voltage is normally kept within +15V to +20V, while turn-off negative gate bias is supposed to be -3V to -5V. With higher the voltage, the gate of the device can be push/pull by larger current and power loss can be reduced. Also, the inversion layer formed at different resistance at different voltage during turn-on. On the other hand, external gate resistance also has a huge impact on device power loss. Higher the $R_{g,ext}$, lower the switching power loss. Hence, converter specs are also important for fine power loss modeling. In conclusion, information required during mission is supposed to be ambient temperature, load/output current, output voltage and input/bus voltage. Besides, gate driver design configuration is also needed for device loss evaluation.

Considering the thermal management design of the power converter, since the temperature rise the toolbox calculates is the temperature rise on top of the deployed system temperature sensor, the thermal network/conduction from device junction to the specific sensor location is also needed from the converter level. The specific derivation method will be discussed in later subsections. Unlike mission profiles during each system operation term, once the thermal network becomes available, no further information is needed from system's thermal design.

Even though to calculate electro-thermal stress in devices need miscellaneous information from the system, all of them should be readily available from converter designing stage. All mission profiles needed for PHM is also obtained by readily deployed system sensor, no extra sensing circuit or addition hardware cost is needed.

7.2 Device Evaluation for Power Loss Calculation

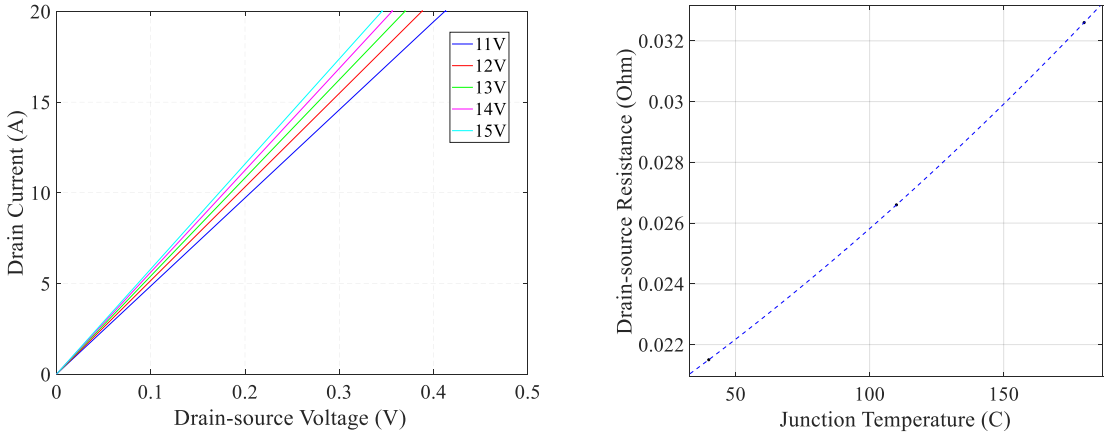
For each device deployed in the system, once information such as drain-source blocking voltage, drain current, gate-source voltage during on and off states are obtained, power loss of the device is calculated and derived.

In this dissertation, device's conduction and switching power loss is directly tested. It can surely provide very accurate power loss result, but it requires abundant hardware-based tests. In this study, such power loss method is demonstrated as example of power loss estimation functionality in the toolbox.

To evaluated device conduction power loss, automated curve tracer is used to extract device on-state resistance at different temperature. In this test, DUT is plugged into the forced air oven for heat-up. At different temperature level, device static parameters are tested. Therefore, over

temperature, device conduction power loss can be calculated during the mission. In static power loss test, several parameters are tested in different operation conditions:

$R_{ds\text{-}on}$: DUT drain-source resistance is evaluated. This is the most critical parameter which is used to evaluated device power loss during conduction state. The specific V_{gs} value during the R_{ds} test is set as 15V which matches the gate driver design in SLB application. However, $R_{ds\text{-}on}$ is also temperature dependent. Hence, the DUT is plugged into the oven during the test starting from 25C as room temperature up to 175 as ambient temperatures. As a result, a look up table can be established regarding different operating temperature.



(a) (b)

Figure 7.2. Tested (a) output charateristic and (b) Rds-on

Output characteristic: Device output characteristic is another critical spec which can be used to extract power loss data during conduction state. On top of the $R_{ds\text{-}on}$ measurement, output characteristic is measured to verify the linearity of the $R_{ds\text{-}on}$ value. According to channel length modulation effect, different operating current may cause voltage drop across drain to source. This electric field may cause $R_{ds\text{-}on}$ change at different load current. As observed in this evaluation test,

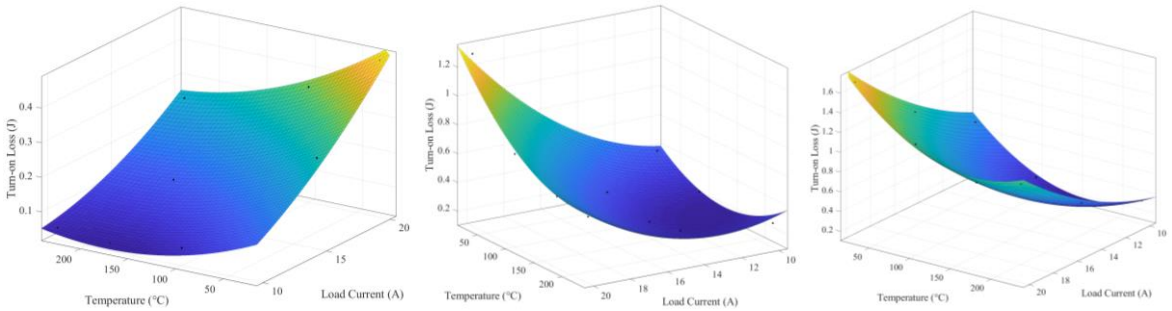
DUT has a very large current rating and very low $R_{ds\text{-}on}$, the linearity of $R_{ds\text{-}on}$ within 20A load current range is very good. It means a consistent $R_{ds\text{-}on}$ can be used to evaluated device conduction power loss at different load current throughout mission.

The specific device conduction loss evaluation result is shown in Figure 7.2. To evaluated device transient power loss during turn-on and turn-off, a double pulse tester is developed to apply hard switching transient to the device under test. As discussed, DPT is widely used to evaluate device transient behavior. Following such circuit configuration, device is switched under hard switching process and corresponding power loss evaluation can be obtained under various conditions since parameters such as bus voltage, load current, gate driver design can be arbitrarily designed and allocated.

After the evaluation, waveform is saved and imported into MATLAB to extract transient power loss. The tested switching transient loss are plotted and fitted to second order equation for switching loss evaluation. The turn-on loss at 200V, 300V and 400V are plotted in Figure 7.3 and turn-off loss at 10A, 15A and 20A are plotted in Figure 7.4. It can be observed that the captured loss evaluation yields to a good second order equation regarding I_{Load} and V_{bus}, which matches the theoretical analysis of the device transient model for both turn-on and turn-off.

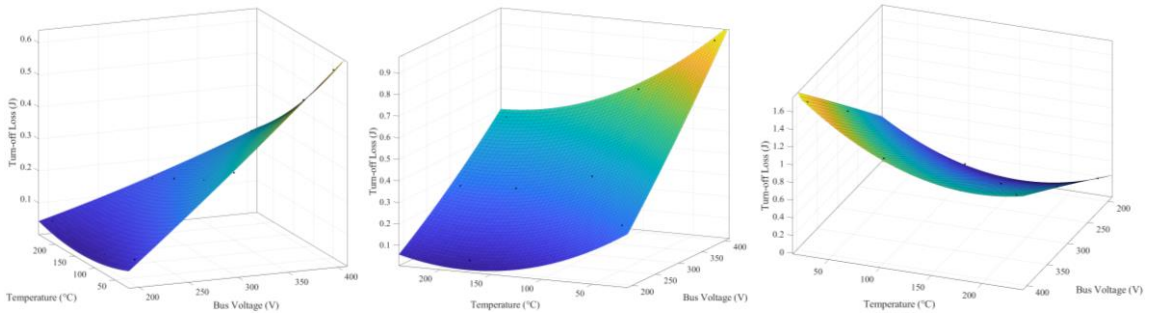
In this subsystem, device conduction power loss, turn-on loss and turn-off loss are determined by input parameter and operating profiles such as duty cycle, bus voltage, load current and junction temperature. In each power loss calculation module, fitted functions are implemented in accordance with device evaluation results. The types of fitted function are determined by device analytical model. In real case of field application, further increasing the evaluated power loss points can improve the power loss calculation accuracy. In the project, we implement 3 data points

in each group regarding bus voltage, load current and temperature for toolbox illustration. In real application, higher data density is recommended to get an accurate power loss prediction subsystem. If more evaluation data is collected and more fulfilled database is established, a look-up table can be used instead of curve fitting and a mapping between operating condition and power loss can be used.



(a) 200V (b) 300V (c) 400V

Figure 7.3. Turn-on loss evaluation over temperature and load current.



(a) 10A (b) 15A (c) 20A

Figure 7.4. Turn-off loss evaluation over temperature and bus voltage.

Based on the device evaluation result obtained by curve tracer and double pulse tester, device power loss under specific condition can be calculated in the converter system and a total power

loss in real-time can be derived and output as the input of thermal network for junction temperature evaluation.

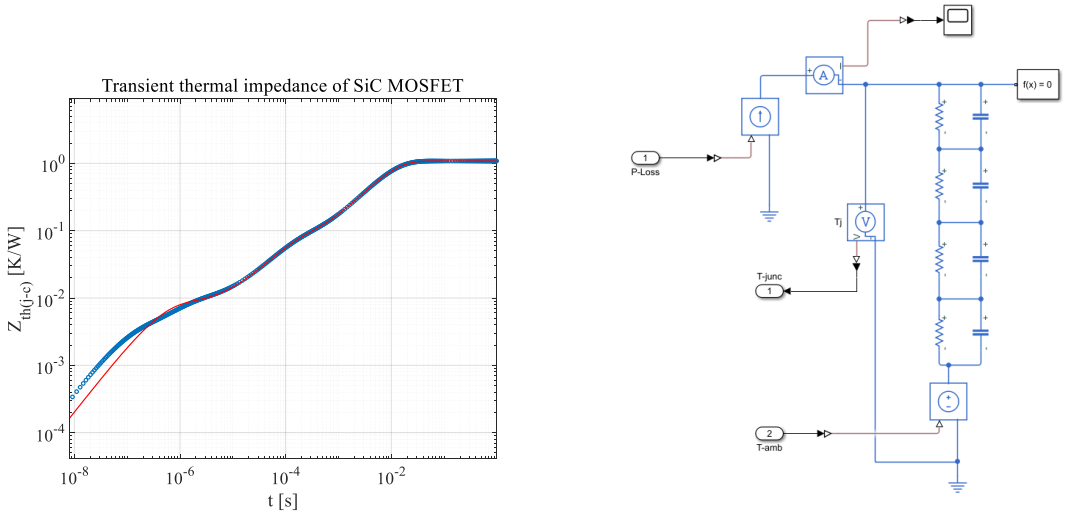
7.3 Thermal Network Calculation and Junction Temperature Profile

The output of the former subsystem is real-time power loss during operation, and the collected power loss is the root cause of junction temperature rise over ambient. Therefore, on top of ambient temperature, device power loss during operation causes temperature mismatch between junction and ambient. Based on such fact, device junction to ambient thermal network needs to be evaluated. The objective is to transfer calculated power loss into T_j increment.

Compared to other thermal conductivity evaluation methods including simulation, a more direct method to obtain lumped thermal model is to conduct direct experimental based thermal transient analysis. The goal of the hardware test is to obtain heating or cooling curve during thermal transient. Since for RC network, the time constant for both charging and discharging is equal, hence either heating or cooling curve can be utilized.

In the thermal network measurement, DUT is actively heated by conducting a constant current in the channel. Once the junction temperature reaches thermal stable state, the current is cut off and the cooling period is captured by both junction temperature sensing and case temperature sensing. To obtain a good resolution of T_j measurement, device reverse voltage drop on body diode is used as the indicator. It has been reported that body diode is a reliable junction temperature indicator regardless of external electro-thermal stresses. However, to accurately utilize it as TSEP, the setup cannot inject any large current to heat up the device during Tj measurement. In our test, a small reverse injected current (100mA) is used to obtain body diode forward voltage. On the other hand, to measure the case temperature, a TI thermal couple (LM60) is tightly attached to the back side

of the sample with a clipper. The thermal couple is calibrated first in the forced air oven so that the case temperature reading can be trustworthy.



(a) (b)

Figure 7.5. (a) Heating/Cooling Curve and (b) transient thermal network of SiC MOSFET

A MATLAB based thermal transient fitted model is developed as shown in Figure 7.5, the least square fit is used to extract lumped thermal model from device cooling/heating curve. Through curve fitting to the thermal transient, R and C in lumped thermal model can be calculated. Therefore, the rise of junction temperature above ambient can be calculated in real-time.

7.4 Lifetime Model Extraction

The output profile from previous subsystem of thermal conductivity is supposed to be calculated junction temperature profile. In the developed health analyzer toolbox, the acquired junction temperature is fed back to the input of power loss calculation subsystem and in real-time, power loss can be updated. Hence, power loss, as a junction temperature related parameter can be evaluated. The toolbox system developed in MATLAB/Simulink is shown in Figure 7.6.

As shown, two main blocks and subsystems is implemented in the system. As discussed, one is power loss evaluation and the other one is thermal network. In Simulink platform, all data and variables are based on time scale and simulated in time series. However, as discussed, package related lifetime is related to thermal swings, other than stress time. The output T_j profile is exported to MATLAB workspace and script file with RUL estimation code is developed to transfer time domain based T_j to electro-thermal stresses. Hence in this section, lifetime model that need to be extracted from aging test and imported into the toolbox is introduced.

From above discussed aging mechanisms, device aging degradation type is categorized into two different level. One is the package related fatigue caused by T_j swing and the other one is the die related aging especially for gate oxide layer. Hence in this toolbox, two different tracks are implemented regarding different aging process.

1) Package Level Lifetime Estimation

For package degradation, junction temperature swing introduce fatigue to both bond-wire and die attachment. Coffin-Manson model is the most widely adopted model which is used to calculate lifetime.

$$N_f = a(\Delta Tj)^{-m} \tag{7.1}$$

In equation (7.1), N_f stands for device consumable thermal cycles, a and m are constant parameters acquired by accelerated aging test. For different devices, lifetime model is supposed to be different due to various device robustness and reliability. As can be observed, damage applied to the device is in exponential relationship with T_j swing amplitude. Once constant a and m are obtained from accelerated aging test (in this case, package degradation evaluation with power cycling), the specific lifetime model of device package can be integrated into the toolbox. In this project, Coffin-

Manson Model is used for TO-247 samples (C3M0120100K) to validate the toolbox. The specific power cycling test procedure and results will be presented in following subsection.

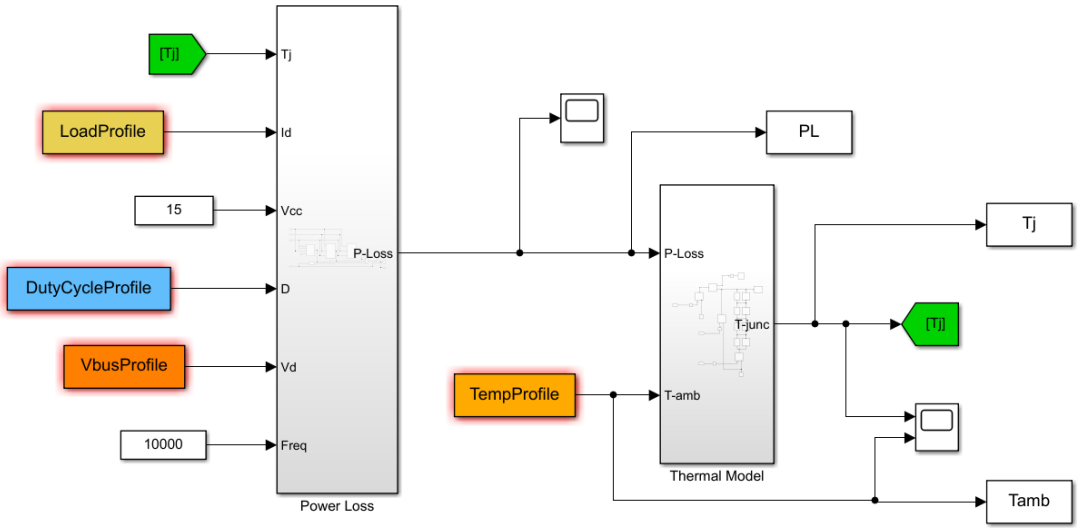


Figure 7.6. Developed toolbox in MATLAB/Simulink.

The Coffin-Manson model only considers temperature swing magnitude other than any other potential impact factors. Considering Schlumberger's application within high temperature environment, ambient temperature impact on reliability also requires extra attention. Hence, LESIT model is recommended.

2) Die Level Lifetime Estimation

Unlike package degradation mechanism which only count for temperature swing numbers, die related degradation can be accessed in time scale. As discussed, electro-thermal stress is applied to the device with gate-source bias voltage and elevated temperature. A widely used gate oxide layer lifetime is E-model [124]:

$$TF = A_o \exp(-\gamma E_{ox}) \exp(Q/K_B T) \tag{7.2}$$

Where TF stands for "time to failure", A_o, γ and Q/K_B are all constant values for each device. In this model, device junction temperature T and gate oxide layer E-field need to be extrapolated from mission profile and converter specs. E-field magnitude can be easily acquired from gate driver voltage applied to the device. In SLB's application and gate driver design, gate voltage is kept consistent at rate voltage (+15V), the specific lifetime model can be simplified and only junction temperature can be considered. Hence, equation (7.2) can be simplified as:

$$TF = A_1 \cdot \exp\left(Q/K_B T\right) \tag{7.3}$$

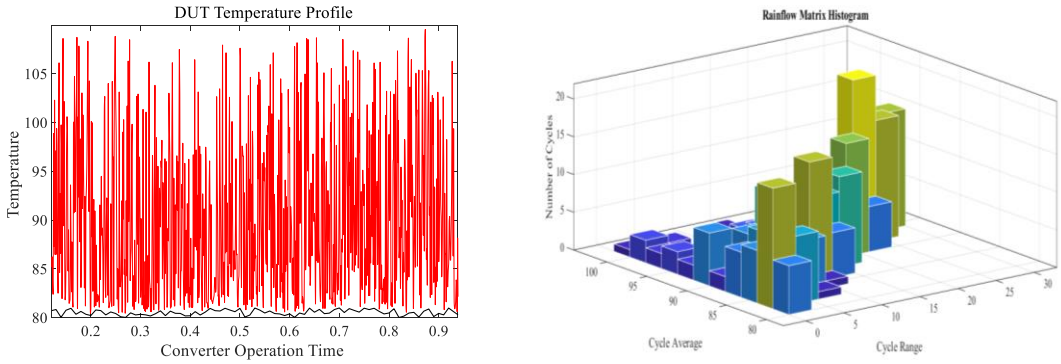
In other to obtain the lifetime constant A_1, HTGB test is conducted on DUTs. In die degradation RUL estimation track inside the toolbox, the accumulated damage can be calculated time step by time step based on Tj profile.

As discussed, unlike die related damage or lifetime prediction in time domain, the package related stress should be counted by thermal cycles instead of time. Hence, an extra step is needed for evaluating thermal stress applied to the device in system. Once the T_j profile is obtained from toolbox Simulink T_j estimation module, a thermal cycle counting method is needed to implement into the toolbox.

In this project, the most widely employed *Rainflow counting method* is used to transfer time based T_j profile into discrete cycles for each mission [125]. For illustration, a random defined T_j profile which is shown in Figure 7.7 (a) is counted into thermal cycles in Figure 7.7 (b). Hence in this way, the T_j profile in time domain is transferred to cycles. As shown in Figure 7.7 (b), thermal cycles are categorized into different temperature swing and mean temperature.

To calculate accumulated damage within certain mission duration, once T_j profile is extracted from the toolbox, all counted cycles within one T_j-swing and T_j-mean condition is used to calculate

corresponding damage. By adding all damage up for all counted thermal cycles, the total accumulated damage can be derived.



(a) Time based (b) Cycle based

Figure 7.7. Extrapolation of T_j profile in time domain.

CHAPTER 8

SUMMARY AND CONCLUSIONS

8.1 Conclusion and Contributions

This dissertation focuses on reliability assessment, condition monitoring and lifetime prediction of SiC MOSFETs. The whole study covers two main parts: test for reliability and design for reliability. In respect of test for reliability, main contributions are listed as follows:

- An overview of SiC MOSFET aging mechanisms and accelerated lifetime tests is carried out. Insights on selection of ALT type, aging test condition, aging precursors are addressed.
- An active channel gate bias test is proposed and developed to age SiC MOSFETs in accelerated manner close to realistic system operating conditions. A new degradation mechanism is observed, and device's lifetime is proofed to be shortened because of the actively conducted load current.
- Comprehensive evaluation and characterization on SiC MOSFET electrical parameters throughout multiple ALTs. Static parameters including $R_{ds\text{-}on}$ and V_{th} are verified to be strong aging precursors for package and chip degradation.
- Device switching transients over power cycling test are comprehensively analyzed and tested through double pulse tests. A retardation of turn-on speed and increased Miller plateau voltage are observed.
- SiC MOSFET degradation impact on system performance is investigated through conductive EMI testing on an 800W active PFC converter. Mitigation is observed for

both common-mode and differential-mode noise is observed due to device's slower switching speed.

In respect of design for reliability, main contributions are listed as follows:

- An on-board condition monitoring method is proposed using Miller plateau voltage. The developed plug-in circuit can be used to capture device's Miller platform in nanosecond resolution and an increment of 0.5V voltage increment can be measured over device's lifetime.
- Turn-on time-based condition monitoring is proposed for high resolution gate driver side sensing. The designed aging detection circuit and employs system microcontroller's readily available HR-capture module for low cost and excellent simplicity.
- A practical in-situ condition monitoring method is developed employing system readily available current/voltage sensors. The proposed method enables aging detection separately on chip and package levels. It is verified in case studies that the proposed solution can achieve accurate aging detection in various converter configurations.
- A SiC MOSFET lifetime estimation toolbox is designed and developed considering system mission profile. For comprehensive state-of-health estimation, both chip and package related device degradation are considered.

8.2 Future Work

Several aspects still need refinements and further investigations:

- Investigation on SiC MOSFET aging patterns and effects in wider range including bipolar degradation.

- Accuracy verification and refinement on lifetime estimation toolbox based on system mission profile.
- With the assistance of lifetime estimation, potential valid lifetime extension methods of SiC MOSFET need to be proposed to enhance system robustness in long term.

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BIOGRAPHICAL SKETCH

Shi Pu (S'17) received a BS degree from the School of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan, China, in 2014, and an MS degree from Auburn University, Auburn, AL, USA, in 2016, both in electrical engineering. He is currently working toward a PhD degree in electrical engineering with The University of Texas at Dallas, Richardson, TX, USA.

His research interests include wide-band-gap device reliability, device characterization, and real-time fault diagnosis.

CURRICULUM VITAE

Shi Pu

EDUCATION

PhD	***Electrical Engineering***	***The University of Texas at Dallas***	2016-2021
MS	***Electrical Engineering***	***Auburn University***	2014-2016
BS	***Electrical Engineering***	***Huazhong Univ. of Science and Technology***	2010-2014

RESEARCH AREA

- Static and switching (double pulse test) characterization of SiC device
- Reliability evaluation and condition monitoring of SiC device
- Smart gate driver design for SiC device
- EM noise evaluation for SiC based power converter
- Design and construction of power converters

RESEARCH EXPERIENCE

Prognostics and Health Management for Drilling System (*Schlumberger*)

Jun 2019 –Sep 2020

- Development of a lifetime prediction toolbox for SiC devices considering mission profile.
- Lifetime model extraction through accelerated aging tests.
- Electro-thermal model development for SiC MOSFET.

Fault Characterization and Degradation Monitoring of SiC MOSFETs *(Texas Instruments)*

Aug 2017 - Aug 2020

- Aging assessment and device characterization over lifetime.
- Develop a SiC based boost-PFC power converter to evaluate device aging effect on converter performance.
- Conducting double pulse tests for switching transient evaluation over lifetime.
- Development of condition monitoring circuits to detect device degradation.

PUBLICATIONS

SELECTED JOURNALS

[1]. **S. Pu**, E. Ugur, F. Yang and B. Akin, "In situ Degradation Monitoring of SiC MOSFET Based on Switching Transient Measurement," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5092-5100, June 2020.

[2]. **S. Pu**, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu and B. Akin, "A Practical On-Board SiC MOSFET Condition Monitoring Technique for Aging Detection," in *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2828-2839, May-June 2020.

[3]. F. Yang, **S. Pu**, C. Xu and B. Akin, "Turn-on Delay Based Real-Time Junction Temperature Measurement for SiC MOSFETs with Aging Compensation," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1280-1294, Feb. 2021.

SELECTED CONFERENCE PUBLICATIONS

[1]. **S. Pu**, E. Ugur and B. Akin, "Real-time degradation monitoring of SiC-MOSFETs through readily available system microcontroller," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 378-382.

[2]. **S. Pu**, E. Ugur, B. Akin and H. Akca, "Investigation of EM radiation changes in SiC based converters throughout device aging," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 190-194.

[3]. **S. Pu**, E. Ugur, F. Yang, C. Xu and B. Akin, "Thermally Triggered SiC MOSFET Aging Effect on Conducted EMI," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, 2018, pp. 51-55.

[4]. **S. Pu**, F. Yang, E. Ugur, B. T. Vankayalapati, C. Xu and B. Akin, "On-Board SiC MOSFET Degradation Monitoring Through Readily Available Inverter Current/Voltage Sensors," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1-5.

[5]. **S. Pu**, F. Yang, E. Ugur, C. Xu and B. Akin, "SiC MOSFET Aging Detection Based on Miller Plateau Voltage Sensing," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1-6.

AWARDS

2019	Student Travel Award	IEEE Transportation Electrification Conference and Expo