2013-01-11

Figure of Merit for and Identification of Sub-60 mV/Decade Devices

UTD AUTHOR(S): Massimo V. Fischetti

Figure of merit for and identification of sub-60 mV/decade devices

William G. Vandenberghe,[1,2,a)] Anne S. Verhulst,[1] Bart Sorée,[1,3] Wim Magnus,[1,3] Guido Groeseneken,[1,2] Quentin Smets,[1,4] Marc Heyns,[1,4] and Massimo V. Fischetti[5]
[1]*imec, Kapeldreef 75, B-3001 Leuven, Belgium*
[2]*Department of Electrical Engineering, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium*
[3]*Department of Physics, Universiteit Antwerpen, Groenenborgerlaan 171, B-2020 Wilrijk, Belgium*
[4]*Department of Material Science, Katholieke Universiteit Leuven, B-3001 Leuven, Belgium*
[5]*Department of Materials Science and Engineering, University of Texas Dallas, Richardson, Texas 75080, USA*

(Received 2 October 2012; accepted 13 December 2012; published online 11 January 2013)

A figure of merit I_{60} is proposed for sub-60 mV/decade devices as the highest current where the input characteristics exhibit a transition from sub- to super-60 mV/decade behavior. For sub-60 mV/decade devices to be competitive with metal-oxide-semiconductor field-effect devices, I_{60} has to be in the 1-10 μA/μm range. The best experimental tunnel field-effect transistors (TFETs) in the literature only have an I_{60} of 6×10^{-3} μA/μm but using theoretical simulations, we show that an I_{60} of up to 10 μA/μm should be attainable. It is proven that the Schottky barrier FET (SBFET) has a 60 mV/decade subthreshold swing limit while combining a SBFET and a TFET does improve performance. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4773521]

In the quest for low power devices, the metal-oxide-semiconductor field-effect (MOSFET) subthreshold swing (SS) limit, which measures 60 mV/decade at room temperature, presents a major obstacle. This SS limitation has motivated research towards transistor concepts which do not exhibit a limit on their subthreshold swing. Examples of devices without a 60 mV/decade limit are the tunnel field-effect transistor (TFET),[1] the impact ionization MOS (I-MOS),[2] the superlattice source FET (SSFET),[3] and the ferroelectric gate FET (FEFET).[4] We will refer to these devices as sub-60 devices.

Research towards sub-60 devices that can improve over the MOSFET has lead to publications reporting either record values of on-currents or record subthreshold swings of sub-60 devices.[5–9] But unfortunately, no good single figure of merit for sub-60 devices is available, which makes it difficult to compare different devices and assess the progress that is being made. Furthermore, the lack of a figure of merit hampers the identification of real candidates for the succession of the MOSFET as a low power device.

In this paper, we propose a figure of merit for sub-60 devices (I_{60}) accounting for both a good swing *and* a good on-current. We show theoretical predictions of I_{60} for TFETs and give an overview of experimentally obtained TFET values. We present a proof that the Schottky barrier FET (SBFET) is not a sub-60 device and show that combining a SBFET and a TFET does not improve sub-60 device performance, contrary to previous claims.[10] We also briefly discuss other sub-60 devices and their performance.

The new device figure of merit we propose here is the highest source-drain current, I_{60}, where the current exhibits a transition from sub-60 to super-60 behavior with respect to gate bias as illustrated in Figs. 1 and 2. The current at which the transition from sub- to super-60 behavior takes place changes with applied drain bias and typically improves as drain bias is increased until it saturates to a maximal value (I_{60}) at large drain bias (Fig. 3). The useful current span will typically be limited by another super-60 to sub-60 transition at low source-drain current levels, induced by an ambipolar current or a source-drain leakage current. By its definition, I_{60} is independent of the workfunction of the gate metal and I_{60} also does not rely on an arbitrary choice of a transistor on- or off-current.

In order for sub-60 devices to be competitive with MOSFETs, I_{60} must ideally be only an order of magnitude below the required on-state current and at least be significantly larger than the required off-state current. A typical off-state current requirement for MOSFETs is of the order of 10^{-4} μA/μm for low-standby power and 10^{-2} μA/μm for low operating power applications, while on-currents well exceeding 100 μA/μm are expected. In the MOSFET, the current at the threshold voltage is usually 1 μA/μm so to be

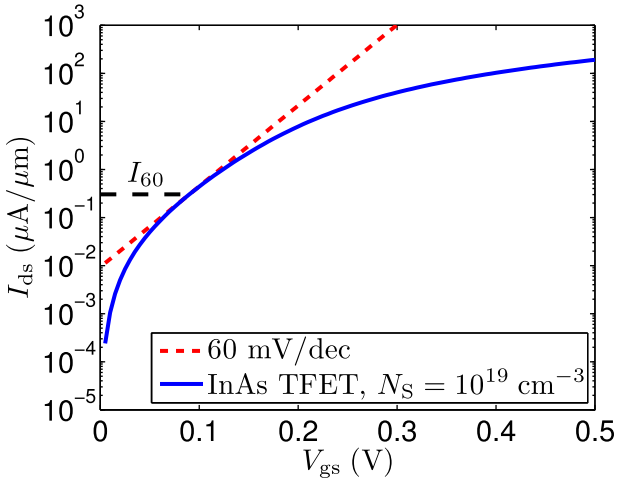

FIG. 1. Illustration of I_{60} in a direct semiconductor TFET with gate over the source (Fig. 4) with $V_{ds} = 0.4$ V. Current is calculated as outlined in Ref. 11.

[a)]Current address: The University of Texas at Dallas, Richardson, Texas 75080, USA. Electronic mail: william.vandenberghe@utdallas.edu.

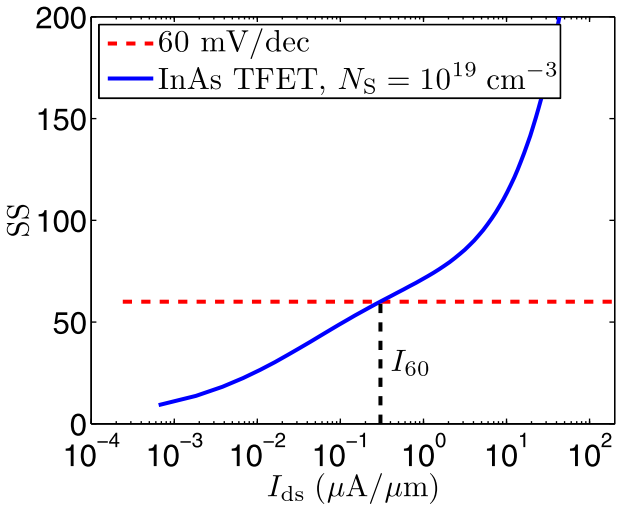

FIG. 2. Definition of I_{60}: current for which the subthreshold swing equals 60 mV/decade. Same TFET configuration as used in Fig. 1.

competitive with MOSFETs, sub-60 devices with an I_{60} in the range of $1-10\,\mu A/\mu m$ are desired.

The most promising sub-60 device at the moment is the TFET. The TFET relies on band-to-band tunneling and in a *n*(*p*)TFET, the valence(conduction) band edge cuts off the thermal carrier tail enabling sub-60 operation, which has been experimentally proven for both the n- and pTFETs.[8,9,12,13] The I_{60} of the experimental sub-60 TFET characteristics presented by Gandhi *et al.*[8] is $2\times10^{-6}\,\mu A/\mu m$, for the characteristics of Krishnamohan *et al.*[5] $10^{-5}\,\mu A/\mu m$, for the characteristics of Jeon *et al.*[14] $10^{-4}\,\mu A/\mu m$, for the characteristics of Ganjipour *et al.*[12] $10^{-5}\,\mu A/\mu m$, for the characteristics of Kim *et al.*[15] $3\times10^{-5}\,\mu A/\mu m$, and for the characteristics of Dewey *et al.*[13] $3\times10^{-3}\,\mu A/\mu m$. The best TFETs in the literature show $I_{60}=6\times10^{-3}\,\mu A/\mu m$ for the *n*TFET (Tomioka *et al.*[16]) and $I_{60}=4\times10^{-4}\,\mu A/\mu m$ the *p*TFET (Gandhi *et al.*[9]).

I_{60} is not only affected by the intrinsic sub-60 capability of a device but also by the maturity of the MOS technology. Some TFETs with a promising on-current demonstrate a high on-current but limited or no sub-60 behaviour, which is attributed to either poor quality of the semiconductor-

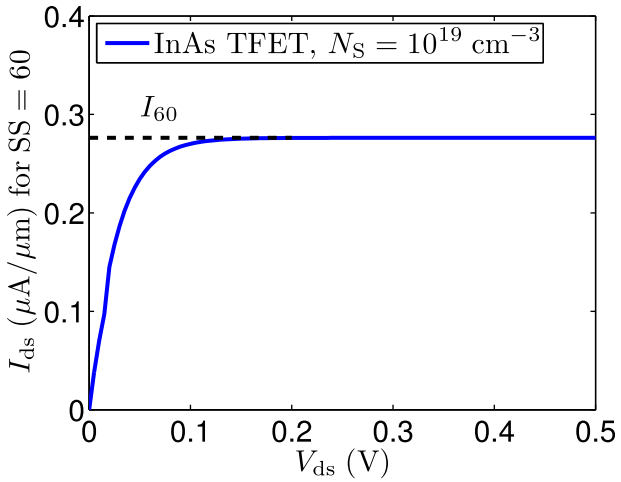

FIG. 3. Current level at the transition of sub-60 to super-60 behavior as a function of V_{ds}.

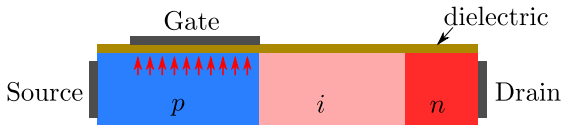

FIG. 4. Illustration of the TFET with the gate over the source only. A gate length of 10 nm and effective oxide thickness (EOT) of 1 nm is used unless specified otherwise.

dielectric interface or high bulk defect density. For these devices, a simple determination of I_{60} is insufficient to assess the promise of the prototype. Nevertheless, a device without I_{60} or with a low I_{60} can only be considered promising if there is a clear route towards an improved I_{60}.

To get a theoretical estimate of the attainable values, we assume a TFET configuration with its gate over the source as schematically shown in Fig. 4. This configuration exhibits a steeper subthreshold swing and therefore a higher drive current for a given supply voltage than the same structure with its gate extending over the channel.[17] We use the approach to calculate the current outlined in Ref. 11, where the current is calculated by integrating the tunneling probability over all available states, properly taking perpendicular momentum into account, and weighing with the Fermi-Dirac distribution determining occupation of the valence and the conduction band. As shown in Fig. 5, for InAs and InSb, an I_{60} of $1\,\mu A/\mu m$ is predicted at optimal doping while for materials with a higher density of states, an I_{60} of $10\,\mu A/\mu m$ should be attainable motivating more research towards heterostructures such as the InAs/Si combination.[16,18,19]

Another device which is investigated in the search for sub-60 devices is the Schottky barrier FET, whose operation is based on tunneling from a metal towards the conduction or valence band of a semiconductor (Fig. 6). Contrary to the TFET, the thermal tail of the carrier distribution is not cut

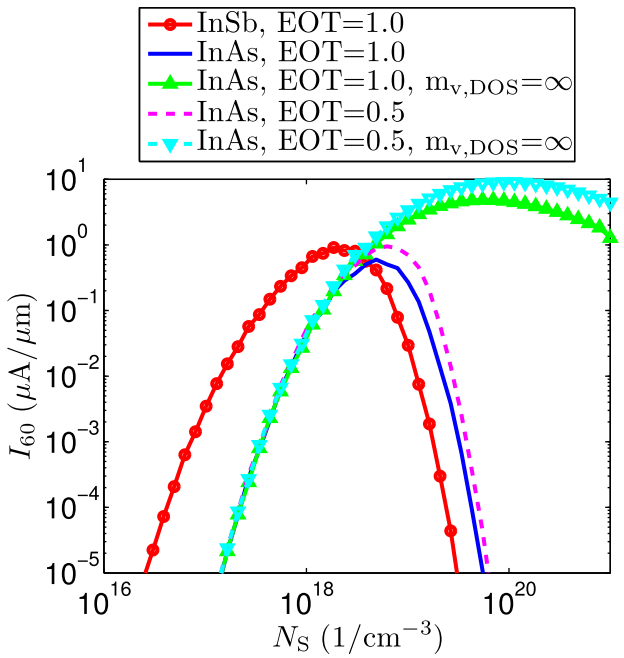

FIG. 5. Theoretical calculation of I_{60} for different materials, different EOT, and different density of states as a function of doping concentration for a TFET with the gate over the source using Eqs. (1)–(5) from Ref. 11.

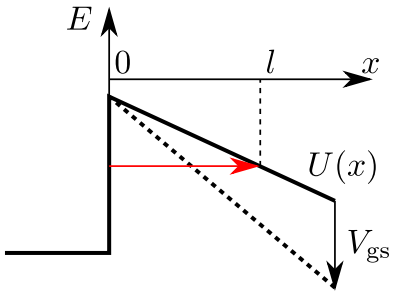

FIG. 6. Illustration of the SBFET working principle for tunneling to the conduction band. The gate bias modulates the potential energy $U(x)$ and the tunnel barrier length (l).

off and ambiguity exists in the literature about whether the SBFET is sub-60 or not.[20,21] In the following paragraphs, we present a rigorous proof that the SBFET SS cannot break the 60 mV/decade limit. We use the ballistic current picture (Eq. (2)) and the WKB approximation (Eq. (3)).

The subthreshold swing is defined by the ratio of the current and the transconductance multiplied by log(10)

$$SS = \log(10)\left|I_{ds}\left(\frac{dI_{ds}}{dV_{gs}}\right)^{-1}\right|. \tag{1}$$

In the ballistic picture, the current is calculated from

$$I_{ds,SB} = \frac{2q}{\hbar}\int \frac{dE}{2\pi} T_{SB}(E)(f_L(E) - f_R(E)) \tag{2}$$

with $f_{L,R}(E)$ the Fermi-Dirac distribution associated with the left and the right side contact and in the WKB approximation, the tunneling probability can be calculated from

$$T_{SB}(E) = \exp\left(-2\int_0^l dx\sqrt{\frac{2m^*(U(x)-E)}{\hbar^2}}\right), \tag{3}$$

$$= \exp(F_{WKB}(E)), \tag{4}$$

where the tunneling probability reduces to 1 for energies exceeding the top of the barrier. The transconductance for the SBFET is given by

$$\frac{\partial I_{ds,SB}}{\partial V_{gs}} = \frac{2q}{\hbar}\int \frac{dE}{2\pi}\frac{\partial T_{SB}(E)}{\partial V_{gs}}(f_L(E) - f_R(E)). \tag{5}$$

The derivative of the tunneling probability is determined by the derivative of the argument of the exponential determining the tunneling probability

$$\frac{\partial F_{WKB}(E)}{\partial V_{gs}} = -2\frac{\partial\int_0^l dx\sqrt{\frac{2m^*(U(x)-E)}{\hbar^2}}}{\partial V_{gs}}, \tag{6}$$

$$= -2\int_0^l dx\sqrt{\frac{m^*}{2\hbar^2(U(x)-E)}}\frac{\partial U(x)}{\partial V_{gs}}. \tag{7}$$

The tunnel path length is a function of the selected energy E, at which the tunneling probability is calculated, and the applied gate bias (V_{gs}) changing the potential energy $U(x)$ inside the SBFET. The change in potential inside the device $-U(x)/q$ can, however, never exceed the change in gate potential V_{gs}. As a result, $-dU(x)/d(qV_{gs}) \le 1$ and

$$\frac{\partial F_{WKB}(E)}{\partial V_{gs}} \le 2q\int_0^l dx\sqrt{\frac{m^*}{2\hbar^2(U(x)-E)}} \tag{8}$$

$$= q\frac{dF_{WKB}(E)}{dE}. \tag{9}$$

Substituting Eq. (9) into Eq. (5) using Eq. (4) yields

$$\frac{\partial I_{ds,SB}}{\partial V_{gs}} \le \frac{2q^2}{\hbar}\int \frac{dE}{2\pi}\frac{dT_{SB}(E)}{dE}(f_L(E) - f_R(E)), \tag{10}$$

integration by parts results in

$$\frac{\partial I_{ds,SB}}{\partial V_{gs}} \le -\frac{2q^2}{\hbar}\int \frac{dE}{2\pi}T_{SB}(E)\frac{d(f_L(E) - f_R(E))}{dE}, \tag{11}$$

and finally using the definition of the Fermi-Dirac distribution leads to

$$\frac{\partial I_{ds,SB}}{\partial V_{gs}} \le \frac{2q^2}{\hbar}\int \frac{dE}{2\pi}T_{SB}(E)\frac{f_L(E) - f_R(E)}{kT}. \tag{12}$$

Now using Eqs. (1) and (2) once again yields $SS \ge \log(10)kT/q$ q.e.d.

A combination of a TFET and a high on-current SBFET has been proposed as a solution to the low TFET on-current.[10] However, the combination of the TFET and the SBFET can never have an average sub-60 swing and the off-current is degraded with respect to the SBFET itself as illustrated in Fig. 7. Our figure of merit captures the lack of improvement in sub-60 operation as I_{60} does not improve for the TFET/SBFET combination.

The use of a ferro-electric gate material presents a possible way to obtain sub-60 behavior. Rusu *et al.*[22] showed an experimental demonstration of sub-60 behavior but did not specify a normalized current. MOSFETs with a superlattice source have been proposed as sub-60 devices[3] but have not been experimentally demonstrated yet.

I-MOS devices have experimentally been shown to exhibit sub-60 behavior. However, I-MOS operates based on

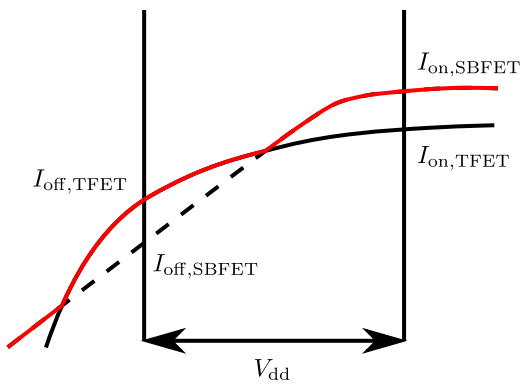

FIG. 7. Illustration of current of a SBFET + TFET. $I_{on} = I_{on,SBFET}, I_{off} = \max(I_{off,TFET}, I_{off,SBFET}) = I_{off,TFET}$. SBFET + TFET average swing is limited to 60 mV/decade.

the principle of avalanching which means an electron in the conduction band gains an energy larger than the bandgap over a short distance, transfers this energy to a second electron, exciting this second electron from the valence band to the conduction band. This means the I-MOS can only show sub-60 behavior when the drain-source voltage exceeds the bandgap. In I-MOS circuits, each I-MOS will have a voltage drop of at least one bandgap, even in the on-state while the voltage drop vanishes in MOSFETs and other sub-60 devices in the on-state. The non-vanishing voltage drop is a major disadvantage for I-MOS circuits and without the ability to efficiently build circuits, the I-MOS cannot be considered a possible candidate for future low-power applications.

In conclusion, we have proposed a new figure of merit for sub-60 devices I_{60} which should be in the $1-10\,\mu A/\mu m$ range to be competitive with conventional MOSFET technology. The TFET is currently the most promising sub-60 device although the best experimental TFET in the literature only realizes an I_{60} of $6\times10^{-3}\,\mu A/\mu m$, falling short of the MOSFET requirements. However, simulation shows that in an optimized direct semiconductor TFET with its gate over the source, an I_{60} of up to $10\,\mu A/\mu m$ can be reached. The SBFET was proven not to be a sub-60 device and a combination of a TFET and a SBFET does not present an improvement. The I-MOS cannot be considered a successor for the MOSFET while more experimental and theoretical results are needed for the SSFET and the FEFET before their potential can be assessed.

William G. Vandenberghe gratefully acknowledges the support of a Ph.D. stipend from IWT-Vlaanderen. The authors thank Danielle Leonelli, Lars-Åke Ragnarsson, and Krishna Bhuwalka for useful discussions. This work was supported by imec's Industrial Affiliation Program.

[1]P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weis, D. Schmitt-Landsiedel, and W. Hansch, Solid-State Electron. **48**, 2281 (2004).
[2]K. Gopalakrishnan, P. Griffin, and J. Plummer, in *International Electron Devices Meeting, 2002, IEDM'02* (2002), pp. 289–292.
[3]E. Gnani, P. Maiorano, S. Reggiani, A. Gnudi, and G. Baccarani, in *2011 IEEE International Electron Devices Meeting (IEDM)* (2011), pp. 5.1.1–5.1.4.
[4]S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008).
[5]T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, in *IEEE International Electron Devices Meeting, IEDM 2008* (2008), pp. 1–3.
[6]F. Mayer, C. Le Royer, J.-F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, in *IEEE International Electron Devices Meeting, IEDM 2008* (2008) pp. 1–5.
[7]D. Leonelli, A. Vandooren, R. Rooyackers, A. S. Verhulst, S. D. Gendt, M. M. Heyns, and G. Groeseneken, Jpn. J. Appl. Phys., Part 1 **49**, 04DC10 (2010).
[8]R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, IEEE Electron Device Lett. **32**, 437 (2011).
[9]R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, IEEE Electron Device Lett. **32**, 1504 (2011).
[10]L. Lattanzio, A. Biswas, L. D. Michielis, and A. M. Ionescu, Appl. Phys. Lett. **98**, 123504 (2011).
[11]W. G. Vandenberghe, A. S. Verhulst, K.-H. Kao, K. D. Meyer, B. Sorée, W. Magnus, and G. Groeseneken, Appl. Phys. Lett. **100**, 193509 (2012).
[12]B. Ganjipour, A. W. Dey, B. M. Borg, M. Ek, M.-E. Pistol, K. A. Dick, L.-E. Wernersson, and C. Thelander, Nano Lett. **11**, 4222 (2011).
[13]G. Dewey, B. Chu-Kung, J. Boardman, J. Fastenau, J. Kavalieros, R. Kotlyar, W. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. Then, and R. Chau, in *2011 IEEE International Electron Devices Meeting (IEDM)* (2011), pp. 33.6.1–33.6.4.
[14]K. Jeon, W.-Y. Loh, P. Patel, C. Y. Kang, J. Oh, A. Bowonder, C. Park, C. Park, C. Smith, P. Majhi, H.-H. Tseng, R. Jammy, T.-J. Liu, and C. Hu, in *2010 Symposium on VLSI Technology (VLSIT)* (2010), pp. 121–122.
[15]S. H. Kim, H. Kam, C. Hu, and T.-J. K. Liu, in *2009 Symposium on VLSI Technology* (2009), pp. 178–179.
[16]K. Tomioka, M. Yoshimura, and T. Fukui, in *2012 Symposium on VLSI Technology (VLSIT)* (2012), pp. 47–48.
[17]K.-H. Kao, A. Verhulst, W. Vandenberghe, B. Soree, W. Magnus, D. Leonelli, G. Groeseneken, and K. De Meyer, IEEE Trans. Electron Devices **59**, 2070 (2012).
[18]A. Verhulst, W. Vandenberghe, K. Maex, S. De Gendt, M. Heyns, and G. Groeseneken, IEEE Electron Device Lett. **29**, 1398 (2008).
[19]K. Moselund, H. Schmid, C. Bessire, M. Bjork, H. Ghoneim, and H. Riel, IEEE Electron Device Lett. **33**, 1453 (2012).
[20]Q. Li, X. Zhu, D. Ioannou, J. Suehle, and C. Richter, in *Device Research Conference, DRC 2009* (2009), pp. 113–114.
[21]J. Knoch and J. Appenzeller, Phys. Status Solidi A **205**, 679 (2008).
[22]A. Rusu, G. Salvatore, D. Jimenez, and A. Ionescu, in *2010 IEEE International Electron Devices Meeting (IEDM)* (2010), pp. 16.3.1–16.3.4.