INTEGRATED GAN POWER CONVERSION: TOPOLOGY, RELIABILITY AND IMPLEMENTATION

by

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Dedicated to my family

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INTEGRATED GAN POWER CONVERSION: TOPOLOGY,

RELIABILITY AND IMPLEMENTATION

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The explosive growth of power electronics has resulted in high power demand and more stringent requirements on power conversion systems. When bridging an increasing high input voltage and a decreasing low output voltage, high step-down ratio power converters demand high power density, high reliability, and high integration level. Compared to classic silicon power devices, new arising gallium nitride (GaN) technology presents the superior figure of merits, and it is regarded as a more promising power device candidate to overcome these challenges. However, because of the high step-down conversion ratio and unique characteristics of GaN power devices, GaN-based dc-dc power conversions face new challenges. Thus, a series of integrated GaN power conversion topologies, schemes and implementations have been explored to address power density, reliability and integration challenges.

Firstly, a GaN-based double step-down (DSD) power topology is presented for direct 48V/1V power conversion. In order to realize closed-loop regulation of the DSD power converter, an adaptive ON- and OFF-time (AO^2T) control with elastic ON-time modulation is developed for both steady state regulation and transient response enhancement. To reinforce the dual-phase

operation reliability of the DSD converter, a master-phase mirroring technique enables adaptive master-slave phase operation, accomplishing automatic phase current balancing.

Secondly, to improve the system reliability of automotive electronics, a low EMI noise high step-down ratio GaN-based buck converter is designed for direct battery-to-load power conversion. It employs an anti-aliasing multi-rate spread-spectrum modulation (MR-SSM) technique to suppress EMI noise and an in-cycle adaptive zero-voltage switching (ZVS) technique to minimize switching losses. Compared to the classic fixed-rate SSM (FR-SSM), the MR-SSM technique adaptively spreads EMI spectra in a wider frequency range without aliasing spikes and, thus, reduces peak EMI noise more effectively. To improve efficiency, an elastic dead-time (t_{dead}) controller facilitates in-cycle adaptive ZVS despite of a continuous switching frequency variation. For the enhancement of GaN power devices driving reliability, a pulse-reinforced level shifting technique is proposed to immune high switching node voltage dv/dt transition.

Thirdly, to enhance the GaN power device reliability of GaN-based power conversion system, an on-chip self-calibrated full-profile dynamic on-resistance sensing strategy is proposed to monitor the online healthy state of power devices. It achieves instant dynamic on-resistance sensing beyond megahertz. Moreover, complicated high-speed current sensing circuits are avoided to reduce implementation cost, and the random sensing errors are calibrated automatically for high sensing accuracy. The online state-of-health condition of GaN-based power converter is thus monitored comprehensively, precisely, and efficiently.

Finally, one monolithic integrated e-mode GaN asymmetrical half-bridge (AHB) power converter is implemented for direct 48V/1V power conversion, which minimizes non-ideal parasitics, enhances power conversion reliability, and reduces system complexity significantly. In the AHB

converter, an auto-lock auto-break (A^2) level shifting technique is developed to address the challenges of pull-up performance, device breakdown risk and dv/dt immunity at switching node voltage. The self-bootstrapped hybrid (SBH) gate driving technique adaptively achieves rail-to-rail dynamic gate driving in normal operation and robust static gate driving during large transients. The on-die temperature sensing facilitates hot spot monitoring and thermal management for high reliability.

In this dissertation, all the proposed GaN dc-dc power converters have been fabricated and tested to demonstrate the proposed system topologies, control schemes, circuit techniques. The measurement results successfully validate the effectiveness of the designs. The high switching frequency, low EMI noise, high reliability, and monolithic integration have been verified to enable GaN dc-dc power conversions.

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CHAPTER 1

BACKGROUND AND MOTIVATION

This chapter introduces the background, motivation, and contributions of this PhD dissertation study. Owing to the proliferative development of power electronics, high-performance power conversion systems are highly desired to deliver the explosive power demand. When converting a high input voltage (V_{IN}) to a low output voltage (V_O), the high step-down ratio power conversion circuits are required for high power density, high efficiency, high reliability and high integration level. On the other hand, as key components in power circuits, power switches affect the power conversion performance greatly. Compared to classic silicon power transistors, arising gallium nitride (GaN) high-electron-mobility transistors (HEMTs) accomplish superior figure of merits (FOMs), enabling the power converter to operate at high switching frequency (f_{SW}) and to consume low power loss. Accordingly, Section 1.1 provides the motivation of integrated GaN power conversion, which is targeted for high power density and high efficiency. Section 1.2 explains major design challenges, in terms of f_{SW}, power density, circuit topology, electromagnetic interference (EMI), GaN power devices reliability, and system integration. To overcome these challenges, the main objectives of this study are to develop advanced GaN power conversion topologies, control schemes, circuit techniques and implementation methods, which are elaborated in Section 1.3. Finally, the organization of the dissertation is described in Section 1.4.

1.1 Motivation of Integrated GaN Power Conversion

The global power electronics market size is projected to increase from $37.4 billion in 2021 to $46.3 billion by 2026, with a compound annual growth rate (CAGR) of 4.4% [MAM-21]. Such

a market growth has been attributed to the integrations of automotive, consumer, and industrial power electronics. Because of the variable power sources and specific supply voltages of electronic devices, a large number of power conversion circuits are needed to bridge different voltage rails. When delivering highly increased power, it becomes crucial to improve the performance of power conversion systems for low power and area cost. For example, as the automotive industry advances towards higher levels of electrification, there has been ever-growing power demand, which imposes unprecedented challenges on power density and reliability of power delivery systems [TI-14]. The main power source comes from the automotive battery, the voltage of which can be 12V, 24V or 48V in future vehicles, while the supply voltage of automotive electronics can be as low as 1V or even sub-V. To convert the high automotive battery voltage to the stable low voltage, efficient and robust power conversion circuits are indispensable for the automotive electronic systems. Conventionally, multi-stage power conversion structures are employed for power delivery. With ever-increasing power density, the single-stage power conversion structure has rapidly emerged as a promising candidate. Historically, an effective way to improve the power density of a power converter is to increase its f_{SW}. As shown in Figure 1.1, with a higher f_{SW}, the charge stored in power passives (inductors and capacitors) can be released to load more frequently, thus facilitating the use of smaller power passives, which are the dominant factors to power density. In addition, high f_{SW} operation is also beneficial for fast transient response, making it possible to meet stringent dynamic performance with small output capacitors. However, increasing f_{SW}, especially with high V_{IN} and low V_O, comes at the high cost of efficiency, as the switching power loss of power switches would rise drastically. As a remedy, more efficient GaN HEMTs can be adopted in replacement of conventional silicon power switches. For the same blocking

voltage, the parasitic capacitances and on-resistance of GaN HEMTs are much smaller than those of silicon counterparts [Lidow-15, Huang-17, Quinn-17]. Thanks to the superior FOMs of GaN HEMTs, integrated GaN power converters can operate more efficiently with higher f_{SW} and higher power density. Accordingly, GaN power devices have seen a bright future in the power electronics market, with a projected CAGR of 70% from 2020 to 2026 [Yole-21].

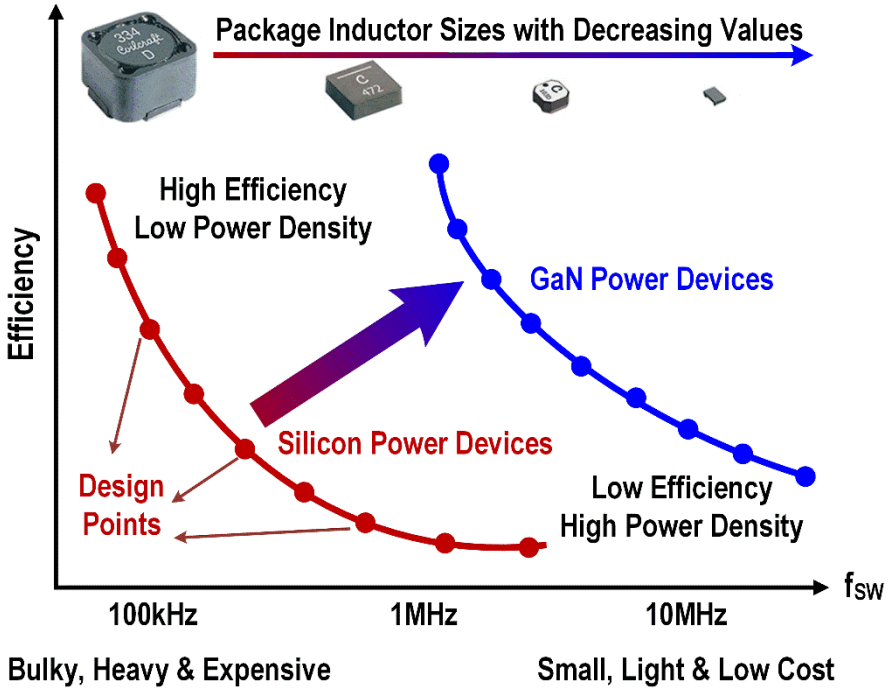


Figure 1.1. Illustrations of the relations among f_{SW}, power density and efficiency.

1.2 Design Challenges of High Step-Down Raito GaN Power Conversion

As discussed in the previous section, advantages of GaN HEMTs, including fast switching, low on-resistance and small parasitic capacitances, enable GaN power converters as encouraging candidates for high step-down ratio dc-dc power conversion. However, due to the high step-down conversion ratio and special properties of GaN HEMTs, new topology, reliability and integration challenges arise correspondingly in the high step-down ratio integrated GaN power converters.

1.2.1 Switching Frequency Challenges of High Step-Down Raito GaN Power Conversion

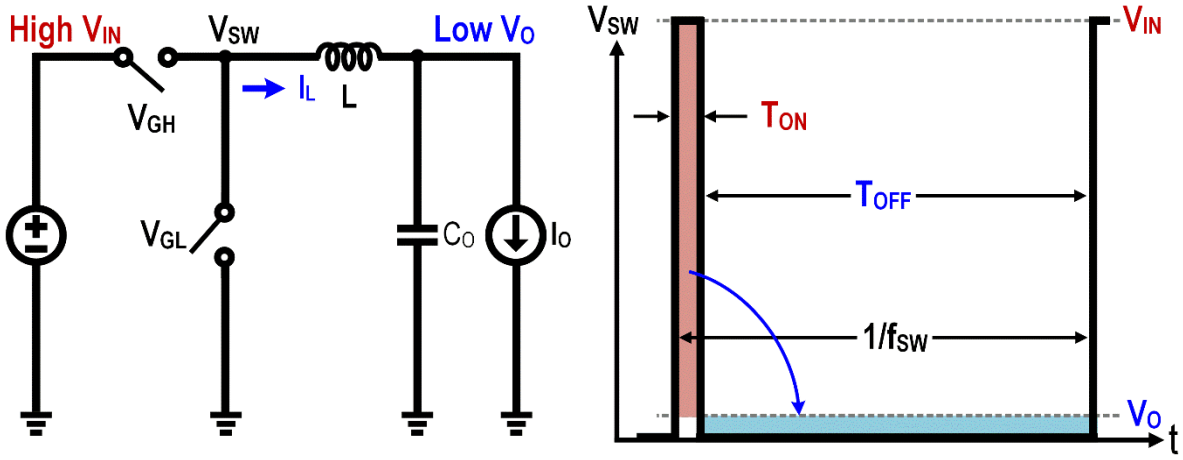


Figure 1.2. Illustration of high V_{IN}/V_O conversion in a half-bridge power converter.

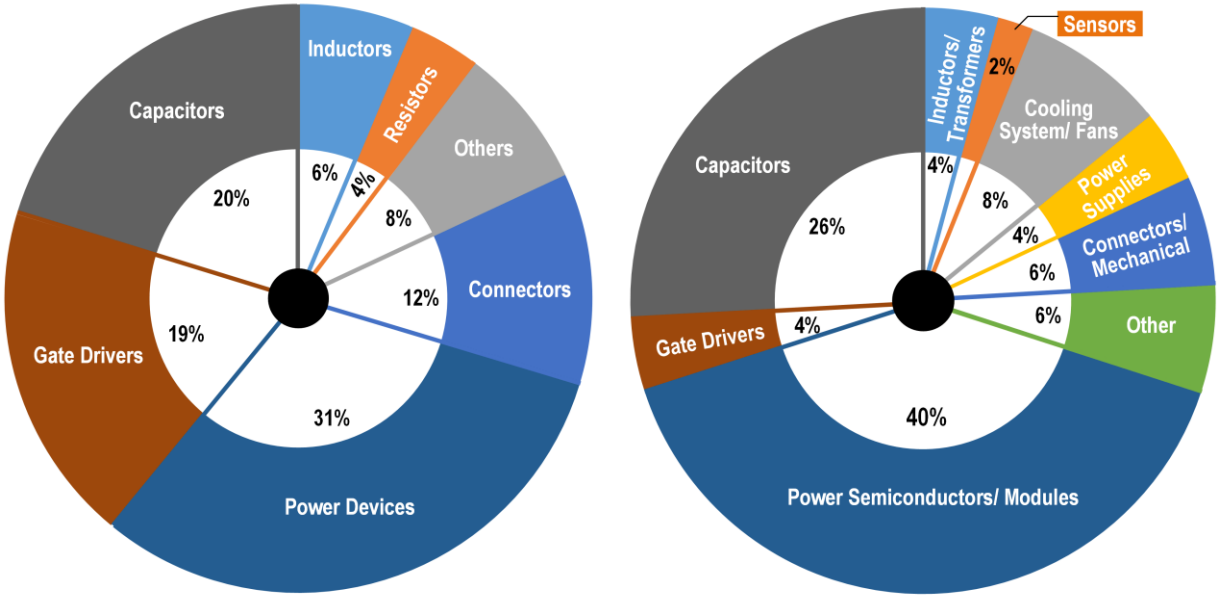
Although the superior GaN HEMTs can be used to reduce the power loss generated by power switches, there are still fundamental constraints on the implementation of a high f_{SW} high V_{IN}/V_O power conversion. Taking the most mature and widely used half-bridge power converter in Figure 1.2 for example, it is composed of two power switches, one inductor and one output capacitor. By controlling high- and low-side power switches, the switching node voltage V_{SW} transits between zero and V_{IN}. With the passive inductor and capacitor filter, one stable V_O is generated. When V_{SW} rises to V_{IN} during the on-duty period T_{ON}, the voltage across the inductor L equals $(V_{IN}-V_O)$, and the inductor is energized. When V_{SW} falls to zero during the off-duty period T_{OFF}, the voltage across L becomes $-V_O$. The inductor energy will be discharged to power the load. In each switching cycle of steady state, the charged and discharged energy of the inductor are equal. Since $(V_{IN}-V_O)$ is significantly much higher than V_O, T_{ON} has to be much lower than T_{OFF}. To achieve high f_{SW}, the value of T_{ON} has to be narrowed extremely due to the large imbalance between T_{ON} and T_{OFF}. Such a narrow T_{ON} would be comparable and sensitive to any delay

elements of feedback control and driving circuits, inducing more circuit design difficulties. Therefore, more advanced and sophisticated power conversion topologies are in high demand for high step-down ratio GaN power converters.

1.2.2 EMI Noise Challenges of High Step-Down Raito GaN Power Conversion

In the electronic system, the electronic devices would be vulnerable to EMI noise, which is typically generated by the switching power converters [Natarajan-20]. The disturbing noise would affect the normal operations, challenging the designs for robust electronic systems. To maintain the safety and reliability of the electronic system, specific electromagnetic compatibility (EMC) standards have to be reinforced strictly. For instance, when converting a high voltage to a low voltage power output, a single-stage GaN power converter is promising to decrease the cost with smaller footprints. But its f_{SW} is constrained low due to the high step-down conversion ratio, inducing large EMI noise at the low frequency range. Furthermore, the large dv/dt and di/dt transients would aggravate EMI noise. Conventionally, passive filters with discrete inductors and capacitors are used to reduce EMI noise [TI-13]. However, they would lead to extra area penalties, nullifying the effort of power density improvement. In terms of control techniques, spread-spectrum modulation (SSM) can be applied in a power converter to attenuate EMI noise. By spreading the switching frequency continuously in a specific range, the peak EMI noise spikes can be attenuated. But its reduction performance is limited because of the constrained low f_{SW}. Moreover, the SSM techniques will increase power loss to degrade efficiency. Hence, effective and efficient EMI suppression techniques are in urgent demand for high step-down ratio GaN power converters.

1.2.3 Reliability Challenges of GaN Power Conversion



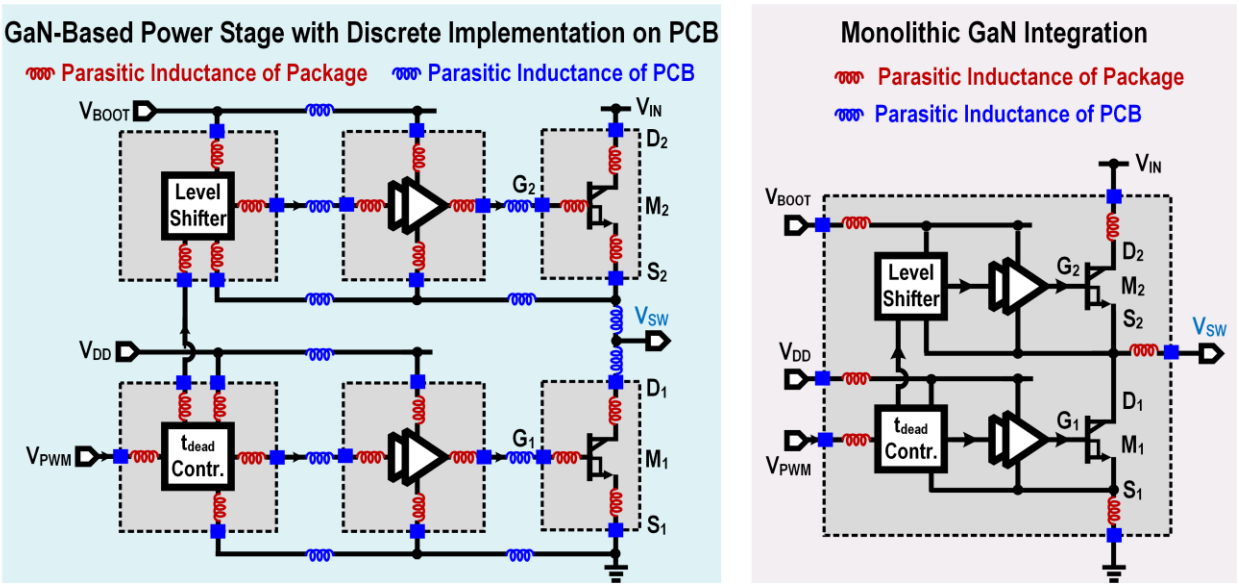
(a) (b)

Figure 1.3. Fragile components in power electronic systems: (a) survey in 2008 [Yang-09], and (b) survey in 2018 [Falck-18].

Many research works have been carried out to improve power density and efficiency with GaN HEMTs. But the corresponding reliability and stability problems are still major hurdles to their widespread adoptions. Furthermore, the reliability requirements of power electric systems have been raised greatly due to the advancing safety-critical and mission-critical applications [Oh-15]. A typical power electronic system is mainly composed of power devices, capacitors, magnetics, controllers and so on. The failure of a single part could result in a catastrophic blackout, long downtime, and high maintenance cost [Peyghami-21]. Among these components, power devices are becoming increasingly important for the entire system's reliability. According to the survey in 2008, Figure 1.3(a) shows that power devices are regarded as the most fragile components [Yang-09]. Following the survey in 2018, power semiconductors and modules are

ranked the most crucial elements for system reliability, which are summarized in Figure 1.3(b) [Falck-18]. Compared to the mature silicon power devices, the newly emerging GaN HEMTs face more reliability challenges due to the less well-studied structures. When a GaN HEMT is switched at high voltage (HV) and high switching frequency, some electrons may get trapped in specific regions of the transistor structure. Following switching transients, these trapped electrons cannot be freed instantaneously when it is turned on. The on-state current capability by two-dimensional electron gas (2DEG) is thus reduced severely. The value of instant dynamic on-resistance (r_{on}) increases much higher than the static one, resulting in much higher conduction loss and lower efficiency. Since the excessive device self-heating would induce potential thermal failure, the dynamic r_{on} degradation is regarded as a major failure of GaN HEMTs [Bahl-16]. Thus, it becomes imperative to ensure high reliability of GaN HEMTs for robust GaN power converters. Conventionally, condition monitoring has been proven to be a cost-effective means of enhancing reliability. It assesses the health status of a system component and takes corrective actions before failure occurs. In order to monitor the healthy state of power devices, variable electrical parameters can be used as condition precursors, such as on-resistance, threshold voltage, gate leakage current and so on. Among these parameters, on-resistance can be a promising healthy signature of GaN HEMTs [Xu-18, Biglarbegian-18, Chen-21, Huang-20]. But because of its high switching frequency, high input voltage, and low on-state drain-source voltage operations, classic dynamic on-resistance sensing circuits suffer from slow sensing speed, low accuracy and high area and power cost. These challenges have resulted in growing demands for a comprehensive, accurate and efficient dynamic r_{on} sensing system, which facilitates online condition monitoring for GaN power devices.

1.2.4 Monolithic Integration Challenges of GaN Power Conversion



(a) (b)

Figure 1.4. GaN-based half-bridge power stage with: (a) discrete, and (b) monolithic implementation.

The superior FOMs of GaN HEMTs contribute to high power density and high efficiency power conversions. However, classic GaN power converters are typically implemented with discrete GaN power devices [Song-15, Chen-19, Yan-19, Ke-21]. These discrete solutions heavily rely on board- and package-level wiring and bonding to connect GaN HEMTs, power passives, gate drivers, level shifters, controllers and auxiliary modules. Taking a GaN-based half-bridge power stage in Figure 1.4(a) as an example, it is implemented with discrete GaN HEMTs, silicon gate drivers, silicon level shifter, and silicon dead-time (t_{dead}) controller on a printed circuit board (PCB). The non-ideal resistive and inductive parasitics of multiple packages and PCB wirings would drastically deteriorate the efficiency and reliability of GaN power converters. Besides, these discrete components cost more area, deteriorating the power density of converters. To fully utilize GaN technology merits, the monolithic integration of GaN power stage in Figure 1.4(b) becomes

appealing. By integrating all the circuits on one GaN chip, it can decrease the area cost for high power density, reduce non-ideal parasitics for high reliability, and increase implementation flexibility greatly. However, compared to the long-established silicon integrated circuit (IC) process, the monolithic GaN IC process is much less mature, challenging the implementation of monolithic GaN integration. Firstly, due to the shared conductive substrate in the GaN-on-Si process, it is hard to isolate the substrate of each device, and the generated crosstalk and back-gating effects limit the performance of monolithic GaN power converters [Jiang-14, Li-18b, Moench-21]. Besides, the monolithic GaN IC process only offers n-channel devices. The lack of p-type transistors prevents direct adoption of classic CMOS gate driving techniques and circuits, imposing unprecedented circuit design challenges. Without p-type transistors, key modules such as level shifters and gate drivers would lose effective pull-up mechanisms towards high voltage nodes such as supply voltages. It would cause potential control malfunction, long propagation delay, high conduction loss and high reliability risk. Thus, the newly proposed circuit design techniques and implementation methods are indispensable for monolithic integrated GaN power converters.

1.3 Research Goals and Contributions

The goals of this dissertation are to overcome the aforementioned challenges of high step-down ratio GaN power conversion. Specifically, power conversion topologies, system design strategies, operation schemes, control methods and circuit techniques are proposed for high step-down ratio integrated GaN dc-dc power conversion, as shown in Figure 1.5. These solutions improve the switching frequency, power density, efficiency, system and device reliabilities, and integration level significantly. The key research contributions are summarized below.

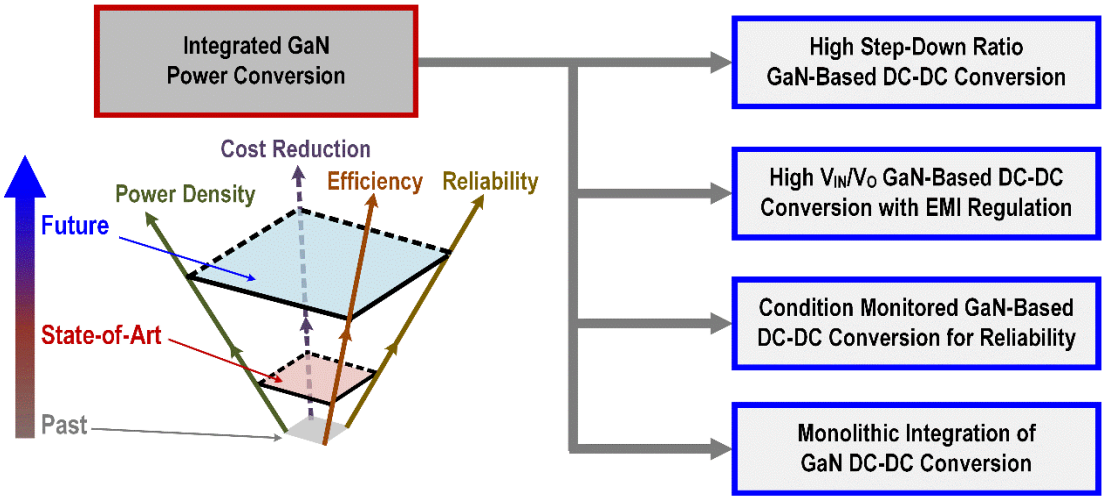


Figure 1.5. Summary of research contributions.

1) High Step-Down Ratio GaN-Based DC-DC Conversion

1.1) Employed a double step-down (DSD) architecture to realize direct 48V/1V power conversion and developed an adaptive ON-OFF time (AO^2T) control for the DSD topology. The DSD topology is divided as master sub-converter and slave sub-converter. In the closed-loop feedback controller, T_{ON} is actively controlled. The output voltage and master sub-converter inductor current are sensed and compared to determine T_{OFF} of the master sub-converter. In order to achieve phase synchronization of the two sub-converters, the master phase mirroring technique is proposed. The slave sub-converter reuses the same T_{ON} and tracks the master switching period within each switching cycle. Thanks to the inherent feedback mechanism of the DSD power stage, automatic phase current balancing is realized without extra control circuits [Yan-19, Yan-20a].

1.2) Developed an elastic ON-time modulation scheme to enable elastic T_{ON} modulation for fast dynamic transient response and to prevent the two sub-converters from T_{ON} overlapping for high reliability. The two sub-converters share one T_{ON} generation circuit to reduce

circuit complexity and ensure equal T_{ON}s of the two sub-converters. In steady state, the value of T_{ON} is stable to realize automatic phase current balancing, which requires the same f_{SW} and duty ratio of each sub-converter. During load transient, the instant output voltage undershoot or overshoot is sensed, and T_{ON} is modulated instantly. Compared to the classic constant ON-time (COT) control scheme, it improves the dynamic transient performance without compromising the static performance. Meanwhile, a compatible T_{ON} overlap prevention module employs digital logic circuits to activate T_{ON}s of master and slave sub-converters alternatively without disastrous T_{ON} overlapping [Yan-19, Yan-20a].

2) High V_{IN}/V_O GaN-Based DC-DC Conversion with EMI Regulation

2.1) Development of an anti-aliasing multi-rate spread-spectrum modulation (MR-SSM) strategy to control high V_{IN}/V_O GaN-based buck converter with low EMI noise. The converter consists of a half-bridge power stage with GaN HEMTs and is regulated by an active shaping controller for V_O regulation and EMI reduction. The developed anti-aliasing MR-SSM scheme adaptively controls the f_{SW} modulation rates for different f_{SW}s, achieving targeted EMI redistribution of high V_{IN}/V_O dc-dc power conversion. It effectively spreads f_{SW} in a wide range for further EMI reduction. Meanwhile, the potential EMI power aliasing spikes generated by the fundamental and harmonics of SSM range are also avoided. Compared to the classic fixed-rate SSM (FR-SSM), it can effectively reduce the aliasing spikes with the same SSM range, and thus improve EMI reduction performance without introducing extra cost [Yan-20b, Yan-21].

2.2) Developed an in-cycle adaptive zero-voltage switching (ZVS) technique, which senses the frequency variations during MR-SSM operation, predicts the upcoming inductor current

profile, and modulates t_{dead}s in each switching cycle. It maintains adaptive ZVS of power switches even though the MR-SSM generates continuously variable inductor current profile. Owing to the proposed active shaping controller, by actively modulating T_{ON}, T_{OFF} is adaptively synchronized with closed-loop regulation, achieving indirect f_{SW} modulation. The switching period T_{SW} is thus proportional to the actively modulated T_{ON}. Since the proposed elastic t_{dead} controller senses T_{ON} variation instantly, the upcoming peak and valley inductor currents can be predicted, and the V_{SW} falling and rising t_{dead}s are modulated accordingly. Therefore, V_{SW} falling and rising rates variations are compensated to achieve adaptive ZVS and maintain high efficiency [Yan-20b, Yan-21].

2.3) Development of a high switching node voltage V_{SW} dv/dt immunity level shifting technique to improve the driving reliability of GaN-based power converters. In the classic integrated level shifter, parasitic capacitances of HV isolated devices induce potential false triggers at the output of level shifter due to high V_{SW} dv/dt transition, deteriorating the reliability of driving circuits greatly. To enhance driving reliability, an energy efficient immunization technique is proposed to compensate the non-ideal coupling effects. The high V_{SW} dv/dt transition is sensed instantly, and one compensated transient current is applied in the logic calculation circuit to maintain the correct and robust output logic signal of level shifter [Yan-20b, Yan-21].

2.4) Developed adaptive operation modes to accommodate a wide load current range. In order to enhance the light load efficiency, one compatible discontinuous conduction mode (DCM) control is developed. Classic power converters with SSM techniques adopt a pulse width modulation (PWM) control scheme, which controls f_{SW} directly. When the load

current is low, the constant PWM control scheme would generate a large negative inductor current, inducing extra conduction loss and compromising efficiency severely. In contrast, the compatible DCM control is activated during light load condition, avoiding large negative inductor current, and maintaining high efficiency [Yan-20b, Yan-21].

3) Condition Monitored GaN-Based DC-DC Conversion for Reliability

3.1) Development of an on-chip self-calibrated full-profile dynamic r_{on} sensing strategy, which monitors the online condition of GaN-based power converter comprehensively. In order to sense the dynamic r_{on}*s* of all GaN HEMTs in GaN-based power converters, a high-speed clamping circuit is required to capture on-state drain-source voltage difference, accommodating high f_{SW} and blocking large off-state drain-source voltage. Due to the extremely low on-state drain-source voltage, the voltage sensing accuracy would be greatly affected by the random offset voltages. To improve the sensing accuracy, the proposed self-calibrated dynamic r_{on} sensing scheme automatically calibrates the sensing errors for high monitoring accuracy. Besides, high-speed and -resolution current sensing circuits are also avoided for implementation simplicity.

3.2) Development of a dual ON-time controlled GaN-based half-bridge buck converter to realize self-calibrated dynamic r_{on} sensing scheme. With two predefined T_{ON}*s* in two operation modes, two different f_{SW}*s* are synchronized automatically with closed-loop V_O regulation. The peak and valley inductor current differences between the two operation modes are constant regardless of variable load current (I_O). These inductor current differences can be used for dynamic r_{on} calculation, eliminating extra high-performance current sensing circuits and contributing to low cost. In addition, thanks to the dual ON-

time operation, there are power loss differences between the two operation modes. The period distribution ratio of the two operation modes can be adaptively adjusted, supporting active thermal control of the power converter for lifetime extension.

3.3) Developed fully integrated dynamic forward r_{on} sensors for high- and low-side GaN power switches, which are incorporated with a GaN-based half-bridge buck converter. The low-side GaN HEMT M_L forward r_{on} sensor is compatible with feedback control circuits, consuming very small area and power. The high-side GaN HEMT M_H forward r_{on} sensor uses one stable floating voltage rail to acquire dynamic on-state drain-source voltage of M_H in each switching cycle. The sensed voltage is then amplified and converted to low voltage domain for further signal processing.

3.4) Development of an event triggered (ET) dynamic reverse r_{on} sensor, which achieves both high sensing precision and low power loss. With the ET sensing scheme, a severe trade-off between long t_{dead} with high reverse conduction loss and short t_{dead} with large sensing errors is overcome. In normal operation, t_{dead} is kept short to minimize reverse conduction loss for high efficiency. Once the event triggering signal is occasionally enabled, t_{dead} is extended and the negative voltage sensing circuit is activated to sense reverse r_{on} of GaN HEMT.

3.5) Development of a dual-rail up-level shifter, which achieves both fast signal transmission and robust gate driving with two separated bootstrapped (BST) rails. One BST rail is employed to supply the power for gate driver, which drives the GaN HEMT directly. It is kept constantly below 5V to protect the gate driver and GaN HEMT from HV breakdown. The other BST rail is designed to supply the power of level shifter, ensuring large voltage

difference and fast signal transition. During t_{dead}, although a large negative V_{SW} is generated by the positive inductor current, the proposed up-level shifter maintains enough voltage difference for fast and reliable driving signal transmission.

4) Monolithic Integration of GaN DC-DC Conversion

4.1) Developed a monolithic integrated e-mode GaN asymmetrical half-bridge (AHB) power converter with synchronous rectifiers of a current doubler for direct 48V/1V power conversion. By integrating all the GaN power devices, gate drivers, up-level shifter, t_{dead} controller, temperature sensor on one GaN chip, the monolithic GaN converter significantly minimizes the area cost, reduces non-ideal parasitics, improves implementation flexibility and enhances reliability. In the monolithic GaN AHB converter, owing to the transformer turns ratio, the T_{ON} limitations in classic half-bridge power converters are overcome, enabling high V_{IN}/V_O conversion for high switching frequency and efficiency.

4.2) Developed an auto-lock auto-break (A^2) level shifting technique to transmit driving control signals between low voltage (LV) and HV domains. It successfully overcomes the pull-up challenges induced by the lack of p-type device in the monolithic GaN process. The logic circuits are also protected from HV breakdown and the output logic immunes high switching node voltage dv/dt transition without false triggers. It paves the way for monolithic GaN integration of switching power converters, in which the sources of the power devices are not constantly ground.

4.3) Development of a self-bootstrapped hybrid (SBH) gate driving technique to control GaN power switches, which achieves both rail-to-rail dynamic gate driving in normal operation

and robust static gate driving during start-up and load transient. With a single power supply, the SBH gate driver generates a rail-to-rail driving voltage for the GaN power switch, minimizing on-resistance of GaN power devices. Furthermore, it maintains robust static gate driving, ensuring high reliability of monolithic GaN converter. The realized short propagation delays support high f_{SW} operation of GaN power circuits and the low power loss contributes to high efficiency.

4.4) Developed an on-die temperature sensing technique in GaN-on-SOI process. The temperature sensor is integrated with the monolithic GaN power converter. It can monitor instantaneous hot spots of the power converter directly without disturbing the normal power conversion operations. Based on the sensed temperature, thermal protection of the monolithic GaN power converter can be realized for high reliability. Compared to classic temperature sensing techniques for discrete GaN devices, which sense temperature-sensitive electrical parameters with extra discrete sensing chips, the proposed design reduces the design complexity and improves sensing accuracy significantly.

1.4 Dissertation Organization

The rest of this dissertation is organized as follows. In Chapter 2, new arising GaN-based power conversions are discussed. It firstly introduces the structures of commercial GaN HEMTs. Then, the key characteristics of GaN HEMTs in power electronic applications are investigated. Finally, based on the GaN HEMTs, a series of step-down dc-dc power conversion circuits are illustrated.

Chapter 3 presents a GaN-based DSD power converter for direct 48V/1V power conversion. Firstly, the limitations on maximizing f_{SW} and efficiency of high step-down ratio power

conversion are analyzed. Aiming to increase the power density with high f_{SW} and low power loss, the DSD power topology shows more advantages over the classic half-bridge buck converter, and it is adopted in the design. Then the design challenges induced by its special operation scheme are discussed. The proposed master-slave AO^{2}T control is introduced to operate the DSD converter with high reliability and fast transient response. In the feedback controller, the operation scheme and circuit implementation of the master phase mirror are described to achieve clock-free phase synchronization and automatic current balancing of the two sub-converters in the DSD topology. After that, the operation scheme and circuit implementation of elastic ON-time modulation are explained to protect power switches from HV breakdown and to enhance dynamic transient performance. The design is implemented with a 180-nm HV bipolar, CMOS DMOS (BCD) process. The measurement results successfully validate the new control scheme and circuit design techniques.

In Chapter 4, one high V_{IN}/V_O GaN-based power converter with EMI regulation is designed for battery-to-load power conversion. Firstly, the EMI noise deteriorations induced by high step-down conversion ratio are analyzed. To suppress EMI noise, in addition to using bulky EMI filters, SSM techniques are widely applied in power converters. The dilemma of SSM techniques in high step-down ratio dc-dc power converters are then investigated. To achieve effective EMI reduction and maintain high efficiency in high step-down ratio power conversion, the proposed anti-aliasing MR-SSM and in-cycle adaptive ZVS techniques are applied in GaN-based half-bridge buck converters. Moreover, to improve the driving reliability of GaN-based power converter, the pulse-reinforced up-level shifting technique is developed. Then the detailed circuit designs are illustrated, which include multi-rate T_{ON} generator, elastic t_{dead} controller and pulse-reinforced up-

level shifter. Finally, the design is fabricated with a 180-nm HV BCD process, and the measurement results are shown to successfully verify the new control scheme and circuit design techniques.

Chapter 5 presents a condition monitored GaN-based power converter for reliability. Online condition monitoring is widely used in power electronics to monitor the healthy state of power converters. The multiple electrical parameters for healthy state signatures are firstly reviewed, and on-resistance of a GaN HEMT is regarded as one crucial healthy signature. Then the classic dynamic r_{on} sensing techniques and technical limitations for GaN HEMTs are investigated. After that, the proposed on-chip self-calibrated full-profile dynamic r_{on} monitoring strategy is introduced to enhance its reliability. It is applied in a half-bridge buck converter, which is regulated by a dual-ON time control scheme. Furthermore, the detailed circuit implementations including integrated M_L forward r_{on} sensor, integrated M_H forward r_{on} sensor, integrated ET M_L reverse r_{on} sensor, and dual-rail up-level shifter, are presented. This design is implemented in a 180-nm HV BCD process. The measured experimental results successfully validate the proposed operation scheme and circuit design techniques.

Chapter 6 proposes one monolithic integrated GaN AHB power converter for direct 48V/1V power conversion. Firstly, the prior arts of monolithic GaN power circuits are introduced. Then, the design challenges of monolithic GaN circuits integrations are discussed. Afterwards, the proposed monolithic GaN AHB converter is presented. It is followed by the detailed circuit implementations of A^2 up-level shifting, SBH gate driving, and on-die temperature sensing and on-die t_{dead} control techniques. The A^2 up-level shifter supports diving signal transmission between LV and HV domains and the SBH gate driver controls the switching of GaN power switch with

low propagation delays and high reliability. The on-die temperature sensor facilitates thermal protection of power converter and on-die t_{dead} controller realizes ZVS operations of GaN power switches. This design is fabricated in a GaN-on-SOI process. The measurement results are presented to successfully verify the proposed circuit design techniques.

Finally, this dissertation is concluded with a summary of major research contributions. Then, the future research directions are discussed in Chapter 7.

CHAPTER 2

GAN POWER SWITCHES & GAN-BASED POWER CONVERSION

In this chapter, the GaN-based power conversions are introduced. As important components in power converters, structures of commercial GaN HEMTs are firstly investigated and discussed in Section 2.1, which mainly include depletion mode GaN HEMT, cascode GaN HEMT and enhancement mode GaN HEMT. After that, to evaluate the performance of GaN HEMTs, key characteristics are analyzed and compared with classic silicon power devices in Section 2.2. With the employment of GaN HEMTs, step-down dc-dc power conversion topologies are introduced and analyzed in Section 2.3. Finally, a summary of GaN power conversion circuit designs is given in Section 2.4.

2.1 Structures of GaN HEMTs

2.1.1 Depletion Mode GaN HEMT

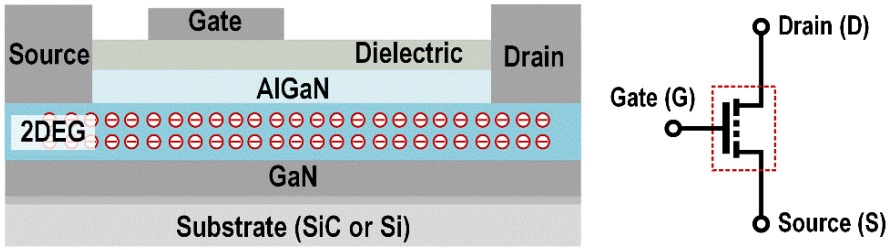


Figure 2.1. Structure and symbol of a d-mode GaN HEMT [Lidow-15].

For the same on-resistance and voltage rating, the parasitic capacitances of GaN transistors are several times lower than those of comparable silicon power devices. Given the lower parasitics and lack of a body diode without reverse recovery loss, GaN HEMTs can switch much faster with much lower switching losses. Initially, the depletion mode (d-mode) GaN HEMTs were employed

as RF power switches in power amplifiers. As shown in Figure 2.1, it is a normally-on device with an equivalent negative threshold voltage [Lidow-15]. When its gate source voltage difference (V_{GS}) is zero, the 2DEG current conduction path between source and drain is turned on inherently, exhibiting a low on-resistance. If V_{GS} is negative enough and below its threshold voltage, the 2DEG current conduction path is depleted to turn off the d-mode GaN HEMT. High voltage difference between drain and source (V_{DS}) can thus be blocked. Although it provides a cost benefit for manufacturers in terms of device production, its negative threshold voltage leads to practical implementation difficulties. For fail-safe considerations, power devices in switched-mode power supplies should be kept off to disconnect the input from the output when a bias power is unavailable. Otherwise, its maximum drain current would be drawn from the supply, leading to excessive thermal dissipation and device burning out. Due to the inherent negative threshold voltage of d-mode GaN HEMT, when the power bias is unavailable, the d-mode GaN HEMT is on for a zero V_{GS}. If a high V_{DS} is applied on the drain and source of d-mode GaN HEMT, a high current is generated through it. The excessive thermal dissipation would burn out the device, challenging system reliabilities. In addition, to control switching of the d-mode GaN HEMT, the gate driving voltage needs to switch between negative and positive rails. The required negative driving circuits are different from conventional gate driving circuits, increasing circuit design complexity greatly.

2.1.2 Cascode GaN HEMT

To solve the fail-safe reliability concern, one series LV silicon MOSFET $M_{Silicon}$ can be connected with the HV d-mode GaN HEMT M_{DGaN}, building a cascode GaN HEMT in Figure 2.2 [Transphorm-21, TI-21]. When the power bias is unavailable, the gate source voltage of $M_{Silicon}$ is

zero. Due to a positive threshold voltage of $M_{Silicon}$, it is kept off to block the high short circuit current through it. If a large voltage difference is applied between drain (D2) and source (S1) of the cascode GaN HEMT, the current through M_{DGaN} will firstly charge the node D1(S2), which is the source of M_{DGaN} and the drain of $M_{Silicon}$. The voltage of D1(S2) rises due to infinite off-state resistance of $M_{Silicon}$, inducing a negative gate source voltage difference of $M_{DGaN.}$ Once the voltage difference is lower than its negative threshold voltage, M_{DGaN} will be turned off to block current through it. The power devices are thus protected from excessive thermal generation. In this way, no extra technology processes are needed in d-mode GaN HEMTs, avoiding cost penalties in GaN device fabrication. When turning on and off the cascode GaN HEMT, it can be indirectly controlled through the gate of $M_{Silicon}$ or directly controlled by the gate of M_{DGaN}. Based on the configurations of driving circuits for cascode GaN HEMT, there are mainly two kinds of driving schemes: indirect cascode gate driving and direct gate driving.

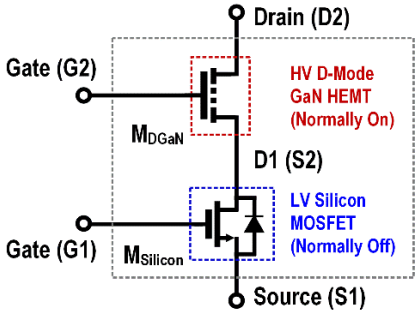


Figure 2.2. Structure of a cascode GaN HEMT.

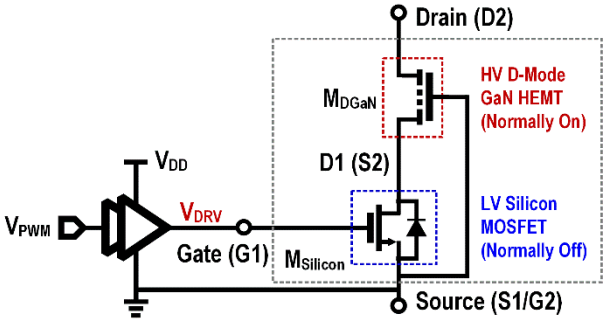


Figure 2.3. Indirect gate driving scheme of a cascode GaN HEMT.

The configuration of indirect cascode gate driving scheme is illustrated in Figure 2.3 [Transphorm-21]. The gate of M_{DGaN} is connected to the source of $M_{Silicon}$. Because of the positive threshold voltage of $M_{Silicon}$, the cascode GaN HEMT can be controlled by the conventional driving circuits, which switch between zero and positive voltages. Complicated negative voltage driving circuits are thus eliminated to simplify circuit designs. For example, when V_{GS} of $M_{Silicon}$ is zero, it is kept off. If a large current is applied from drain to source of the cascode GaN HEMT, the source of M_{DGaN} rises, and M_{DGaN} is turned off due to its large negative gate source voltage difference. On the other hand, when V_{GS} of $M_{Silicon}$ is higher than its threshold voltage, $M_{Silicon}$ is turned on with a very small on-resistance, and the gate source voltage difference of M_{DGaN} falls close to zero to turn on M_{DGaN}. Thus, classic gate driving circuits can control the cascode GaN HEMT directly with low design complexity. Nevertheless, since the switching of M_{DGaN} is indirectly controlled through $M_{Silicon}$, the gate driving signal of M_{DGaN} could be affected by the different current and voltage occasions and its dv/dt transition is lack of control. Besides, $M_{Silicon}$ keeps switching continuously, and its parasitics lead to extra switching losses. In addition, during the reverse condition period, the reverse current flows from the body diode of $M_{Silicon}$ and M_{DGaN}. The reverse recovery loss of $M_{Silicon}$ increases power loss further, compromising the merits of GaN devices that its lack of body diode eliminates reverse recovery loss.

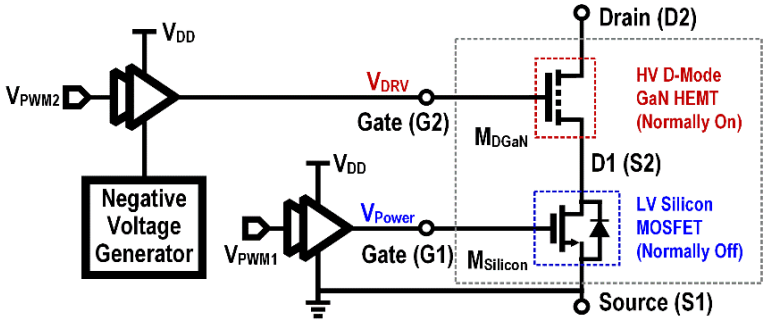


Figure 2.4. Direct gate driving scheme of a cascode GaN HEMT.

Accordingly, the direct gate driving scheme of a cascode GaN HEMT is employed [TI-21]. Figure 2.4 presents the direct driving scheme. Compared to the one single gate in the indirect cascode driving scheme, the gates of $M_{Silicon}$ and M_{DGaN} are separated. Overall, there are two gate terminals of the cascode GaN HEMT. When the power source of driving circuits is unavailable, $M_{Silicon}$ is kept off to prevent short through current of d-mode GaN HEMT. On the other hand, if the main power source is available, $M_{Silicon}$ is kept constantly on by a high driving voltage V_{Power}. Meanwhile, one negative voltage rail is generated for the driving circuits of M_{DGaN}. The driving voltage of M_{DGaN} gate (G2) is switched between negative and positive values to control the switching of M_{DGaN}. In this way, the non-ideal effects induced by parasitic capacitors and potential reverse recovery loss of $M_{Silicon}$ are eliminated to maximize the switching performance. Furthermore, since M_{DGaN} is controlled directly by the driving circuits, the driving strength can be accommodated adaptively in different voltage and current levels, optimizing driving reliability. However, the extra negative rail voltage generator would increase circuit design complexity.

2.1.3 Enhancement Mode GaN HEMT

Targeting on fully taking advantage of GaN devices, the d-mode and cascode GaN HEMTs can be improved further. From the technology process view, a single GaN HEMT with a positive threshold voltage is becoming more promising in switching power circuits since the fail-safe concern can be solved inherently. However, extra technology fabrication processes are necessary to turn off the 2DEG current conduction path when the gate source voltage difference is zero. Divided by different positive threshold voltage implementation processes, there are mainly three kinds of enhancement mode (e-mode) GaN HEMTs, specifically, p-GaN, recessed gate, and implanted gate [Lidow-15].

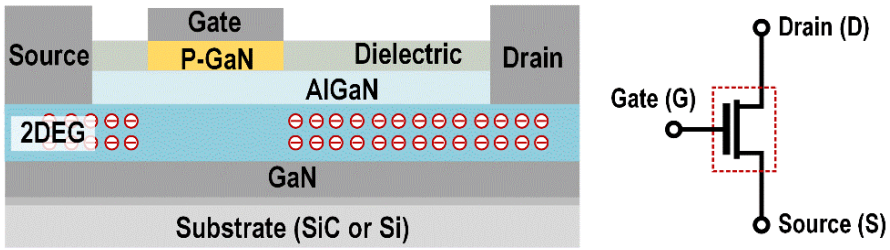


Figure 2.5. Structure and symbol of an e-mode GaN HEMT [Lidow-15].

Figure 2.5 presents the structure and symbol of an e-mode GaN HEMT. Among different technology implementation techniques, p-GaN device was the first commercially available e-mode GaN HEMT in the market [Davis-10, Chen-17a]. By appropriately controlling doping level and thickness of the p-GaN layer, a large number of negative charges can be generated in the p-GaN layer. These charges would deplete the 2DEG conduction path when V_{GS} is zero, keeping the device normally off. If V_{GS} rises higher than the positive threshold voltage, 2DEG path is resumed and the e-mode GaN HEMT is turned on. Besides, etching away the AlGaN barrier layer can also realize the e-mode GaN HEMT, since the inherent positive charges under the gate electrode are removed. To reduce the gate leakage current, an insulating dielectric layer is employed to realize a recessed gate e-mode GaN structure [Lanford-05]. In addition, the implanted gate e-mode GaN structure can be fabricated by implanting fluorine atoms in the AlGaN barrier layer [Cai-06]. The trapped negative charges in the AlGaN layer can also deplete the 2DEG current conduction path inherently. By using a Schottky gate, the e-mode GaN HEMT is realized.

2.2 Characteristics of GaN HEMTs

2.2.1 Breakdown Voltage

In power electronics, an ideal power switch does not consume power. However, the actual power switches cannot ensure zero voltage drop during on state and the value of blocking voltage

in off state is not infinite. Therefore, specific characteristic parameters are used to describe the properties of real power devices.

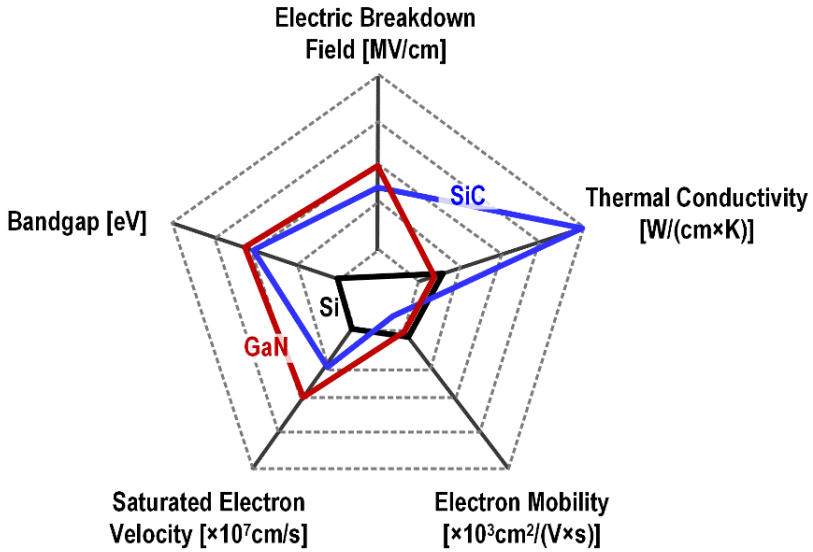


Figure 2.6. Key characteristics comparison among Si, GaN and SiC materials [Zetterling-00].

When the power switch is off, the blocked drain-source voltage should be below one specific value, named breakdown voltage. The breakdown voltage of a GaN HEMT is determined by the electrical field. Figure 2.6 shows key characteristics comparison among Si, GaN and silicon carbon (SiC) materials [Zetterling-00]. GaN and SiC materials can achieve much higher electric breakdown filed and bandgap than the Si counterpart, contributing to higher voltage operation of GaN and SiC circuits. The higher electron velocity helps GaN and SiC operate at a higher f_{SW} than Si devices. Overall, owing to characteristics of wide bandgap (WBG) materials, the WBG power devices are regarded as the next-generation power switches.

2.2.2 On-Resistance

When the power switch is turned on, there is a small on-resistance across the power switch. The non-zero on-resistance generates conduction loss and deteriorates efficiency. The actual on-

resistance is the sum of all the resistive parts of GaN HEMT, including parasitic contact resistances of source and drain terminals, and the on-resistance of 2DEG. The voltage rating of SiC power devices stays at and above 650V, while the voltage rating of GaN power devices ranges from tens volts to hundreds of volts [Quinn-17]. If the blocking voltages are the same, on-resistance and parasitics capacitances of GaN devices are much lower than that of silicon counterparts, enabling higher switching frequency and higher efficiency in GaN-based power converters.

Even though the technology and material analysis reveal GaN HEMTs achieve lower on-resistance than silicon devices, its on-resistance is affected by dynamic transient scenarios owing to its unique characteristics. In a GaN-based switching power converter, the GaN HEMT is continuously switching between off-state and on-state. Some electrons may get trapped in specific regions of the transistor structure when switched at high voltage and high f_{SW}. Following switching transients, the trapped electrons cannot be freed instantaneously when the GaN device is turned on. The on-state current carrying capability by 2DEG is thus reduced [Li-18a]. The value of instant dynamic on-resistance increases much higher than the static one, generating much higher conduction loss and lower efficiency. Accordingly, the excessive device self-heating effect would be detrimental to thermal failure, inducing potential reliability challenges [Bahl-16]. As a result, high reliability of GaN HEMTs is of paramount importance for robust GaN-based power converters. These static and dynamic on-resistances of GaN HEMTs are needed to be carefully considered when GaN HEMTs are employed in high f_{SW} power conversion systems.

2.2.3 Reverse Recovery and Reverse Conduction

Since the GaN HEMT only uses majority carrier conduction, without minority carrier conduction, the device can be turned off instantly if the source-drain bias disappears. Compared

to conventional HV silicon power devices, there is no classic parasitic PN body diodes of GaN HEMTs, which eliminates the reverse recovery loss. However, due to the lack of a classic body diode, when V_{GS} is zero, the reverse conducting current would generate a large reverse voltage drop between source and drain. It could be much larger than the forward voltage drops of PN diodes or Schottky diodes. A much higher reverse conduction loss of the GaN HEMT is thus generated, and it will degrade the efficiency. Besides, the reverse voltage drop is also affected by the off-state V_{GS}, which is shown in Figure 2.7. According to a GaN HEMT model, if reverse currents are same, a lower V_{GS} induces a larger reverse voltage drop across the device, increasing reverse conduction loss further [EPC-19]. Thus, special gate driving circuits are desired to minimize the reserve conduction loss for high efficiency.

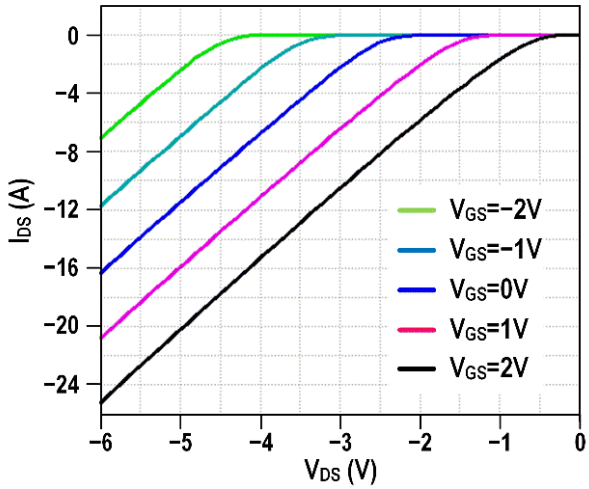


Figure 2.7. Effects of reverse current and V_{GS} on reverse voltage drop [EPC-19].

2.3 Step-Down DC-DC Power Converters

2.3.1 Low Dropout Regulators

To realize step-down dc-dc power conversion, a power conversion module can be simplified as one variable impedance network, which is typically composed of power switches,

capacitors, inductors and transformers [Wilson-00]. The feedback controller senses the output voltage V_O and controls the variable impedance network to regulate V_O. For different V_{IN} and I_O occasions, the equivalent impedance of the power converter can be adjusted correspondingly to maintain a stable V_O. In terms of impedance network implementations, there are several kinds of power converters, including low dropout (LDO) regulators, switched-capacitor power converters, switch mode power converters, and isolated switch mode power converters.

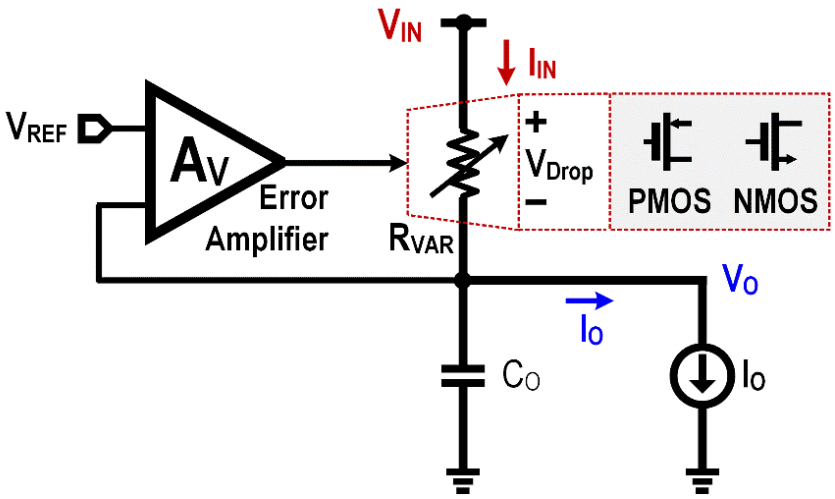


Figure 2.8. Typical LDO structure.

A typical LDO structure is illustrated in Figure 2.8. One tunable resistor R_{VAR} is connected in series with the load [Ma-13]. By controlling the value of R_{VAR}, a constant V_O is realized for different input voltages and load currents. Conventionally, R_{VAR} is implemented by either the PMOS or NMOS device. Without extra bulky inductors and capacitors, LDO performs the advantages of low area cost, fast transient response, and small V_O ripple. It is widely used in integrated low voltage power conversions, which require low noise of V_O. If the power loss of the amplifier is neglected, input current I_{IN} flows through R_{VAR} and equals load current I_O. The main power loss is induced by the voltage drop across R_{VAR}, V_{Drop}, which is the voltage difference

between V_{IN} and V_O. A higher V_{Drop} would generate a larger power loss and a lower efficiency. Thus, it is not suitable for high V_{IN} to low V_O dc-dc power conversion.

2.3.2 Switched-Capacitor Power Converters

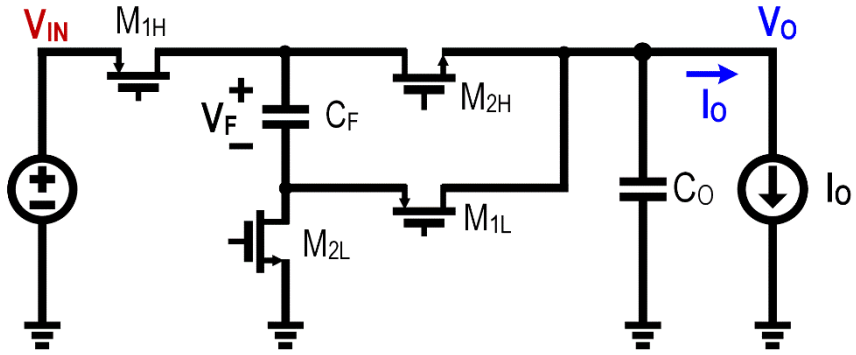


Figure 2.9. Circuit schematic of a 2:1 switched-capacitor converter.

The typical switched-capacitor converter is composed of capacitors and power switches. The switched-capacitor network is used to realize a variable impedance network [Seeman-08, Ma-13]. By switching several flying capacitors through power switches, one specific V_{IN}/V_O ratio can thus be achieved. Figure 2.9 presents the circuit schematic of a 2:1 switched-capacitor dc-dc power converter with one flying capacitor C_F and four power switches. There are two operation phases of the converter. In one phase, the switches M_{1H} and M_{1L} are turned on. The top plate of C_F is connected to V_{IN} and its bottom plate is connected to V_O. In the other phase, M_{2H} and M_{2L} are turned on, connecting the top plate of C_F to V_O, and the bottom plate of C_F to ground. In steady state, the voltage across C_F is stable, and V_O equals

$$V_O = 0.5 \times V_{IN}. \tag{2.2}$$

Since these power switches and capacitors can be integrated on-chip, the fully integrated switched-capacitor converter can reduce area cost significantly. But its voltage conversion ratio is fixed in one topology. For a constant V_{IN}, the limited V_O range constrains the widespread applications.

2.3.3 Switch Mode Power Converters

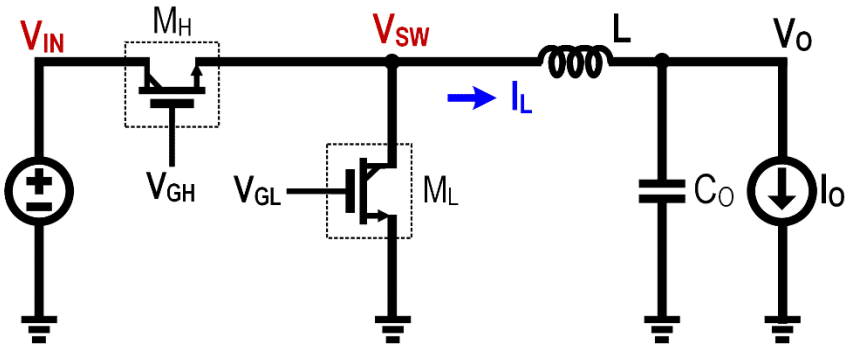


Figure 2.10. Circuit schematic of a half-bridge buck converter.

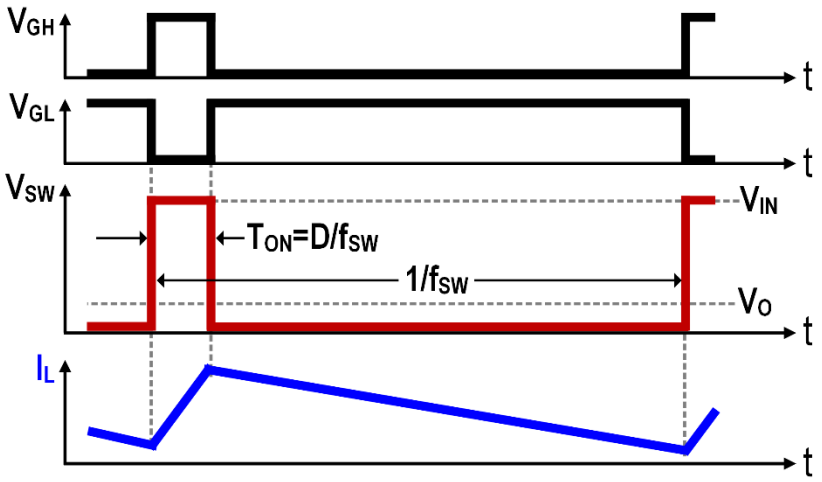


Figure 2.11. Operation waveforms of a half-bridge buck converter.

In power electronics, the switch mode power converters use power switches and passive inductors as the tunable impedance network. Figure 2.10 shows the circuit schematic of a synchronous half-bridge buck converter. The power switches M_H and M_L are switched alternatively by the gate driving signals V_{GH} and V_{GL}, respectively, and the switching node voltage V_{SW} transits between V_{IN} and zero periodically. The passive inductor and capacitor generate a stable V_O based on the duty ratio of V_{SW}. The key operation waveforms are shown in Figure 2.11. When M_H is turned on, V_{SW} rises to V_{IN} to energize the inductor, and the voltage across the inductor is $(V_{IN}-V_O)$.

After a period of on-duty time T_{ON}, M_L is turned on, and V_{SW} falls zero. The voltage across inductor is $-V_O$ and the energy in inductor is discharged to power V_O. In steady state, the charged and discharged energies are equal. Then the generated V_O can be expressed as

$$V_O = V_{IN} \times T_{ON} \times f_{SW}. \tag{2.3}$$

In a fixed f_{SW} operation, V_O can be regulated through modulating T_{ON}. The size and weight of such a switching buck converter are mainly determined by the essential inductor and output capacitor. To reduce the system volume and improve power density, a high f_{SW} is desirable to allow the employment of small passive components. Meanwhile, the high f_{SW} is also beneficial for fast transient response of power converters. However, according to equation (2.3), f_{SW} is determined by the values of V_{IN}, V_O and T_{ON}. If V_{IN}/V_O is significantly high, f_{SW} is constrained low since the feedback controller and driving circuits can hardly realize an extremely small T_{ON}. Thus, for the high V_{IN}/V_O dc-dc power conversion, the limited low f_{SW} induces large area cost, low power density and sluggish transient response.

2.3.4 Isolated Switch Mode Power Converters

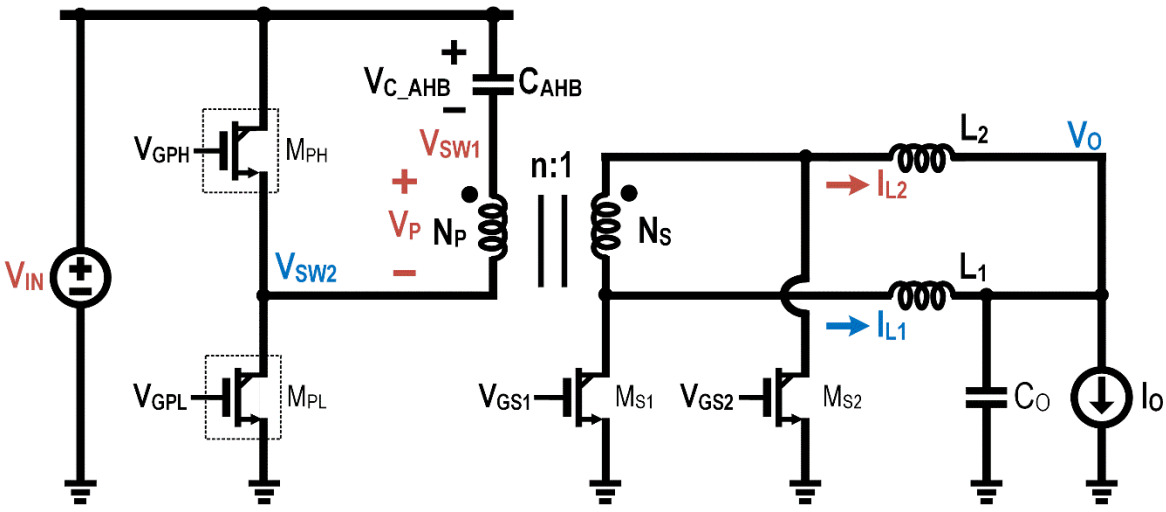


Figure 2.12. Circuit Schematic of an AHB converter [OnSemi-08].

Isolated switch mode power converters can achieve higher step-down conversion ratio and isolation functions because the transformer allows turns ratio between primary and secondary windings. The V_{IN}/V_O conversion ratio can be extended greatly with a large T_{ON} at high f_{SW}. Thus, it is becoming attractive in high step-down ratio dc-dc power conversions. Among these topologies, the AHB power converter is widely used [OnSemi-08]. As shown in Figure 2.12, on the primary side, half-bridge power stage with M_{PH} and M_{PL} are used, and the primary magnetizing inductance is serially connected with one flying capacitor C_{AHB}. On the secondary side, a current doubler is adopted to replace classic single-ended configuration. The synchronous rectifiers are realized with two power switches M_{S1} and M_{S2}. In steady state, M_{PH} and M_{PL} are switched alternatively, and C_{AHB} is charged and discharged periodically by the primary magnetizing inductance current. The voltage across C_{AHB}, V_{C_AHB}, is stable as

$$V_{C\_AHB} = V_{IN} \times T_{ON} \times f_{SW}. \tag{2.4}$$

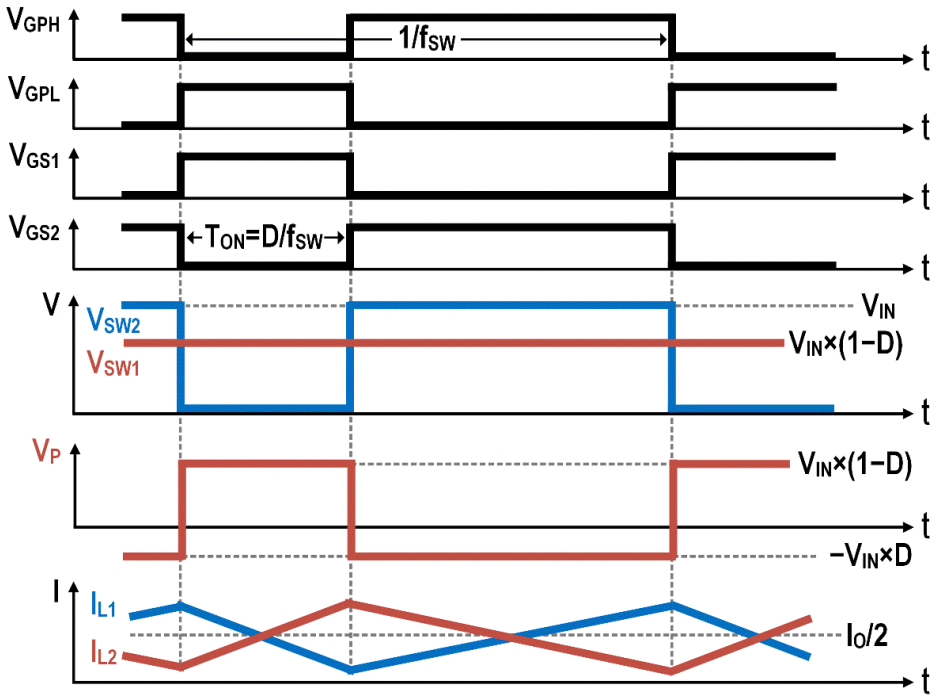


Figure 2.13. Operation waveforms of an AHB converter [OnSemi-08].

Figure 2.13 illustrates the key operation waveforms of an AHB converter in steady state. The four power switches M_{PH}, M_{PL}, M_{S1} and M_{S2}, are controlled by driving V_{GPH}, V_{GPL}, V_{GS1} and V_{GS2}, respectively. When M_{PL} and M_{S1} are turned on, V_{SW2} falls zero, generating a positive V_P across primary magnetizing inductance. The secondary-side current is conducted by M_{S1}, and inductor current I_{L2} rises and I_{L1} falls. When M_{PL} is turned off, the primary inductance current charges the switching node capacitance, realizing soft switching of M_{PH}. After V_{SW} crosses V_{IN}, M_{PH} is turned on with zero voltage difference. The value of V_P becomes $-V_{C\_AHB}$, and M_{S2} is turned on to conduct the rising I_{L1} and the falling I_{L2}. At the end of switching period, M_{PH} turns off, and the primary inductance current discharges the switching node capacitance for soft switching of M_{PL}. After V_{SW} falls zero, M_{PL} is turned on with zero voltage difference, reducing the switching loss in high f_{SW} operation. In steady state, V_O equals

$$V_O = V_{IN} \times T_{ON} \times f_{SW} \times (1 - T_{ON} \times f_{SW})/n. \tag{2.5}$$

Here, n represents the transformer turns ratio of primary- and secondary-side windings. By setting a small n, a high V_{IN}/V_O power conversion can be realized. By controlling the T_{ON} at a fixed f_{SW}, the stable V_O can be regulated. Compared to the half-bridge buck converter in equation (2.3), the turns ratio n provides additional voltage conversion, supporting a high f_{SW} operation. Owing to the complementary operation, the inductor current ripples of I_{L1} and I_{L2} are cancelled by each other, enabling low V_O ripple with a small output capacitor. It can also achieve soft switching of primary devices by utilizing the leakage inductance, and thus the switching loss can be reduced greatly, enabling the converter to operate at high frequency and efficiency. Besides, as the two primary power switches are switched complementarity, the ringing problem caused by leakage inductance is also eliminated for high reliability. However, the extra transformer will increase the total volume

cost. Another drawback of AHB converter is that the voltage stresses of secondary-side power devices are asymmetrical, and they are related to the duty cycle.

2.4 Summary

In this chapter, the structures of commercial GaN HEMTs are reviewed. Compared to d-mode GaN HEMTs, cascode and e-mode GaN HEMTs can improve the deployment flexibility owing to their positive threshold voltages. However, they require one extra series LV silicon device or additional fabrication processes. In contrast to classic HV silicon power devices with a same voltage rating, the GaN HEMTs can achieve both small parasitic capacitances and low on-resistance, enabling high switching frequency and high efficiency of GaN power conversion. However, due to their unique characteristics, such as dynamic on-resistance and large reverse conduction drop, special driving and control techniques are desired for robust and efficient GaN power converters. When GaN HEMTs are used for high step-down ratio power conversion, the switching frequency of classic switch mode power converter is constrained low, inducing low power density. The isolated switch mode power converter can accomplish high step-down ratio power conversion at high switching frequency, but the bulky transformer would consume more area. Thus, sophisticated power conversion topologies are in high demand for high step-down ratio power conversion.

CHAPTER 3

HIGH STEP-DOWN RATIO GAN-BASED DC-DC CONVERSION[*]

As discussed in Section 1.2.1, in order to satisfy the increasing power demand with high input voltage and low output voltage, high switching frequency high step-down ratio power conversion is highly desirable for high power density. But because of the high step-down conversion ratio, the maximum achievable switching frequency of the single-stage power converter is constrained low, which makes the reduction of passive inductors and capacitors challenging. In this chapter, a GaN-based DSD converter is introduced for direct 48V/1V power conversion. Firstly, the detailed technical challenges of high step-down ratio dc-dc power conversion with the half-bridge power converter, including limited switching frequency and large power loss, are analyzed in Section 3.1. After that, the operation principle and design considerations of DSD converter, and the proposed GaN-based DSD converter are introduced in Section 3.2. Section 3.3 then explains the operation scheme and circuit designs of master phase mirroring, which synchronizes two sub-converters of DSD topology. Meanwhile, the circuit implementation of on-chip inductor current sensor is presented for the closed-loop current mode regulation. In Section 3.4, the operation principle and circuit implementation of elastic on-time modulation are illustrated for fast dynamic response. The circuit of T_{ON} overlap prevention module is also elaborated for high reliability. The measurement results of the proposed design are provided in Section 3.5 to successfully verify the functionality and performance. Finally, this chapter is summarized.

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3.1 Technical Challenges of High Step-Down Ratio DC-DC Conversion

3.1.1 Limited Switching Frequency and Low Power Density

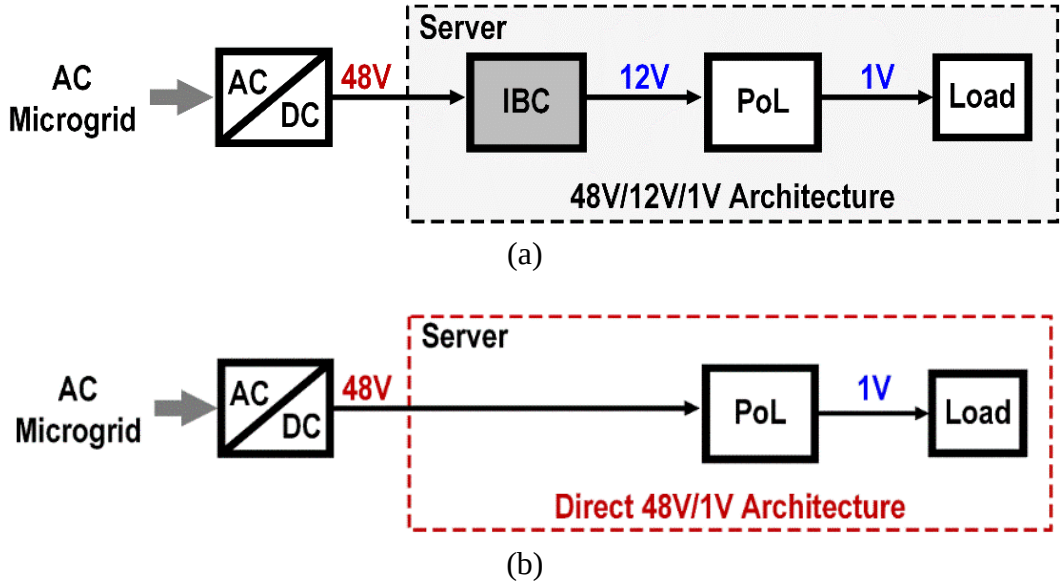


Figure 3.1. Power delivery system architectures: (a) conventional 48V/12V/1V architecture, and (b) direct 48V/1V architecture [Yan-20a].

As introduced in Chapter 1, the proliferative development of datacenter applications, as a direct result of explosive growth of big data, cloud computing and internet of things, has led to significant architecture and design strategy challenges on modern power delivery technologies. Conventionally, a two-stage 48V/12V/1V architecture is commonly employed for the end stages of power delivery, as illustrated in Figure 3.1(a). It usually consists of two dc-dc power conversion stages: an intermediate bus converter (IBC) stage that converts 48V down to 12V, and a point of load (PoL) converter stage that converts 12V to a well-regulated 1V for load applications. The advantage of this architecture lies in the fact that it has been well adopted for many years. Both IBC and PoL converters have been continuously improved, with fairly mature design technologies. Margins for further improvement on efficiency and performance have been slim. With ever-

increasing rack power density, single-stage, direct 48V/1V architectures such as *Google Architecture* have rapidly emerged [Li-17]. As illustrated in Figure 3.1(b), by merging the IBC and PoL stages into a single dc-dc power conversion stage, the direct 48V/1V solution reduces I^2R distribution loss on the power bus significantly and offers higher power density and deployment flexibility [Li-17, Oliver-12]. According to *Vicor Power*, direct 48V/1V power architecture can save 'Big Data' $500,000 per datacenter per year [Oliver-12]. However, as many new technologies, it also brings new technical challenges in implementation reality. In this specific case, design engineers face significant challenges in achieving extremely short ON-time in single-stage power conversion, overcoming imbalanced power distribution and increased reliability risks.

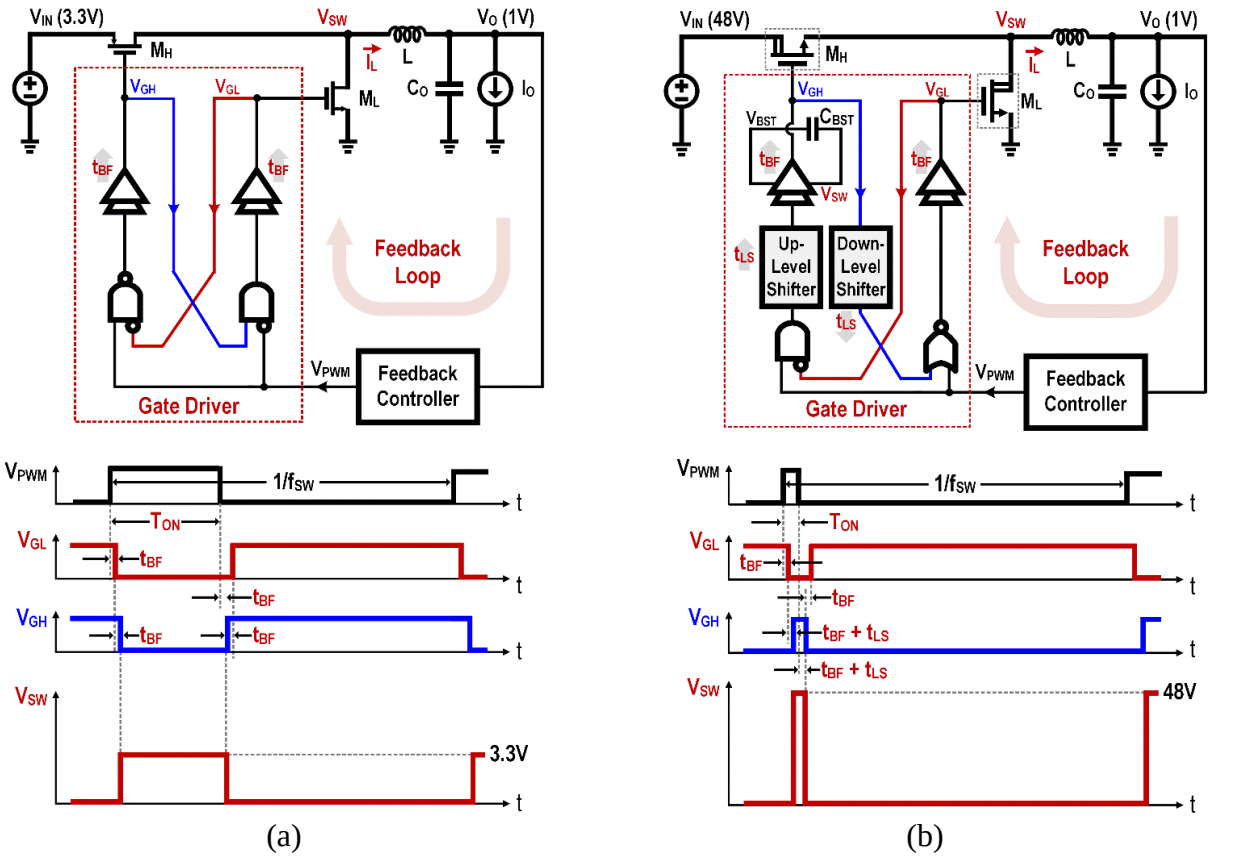


Figure 3.2. Illustrations of (a) a classic LV half-bridge architecture with key operation waveforms, and (b) an HV bootstrapped half-bridge architecture with key operation waveforms [Yan-20a].

To address these challenges, we first examine the most mature power conversion architecture designs: the half-bridge architecture, as shown in Figure 3.2(a), which is arguably the most frequently employed architecture by the IBC and PoL converters in conventional two-stage architectures. The success of the half-bridge architecture is owing to its simple and efficient structure and well-established control methods. With vast research efforts over the past decades, these converters are well optimized and can easily surpass 90% efficiency mark [TI-15, Maxium-18, ADI-18, Intel-18]. In addition to efficiency, a notable trend among these converters is that the switching frequency has been elevated continuously and has been above MHz level. This leads to multiple benefits. First, it reduces power passives effectively, leading to lower cost, smaller system volume and higher power density. Second, the use of small magnetic components helps reduce the EMI emission [Oliver-16]. Third, high switching frequency is generally beneficial for transient performance of a power converter. Hence, in this study, we take an average switching frequency of these converters [TI-15, Maxium-18, ADI-18, Intel-18] at 2MHz as the benchmark frequency. Simply raising the input voltage V_{IN} from 3.3V (Figure 3.2(a)) to 48V (Figure 3.2(b)) reveals some drastic parameter changes. The first is the ON-time of the converter T_{ON}. For a half-bridge buck converter, the T_{ON} in steady state can be computed as

$$T_{ON} = V_O/(V_{IN} \times f_{SW}), \tag{3.1}$$

where V_O, V_{IN} and f_{SW} represent output voltage, input voltage and switching frequency, respectively. For the 3.3V/1V power conversion at 2MHz, T_{ON} is about 151.5ns, without considering other delay elements. In reality, however, the accuracy of T_{ON} is impacted by the turn-on/-off times of power switches M_H and M_L, the delay of buffer driver t_{BF}, the gate drive t_{dead} that prevents the gate driving signal V_{GH} and V_{GL} from turning on M_H and M_L simultaneously, and other

delays by elements in the feedback loop. In general, at 3.3-V V_{IN}, the aforementioned delays are in the order of nanoseconds, which is much smaller than the required 151.5-ns T_{ON}. Hence, it is not substantially challenging to achieve T_{ON} accurately. However, for direct 48V/1V power conversion, T_{ON} would be drastically reduced to 10.4ns at 2MHz, which is comparable and sensitive to literally any delay elements of gate driver and feedback loop. In addition, due to the high V_{IN} (48V), higher breakdown voltage, bulkier power devices have to be used, which potentially cause the increases on all above delays. Furthermore, at 48-V V_{IN}, bootstrapping techniques are usually needed to reduce the switching loss and retain effective gate driving. Moreover, up- and down-level shifters are essential to transmit diving signals between low and high voltage domains, but they will add substantial delay t_{LS} into the driving control loop [Song-15]. Consequently, accurately accomplishing 10.4-ns T_{ON} in high-voltage, high-current power converters has been extremely challenging if not impossible. In other words, f_{SW} in 48V/1V conversion has to be below 2MHz to switch power devices reliably. But the value and size of passive inductor and capacitor increase correspondingly, compromising the power density of power conversion system.

3.1.2 High Power Loss and Low Efficiency

The second significant challenge for direct 48V/1V power conversion in the half-bridge architecture is the highly increased power loss. To demonstrate this, a 180-nm TSMC BCD process [TSMC-17] is used to estimate the power changes. In 3.3V/1V architecture in Figure 3.2(a), 5V devices can be used to implement the power switches M_H and M_L. For a load current of 1A and a switching frequency of 2MHz, the sizes of M_H and M_L are optimized simultaneously for minimum total power loss, which includes high and low-side power switch conduction loss ($P_{CON(HS)}$ and

$P_{CON(LS)}$), output capacitance loss of high and low-side power switches ($P_{COSS(HS)}$ and $P_{COSS(LS)}$), switching loss (P_{SW}), reverse recovery loss (P_{RR}) and t_{dead} reverse conduction loss (P_{DT}) [Jauregui-11]. With the same load current and frequency, for direct 48V/1V architecture in Figure 3.2(b), compatible higher breakdown voltage NMOS M_H and M_L are used, and we use the same approach to optimize the transistor sizes for maximum efficiency. The power losses comparison between the two architectures are detailed in Figure 3.3. Although the switching loss P_{SW} is analyzed using the same gate driving delay, it is proportional to the voltage swing of switching node voltage V_{SW}. P_{SW} increases greatly because V_{SW} swing increases from 3.3V to 48V. Besides, due to the high voltage power switches in 48V/1V power converter, the parasitic capacitances of these high voltage devices are much larger than those of low voltage devices. It results in higher $P_{COSS(HS)}$, $P_{COSS(LS)}$ and P_{RR}. Overall, the power loss in 48V/1V power conversion is about 19 times of that in 3.3V/1V power conversion, implying a more challenging nature of accomplishing high efficiency.

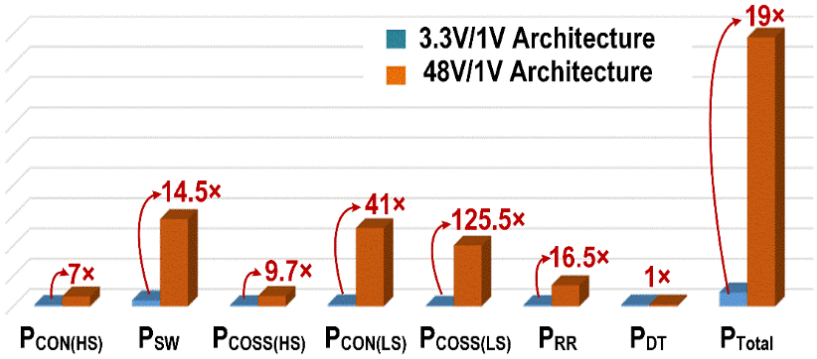


Figure 3.3. Power loss comparison in half-bridge buck converter [Yan-20a].

Because of the above challenges, the classic half-bridge architecture is not a favorable choice for efficient direct 48V/1V power conversion at high switching frequency. To relax the duty cycle limitation, a classic 3-level converter can be considered as an alternative, which consists of four power switches, one flying capacitor and one inductor [Liu-16]. However, although voltage

ratings of the four power switches are reduced to $V_{IN}/2$, there are always two power switches in series presented in the power path during each operation phase. Efficiency is thus degraded greatly. Other alternative architectures have been proposed recently. A 48V/1V sigma converter in [Ahmed-17] adopts a quasi-parallel architecture with an LLC resonant DC/DC transformer in the upper stage and a buck converter in the lower stage. But the complex structure, high voltage power switches and isolated gate drivers deteriorate the power density. In addition, it requires a complicated startup control, and its efficiency severely degrades with input voltage variations. A hybrid architecture in [Seo-18] consists of multiple discrete flying capacitors and power switches and accomplishes the 48V/1V power conversion on a PCB, which also faces power density challenge. A switched tank converter in [Jiang-19] utilizes zero current switching technique to reduce switching loss. But the large number of magnetic components and switches leads to high cost and low power density. In addition, an additional half-bridge converter is still needed to generate a well-regulated output voltage around 1V.

3.2 The DSD Architecture and Design Considerations

3.2.1 Understanding of the DSD Architecture

In search for an efficient and power-density-conscious architecture for direct 48V/1V power conversion, a DSD architecture was reported in [Nishijima-05], which is shown in Figure 3.4. Compared to conventional two-phase buck converters, only one extra flying capacitor C_F is used in this architecture. C_F naturally transforms the architecture into two sub-converters and the switching node voltage swings in each sub-converter are reduced by $V_{IN}/2$ as a result. Thus, both the switching frequency and conversion efficiency of 48V/1V power conversion are improved.

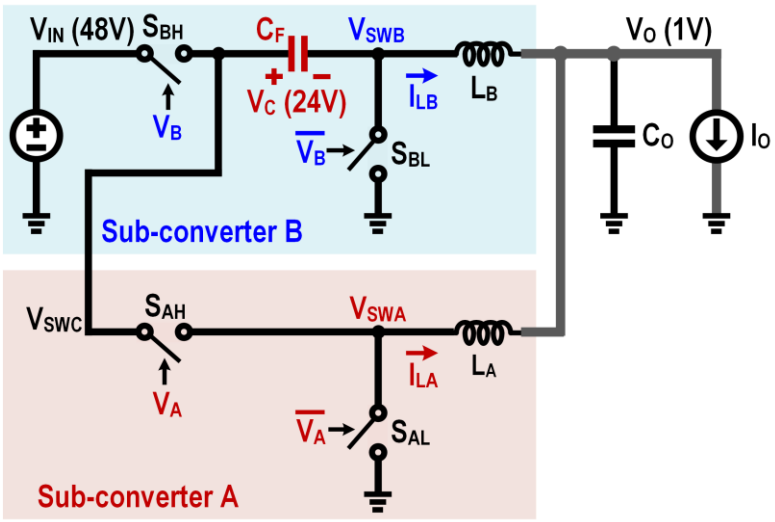


Figure 3.4. Architecture of a DSD power converter [Nishijima-05, Yan-20a].

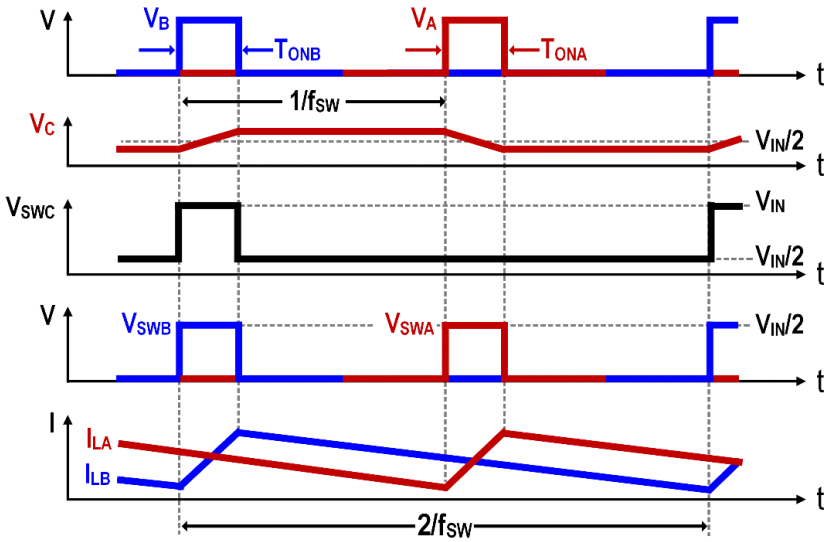


Figure 3.5. Key operation waveforms of a DSD power converter [Nishijima-05, Yan-20a].

Figure 3.5 illustrates the key operation waveforms. In steady state, sub-converter A and sub-converter B energize inductor current I_{LA} and I_{LB} alternatively, and C_F is discharged and charged periodically. When the gate signal V_B is logic high and V_A is logic low, power switches S_{BH} and S_{AL} are on while the power switches S_{BL} and S_{AH} are off. C_F is charged up by inductor current I_{LB}. When the gate signal V_B is low and V_A is high, C_F is discharged to supply I_{LA} during

the ON-time of sub-converter A. Thereby in steady state I_{LA} and I_{LB} are balanced, and the voltage V_C across C_F is stable as $V_{IN}/2$ with constant voltage ripple. The switching nodes V_{SWA} and V_{SWB} switch between zero and $V_{IN}/2$ and V_{SWC} switches in the range of $V_{IN}/2$ and V_{IN}. Thus, compared to the classic half-bridge architecture, the voltage stress on power switch S_{AL}, S_{BL} and S_{BH} is reduced from V_{IN} to $V_{IN}/2$. This makes the use of lower voltage rating power switches with smaller parasitic capacitances possible, benefiting the lower switching loss, cost and size. Meanwhile, with halved equivalent input voltage, the ON-time equals

$$T_{ON,DSD} = 2 \times V_O/(V_{IN} \times f_{SW}), \tag{3.2}$$

which is doubled compared to half-bridge architecture. To equate f_{SW} in half-bridge buck converter, the two-phase DSD architecture only needs to operate at $f_{SW}/2$, extending T_{ON} by 4 times in total. The extended T_{ON} mitigates the extreme delay requirements in gate driver and feedback controller.

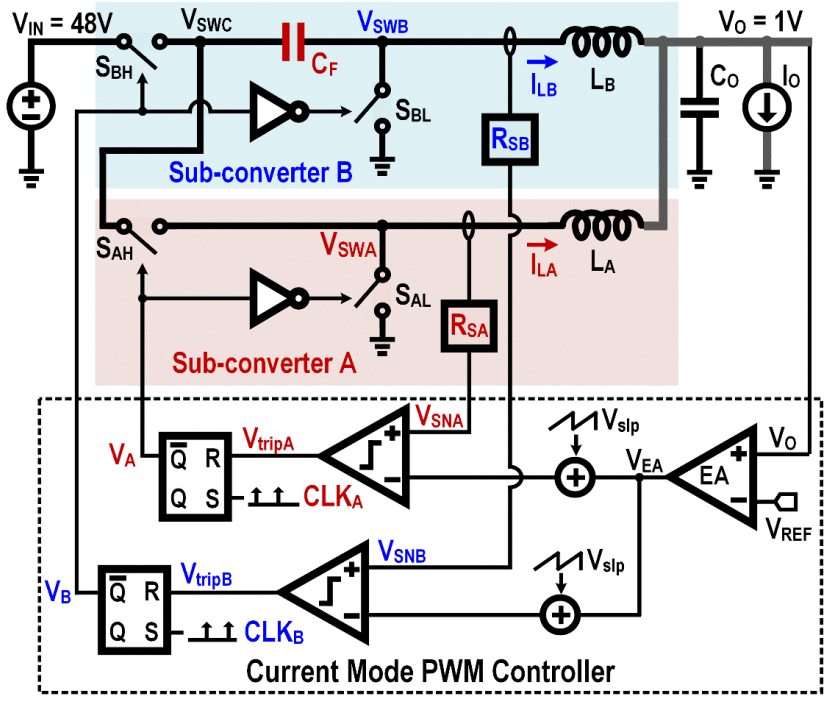


Figure 3.6. Circuit block diagram of a conventional two-phase current mode DSD power converter [Yan-20a].

However, with the DSD architecture, the reliability issues deteriorate significantly due to its largely increased complexity. Figure 3.6 shows the circuit block diagram of conventional two-phase current mode PWM controller to regulate the DSD architecture. In the PWM controller, the two sub-converters are synchronized by 180-degree phase shifted clock signals CLK_A and CLK_B. The leading edges of the two sub-converters are regulated by two independent feedback loops. The output voltage V_O compares with reference voltage V_{REF} by error amplifier (EA) to generate proper V_{EA} for the current mode regulation. Two inductor current sensors sense I_{LA} and I_{LB} of the two sub-converters. The sensed voltage V_{SNA} and V_{SNB} are compared with the sum of slope compensation voltage V_{slp} and V_{EA} separately to determine the leading edge of ON-times (T_{ONA} and T_{ONB}).

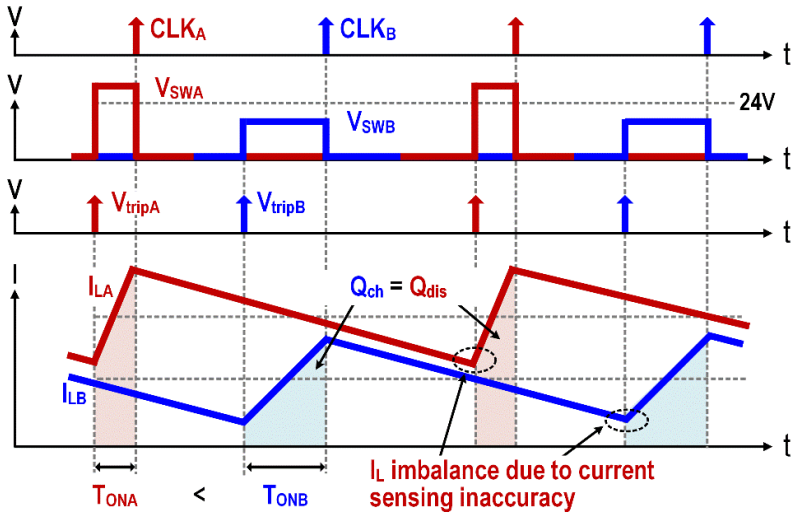


Figure 3.7. Phase current imbalance in a classic two-phase current mode DSD power converter [Yan-20a].

Conventionally, the on-chip sense-FET based current sensors are used for low circuit complexity [Ki-98]. But the equivalent inductor current sensing resistors R_{SA} and R_{SB} in the two sub-converters are highly related to the on-resistance of the power switches S_{AL} and S_{BL}. Since the power switch on-resistance has a wide random variation range, there is potential inductor current

sensing mismatch between sub-converter A and B. In addition, the power paths of the two sub-converters are not strictly symmetrical. The two inductor current sensors can hardly match perfectly. Therefore, as shown in Figure 3.7, the feedback loops have to generate a mismatch between T_{ONA} and T_{ONB} to compensate the circuit mismatch. Due to the extremely short ON-time in direct 48V/1V power conversion, the mismatch between T_{ONA} and T_{ONB} would be significant, leading to substantial phase current imbalance, and thus causing hot spots issues.

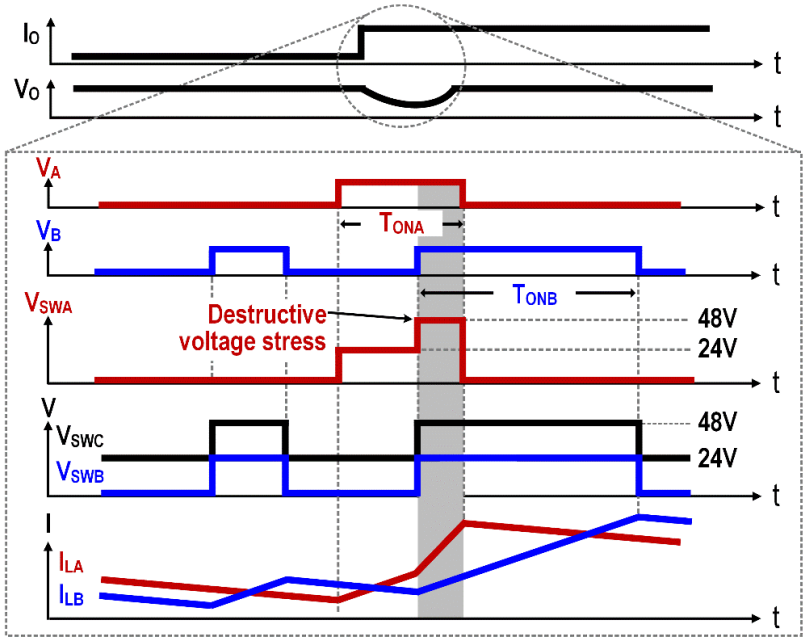


Figure 3.8. Cross-phase T_{ON} overlap at load transient in a classic two-phase current mode DSD power converter [Yan-20a].

In addition, its reliability is challenged during load transient operations. For instance, when the load current I_O increases suddenly, ON-times of the two sub-converters T_{ONA} and T_{ONB} expand simultaneously. As the two sub-converters operate independently, there is no mechanism to prevent T_{ONA} and T_{ONB} from overlapping, which causes both S_{AH} and S_{BH} to be conductive and pushes the switching node V_{SWA} to 48V. As is shown in Figure 3.8, the cross-phase T_{ON} overlap creates destructive voltage stress on S_{AL} and causes false charging on I_{LA}. Thus, serious reliability

issues will be generated. Compared to PWM control, the COT control can be employed for low duty ratio conversion thanks to its high bandwidth design capability [Yan-13]. However, it also faces similar reliability issues. In addition, the fixed T_{ON} still results in slow transient response and large output voltage damping in load transients. Also, with varying switching frequency and no reference clock, it would be difficult to accomplish phase synchronization in DSD architecture.

3.2.2 Proposed GaN-Based DSD Power Converter

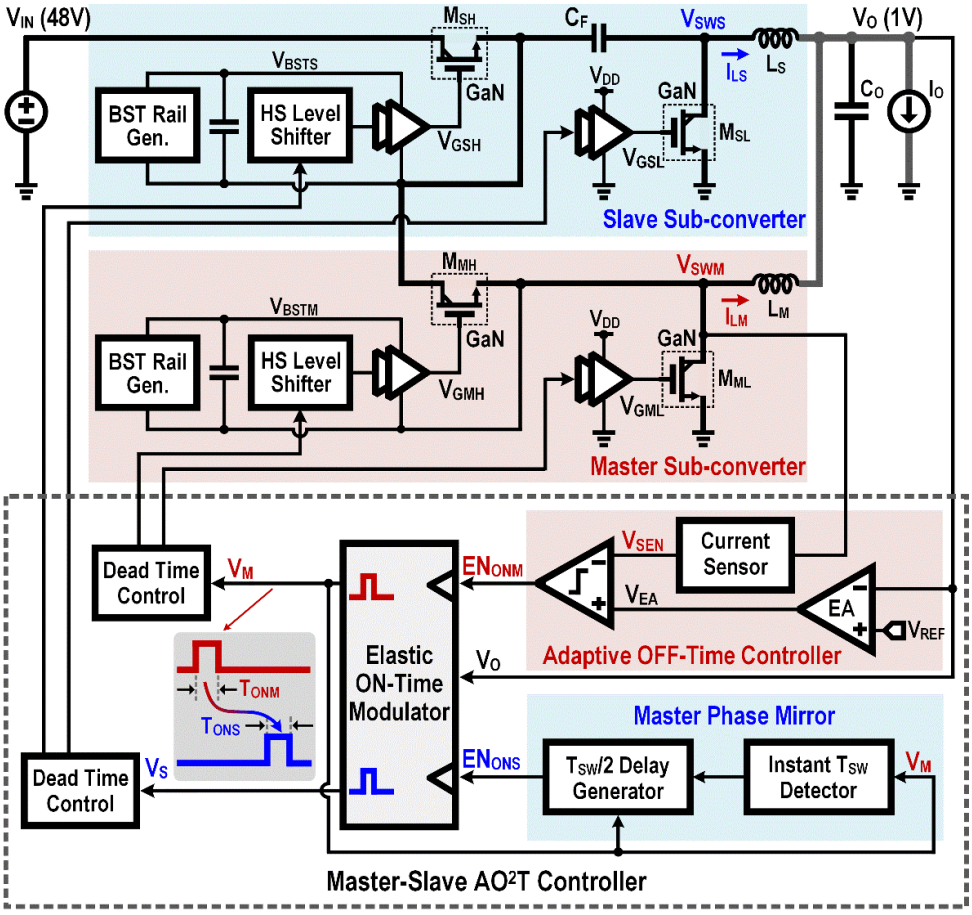


Figure 3.9. Block diagram of the proposed GaN-based DSD power converter [Yan-20a].

In order to overcome the above-mentioned design issues, a new GaN-based DSD power converter in Figure 3.9 is proposed for improved operation reliability and fast transient response.

It employs all n-channel e-mode GaN HEMTs as power switches for superior switching performance [Lidow-15]. The parasitics of GaN HEMTs are much smaller than those of HV silicon MOSFETs for comparable on-resistance and voltage rating. So, it is beneficial for high conversion efficiency at high switching frequency. To avoid the harmful cross-phase T_{ON} overlap and phase current imbalance of the two sub-converters, the DSD topology is divided as a master sub-converter and a slave sub-converter. A master-slave AO^{2}T control scheme is designed for V_O regulation with high reliability. In the master-slave AO^{2}T controller, the adaptive OFF-time controller is designed to regulate the master sub-converter by valley current mode control scheme. The master phase mirror realizes clock-free phase synchronization of the slave sub-converter with the same ON-time and frequency of the master sub-converter. The adopted only one inductor current sensor eliminates the potential current sensing mismatch induced by multiple inductor current sensors. Thanks to the inherent feedback loop of the DSD architecture, the proposed power converter achieves automatic inductor current balancing without extra control circuits [Shenoy-15]. Intuitively, if average inductor current I_{LM} in master sub-converter is higher than average inductor current I_{LS} in slave sub-converter, in each switching cycle C_F discharging is higher than C_F charging. So, the voltage across C_F, V_C, decreases. Then the average I_{LM} falls gradually because of the decreasing inductor charge voltage ($V_C - V_O$). In contrast, the average I_{LS} rises due to its increasing inductor charge voltage ($V_{IN} - V_C - V_O$). With parasitics in the architecture, I_{LM} and I_{LS} will be balanced, and V_C is stable as $V_{IN}/2$ finally. On the other hand, elastic ON-time modulator (EOM) modulates ON-time adaptively during I_O transient to minimize V_O variation and prevents cross-phase T_{ON} overlap for high reliability. High speed level shifters and bootstrap rail generators are also designed to drive GaN HEMTs efficiently.

3.3 Master Phase Mirroring

3.3.1 Operation Scheme

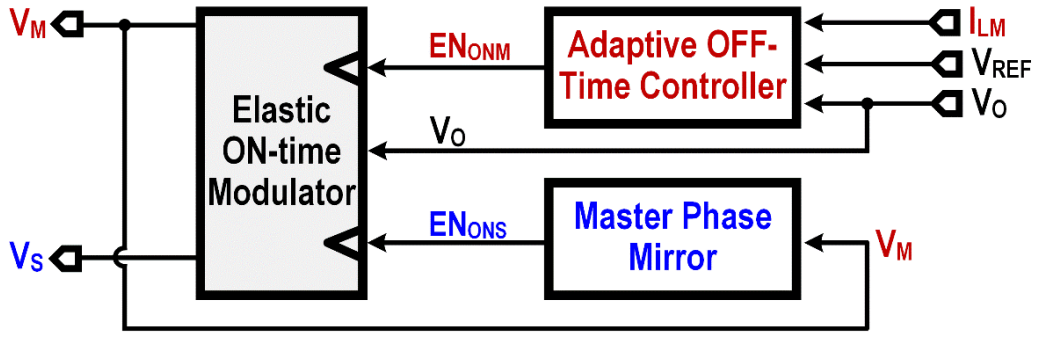


Figure 3.10. Simplified block diagrams of AO^{2}T controller.

As described in Section 3.2, although it is straightforward to use two separated inductor current sensors to realize current mode feedback regulation, there is potential current sensing mismatch between the two on-chip current sensors, inducing phase current imbalance. The current sensing mismatch aggravates for discrete GaN power device. This problem becomes significant for extreme low duty ratio conversion. Based on these analyses, the current mode master-slave AO^{2}T control is proposed with only one inductor current sensor. The DSD architecture is divided as master and slave sub-converters. As shown in Figure 3.10, the feedback controller can be simplified as three main function blocks. The master sub-converter is regulated by the current mode adaptive OFF-time control while the latter one is regulated by master phase mirroring. V_M and V_S are the driving input signals of master and slave sub-converters. By sensing V_O, reference voltage V_{REF}, and master sub-converter inductor current I_{LM}, an optimized off-duty time of V_M is generated by the adaptive OFF-time controller for V_O regulation. The elastic ON-time modulator actively controls the on-duty times of V_M and V_S. The off-duty time of V_S is controlled by the master phase mirror in order to track the instant switching frequency of V_M.

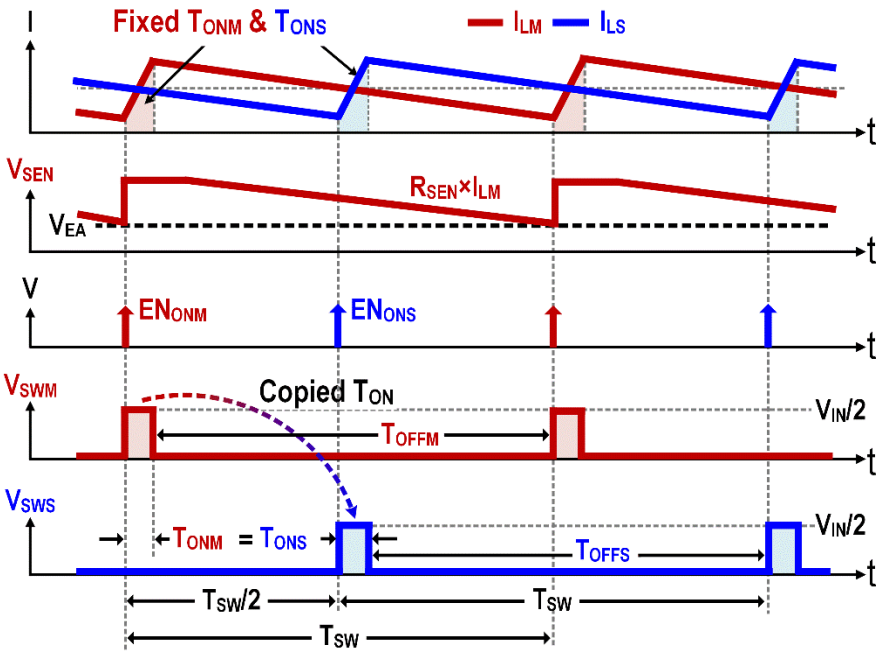


Figure 3.11. Adaptive OFF-time control in collaboration with master phase mirroring [Yan-20a].

Figure 3.11 shows the detailed operation waveforms of the master slave control scheme. In the current mode adaptive OFF-time control for master sub-converter, V_{SEN} represents the equivalent sensed voltage of inductor current I_{LM} in master sub-converter. V_{EA} is the output of an error amplifier based on the comparison of output voltage V_O and V_{REF}. Master sub-converter ON-time T_{ONM} is initialized at the trip point of V_{SEN} and V_{EA}. Then GaN switch M_{MH} is on and switching node voltage V_{SWM} rises to $V_{IN}/2$ to charge the master sub-converter inductor L_M until T_{ONM} expires. Meanwhile, the instant switching period T_{SW} of the master sub-converter is recorded in master phase mirroring regulation. After T_{ONM} expires, M_{MH} is off and M_{ML} is on, the master sub-converter enters the discharge phase T_{OFFM}, which is defined adaptively by I_O. In the master phase mirroring control for slave sub-converter, the ON-time of slave sub-converter T_{ONS} is enabled at the instant of $T_{SW}/2$. Then M_{SH} is turned on to pull slave sub-converter switching node voltage V_{SWS} to $V_{IN}/2$ and charge slave sub-converter inductor L_S for the same T_{ON}, followed by similar switching actions

described in the master sub-converter. In steady state with constant T_{ONM}, T_{SW} of the master sub-converter is constant because of the stable I_O. In the slave sub-converter, T_{ONS} is kept the same as T_{ONM} and the mirrored $T_{SW}/2$ phase delay is also constant. Therefore, the master and slave sub-converters are synchronized without reference clock. The automatic phase current balancing is accomplished by the two synchronized sub-converters consequently.

3.3.2 Circuit Implementation

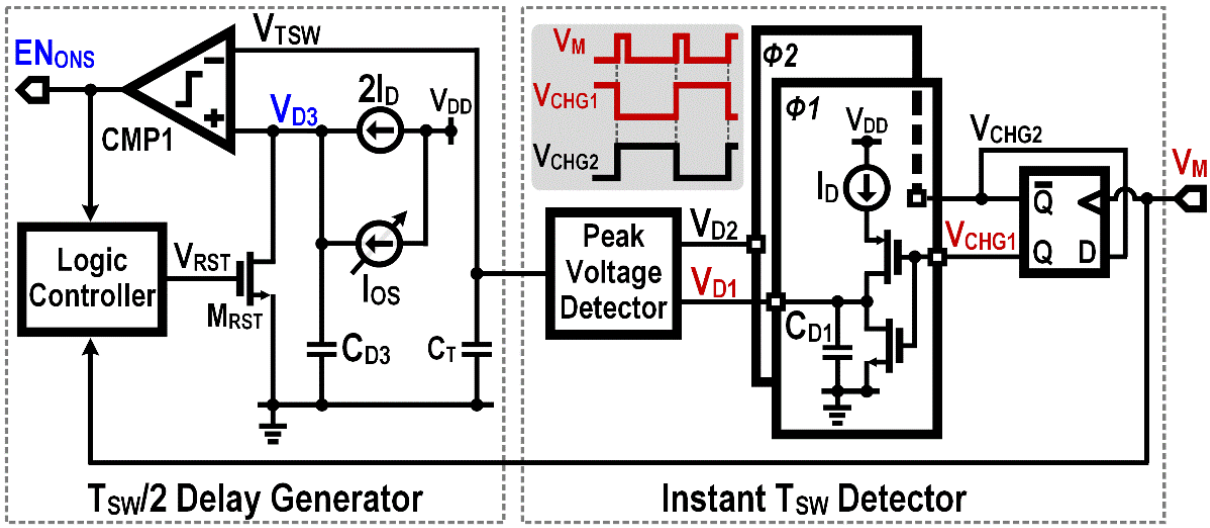


Figure 3.12. Circuit schematic of master phase mirror [Yan-20a].

Figure 3.12 depicts the schematic of master phase mirror. It includes an instant T_{SW} detector and a $T_{SW}/2$ delay generator. The instant T_{SW} detector records the instant $T_{SW}(t)$ determined by the feedback loop of the master sub-converter. Despite $T_{SW}(t)$ continuously varies with load, an instant V_{TSW} changes correspondingly to track the switching period of master sub-converter. The $T_{SW}/2$ delay generator uses V_{TSW} as a reference and generates instant $T_{SW}/2$ triggering signal for slave sub-converter. Thus, the master phase mirror copies the instant master phase ($=T_{SW}(t)/2$) immediately to the upcoming slave phase, achieving clock/phase synchronization without reference clock.

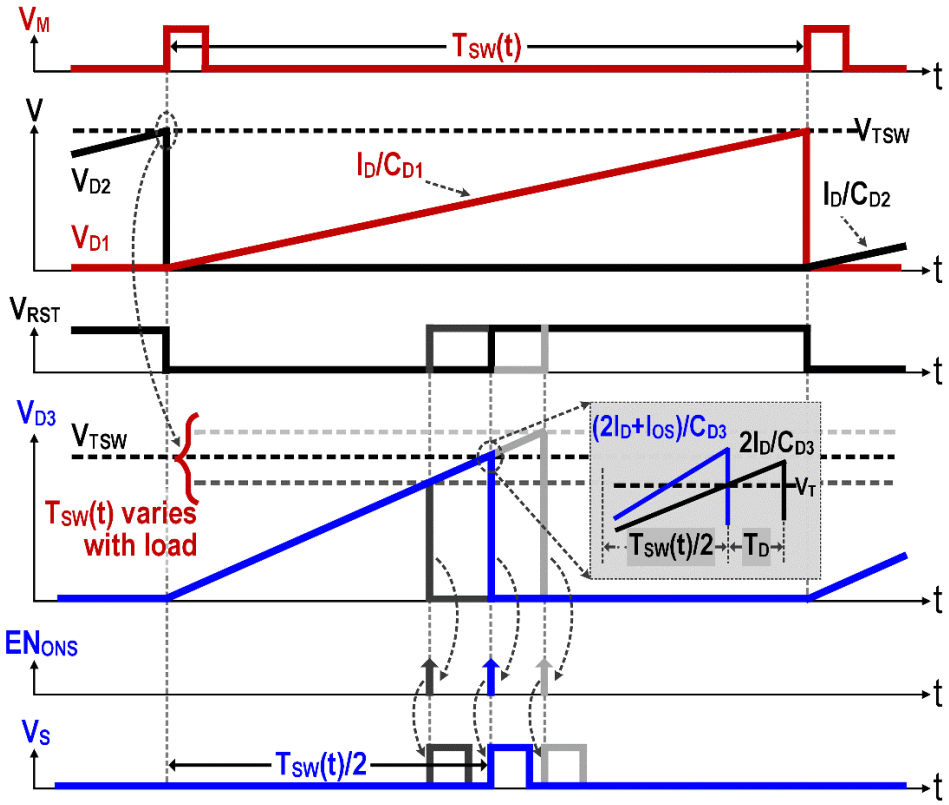


Figure 3.13. Operation waveforms of master phase mirror [Yan-20a].

The detailed operation waveforms are shown in Figure 3.13. At the start of a $T_{SW}(t)$, the master sub-converter gate drive signal V_M turns to logic high to initialize T_{ONM}. Meanwhile, the rising edge of V_M triggers I_D to charge the capacitor C_{D1} or C_{D2} alternately till the next switching cycle of V_M. At the end of this $T_{SW}(t)$, the respective V_{D1} or V_{D2} rises to its peak value V_{TSW},

$$V_{TSW} = T_{SW}(t) \times (I_D/C_{D1}). \tag{3.3}$$

Then the peak voltage detector records the peak value V_{TSW} and sends it to the $T_{SW}/2$ delay generator. In the next $T_{SW}(t)$, the rising edge of V_M sets V_{RST} logic low to turn off M_{RST}. Then the capacitor C_{D3} in the $T_{SW}/2$ delay generator is charged at a doubled rate by a current of $2I_D$. After a period of delay t_{delay}, the voltage on C_{D3}, V_{D3} reaches V_{TSW}. Then the comparator CMP1 sets EN_{ONS} high to turn on M_{RST} and V_{D3} resets to zero. As a result, one positive pulse of EN_{ONS} is

generated for master phase mirroring. The slave sub-converter gate drive signal V_S is thus triggered high to enable the ON-time of the slave sub-converter. The delay period t_{delay} equals

$$t_{delay} = V_{TSW} \times C_{D3}/(2I_D). \quad (3.4)$$

In the circuit and layout designs, the capacitors C_{D1}, C_{D2} and C_{D3} are kept same.

$$C_{D1} = C_{D2} = C_{D3}. \quad (3.5)$$

By combining equations (3.3), (3.4) and (3.5),

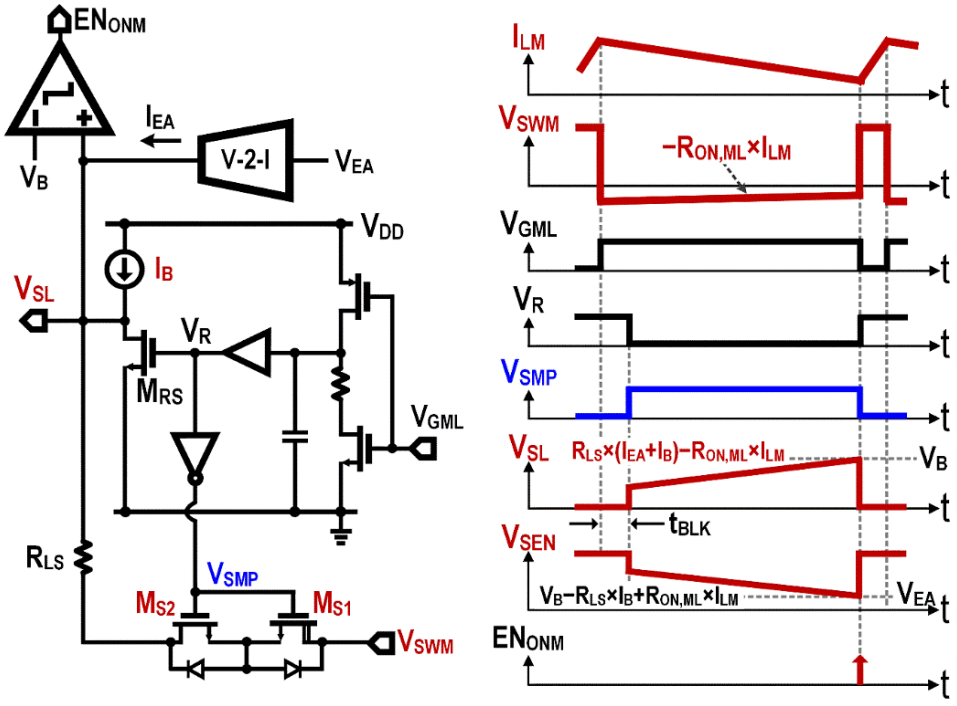
$$t_{delay} = T_{SW}(t)/2. \quad (3.6)$$

V_{D3} thus reaches V_{TSW} right at the instant of $T_{SW}(t)/2$, which initiates the ON-time of the slave sub-converter. The offset current I_{OS} in $T_{SW}/2$ delay generator is designed to compensate control loop delay adaptively in order to record the $T_{SW}/2$ delay precisely. As V_{TSW} is updated for different $T_{SW}(t)$ of master sub-converter, $T_{SW}/2$ delay generator realizes $T_{SW}(t)/2$ delay in each switching cycle according to different V_{TSW}.

As an important part for closed loop regulation, Figure 3.14(a) shows the circuit schematic of on-chip inductor current sensor in adaptive OFF-time controller. One HV NMOS M_{S1} and one LV NMOS M_{S2} operate as the back-to-back sampling switch to block V_{SWM} when V_{SWM} is high. M_{S1} and M_{S2} sense equivalent inductor current I_{LM} when V_{SWM} is low. The operation waveforms are presented in Figure 3.14(b). At the beginning of OFF-time in the master sub-converter, V_{SWM} falls below zero and the gate signal V_{GML} rises high to turn on the low-side power switch M_{ML}. Then V_{SWM} starts to rise due to the falling inductor current I_{LM}. After a blanking period t_{BLK}, V_R falls low and V_{SMP} rises high to turn on M_{S1} and M_{S2}. The current sensor starts to sense I_{LM} by sensing V_{SWM}. t_{BLK} is designed to avoid V_{SWM} ringing during its falling edge due to parasitic inductance and capacitance. With fixed bias current and shifting resistor, the voltage V_{SL} equals

$$V_{SL} = R_{LS} \times I_B - R_{ON,ML} \times I_{LM}. \quad (3.7)$$

Here, $R_{ON,ML}$ is the on-resistance of M_{ML}. When V_{GML} goes low, V_{SL} is set zero by switch M_{RS}. Therefore, V_{SL} contains inductor current I_{LM} information during the OFF-time of the master sub-converter and it can be used for its valley current mode control.



(a) (b)

Figure 3.14. On-chip inductor current sensor: (a) circuit schematic and (b) operation waveforms [Yan-20a].

3.4 Elastic ON-Time Modulation

3.4.1 Operation Scheme

During dynamic transients, I_O changes. In the conventional COT control, only the OFF-time T_{OFF} is modulated to respond to the new I_O while T_{ON} is fixed during load transition, which results in sluggish transient response and large V_O variations. To improve the load transient

response, the proposed elastic on-time modulation operation scheme is illustrated in Figure 3.15. During load transient, OFF-time of master and slave sub-converters are modulated by adaptive OFF-time control and master phase mirroring respectively. Meanwhile, T_{ON} is also elastically adjusted to satisfy the new I_O, making the control an adaptive ON-time control. Combining the adaptive OFF-time control in steady state and the adaptive ON-time control in dynamic transient, the converter thus accomplishes a truly adaptive ON-OFF-time control. Compared to COT control, the output voltage variation during load transition is reduced.

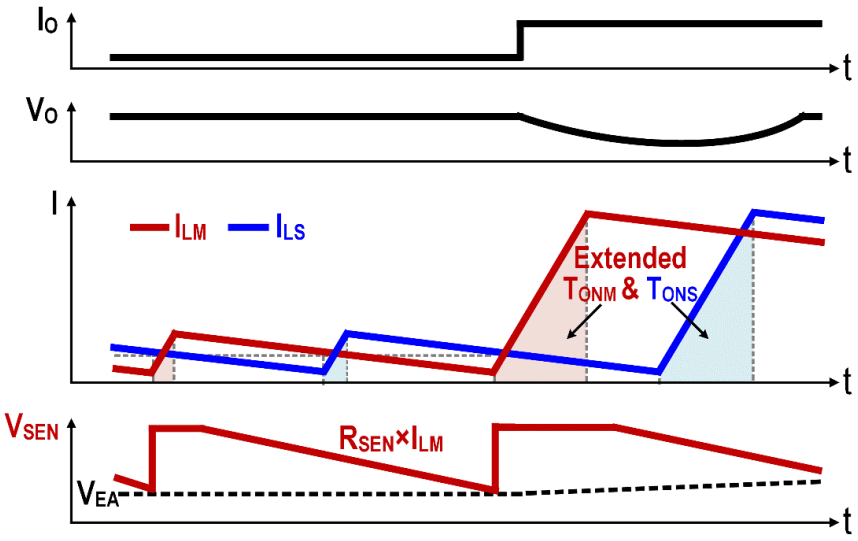


Figure 3.15. Proposed elastic ON-time modulation operation scheme [Yan-20a].

3.4.2 Circuit Implementation

Figure 3.16 shows the schematic of the proposed EOM. Master and slave sub-converters share one ON-time generator to realize the same ON-time. The T_{ON} overlap prevention module protects DSD architecture from cross-phase T_{ON} overlap for reliability. The detailed operation waveforms are explained in Figure 3.17. At the beginning of ON-time T_{ONM} or T_{ONS}, V_{RS} is triggered to logic low by V_M or V_S. Then the charge current I_{CON} starts to charge capacitor C_{ON}.

When the voltage V_{RMP} on capacitor C_{ON} reaches V_{REF}, the output of comparator CMP2 will generate a positive pulse of V_{CMP} to terminate the ON-time. Thus, the ON-time T_{ON} equals

$$T_{ON} = T_{ONM} = T_{ONS} = C_{ON} \times V_{REF}/I_{CON}. \tag{3.8}$$

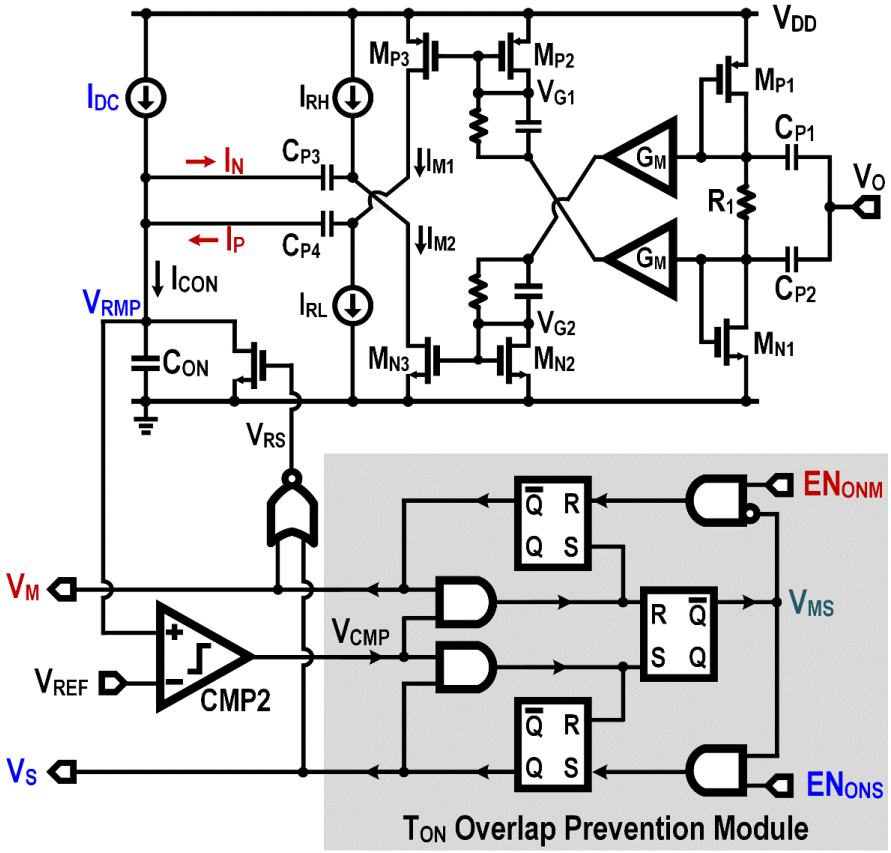


Figure 3.16. Circuit schematic of elastic ON-time modulator [Yan-20a].

In steady state, I_{CON} equals the constant current I_{DC} generating constant T_{ON}, which leads to fixed switching frequency. During load transient response, I_{CON} is modulated elastically to generate optimized T_{ON} for improved response. When I_O rises abruptly, V_O drops due to control loop delay. Two inverting OTA amplifiers, consisting of C_{P1}, C_{P2} and G_M modules, amplify the V_O drop at the outputs V_{G1} and V_{G2}. V_{G1} and V_{G2} increase accordingly. The increase of V_{G2} results in the I_{M2} increase. If I_{M2} exceeds a reference current I_{RH}, a portion of I_N would flow into M_{N3} to

compensate for the deficit. Hence, the charge current I_{CON} decreases. Note that the trip point of V_{RMP} and V_{REF} determines T_{ON} in the EOM. The reduced I_{CON} effectively reduces V_{RMP} rising slope and extends T_{ON} during I_O step-up. Similarly, when I_O steps down, the EOM responds to shorten T_{ON}. After load transients, T_{ON} in the *EOM* would remain constant in steady state, until the next load transient occurs.

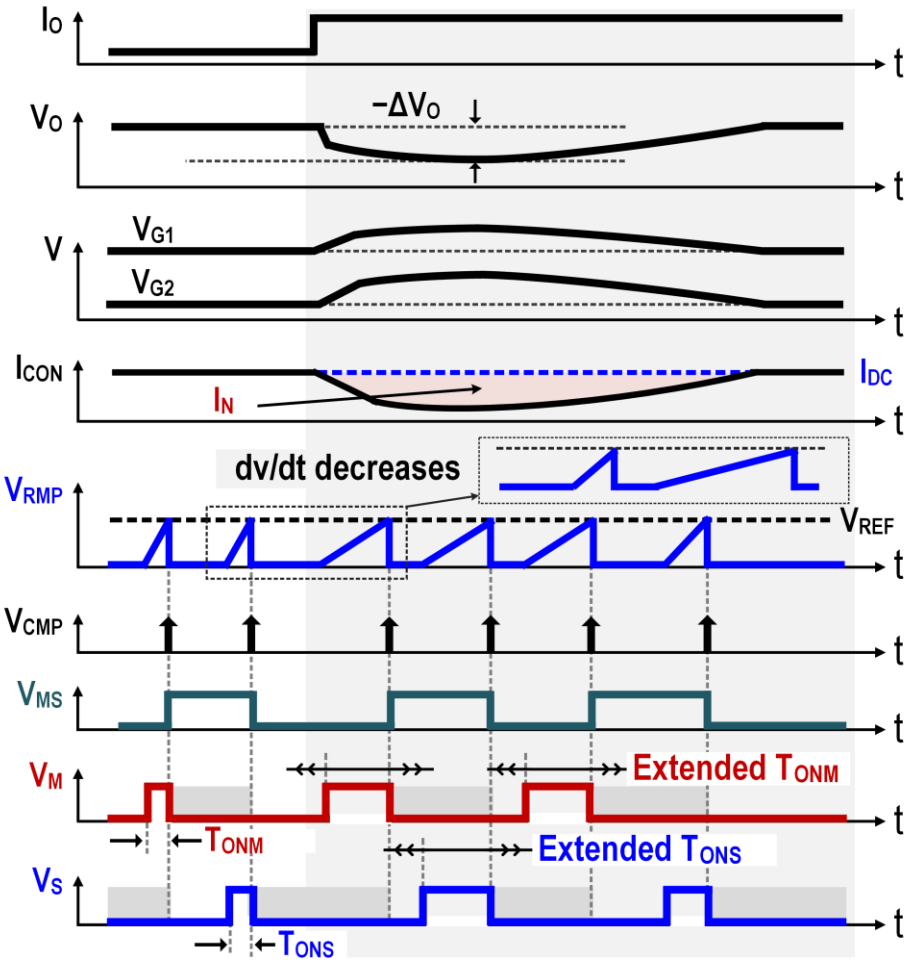


Figure 3.17. Operation waveforms of elastic ON-time modulator [Yan-20a].

Note that the above operations hold, only when $T_{ON}<T_{SW}/2$. For extreme I_O increase, T_{ON} may expand beyond $T_{SW}/2$. T_{ONM} and T_{ONS} would thus overlap, causing over-voltage stress and false charging issues. To prevent this, key operation waveforms of T_{ON} overlap prevention module

are illustrated in Figure 3.17. When T_{ONM} is active, the module sets the feedback signal V_{MS} to "0", which disables the T_{ONS} generation signal EN_{ONS} and thus the slave sub-converter gate drive signal V_S. T_{ONS} is thus blocked to avoid overlapping T_{ONM}. As T_{ONM} expires, the comparator CMP2 flips. V_{CMP} becomes "1" and thus turns V_{MS} to "1", which disables EN_{ONM} and activates EN_{ONS}. V_S turns into "1" to start T_{ONS}. Similarly, during T_{ONS}, the overlap prevention module blocks T_{ONM} until T_{ONS} expires.

3.5 Experimental Verification

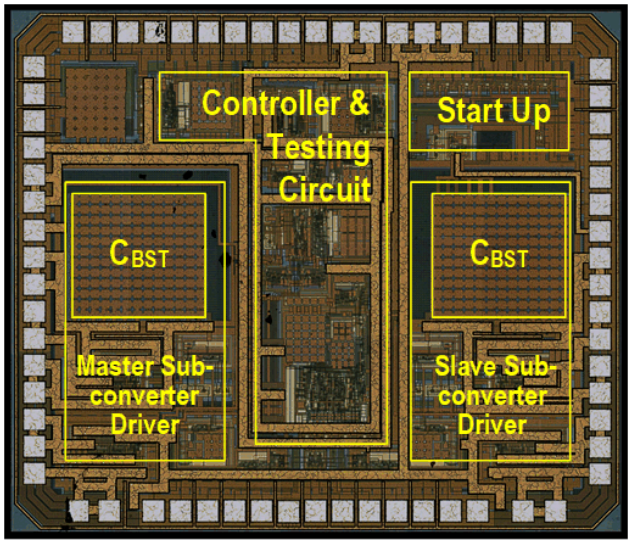


Figure 3.18. Chip micrograph [Yan-20a].

The proposed design is implemented using a 180-nm HV BCD process [Yan-19, Yan-20a]. Figure 3.18 shows the chip micrograph with integrated bootstrapped capacitors, driver circuits, controller and testing circuits. The active die area of the chip is 1.46mm^2. Figure 3.19. presents the photograph of the PCB test board. Four e-mode GaN HEMTs are used as the power switches in the DSD power converter. It achieves 2MHz in each sub-converter for direct 48V/1V dc-dc power conversion with two 0.9-µH inductors and one 22-µF output capacitor. It delivers the maximum

load current of 1.5A. The efficiency measurement results at various input voltages and switching frequency conditions are shown in Figure 3.20. The maximum efficiency for direct 48V/1V power conversion is 85.4%, 79% and 56.8% when the switching frequency of each sub-converter is 100kHz, 250kHz and 2MHz, respectively. As off-chip GaN switches are employed in this design, power transistor sizing techniques such as in [Song-15] are not applicable in this work, which partially leads to the lower efficiencies than the expected.

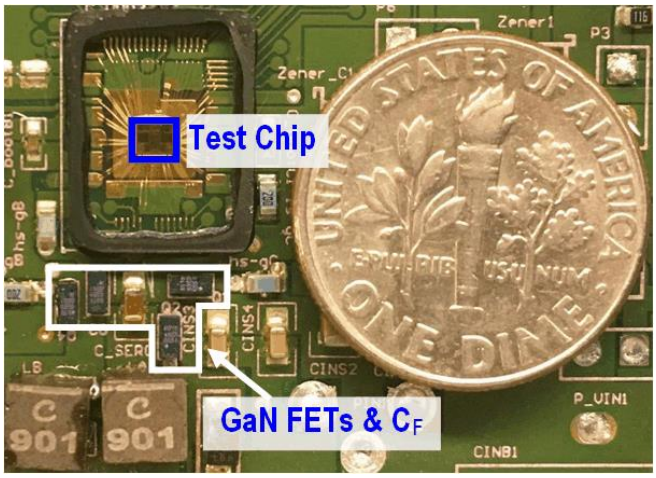


Figure 3.19. Photograph of PCB test board [Yan-20a].

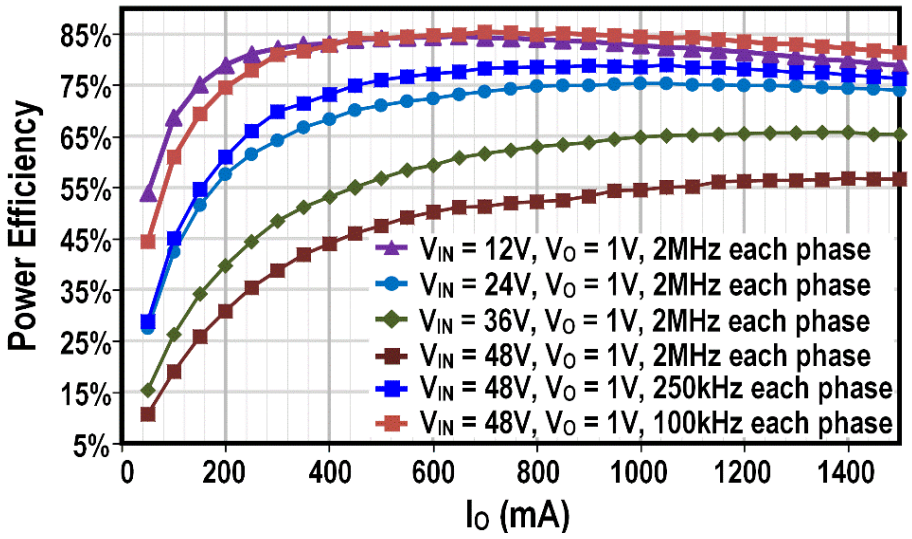


Figure 3.20. Measured efficiency [Yan-20a].

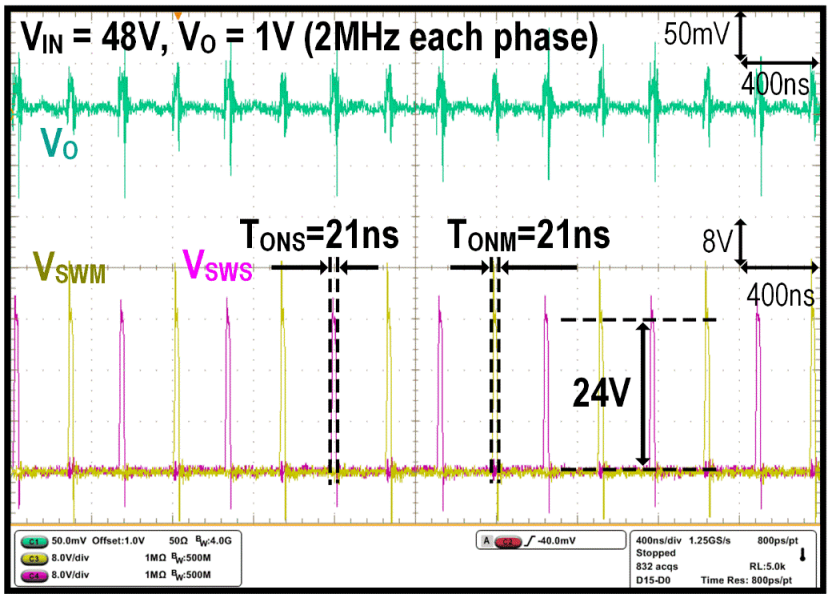


Figure 3.21. Steady state behavior measurements: T_{ONM} and T_{ONS} with reference to V_O [Yan-20a].

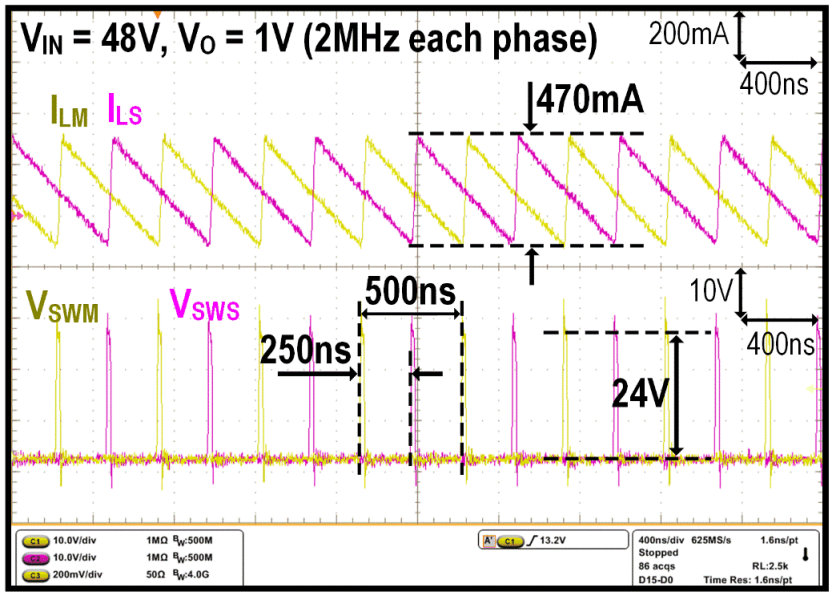
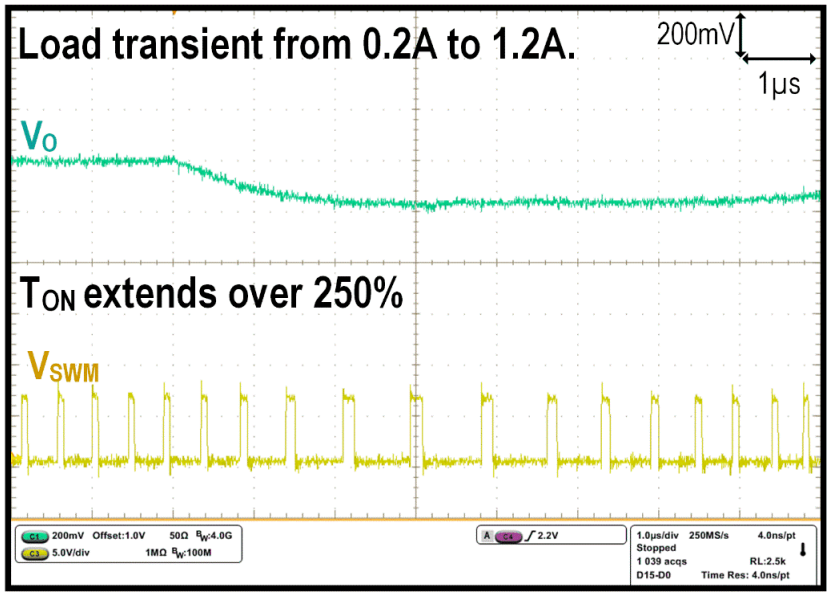


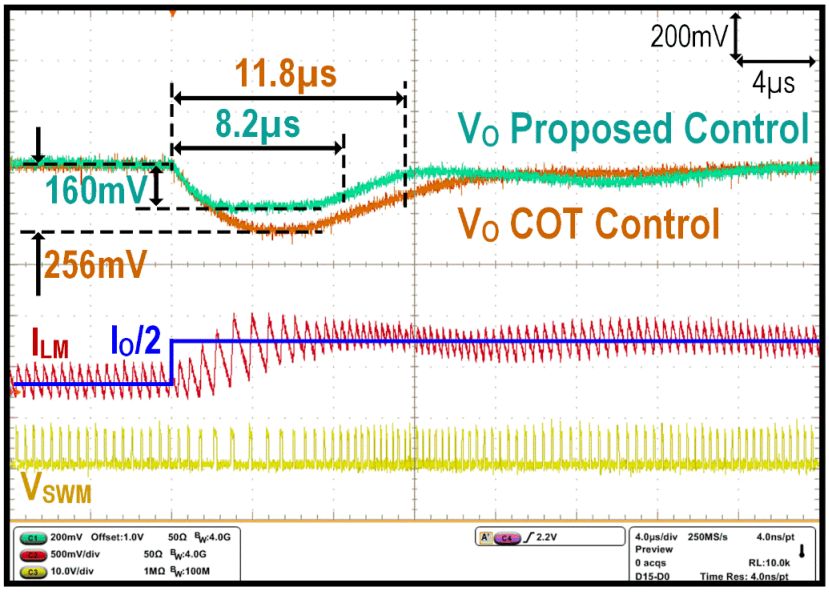
Figure 3.22. Steady state behavior measurements: balanced currents I_{LM} and I_{LS} with reference to T_{ONM} and T_{ONS} [Yan-20a].

To validate the switching operation, Figure 3.21 shows steady state behavior measurements of the 48V/1V power conversion at 200mA and 2MHz. T_{ONM} and T_{ONS} are steadily measured as 21ns with reference to V_O are shown in Figure 3.21. The switching nodes voltages V_{SWM} and V_{SWS}

switch between 0 and 24V, which clearly verify the well-regulated switching actions. In Figure 3.22, the balanced I_{LM} and I_{LS} prove the phase synchronization and automatic phase current balancing, thanks to the master phase mirror.

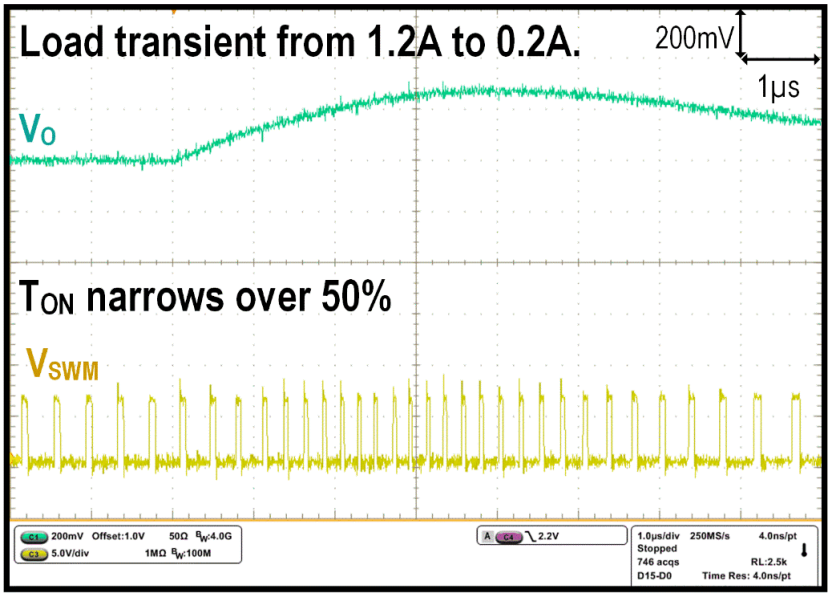


(a)

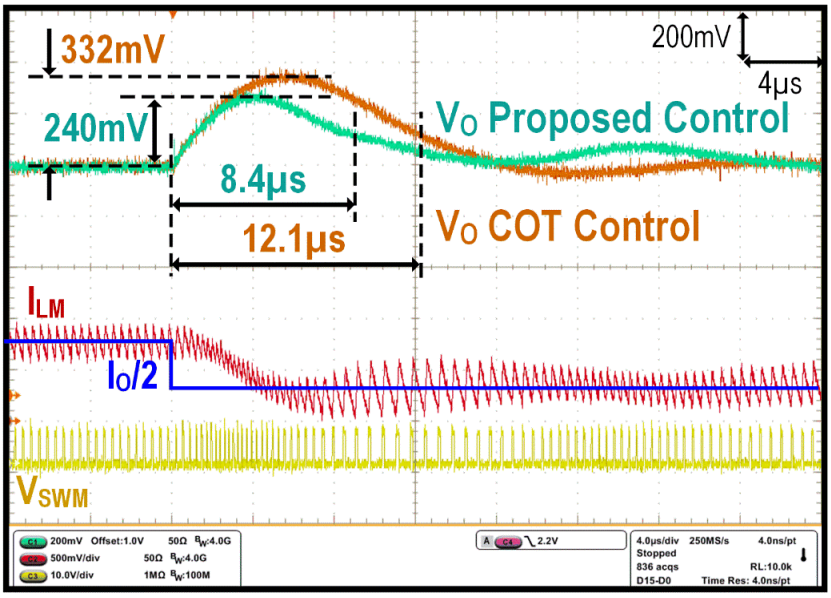


(b)

Figure 3.23. Load step-up transient behavior measurements: (a) T_{ON} modulation with reference to V_O undershoot, and (b) transient performance comparison with COT control [Yan-20a].



(a)



(b)

Figure 3.24. Load step-down transient behavior measurements: (a) T_{ON} modulation with reference to V_O overshoot, and (b) transient performance comparison with COT control [Yan-20a].

Figure 3.23 shows the load step-up transient behavior measurements when V_{IN} is at 12V, and V_O is at 1V. As shown in Figure 3.23(a), in response to 1-A load step-up, the ON-time of the converter is extended by over 250% from the steady state, thanks to the EOM circuit. Figure

3.23(b) shows its transient response comparison with a classic fast transient COT control counterpart. It reduces the V_O undershoot from 256mV to 160mV and the 10% settling time from 11.8µs to 8.2µs, with the AO^{2}T control. Figure 3.24 presents the transient response of 1-A load step-down. Thanks to the AO^{2}T control, the ON-time is reduced by over 50% in Figure 3.24(a). Compared to the COT control, V_O overshoot is suppressed from 332mV to 240mV, with a 10% settling time reducing from 12.1µs to 8.4µs in Figure 3.24(b). In addition, in all transient tests, the swing of V_{SWM} is kept as half of V_{IN}, proving that the cross-phase T_{ON} overlap is successfully prevented. Figure 3.25 illustrates the overview load transient response with the measured V_O, I_{LM}, V_{SWM}. Well-regulated V_O is achieved during load transients and T_{ON} overlap is avoided constantly.

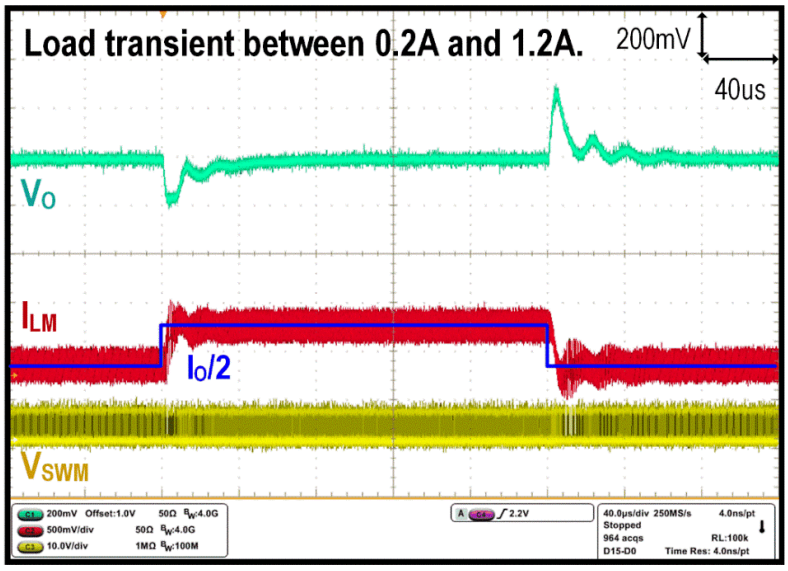


Figure 3.25. The measured load transients between different I_O values.

Finally, Table 3.1 compares this work to the prior arts of DSD power converters [Nishijima-05, TI-16, Shenoy-16, Vekslender-16]. With 4 times higher input voltage, this design faces 4 times higher switching loss, 16 times higher output capacitor loss and 4 times higher breakdown voltage, making it much more challenging to switch faster and remain efficient. This is reflected in the efficiency results. On the other hand, due to limited options on GaN switches,

optimal transistor sizing is not implemented in this design, which contributes to another factor of lower peak efficiency. In terms of operation speed, thanks to the proposed circuit techniques, it achieves almost 5 times lower minimum equivalent duty ratio of 2.1% at 2MHz.

Table 3.1. Performance comparison of proposed GaN DSD converter to prior arts [Yan-20a].

Design	[Nishijima-05] INTELEC 2005	[TI-16] TI TPS54A20	[Shenoy-16] APEC 2016	[Vekslender-16] APEC 2016	This Work
Architecture	DSD Power Stage Only	DSD Power Converter	DSD Power Converter	DSD Power Converter	DSD Power Converter
Implementation	Board Level	On-chip	On-chip	Board FPGA	On-chip
Input Voltage	12V	12V	12V	12	48V
Output Voltage	1.5V	1.2V	1.2V	1.5	1V
Minimum Duty Ratio	12.5%	10%	10%	12.5%	2.1%
Maximum Switching Frequency	250kHz	2MHz	5MHz	1.25MHz	2MHz
Inductor	0.45µH	0.22µH	0.1µH	0.6µH	0.9µH
Output Capacitor	660µF	94µF	91µF	50µF	22µF
Flying Capacitor	47µF	2.2µF	1µF	10µF	1µF
Power Switch Type	Silicon FET	Silicon FET	Silicon FET	Silicon FET	GaN HEMT
Maximum Load Current	40A	10A	10A	8A	1.5A
Peak Efficiency	93% (Open loop)	85%	87.7% @ 2MHz	Not Reported	85.4% @ 100kHz, 79% @ 250kHz, 56.8% @ 2 MHz

3.6 Summary

In this chapter, the designed GaN-based two-phase DSD power converter is presented, which achieves direct 48V/1V power conversion at 2MHz. The proposed master–slave AO^{2}T control facilitates clock-free phase synchronization and automatic phase current balancing without extra control circuits. Meanwhile, with the proposed elastic ON-time modulation scheme, the load transient response is largely improved compared to conventional COT control. In addition, the converter is designed to prevent cross-phase T_{ON} overlap on all occasions for improved reliability. The experimental results successfully validate the proposed techniques and circuits in this design.

CHAPTER 4

HIGH V_{IN}/V_O GAN-BASED DC-DC CONVERSION WITH EMI REGULATION[†]

Regarding Section 1.2.2, the electronic equipment in the electronic systems is vulnerable to EMI noise. To ensure reliable operation of the whole system, EMC standards specify that EMI noise generated by a switching power converter should be below specific values in specific frequency ranges. Conventionally, the passive EMI filters are widely used to reduce the EMI noise. But they have to consume large area, compromising the power density of power converter. In order to attenuate the EMI noise with low cost, this chapter proposes one effective and efficient EMI reduction technique for high step-down ratio GaN-based dc-dc converter. The inherent EMI noise challenges of high V_{IN}/V_O dc-dc power converter with fixed f_{SW} and the dilemma of conventional SSM techniques are firstly discussed in Section 4.1. Then in Section 4.2, the proposed GaN-based dc-dc converter with the anti-aliasing MR-SSM technique is presented to suppress EMI noise effectively in high V_{IN}/V_O power converter. Meanwhile, the in-cycle adaptive ZVS technique is developed to maintain optimized ZVS regardless of continuous f_{SW} variation in SSM operation. The efficiency deteriorations due to frequency modulation can thus be overcome. The detailed circuit implementations are illustrated in Section 4.3, which include multi-rate T_{ON} generator, elastic t_{dead} controller and pulse-reinforced up-level shifter. After that, the measurement results are shown in Section 4.4 to verify the functionality and performance of the proposed design. Finally, a summary of this chapter is given.

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4.1 Design Considerations of Low EMI High V_{IN}/V_O Direct Power Conversion

4.1.1 EMI Deterioration in High V_{IN}/V_O Direct Power Conversion

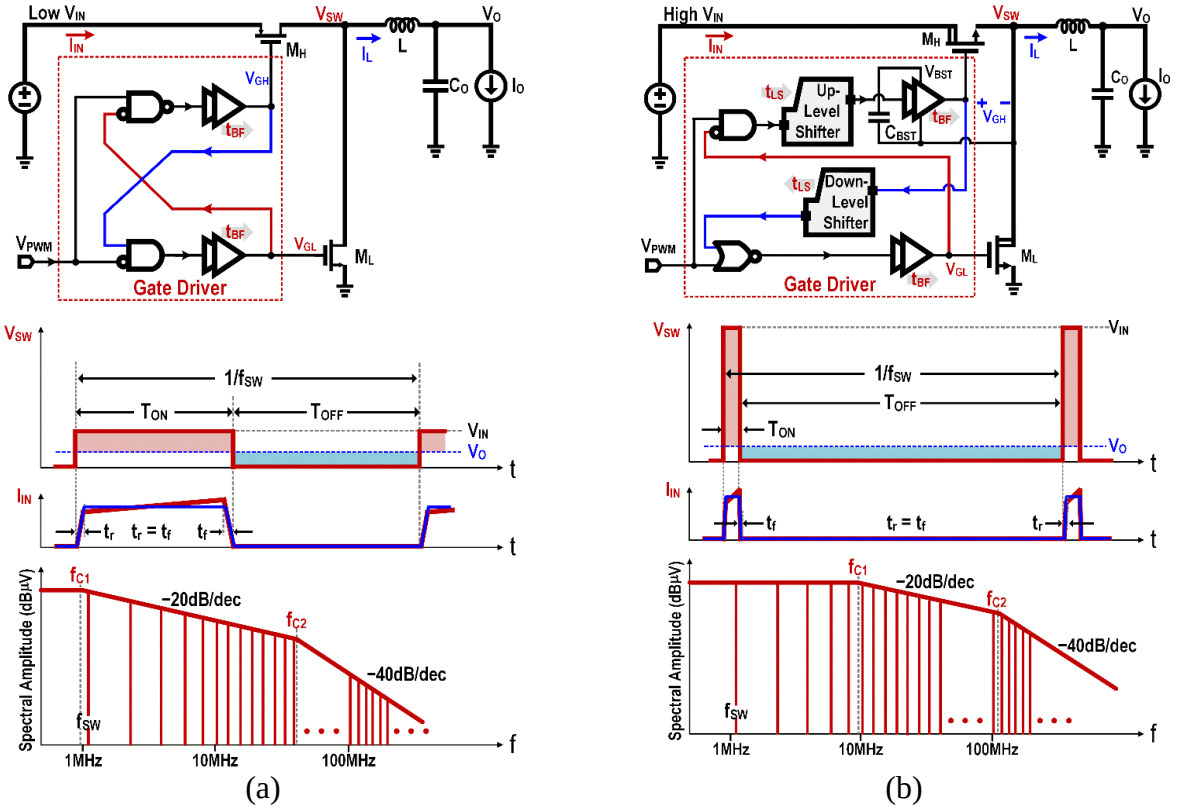


Figure 4.1. Key switching operation behaviors of (a) a classic low-V_{IN} half-bridge power converter, and (b) a high-V_{IN} bootstrapped half-bridge power converter [Yan-21].

The single-stage power conversion structure is advantageous over classic multi-stage power conversion structures in saving area and power cost. However, in power electronic system, the EMI emission noise, which would affect system reliability and signal communications, should also be well-regulated to satisfy standard EMI specifications [Hegarty-18]. The EMI noise performance in high V_{IN}/V_O power conversion becomes different from classic low V_{IN}/V_O power conversion. Theoretically, in steady state, f_{SW} of a classic half-bridge power converter equals

$$f_{SW} = V_O/(V_{IN} \times T_{ON}). \tag{4.1}$$

It is clear that T_{ON} is affected by V_{IN}/V_O for a constant f_{SW}. Compared to the low-V_{IN} half-bridge converter in Figure 4.1(a), V_{IN}/V_O of the high-V_{IN} half-bridge converter in Figure 4.1(b) increases greatly. Thus, T_{ON} has to be shortened significantly, if both operate at the same high f_{SW}, inducing many design challenges of gate drivers, level shifters and feedback controllers [Yan-20a]. In the meantime, because of the extreme short T_{ON}, EMI noise elevates drastically in the high-V_{IN} half-bridge converter, which would negatively affect the reliability of automotive electronics. In the half-bridge converter, the switching transitions of switching node voltage V_{SW} and input current I_{IN} have been considered highly associated with the EMI noise [Roy-16]. As shown in Figure 4.1(a), V_{SW} and I_{IN} rise high during T_{ON} and fall to zero during the OFF-time (T_{OFF}). If the ripples at V_{SW} and I_{IN} during T_{ON} are ignorable, V_{SW} and I_{IN} can be simplified as trapezoidal waveforms. The spectral envelope of the trapezoidal waveform in the frequency domain is obtained by Fourier analysis to represent the corresponding EMI noise spectrum. In the spectrum, the two corner frequencies f_{c1} and f_{c2} can be computed as [Mardiguian-00]

$$f_{c1} = 1/(\pi \times T_{ON}), \tag{4.2}$$

$$f_{c2} = 1/(\pi \times t_r). \tag{4.3}$$

Here, t_r represents the rise time of the trapezoidal waveform and is assumed equal to the fall time t_f. f_{c1} is relatively low and is affected by T_{ON}, while f_{c2} stays high and is determined by t_r. Above f_{c1}, the locus of the maximum amplitudes rolls off at a rate of 20dB/dec until f_{c2}. Beyond f_{c2}, it decays at 40dB/dec. For the low-V_{IN} half-bridge converter in Figure 4.1(a), f_{c1} can be lower than the fundamental switching frequency f_{SW} due to the long T_{ON}, and the amplitudes of f_{SW} and its harmonics decrease along with frequency. However, in the high-V_{IN} half-bridge converter, as shown in Figure 4.1(b), f_{c1} becomes much higher than f_{SW} because of the extremely short T_{ON}.

Thus, the amplitudes of f_{SW} and its low harmonics do not decrease along with the frequency, inducing much higher EMI noise around low frequency region. Furthermore, the short T_{ON} demands much shorter t_r, pushing f_{c2} higher. Hence, the EMI noise around higher harmonics of f_{SW} also elevates, aggravating the challenges of EMI suppression.

4.1.2 Dilemma of SSM Techniques

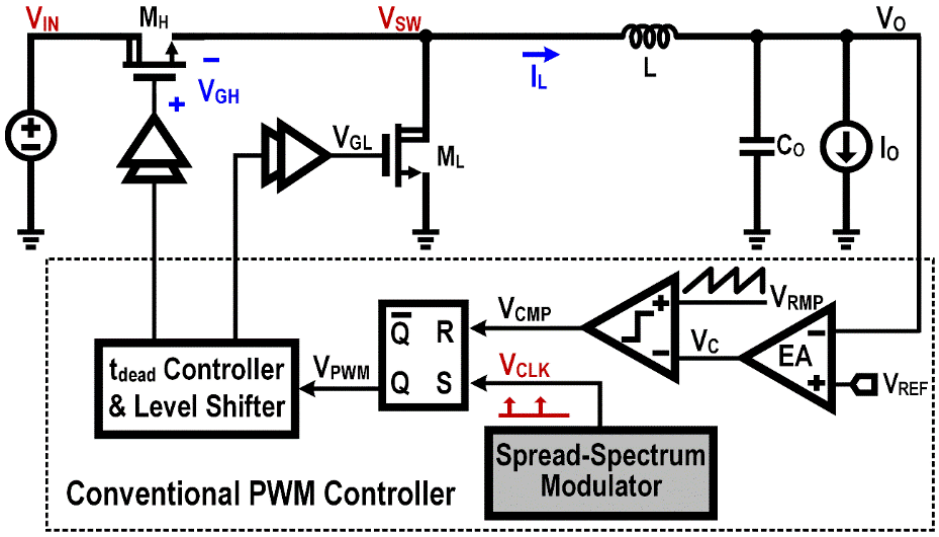


Figure 4.2. Applying spread-spectrum modulation to a power converter [Yan-21].

Conventionally, SSM techniques have been reported in power converters to attenuate EMI [Gonzalez-07, Ke-18, Ho-10, Chen-19]. Figure 4.2 shows a simplified construction of applying a spread-spectrum modulator to a PWM controlled half-bridge power converter. The controller senses V_O and generates a triggering signal V_{CMP} for closed-loop regulation. By controlling the frequency of clock signal (V_{CLK}), the modulator determines f_{SW} of the converter directly. For the SSM operation, f_{SW} varies constantly rather than staying constant. Since the total EMI noise energy is constant based on the Carson's rule, the high EMI spikes, which concentrate at fixed f_{SW} and its harmonics, would be compressed to a wide frequency range, leading to peak EMI noise suppression.

However, the challenge is on the degree of its effectiveness and complexity. One most straightforward way of such is the FR-SSM, as illustrated in Figure 4.3. In an FR-SSM, f_{SW} is periodically modulated at a fixed rate within a specific SSM frequency range (Δf) [Gonzalez-07, Ke-18]. The EMI suppression effectiveness can be expressed by a modulation index m_f, which is

$$m_f = \Delta f / f_M. \tag{4.4}$$

Here, f_M is modulation frequency. Theoretically, a lower f_M or higher Δf generates a higher m_f, enhancing EMI reduction [Chen-19, Tse-02]. However, under certain EMI/EMC regulation standards, f_M cannot be extremely low and should be higher than the specified EMI measurement bandwidth. Besides, it is often kept higher than 20kHz to avoid audible noise [Tse-02, Deutschmann-13]. Meanwhile, Δf cannot be too high either.

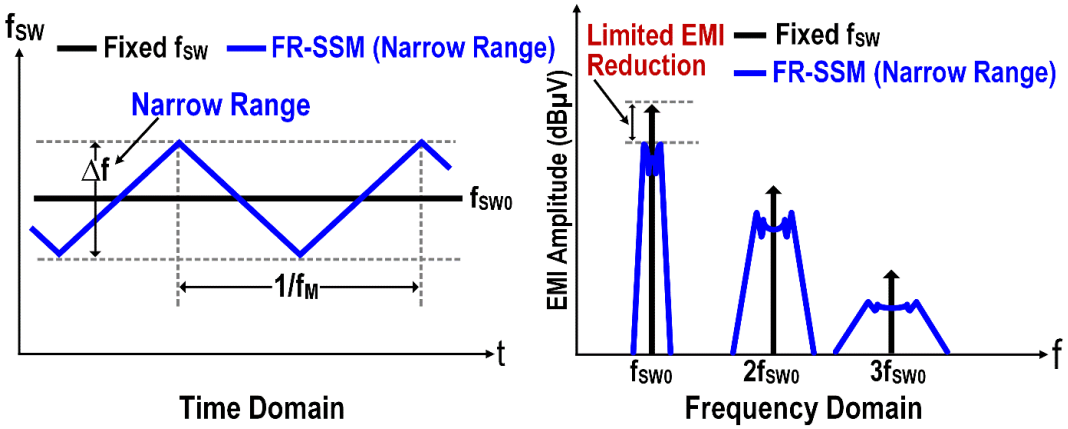


Figure 4.3. Illustrations of FR-SSM technique with a narrow SSM frequency range [Yan-21].

Theoretically, the EMI noise can be reduced further by extending the SSM frequency range Δf. As shown in Figure 4.4, although EMI spikes are reduced more significantly with a wider Δf, large power aliasing spikes would occur around fundamental and harmonics of the SSM frequency range, deteriorating the EMI reduction performance. The worst case is often found in the high V_{IN}/V_O power conversion, which, as addressed earlier, is much difficult to achieve high f_{SW} due to the

extremely shortened T_{ON}. For example, if f_{SW} is 10MHz, ±5% of f_{SW} SSM frequency range would achieve significant EMI reduction. But if f_{SW} drops to 1MHz, the SSM frequency range would have to be ±50% of f_{SW} to achieve a similar level of EMI reduction. With such a large percent of SSM frequency range, EMI power aliasing spikes would much more likely to occur, countering the EMI reduction effect seriously.

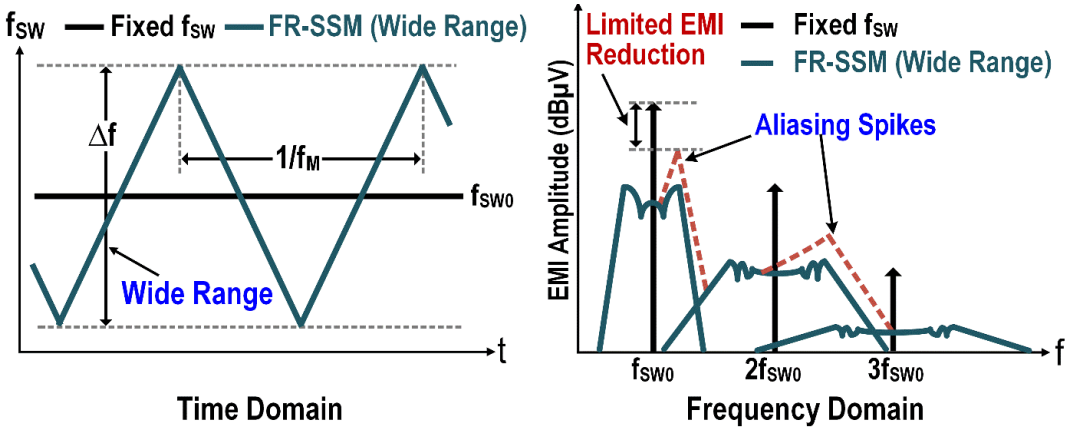


Figure 4.4. Illustrations of FR-SSM technique with a wide SSM frequency range [Yan-21].

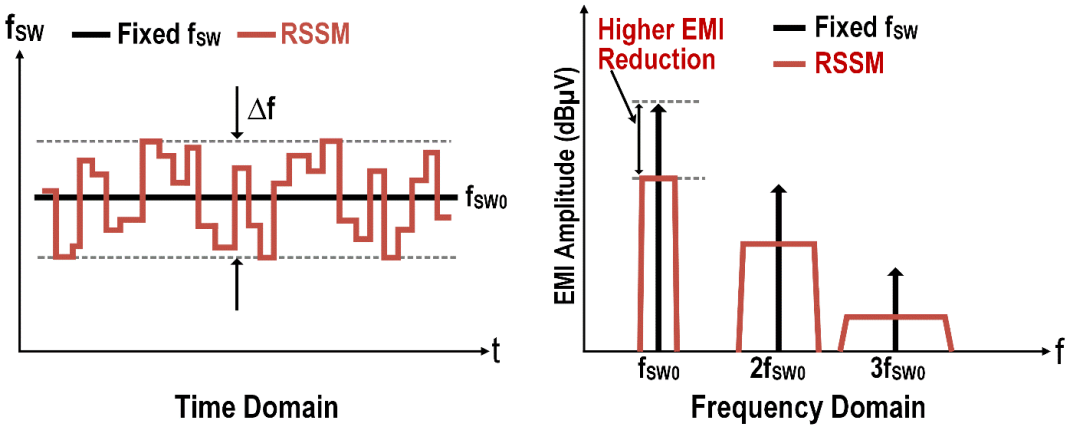


Figure 4.5. Illustration of RSSM technique [Yan-21].

Compared with FR-SSM, random spread-spectrum modulation (RSSM) approach in Figure 4.5 is usually more effective [Ho-10, Chen-19]. In an RSSM, f_{SW} is modulated in a random pattern with an equivalent zero f_M. For the same Δf, the EMI reduction of RSSM is more effective. However,

circuit design and implementation on RSSM become much more complicated. Besides, continuously random f_{SW} complicates the V_O regulation, another important performance parameter in a dc-dc power converter. There would be obvious V_O jittering if conventional feedback regulation circuits were used to regulate V_O in RSSM. To achieve tight V_O regulation, specific control circuity would be needed, which requires far more power and silicon overheads.

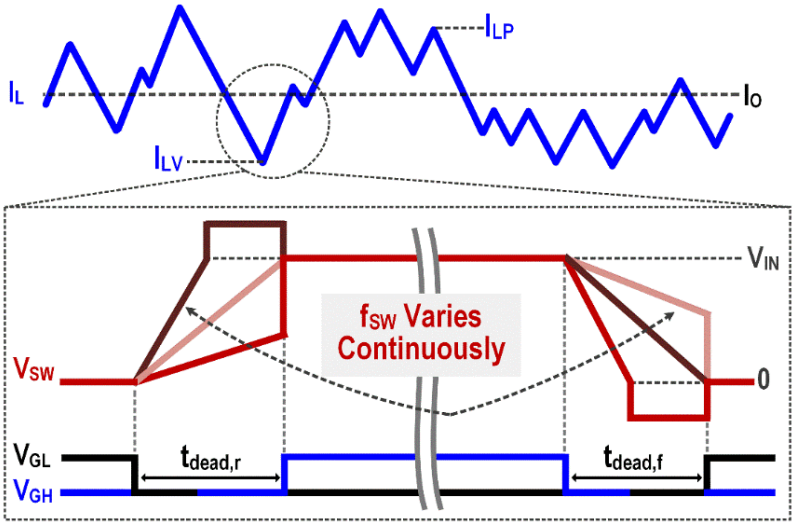


Figure 4.6. Non-ideal ZVS operation due to SSM techniques [Yan-21].

In addition, although the SSM techniques reduce EMI noise, they deteriorate the efficiency due to its complication on the power switches ZVS execution. As shown in Figure 4.6, as f_{SW} is modulated continuously, I_L varies between switching cycles. If the conventional fixed t_{dead} control is adopted in the driver circuits, continuously varying peak and valley inductor currents I_{LP} and I_{LV} will induce non-ideal ZVS of power switches M_H and M_L. The efficiency is thus degraded by the extra reverse conduction loss and switching loss. The degradation exacerbates in a GaN-based power converter due to the large reverse voltage drop and reverse conduction loss of a GaN HEMT, which lacks a body diode. To minimize power loss during t_{dead}, several t_{dead} schemes were reported [Ke-21, Lee-11, Wittmann-15]. In [Ke-21], by sensing load current and input voltage in a fixed

f_{SW} half-bridge buck converter, t_{dead}s are adjusted to minimize the power loss. [Lee-11] proposes a closed-loop t_{dead} optimization technique in a low-voltage half-bridge buck converter. The switching node voltage is captured in each switching cycle with stable I_{LP} and I_{LV}, and the gate driver delays are calibrated for a near-optimal t_{dead} control. One digital t_{dead} modulation scheme for a high-voltage half-bridge converter is presented in [Wittmann-15]. The high switching node voltage is sensed and compared with reference voltages to adjust the number of digital delay cells for t_{dead} optimization. However, the above t_{dead} optimization techniques only work with fixed f_{SW}, I_{LP} and I_{LV}, and are not compatible with SSM techniques.

4.2 System Architecture and Operation Techniques

4.2.1 System Architecture

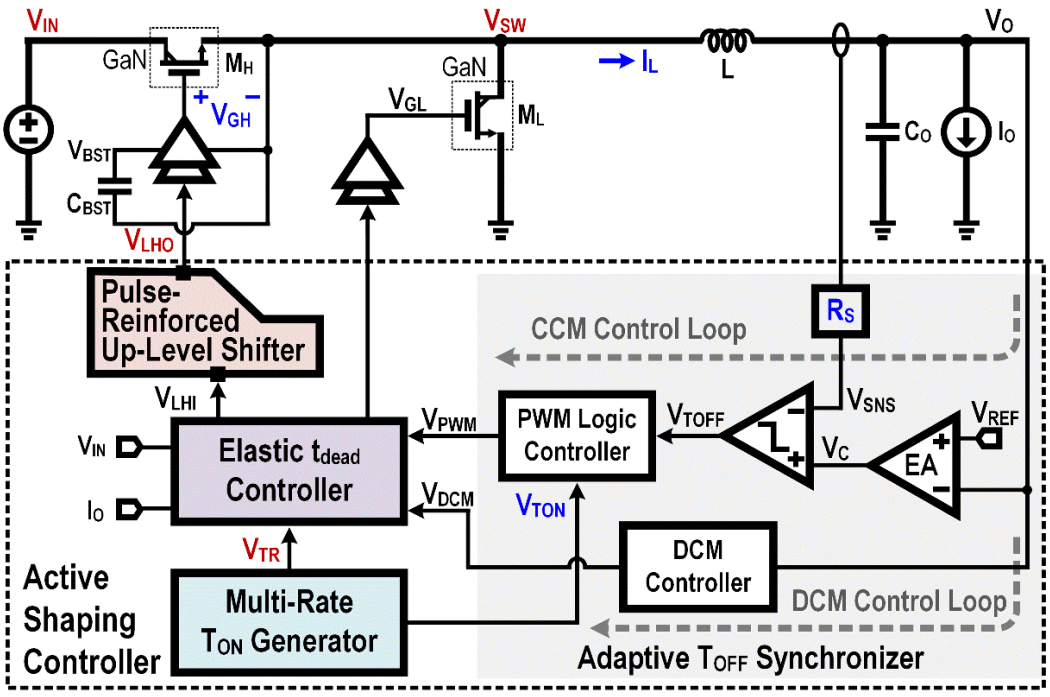


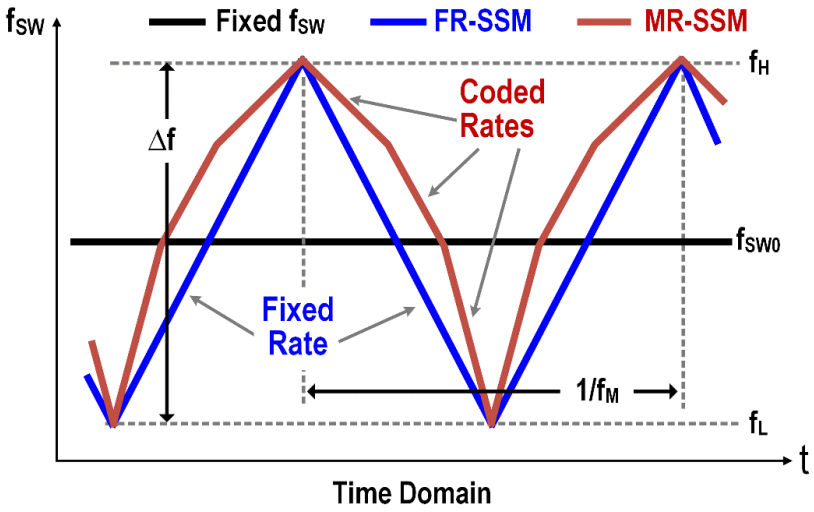
Figure 4.7. Block diagram of the proposed high-V_{IN} bootstrapped half-bridge power converter [Yan-21].

Figure 4.7 illustrates the system architecture of the proposed power converter. It primarily consists of a GaN-based half-bridge power stage, gate driver, elastic t_{dead} controller, pulse-reinforced (PR) up-level shifter, multi-rate T_{ON} generator (MRTG) and adaptive T_{OFF} synchronizer. In the power stage, two n-channel e-mode GaN HEMTs are employed as power switches to achieve superior switching performance. To realize anti-aliasing MR-SSM for effective EMI attenuation in the high V_{IN}/V_O power conversion, the MRTG and adaptive T_{OFF} synchronizer are employed for active shaping control. Besides, the elastic t_{dead} controller accomplishes in-cycle adaptive ZVS during SSM operation, maintaining high efficiency regardless of continuously variable f_{SW}. To enhance the driving reliability, the PR up-level shifter is proposed to immune the high V_{SW} dv/dt transition. Moreover, to realize high efficiency over a wide load current I_O range, the DCM control loop is designed for light load efficiency improvement.

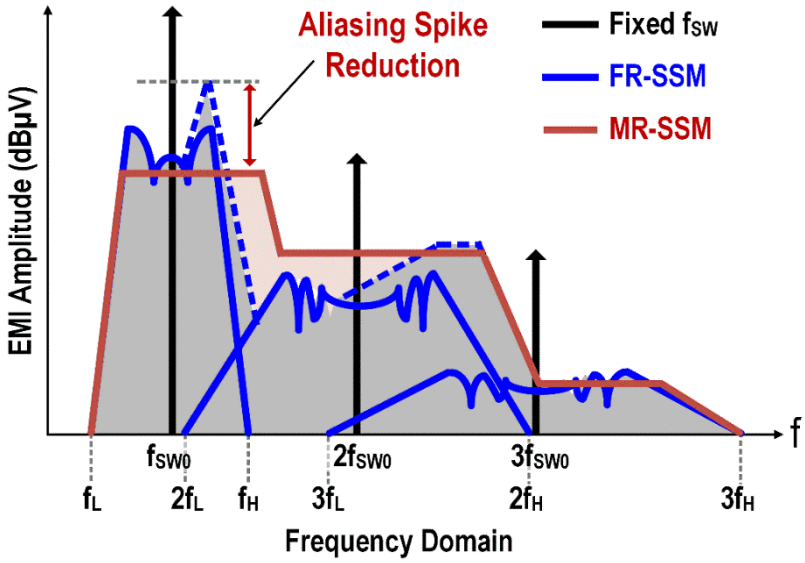
4.2.2 Anti-Aliasing MR-SSM Technique

As described in Section 4.1, although a wider FR-SSM frequency range can achieve better EMI noise reduction, the generated power aliasing spikes would compromise the improvement. This problem becomes significant for the high V_{IN}/V_O power conversion with limited achievable f_{SW}. Although the absolute value of SSM range is small, it would take a high percentage of the low f_{SW} and induce aliasing spikes between fundamental and harmonic ranges. Based on these analyses, an anti-aliasing MR-SSM technique is proposed to both extend SSM frequency range and avoid the power aliasing spikes. As is shown in Figure 4.8, compared to the classic FR-SSM, which modulates f_{SW} with a fixed rate and spreads EMI noise equally, it successfully achieves a targeted redistribution of EMI energy by adapting the f_{SW} modulation rate to the frequency range. As illustrated in Figure 4.8(a), there are three different f_{SW} modulation rates for different f_{SW} ranges. Specifically, A lower

f_{SW} is modulated with a faster rate, reducing its occurrence in the time domain. Thus, in Figure 4.8(b), the spectra show that the EMI energy carried by such a frequency component and its corresponding harmonics is suppressed, eliminating the EMI power aliasing spikes, which are inevitable in FR-SSM.



(a)



(b)

Figure 4.8. Comparison of the proposed anti-aliasing MR-SSM with FR-SSM in (a) time domain, and (b) frequency domain [Yan-21].

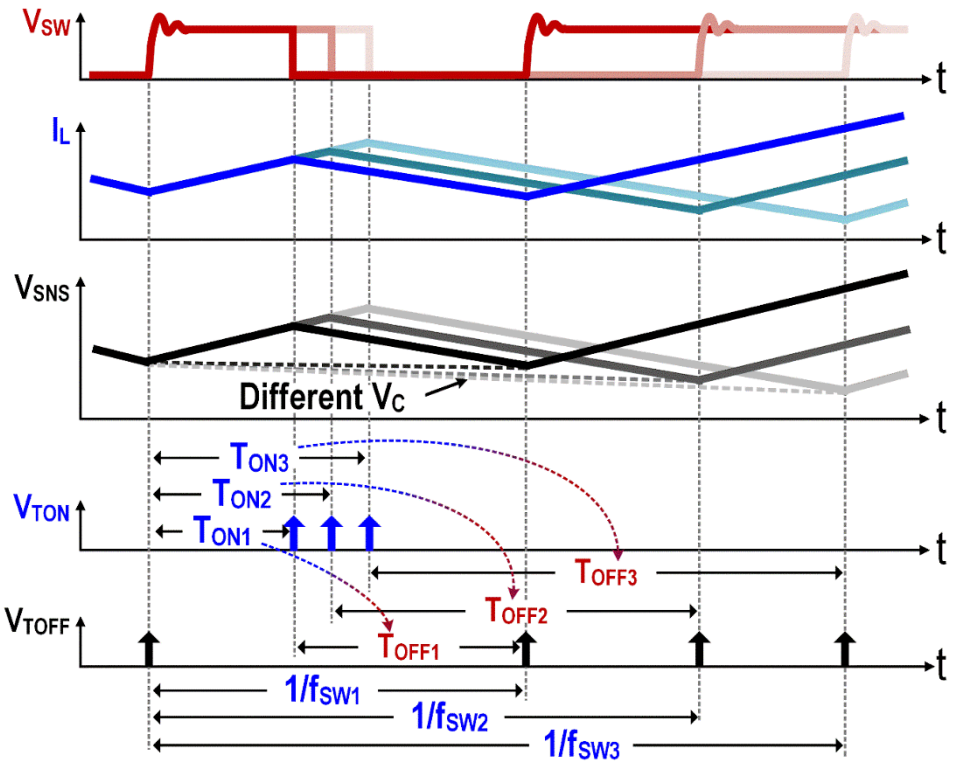


Figure 4.9. Illustration of the active shaping control for the anti-aliasing MR-SSM [Yan-21].

The anti-aliasing MR-SSM technique is executed by an active shaping control. Instead of being modulated directly in conventional methods, f_{SW} is modulated indirectly by the actively controlled T_{ON} and adaptively synchronized T_{OFF}. The MRTG modulates T_{ON} on basis of the predefined multi-rate T_{ON} pattern, while T_{OFF} is controlled by the adaptive T_{OFF} synchronizer shown in Figure 4.7. As illustrated in Figure 4.9, V_{SNS} represents the sensed voltage of inductor current I_L, and V_C is the output of the error amplifier (EA) through the comparison between V_O and reference voltage V_{REF}. In each switching cycle, T_{ON} is initialized by V_{TOFF} when V_{SNS} falls below V_C. Then the GaN switch M_H is turned on and V_{SW} rises to V_{IN} to charge the inductor L until T_{ON} expires. On the other hand, T_{ON} is actively terminated by V_{TON} from MRTG, which modulates the value of T_{ON} directly with coded rates. Within one MR-SSM cycle ($1/f_M$), T_{ON} gradually increases from its

minimum to maximum, and then decreases gradually to its lower boundary again. In response to a longer T_{ON}, T_{OFF} is extended correspondingly while retaining a near-constant T_{ON}/T_{OFF}, and thus a tight V_O regulation. The instant f_{SW} of half-bridge converter is computed as

$$f_{SW} = 1/(T_{ON} + T_{OFF}). \tag{4.5}$$

Thus, with a multi-rate T_{ON} modulation profile, multi-rate f_{SW} is modulated indirectly for anti-aliasing MR-SSM.

4.2.3 In-Cycle Adaptive ZVS Technique

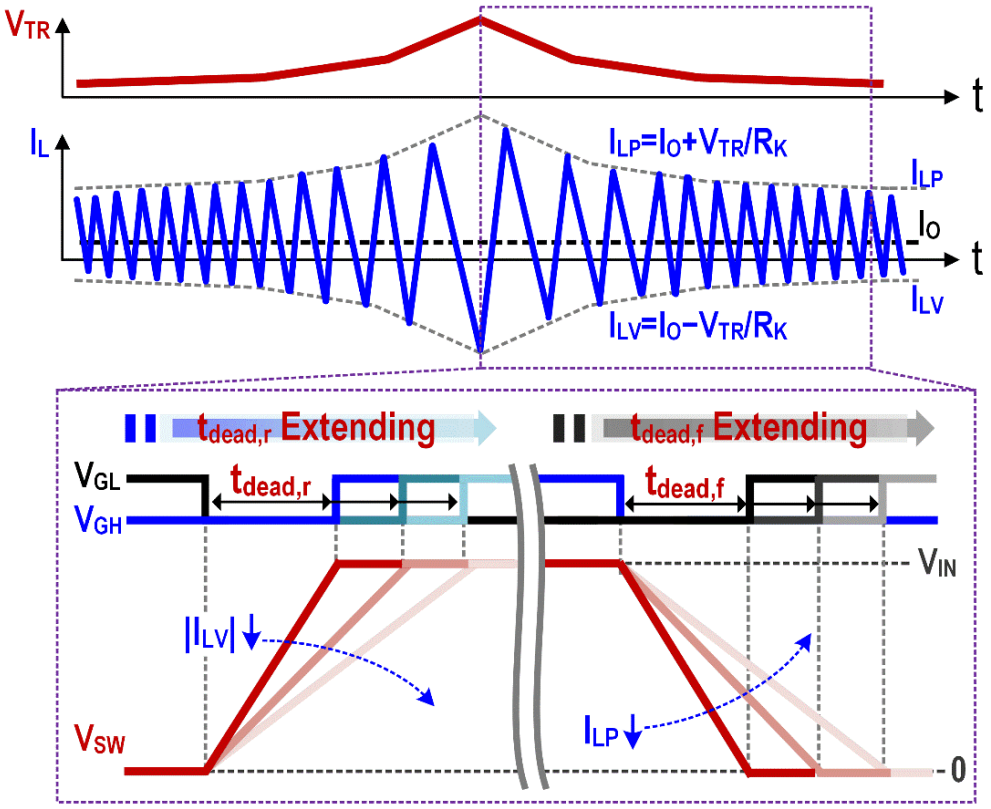


Figure 4.10. Illustration of the in-cycle adaptive ZVS operation scheme [Yan-21].

In order to realize in-cycle adaptive ZVS compatible with MR-SSM technique, the elastic t_{dead} controller optimizes t_{dead}s by predicting the upcoming I_L, and the operation scheme is illustrated

in Figure 4.10. The I_L prediction is realized according to the voltage signal V_{TR} in MRTG. V_{TR} is proportional to the coded T_{ON} and switching period T_{SW}. For example, if the periodic V_{TR} drops, the modulated T_{ON} and synchronized T_{OFF} both decrease accordingly. Because of the decreasing T_{SW}, the peak-to-peak I_L ripple drops. For a fixed I_O, the average value of I_L is maintained almost constant as I_O thanks to the active shaping control. Thus, I_{LP} and I_{LV} can be expressed as

$$I_{LP} = I_O + V_{TR}/R_K. \tag{4.6}$$

$$I_{LV} = I_O - V_{TR}/R_K. \tag{4.7}$$

Here, R_K is the equivalent modulation resistor, which is constant for fixed power conversion specifications. As a result, I_{LP} and $|I_{LV}|$ both drop proportionally due to the falling V_{TR}. For a specific half-bridge converter, the switching node parasitic capacitor C_{SW} is constant. During V_{SW} falling edge, C_{SW} is discharged by the positive I_{LP}. As I_{LP} decreases gradually, the falling edge dead-time $t_{dead,f}$ is extended by the elastic t_{dead} controller for optimal ZVS turn-on of M_L. Similarly, when C_{SW} is charged to V_{IN} by the negative I_{LV}, and the rising edge dead-time $t_{dead,r}$ extends correspondingly to compensate $|I_{LV}|$ variation. On the other hand, when V_{TR} rises, by the prediction of upcoming I_{LP} and I_{LV}, $t_{dead,f}$ and $t_{dead,r}$ are also narrowed continuously for optimized ZVS of power switches. In addition, V_{IN} and I_O are also sensed by the elastic t_{dead} controller to generate optimal constant delays, accommodating wide V_{IN} and I_O ranges.

4.3 Key Circuit Implementation

4.3.1 Multi-Rate T_{ON} Generator

As the core hardware of the anti-aliasing MR-SSM, the circuit schematic of the MRTG is illustrated in Figure 4.11. The MRTG periodically modulates T_{ON} with the coded rates and thus the

occurrences of f_{SW} during SSM operation are actively redistributed to compress EMI spikes. To accomplish such, the multi-rate I_{TR} generator regulates the voltage V_{TR} by the programmable control voltage $V_{CH1\sim3}$.

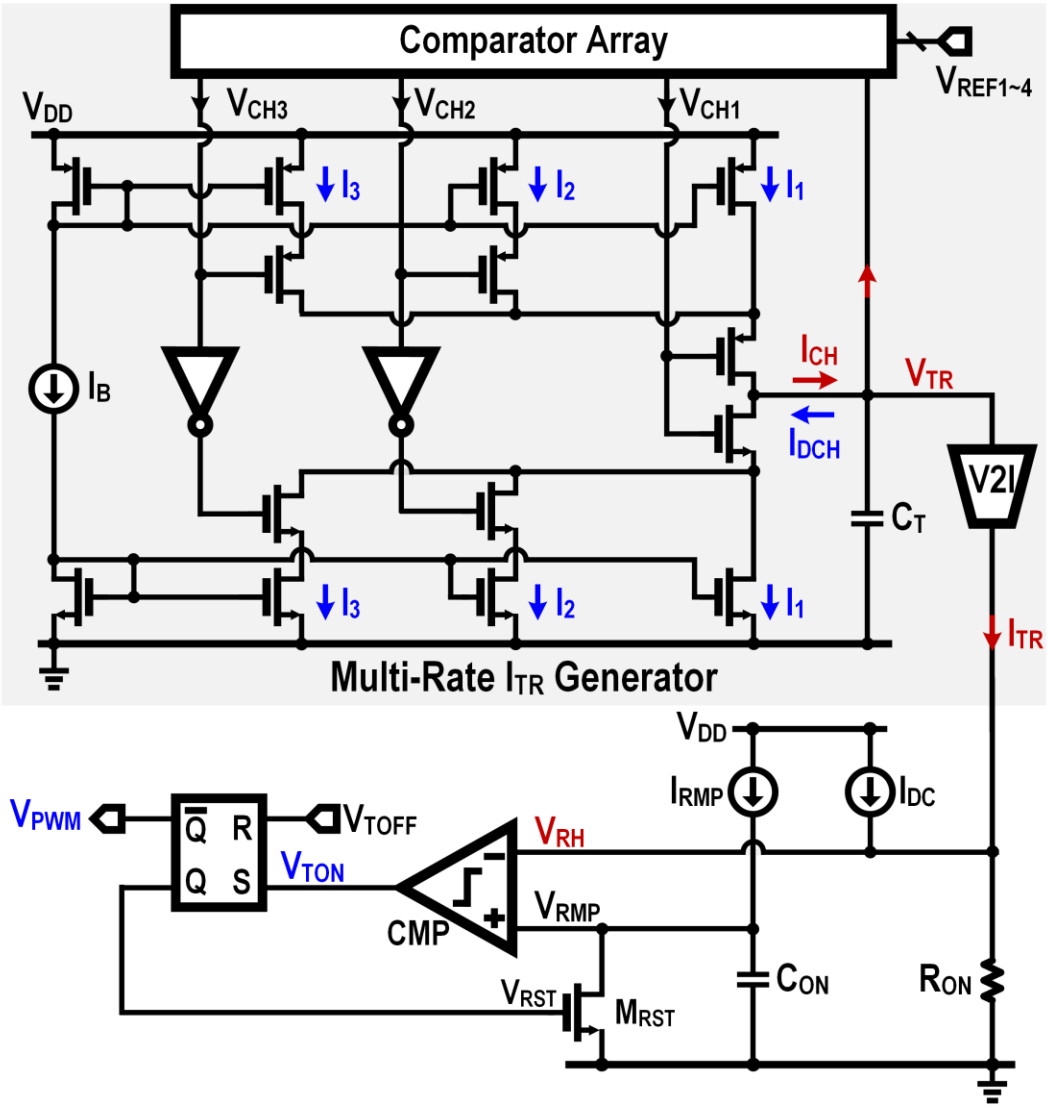


Figure 4.11. Circuit schematic of the MRTG [Yan-21].

The key operation waveforms are given in Figure 4.12. At the start of T_{ON} modulation cycle, a low V_{CH1} enables a coded charge current I_{CH} which equals I_1. Hence, the capacitor C_T is charged by I_{CH} and V_{TR} rises from V_{REF1}. Once V_{TR} hits V_{REF2}, V_{CH2} is triggered low and I_2 is added to I_{CH}.

Afterward, V_{CH3} turns low if V_{TR} crosses V_{REF3}, increasing I_{CH} by I_3. Accordingly, the rising rates of V_{TR} are adaptively adjusted by the coded I_{CH}.

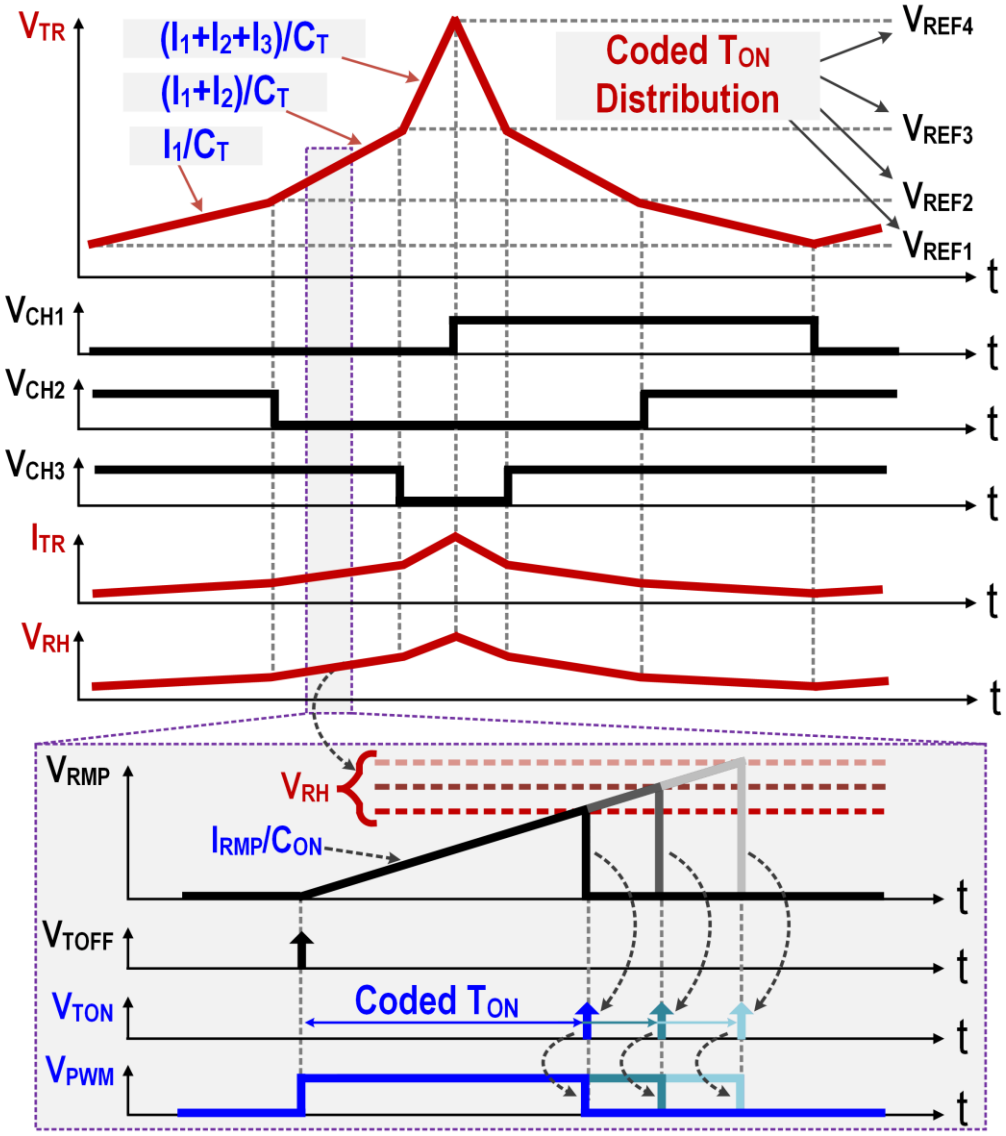


Figure 4.12. Operation waveforms of the MRTG [Yan-21].

When V_{TR} exceeds V_{REF4}, V_{CH1} turns high and C_T starts to be discharged by a complementary coded current I_{DCH}, achieving multiple falling rates of V_{TR}. V_{CH1} is triggered low until V_{TR} falls to V_{REF1}, initializing the next modulation cycle. Therefore, a periodic multi-rate V_{TR} is generated. With

a voltage to current conversion module (V2I), a multi-rate I_{TR} is provided on resistor R_{ON}, and the voltage V_{RH} equals

$$V_{RH} = R_{ON} \times (I_{DC} + I_{TR}). \tag{4.8}$$

Here, I_{DC} is the static biasing current to ensure V_{RH} constant positive for T_{ON} generation. Thanks to the multi-rate I_{TR}, V_{RH} is correspondingly modulated with the coded transient shape for multi-rate T_{ON} generation. At the beginning of T_{ON}, M_{RST} is turned off by V_{RST}, and the capacitor C_{ON} is charged up by a current I_{RMP}. Once the rising V_{RMP} crosses V_{RH}, a positive V_{TON} is triggered to terminate T_{ON}. Thus, T_{ON} equals

$$T_{ON} = V_{RH} \times C_{ON}/I_{RMP}. \tag{4.9}$$

As the trip point of V_{RMP} and V_{RH} determines T_{ON}, the constant I_{RMP} and modulated V_{RH} realizes the coded T_{ON}. With the adaptively synchronized T_{OFF}, the MR-SSM achieves targeted f_{SW} redistribution to avoid EMI power aliasing spikes.

4.3.2 Elastic t_{dead} Controller

To realize in-cycle adaptive ZVS, Figure 4.13 depicts the detailed circuit implementation of elastic t_{dead} controller. To avoid shot through current of high- and low-side power switches M_H and M_L, digital logic circuits are employed to generate nonoverlapping driving signals V_{GH} and V_{GL}. In the logic circuits, the static and elastic delay cells are used to optimize t_{dead}s for variable occasions. Despite that f_{SW}, I_{LP} and I_{LV} vary continuously, the elastic t_{dead} controller predicts and compensates V_{SW} slew rate deviations for optimal ZVS. To achieve such, the I_L prediction is achieved by the calculation of key parameters such as V_{IN}, I_O and V_{TR}. Therefore, the static delay t_{SD} and the elastic delay t_{ED} are then generated to optimize $t_{dead,f}$ and $t_{dead,r}$ instantly in each switching cycle.

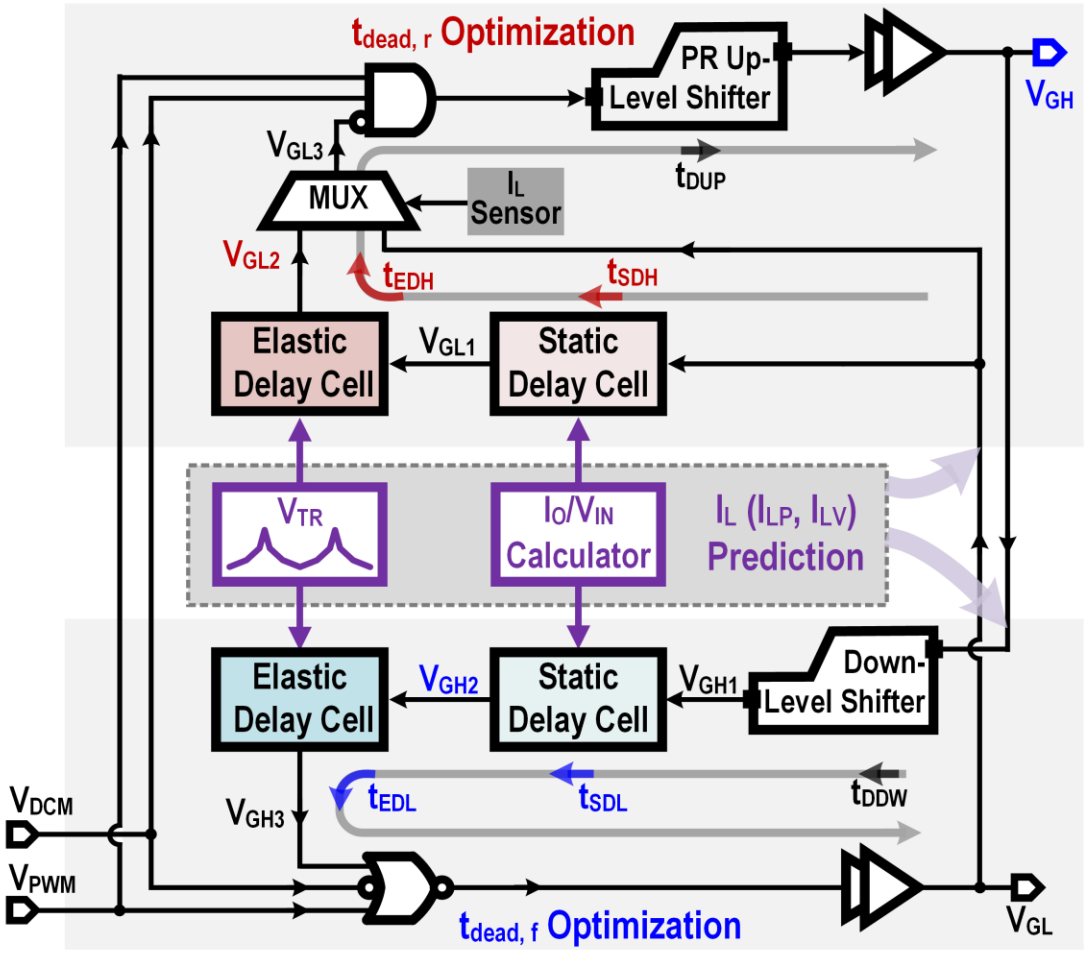
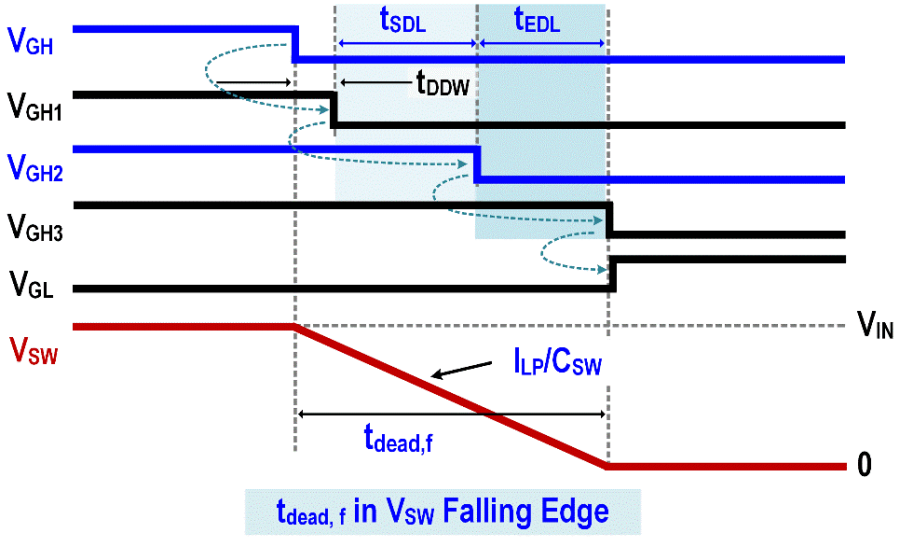
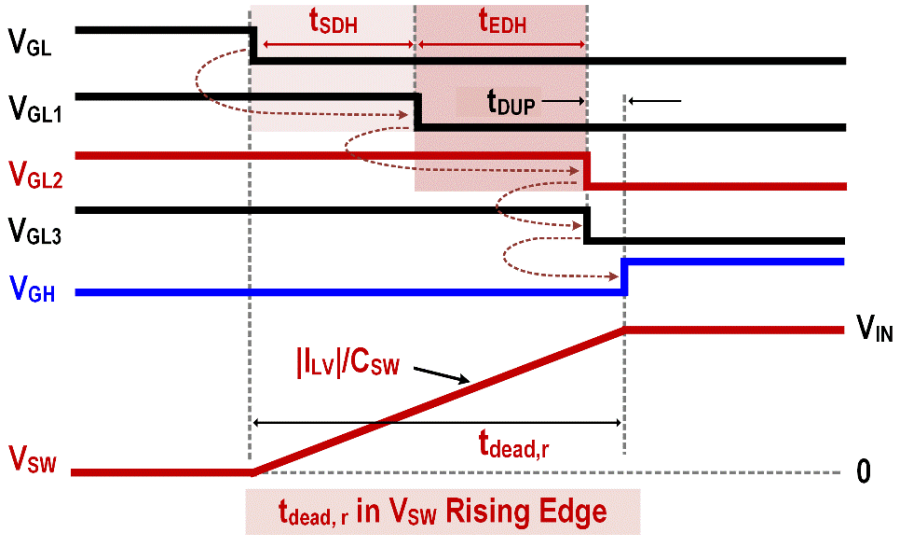


Figure 4.13. Circuit schematic of the elastic t_{dead} controller [Yan-21].

Figure 4.14 illustrate the key operation waveforms. As shown in Figure 4.14(a), during $t_{dead,f}$, the static delay t_{SDL} is modulated based on stable V_{IN} and I_O values, whereas the elastic delay t_{EDL} is optimized by the transient V_{TR} cycle by cycle. If V_{TR} decreases for the MR-SSM, the instant f_{SW} decreases and I_{LP} falls. t_{EDL} extends accordingly to achieve ZVS turn-on of M_L. Similarly, in Figure 4.14(b), a complementary operation takes place in V_{SW} rising interval to adjust t_{SDH} and t_{EDH} for ZVS of M_H if I_{LV} is negative. When I_{LV} is above zero, t_{SDH} and t_{EDH} are eliminated to minimize $t_{dead,r}$ and reduce reverse conduction loss. Hence, in-cycle adaptive ZVS is accomplished to minimize potential power losses associated with the MR-SSM technique.



(a)

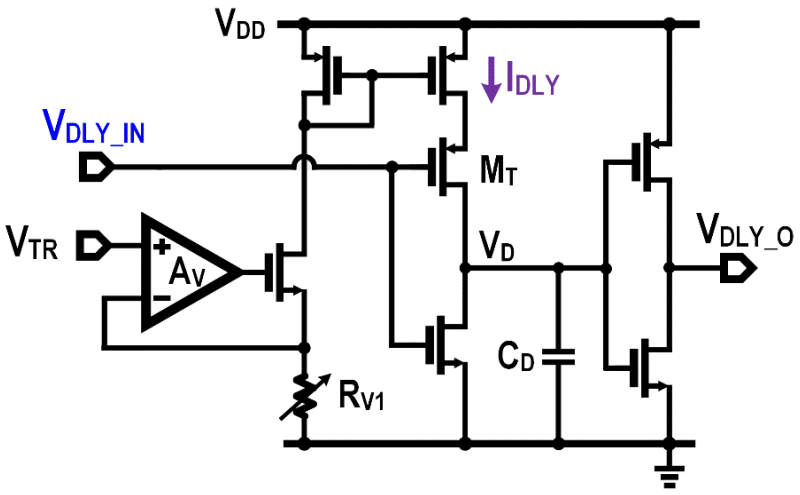


(b)

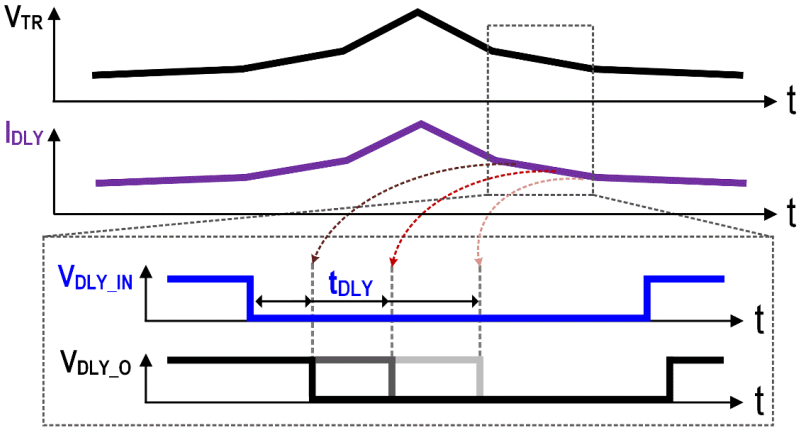
Figure 4.14. Operation waveforms of the elastic t_{dead} controller: (a) $t_{dead,f}$ in V_{SW} falling interval, and (b) $t_{dead,r}$ in V_{SW} rising interval [Yan-21].

Figure 4.15(a) shows the circuit schematic of elastic delay cell used in elastic t_{dead} controller. When the digital input V_{DLY_IN} falls to zero, M_T is turned on and the current I_{DLY} starts to charge the capacitor C_D. Once the voltage on C_D, V_D, rises higher than the threshold voltage of the following inverter, V_{DLY_O} falls zero. Thus, the falling edge between V_{DLY_IN} and V_{DLY_O}, t_{DLY}, is

determined by I_{DLY}, which is generated by V_{TR}. As shown in Fig. 4.15(b), a decreasing V_{TR} induces a lower I_{DLY}. The falling edge delay between V_{DLY_IN} and V_{DLY_O} is thus extended, facilitating elastic t_{dead} control.



(a)



(b)

Figure 4.15. (a) Circuit schematic, and (b) operation waveforms of the elastic delay cell [Yan-21].

4.3.3 Pulse-Reinforced Up-Level Shifter

To improve the driving reliability of power stage, the circuit schematic of the proposed PR up-level shifter is shown in Figure 4.16. The high voltage devices M_{d1} and M_{d2} are employed to

isolate the high and low voltage domains. In the low voltage domain, the digital input signal V_{LHI} controls the low voltage devices M_1 and M_2. The currents through M_3 and M_4 are determined indirectly, and the voltage difference between V_{SG3} and V_{SG4} change accordingly during the signal transmission period. The following circuits compare the voltage difference and generate a digital output V_{LHO} instantly. However, there are parasitic capacitors at the drains of M_3 and M_4 (C_{P1} and C_{P2}), which are mainly induced by M_{d1} and M_{d2}. During V_{SW} dv/dt transition, high non-ideal coupled currents I_{CP1} and I_{CP2} are generated through M_3 and M_4, respectively. V_{SG3} and V_{SG4} both increase, and the voltage difference becomes very small. It would flip the output of level shifter V_{LHO} falsely and generate disastrous false turn-on of power switches, deteriorating the driving reliability. To immune the negative effects and maintain constant V_{LHO} during V_{SW} transition, one active I_{CP} current generator and two pulse generators are adopted.

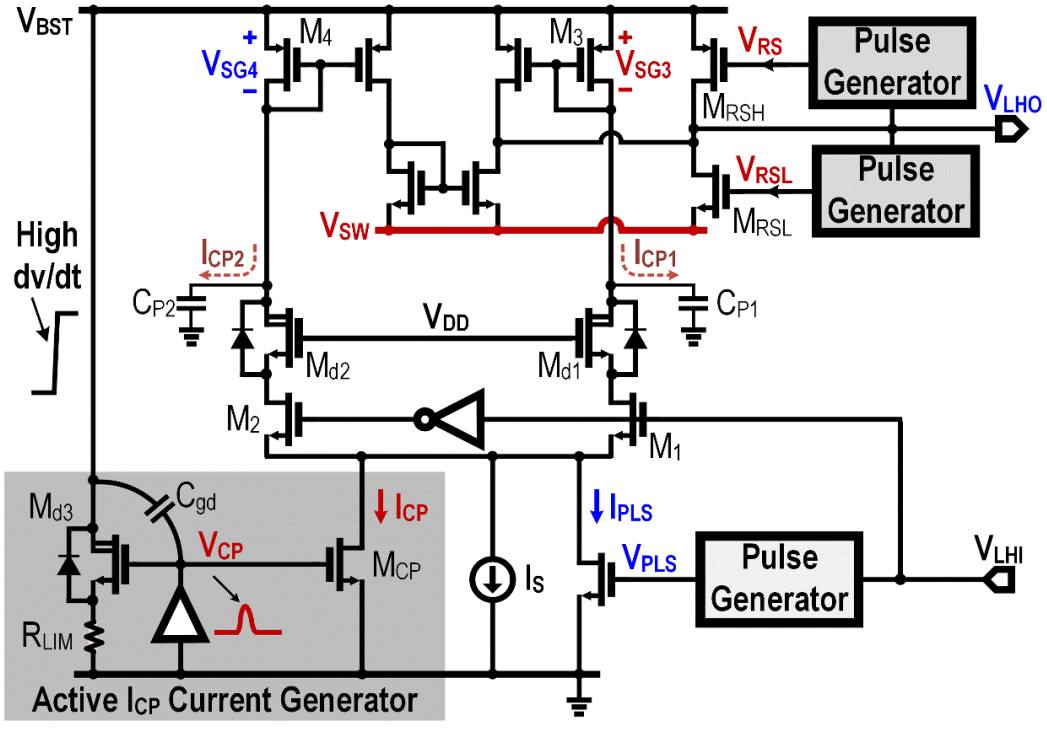
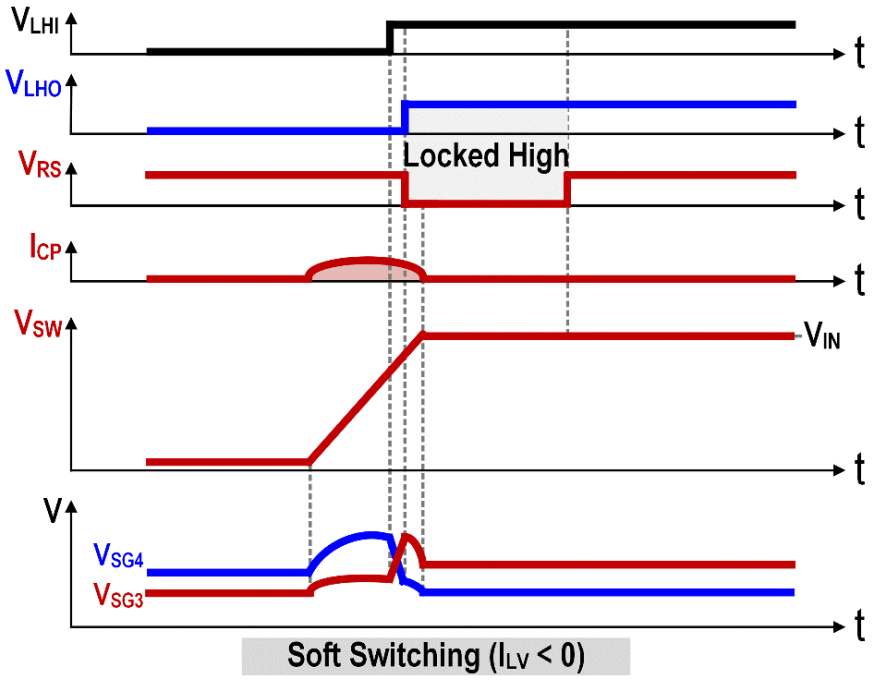
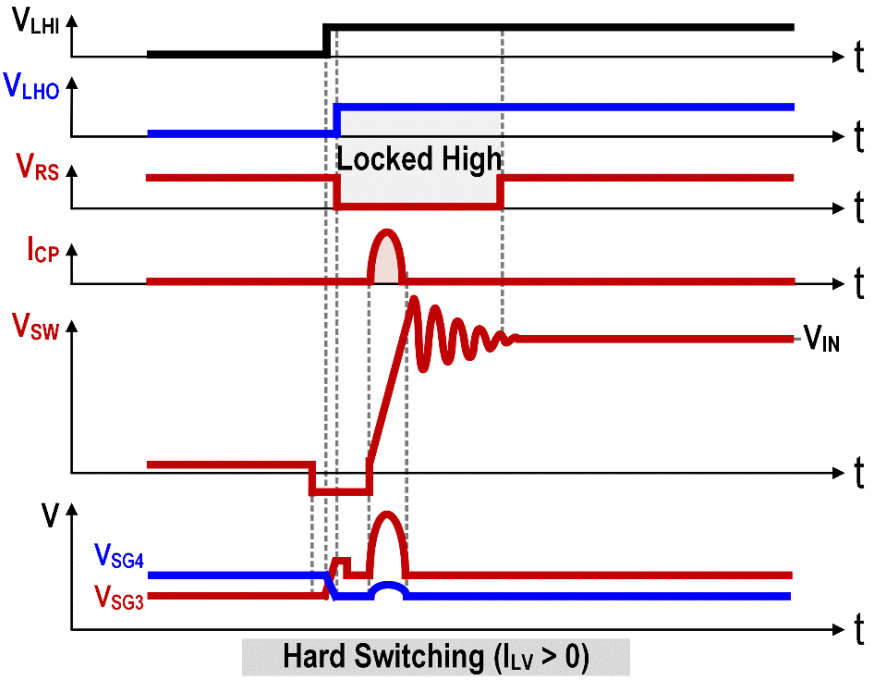


Figure 4.16. Circuit schematic of the pulse-reinforced up-level shifter [Yan-21].



(a)



(b)

Figure 4.17. Operation waveforms of the pulse-reinforced up-level shifter with (a) negative I_{LV} and (b) positive I_{LV} [Yan-21].

The reliability is improved for both soft and hard switching operations, which are illustrated in Figure 4.17. If I_{LV} can go slightly negative in Figure 4.17(a), C_{SW} can be charged up by I_{LV} and V_{SW} rises to V_{IN} before the high-side GaN switch M_H is turned on, achieving a soft switching of half-bridge converter. Therefore, V_{SW} starts to rise before the input of level shifter V_{LHI} turns high. At the beginning of V_{SW} rising period, the low static current I_S flows through M_4, keeping V_{SG4} higher than $V_{SG3,}$ and V_{LHO} is low. During V_{SW} rising period, the active I_{CP} current generator senses the corresponding V_{BST} dv/dt transition and generates a positive voltage pulse of V_{CP}. M_{CP} generates a coupled I_{CP}, which is much higher than the non-ideal I_{CP1} and I_{CP2}. Since I_{CP} passes through M_4, V_{SG4} becomes far higher than V_{SG3} to keep V_{LHO} low, avoiding potential false triggers. On the other hand, for a hard switching operation with a positive I_{LV} in Figure 4.17(b), V_{SW} rises to V_{IN} after M_H is turned on. Thus, V_{LHI} and V_{LHO} are high when V_{SW} rises to V_{IN}. Because of the I_S through M_3, V_{SG3} is higher than V_{SG4}. During V_{SW} transition, the actively generated high I_{CP} increases V_{SG3} further above V_{SG4} to ensure V_{LHO} high reliably. Besides, at the output of level shifter, one negative pulse of V_{RS} is generated by the pulse generator during V_{SW} ringing period. The turned-on M_{RSH} locks V_{LHO} high. Thus, the false trigger possibility induced by V_{SW} ringing is also eliminated for high reliability. Similarly, a positive pulse V_{RSL} is generated by sensing the falling edge of V_{LHO}. During the V_{SW} falling edge, M_{RSL} is turned on to lock V_{LHO} to zero and avoid potential false triggering.

4.4 Experimental Verification

The proposed design is implemented using a 180-nm HV BCD process. Figure 4.18 shows the chip micrograph of this design with MRTG, elastic t_{dead} controller, buffer driver and level shifters. The active die area is 0.87mm^2. The photograph of PCB test board is presented in Figure

4.19. Two e-mode GaN HEMTs are used as the power switches in the power converter with one 1-µH inductor and one 22-µF output capacitor. With an input power supply ranging from 5V to 24V, the converter delivers a maximum output current I_O of 1.2A at 1-V V_O.

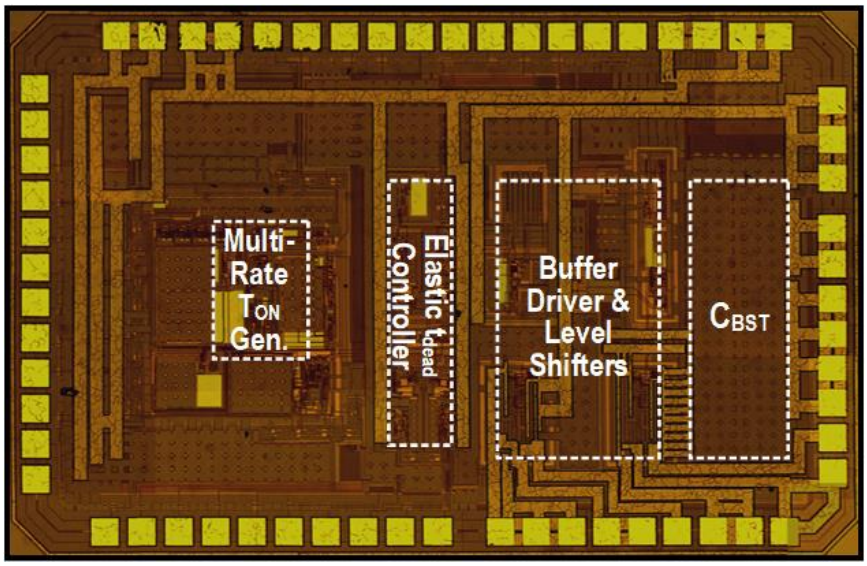


Figure 4.18. Chip micrograph [Yan-21].

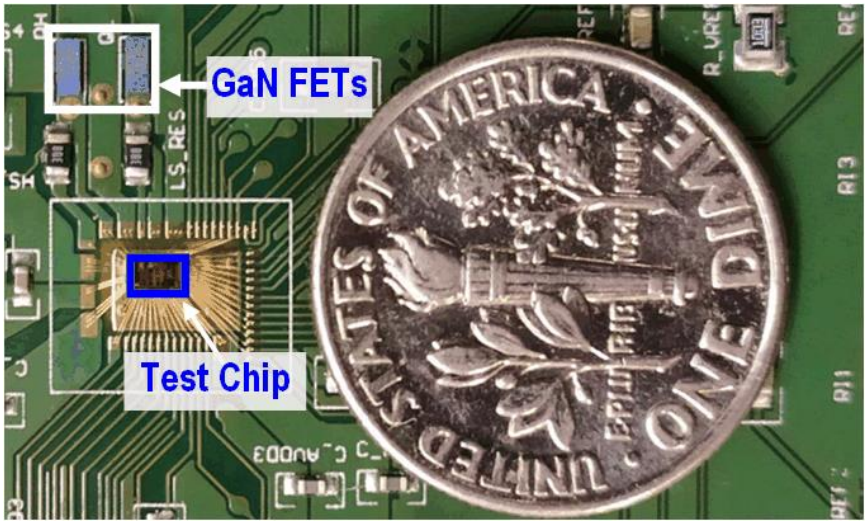
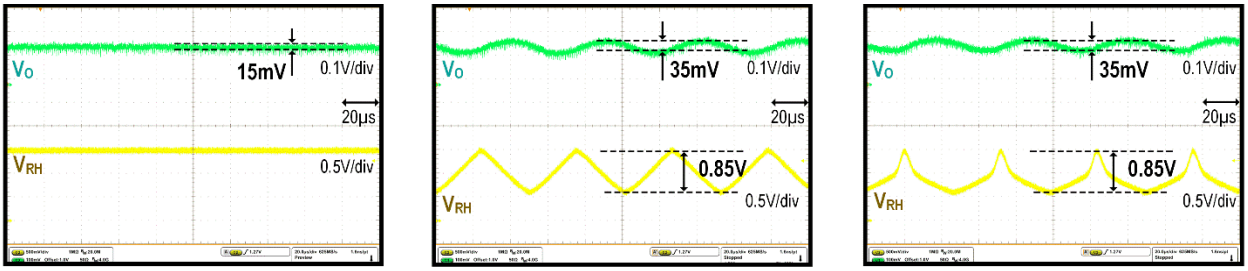


Figure 4.19. Photograph of PCB test board [Yan-21].

To validate the anti-aliasing MR-SSM technique, Figure 4.20(a)-(c) show the measured V_O and V_{RH} under a conventional current mode COT control, the FR-SSM and the anti-aliasing MR-

SSM, respectively. While T_{ON} is equally modulated in every cycle under the FR-SSM, it is done unequally for better f_{SW} redistribution in the MR-SSM. As a compromise to the EMI suppression, compared to the fixed f_{SW} operation under the COT control, the FR-SSM and the anti-aliasing MR-SSM operations both increase V_O ripples by about 20mV, which is still much smaller than those in RSSM operation [Ho-10].



(a) (b) (c)

Figure 4.20. Measured V_O and V_{RH} under (a) the COT control, (b) the FR-SSM control, and (c) the anti-aliasing MR-SSM control [Yan-21].

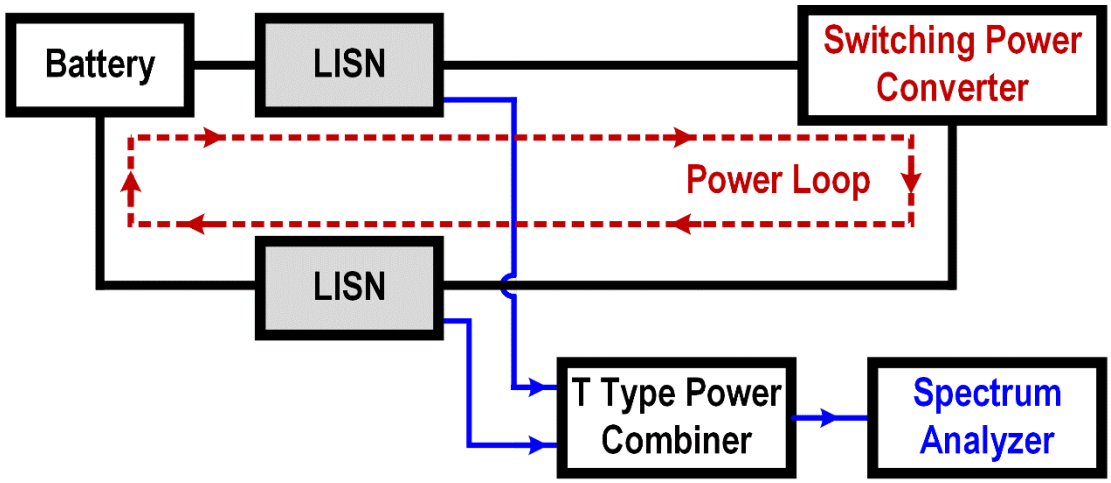
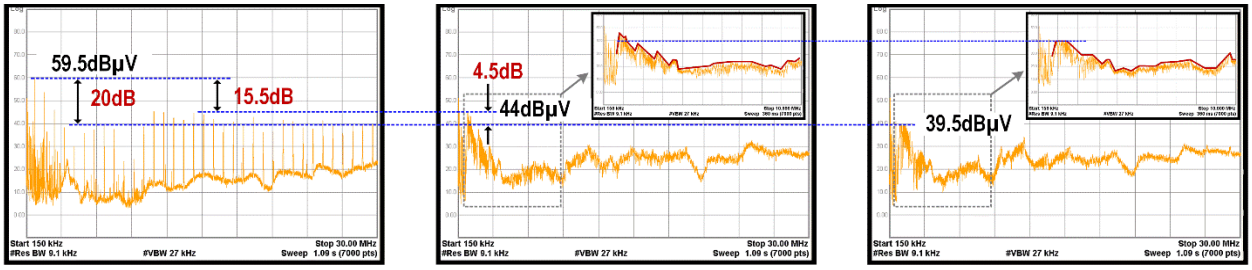


Figure 4.21. Conducted EMI measurement setup.

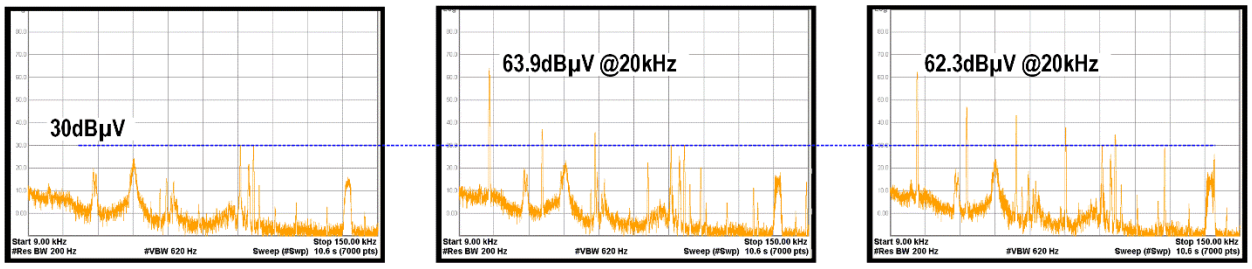
To achieve pre-compliance EMI noise measurement, the EMI noise measurement setup is shown in Figure 4.21. The line impedance stabilization network (LISN) is employed between the input source and power converter for the conducted EMI noise measurement. With one T type power combiner, the two output signals of LISNs are combined as a single port output signal. It is

captured by the spectrum analyzer for EMI noise spectrum analysis. The measured conducted EMI emission noise spectra from 150kHz to 30MHz in the three controls are shown in Figure 4.22. Benefiting from the targeted f_{SW} redistribution, the anti-aliasing MR-SSM reduces the peak EMI emission noise by 20dB, accomplishing 29% improvement with 4.5dB further peak EMI reduction over the FR-SSM, which is modulated with the same frequency range from 0.9MHz to 2.1MHz.



(a) (b) (c)

Figure 4.22. Measured conducted EMI from 150kHz to 30MHz under (a) the COT control, (b) the FR-SSM control, and (c) the anti-aliasing MR-SSM control [Yan-21].



(a) (b) (c)

Figure 4.23. Measured conducted EMI from 9kHz to 150kHz under (a) the COT control, (b) the FR-SSM control, and (c) the anti-aliasing MR-SSM control.

Figure 4.23 illustrates the measured conducted EMI spectra from 9kHz to 150kHz with COT, FR-SSM and anti-aliasing MR-SSM controls. It shows that the EMI spike at 20kHz in COT control is relatively low. And it rises to 63.9dBµV in FR-SSM control and 62.3dBµV in MR-SSM control. This is consistent with the SSM modulation frequency. Although the EMI spikes between 9kHz and 150kHz become higher than fixed f_{SW} control due to SSM techniques, they can satisfy the EMI/EMC standards, in which the specified EMI noise levels of such range are also high.

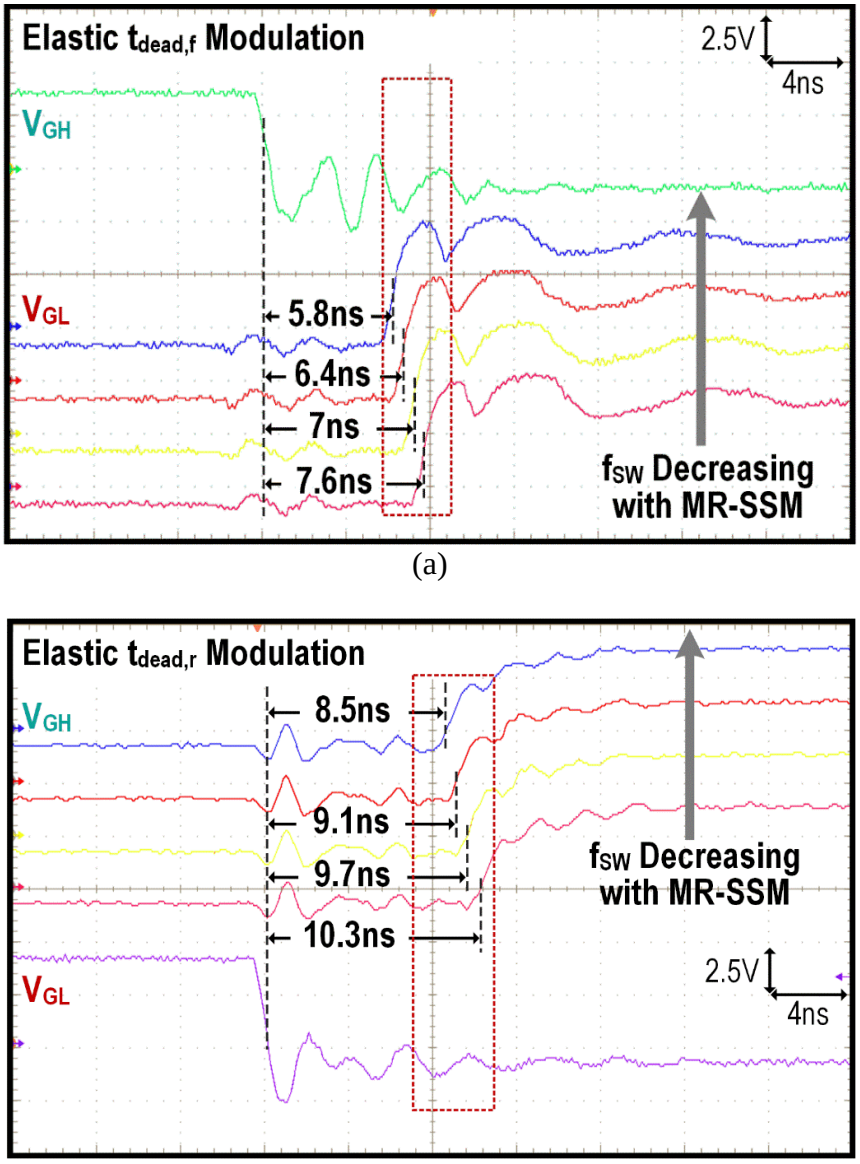
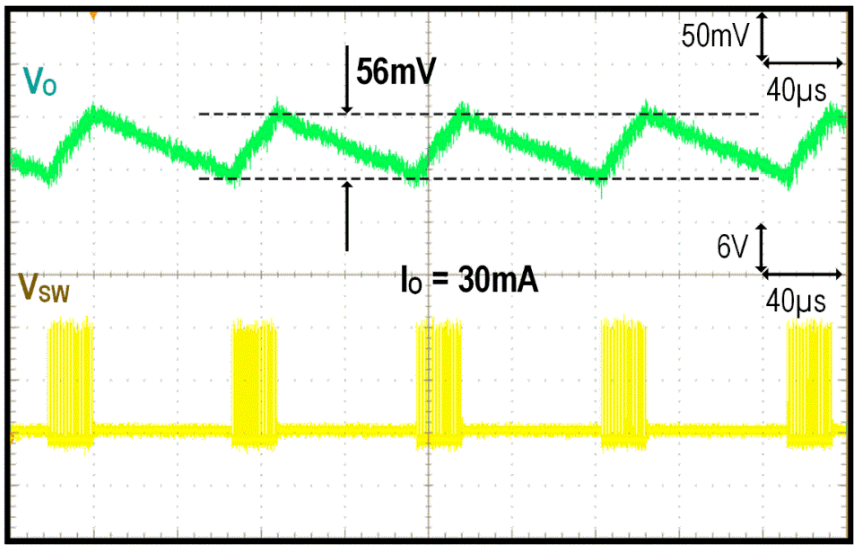


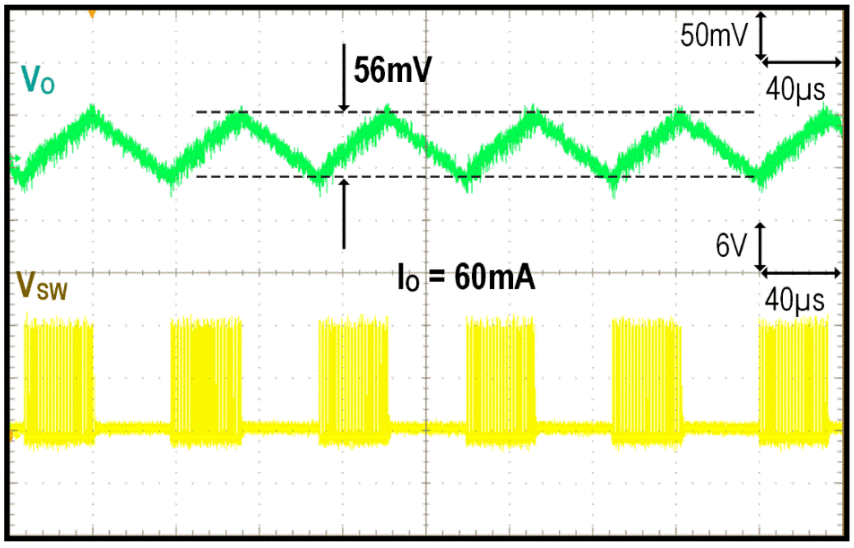
Figure 4.24. Measured gate driving signals V_{GH} and V_{GL}, with (a) elastic $t_{dead,f}$ modulation, and (b) elastic $t_{dead,r}$ modulation [Yan-21].

To evaluate the effectiveness of in-cycle adaptive ZVS technique under the proposed MR-SSM operation, Figure 4.24(a) illustrates measured elastic $t_{dead,f}$ behavior under different f_{SW}. According to the gate driving signals V_{GH} and V_{GL}, $t_{dead,f}$ is elastically modulated between 5.8ns and 7.6ns to compensate continuous I_{LP} variation during MR-SSM. Similarly, $t_{dead,r}$ in Figure

4.24(b) is optimized between 8.5ns and 10.3ns. The elastic t_{deads} ensure optimal ZVS turn-on of power switches regardless of continuous f_{SW} variation during MR-SSM operation.



(a)

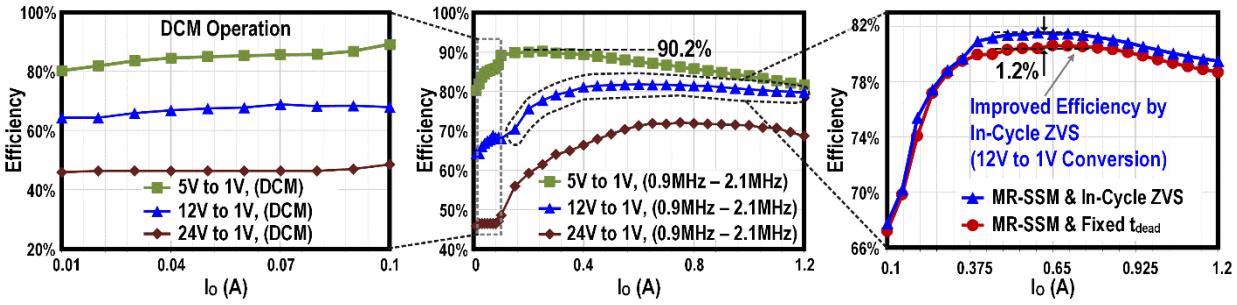


(b)

Figure 4.25. Measured V_O and V_{SW} with reference to various light load conditions: (a) I_O=30mA, and (b) I_O=60mA [Yan-21].

Figure 4.25(a)-(b) show the measured V_O and V_{SW} with reference to variable light load current in DCM operation. When I_O is 30mA and 60mA, the V_O ripple is measured as 56mV.

Compared to conventional SSM techniques, which modulate f_{SW} directly without the consideration of light load efficiency, the converter not only modulates f_{SW} indirectly for EMI reduction, but also activates the DCM operation to improve light load efficiency.



(a) (b) (c)

Figure 4.26. (a) Efficiency in DCM operation for light load, (b) efficiency at the full load range, and (c) efficiency improvement by in-cycle adaptive ZVS technique [Yan-21].

Table 4.1. Performance comparison of proposed buck converter to prior arts [Yan-21].

Design	[Ke-18] JSSC 2018	[Ho-10] CICC 2010	[TI-17] TI LM25141	This Work
Process	350nm BCD	180nm CMOS	N/A	180nm BCD
Input Voltage	3V – 40V	2V – 3.3V	8V – 18V	5V – 24V
Nominal Output Voltage	5V	1.5V	3.3V	1V
Minimum Duty Ratio	21%	45.5%	18.3%	4.2%
Minimum T_{ON}	40ns	N/A	70ns	20ns
SSM Method	FR-SSM	RSSM	FR-SSM	MR-SSM
SSM Range	9.1MHz – 10.9MHz	0.8MHz – 1.2MHz	2.09MHz – 2.31MHz	0.9MHz – 2.1MHz
Peak EMI Reduction	33dB	16dB	8dB	20dB
DCM Operation	No	No	Yes	Yes
In-Cycle ZVS	No	No	No	Yes
Load Current Range	0.05A – 1.5A	0.1A – 0.5A	0.1A – 5A	0.01A – 1.2A
Peak Efficiency	85.5%	N/A	90%	90.2%

Figure 4.26 shows the measured efficiency of the converter with a peak value of 90.2% for 5V/1V conversion, 81.8% for 12V/1V conversion, and 72.1% for 24V/1V conversion. Thanks to

the DCM operation, the efficiency retains high at light load between 0.01A and 0.1A. Furthermore, the in-cycle adaptive ZVS technique improves efficiency by 1.2%. Finally, Table 4.1 compares this work with the prior arts [Ke-18, Ho-10, TI-17]. It achieves over 4 times lower minimum duty-ratio for high step-down ratio power conversion. Thanks to the anti-aliasing MR-SSM technique, effective peak EMI reduction is accomplished in the high V_{IN}/V_O power conversion. Meanwhile, the in-cycle adaptive ZVS technique further improves the efficiency over a wider I_O range.

4.5 Summary

In this chapter, a GaN-based switching power converter with anti-aliasing MR-SSM and in-cycle adaptive ZVS techniques is presented. The anti-aliasing MR-SSM spreads EMI spectra in a wide frequency range without aliasing spikes, attenuating the peak EMI effectively in high step-down ratio power converters. An elastic t_{dead} controller optimizes t_{dead} within each cycle, accomplishing in-cycle adaptive ZVS during the MR-SSM operation and, thus, maintaining high efficiency. In addition, a PR up-level shifter enhances the driving reliability for high V_{SW} dv/dt transition. The experimental results successfully validate the proposed techniques and circuits in this design.

CHAPTER 5

CONDITION MONITORED GAN-BASED DC-DC CONVERSION FOR RELIABILITY

As discussed in Section 1.2.3, the reliability challenges of GaN power devices constrain the widespread adoption of GaN-based power conversions. In this chapter, an on-chip self-calibrated full-profile dynamic r_{on} monitoring strategy is proposed to enhance its reliability. Firstly, prior dynamic r_{on} sensing circuits are reviewed and design considerations of full-profile dynamic r_{on} sensing in GaN-based power converters are analyzed in Section 5.1. Then Section 5.2 elaborates the on-chip self-calibrated full-profile dynamic r_{on} sensing scheme for a GaN-based half-bridge power converter. In Section 5.3, the detailed circuit implementations of integrated tri-state dynamic r_{on} sensors, including M_L forward r_{on} sensor, M_H forward r_{on} sensor, and ET M_L reverse r_{on} sensor, are presented. Meanwhile, dynamic BST generator and dual-rail up-level shifter are also illustrated. After that, the measurement results as shown in Section 5.4 successfully validate the functionality and performance of the design. Finally, this chapter is summarized.

5.1 Design Considerations

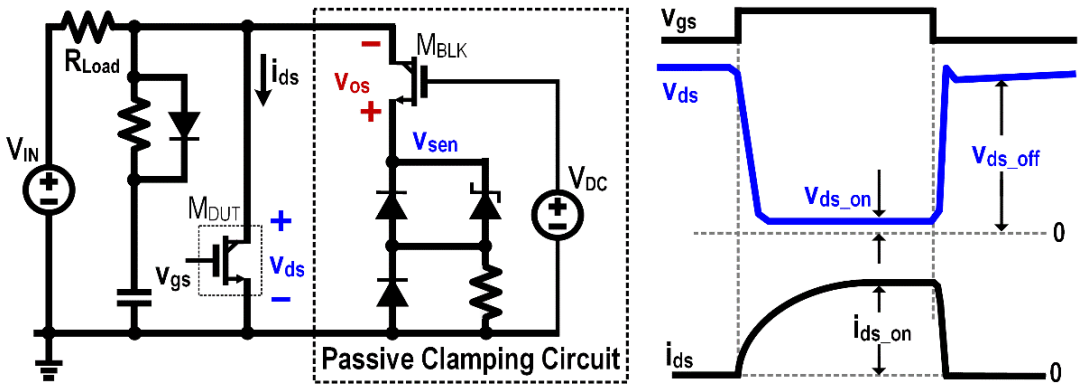
5.1.1 Dynamic r_{on} Sensing

Conventionally, condition monitoring, which assesses the health status of a system component and takes corrective actions before failure occurs, has been proven to be a cost-effective means of enhancing reliability. The condition precursors can be used to represent the healthy state of power components [Witczak-21]. In a normal state, its value is below the fault threshold, and it starts a faulty mode when the precursor crosses the fault threshold. This may be caused by the natural aging process or external destructive influences, and the performance of

power system decreases. If the precursor further increases higher than the failure threshold, the system cannot work, and it is usually named as the end of life. In power converters, on-resistance of the power device is a critical variable and widely used as a precursor signature identification of condition monitoring [Bahl-16, Xu-18, Haque-17, Biglarbegian-18, Chen-21, Huang-20]. [Xu-18] uses the Keysight B1506A curve tracer to capture the static on-resistance of GaN HEMT and adopts it as an offline aging precursor. It is observed that the static on-resistance gradually increases over the aging process. But the operation of switching power circuits has to be stopped occasionally, interrupting its normal operation and affecting the power electronic system. Besides, due to the unique GaN HEMT structure, the value of instant dynamic on-resistance increases much higher than the static one when switched at high voltage and high f_{SW}. It is highly affected by multiple switching parameters, such as off-state blocking voltage, f_{SW}, conduction period and so on [Li-18a, Zulauf-20a]. Thus, the static on-resistance can hardly represent the real-time states of GaN HEMTs. To ensure the normal operation of converters, online state-of-health monitoring through dynamic r_{on} can be very useful [Haque-17, Biglarbegian-18, Chen-21, Huang-20]. Hence, comprehensive, accurate and efficient dynamic r_{on} sensing techniques are indispensable for in-situ monitoring without compromising the performance of power converters.

Previously, various studies have implemented different switching circuits for dynamic on-resistance analysis. Theoretically, both on-state drain-source current (i_{ds_on}) and voltage (v_{ds_on}) should be sensed for dynamic r_{on} calculation. But classic current sensing techniques suffer from either high cost or low accuracy [Zhang-17]. Moreover, since v_{ds_on} is significantly lower than the off-state voltage (v_{ds_off}) of the GaN HEMT in switching action, building sense circuitry to accommodate such a large dynamic voltage range with high resolution and high speed becomes

far more challenging. Commercial voltage clipping probes can avoid saturation induced by the high v_{ds_off} and maintain high resolution of the low v_{ds_on} [Cai-17, Martínez-19]. However, these probes are bulky and expensive for implementation. To overcome these challenges, specialized clamping circuits are designed for dynamic on-resistance measurement [Lu-11, Pozo-20, Gelagaev-15, Foulkes-18, Jones-19, JEDEC-19].

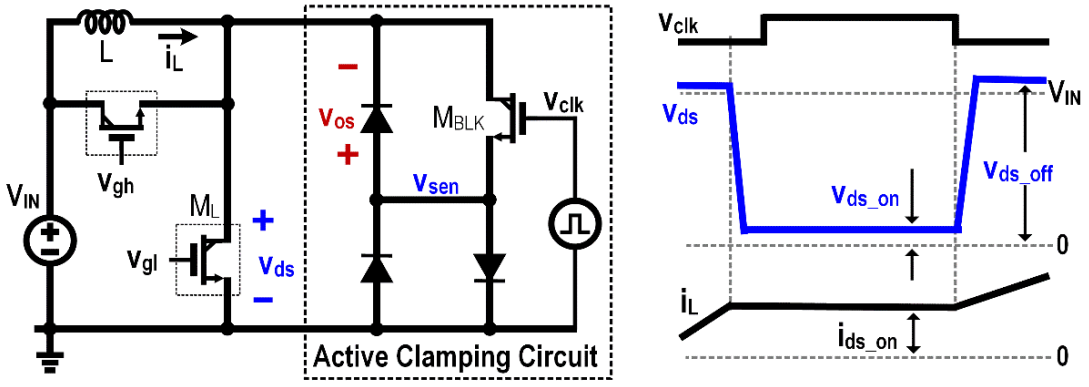


(a) (b)

Figure 5.1. Hard switching circuit with a passive clamping circuit: (a) circuit structure, and (b) key operation waveforms [Lu-11, Pozo-20].

Figure 5.1 shows a passive clamping circuit in a hard switching GaN circuit, which predefines i_{ds_on} of the GaN HEMT M_{DUT} by adjusting the load resistor R_{Load} [Lu-11, Pozo-20]. In the clamping circuit, a blocking switch M_{BLK} is controlled by a DC voltage. When M_{DUT} is off, the high v_{ds_off} is blocked, and the sensed voltage v_{sen} is clamped to a low voltage. Conversely, if M_{DUT} is turned on, v_{sen} tracks the low positive v_{ds_on}. But v_{sen} is affected by the offset voltage across M_{BLK}, v_{os}, which deteriorates dynamic on-resistance sensing accuracy and condition monitoring fidelity. Besides, the low sensing speed of the clamping circuit constrains the maximum f_{SW} of GaN circuits. This predefined resistive load switching circuit is not typically used in the power electronic applications. To improve the clamping circuit sensing speed, current mirror and ultra-fast diodes are employed to replace HV blocking MOSFET [Gelagaev-15]. However, the required differential

voltage probes cannot fully attenuate the common mode signal portion of the measurement. Low sensing accuracy is still induced by the existing measured offsets. To remove the non-ideal offset voltages in the clamping circuit, [Foulkes-18] measures multiple voltage signals simultaneously and calculates v_{ds_on} manually. But the needed multiple single-ended voltage probes must be aligned well, increasing implementation complexity. To switch the GaN HEMT at a high f_{SW} with an inductive load, which is more similar to switching power converters, a double pulse test (DPT) setup is depicted in Figure 5.2 [Jones-19, JEDEC-19]. It demonstrates the measurement of dynamic on-resistance of low-side GaN HEMT, M_L. A bulky current probe is used to measure i_{ds_on} of M_L, and an active clamping circuit is designed to sense its v_{ds_on}. The blocking switch M_{BLK} is controlled by a clock signal v_{clk} to transmit low v_{ds_on} and block high v_{ds_off}. However, the precision is compromised by the offset voltage v_{os} of M_{BLK}, too. In addition, the constantly positive v_{ds_on} cannot fully represent the operation states in power converters.

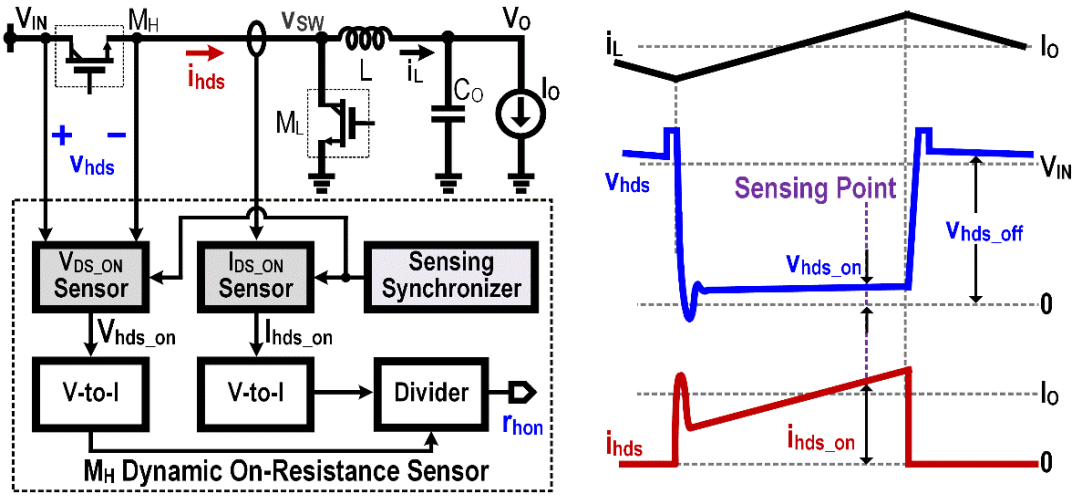


(a) (b)

Figure 5.2. Double pulse test setup circuit with an active clamping circuit: (a) circuit structure, and (b) key operation waveforms [Jones-19, JEDEC-19].

In the above dedicated dynamic on-resistance analysis circuits, i_{ds_on} is either indirectly predefined by actively controlling load current (I_O) or measured by a split-core current probe. But they are not applicable for the integrated i_{ds_on} sensing in power converters with the variable I_O. In

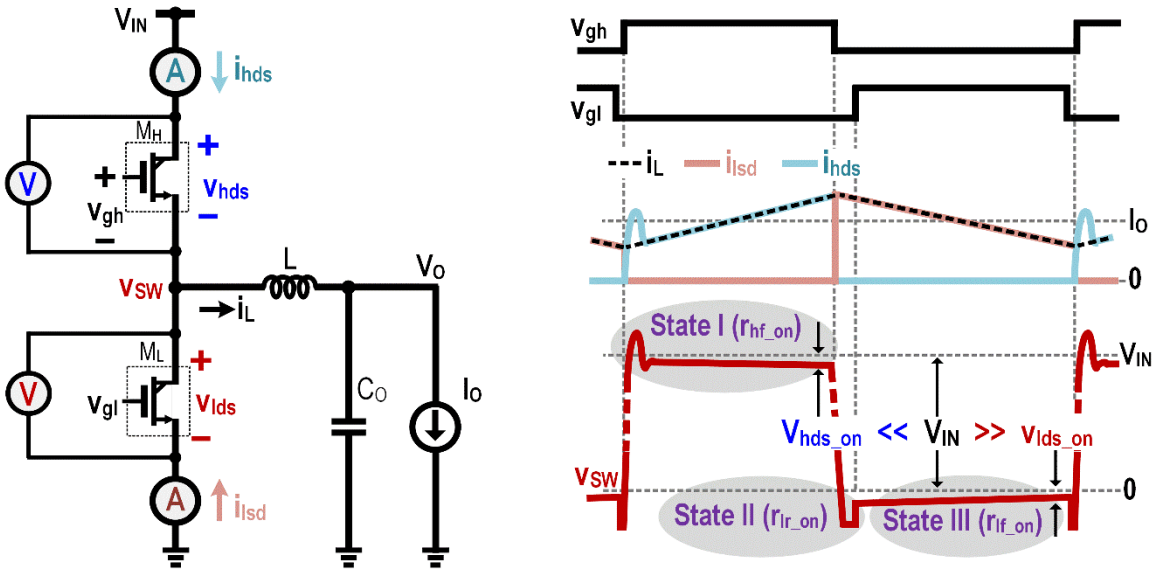
addition, the sensed v_{ds_on} is constantly positive and ground-referenced, and it cannot thoroughly represent operation states in power converters, which would include a negative or floating v_{ds_on}. Overall, the integrated dynamic on-resistance sensing techniques in GaN-based power converters have not been sufficiently developed yet. [Chen-21, Huang-20] present integrated dynamic on-resistance sensing circuits of the high-side GaN HEMT M_H in a buck converter. In Figure 5.3(a), the transient v_{hds} and i_{hds} of M_H are sensed separately, converted by two voltage-to-current (V-to-I) conversion modules, and calculated by one divider circuit. Figure 5.3(b) presents the operation waveforms. When M_H is on, v_{SW} rises close to V_{IN} and the positive v_{hds} falls close to zero, which increases along with the rising inductor current i_L. With a synchronizer, the transient v_{hds_on} and i_{hds_on} of M_H are sensed simultaneously for dynamic on-resistance calculation. However, these extra voltage and current sensing and calculation circuits induce more area and power overheads. Besides, the random errors in v_{hds_on} and i_{hds_on} sensing circuits would deteriorate dynamic on-resistance accuracy. Since there are multiple operation states with several dynamic on-resistances, only M_H dynamic on-resistance cannot fully represent the healthy states of buck converters.



(a) (b)

Figure 5.3. Dynamic r_{on} sensing of GaN HEMT M_H in a buck converter: (a) circuit structure, and (b) key operation waveforms [Chen-21, Huang-20].

5.1.2 Tri-State Operation



(a) (b)

Figure 5.4. (a) Circuit structure of half-bridge buck converter, and (b) key operation waveforms illustrating three operation states.

Since the synchronous half-bridge buck converter is widely adopted in power electronics, high reliability should be ensured with state-of-health monitoring through full-profile dynamic r_{on}s sensing of GaN HEMTs. In the buck converter of Figure 5.4(a), two GaN HEMTs M_H and M_L are switched periodically by the driving signals v_{gh} and v_{gl}. Based on inductor current i_L flowing paths, there are mainly three dynamic r_{on} conduction states: M_H forward conduction state (I), M_L reverse conduction state (II) and M_L forward conduction state (III) [JEDEC-21]. Figure 5.4(b) shows that in state I, M_H is on, and i_L flows from input voltage source (V_{IN}) through M_H forward on-resistance (r_{hf_on}). As the shoot-through current is detrimental to the power switches, v_{gh} and v_{gl} are designed as non-overlapping signals to avoid turning on M_H and M_L simultaneously. Thus, state II represents t_{dead} that M_H and M_L are kept off by zero v_{gh} and v_{gl}. In such a state, the continuously positive i_L discharges switching node capacitor and then flows from ground through M_L reverse on-resistance

(r_{lr_on}). After t_{dead}, M_L is turned on by the high v_{gl} to initiate state III and M_L forward on-resistance (r_{lf_on}) conducts i_L. Clearly, in the three transient conduction states, dynamic r_{on}s vary significantly. To obtain the values of dynamic r_{on}s, the straightforward way is to measure both on-state drain-source voltages (v_{hds}, v_{lds}) and currents (i_{hds}, i_{lsd}) directly with multiple voltage and current sensors. Then dynamic r_{on}s can be calculated if v_{hds} and v_{hds} are divided by i_{hds} and i_{lsd}, respectively. Nevertheless, due to the three unique high voltage and high f_{SW} operation states, it is challenging to design integrated sensing and calculation circuits with both high accuracy and low cost.

5.1.3 Full-Profile Dynamic r_{on} Sensing

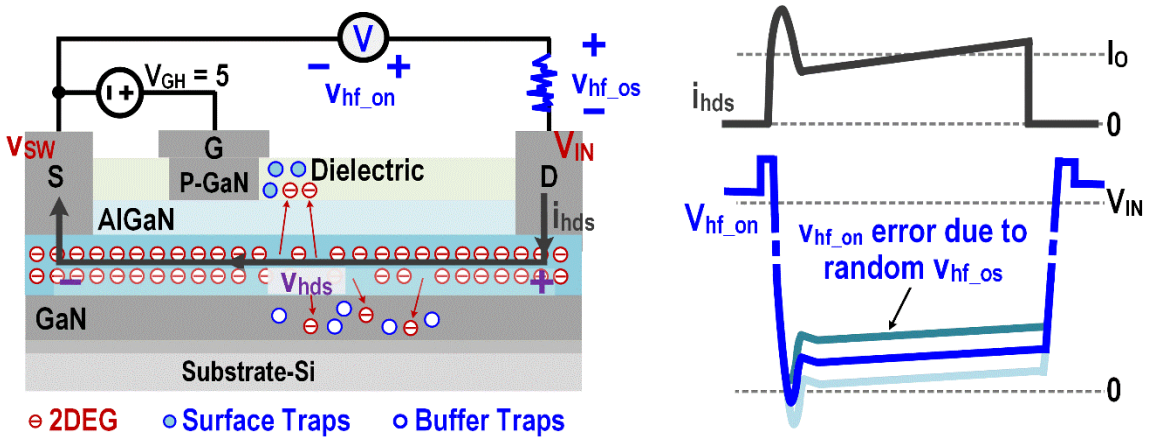


Figure 5.5. Illustrations of M_H forward conduction in state I.

To monitor the full-profile dynamic r_{on}, all the transient operation states need to be analyzed separately. Firstly, to minimize conduction loss of power switches, the on-state voltage is constrained very small, resulting in more sensing difficulties in each state. Specifically, during state I in Figure 5.5, M_H is on and its transient i_{hds} equals i_L, which flows from drain to source of M_H. The low positive v_{hds} increases gradually with the rising i_{hds}. The sensed voltage v_{hf_on} is

$$v_{hf\_on} = r_{hf\_on} \times i_{hds} + v_{hf\_os}. \tag{5.1}$$

Here, v_{hf_os} represents the random offset voltage in the voltage sensing path, which would deteriorate v_{hds} accuracy severely. Besides, the source of M_H is switching node voltage v_{SW}, and it switches between zero and V_{IN} periodically. The floating v_{hf_on} needs to be converted to a ground-referenced voltage for further signal processing, which would induce more errors.

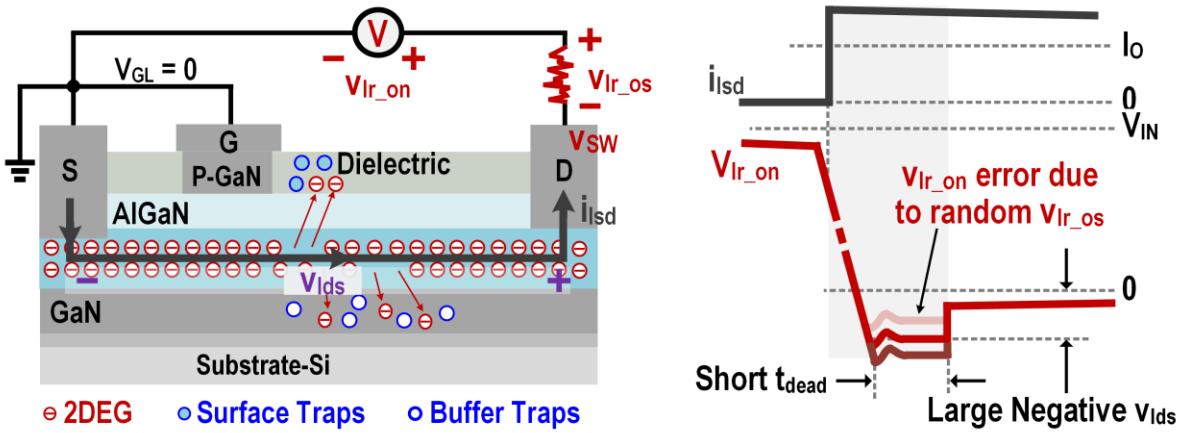


Figure 5.6. Illustrations of M_L reverse conduction in state II.

In state II of Figure 5.6, r_{lr_on} conducts i_L from source to drain of M_L, and a large negative reverse voltage drop v_{lds} across M_L is generated since M_L lacks a body diode. With a zero v_{gl}, v_{lds} is the sum of reverse threshold voltage and the voltage drop across r_{lr_on} [Jones-16, Sun-19, Liu-19b, Sørensen-15]. Thereby, the sensed voltage v_{lr_on} is

$$v_{lr\_on} = -V_{THR} - r_{lr\_on} \times i_{lsd} + v_{lr\_os}. \tag{5.2}$$

Here, V_{THR} is the reverse threshold voltage of M_L, and v_{lf_os} is the sensing offset voltage. Such a large negative v_{lds}, which could be as low as −3V, is hard to be sensed precisely with integrated circuits. A negative v_{SW} sensing scheme is proposed in [Chen-17b], but it requires highly sophisticated circuits and relies on a long t_{dead} for high accuracy, which is harmful to efficiency. The severe tradeoff between short t_{dead} with low power loss and long t_{dead} with high sensing precision limits its performance.

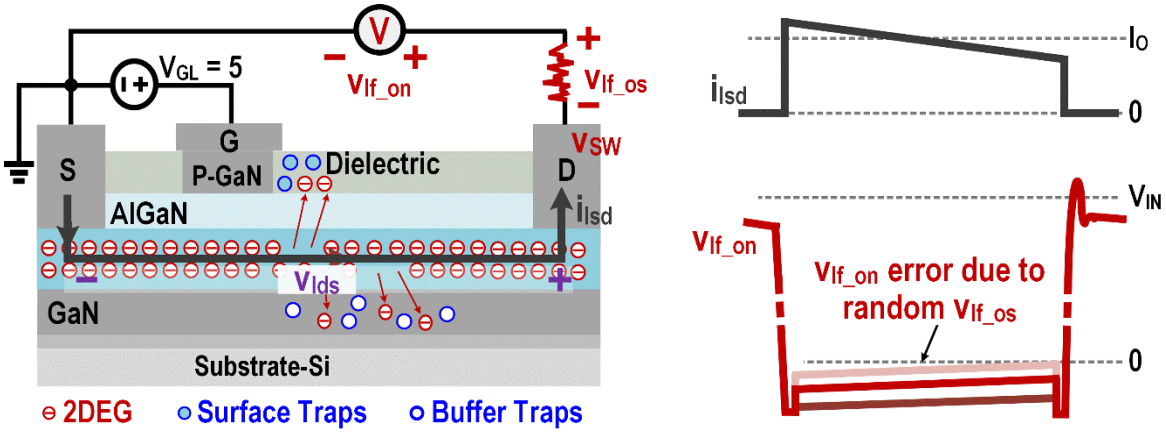


Figure 5.7. Illustrations of M_L forward conduction in state III.

After t_{dead}, state III is shown in Figure 5.7. M_L is turned on by a high driving voltage v_{gl}, and i_L continues flowing through the forward on-resistance of M_L with a negative V_{lds}. Along with the falling i_L, the sensed v_{lf_on} equals

$$v_{lf\_on} = -r_{lf\_on} \times i_{lsd} + v_{lf\_os}, \tag{5.3}$$

where v_{lf_os} is the sensed offset voltage in state III. It is still tricky to sense the value of negative voltage precisely with integrated circuits.

On the other hand, sensing the absolute value of GaN power switch transient current with integrated circuits is also challenging. Classic current measurement techniques, like coaxial shunt, current transformer, split-core current probe and Rogowski coil, would introduce large area cost and implement complexity, and are not suitable for integrated current sensing [Zhang-17]. In contrast, the DCR and series resistor current sensors for buck converters save area and power cost [Lauer-18]. However, the sensing accuracy is highly affected by the value of the parasitic or series resistor, which could vary in a range or lead to extra power loss. Therefore, low-cost tri-state dynamic r_{on} sensing techniques, which does not compromise the integrity of the measurement fidelity, are in high demand.

5.2 On-Chip Self-Calibration

5.2.1 Operation Scheme

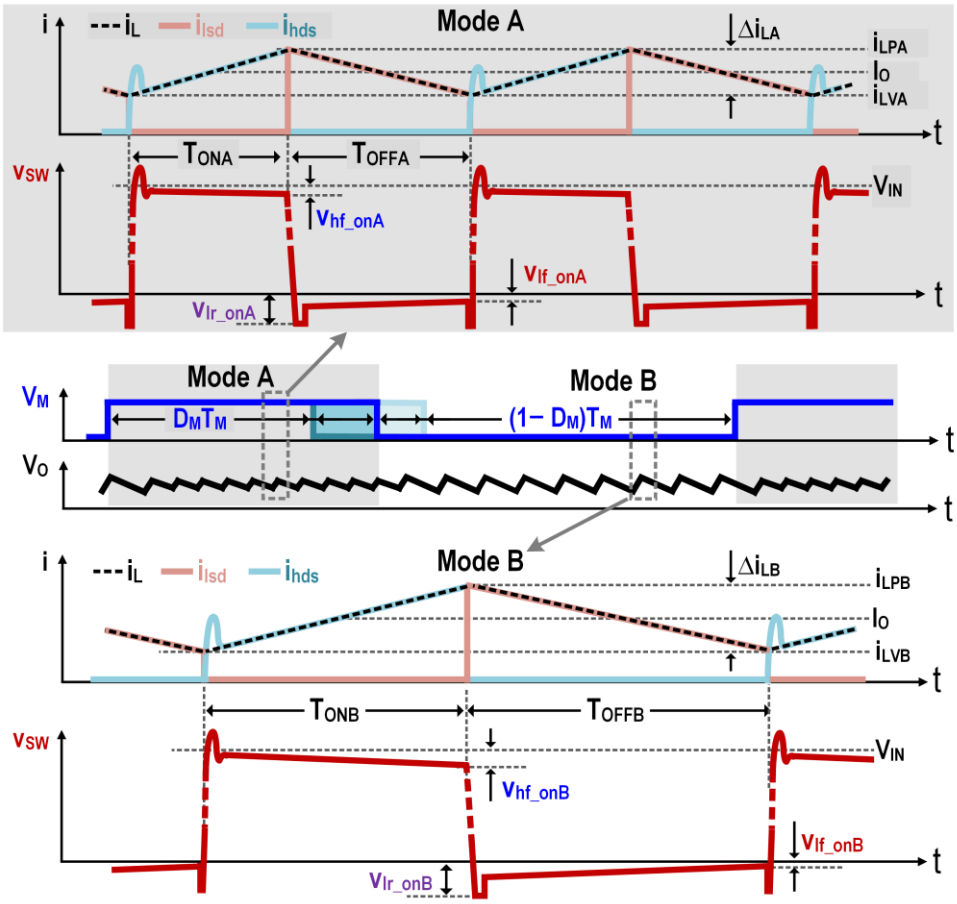


Figure 5.8. Operation scheme of the proposed on-chip self-calibrated full-profile dynamic r_{on} sensing strategy.

To sense the dynamic r_{on}s of GaN HEMTs in all the three states accurately and efficiently, an on-chip self-calibrated full-profile dynamic r_{on} sensing strategy is proposed in Figure 5.8. There are two operation modes with two predefined ON-times (T_{ONS}) in steady state. When the mode signal V_M is high, a constant T_{ONA} is generated in mode A. With a closed-loop control of output voltage V_O, an OFF-time T_{OFFA} is synchronized with a stable i_L profile. The peak and valley values of i_L are i_{LPA} and i_{LVA}. i_L ripple Δi_{LA} is expressed as

$$\Delta i_{LA} = i_{LPA} - i_{LVA} = (V_{IN} - V_O) \times T_{ONA}/L. \quad (5.4)$$

Here, L is the inductor value. At the end of T_{OFFA} in each switching cycle, considering the non-ideal v_{lf_os}, the value of sensed v_{lf_on} is v_{lf_onA} and it equals

$$v_{lf\_onA} = -r_{lf\_on} \times i_{LVA} + v_{lf\_os}. \quad (5.5)$$

Similarly, at the end of T_{ONA}, the value of sensed v_{hf_on} is v_{hf_onA}, which is expressed as

$$v_{hf\_onA} = r_{hf\_on} \times i_{LPA} + v_{hf\_os}. \quad (5.6)$$

During t_{dead}, M_L reverse r_{on} sensing accuracy for v_{lds} is also affected by the non-ideal v_{lr_os}. The value of v_{lr_on}, v_{lr_onA}, is

$$v_{lr\_onA} = -V_{THR} - r_{lr\_on} \times i_{LPA} + v_{lr\_os}. \quad (5.7)$$

It is obvious that the random and unpredictable offset voltages v_{lf_os}, v_{hf_os} and v_{lr_os} could take a high percentage of the low v_{lf_onA}, v_{hf_onA} and v_{lr_onA}, respectively. These contaminated voltages cannot accurately represent healthy conditions of GaN HEMTs in the power converter.

To remove the non-ideal offset voltages and calibrate the sensed voltages, in addition to mode A, another mode B with a longer ON-time T_{ONB} is employed with zero V_M. The ON-time difference ΔT_{ON} equals

$$\Delta T_{ON} = T_{ONB} - T_{ONA}. \quad (5.8)$$

In steady state, a longer OFF-time T_{OFFB} is synchronized and another stable i_L profile is generated with stable peak and valley inductor currents i_{LPB} and i_{LVB}. i_L ripple Δi_{LB} is

$$\Delta i_{LB} = i_{LPB} - i_{LVB} = (V_{IN} - V_O) \times T_{ONB}/L. \quad (5.9)$$

Due to the longer T_{ONB}, Δi_{LB} becomes larger than Δi_{LA}. In Figure 5.8, from mode A to B, the peak inductor current increases from i_{LPA} to i_{LPB}, and the valley inductor current decreases from i_{LVA} to i_{LVB}. The peak and valley inductor current differences Δi_{LP} and Δi_{LV} between the two modes are

$$\Delta i_{LP} = i_{LPB} - i_{LPA}. \tag{5.10}$$

$$\Delta i_{LV} = i_{LVA} - i_{LVB}. \tag{5.11}$$

After combining equations (5.4), (5.8), (5.9), (5.10) and (5.11),

$$\Delta i_{LP} + \Delta i_{LV} = (V_{IN} - V_O) \times \Delta T_{ON}/L. \tag{5.12}$$

In steady states, the average values of i_L in mode A and mode B equal the same I_O. Thus,

$$(i_{LPA} + i_{LVA})/2 = (i_{LPB} + i_{LVB})/2 = I_O. \tag{5.13}$$

By the combination of equations (5.10)–(5.13),

$$\Delta i_{LP} = \Delta i_{LV} = 0.5 \times (V_{IN} - V_O) \times \Delta T_{ON}/L. \tag{5.14}$$

For constant V_{IN}, V_O and L, Δi_{LP} and Δi_{LV} are only determined by ΔT_{ON}, regardless of I_O variations.

Because of the stable i_L profile in mode B, the voltages across dynamic r_{on}s of M_H and M_L are sensed correspondingly. For the same sensing circuits, the random offset voltages in mode B equal those in mode A. The sensed voltage values are v_{lf_onB}, v_{hf_onB} and $v_{lr\_onB,}$ which equal

$$v_{lf\_onB} = -r_{lf\_on} \times i_{LVB} + v_{lf\_os}. \tag{5.15}$$

$$v_{hf\_onB} = r_{hf\_on} \times i_{LPB} + v_{hf\_os}. \tag{5.16}$$

$$v_{lr\_onB} = -V_{THR} - r_{lr\_on} \times i_{LPB} + v_{lr\_os}. \tag{5.17}$$

With equations (5.5)–(5.7) and (5.15)–(5.17), the sensed differences between mode A and B are:

$$\Delta v_{lf\_on} = |v_{lf\_onA} - v_{lf\_onB}| = r_{lf\_on} \times \Delta i_{LV}. \tag{5.18}$$

$$\Delta v_{hf\_on} = |v_{hf\_onA} - v_{hf\_onB}| = r_{hf\_on} \times \Delta i_{LP}. \tag{5.19}$$

$$\Delta v_{lr\_on} = |v_{lr\_onA} - v_{lr\_onB}| = r_{lr\_on} \times \Delta i_{LP}. \tag{5.20}$$

It shows that the offset voltages (v_{lf_os}, v_{hf_os} and v_{lr_os}) are eliminated automatically and the sensed voltage differences (Δv_{lf_on}, Δv_{hf_on}, Δv_{lr_on}) are only related to Δi_{LP} and Δi_{LV}. The sensing accuracy is thus improved significantly. According to equation (5.14), the values of Δi_{LP} and Δi_{LV} are

constant with the predefined ΔT_{ON}, which is not vulnerable to the variable I_O affected by application conditions. Thereby, high-speed and high-precision current sensors are avoided for dynamic r_{on} calculation, reducing circuit complexity greatly with low overheads.

Meanwhile, the period of mode A, D_M, can be actively controlled to optimize efficiency of the power converter. Based on the power loss difference between mode A and mode B, the period ratio $D_M/(1-D_M)$ can be adaptively optimized, supporting active thermal control of GaN-based power converter for lifetime extension. Compared to the proactive temperature frequency scaling method in [Chen-21], which induces a continuously variable f_{SW}, only two fixed f_{SW}s are generated in this design. Its predictable EMI noise highly simplifies EMI filter design and improve reliability.

5.2.2 System Architecture

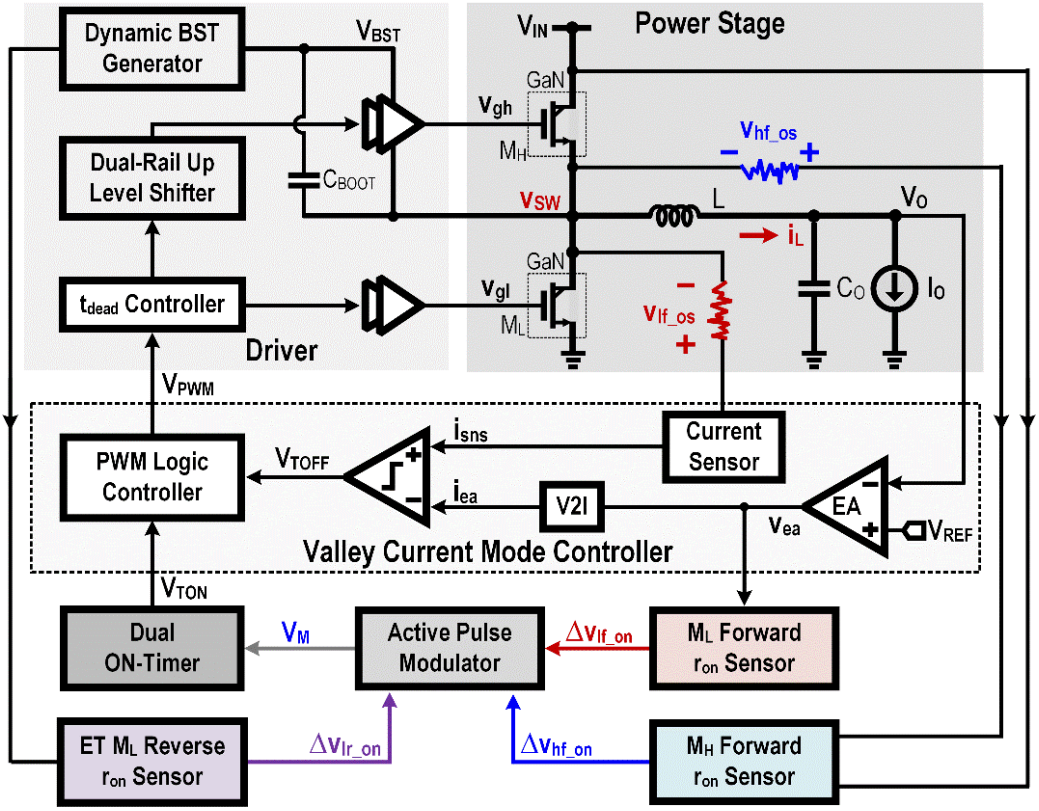


Figure 5.9. Block diagram of the proposed GaN-based buck converter.

Figure 5.9 illustrates the proposed adaptive dual ON-time (DOT) controlled GaN-based buck converter, incorporating the on-chip self-calibrated full-profile dynamic r_{on} sensing strategy. It mainly includes two e-mode GaN HEMTs in the power stage, dual ON-timer, valley current mode controller, integrated tri-state dynamic r_{on} sensors, active pulse modulator, and driver circuits with dynamic BST generator and dual-rail up-level shifter. The dual ON-timer predefines T_{ONA} and T_{ONB} in two operation modes, and the valley current mode controller synchronizes corresponding T_{OFFA} and T_{OFFB} for closed-loop regulation. The integrated tri-state dynamic r_{on} sensors including M_L forward r_{on} sensor, M_H forward r_{on} sensor and ET M_L reverse r_{on} sensor, achieve high sensing accuracy with low area and power overheads. The active pulse modulator controls mode transition and supports active thermal control of the converter. The dynamic BST circuit is developed to control BST rail voltage, and the dual-rail up-level shifter maintains high-speed driving signal transmission regardless of large negative v_{SW} during t_{dead}.

5.3 Circuit Implementations

5.3.1 Integrated M_L Forward r_{on} Sensor

As described in Section 5.1, the separated voltage and current sensing scheme would induce high area and power penalties. Thanks to the proposed DOT control, complicated current sensing circuits are eliminated for simple implementation and low cost. Besides, the requirement of voltage sensing precision is also reduced greatly since the DOT operation can eliminate sensing errors inherently. Furthermore, the M_L forward r_{on} sensing circuit is compact with the feedback controller of power converter with low silicon and power overheads. The circuit schematic of the integrated M_L forward r_{on} sensor is shown in Figure 5.10. In addition to the circuits of valley current

mode controller for the closed-loop V_O regulation, only one PMOS (M_2), one resistor (αR_{OSL}), two sensing switches (S_{LA} and S_{LB}) and two sampling capacitors (C_{LA} and C_{LB}) are added for M_L forward r_{on} sensing.

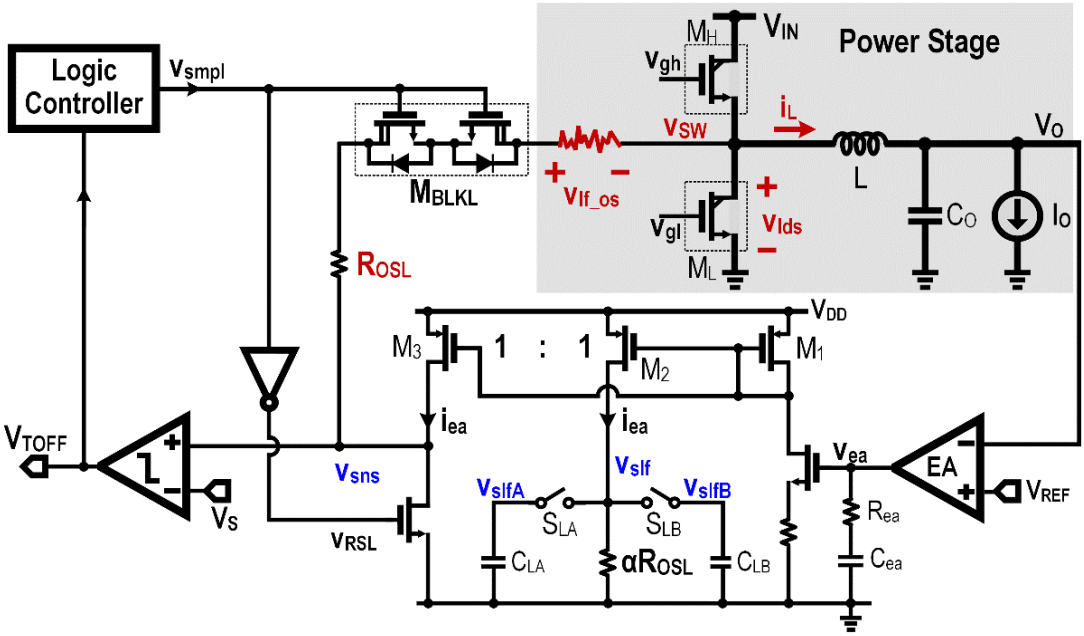


Figure 5.10. Circuit schematic of integrated M_L forward r_{on} sensor.

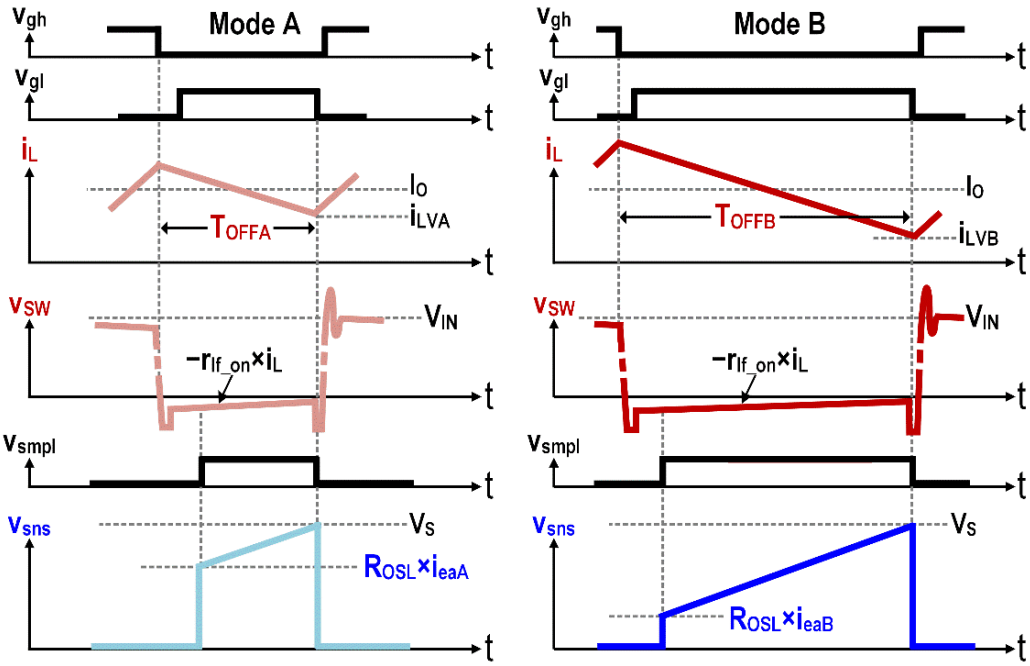


Figure 5.11. Operation waveforms of integrated M_L forward r_{on} sensor.

Figure 5.11 describes the operation waveforms of valley current mode control and M_L forward r_{on} sensing. At the beginning of T_{OFF}, v_{gh} turns low to turn off M_H. v_{SW} falls below zero due to the freewheeling i_L through the turned-off M_L. Then M_L is turned on by the high v_{gl}, and r_{lf_on} starts to conduct i_L, generating a negative v_{SW}. After a blanking period, v_{smpl} turns on the blocking switch M_{BLKL}. Thanks to the feedback current i_{ea} on R_{OSL}, the negative v_{SW} is shifted up to a positive v_{sns}, which tracks v_{SW} rising path due to the falling i_L. Once v_{sns} crosses the constant reference voltage V_S, V_{TOFF} is triggered high to terminate T_{OFF}. In steady state, a constant i_{ea} is generated by the feedback voltage of error amplifier v_{ea} for V_O regulation. One current mirror copies i_{ea} on the matched resistor αR_{OSL}. Thus, the voltage on αR_{OSL} equals

$$v_{slf} = \alpha \times R_{OSL} \times i_{ea}. \tag{5.21}$$

In mode A, for a stable valley inductor current i_{LVA}, if the non-ideal v_{lf_os} is considered, the value of V_S is

$$V_S = R_{OSL} \times i_{eaA} - r_{lf\_on} \times i_{LVA} + v_{lf\_os}. \tag{5.22}$$

Here, i_{eaA} is the value of stable i_{ea} in steady state. By combining equations (5.21) and (5.22), the value of v_{slf} is v_{slfA}, and it equals

$$v_{slfA} = \alpha \times (V_S + r_{lf\_on} \times i_{LVA} - v_{lf\_os}). \tag{5.23}$$

Similarly, in steady state of mode B, when the valley inductor current is stable as i_{LVB}, the value of V_S equals

$$V_S = R_{OSL} \times i_{eaB} - r_{lf\_on} \times i_{LVB} + v_{lf\_os}. \tag{5.24}$$

Here, i_{eaB} is the stable value of i_{ea} in mode B. By combining equations (5.21) and (5.24), the value of v_{slf} is v_{slfB}, and it equals

$$v_{slfB} = \alpha \times (V_S + r_{lf\_on} \times i_{LVB} - v_{lf\_os}). \tag{5.25}$$

After combining equations (5.11), (5.23) and (5.25), the sensed voltage difference of v_{slf} between mode A and mode B is

$$\Delta v_{slf} = v_{slfA} - v_{slfB} = \alpha \times r_{lf\_on} \times \Delta i_{LV}. \tag{5.26}$$

As the resistor ratio α can be controlled precisely by matching two integrated resistors, the sensed Δv_{slf} is only related to the predefined Δi_{LV}, which is controlled by a constant ΔT_{ON}. Thus, the amplified Δv_{slf} can represent r_{lf_on} directly without non-ideal v_{lf_os} and complicated current sensors. At the ends of the two operation modes, the two values (v_{slfA}, v_{slfB}) of v_{slf} are sampled on capacitors C_{LA} and C_{LB} respectively for further system characterization and optimization.

5.3.2 Integrated M_H Forward r_{on} Sensor

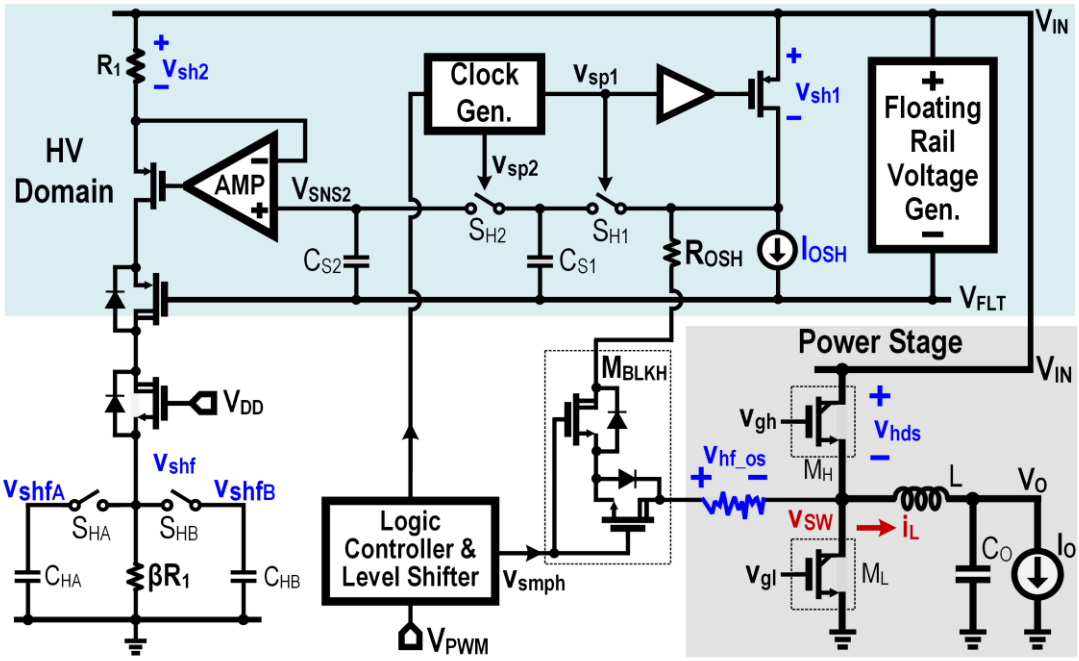


Figure 5.12. Circuit schematic of integrated M_H forward r_{on} sensor.

The circuit schematic of the proposed integrated M_H forward r_{on} sensor is depicted in Figure 5.12. It includes two voltage domains for both dynamic v_{hds} sensing and signal processing. In the HV domain, a constant rail voltage V_{FLT} is regulated by a floating rail voltage generator, generating

a constant voltage difference between V_{IN} and V_{FLT} to power sensing circuits in HV domain. A high voltage blocking switch M_{BLKH} and sampling circuits are controlled by V_{PWM} through the logic controller and level shifter. In each switching cycle, the peak value of v_{hds} is captured at the end of T_{ON} in the HV domain and it is converted down to the LV domain value for further condition monitoring analysis.

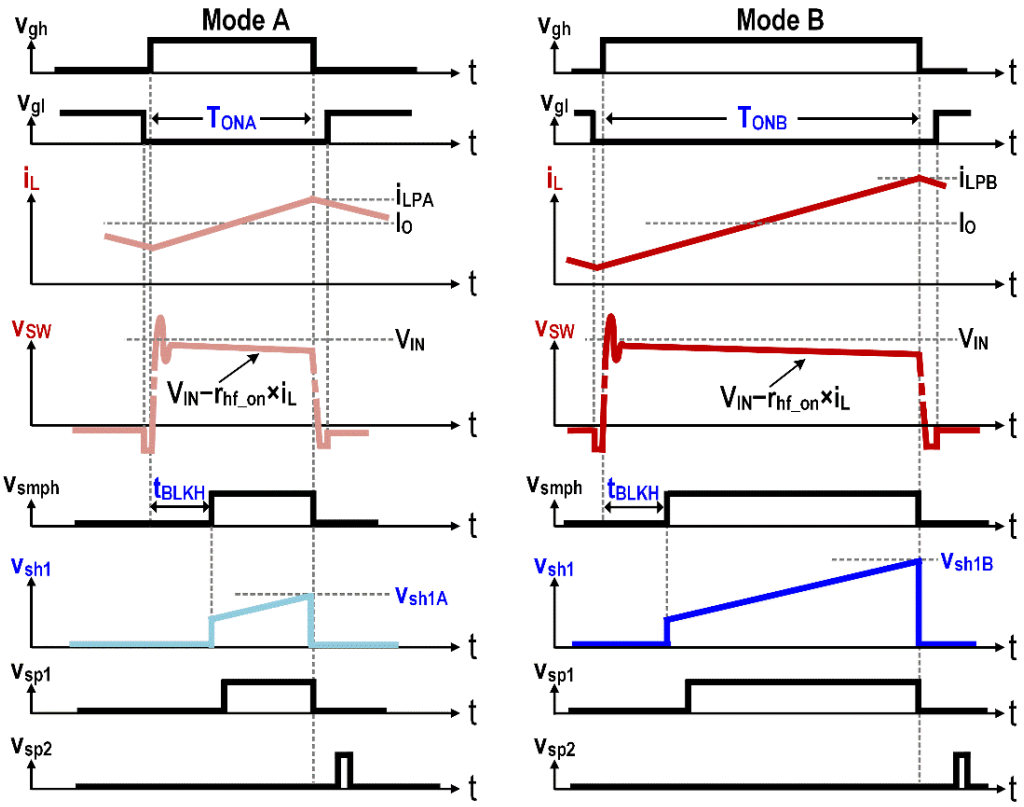


Figure 5.13. Operation waveforms of integrated M_H forward r_{on} sensor.

Figure 5.13 demonstrates the detailed operation waveforms. At the start of T_{ONA} in mode A, M_H is turned on by v_{gh} and v_{SW} rises close to V_{IN}. Due to the conducting i_L through M_H, v_{SW} is

$$v_{SW} = V_{IN} - r_{hf\_on} \times i_L. \tag{5.27}$$

After a blanking period t_{BLKH}, the v_{SW} ringing settles down to a stable value. With the logic controller and level shifter, the sample signal v_{smph} rises high to turn on the blocking switch M_{BLKH}

for v_{SW} sensing in the HV domain. v_{SW} is further shifted down by an offset resistor R_{OSH} and an offset current I_{OSH}, ensuring v_{sh1} to be constant positive regardless of v_{SW} ringing effects. Considering the non-ideal v_{hf_os}, v_{sh1} is expressed as

$$v_{sh1} = R_{OSH} \times I_{OSH} + r_{hf\_on} \times i_L - v_{hf\_os}. \tag{5.28}$$

The switch S_{H1} is turned on by v_{SP1} and the voltage on C_{S1} tracks v_{sh1} till the end of T_{ONA}. Thus, in mode A, the peak value of v_{sh1}, v_{sh1A}, is kept on C_{S1} and it equals

$$v_{sh1A} = R_{OSH} \times I_{OSH} + r_{hf\_on} \times i_{LPA} - v_{hf\_os}. \tag{5.29}$$

Then a positive pulse v_{sp2} transmits v_{sh1A} to the input of amplifier with capacitor C_{S2}, which is further converted to v_{shf} in the LV domain. The value of v_{shf}, v_{shfA}, is

$$v_{shfA} = \beta \times (R_{OSH} \times I_{OSH} + r_{hf\_on} \times i_{LPA} - v_{hf\_os}). \tag{5.30}$$

Similarly, in mode B with stable i_{LPB}, the same sampling operation repeats, and the value of sensed v_{shf}, v_{shfB}, is

$$v_{shfB} = \beta \times (R_{OSH} \times I_{OSH} + r_{hf\_on} \times i_{LPB} - v_{hf\_os}). \tag{5.31}$$

By combining equations (5.10), (5.30) and (5.31), the sensed voltage difference between mode A and mode B, Δv_{shf} equals

$$\Delta v_{shf} = v_{shfB} - v_{shfA} = \beta \times r_{hf\_on} \times \Delta i_{LP}. \tag{5.32}$$

In the DOT operation of the half-bridge converter, it shows that Δv_{shf} is determined by constant Δi_{LP} and the ratio β, which can be controlled precisely with two integrated resistors R_1 and βR_1. Besides, according to equation (5.14), the value of Δi_{LP} can be actively determined by the on-duty time difference between mode A and mode B. With a fixed power conversion specification, the value of Δi_{LP} can be kept constant regardless of load current variations. Thus, the dynamic r_{hf_on} can be expressed by the stable Δv_{shf} equivalently without extra sensing errors. The

high-resolution current sensors are also eliminated for circuity simplicity and low cost. At the ends of mode A and mode B, the two stable values (v_{shfA}, v_{shfB}) of v_{shf} are sensed on capacitor C_{HA} and C_{HB}, respectively, and they are used for further signal processing regarding dynamic r_{on} analysis.

5.3.3 Integrated ET M_L Reverse r_{on} Sensor

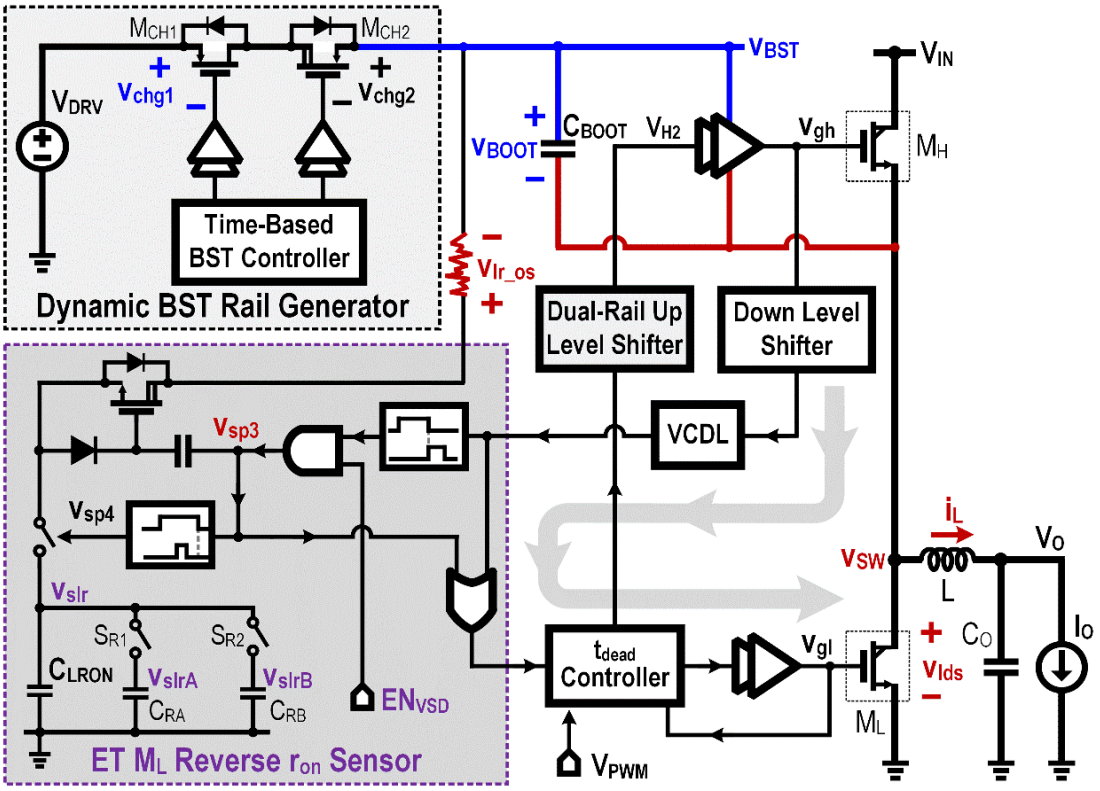


Figure 5.14. Circuit schematic of integrated ET M_L reverse r_{on} sensor.

To sense M_L reverse r_{on} efficiently and precisely, the ET sensing scheme is employed for r_{lr_on} sensing, which breaks the severe trade-off of low power loss and high sensing accuracy. The circuit schematic of ET M_L reverse r_{on} sensor is shown in Figure 5.14. The ET M_L reverse r_{on} sensor is compatible with the dynamic BST rail generator to simplify the design complexity. With a dynamic BST rail generator, the voltage on BST capacitor C_{BOOT}, v_{BOOT}, is constant for a stable I_O in both mode A and mode B. Thus, the constantly positive v_{BST} can be used for negative v_{SW} sensing

indirectly, eliminating complicated negative v_{SW} sensing circuits. During normal operation, the low EN_{VSD} disables ET M_L reverse r_{on} sensor with minimized t_{dead}, achieving high conversion efficiency. In comparison, when the sensing scheme is occasionally activated by high EN_{VSD}, t_{dead} is extended long to ensure high sensing accuracy of negative v_{SW}.

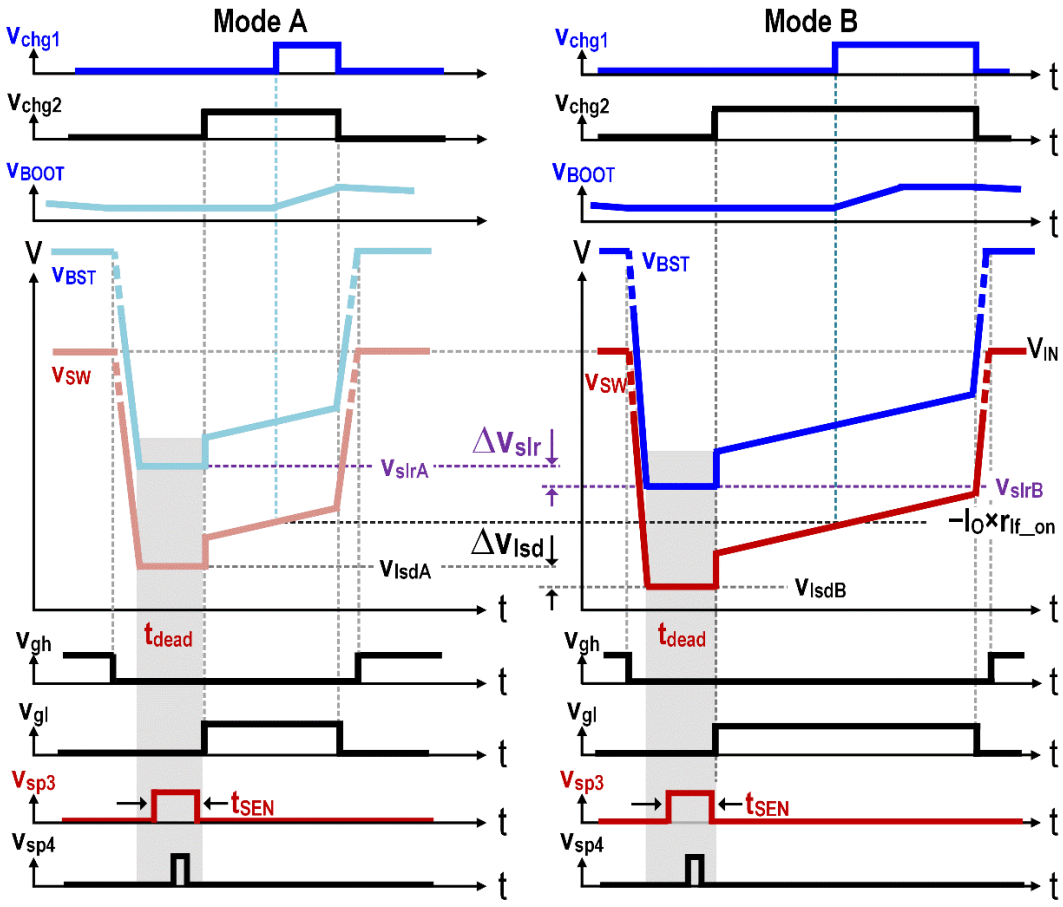


Figure 5.15. Operation waveforms of integrated ET M_L reverse r_{on} sensor.

Figure 5.15 depicts the operation waveforms. In each switching cycle, the dynamic BST rail generator senses the value of T_{OFF} and turns on the BST charge switches M_{CH1} and M_{CH2} at the middle of T_{OFF}. Then C_{BOOT} starts to be charged when v_{SW} crosses $(-r_{lf\_on} \times I_O)$ in both mode A and mode B. Thus, v_{BOOT} across C_{BOOT} is only dependent on I_O. When M_L reverse r_{on} sensor is activated, v_{SP3} and v_{SP4} control sensing switches, and the positive v_{BST} during t_{dead} is transmitted to capacitor

C_{LRON}. Then the voltage on C_{LRON}, v_{slr}, is sensed efficiently. In mode A, when M_L is reversely conducting i_{LPA} during t_{dead}, the sensed voltage v_{slr} is affected by the non-ideal v_{lr_os}. The value of v_{slr}, v_{slrA}, is expressed as

$$v_{slrA} = v_{BOOT} - V_{THR} - r_{lr\_on} \times i_{LPA} + v_{lr\_os}. \tag{5.33}$$

Similarly, in mode B, when M_L is reversely conducting i_{LPB}, the sensed value of v_{slr}, v_{slrB}, is

$$v_{slrB} = v_{BOOT} - V_{THR} - r_{lr\_on} \times i_{LPB} + v_{lr\_os}. \tag{5.34}$$

At the ends of mode A and mode B, the values of v_{slrA} and v_{slrB} are sampled on capacitors C_{RA} and C_{RB}, respectively. The sensed voltage difference between mode A and mode B equals,

$$\Delta v_{slr} = v_{slrA} - v_{slrB} = r_{lr\_on} \times \Delta i_{LP}. \tag{5.35}$$

It shows the non-ideal v_{lr_os} is removed and the clean Δv_{slr} is only determined by the constant Δi_{LP}, Hence, Δv_{slr} can be used to represent the equivalent r_{lr_on} with high sensing accuracy.

5.3.4 Dual-Rail Up-Level Shifter

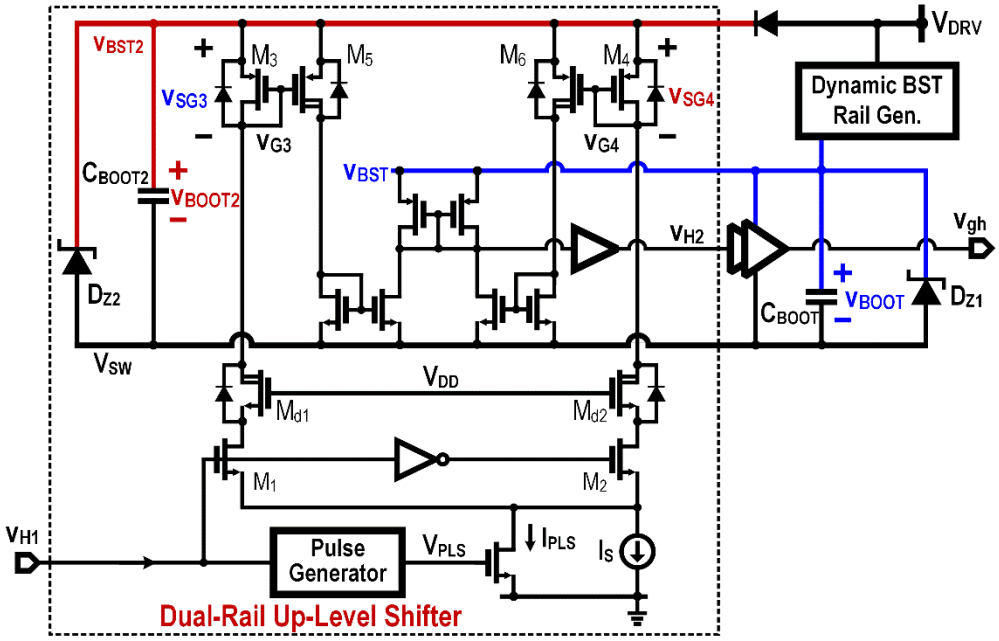


Figure 5.16. Circuit schematic of dual-rail up-level shifter.

Figure 5.16 shows the circuit schematic of the proposed dual-rail up-level shifter in GaN driving circuits. In contrast to conventional up-level shifters, two separated BST rail voltages, instead of one shared rail voltage, are employed in the up-level shifter. In the dual-rail up-level shifter, the voltage v_{BOOT} across C_{BOOT} is regulated by the dynamic BST rail generator to supply power of buffer diver for GaN HEMT M_H. It is constantly regulated below 5V to protect the driving circuits and M_H from HV breakdown. In addition to v_{BST}, one extra BST rail voltage v_{BST2} is adopted in the up-level shifter. The BST capacitor C_{BOOT2} is charged by V_{DRV} directly through one HV diode. v_{BST2} is kept constant above 3V even though v_{SW} can be lower than −3V during t_{dead}. v_{BST2} is designed to maintain low propagation delay of up-level shifter during t_{dead} to improve the driving reliability. The two rail voltages (v_{BST}, v_{BST2}) achieve both low propagation delay and high reliability for M_H driving stage. Compared to the up-level shifters with separated BST rail voltages in [Ming-19, Liu-19a], the major difference of this work lies in the measured verifications with buck converters, illustrating that its performance is not affected by the large negative v_{SW}.

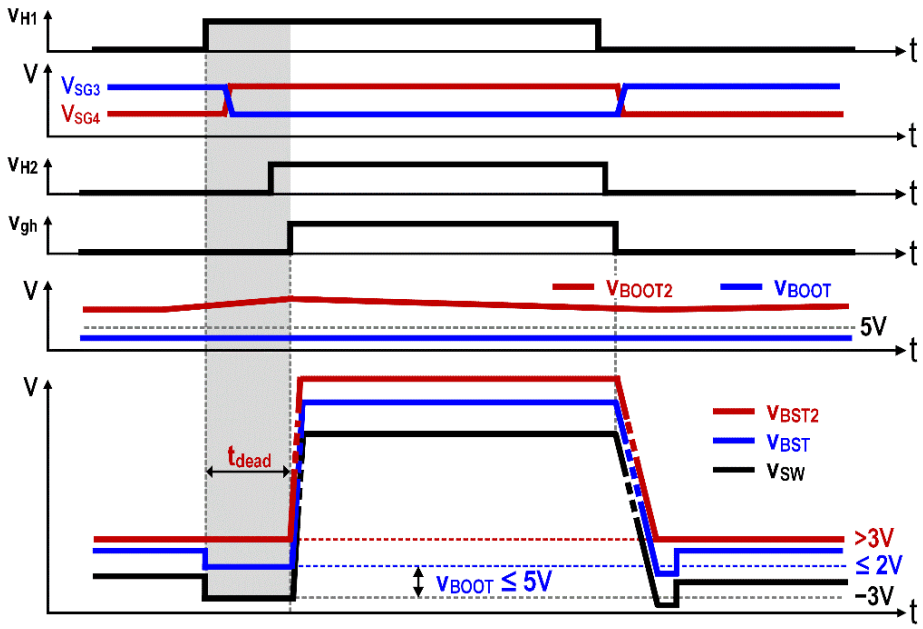


Figure 5.17. Operation waveforms of dual-rail up-level shifter.

The operation waveforms are explained in Figure 5.17. For a positive valley inductor current i_{LV}, when M_L is turned off, i_{LV} freewheels through the r_{lr_on} of M_L. Because of the peculiar characteristics of the GaN HEMT, v_{SW} could be largely negative for a largely positive i_{LV}. Thanks to the dynamic BST rail generator for buffer driver, v_{BOOT} is below 5V and v_{BST} could be below 2V during t_{dead} as a consequence. When v_{H1} rises high, M_1 is turned on and M_2 is off. The static current I_S and pulse current I_{PLS} pass through M_1 and M_3, inducing a much higher v_{SG3} than v_{SG4}. Since the low v_{BST} is replaced by the high v_{BST2}, enough margin of v_{SG3} increment is maintained and v_{G3} is far above zero for fast signal transmission. Because of the high v_{BOOT2}, two extra HV PMOS M_5 and M_6 are used to transmit the driving signal from v_{BOOT2} rail to v_{BOOT} rail. v_{H2} rises high, and the output of buffer driver v_{gh} turns on the power device.

5.4 Experimental Verification

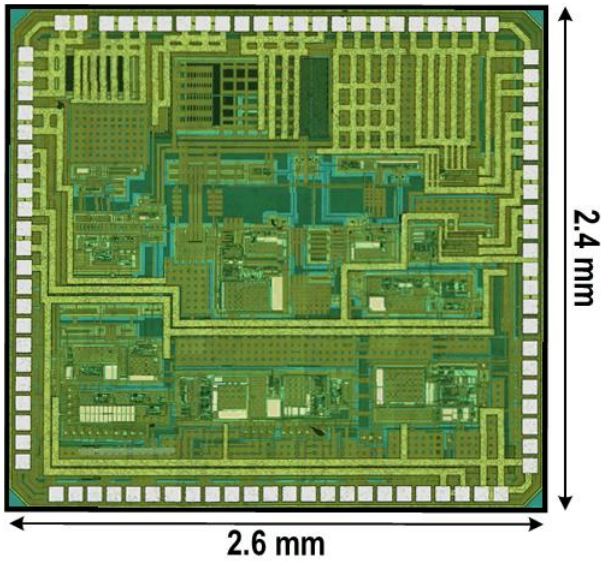


Figure 5.18. Chip micrograph.

The proposed design is implemented using a 180-nm HV BCD process. Figure 5.18 shows the chip photograph with a total area of 6.24mm^2. In Figure 5.19, two e-mode GaN HEMTs are

used as power switches in the buck converter on PCB. With one 640-nH inductor and one 22-µF output capacitor, the converter operates with 5 to 12V V_{IN} and delivers a regulated 1V V_O with a maximum I_O of 1A. The instant full-profile tri-state dynamic r_{on} sensing system for GaN HEMTs consumes only 0.3mm^2 and 1.1mW, and 4.8% chip and 0.077% power overheads are generated by the state-of-health monitoring system.

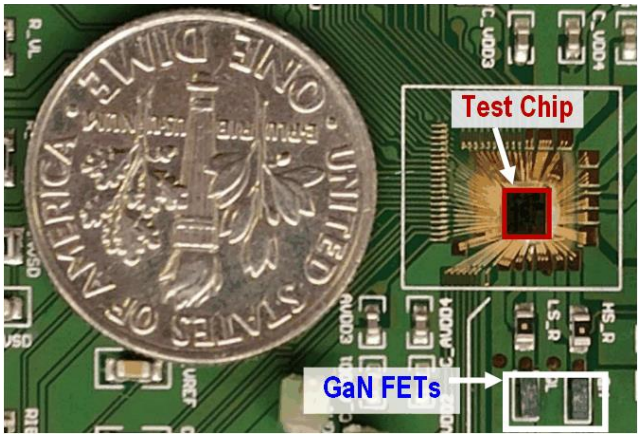


Figure 5.19. Photograph of PCB test board.

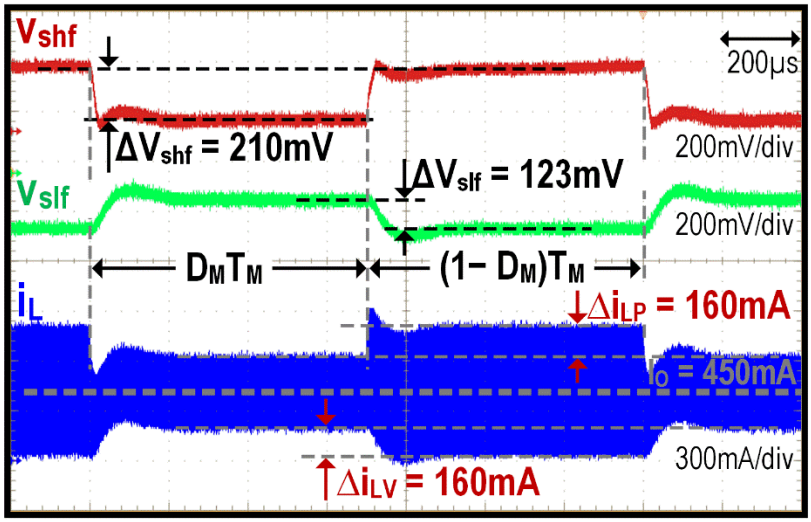
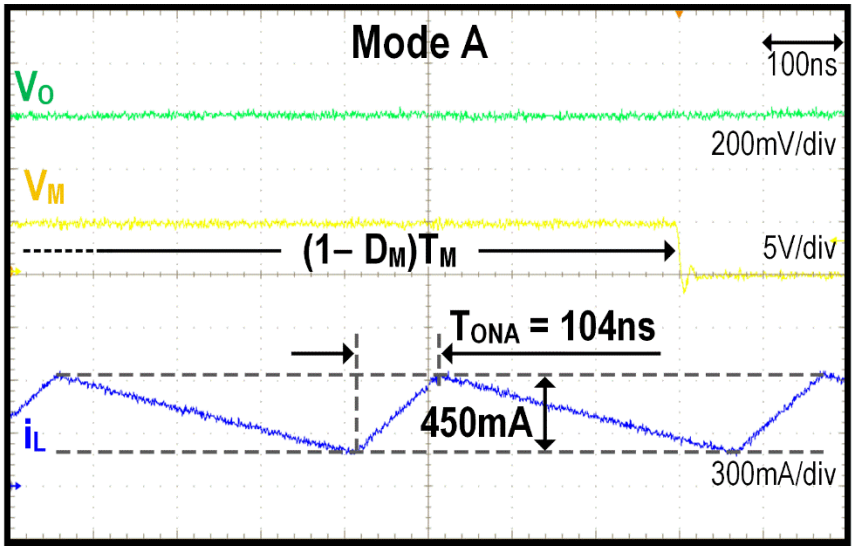


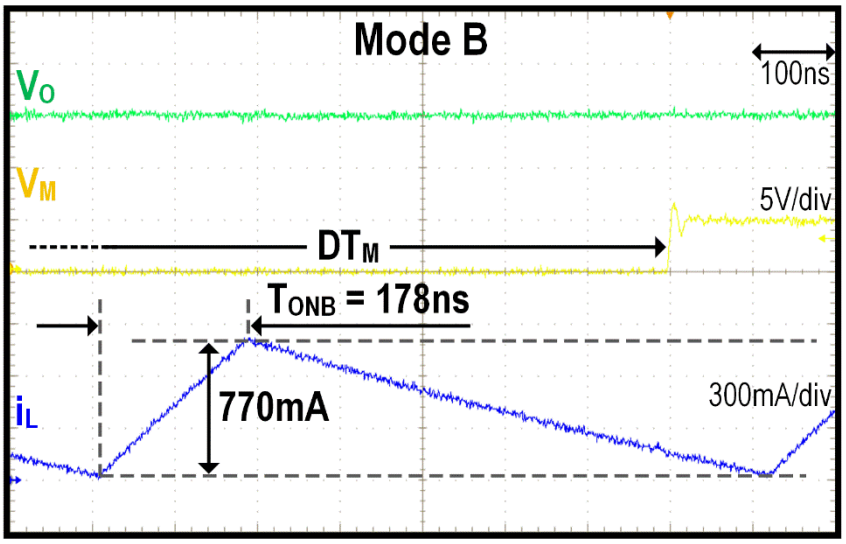
Figure 5.20. Measured full-profile waveforms of adaptive DOT operation and sensed M_H and M_L dynamic forward r_{on}s.

To validate the instant dynamic r_{lf_on} and r_{hf_on} sensing in M_L forward conduction and M_H forward conduction states, Figure 5.20 shows the measured transient full-profile waveforms of

adaptive DOT operation and the sensed dynamic M_H and M_L forward r_{on}s when I_O is 450mA. In mode A and mode B, the values of average I_L are both 450mA. But due to the predefined ON-time difference in the two modes, two different I_L profiles are generated and the sensed v_{shf} and v_{slf} change accordingly. Δi_{LP} and Δi_{LV} are stable as 160mA, and the sensed Δv_{shf} and Δv_{slf} are measured as 210mV and 123mV, respectively.



(a)



(b)

Figure 5.21. Measured adaptive DOT operation: (a) zoomed-in view in mode A, and (b) zoomed-in view in mode B.

The zoomed-in view in mode A is shown in Figure 5.21(a). For a positive V_M, a short T_{ONA} is 104ns and the i_L peak-to-peak ripple is 450mA. On the other hand, Figure 5.21(b) presents the zoomed-in view in mode B. The mode control signal V_M is zero and the long T_{ONB} equals 178ns with 770-mA i_L peak-to-peak ripple. Meanwhile, it is also verified that the converter can achieve well-regulated V_O in the two operation modes.

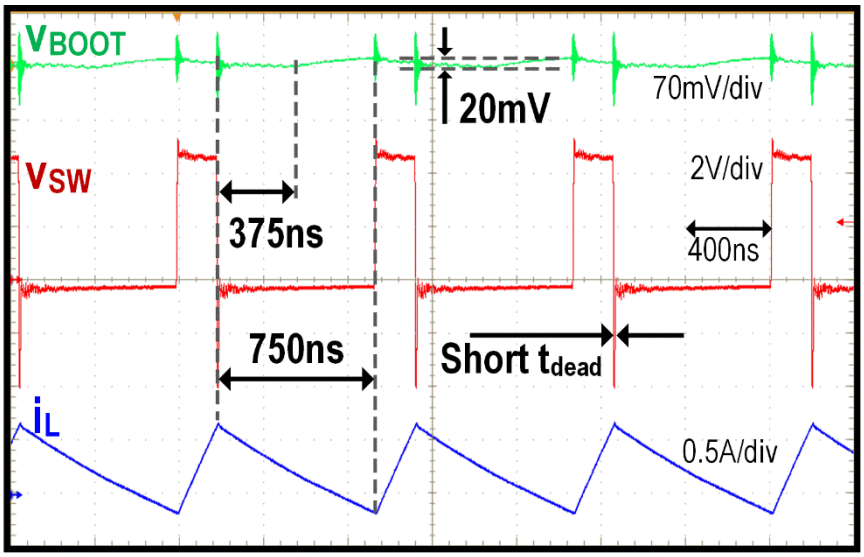
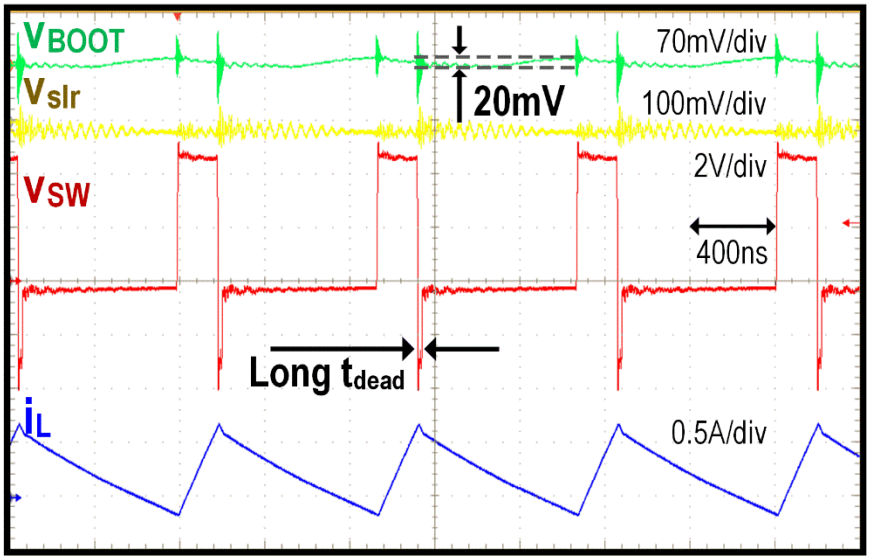
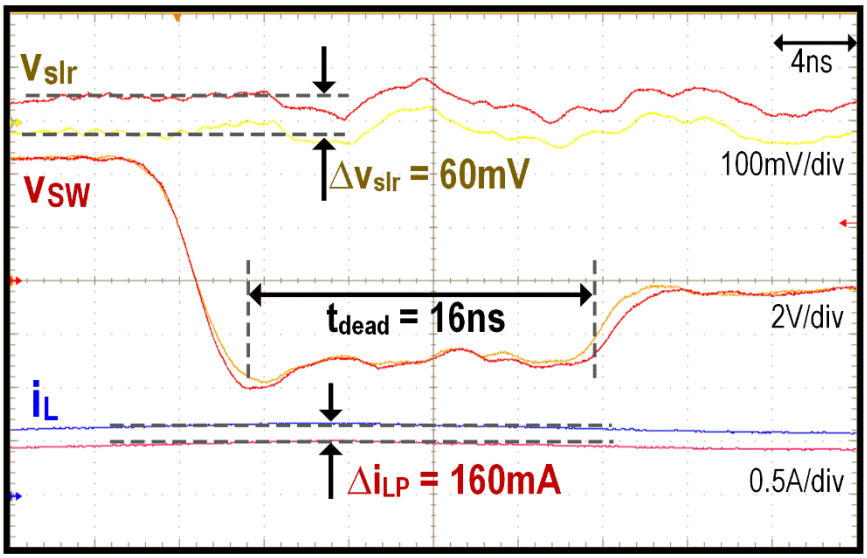


Figure 5.22. Measured operation waveforms of dynamic BST.

In order to evaluate ET M_L reverse r_{on} sensing, Figure 5.22 illustrates the key measured waveforms including v_{BOOT}, v_{SW} and i_L when the sensing scheme is disabled. It shows that t_{dead} is minimized for high power efficiency in normal operation. With a 750-ns T_{OFF}, the bootstrap rail voltage gets charged after a delay period of 375ns. The BST rail voltage v_{BOOT} ripple is below 20mV. In comparison, when the M_L reverse r_{on} sensing scheme is enabled, the key waveforms are explicated in Figure 5.23(a), showing an extended t_{dead} for high r_{lr_on} sensing accuracy with a positive v_{SLR}. In Figure 5.23(b), during r_{lr_on} sensing period, the v_{SW} falling edge t_{dead} is extended to about 16ns for precise r_{lr_on} sensing. In the DOT operation, due to the 160mA Δi_{LP}, the sensed Δv_{SLR} is 60mV.



(a)

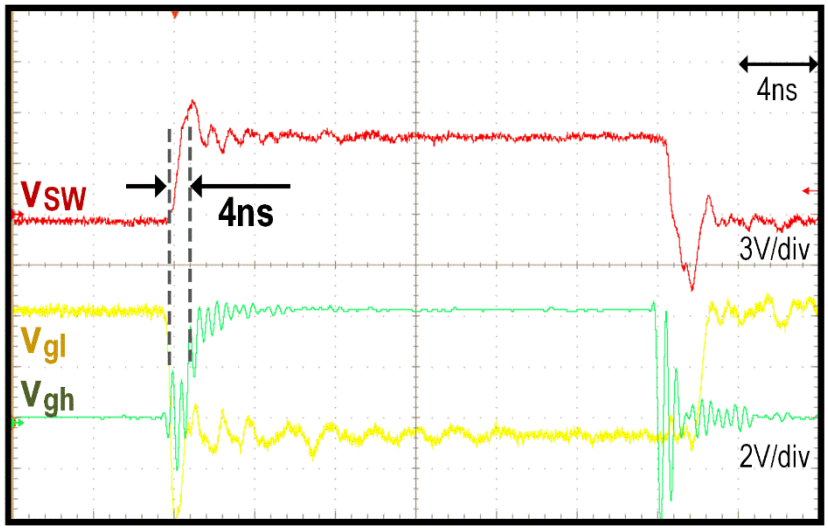


(b)

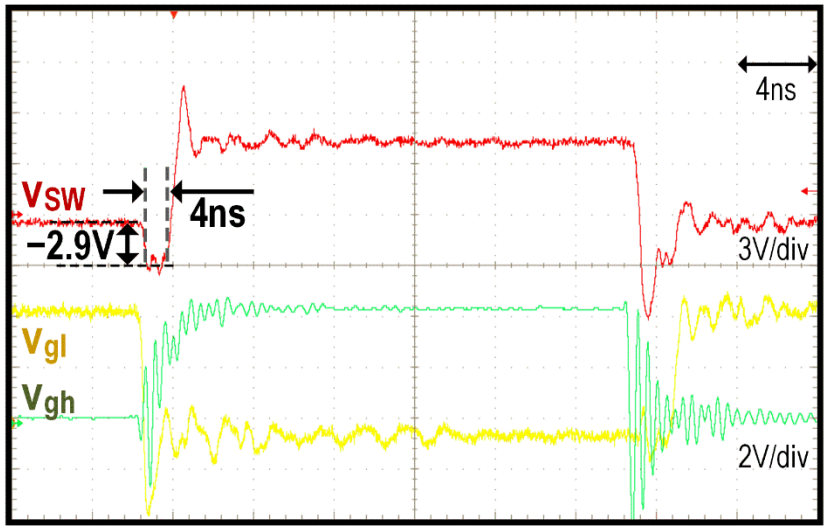
Figure 5.23. Measured ET M_L reverse r_{on} sensing: (a) steady state waveforms when sensing is enabled, and (b) zoom-in Δv_{slr} during t_{dead} for DOT operation.

When verifying the functions of the proposed dual-rail up-level shifter, Figure 5.24 shows measured transient waveforms of switching node voltage and gate driving signals, v_{SW}, v_{gh} and v_{gl} with either a negative or positive i_{LV}. For a negative i_{LV} in Figure 5.24(a), v_{SW} is charged up by i_{LV} automatically, showing a 4-ns t_{dead} for v_{SW} rising edge. In Figure 5.24(b), even though v_{SW} is as low

as −2.9V due to the positive i_{LV}, t_{dead} is still maintained as 4ns. Thus, it is proved that the dual-rail up-level shifter performance is not affected by large negative v_{SW} during t_{dead} and can maintain low propagation delay.



(a)



(b)

Figure 5.24. Measured v_{SW}, v_{gh} and v_{gl} with (a) negative i_{LV}, and (b) positive i_{LV}.

The efficiency measurement is also shown in Figure 5.25 with the two T_{ONS} and D_{MS}, and the peak efficiency is 89.2%. Figure 5.26 provides the power loss for $D_M=0.9$ and $D_M=0.1$ with a maximum loss difference of 32mW. When the aging precursor of GaN HEMT exceeds the aging

threshold, an active thermal control is activated automatically by modulating D_M to extend GaN HEMTs lifetime in Figure 5.27. If the sensed full-profile r_{on} increases, D_M decreases to reduce power loss and slow down aging process (r_{on} rising). Compared to a two-step driver for active thermal control [Prasobhu-16], although the power loss modulation range in this design is low, beyond-MHz operation without hardware overhead is facilitated.

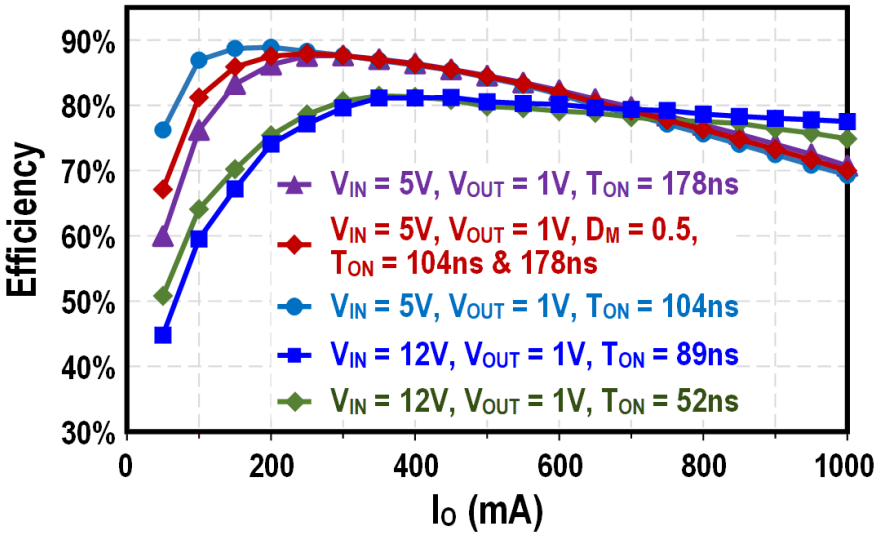


Figure 5.25. Measured Efficiency with T_{ON}s and D_Ms.

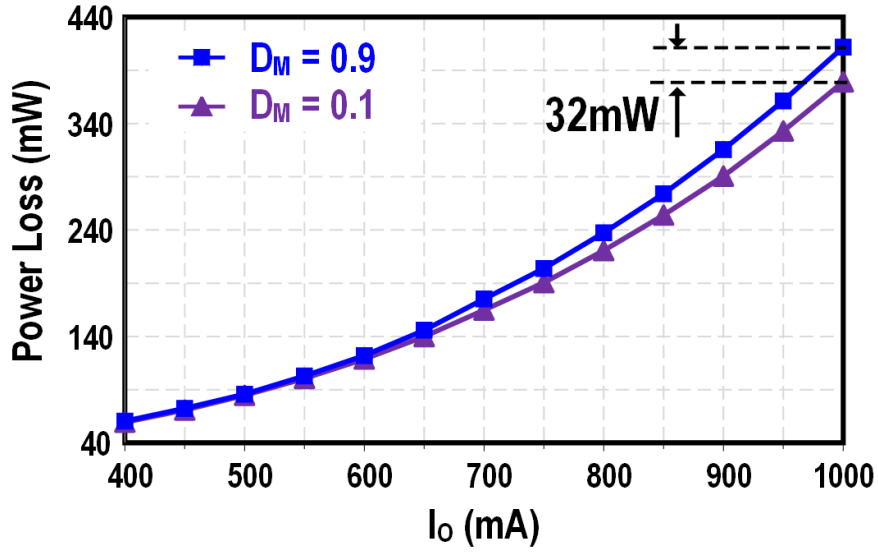


Figure 5.26. Measured power loss for different D_Ms.

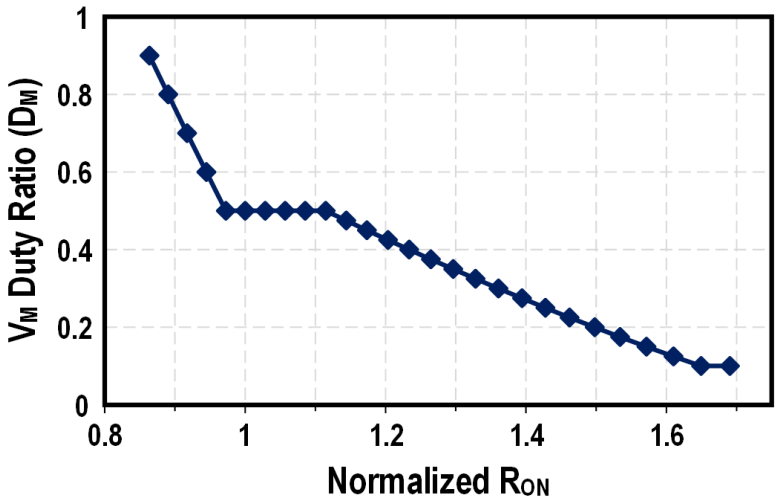


Figure 5.27. Active thermal control through D_M modulation.

5.5 Summary

In this chapter, an on-chip self-calibrated full-profile dynamic r_{on} sensing strategy for online condition monitoring of GaN-based power converter has been introduced, discussed and verified. The fully integrated tri-state dynamic r_{on} sensors are implemented in half-bridge buck converter. Thanks to the proposed strategy, dynamic r_{on} sensing errors are calibrated inherently, minimizing area and power overheads of the power converter. Meanwhile, the ET M_L reverse r_{on} sensor enables accurate negative switching node voltage sensing with short t_{dead}, without compromising efficiency. In addition, the dual-rail up-level shifter improves the GaN driving reliability by overcoming large negative switching node voltage during t_{dead} challenge. The experimental results successfully validate the proposed techniques and circuits in this design.

CHAPTER 6

MONOLITHIC INTEGRATION OF GAN DC-DC CONVERSION

With regard to Section 1.2.4, traditional discrete GaN-based power conversion implementations heavily rely on board- and package-level wiring and bonding to connect GaN transistors, power passives, gate drivers, level shifters, controllers and auxiliary modules, introducing substantial resistive and inductive parasitics. The situation deteriorates drastically under current industry trends towards high power density and high f_{SW}, where the adverse impacts of the parasitics grow rapidly against efficiency, reliability and performance. To unlock the potential of GaN technology, the ideal and ultimate solution is to achieve monolithic circuit integration, which can significantly reduce parasitics, save area cost, improve implementation flexibility, and enhance reliability. This chapter presents a monolithic integrated GaN AHB switching power converter for 48V/1V power conversion. Firstly, Section 6.1 introduces monolithic GaN power circuits. Then, the challenges of monolithic GaN power converter integrations are discussed in Section 6.2. Furthermore, Section 6.3 presents the monolithic integrated GaN AHB switching power converter, followed by implementations of A^2 up-level shifting, SBH gate driving, on-die temperature sensing and on-die t_{dead} control techniques. Section 6.4 verifies the proposed design with experimental results. Finally, a summary of this chapter is given in Section 6.5.

6.1 Introduction of Monolithic GaN Power Circuits

6.1.1 GaN Technology Process

GaN power ICs are treated as potential next-generation power conversions. In 2009, [Wong-09] presents a basic GaN technology, including d-mode, e-mode GaN HEMTs, Schottky

diodes, power HEMTs, and power rectifiers. Since then, a series of circuit blocks are developed based on the GaN technology, including comparator, temperature sensor, sawtooth generator and PWM controller for closed-loop control of power converters [Liu-11, Kwan-13, Wang-14]. [Risbud-16] reports a cell library in a monolithic GaN process, including current source, comparator, bias, logic and reference circuities. Meanwhile, multiple GaN power devices are also designed on one chip. In [Uemoto-09], a three-phase GaN inverter for the motor drive is fabricated on the GaN process and these GaN power switches are driven by discrete driving circuits. But the parasitics on the driving paths between GaN HEMTs and driving circuits limit the driving stability and reliability. To reduce non-ideal parasitics and improve implementation flexibility, monolithic GaN integration becomes promising. In [Ujita-14], one LV asymmetric synchronous buck circuit for point of load converter is reported. It incorporates high- and low-side power switches and gate driving circuits on one GaN chip. But its gate driving circuits consume large power. In [Sepahvand-16], a monolithic GaN buck converter with d-mode GaN HEMTs operates up to 100MHz. However, due to the negative threshold voltage of d-mode GaN devices, multiple power supplies are used to supply the power for gate driving circuits, increasing the implementation complexity. As an alternative way, the hybrid integration with chip-on-chip bonding is developed for monolithic power IC integration in [Lerner-16]. The GaN transistors are selected from GaN wafer, and the control and driving circuits are fabricated with CMOS process. With the specific stamps, the GaN power transistors are transferred and released on the targeted CMOS IC chip. The heterogeneous integration of GaN and BCD technology is also demonstrated by co-designing the BCD circuits and GaN devices [Aklimi-17, Meng-19]. After designing the control and driving circuits with a mature BCD process, one extra under-bump metallization (UBM) layer is designed

on the BCD wafer. The GaN power devices are directly mounted on the BCD circuits. On the other hand, [Liu-18] employs integrated passive devices (IPD) technology. The power converter is heterogeneously integrated with gate driver, GaN HEMTs, planar inductor and metal-insulator-metal capacitors on IPD substrate.

6.1.2 GaN Half-Bridge Power Converters

In power electronic circuits, the synchronous half-bridge power stage is widely used in multiple power conversion systems, for example, synchronous buck and boost converters, AHB converters, active clamped forward (ACF) converters, full-bridge converters, LLC resonant converters, class D switching audio amplifiers, and motor drive inverters, etc. Ideally, with one PWM control signal V_{PWM} and adjustable t_{dead} controller, high- and low-side power switches in the half-bridge power stage are switched periodically. To realize the power stages of GaN half-bridge power converters, there are several different implementation approaches. [Song-15, Chen-19, Yan-19, Ke-21] employ discrete GaN power devices and silicon driving circuits, which mainly include gate drivers, level shifter (LVSF) and t_{dead} controller. As shown in Figure 6.1, on the PCB, two GaN power switches and driving circuits are connected through PCB wirings, building a GaN-based half-bridge power stage. However, such a solution suffers from complicated PCB designs, and these discrete components exacerbate area cost. To reduce the PCB complexity and non-ideal parasitics, the integrated GaN half-bridge power stage is proposed in Figure 6.2 [Reusch-15]. With the progress of GaN technology, high- and low-side GaN power switches can be integrated on one chip. Thus, the number of discrete components on PCB is reduced. Whereas, targeting on high f_{SW} and low switching loss, the driving currents of gate driving signals V_{GH} and V_{GL} should be high enough to minimize the turn-on or -off transitions of GaN power switches. But V_{GH} and V_{GL} have

to pass through bonding wires in the package and PCB wirings, which contain inductive and resistive parasitics. These parasitics would limit the driving speed and lead to large ringing spikes of driving signals, challenging driving reliabilities. They are becoming the bottleneck for high f_{SW} and high reliability GaN power converters. Although these discrete GaN HEMTs provide extra Calvin connection pins for the driving circuits, the non-ideal parasitics still constrain their switching performance.

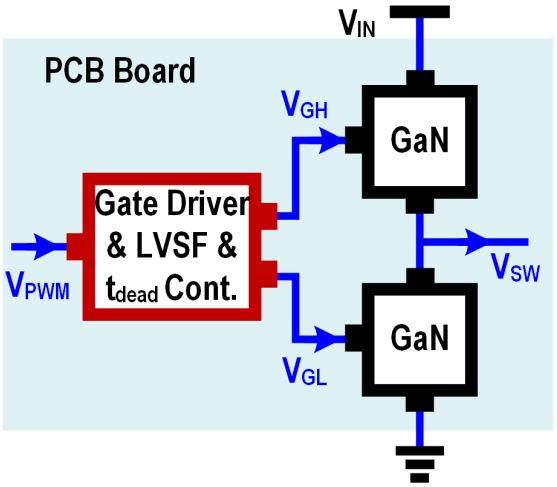


Figure 6.1. GaN half-bridge power stage with discrete GaN power switches and silicon driving circuits.

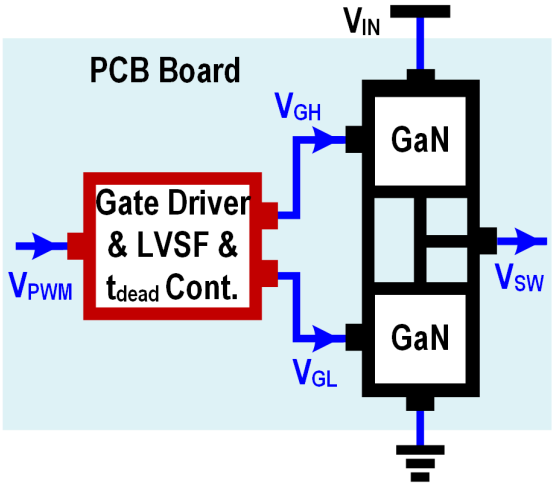
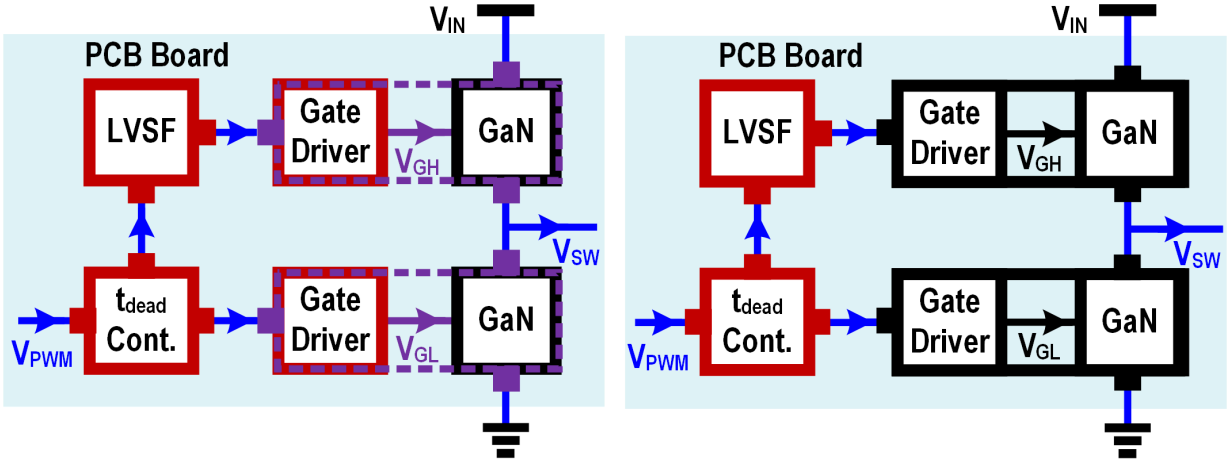


Figure 6.2. GaN half-bridge power stage with integrated GaN power switches and silicon driving circuits.



(a) (b)

Figure 6.3. GaN half-bridge power stage: (a) co-packaged GaN power switch and silicon gate driver, (b) integrated GaN power switch and GaN gate driver.

To minimize the parasitics on gate driving paths, Figure 6.3 illustrates that the GaN power switch and its gate driver are either packaged or integrated as one chip with different approaches. In Figure 6.3(a), [TI-21] uses the co-packaging technique, in which the GaN power switch and the silicon gate driver are connected through internal bonding wires and packaged as one chip. Thanks to the mature BCD process, a robust and multi-functional gate driver is developed to control the switching of GaN power switch. But the extra co-packaging process increases the total system cost. Furthermore, the high driving current has to pass through the internal bonding wires, the parasitics on which would still affect the driving performance. On the other hand, Figure 6.3(b) shows that the GaN power switch and its gate driver are integrated on one GaN chip, which is employed in [Navitas-20]. With a monolithic GaN technology process, the power switch and the gate driver are connected by the internal metal. By eliminating bonding wires and PCB wirings in the driving loop, the GaN power device can be switched with a faster rate and higher reliability. However, since the GaN process is less mature than the classic Si BCD process. It only provides limited device options with only n-type GaN HEMTs. The lack of a complementary p-type GaN

device makes reliable and efficient gate driving design challenging, especially in optimizing the driving strength, reliability and power loss.

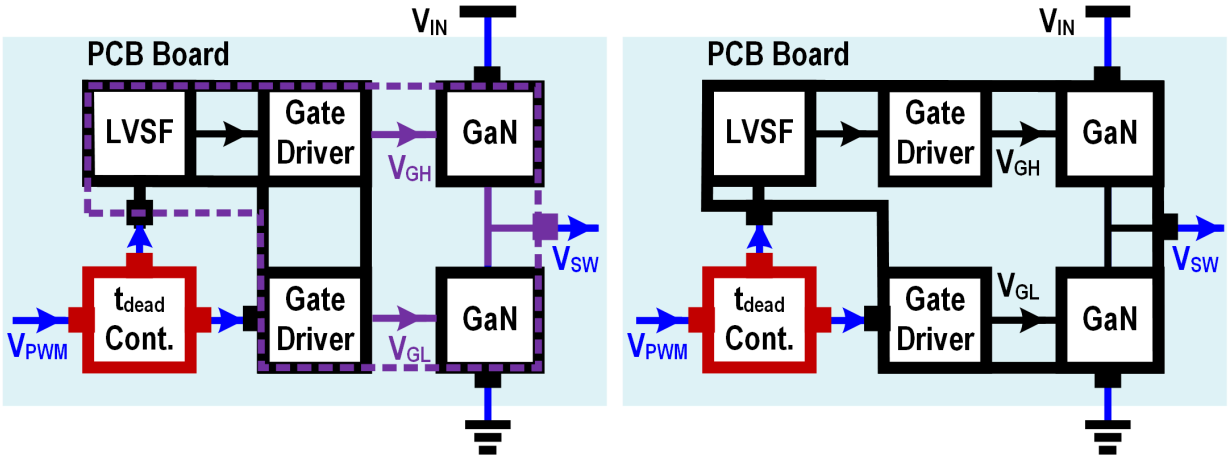


Figure 6.4. GaN half-bridge power stage: (a) co-packaged GaN power switches, silicon gate driver and level shifter, (b) integrated GaN power switches, GaN gate driver and level shifter.

In the above approaches, although the driving performance is improved by incorporating the gate driver and GaN power switch, implementing the half-bridge power stage is still complicated. On the PCB, the two discrete GaN power switches with gate driver, level shifter and t_{dead} controller consume much large area, which is detrimental to power density and system flexibility. In Figure 6.4(a), the level shifter and gate drivers are integrated by BCD process and the bare die is co-packaged with two GaN power switches [TI-18, ST-20]. Similarly, the commercial product NV6252 from Navitas co-packages two GaN modules, which include one GaN power switch and its gate driver on one GaN chip, building a GaN half-bridge power stage [Navitas-18]. In order to minimize the parasitics induced by bonding wires on the driving paths, [EPC-21] proposes an integrated half-bridge power stage in Figure 6.4(b), which incorporates level shifter, gate drivers and power switches on one GaN chip. But it suffers from large area cost and high static power loss, compromising the merits of GaN technology. In addition, it requires two

separated input signals to control high- and low-side GaN power switches separately, and one extra t_{dead} control chip is necessary. Overall, two discrete chips are needed to be soldered on the PCB for the half-bridge power converter.

6.1.3 Introduction of Monolithic GaN Process

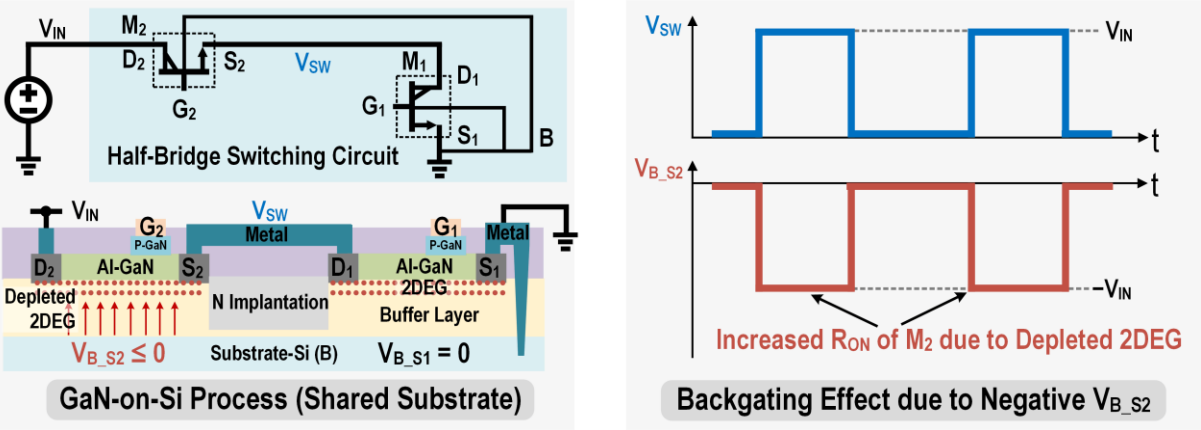


Figure 6.5. Challenges on monolithic integration of power converters with GaN-on-Si process.

In classic implementations of GaN half-bridge power converters with discrete components, the substrates of high- and low-side GaN HEMTs are independent. The substrate is tied to the source of each GaN power switch inherently. However, if the half-bridge power stage is integrated with the GaN-on-Si process in Figure 6.5, the integrated high- and low-side power switches share a common conductive substrate. The switching operations on the conductive silicon substrate would cause static and dynamic electrical field-related degradation effects [Moench-21]. Firstly, the switching operations of HV GaN devices will exert crosstalk voltage or current signals on LV devices, affecting the operation points of controlling and driving circuits, and inducing potential disturbances and false operations [Jiang-14]. Besides, in a switching power converter, the sources of all GaN devices are not connected together. Due to the shared substrate, connecting a substrate to source is not feasible for each GaN device. The voltage difference between substrate and source

of a GaN device is detrimental to its performance. For example, the substrate (B) of the chip is connected to the ground in Figure 6.5. The substrate source voltage difference of M_1 is constantly zero, while the substrate source voltage difference of M_2 (V_{B_S2}) changes during the switching operation. When M_2 is turned on, the switching node voltage V_{SW} rises to V_{IN}. V_{B_S2} decreases from zero to $-V_{IN}$. The back-gating effect, that the negative V_{B_S2} modulates the 2DEG-channel conductivity and increases the on-resistance of M_2 greatly, deteriorates the performance of GaN device severely [Li-18b].

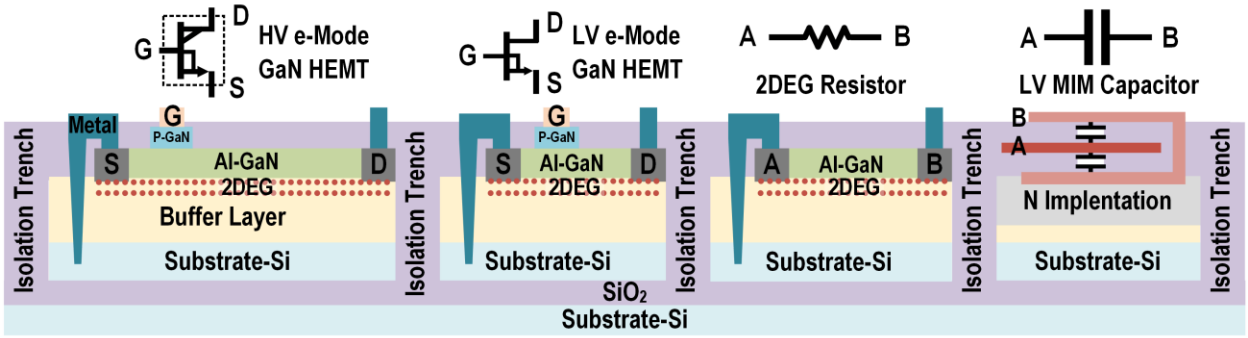


Figure 6.6. Schematic and process cross-sections of the GaN IC components on the GaN-on-SOI process.

Compared to the GaN-on-Si process, the GaN-on-SOI process in Figure 6.6 can maintain the merits of GaN technology and isolate the substates of each GaN device with isolation trenches [Li-19]. It uses one additional layer to isolate the individual substrate from the main silicon substrate, achieving full dielectric isolation. With a buried oxide under the active die and trench isolations on the sides, the substrate of each device can be isolated effectively. Thereby, local source-to-substrate termination is allowed, and the substrates of high- and low-side power switches can be connected to the sources of high- and low-side power switches, respectively [Wei-21]. The crosstalk and back-gating effects are thus overcome, enabling monolithic integration of multiple GaN power devices. Besides, owing to the elimination of latch-up risk, high temperature and high

voltage operation, and low leakage current, the SOI process becomes promising for planar GaN HEMTs integration. However, in the GaN-on-SOI process, only four types of devices are available, namely HV e-mode GaN HEMT, LV e-mode GaN HEMT, 2DEG resistor and LV metal-insulator-metal (MIM) capacitor. The lack of d-mode GaN HEMTs and compatible p-type devices induces more design challenges of monolithic GaN power circuits. Furthermore, the monolithic GaN integration level is also constrained by the design kits' low maturity and limited kinds of GaN HEMT voltage ratings [Jiang-21].

6.2 Monolithic GaN Power Converter Integration

6.2.1 Monolithic GaN Half-Bridge Power Converters

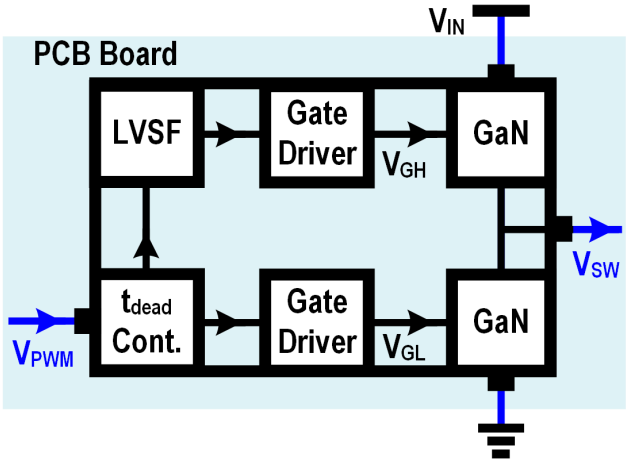


Figure 6.7. Illustration of monolithic GaN half-bridge power stage.

In the above prior arts of GaN half-bridge power stage, there are several signs of progress for higher integration level of GaN power circuits. However, further improvements can be made with much more efficient and compact integration to fully exploit the advantages of GaN technology. As shown in Figure 6.7, in a monolithic integrated GaN half-bridge power stage, GaN power switches, gate drivers, level shifter, and t_{dead} controller are fully integrated on one single

GaN chip. It can reduce parasitics with high implementation flexibility. Besides, the discrete component counts, design time, PCB area and total cost can be thus saved substantially. Additional functionalities, such as temperature sensing and thermal protection, can enable the cost savings and performance improvements possibilities with this type of IC.

6.2.2 Design Challenges of Monolithic GaN Level Shifting

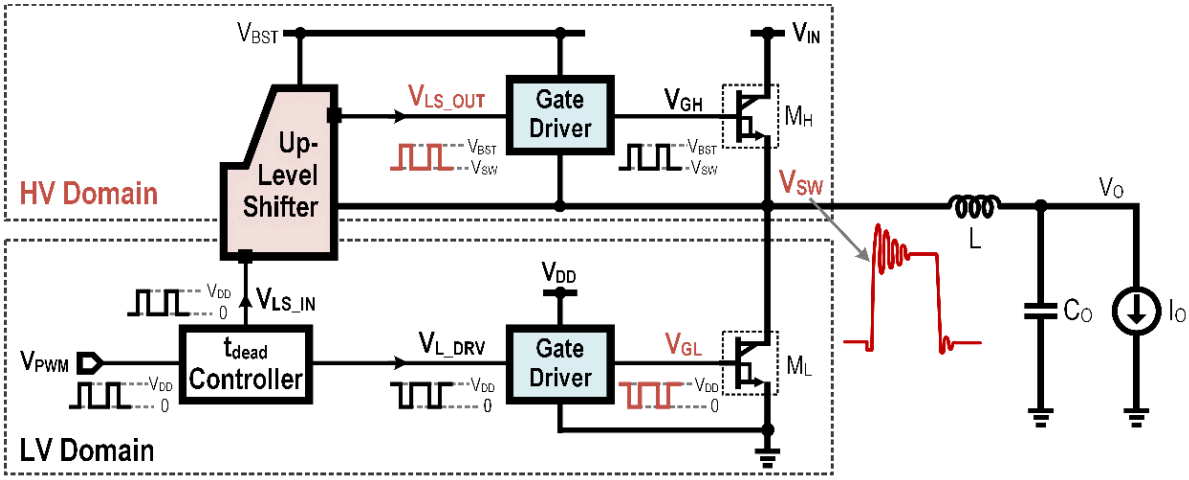


Figure 6.8. Illustration of synchronous half-bridge power converter.

When implementing the synchronous half-bridge power converter in Figure 6.8, there are several design challenges on level shifting and gate driving due to the immature GaN-on-SOI process. Without p-type transistors, key modules such as level shifters and gate drivers would lose effective pull-up mechanisms towards high voltage nodes such as supply voltages, causing potential control malfunction, long propagation delay, high conduction loss and high reliability risk. This largely accounts for today's very limited GaN power ICs in the commercial market, with only the simplest open-loop half-bridge converter being reported.

For any intermediate- and high-voltage power circuits, up-level shifters are essential to translate one LV PWM control signal V_{PWM} into HV domain. Due to the absence of p-type devices,

the pull-up circuit of a level shifter often has to be implemented with on-die resistor(s). The dilemma is that such a resistive pull-up circuit must present a high resistance to reduce quiescent current, when the pull-down n-type GaN switch is on to transmit a "0". However, the same pull-up circuit has to be low resistive to transmit a "1" control signal effectively to the HV circuit domain. The conflicting requirements suggest compromised performance on chip area, power consumption and level shifter delay, which are confirmed by large power and chip area consumption reported in [EPC-21, Navitas-18]. More seriously, as the interface to HV domain, a level shifter continuously faces risks of disastrous breakdown and false triggering. As shown in Figure 6.9, the HV switching node V_{SW} often sees high dynamic dv/dt changes, spikes and ringing effects due to the nature of a switching converter. For a Si CMOS level shifter, HV clamping diodes (D_{CLP}) and latch circuits using complementary devices can be employed to block the HV interference and prevent false triggering. Without p-type transistors and power diodes in GaN process, up-level shifting gets very challenging. Consequently, without up-level shifter, it makes driving high-side GaN power switches impossible. Hence, even very recent research works integrate only low-side n-type GaN transistor and its gate driver.

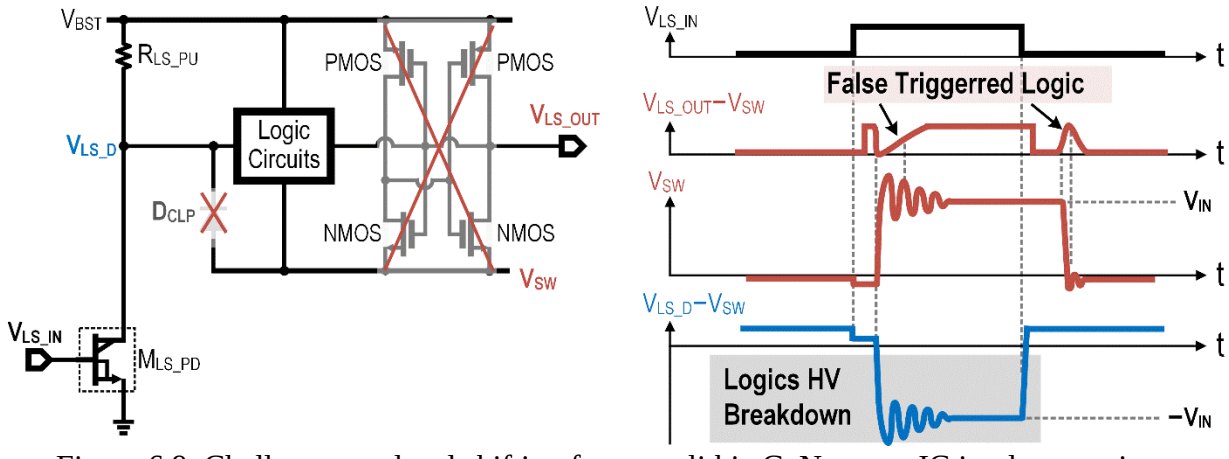


Figure 6.9. Challenges on level shifting for monolithic GaN power IC implementations.

6.2.3 Design Challenges of Monolithic GaN Gate Driving

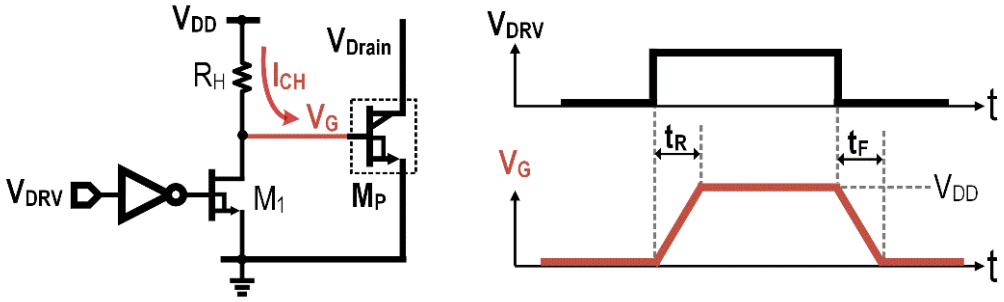


Figure 6.10. The monolithic final gate driving stage with LV GaN HEMT and 2DEG resistor.

On the other hand, regardless of driving high- or low-side GaN switches, classic CMOS gate driving circuits are no longer applicable in the GaN-on-SOI process. Without a complementary p-type transistor, there are new design challenges of designing efficient, fast, and reliable gate driver with the monolithic GaN process. The power device M_P must be fully turned on and off and its gate driving voltage should swing rail-to-rail for the sake of efficiency and speed. In the monolithic GaN driver [Ujita-14, Liang-19], both d-mode GaN HEMTs and e-mode GaN HEMTs are employed in the driver. However, the GaN-on-SOI process lacks d-mode GaN device, and only e-mode GaN HEMT and 2DEG resistor are available for the driver circuit. In Figure 6.10, the LV GaN HEMT M_1 is used to turn off M_P by pulling down its gate driving signal V_G to ground. When M_1 is off, the current through 2DEG resistor R_H charges the gate capacitor of M_P. V_G rises high to turn on M_P. To achieve high f_{SW} and low power loss, the rising and falling time (t_R and t_F) of V_G need to be as small as possible. R_H should be small enough for a high charge current I_{CH} and a short t_R. But the small R_H would contradict t_F reduction and induce high static power. When turning off M_P, the discharging current through M_1 should be several times higher than I_{CH} to keep a short t_F. Due to the small R_H, a large static DC current will flow through R_H and M_1. The generated tens of milliamps current from the V_{DD} to the ground induces high static power loss.

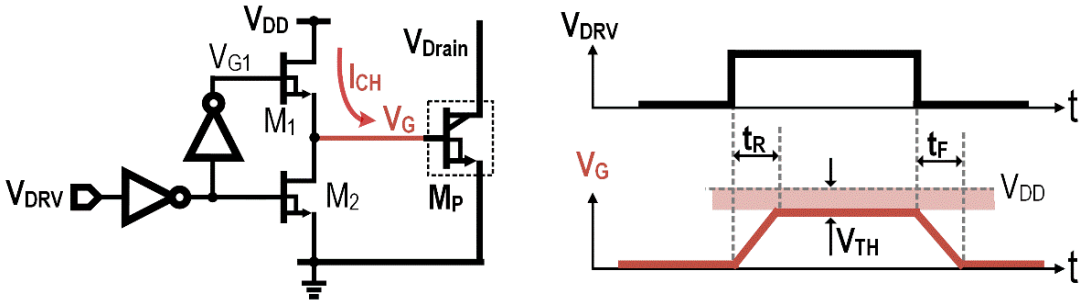


Figure 6.11. The monolithic final gate driving stage with two LV GaN HEMTs.

To reduce the power loss induced by the pull-up resistor, the gate driving circuits can be realized with all LV GaN HEMTs (M_1 and M_2) in Figure 6.11. M_1 is used to turn on M_P and M_2 is employed to turn off M_P. Since M_1 and M_2 are not turned on at the same time, high static current thus is eliminated for low power loss in the gate driver. However, because of the positive threshold voltage (V_{TH}) of the e-mode GaN HEMT M_1, the maximum gate driving voltage V_G will be degraded by V_{TH}. Note that the V_{TH} of a GaN transistor is usually several times bigger than of a comparable Si MOSFET. Hence, the resulting gate drive voltage drop can lead to partial turn-on of M_P, increasing on-resistance and conduction loss of M_P substantially.

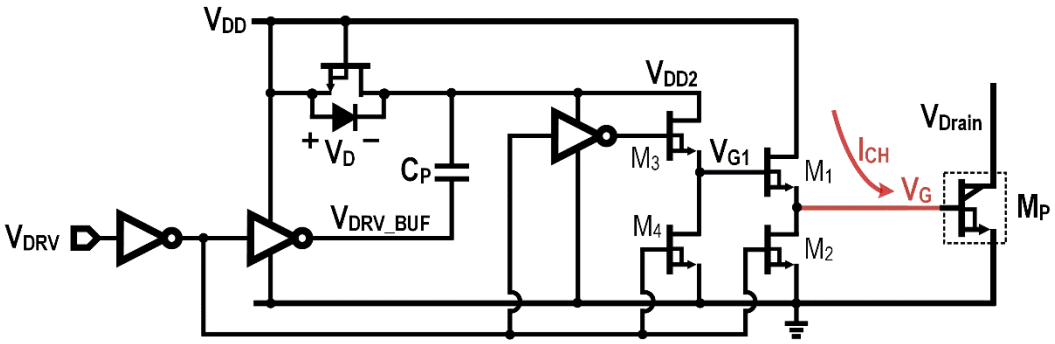


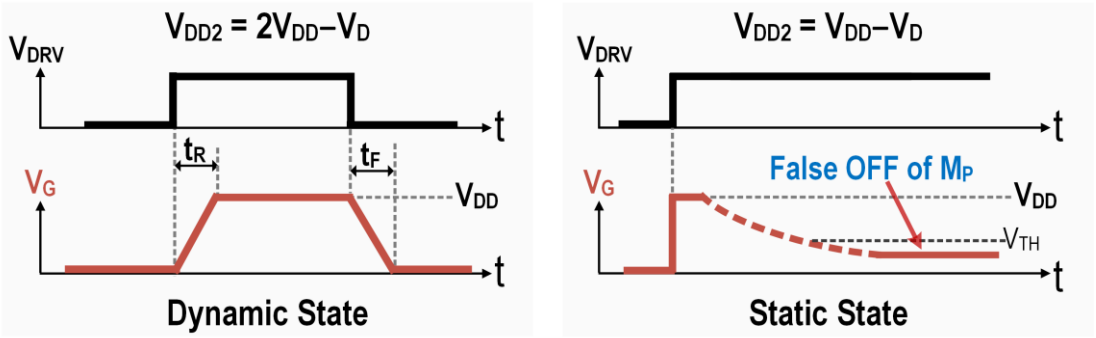
Figure 6.12. Circuit schematic of monolithic final gate driving stage with LV GaN HEMTs and bootstrapped circuits.

To fully turn on M_P, [Tang-18] uses two separated power supplies. One high voltage power source is adopted to supply the gate driving of M_1, and its positive threshold voltage V_{TH} effect can thus be compensated. However, the two external power sources increase implementation

complexity. In [Kaufmann-20, Chen-20], one integrated charge pump circuit with the driving circuits is presented, which boosts V_G when M_P is turned on. As shown in Figure 6.12, the body diode of GaN HEMT and pump capacitor C_P compose charge pump circuits. When the driving signal V_{DRV} is low, M_2 is turned on to pull V_G ground and keep M_P off. Meanwhile, V_{DRV_BUF} is zero and C_P is charged up by V_{DD}. When V_{DR} rises high, V_{DRV_BUF} becomes V_{DD} and V_{DD2} is boosted, and it equals

$$V_{DD2} = 2V_{DD} - V_D. \tag{6.1}$$

Here, V_D is the voltage drop across the body diode. Owing to the high V_{DD2}, V_G is charged to V_{DD}, and M_P is fully turned on, which is shown in Figure 6.13(a).



(a) (b)

Figure 6.13. Key operation waveforms in (a) dynamic switching control, and (b) static DC control.

However, such charge pump circuits are only appliable for a switching circuit, in which occasion M_P is continuously switched between on and off states. Without a recharge mechanism, on-die C_P can be deeply discharged by large gate leakage, causing catastrophic switch false-off. As shown in Figure 6.13(b), when M_P is kept on for a long period of time during start-up or load transients, the large leakage currents of GaN devices would discharge C_P. The body diode in the charge pump circuit would adversely decrease V_{DD2}. The large threshold voltage drops of M_1 and M_3 further counter the voltage boosting effort by the charge pump, falsely turning off M_P.

6.2.4 Monolithic GaN Thermal Protection

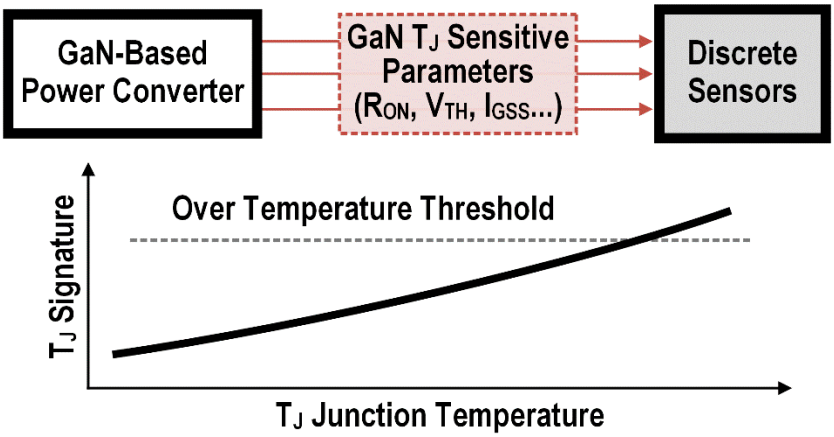


Figure 6.14. Thermal protection in monolithic GaN power converters.

Apart from level shifting and gate driving challenges, thermal effect is crucial in GaN power ICs, which operate at high power density. In a power converter, the self-heating effects are related to the rapid rise of die temperature of GaN HEMTs, posing serious reliability risks on the power conversion during operation. To mitigate the reliability risks, it would be highly desirable to facilitate on-die temperature sensing for hot spot monitoring and thermal protection. Once the on-die temperature exceeds the safe threshold value, protection actions are enabled to protect the GaN HEMTs from overheated breakdown. However, the commercially available GaN devices are discrete components without specialized temperature sensors. To monitor the real-time temperature of GaN HEMTs, the straightforward way is to use an infrared camera. But such bulky equipment introduces more implementation complexity. Another way is to capture the key electrical parameters of GaN HEMTs, which are affected by different junction temperature (T_J). As shown in Figure 6.14, GaN HEMTs temperature sensitive parameters, such as on-resistance, threshold voltage and gate leakage current, are used as T_J signatures and sensed by discrete sensors [Chen-21]. However, this can be very impractical for power converters since the sensing schemes

would disturb the normal operation of power converters occasionally. Besides, the low sensing accuracy is highly affected by the correlations between T_J signature and T_J, and the required multiple chips increase system cost.

6.3 Proposed Monolithic GaN AHB DC-DC Power Converter

6.3.1 System Architecture and Operation Scheme of AHB Power Converter

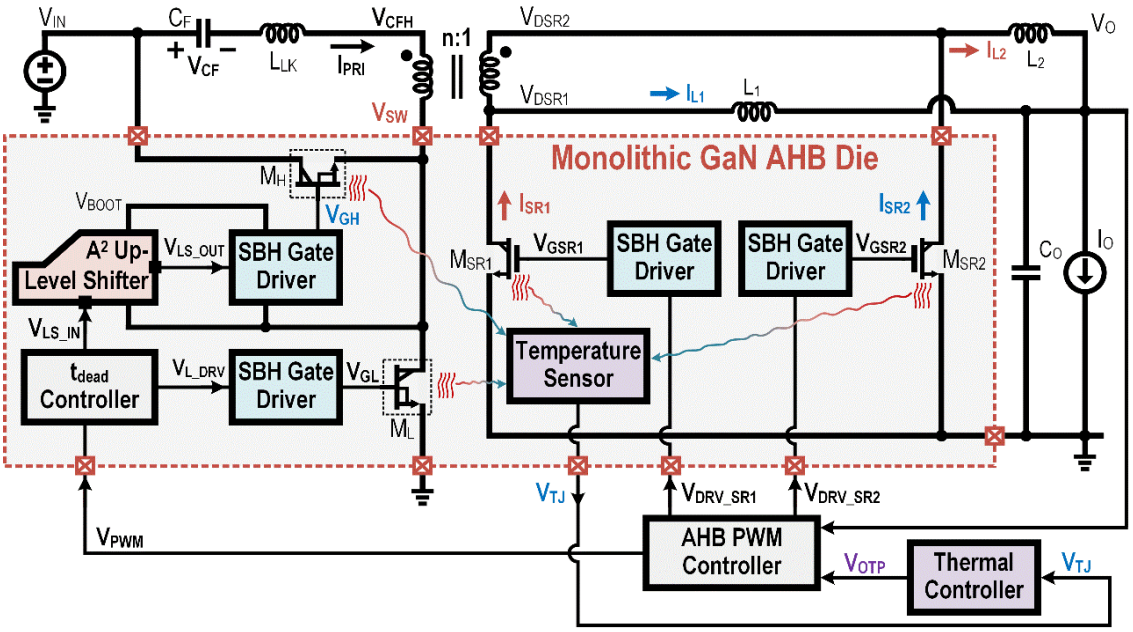


Figure 6.15. Block diagram of proposed monolithic GaN AHB power converter.

To address the aforementioned concerns, a monolithic GaN AHB power converter is proposed, achieving direct 48V/1V DC-DC power conversion in a GaN-on-SOI process. As illustrated in Figure 6.15, the design features the following highlights: 1) A^2 up-level shifting technique and circuit to address the challenges of pull-up performance, device breakdown risk and dv/dt immunity at V_{SW}, 2) SBH gate driving technique and circuit to adaptively achieve rail-to-rail dynamic gate driving in normal operation and robust static gate driving during large transients, 3) on-die temperature sensing to facilitate hot spot monitoring and thermal management, and 4) on-

die t_{dead} control to enable ZVS operation. Thanks to the proposed A^2 up-level shifting and SBH gate driving, it allows the chip integration effort to go beyond basic converter topology and effectively operate more sophisticated architectures that address currently most pressing technical challenges. Accordingly, the design highlights are demonstrated in an advanced AHB conversion topology, requiring one high-side and three low-side GaN power switches, up-level shifter and four gate drivers. Compared to the half-bridge buck topology, the AHB converter presents a much balanced 2-phase current delivery and requires a relaxed minimum on-duty time which is critical to the 48V/1V power delivery. On the primary side, two HV GaN power switches are softly switched. On the secondary side, the current doubler is used to achieve low output voltage and high output current. The synchronous rectifiers with two LV GaN HEMTs replace passive diodes to reduce conduction power loss for high efficiency.

The timing diagrams of the monolithic GaN AHB converter are illustrated in Figure 6.16. With the three digital control PWM signals V_{PWM}, V_{DRV_SR1}, V_{DRV_SR2} from feedback controller, the primary and secondary power switches are switched complementary by the integrated driving circuits. In steady state, when the gate driving signal V_{GL} turns on M_L during the duty ratio D, the switching node voltage V_{SW} falls zero. The flying capacitor C_F is charged by a positive primary current I_{PRI}. Meanwhile, M_{SR1} of the secondary side is also turned on to conduct a rising inductor current I_{L2} and a falling inductor current I_{L1}. When the gate driving signal V_{GH} turns on M_H during the duty ratio $(1-D)$, V_{SW} rises to V_{IN} and C_F is discharged by the negative I_{PRI}. According to the voltage-second balance of the transformer primary magnetizing inductance, the following is obtained:

$$(V_{IN} - V_{CF}) \times D = V_{CF} \times (1 - D). \tag{6.2}$$

Thus, in steady state, the stable voltage across C_F, V_{CF} equals

$$V_{CF} = D \times V_{IN}. \tag{6.3}$$

Considering the voltage-second balance of output inductor L_1 and L_2 respectively,

$$(\frac{V_{IN}-V_{CF}}{n} - V_O) \times D = V_O \times (1-D). \tag{6.4}$$

Here, n represents the transformer turns ratio. After simplifying equation (6.4),

$$V_O = D \times (1-D) \times V_{IN}/n. \tag{6.5}$$

It shows that the turns ratio n contributes to a high V_{IN}/V_O conversion. The product of D and $(1-D)$ increases the conversion ratio further.

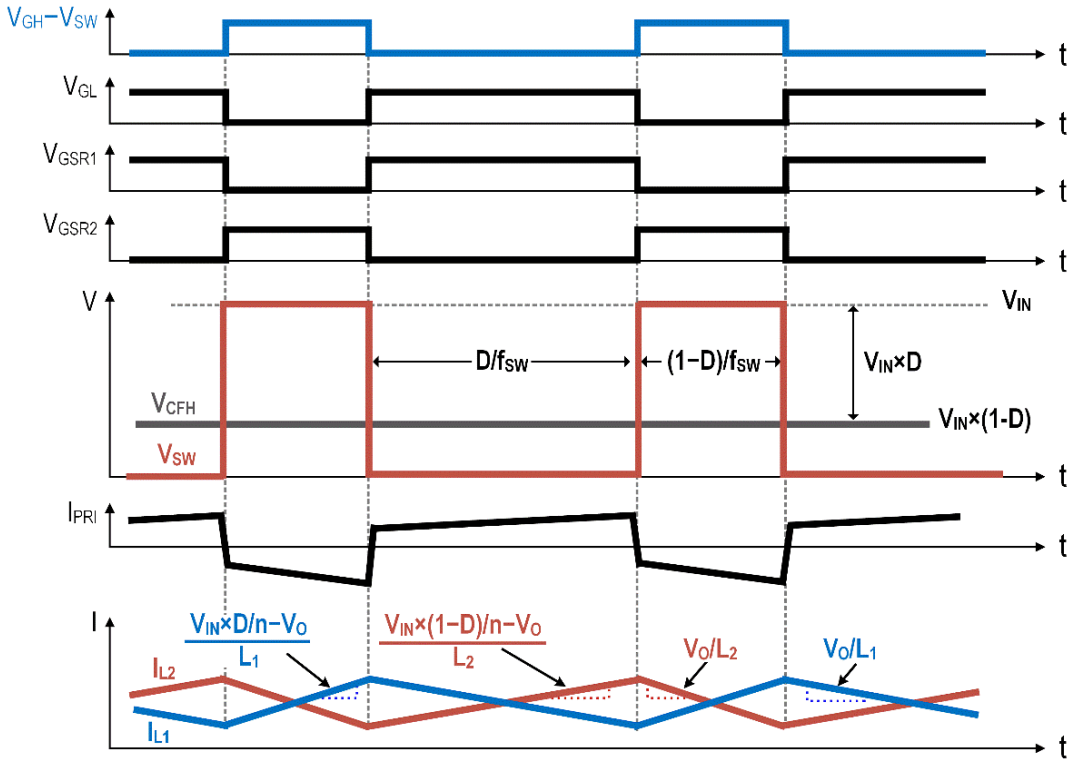


Figure 6.16. Operation timing diagrams of proposed monolithic GaN AHB power converter.

During switching operations, V_{SW} switches between zero and V_{IN}, and the voltage stress of primary devices M_H and M_L equals V_{IN}. When V_{SW} switches to V_{IN}, the voltage across the primary

inductance equals $D \times V_{IN}$. M_{SR2} is turned on and the secondary-side inductance operates as an equivalent current source to support the power for L_1. Meanwhile, I_{L2} decreases with a rate of V_O/L_2. The voltage stress for the off-state M_{SR1} is

$$V_{DS\_MSR1} = D \times V_{IN}/n. \tag{6.6}$$

Similarly, when V_{SW} switches to zero, the voltage across the primary inductance equals $(1-D) \times V_{IN}$, and the voltage stress for the off-state M_{SR2} is

$$V_{DS\_MSR2} = (1 - D) \times V_{IN}/n. \tag{6.7}$$

Due to the complementary ripples of I_{L1} and I_{L2}, the output voltage V_O ripple is compensated significantly, allowing a small output capacitor. According to equations (6.6) and (6.7), the voltage stresses of M_{SR1} and M_{SR2} are much smaller owing to the employment of the transformer. But their values are correlated to the duty ratio D, which is a major drawback of the AHB converter. In this work, because of the low V_O, LV GaN devices can sustain the voltage rating of M_{SR1} and M_{SR2} in a wide duty ratio range. On the other hand, by utilizing the leakage inductance L_{LK} of the transformer, the AHB converter achieves inherent soft switching on primary switches, eliminating switching loss greatly.

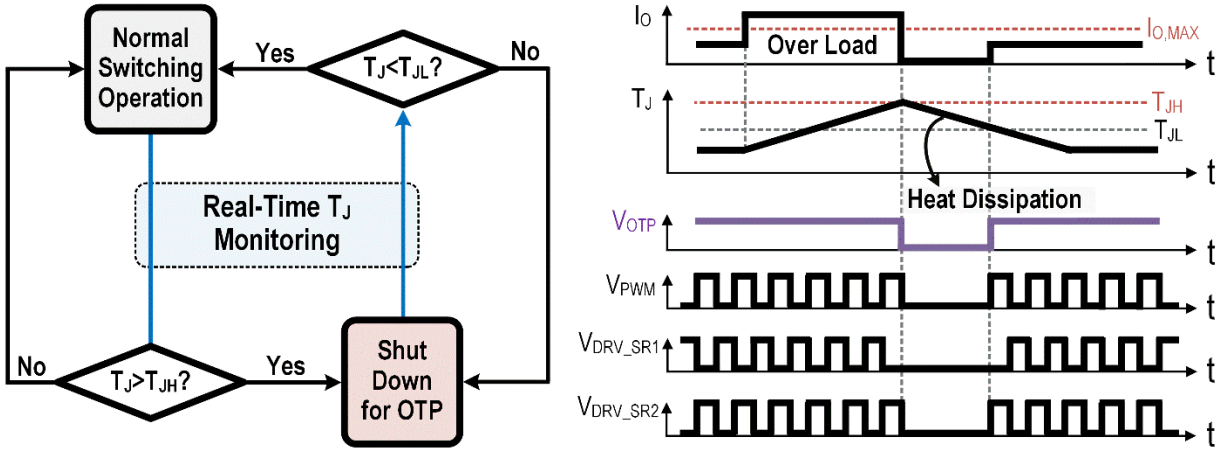


Figure 6.17. Thermal protection scheme of proposed GaN AHB power converter.

On the other hand, the on-die temperature sensor monitors hot spots and facilitates thermal protection of the monolithic GaN AHB power converter. Figure 6.17 presents the thermal protection scheme of the proposed converter. Thanks to the proposed on-die temperature sensor, its readout signal V_{TJ}, retains one-to-one mapping to instant on-die temperature T_J. It is actively fed into a thermal controller. If an overload event occurs, which elevates T_J beyond its safety temperature limit T_{JH}, the output signal of thermal controller V_{OTP} would change to logic low, and the converter would be shut down to dissipate excessive heat for over temperature protection (OTP). After a period of power dissipation, it resumes normal operation until T_J falls below the hysteretic threshold T_{JL}.

6.3.2 Monolithic GaN A^2 Up-Level Shifting

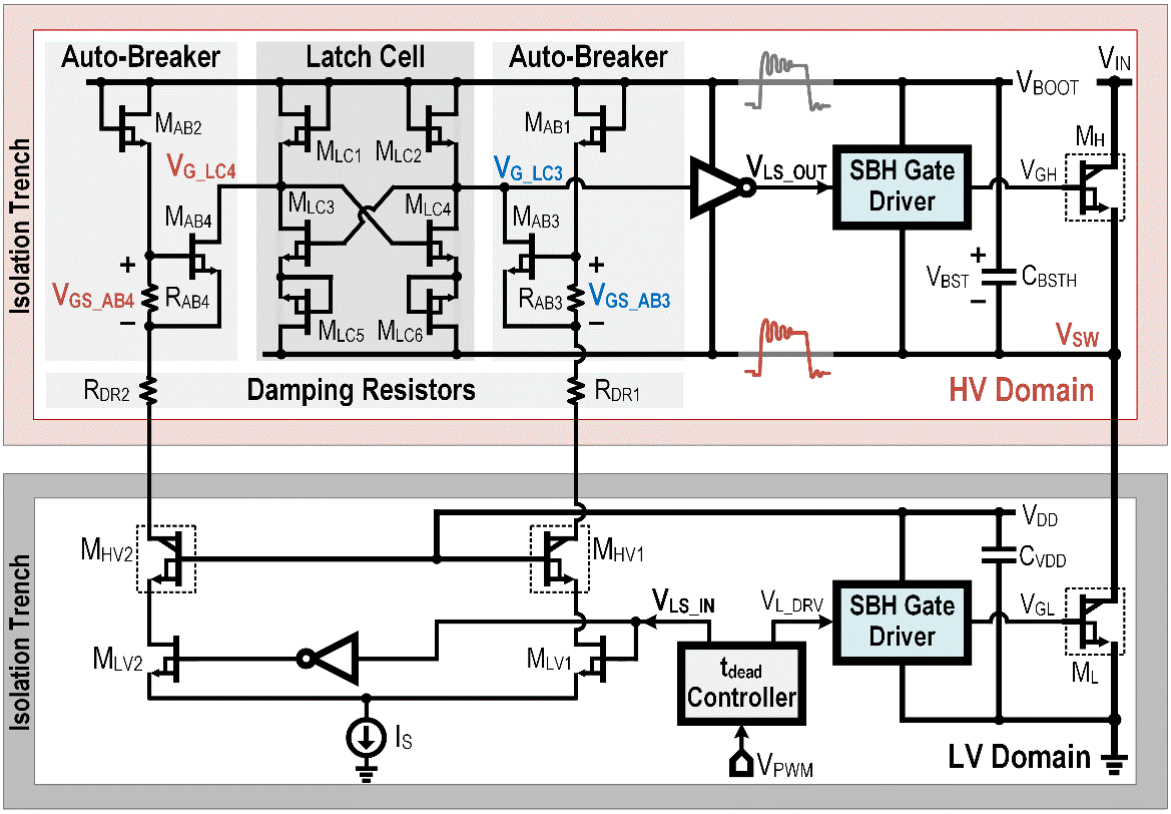


Figure 6.18. Circuit schematic of proposed A^2 up-level shifting technique.

To fully take advantage of GaN process, Figure 6.18 illustrates the circuit schematic of the proposed A^2 up-level shifting technique. The nature of level shifting circuit divides the circuit into HV and LV domains, which are physically isolated by isolation trenches in the GaN-on-SOI process. Two HV e-mode GaN HEMTs M_{HV1} and M_{HV2} isolate two voltage domains and transmit driving signals. The gates of M_{HV1} and M_{HV2} are biased by the low voltage supply voltage V_{DD}. The auto-breakers and latch cell ensure fast and reliable level shifting with low power loss. Two damping resistors R_{DR1} and R_{DR2} are inserted between the drains of HV GaN HEMTs and HV domain to filter non-ideal coupled voltage glitches for high reliability.

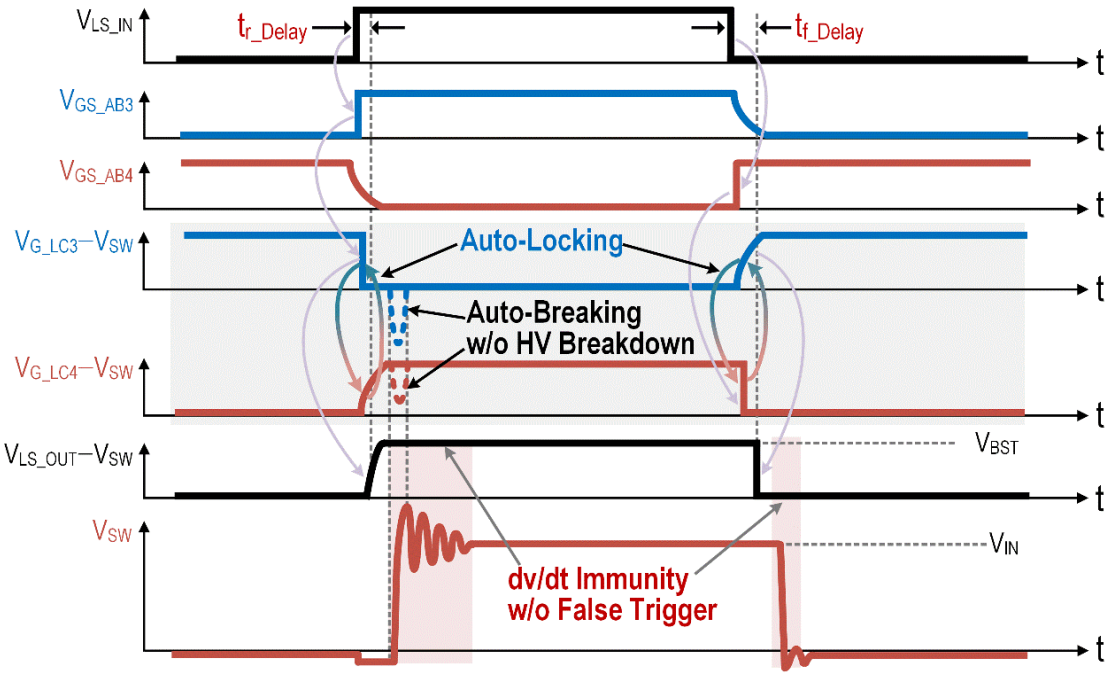


Figure 6.19. Operation waveforms of proposed A^2 up-level shifting technique.

The operation waveforms of the proposed A^2 up-level shifting technique are presented in Figure 6.19. When the input voltage of the up-level shifter V_{LS_IN} rises from low to high, M_{LV1} turns on and M_{LV2} switches off. The tail current I_S is fully steered through M_{LV1} and M_{HV1}, generating an instant high V_{GS_AB3} across R_{AB3}. M_{AB3} is thus turned on, pulling V_{G_LC3} down to turn off M_{LC3}.

Meanwhile, M_{LC4} is quickly turned on by high V_{G_LC4}. The latch cell consisting of transistors M_{LC1}-M_{LC6} automatically locks V_{LS_OUT} into steady state using a positive feedback mechanism, facilitating reinforced pulling strength with high speed and blocking V_{SW} spikes and ringing from causing false triggering. As a result, the up-level shifter output voltage V_{LS_OUT} shifts from V_{SW} to V_{BST}+V_{SW}, achieving fast up-level shifting without p-type transistors. Similarly, a complementary operation takes place when V_{LS_IN} falls to zero, with V_{LS_OUT} returning to V_{SW}. To avoid false triggering events and transmit the driving signal robustly, two auto-breakers are built with LV GaN transistors M_{AB1}-M_{AB4}, and R_{AB3} and R_{AB4}. The breakers automatically break the nodes V_{G_LC3} and V_{G_LC4} from falling below V_{SW}, protecting GaN devices from breakdowns caused by HV spikes at V_{SW}. Two damping resistors R_{DR1} and R_{DR2} further mitigate non-ideal effects induced by V_{SW} dv/dt dynamics.

6.3.3 Monolithic GaN SBH Gate Driving

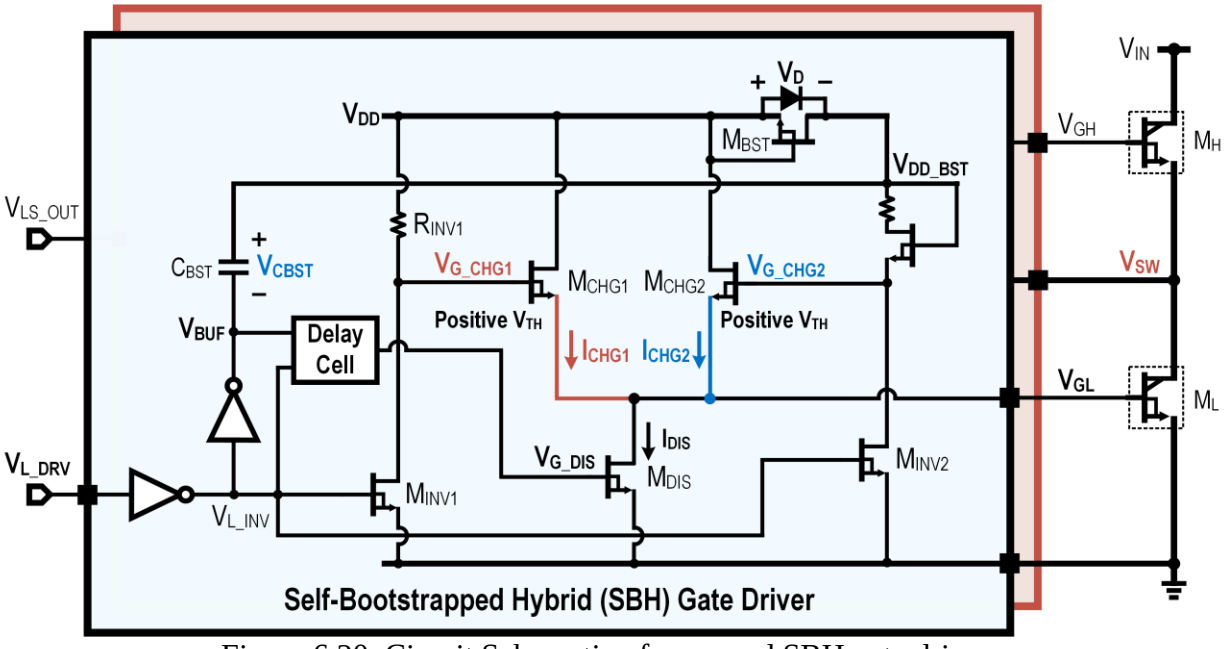
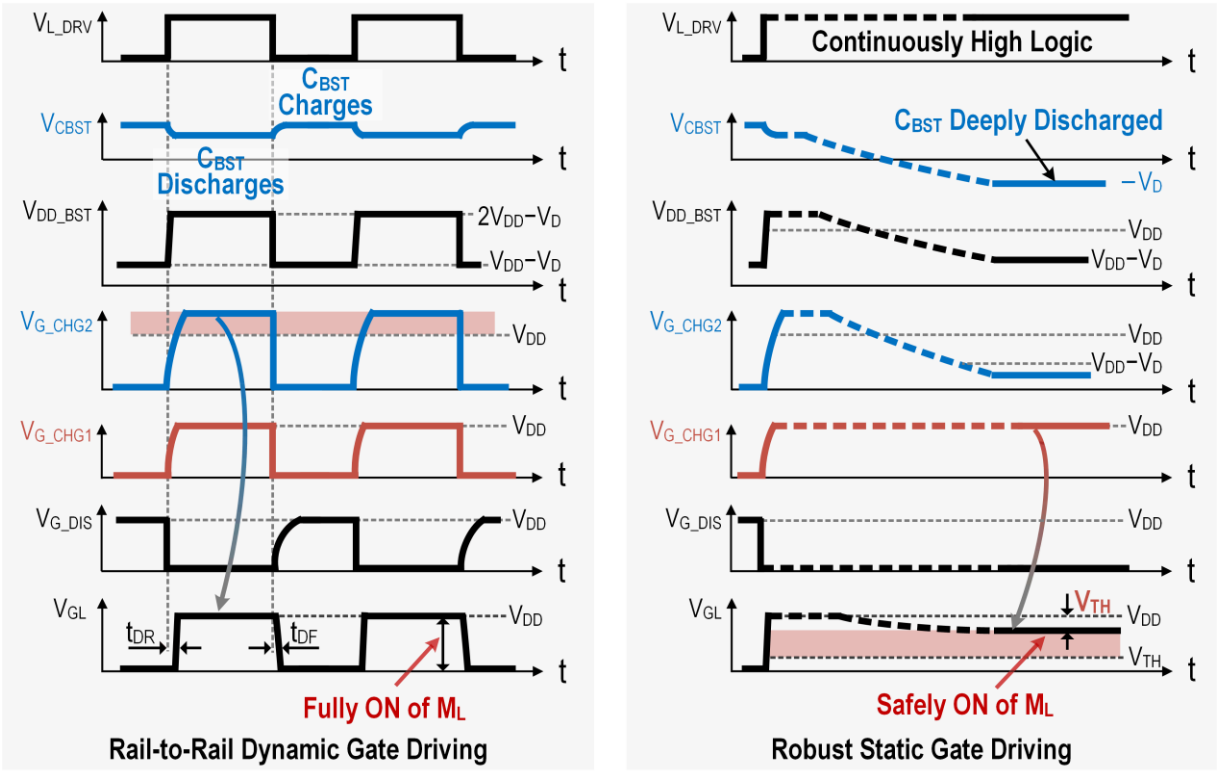


Figure 6.20. Circuit Schematic of proposed SBH gate driver.

Figure 6.20 shows the circuit schematic of the proposed SBH gate driver, which adaptively achieves rail-to-rail dynamic gate driving in steady-state operation and robust static gate driving during start-up and load transients. The adaptive hybrid driving scheme is realized by two e-mode GaN charging switches (M_{CHG1} and M_{CHG2}). When the power converter is in a normal operation, power switches such as M_L and M_H are turned on and off periodically. The SBH gate driver charges its bootstrap capacitor C_{BST} periodically by taking advantage of the converter's natural switching actions. With the dynamic charge switch M_{CHG2}, the self-bootstrapping mechanism in the gate driver can compensate the large threshold voltage drop V_{TH}, keeping the voltage swing at the gate of GaN switch M_L rail-to-rail. Thus, fast switching and low on-resistance of power switches are achieved. When the power converter is in start-up or load transients, the power switches would be kept continuously on. Although the self-bootstrapping mechanism cannot operate properly without switching operation, the SBH gate driver can still maintain reliable gate driving voltage owing to the paralleled static charge switch M_{CHG1}.

Figure 6.21 illustrates the detailed operation waveforms of SBH gate driver. Firstly, the dynamic switching control is presented in Figure 6.21(a). When the input voltage of gate driver V_{L_DRV} is low ("0"), M_{INV1} and M_{INV2} are on to pull V_{G_CHG1} and V_{G_CHG2} low. The two charging switches M_{CHG1} and M_{CHG2} are thus off. Meanwhile, because V_{BUF} is low, the bootstrap capacitor C_{BST} is pre-charged through the body diode of M_{BST}, making V_{CBST} equal to $V_{DD}-V_D$. Once V_{L_DRV} switches from low to high, M_{INV1} and M_{INV2} are turned off. Due to the presence of R_{INV1}, V_{G_CHG1} rises to V_{DD} to turn on M_{CHG1}. Meanwhile, V_{BUF} rises to V_{DD}. V_{DD_BST} is self-bootstrapped to $2V_{DD}-V_D$. V_{G_CHG2} is thus equal to $2V_{DD}-V_D$ as M_{INV2} is off. M_{CHG2} is then turned on. Since M_{DIS} is kept off by the low V_{G_DIS}, V_{GL} is charged up by I_{CHG1} and I_{CHG2}. As V_{GL} rises, M_{CHG1} will be shut

off. However, since V_{G_CHG2} is bootstrapped sufficiently high, it eventually pulls V_{GL} to V_{DD}, enabling fully turn-on of M_L. The periodic charging on C_{BST} prevents large GaN gate leakage from triggering false-off events. On the other hand, the period discharging on C_{BST} refrains the gate drive voltage V_{GL} from rising too high to jeopardize the reliability. Note that there are events such as start-up, shut-down or large load transients, when the driving control signal keeps logically high and power switches have to stay on continuously for a long period. For the M_L in Figure 6.21(b), it is steadily controlled by high V_{L_DRV}. In such a scenario, C_{BST} would be deeply discharged. The gate driver enters a robust static gate driving mode for high robustness and reliability. V_{G_CHG1} stays at V_{DD}, allowing M_{CHG1} to dominate the driving path. Despite that V_{GL} is lower than V_{DD} by V_{TH}, it suffices to keep M_L on safely.



(a) (b)

Figure 6.21. Operation waveforms of proposed SBH gate driver with (a) dynamic switching control, and (b) static DC control.

6.4 Experimental Verification

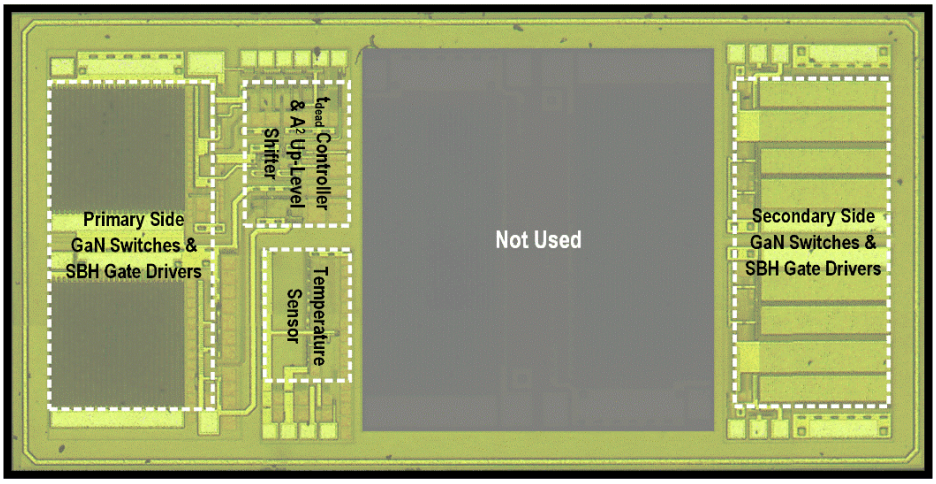


Figure 6.22. Chip photograph.

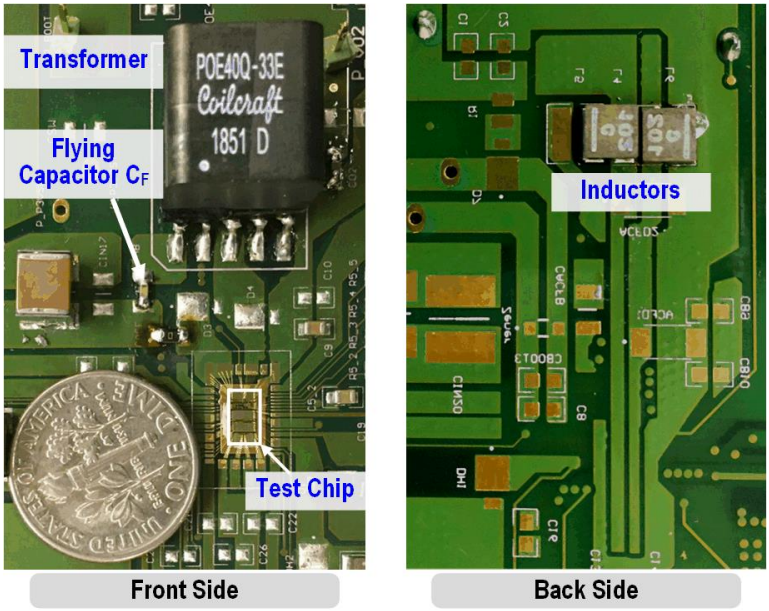


Figure 6.23. Photograph of PCB test board.

The proposed design is implemented using a GaN-on-SOI process. Figure 6.22 shows the chip photograph of proposed monolithic GaN power IC. The active die area of the monolithic GaN AHB converter is 4.5mm^2. It includes two HV primary-side GaN switches with their SBH gate drivers, A^2 up-level shifter, t_{dead} controller, two LV secondary-side GaN switches with their SBH

gate drivers, and temperature sensor. In addition to the AHB converter, two separated HV GaN power switches with their SBH gate drivers are also fabricated. They are used in the standard DPT setup to evaluate the performance of HV GaN HEMT and SBH gate driver. The PCB photograph of AHB converter is illustrated in Figure 6.23. On the front side, one 4.7-µF flying capacitor C_F and one transformer are used in the AHB power stage. On the back side, two 1-µH inductors are used in the synchronous current doubler.

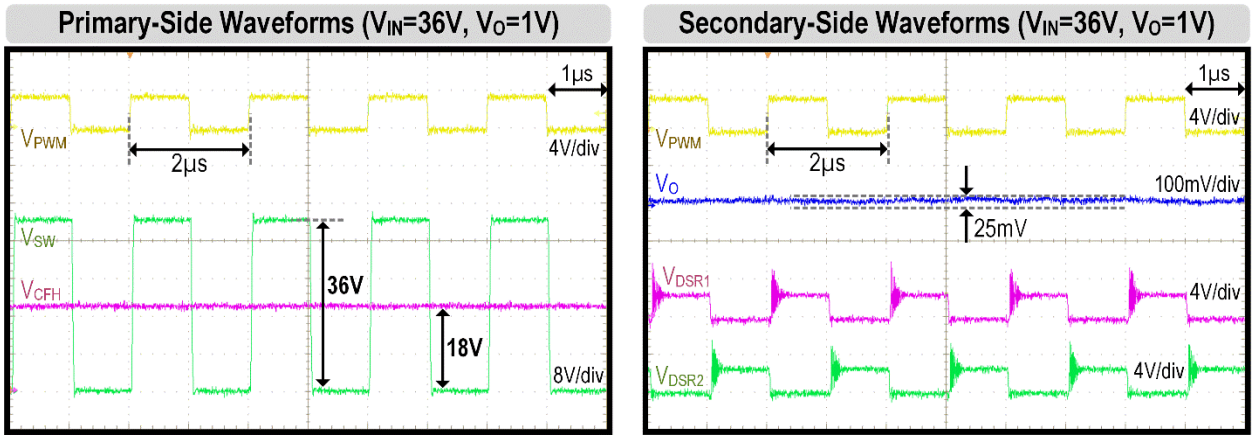


Figure 6.24. Measured key steady-state primary-side and secondary-side operation waveforms of AHB converter for 36V/1V power conversion.

To validate the performance of monolithic GaN AHB power converter, the steady-state primary- and secondary-side switching node voltages are measured. While the nominal input voltage V_{IN} is designed as 48V, the converter can accommodate a wide range of input voltage level, owing to the advantageous topology of AHB converter and high breakdown voltage of HV GaN switch. Firstly, Figure 6.24 demonstrates the converter's steady-state operations at 36-V V_{IN} and 1-V V_O when f_{SW} is 500kHz and I_O is 3A. For the primary-side, the switching node voltage V_{SW} is measured, aligning to the PWM control voltage V_{PWM} with a duty ratio of 50%. Its fast-switching transitions between zero and 36V clearly validate the effectiveness of the proposed A^2 up-level shifter and SBH gate drivers, which directly reveal rail-to-rail turn-on/-off of the high- and low-

side power switches M_H and M_L. The duty ratio of V_{SW} coincides well with V_{IN}/V_O level and the converter's PWM control. The steady-state flying capacitor voltage V_{CF} $(=V_{IN}-V_{CFH})$, which is verified by the 18-V V_{CFH}, confirms fully turn-on and -off of both M_H and M_L, proving valid operation of the proposed SBH gate drivers. For the secondary-side measurements, the switching nodes V_{DSR1} and V_{DSR2} for the respective inductors L_1 and L_2 are also tested, aligning to V_{PWM}. The waveforms verify the complementary switching operations of LV GaN switches M_{SR1} and M_{SR2}. Benefiting from the AHB topology's complementary two-phase operation on the secondary side, the two-phase inductor currents are canceled by each other, and the V_O ripple is measured below 25mV.

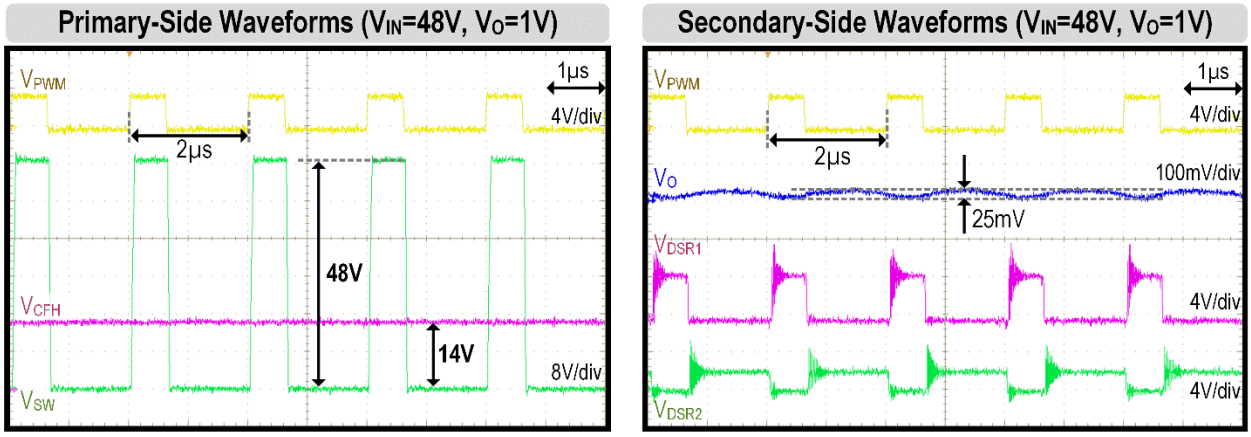


Figure 6.25. Measured key steady-state primary-side and secondary-side operation waveforms of AHB converter for 48V/1V power conversion.

Similarly, when V_{IN} becomes 48V and V_O is 1V, the measured steady-state primary- and secondary-side switching node waveforms are illustrated in Figure 6.25. The duty ratio is adjusted accordingly for 1-V V_O generation with a constant 500kHz f_{SW}. V_{SW} switches between zero and 48V periodically and V_{CFH} becomes stable as 14V, verifying that the voltage across C_F is stable as 34V. On the secondary side, V_{DSR1} and V_{DSR2} also switch complementarily to maintain V_O ripple below 25mV.

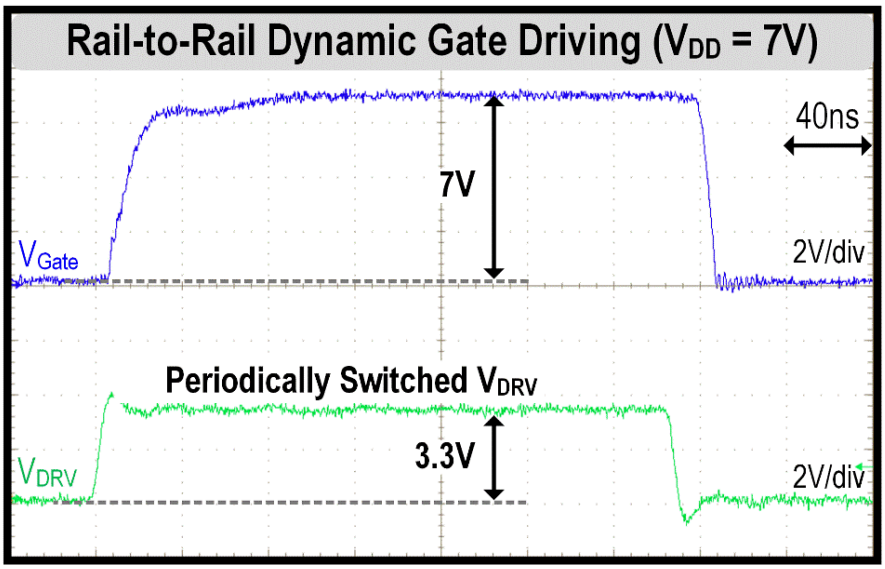


Figure 6.26. Measured control and gating driving signals of SBH gate driver for dynamic driving.

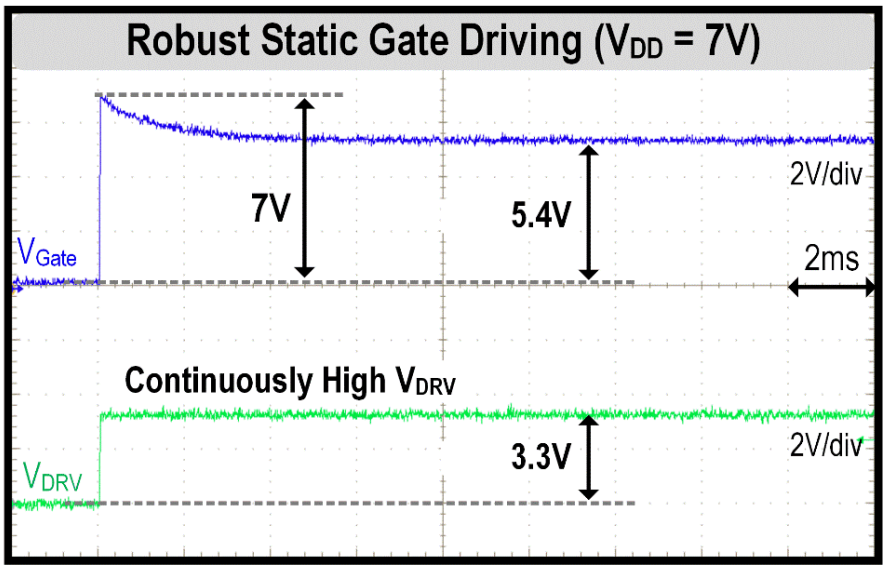


Figure 6.27. Measured control and gating driving signals of SBH gate driver for static driving.

In order to validate the proposed monolithic GaN SBH gate driving technique, the SBH gate driver is measured individually when driving the GaN power switch. Figure 6.26 shows the measured transient control signal V_{DRV} and gate driving signal V_{Gate}, when V_{DRV} is continuously switching, and the gate driver is powered by a 7-V DC power supply V_{DD}. It validates that the SBH gate driver is compatible with 3.3-V logic control. The gate driving signal V_{Gate} switches between

zero and 7V periodically, verifying the rail-to-rail dynamic gate driving. The measured results of SBH gate driver in static control are presented in Figure 6.27. When a static 3.3V DC voltage is applied on V_{DRV}, it represents the positive logic of SBH gate driver. V_{Gate} decreases from 7V gradually because of the leakage current of GaN devices. Finally, V_{Gate} is stable as 5.4V. Since it is much higher than V_{TH} of the GaN power switch, the SBH gate driver accomplishes robust static gate driving control.

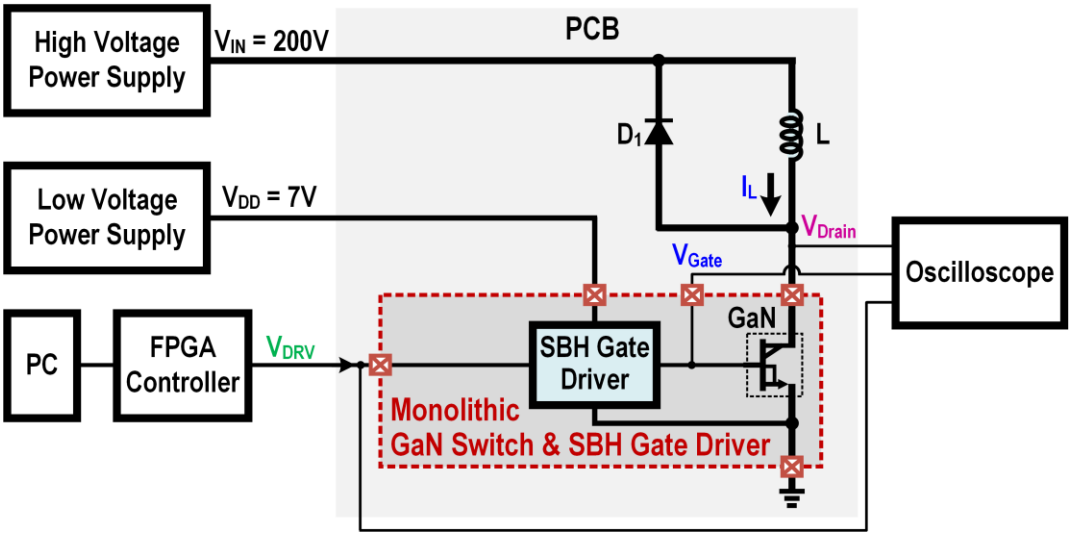


Figure 6.28. DPT setup for HV GaN power switch and SBH gate driver.

Figure 6.28 illustrates the standard DPT setup for the monolithic GaN switch & SBH gate driver when verifying its dynamic switching performance. With one passive inductor L and one power diode D_1, the DPT circuits are built with the monolithic GaN switch & SBH gate driver on PCB. A 200-V power supply is used to power the DPT circuit, and a 7-V power source provides the power for SBH gate driver. The FPGA controller generates a 3.3-V logic signal V_{DRV} with programmed pulse values. The oscilloscope is adopted to capture the transient waveforms of digital control signal V_{DRV}, gate driving signal of SBH gate driver, V_{Gate}, and switching drain voltage of HV GaN power switch, V_{Drain}.

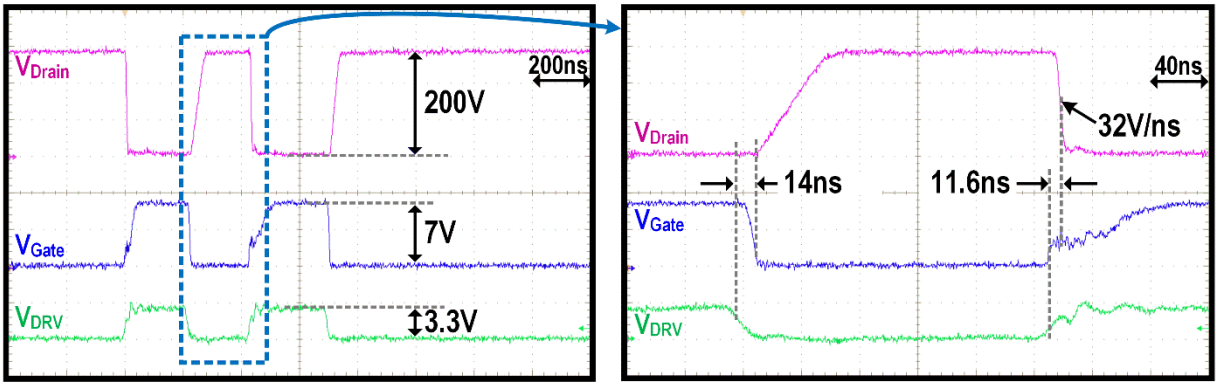


Figure 6.29. Measured transient waveforms in DPT setup.

The measurement results in DPT setup are presented in Figure 6.29. The 3.3-V digital logic signal V_{DRV} controls the switching of GaN power device through the monolithic GaN SBH gate driver. By greatly reducing non-ideal parasitics on the driving path, efficient and reliable driving signal is realized with 11.6-ns and 14-ns rising edge and falling edge propagation delays, respectively. The HV GaN power switch can withstand the drain-source voltage difference as high as 200V. The SBH gate driver realizes a 32V/ns dv/dt slew rate of V_{Drain}.

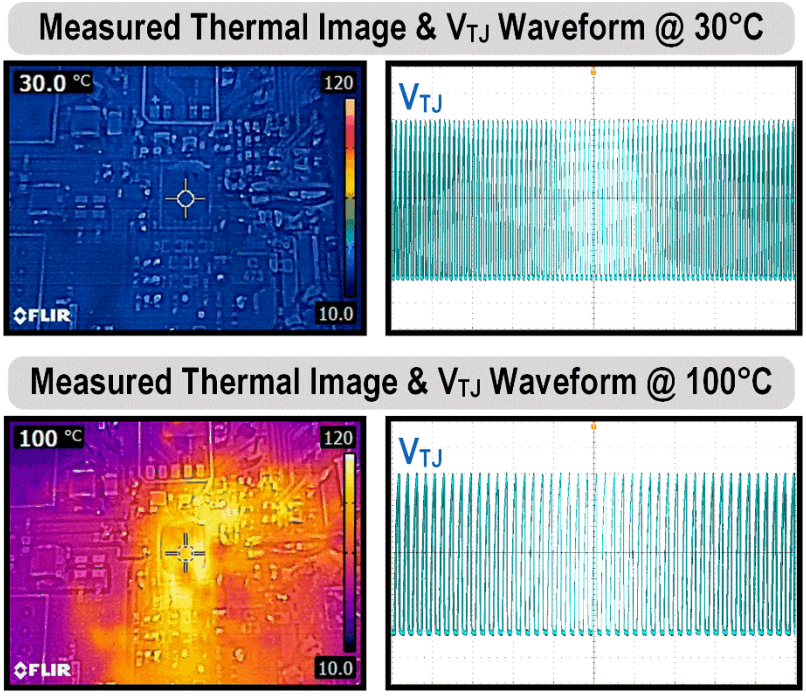


Figure 6.30. Measured thermal images and transient output V_{TJ} at 30°C and 100°C.

To validate the performance of the on-die temperature sensor, it is measured with different temperature conditions. When it is powered by a 7-V supply voltage, Figure 6.30 presents the measured thermal images and transient output signal V_{TJ} under 30°C and 100°C, respectively. It shows that the oscillation frequency of V_{TJ} changes obviously due to different on-chip temperatures. Furthermore, Figure 6.31 summarizes the normalized oscillating frequency versus on-chip temperature from −50°C to 150°C under different supply voltages. The oscillation frequency changes over 3.6 times versus the whole temperature range, accomplishing high T_J monitoring accuracy for over temperature protection.

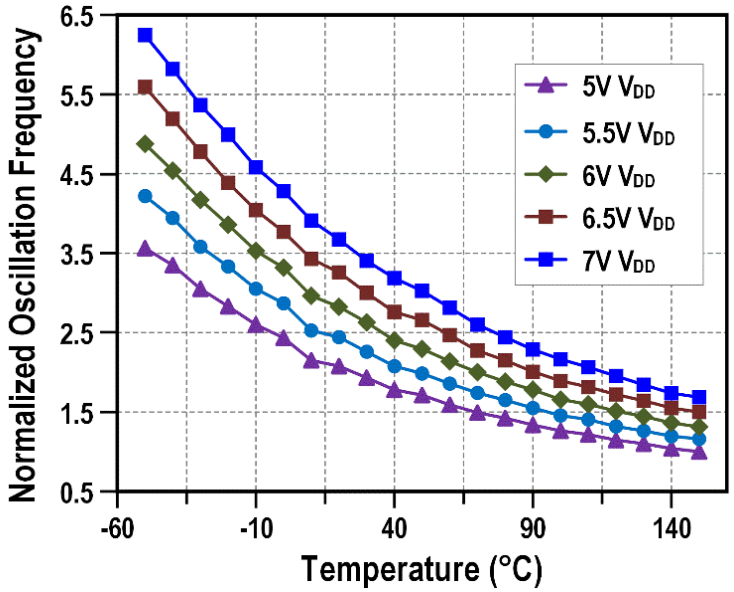


Figure 6.31. Measured normalized oscillation frequency versus temperature with different supply voltages.

The measured efficiencies of monolithic GaN AHB converter are presented in Figure 6.32. In the load current range of 5A, the peak efficiencies are 83.4% and 80.3% for 36V/1V and 48V/1V power conversions, respectively. On the secondary side, high conduction losses of power switches, which are induced by the large on-resistance of GaN power switches, affect the efficiency severely. The efficiencies can be improved further by reducing the on-resistances of secondary-side power

switches. Besides, in the design, due to the technology constraint, chip on board (COB) bonding is adopted. The monolithic GaN chip is directly mounted on PCB and electrically interconnected to its PCB pads through bonding wires. Compared to the land grid array (LGA) and ball grid array (BGA) chip scale packages, it suffers from larger parasitics at the main power loop, which would deteriorate its switching performance to some extent.

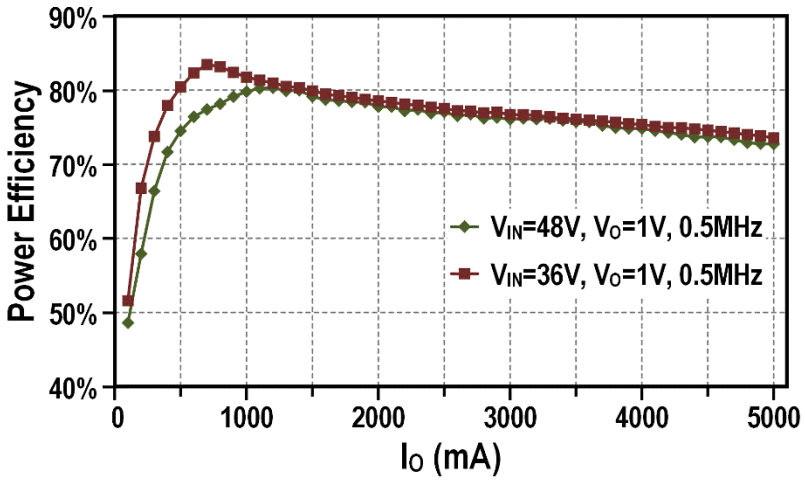


Figure 6.32. Efficiency of monolithic GaN AHB converter.

Figure 6.33 depicts the comparison chart with prior monolithic GaN power IC works. This work achieves the highest level of GaN power IC integration reported, including four on-die power switches, gate drivers, level shifter, t_{dead} controller, and temperature sensor. It is the first monolithic GaN AHB converter and the first monolithic GaN converter achieving direct 48V/1V power conversion. Table 6.1 shows the detailed performance comparison. The monolithic GaN AHB converter realizes a higher conversion ratio, frequency and current density than the others. In contrast to commercial products (EPC2152, NV6252), this work consumes at least 46% less static power and 55% smaller chip area than them, despite of the doubled number of gate drivers. The SBH gate driver achieves lowest propagation delays, rail-to-rail dynamic gating driving and robust static gate driving.

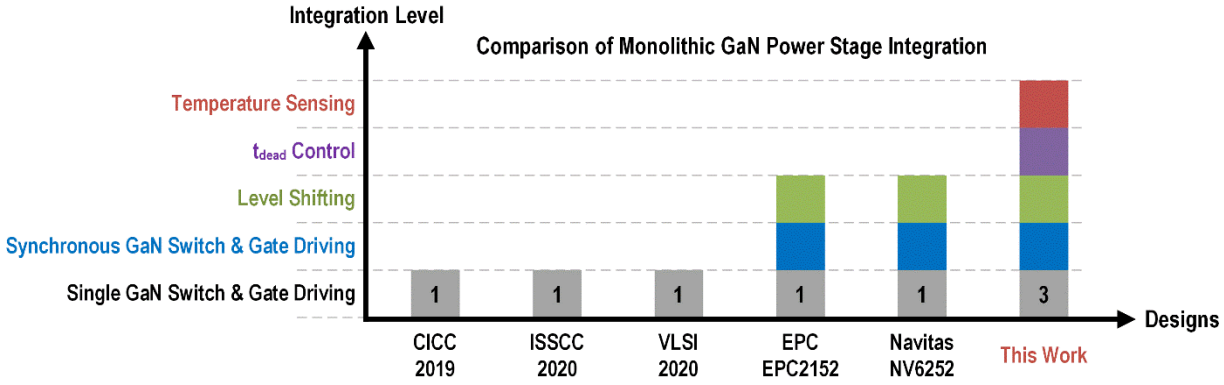


Figure 6.33. Comparison chart with prior monolithic GaN power IC works.

Table 6.1. Performance comparison of proposed monolithic GaN AHB converter to prior arts.

Design		[EPC-21] EPC EPC2152	[Navitas-18] Navitas NV6252	[Liang-19] CICC 2019	[Kaufmann-20] ISSCC 2020	[Chen-20] VLSI 2020	This Work
Power Stage		Half-Bridge	Half-Bridge	Nonsynchronous Buck with Diode	Floating Buck with Diode	Switching Circuit with Resistor	**AHB Converter**
Integration Content		High-Side Switch & Low-side Switch & Gate Drivers & Level Shifter	High-Side Switch & Low-side Switch & Gate Drivers & Level Shifter	Switch & Gate Driver	Switch & Gate Driver	Switch & Gate Driver	**High-Side Switch & Low-side Switches & Gate Drivers & Level Shifter & t_{dead} Controller & Temperature Sensor**
GaN Device		N/A	N/A	E-Mode, D-Mode	E-Mode	E-Mode, D-Mode	**E-Mode**
Input to Output		48V to 12V	500V to 200V*	29V to10V	400V to 50V	N/A	**36V/48V to 1V**
Output Current		12.5A	5A	0.033A	0.57A	N/A	**5A**
Active Chip Area		9.97mm^2	48mm^2	N/A	2.1mm^2	3mm^2	**4.5mm^2**
Current Density		1.25A/mm^2	0.1A/mm^2	N/A	0.24A/mm^2	N/A	**1.1A/mm^2**
Static Power		264mW	129mW	N/A	N/A	3.6mW	**70mW**
Gate Driver	Propagation Delays	20ns/20ns	15ns/15ns	N/A	50ns/50ns	40ns/40ns*	**11.6ns/14ns**
	Rail-to-Rail Dynamic & Robust Static Driving	N/A	N/A	No & Yes	Yes & No	Yes & No	**Yes & Yes**
	No. of Gate Driver	2	2	N/A	N/A	1	**4**

* Estimated

6.5 Summary

In this chapter, monolithic GaN power integration circuits have been introduced, discussed and verified on GaN-on-SOI process. The monolithic GaN AHB power converter is proposed for

direct 48V/1V power conversion with high switching frequency, efficiency and reliability. In the AHB converter, A^2 up-level shifting technique is developed to transmit driving control signals between LV and HV domains. The designed SBH gate driver achieves both rail-to-rail dynamic gate driving and robust static gate driving, accomplishing low on-resistance of GaN power switch and reliable control. Besides, the on-die temperature sensor is proposed to monitor real-time hot spots of AHB converter with low cost, facilitating thermal protection for high reliability. Finally, the experimental results successfully validate the proposed techniques and circuits in this design.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Single-stage high step-down ratio dc-dc power conversion is becoming popular owing to explosive power demand in power electronics. However, because of the high step-down conversion ratio, the switching frequency is constrained low, inducing the penalties of large passive power components and low power density. Besides, the limited low switching frequency increases the EMI noise power at low frequency range and aggravates EMI reduction difficulties with classic techniques. In order to mitigate these challenges, GaN HEMTs have superior switching performance than silicon power devices and have become promising candidates. However, the newly emerging GaN power devices are not fully researched yet compared to the mature silicon power devices. The reliability and stability issues constrain the widespread adoptions of GaN power devices. Furthermore, the current GaN power converters are implemented with discrete GaN power devices and driving and control circuits on PCB. Such implementations suffer from large parasitics and large area cost, which constrain the reliability and performance of GaN technology. As a result, a series of integrated GaN power conversion solutions have been proposed in this dissertation to address the aforementioned challenges.

In this work, one GaN-based DSD power converter is firstly presented, which accomplishes direct 48V/1V power conversion at 2MHz. The proposed master-slave AO^2T control facilitates clock-free phase synchronization and automatic phase current balancing without extra control circuits. Meanwhile, with the proposed elastic ON-time modulation scheme, the load transient response is largely improved compared to the conventional COT control. In addition, the

DSD power converter is protected from disastrous cross-phase T_{ON} overlap on all occasions for high reliability.

Besides, a GaN-based switching power converter with anti-aliasing MR-SSM and in-cycle adaptive ZVS techniques is presented for high step-down ratio dc-dc power conversion. The anti-aliasing MR-SSM actively controls f_{SW} modulation rates for different f_{SW}s, achieving targeted redistribution of EMI energy. It can spread EMI spectra in a wide frequency range without aliasing spikes, attenuating the peak EMI more effectively than classic FR-SSM. An elastic t_{dead} controller optimizes t_{dead} within each switching cycle, accomplishing in-cycle adaptive ZVS during the MR-SSM operation and, thus, maintaining high efficiency. In addition, the proposed pulse-reinforced up-level shifter enhances the driving reliability for high V_{SW} dv/dt transition.

Moreover, an on-chip self-calibrated full-profile dynamic on-resistance sensing strategy has been proposed for the online condition monitoring of GaN-based power converters. The fully integrated tri-state dynamic on-resistance sensors are implemented in a GaN-based half-bridge power converter, which is regulated by a dual ON-time control with two predefined T_{ON}s. Thanks to the proposed strategy, sensing errors are calibrated automatically with high accuracy and low cost. The M_H and M_L forward dynamic r_{on} sensors are compatible with the feedback controller, ensuring low area and power overheads. Meanwhile, the ET M_L reverse r_{on} sensor enables accurate negative V_{SW} sensing within a short t_{dead} without compromising efficiency. The dual-rail up-level shifter overcomes large negative switching node voltage during t_{dead} challenges and improves the GaN driving reliability.

Finally, one monolithic integrated GaN AHB power converter is designed for direct 48V/1V power conversion. In the converter, two HV GaN HEMTs are used as primary power

switches, while two LV GaN HEMTs are used as synchronous rectifiers of the secondary-side current doubler. In addition to the GaN power switches, monolithic GaN SBH gate drivers, A^2 up-level shifter, t_{dead} controller, and temperature sensor are also integrated on one GaN chip. The SBH gate driver realizes both rail-to-rail dynamic gate driving in normal operation and robust state gate driving during start-up and load transients. By fully turning on GaN power switches, the on-resistance is minimized for high efficiency. The robust static gate driving voltage ensures reliable driving logic control regardless of large leakage currents of GaN devices. The short propagation delays and low power loss enable high f_{SW} operation of power converters. Meanwhile, the A^2 up-level shifter accomplishes fast and reliable driving signal transmission from LV domain to HV domain, paving the way for a monolithic integrated switching power converter with different voltage domains. Furthermore, the on-chip temperature sensor monitors the hot spots of the monolithic GaN power converter directly with high accuracy and low complexity, facilitating thermal protection.

All the proposed GaN power converters have been fabricated, tested to demonstrate the proposed operation scheme and design techniques. The effectiveness is verified successfully with measurements results: high switching frequency, high efficiency, low EMI noise, high reliability and monolithic integration of GaN power conversions.

7.2 Future Work

In this research, multiple integrated GaN power converters have been proposed for high step-down ratio dc-dc power conversion, targeting on power density and efficiency improvements, EMI noise reduction, reliability enhancement, and monolithic integration. Future research and investigation can be conducted in the following aspects: further increasing the switching frequency

for low area cost and high power density, optimizing EMI reduction techniques with low area and power overheads, brilliant power converters with self-diagnosis functions, and more reliable and efficient monolithic GaN integration designs.

Firstly, to improve the power density of high step-down ratio power converters, the hybrid power conversion topologies, which incorporate passive inductors and capacitors, are becoming promising. But their operation schemes become much more complicated than the classic half-bridge power converter. More efficient and robust feedback control, gating driving, bootstrapping, start-up, capacitor balancing, and protection circuits are thus needed. Besides, the isolated switch mode power converters are promising for high step-down ratio dc-dc power conversions thanks to the transformer turns ratio. But classic off-the-shelf transformers are mainly used for low switching frequency, inducing its bulky size and compromising the power conversion performance. Specialized transformers are needed for high frequency high V_{IN}/V_O dc-dc power converters.

Secondly, SSM techniques can be used to reduce EMI noise, but they will introduce area and power overheads. The EMI noise of a switching power converter is affected by its power conversion specifications, such as input voltage, output voltage and load current. Optimizing the EMI reduction techniques adaptively for different power conversion occasions can improve the overall performance of a power converter. Besides, the active EMI filter, which adopts an operational amplifier and small decoupling capacitors, can be used to attenuate EMI noise with low area cost. The integration of an active EMI filter becomes a meaningful EMI reduction way for area-efficient power converter designs. Moreover, classic SSM techniques are not suitable for the hybrid power converters since the continuous frequency modulation could contradict their operation schemes and challenge reliabilities. Realizing effective and reliable EMI attenuation

solutions for hybrid power converters is also desired. In addition to the conductive EMI noise, the radiated EMI noise can be suppressed by optimizing the gate driving circuits in different power conversion topologies.

Thirdly, online condition monitoring is crucial to monitor the healthy state and ensure high reliability of GaN power converters. More advanced condition monitoring strategies are highly desired. The brilliant switching power converter, which diagnoses its healthy state automatically and actively optimizes its operation states for lifetime extension, is highly promising for further power conversion systems. Besides, the area and power overheads induced by the monitor and diagnosis system can be further reduced. Meanwhile, since the key parameters of GaN power converters are susceptible to multiple factors, the monitor and diagnosis system needs to distinguish if a specific parameter variation is critical for the power converter lifetime.

Last but not least, this research has provided groundwork in monolithic GaN power converters. For future work, designs of robust and efficient monolithic GaN power converters are very important. Due to the lack of compatible p-type devices, the monolithic GaN gate driving circuits suffer from a much higher power loss. Special circuit design techniques are crucial to improve the speed, reduce the cost, and enhance the reliability of the monolithic GaN gate driver. Moreover, a monolithic GaN down-level shifter is crucial when implementing complicated power conversion topologies. The fast, efficient, and robust monolithic GaN feedback controller is also desired for future monolithic GaN power converters.

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PUBLICATIONS

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2. **D. Yan** and D. B. Ma, "An automotive-use battery-to-load GaN-based switching power converter with anti-aliasing MR-SSM and in-cycle adaptive ZVS techniques," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 56, no. 4, pp. 1186-1196, Austin, TX, USA, Apr. 2021.

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