Dual-Gate MoS_2 Transistors with Sub-10 NM Top-Gate High-K Dielectrics

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Dual-gate MoS_2 transistors with sub-10 nm top-gate high-k dielectrics

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High quality sub-10 nm high-k dielectrics are deposited on top of MoS_2 and evaluated using a dual-gate field effect transistor configuration. Comparison between top-gate HfO_2 and an Al_2O_3/HfO_2 bilayer shows significant improvement in device performance due to the insertion of the thin Al_2O_3 layer. The results show that the Al_2O_3 buffer layer improves the interface quality by effectively reducing the net fixed positive oxide charge at the top-gate MoS_2/high-k dielectric interface. Dual-gate sweeping, where both the top-gate and the back-gate are swept simultaneously, provides significant insight into the role of these oxide charges and improves overall device performance. Dual-gate transistors encapsulated in an Al_2O_3 dielectric demonstrate a near-ideal subthreshold swing of ~60 mV/dec and a high field effect mobility of 100 cm^2/V·s. *Published by AIP Publishing.*
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Transition metal dichalcogenides (TMDs) are being intensely investigated due to their unique 2D properties that can be utilized in low-power, high-mobility circuitry.[1–5] For semiconducting TMDs like MoS_2, their integration with ultrathin high-k dielectrics such as HfO_2 and Al_2O_3 has proven quite challenging due to the relatively inert TMD surface.[6,7] To achieve performance close to the current level of CMOS technology, deposition of uniform, pin-hole free sub-10 nm high-k dielectric films is necessary. Recent developments in surface functionalization have been used to demonstrate deposition of ultrathin high-k dielectric films on MoS_2.[8–11] The deposition of high-k dielectrics on the top surface of back-gate (BG) MoS_2 FETs has been shown to significantly affect the ON and OFF current as well as create a V_T shift.[12,13] There have also been multiple studies demonstrating a significant influence of the back-gate bias[14–17] as well as the choice of dielectrics.[18,19] The use of a biasing method known as dual-gate (DG) sweeping[20,21] helps to further elucidate the effects of oxide charges on device performance and achieve overall better control of the MoS_2 channel. In this study, we compare the effects of HfO_2 deposition to Al_2O_3/HfO_2 bilayer deposition on MoS_2 in terms of device performance and show how oxide charges play a role. Using the dual-gate sweeping methodology, this work shows significant improvements in threshold voltage, subthreshold swing (SS), mobility, and hysteresis, for the $Al_2O_3/MoS_2/Al_2O_3/HfO_2$ gate stack compared to the $Al_2O_3/MoS_2/HfO_2$ gate stack due to the reduction of net fixed positive oxide charge at the top-gate MoS_2/high-k dielectric interface. This results in a near-ideal SS of ~60 mV/dec, high field effect mobility (μ_{FE}) values >100 cm^2/V·s, and an I_{ON}/I_{OFF} of ~10^6.

Atomic layer deposition (ALD) of Al_2O_3 (~27 nm) at 250 °C onto a p^{++} Si wafer was used for back gate isolation. On the opposite side of the Si wafer, Al was deposited for a backside wafer contact followed by a 400 °C forming gas anneal to reduce oxide charge. The ALD Al_2O_3 then serves as the "substrate" and back gate oxide for exfoliated multi-layer MoS_2 flakes.[18] Using photolithography, source/drain contacts are defined on the transferred flakes (~4–8 nm thickness) followed by e-beam evaporation of Ti/Au contacts with a lift-off process. The flakes also undergo a 5 s O_2 plasma exposure ("de-scum") at 50 W to remove photoresist residue prior to contact metal deposition on natural MoS_2. Electrical back-gate measurements are then performed followed by a 300 °C UHV anneal for 2 h to facilitate desorption of residual contaminants.[22] Then, a 15 min *in-situ*, room-temperature UV-ozone surface treatment with subsequent ALD of either HfO_2(9 nm) or Al_2O_3/HfO_2(3 nm/6 nm) was deposited at 200 °C to produce $p^{++}Si/Al_2O_3/MoS_2/HfO_2$ or $p^{++}Si/Al_2O_3/MoS_2/Al_2O_3/HfO_2$ structures[10,11] (Fig. S1). After high-k dielectric deposition, back-gate electrical measurements are performed, followed by photolithography of a Pd/Au top-gate for further sequential device measurements. The structures are compared sequentially using a back-gate (BG) sweep mode, a top-gate (TG) sweep mode, and a dual-gate (DG) sweep mode for comparison of the device response. It is noted that no other post-metal gate deposition anneals were conducted in this study.

Prior to any top-gate high-k dielectric deposition, back-gate MoS_2 FETs ($p^{++}Si/Al_2O_3/MoS_2$) were electrically characterized in order to compare the I-V response before and after the top-gate ALD process. The transfer curves shown in Fig. 1(a) (left) compare the electrical response before and after HfO_2 deposition, where a significant increase in OFF current, an increase in ON current, and a negative threshold voltage shift ($-\Delta V_T$) are observed. However, as seen in Fig. 1(a) (right), the deposition of the high-k dielectric bilayer (Al_2O_3/HfO_2), where the Al_2O_3 is deposited on MoS_2 before the HfO_2 cap, results in a slight increase in both OFF and ON currents as well as a positive threshold voltage shift ($+\Delta V_T$). Previous studies that investigated the electrical response after high-k dielectric deposition demonstrated that both HfO_2 and Al_2O_3 deposition result in a higher OFF current and a $-\Delta V_T$, but there was no inclusion of a UHV anneal to remove surface contaminants nor was there a functionalization treatment

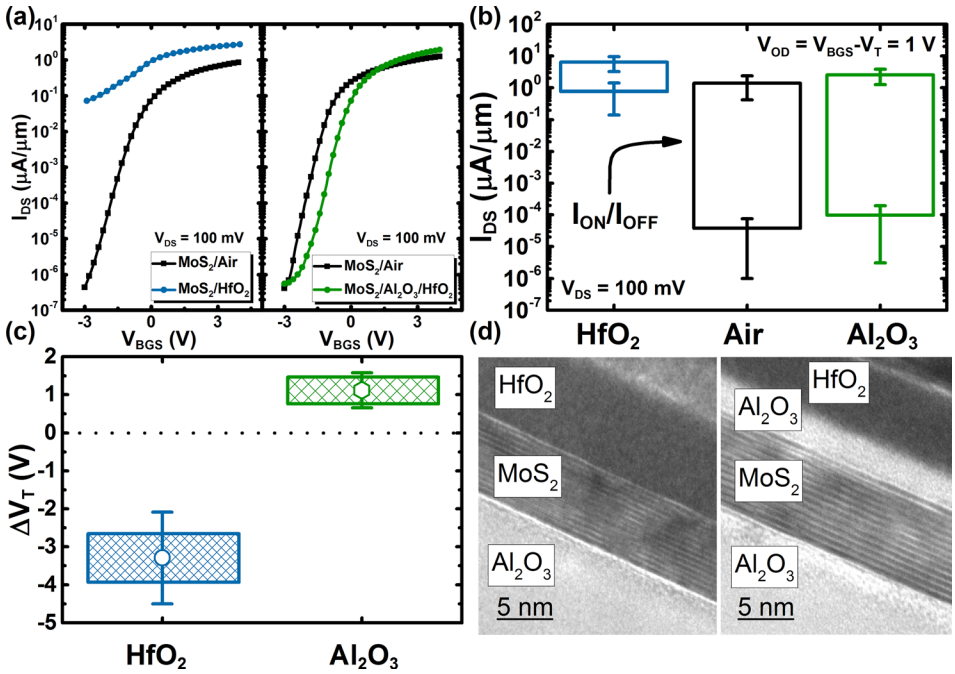

FIG. 1. (a) The transfer characteristics of back gated MoS_2 MOSFETS ($W = 15$–$20\,\mu m$ and $L = 4\,\mu m$) before and after the HfO_2 (left) and the Al_2O_3/HfO_2 bilayer (right) deposition and (b) average ON and OFF currents as well average I_{ON}/I_{OFF} ratios for multiple BG MoS_2 FETs pre- and post-high-k dielectric deposition. The high OFF current after HfO_2 deposition indicates the introduction of fixed positive oxide charge resulting in an actively conducting top channel. (c) The threshold voltage shift (ΔV_T) after high-k dielectric deposition differs for each gate stack with a negative ΔV_T for HfO_2 and positive ΔV_T for the Al_2O_3/HfO_2 bilayer with the (d) TEM images illustrating $Al_2O_3/MoS_2/HfO_2$ and $Al_2O_3/MoS_2/Al_2O_3/HfO_2$ stack structures.

like UV-ozone to ensure a pin-hole free film.[12,13] A recent study by Liu *et al*. demonstrated the same trends after Al_2O_3 deposition as this work with the inclusion of their own functionalization treatment consisting of O_2 plasma exposure prior to ALD.[8] Here, they demonstrated a slightly higher OFF current and a $+\Delta V_T$, consistent with the results shown in Fig. 1(a). This suggests that the inclusion of a functionalization treatment is key for achieving enhanced device performance.

After looking at the electrical characteristics of multiple back-gate MoS_2 FETs, several trends emerge. The OFF and ON currents before and after high-k dielectric deposition in Fig. 1(b) demonstrate a trend of a significantly higher OFF current after HfO_2 deposition, and a $-\Delta V_T$ is observed as shown in Fig. 1(c). This suggests that there is significant fixed positive oxide charge at the MoS_2/HfO_2 interface, which also likely accounts for the increase in ON current since the positive oxide charge may be inducing a higher electron concentration[23] in the channel. It is also prudent not to rule out the role of the UHV anneal and the ALD process on the contact interface, which may result in a reduction of contact resistance,[24] also potentially contributing to the increase in ON current. A potential mechanism behind the $-\Delta V_T$ may be due to oxygen vacancies in the HfO_2. Valsaraj *et al*.[25] presented theoretical and experimental studies which indicate that a $-\Delta V_T$ after deposition of HfO_2 on MoS_2 is due to oxygen vacancies in the HfO_2 film. Other works have shown the presence of positively charged oxygen vacancies from ALD HfO_2.[26–28] This positive charge results in a corresponding electron density on MoS_2, which can be considered as an effective *n*-type doping of the MoS_2 channel.[25] The trends observed in Figs. 1(b) and 1(c) for the bilayer deposition (with Al_2O_3 directly on the MoS_2 top interface instead of HfO_2) show slight increases in OFF and ON currents as well as a $+\Delta V_T$ suggesting a significant reduction of fixed positive oxide charge at the top-gate MoS_2/high-k dielectric interface or potentially the introduction of negative oxide charge due to the insertion of the ultrathin Al_2O_3 layer between MoS_2 and HfO_2. The latter has been demonstrated for Al_2O_3 deposited by ALD on InGaAs[29] and GaSb[30] surfaces, where negative charge at the Al_2O_3/III-V interface was found. Impedance spectroscopy is needed to definitively determine the source of the improvement in the I-V response after the introduction of Al_2O_3 between MoS_2 and HfO_2.[31] Overall, fixed positive oxide charge at the MoS_2/HfO_2 interface after high-k dielectric deposition on MoS_2 appears to result in poor device characteristics, and the insertion of Al_2O_3 on MoS_2 prior to HfO_2 allows for significantly improved device performance for the $p^{++}Si/Al_2O_3/MoS_2/Al_2O_3/HfO_2$ stack compared to the $p^{++}Si/Al_2O_3/MoS_2/HfO_2$ stack [stacks shown in Fig. 1(d)].

After the high-k dielectric deposition and BG-only device measurements, the top-gate metal electrode was deposited and patterned and the DG FETs were then electrically characterized using a BG sweep, a TG sweep, and our DG sweep approach. The motivation behind the development of the DG sweep stems from the extremely high OFF current following HfO_2 deposition, which, as reported previously,[32] often requires a high temperature anneal in order to remove the fixed positive oxide charge and achieve adequate channel depletion. Such annealing can have certain unwanted side-effects such as formation of polycrystalline HfO_2 or a reduction in ON current.[33,34] Additionally, the common use of a TG bias sweep with a fixed-BG bias—often employed with a thick SiO_2 back-gate dielectric in the literature—typically results in V_T shifts and major changes in the OFF/ON currents.[14–16] By using multiple bias configurations, we are able to deconvolute the impact of each interface and dielectric.

Starting with the $Al_2O_3/MoS_2/HfO_2$ stack, a comparison can be made between a TG sweep with a fixed-BG bias and a DG sweep on the same device. For the TG sweep with a fixed-BG bias in Fig. 2(a) (left), there are changes in the OFF and ON currents as well as V_T shifts as the BG bias is stepped from -5 V to 5 V for each TG sweep, similar to previous reports.[15,16] While choosing a TG sweep at a -5 V BG

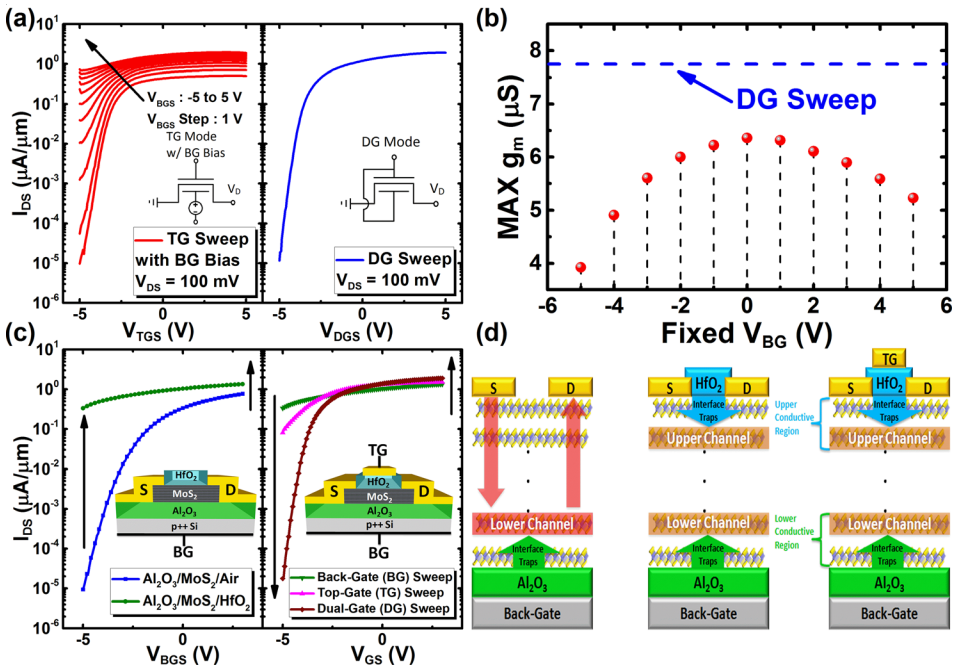

FIG. 2. (a) Comparison between the commonly used TG sweep with a fixed-BG bias (left) and a DG sweep (right) demonstrating the lowest OFF current, the highest ON current, and a better overall subthreshold swing than any TG sweep with a BG bias. (b) The extracted maximum transconductance (g_m) as a function of fixed-BG bias indicates a reduction in g_m due to a fixed-BG bias which can lead to an underestimation of mobility. (c) The transfer curves before and after HfO_2 deposition (left) along with the BG, TG, and DG sweeps (right) indicate the (d) formation of a secondary channel due to the introduction of fixed positive oxide charge with only a DG sweep being able to deplete both channels.

bias provides a low OFF current, there is a sacrifice of an order of magnitude in the ON current observed. The inverse is true for a BG bias of +5 V where there is not only a high OFF current but also a high ON current. In order to achieve the highest ON current and the lowest OFF current, a DG sweep, which sweeps the BG and TG simultaneously (Fig. S2) using the same voltage range and the same voltage step, was investigated.

As shown in Fig. 2(a) (right), the DG sweep provides the highest ON current and the lowest OFF current and a better overall SS than any of the TG sweeps with a fixed-BG bias [Fig. 2(a) (left)]. Furthermore, mobility is often extracted using the transconductance (g_m) of a transfer curve that consists of a TG sweep with a fixed-BG bias.[35,36] The behavior of g_m as a function of the fixed-BG bias in Fig. 2(b), along with the position of the peak transconductance often used to extract the peak mobility, demonstrates a reduction in g_m with any fixed-BG bias. This suggests that with a fixed-BG bias, there is an underestimation of the mobility where a TG sweep without any BG bias achieves the highest peak g_m value. Similar to a FinFET, the DG sweep configuration allows for better overall control of the MoS_2 channel and does so without degrading g_m nor the OFF and ON currents.

Using this electrical characterization methodology, the role of oxide charge in DG MoS_2 FET performance can be further elucidated. As shown in Fig. 1(a) (left), the deposition of HfO_2 on MoS_2 results in an extremely high OFF current which may completely be due to the introduction of fixed positive oxide charge. In Fig. 2(c), a comparison of the transfer curve before and after HfO_2 deposition and the BG, TG, and DG sweeping modes of the $Al_2O_3/MoS_2/HfO_2$ stack are shown. In Fig. 2(c) (right), neither a BG sweep nor a TG sweep can deplete the MoS_2 channel to its original OFF state prior to any top dielectric deposition. This suggests that the introduction of fixed positive oxide charge induces the formation of a secondary conduction channel at the top MoS_2/HfO_2 interface as illustrated schematically in Fig. 2(d) where neither a BG nor TG sweep can turn off the device. With a DG sweep in Fig. 2(c) (right), the transfer curve shows full gate modulation with the OFF current almost the same value as prior to HfO_2 deposition as shown in Fig. 2(c) (left). The DG sweep is thus able to deplete "both" channels and turn off the FET, suggesting that the high OFF current after HfO_2 deposition is a phenomenon caused primarily by fixed positive oxide charge at the MoS_2/HfO_2 interface. Although a DG sweep can neutralize the effects of the fixed positive oxide charge, the transfer curve, with a V_T of −3.7 V as well as an SS of ∼200 mV/dec, still lacks the optimal performance that is theoretically possible.

Introducing an ultrathin Al_2O_3 layer between MoS_2 and HfO_2 may be able to buffer some of the effects of the fixed positive oxide charge introduced by the HfO_2 as there appears to be minimal changes in OFF/ON currents and SS after the Al_2O_3/HfO_2 bilayer deposition (see Fig. 1). Comparing the different sweeping modes for the $Al_2O_3/MoS_2/Al_2O_3/HfO_2$ stack in Fig. 3(a) shows significant improvement going from BG sweep to TG sweep and then finally DG sweep where the transfer curve "straightens out," the OFF current decreases, the ON current increases, and the SS becomes steeper. As with the $Al_2O_3/MoS_2/HfO_2$ stack, the DG sweep shows the best device characteristics due to better electrostatic control over the MoS_2 channel. As shown in Fig. 3(c), the DG sweep for the $Al_2O_3/MoS_2/Al_2O_3/HfO_2$ gate stack demonstrates a near-ideal SS of ∼60 mV/dec, an I_{ON}/I_{OFF} of $\sim 10^6$, and a μ_{FE} of 100 $cm^2/V{\cdot}s$. Furthermore, the output characteristics in Fig. 3(b) show linearity and have a Y-Function-extracted[37] contact resistance (R_C) of ∼1 kΩ·μm, suggesting that reduction in R_C is necessary to prevent underestimation of the device mobility.[38,39] The value of R_C is sufficiently low that it does not have an impact on the evaluated SS (see Fig. S5). Comparing the DG sweeps of the two different gates stacks in Fig. 3(d), the insertion of Al_2O_3 prior to HfO_2 deposition improves device performance on all fronts, specifically a more positive V_T, steeper SS, and smaller hysteresis. Moreover, there is a

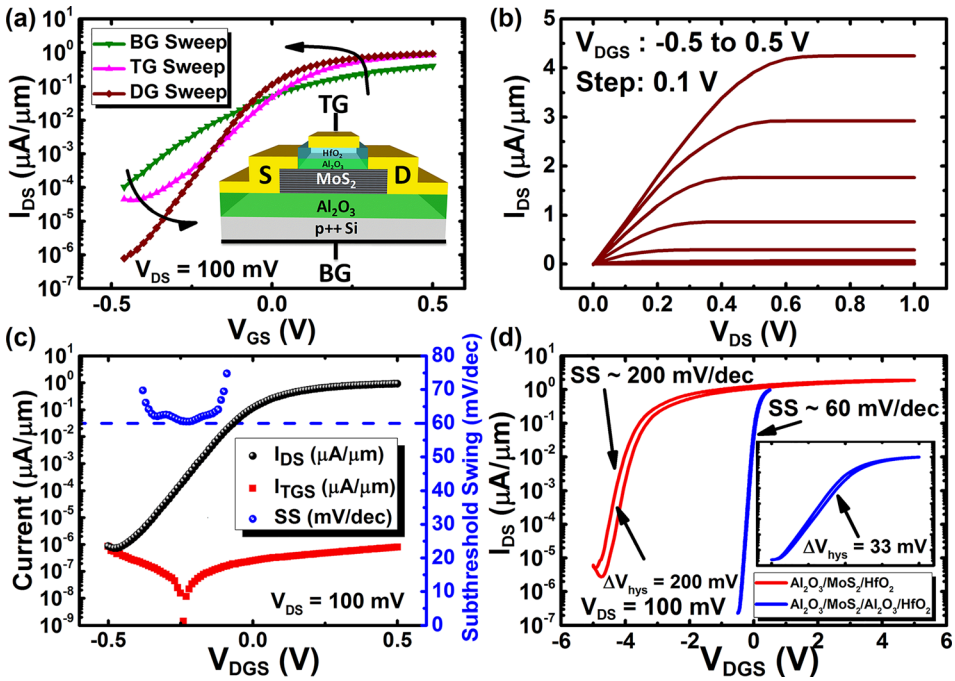

FIG. 3. (a) Transfer curves of the $p^{++}Si/Al_2O_3/MoS_2/Al_2O_3/HfO_2$ gate stack in BG, TG, and DG sweep modes with the inset showing the DG MoS_2 FET cross-section. (b) The output characteristics with linear I-V and (c) the DG sweep demonstrating a near-ideal SS of ~60 mV/dec, an I_{ON}/I_{OFF} of $\sim 10^6$, and a μ_{FE} of 100 $cm^2/V{\cdot}s$. (d) Comparison between the $p^{++}Si/Al_2O_3/MoS_2/HfO_2$ gate stack and the $p^{++}Si/Al_2O_3/MoS_2/Al_2O_3/HfO_2$ shows a more positive V_T, smaller hysteresis, and better overall device performance due to the insertion of the thin Al_2O_3 layer between MoS_2 and HfO_2.

significant improvement in mobility[20] (Fig. S3), which, according to Ma and Jena, has to do with the surrounding dielectric environment, among other factors.[40] Previous studies have shown the influence of the back-gate dielectric on top-gate performance, where changing the gate stacks from $HfO_2/MoS_2/HfO_2$ to $SiO_2/MoS_2/HfO_2$ to $Al_2O_3/MoS_2/HfO_2$ improves the top-gate device performance, which is consistent with Ma *et al*. predictions.[18,19] The same consistency is evident in this study, where there is significant improvement in mobility going from $Al_2O_3/MoS_2/HfO_2$ to $Al_2O_3/MoS_2/Al_2O_3$. Further improvements in device performance are dependent on impurity control and significant reductions in R_C. The encapsulation of MoS_2 by high-k dielectrics to control the semiconductor/dielectric interface is also an aspect that requires further study. It has been shown, for example, that Al_2O_3 and HfO_2 have different ability to inhibit uncontrolled surface oxidation for III-V semiconductors,[22] and the impact of such effects is anticipated to also play a role for such TMD interfaces.

Comparison between top-gate HfO_2 and Al_2O_3/HfO_2 bilayer deposition in terms of DG MoS_2 FET performance demonstrates significant improvements due to the insertion of the Al_2O_3 between MoS_2 and HfO_2. DG MoS_2 FETs with a top- and back- Al_2O_3 gate dielectric demonstrate a near-ideal SS of ~60 mV/dec, an I_{ON}/I_{OFF} of 10^6, and a μ_{FE} of 100 $cm^2/V{\cdot}s$. These improvements resulting from the bilayer gate oxide (Al_2O_3/HfO_2) can be attributed to the reduction of fixed positive oxide charge at the top-gate MoS_2/high-k dielectric interface as well as the use of a DG sweeping mechanism. The DG sweeping, where both the BG and TG are swept simultaneously, helps further elucidate the role of oxide charge and, most significantly, provides better electrostatic control of the MoS_2 channel. This study provides significant insights into the influence of oxide charge on device performance as well the use of dual-gate electrical characterization methodology in order to integrate ultrathin high-k dielectrics with TMDs for future device applications.

See supplementary material for back-gate device structure schematic cross-sections, further details about dual-gate sweeping methodology, dual-gate mobility extraction, details about gate leakage after HfO_2 deposition, and the impact of contact resistance on evaluated subthreshold swing.

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