FERROELECTRIC $Hf_xZr_{1-x}O_2$ FOR NEXT GENERATION NON-VOLATILE MEMORY APPLICATIONS AND ITS RELIABILTY

by

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To my family

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The University of Texas at Dallas, 2021

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To keep up with the increasing memory demands, developing memories with higher densities, speed and energy efficiency is necessary at different levels of the memory hierarchy. Ferroelectric materials have been considered alternative memory components; however, the conventional perovskite-based ferroelectric materials pose several challenges due to CMOS integration, high thermal budget, and scaling to sub 70 nm thicknesses. In this regard, the discovery of ferroelectricity in doped HfO_2 thin films was revolutionary as HfO_2 is already employed in front end CMOS as a high-k dielectric material for scaled thicknesses (<10 nm) . Additionally, doping HfO_2 films with ZrO_2, i.e., $Hf_{0.5}Zr_{0.5}O_2$ (HZO) showed stable ferroelectric phase crystallization at back-end of line compatible temperatures (<450 °C).

This dissertation addresses some critical issues on the stress-induced crystallization of the ferroelectric phase in HZO films, the reliability properties of metal-ferroelectric-metal (MFM) structures, scaling ferroelectric HZO films on silicon substrates, and their reliability. First, the driving forces for the crystallization of pure ferroelectric phase in HZO thin films were addressed and the role of the TiN top electrode in phase crystallization at low process temperatures (400 °C) is studied. Then, the reliability of 10 nm thick HZO films was studied, and the various

ferroelectric device reliability properties and mechanisms were evaluated for metal-ferroelectric-metal structures. Finally, the ferroelectric HZO films were integrated directly on silicon for Fe-FET applications and the effect of ferroelectric device reliability based on scaling HZO films on silicon structures was studied.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Based on the decadal plan published by the semiconductor research corporation (SRC) in October 2020[1], the memory/storage demands are expected to continue growing exponentially owing to increased memory requirements, internet of things (IoTs) and autonomous driving (just to mention some). To keep up with the increasing needs, developing memories with higher densities, speed and energy efficiency is necessary at different levels of the memory hierarchy (memory hierarchy shown in Fig 1.1). Until today, there is no memory that can operate in all levels of the memory hierarchy i.e., show non-volatility and significant memory density like the NAND flash at the same time show significant speed, low power and endurance like SRAMs and DRAMs.[1,2] To bridge the gap, storage class memories using a 3DXpoint phase-change memory (PCRAMs) were commercialized recently (in 2015) by Intel/Micron for memory requirements with a faster non-volatile read/write and higher endurance compared to NAND, but these memories could not replace the current DRAM or NAND flash technologies.

Therefore, there is a growing need for fast memory devices, that operate at low voltages and show non-volatility. Several emerging memories are being explored that can complement (if not replace) existing memory technologies. Among them, ferroelectric random-access memory (Fe-RAM) is one of the most promising candidates because of its fast low voltage operation and non-volatility. Since DRAM uses a dielectric for the memory operation (1-Transistor and 1-capacitor cell), it is a very straightforward approach to replace the dielectric with the ferroelectric material to realize Fe-RAMs. Additionally, using ferroelectric field-effect-transistors (Fe-FETs)

as a 1-T cell for data storage is also very advantageous because of its high-density and 3-D integration capability like NAND flash[1-2].

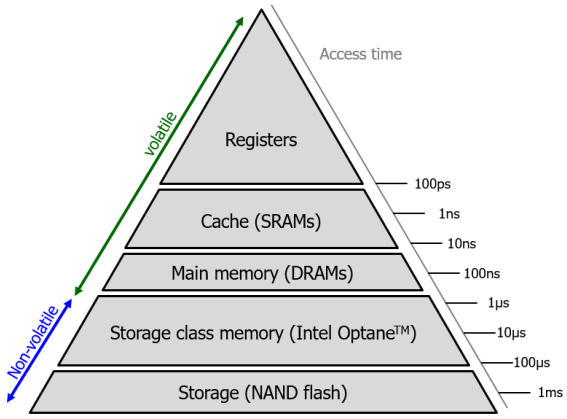

Figure 1.1: Memory hierarchy showing the different memory classes, their operation speed and memory retention capabilities (volatile or non-volatile). Adapted with permission from Ref [1] © 2018 IEEE.

However, several challenges and issues prevent the practical realization of ferroelectrics in state-of-the-art memory devices. Some of the critical challenges that need to be addressed are:[3-5]

(i) large polarization response (>15µC/cm^2).

(ii) scaling to sub-10nm thickness for low voltage operation.

(iii) low thermal budget (<450°C) for back-end-of-line (BEOL) integration.

(iv) endurance switching for >10^{12} cycles.

(v) stable lifetime (data retention and imprint) for 10-year operation.

(vi) Complementary-metal-oxide-semiconductor (CMOS) compatibility,

(vii) minimized interface effects when integration on silicon/dielectrics

1.2 Structural and electrical properties of ferroelectrics

The molecular theory describing all crystalline systems and symmetries predicts that among the 32 crystallographic point groups (sub-divided into 230 space groups), there are 10 polar groups with a unique polar axis and without an inversion center (non-centrosymmetric)[3]. This means that there are certain classes of crystals in which certain atoms can be present in two equilibrium sites in the lattice. These crystals can show spontaneous polarization in the direction of the polar axis if these ions are displaced between the two equilibrium sites (the displacement can happen based on mechanical stress, temperature, and electric fields). If the spontaneous polarization can be re-oriented and reversed by applying a sufficiently large electric field, then the material system is said to be "ferroelectric" [3-7]. The remnant polarization persists even after the applied field is removed, making it a viable option for non-volatile memory storage. It should also be noted that not every polar crystal is ferroelectric. For example, the wurtzite structure is polar, but it cannot be reoriented at known experimental electric fields[6].

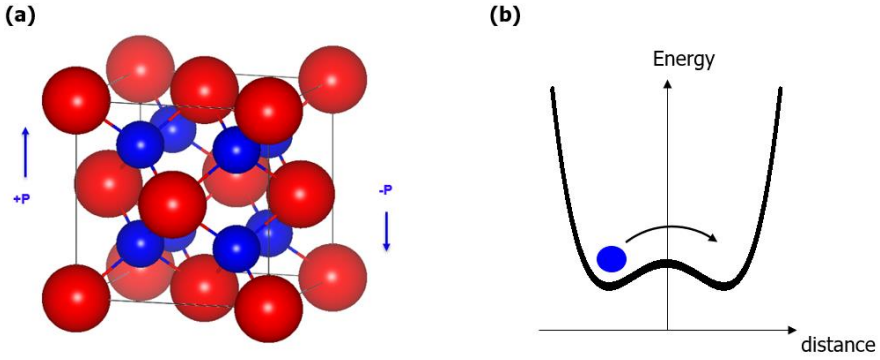

Figure 1.2: (a) An example of a non-centrosymmetric space group (with distorted fluorite structure) that can exhibit ferroelectricity by the displacement of blue ions. (b) a double-well energy vs. distance profile where the dip in energies represents the two stable polarization states in the ferroelectric.

In the case of regular dielectrics, the two main reasons for polarization due to applied electric fields are (i) electronic polarization, which arises because the applied electric field shifts the center of the charge of the electron shells from the nucleus and (ii) ionic polarization, which originates from the fact that the cations and anions in the lattice also displace due to the applied electric field. The amount of polarization obtained depends on the dielectric susceptibility of the material. In ferroelectric materials, if the applied field exceeds the coercive field (E_c), there is an additional spontaneous polarization from the dipole and domain wall motion. Ferroelectric materials have this additional "orientation polarization," [7] which is dependent on the electric field. Figure 1.2 (a) shows an example of a non-centrosymmetric distorted fluorite structure that can exhibit ferroelectricity by the displacement of blue ions, and Figure 1.2 (b) the energy profile of the ferroelectric switching process where the two stable polarization states of the displaced atoms.

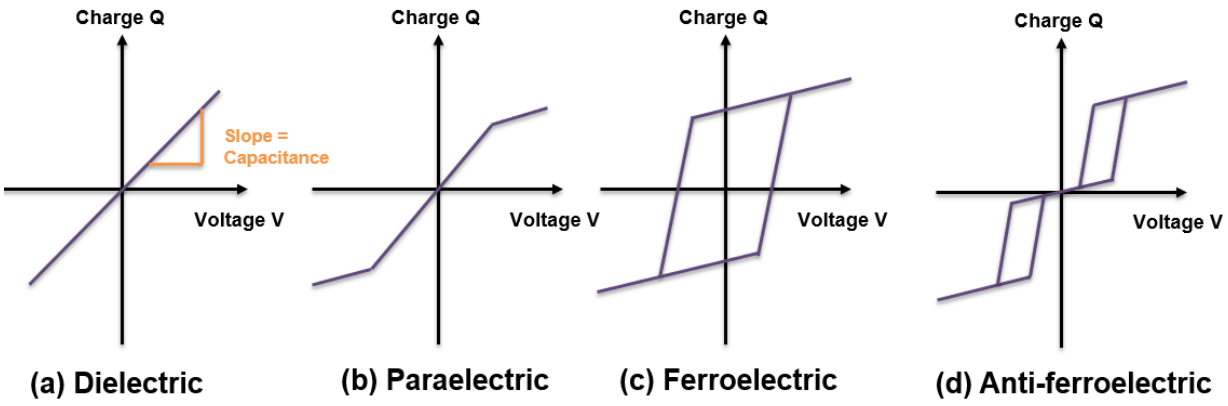

Figure 1.3: (a) The Charge-Voltage response of a linear dielectric, (b) The Q-V characteristics of a paraelectric. A paraelectric material does not show any spontaneous polarization, (c) The Q-V response of a ferroelectric. Spontaneous polarization is observed, (d) The Q-V response of an anti-ferroelectric. An anti-ferroelectric shows double hysteresis loop with no remnant polarization.

The charge in a ferroelectric material can be represented from Maxwell's first equation[6] as :

$$Q = \varepsilon_0 \varepsilon_r E + P$$

where Q is the charge obtained from the ferroelectric, $\varepsilon_0 \varepsilon_r E$ is the dielectric contribution to the obtained charge and "P" is the charge gained due to ferroelectric dipole motion. ε_0 is the permittivity of free space which is equal to $8.854 \times 10^{-12} \frac{F}{m}$ and ε_r is the relative permittivity of the material. E is the electric field in $\frac{V}{m}$. Figure 1.3 shows the different polarization (charge)-voltage responses of a dielectric, paraelectric, ferroelectric and an antiferroelectric material.

1.3 Conventional Ferroelectric Materials

Ferroelectricity was first discovered in Rochelle salts ($NaKC_4H_4O_6 \cdot 4H_2O$) by Valasek in 1921.[8] Valasek noticed that the remnant polarization can be switched by the application of an electric field (analogous to the magnetization of a ferromagnet by the application of a magnetic field) and coined the term "ferroelectrics". Rochelle salts then started to be widely studied in academia but failed to have a practical application because it was soluble in H_2O and has a very low Curie temperature, just above room temperature (Curie temperature is the temperature above which a material phase transforms from a ferroelectric phase to a non-ferroelectric phase).[9-11] The first ferroelectric to have practical application was $BaTiO_3$ (BTO) and was commercialized during the 1950s as a transducer material.[12] Since then, ferroelectricity has been intensively studied for use in various applications including Fe-RAMs for non-volatile memory as it can exhibit spontaneous polarization.[13-15] Most of the commonly known ferroelectric materials have a perovskite structure with ABO_3 structure. Lead-Zirconate-Titanate ($Pb(Zr,Ti)O_3$) and BTO are the most studied ferroelectric ceramics. As of today, embedded planar capacitor FRAM cells

using PZT are embedded in the complementary metal-oxide semiconductor (CMOS) process flow at the 130 nm node[16]. In this technology, 70 nm thick PZT films were accessed using a 1-Transistor cell (1-T 1-C structure) and operate at 1.5 Volt[16]. Scaling below the 130 nm technology node was very difficult because these films were very difficult to integrate with 3-D structured silicon substrates. Atomic Layer Deposition (ALD) technique is desirable to grow films in trenches and on 3-D structures as it is a sequential layer-by-layer chemical reaction on the surface. However, it is challenging to develop an ALD process for PZT thin films because of the relatively larger size of Pb. Also, since these materials are relatively thick (>70 nm), the integration of these films in the current technology nodes (sub-10 nm) is almost impossible since the ferroelectric properties suffer drastically as devices scale down below 50 nm because of the depolarization fields generated during integration with semiconductors or insulators.[17,18] Therefore, to realize commercial ferroelectrics in the sub-10 nm technology nodes, there is a need to realize ferroelectric properties in ALD deposited thin films. The recently discovered ferroelectricity in HfO_2 thin films discussed in the next section paves the way to realize the commercialization of FeRAMs or FeFETs in the current technology nodes.

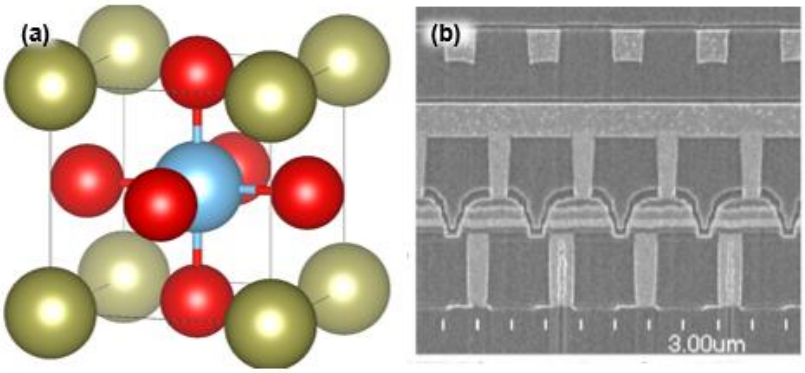

Figure 1.4 : (a) A perovskite PZT ferroelectric unit cell. The atoms in the center (in this case, titanium) is non-centrosymmetric and is responsible for the ferroelectric switching charge. (b) show the device structure and cross sectional TEM image of commercialized FeRAMs from Texas Instruments Inc using PZT at the 130 nm node. Re-printed with permission from Ref [16] © 2018 IEEE.

1.4 Ferroelectricity in doped HfO_2 thin films

In 2011, ferroelectricity was first discovered in doped HfO_2 thin films when trying to study high-k dielectric properties for DRAM applications[19]. The 10 nm thick HfO_2 thin films were doped with 3-5% of Si, and they showed ferroelectric properties with remnant polarization of ~10μC/cm^2. Since then, the ferroelectric properties of HfO_2 films with various dopants, including Zr, La, Gd, Y and Al [19-35] have been reported. In this dissertation, the word "dopant" essentially means alloying. The actual definition of doping is the addition of impurities in ppm or ppb, but the ferroelectric/ALD community often use the term "doping" for alloying and hence, a similar terminology is followed in this dissertation. Especially with ZrO_2 doping, the observed ferroelectricity drew lots of attention in the research community because the crystallinity of both the HfO_2 and ZrO_2 systems have been well studied and there was no indication of a ferroelectric phase in its equilibrium phase diagram, even at higher temperatures[36-38]. Moreover, both HfO_2 and ZrO_2 are some of the most studied material systems for more than half a century for

applications in refractory linings[36-38]. Figure 1.5 shows the equilibrium phase diagrams of the HfO_2-ZrO_2 bulk systems showing stable monoclinic (-M) till ~800 °C and tetragonal (-T) / cubic (-C) phases at higher temperatures. These systems have also been extensively studied for the past 15 years for applications as a high-k gate dielectric in Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) and DRAM applications,[39] but somehow, the ferroelectric phase remained hidden until a decade ago. The reported crystal structure that was observed in the ferroelectric HfO_2 was the orthorhombic phase with Pca21 space group.

Various factors were found to be responsible for the formation of this orthorhombic phase in HfO_2 thin films, doping[19-35], annealing temperature[25,40], electrode stress[41,42], surface energy[44] and ferroelectric film thickness[45,46] were found to be some of the most important "knobs" in realizing the ferroelectric phase in HfO_2.

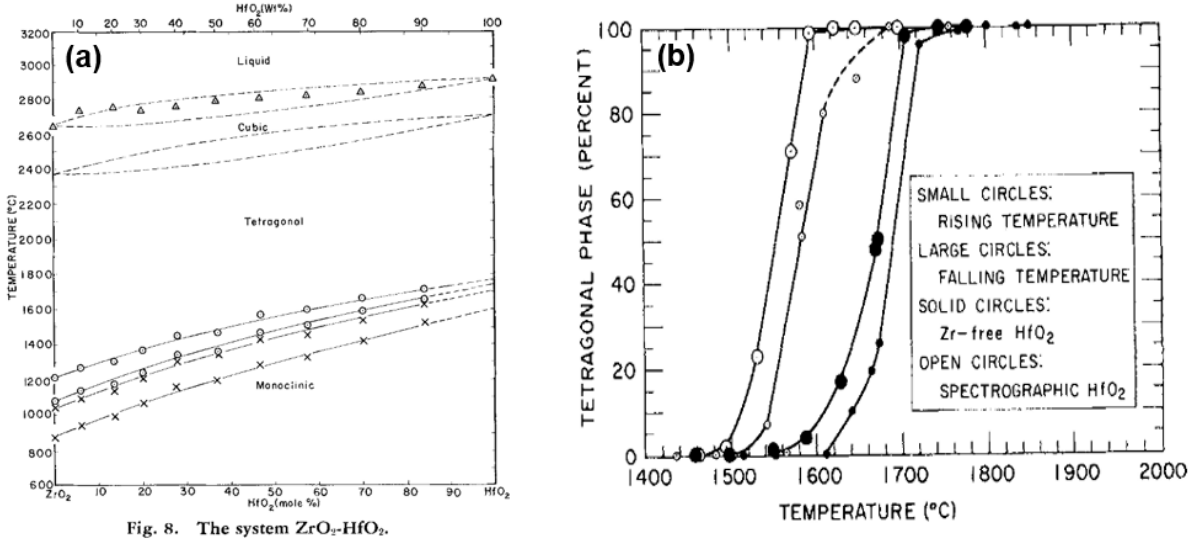

Fig. 8. The system ZrO_2-HfO_2.

Figure 1.5: (a)The equilibrium HfO_2-ZrO_2 phase diagram obtained using high temperature X-Ray Diffraction. Reprinted with permission from Ref [38]. Copyright (1963) Wiley, (b)diffusion less phase transformation in bulk HfO_2 (caused by rapid cooling) still shows very stable monoclinic phase to 1400°C Reprinted with permission from Ref [36]. Copyright (1963) Wiley.

It should be noted that to get the ferroelectric phase, the doping concentration is lower than 10% for most of the dopants. Controlling the composition for such low doping concentration is very difficult using ALD, but for Zirconium oxide, the best ferroelectric properties that were reported had a composition of ~50% ZrO_2. Hence, Hafnium Zirconate ($Hf_{0.5}Zr_{0.5}O_2$) a.k.a HZO can be easily deposited using ALD, since the deposition can be carried out just by depositing alternating cycles of Hafnium precursor pulse, oxidant, and Zirconium precursor pulse and oxidant.[27] Increasing the HfO_2 concentration makes the films crystallize to the equilibrium monoclinic phase (space group: $P2_1/c$) while increasing the concentration of ZrO_2 makes the films crystallize to the tetragonal phase (space group: $P4_2/nmc$). Table 1.1 shows the summary of reported ferroelectric properties using different doping materials in HfO_2 thin films. Additionally, the best ferroelectric properties for HfO_2 thin films can be obtained at thickness of ~10 nm compared to PZT/BTO thin films (which need ~100 nm thickness) making 3-D integration and nano-structured templates highly possible using ferroelectric HfO_2. Compared to the bandgap of 3-4 eV for PZT[47] thin films, ferroelectric HfO_2 has a bandgap of ~5.5 eV[48] which can facilitate lower leakage currents and higher breakdown voltages for the 10 nm films. Also, HfO_2 and ZrO_2 (and TiN, which is the most used electrode for ferroelectric HfO_2) have been already used in the semiconductor industry for logic and DRAM applications[49] and hence ferroelectric HZO films can easily replace the current high-k dielectrics without significant process optimization.

Table 1.1: A table showing the various dopants in HfO_2 which results in a ferroelectric phase. Adapted from Ref [25]. Copyright (2015) Wiley.

Dopant	Si	Zr	Y	Al	Gd	Sr	La
Valence	+4	+4	+3	+3	+3	+2	+3
Atomic Radius	110	155	180	125	180	200	195
Theoretical Pr	41	50	40	48	53	48	N/A
Experiment Pr	24	17	24	16	12	23	45
Ec	0.8 - 1.0	1.0	1.2 - 1.5	1.3	1.75	2.0	1.2
Doping %	4	50	5.2	4.8	2	9.9	N/A
AFE	O	O	X	O	X	X	N/A

Another critical parameter that is responsible for the ferroelectric phase transformation is the mechanical stress/capping layer effect from the electrodes[41,42,43]. Various theoretical investigations have shown that stress is an important factor for the crystallization of the ferroelectric orthorhombic (-O) phase in HZO.

1.5 Ferroelectric terminologies and methods of measurement

Historically, all initial measurements on ferroelectrics were done using the method developed by Sawyer and Tower by using a reference capacitor with a much larger capacitance in comparison to the ferroelectric (so almost entire voltage drop happens across the ferroelectric)[50-51]. From the voltage drop across the linear capacitor, the charge across the ferroelectric can be obtained (by charge equality). The drawbacks of this measurements are (i) the entire voltage drop does not happen in the ferroelectric capacitor and (ii) the parasitic cable

capacitances become more significant in measuring small ferroelectric capacitors. Both the shunt and virtual ground methods offer better precision ferroelectric measurements.[52] Figure 1.6 shows the schematic circuit diagram of the sawyer-tower circuit, shunt method and virtual ground methods for the measurement of ferroelectric capacitors.

The shunt method uses a resistor (forming an R-C circuit) and measures the voltage drop across the resistor to acquire the instantaneous current, *i* produced by the applied voltage (and hence charge $Q=i\cdot dt$) where dt is the time to obtain ferroelectric charge. All pulse WRITE/READ measurements discussed in later sections are measured using this method to calculate the charge obtained purely by dipole motion in the dielectric. The virtual ground method is the most precise of all the methods and uses an operational amplifier and a feedback resistor to calculate the charge across the ferroelectric. All P-E hysteresis measurements done using a Keithley 4200-SCS use this method to extract charge.

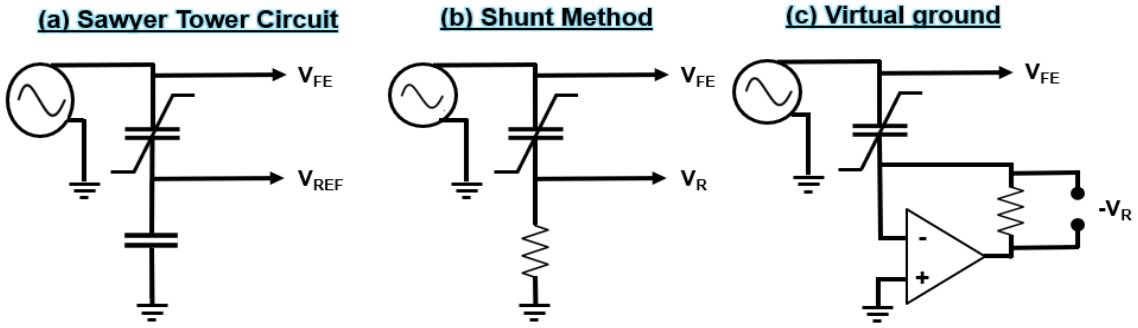

Figure 1.6: Various methods to measure the ferroelectric hysteresis. (a) shows the traditional Sawyer tower circuit, (b) Shunt method and (c) Virtual ground method [22]. V_{FE} is the voltage across the ferroelectric, V_{REF} is the voltage across a reference capacitor of very high capacitance, V_R is the voltage across a resistor.

The typical P-E hysteresis obtained by ferroelectric switching is shown in figure 1.7 At 0 Volt, the height of the ferroelectric hysteresis is called 2×remenant polarization ($2P_r$) and the

width of the ferroelectric hysteresis at charge 0 (i.e, at the middle of ferroelectric switching) is called 2×coercive field ($2E_c$). The voltage at which the switching process starts to saturate is called saturation voltage (V_{sat}). It should be noted that once the switching process is done, if an additional voltage pulse is given in the same direction (usually called a non-switching pulse), the response of the ferroelectric is like that of a normal dielectric (as shown in Figure 1.7, b) provided the amount of depolarization fields or relaxation components are significantly lower. This behavior can help us extract the dielectric constant of the ferroelectric and the amount of charge obtained from dipole motion.

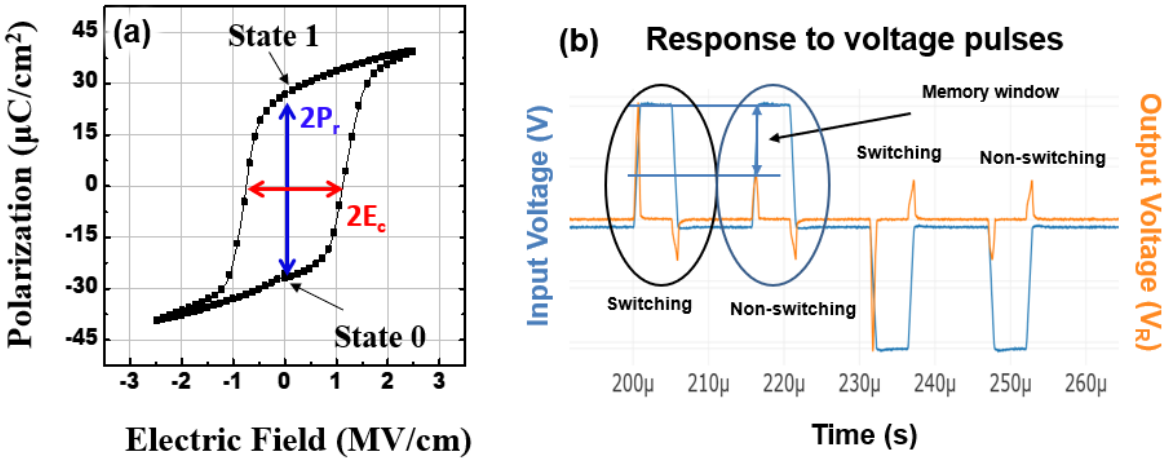

Figure 1.7: (a) An example of the P-E hysteresis obtained when triangular voltage pulses are sent to a ferroelectric, (b) an example of Positive Up Negative Down (PUND) measurement done using the shunt method demonstrating memory behavior in the ferroelectric.

1.6 Issues and challenges

Although ferroelectric HfO_2 has made way for various types of non-volatile memory devices, multiple issues and challenges prevent the commercialization of these devices. In most cases, the HZO films have a small fraction of the equilibrium non-ferroelectric -M phase that

crystallizes along with the ferroelectric phase.[53-56] The primary mechanism of the ferroelectric phase crystallization in HZO thin films is to anneal amorphous films in the presence of a capping layer (as shown in Fig 1.8) at high temperature to form the tetragonal phase (which is structurally very similar to the orthorhombic phase) and during cooling, the orthorhombic phase crystallizes out.[19,32,33,57]

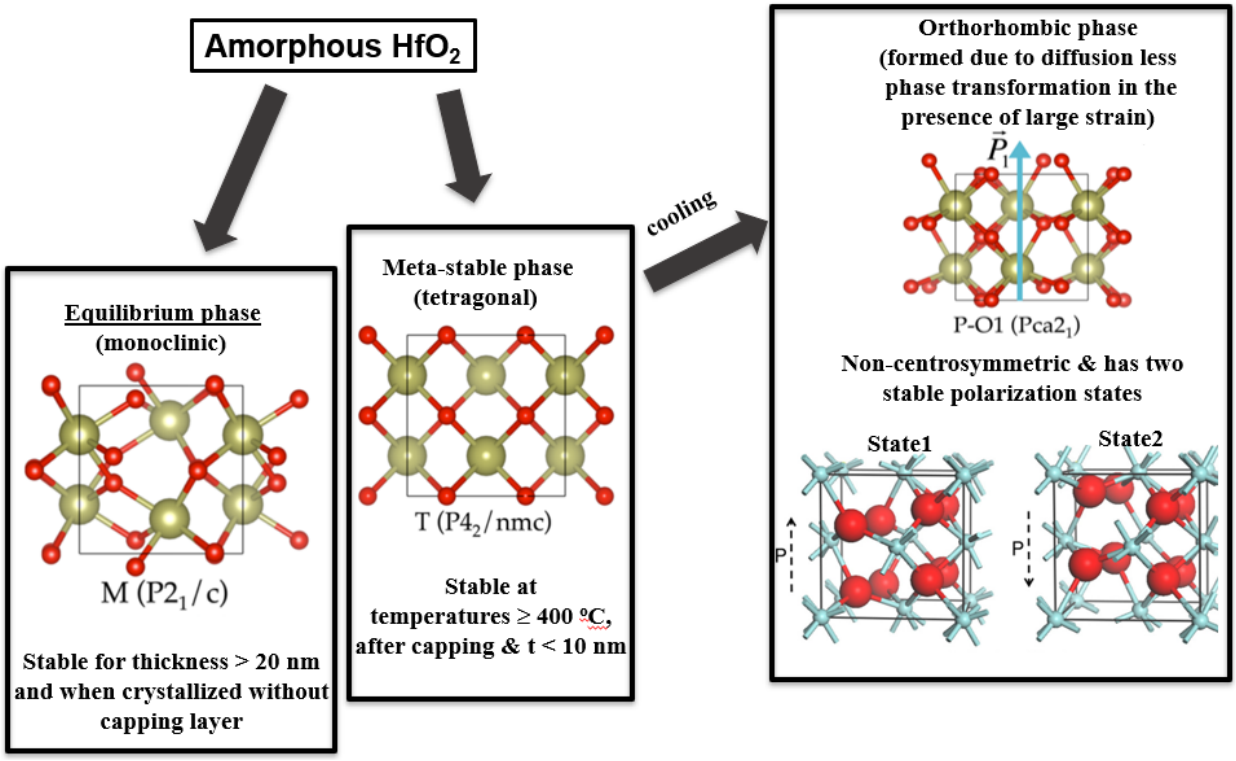

Figure 1.8: Ferroelectric orthorhombic phase crystallization mechanism for doped-HfO_2 thin films. Reprinted with permission from REF[19]. Copyright AIP Advances and REF[57]. Copyright (2017) American Chemical Society.

Hence, for the thickness range (5-20 nm) it is expected that the as-deposited HZO films are amorphous for proper crystallization of the -O phase. During the deposition of HfO_2 thin films, it is possible for the -M phase to crystallize even in as-deposited films for thickness ~10 nm.[57] Based on the literature survey of different precursors for HfO_2 and ZrO_2 deposition, for the

as-deposited films to be amorphous, the deposition temperature must be below 300 °C, without having significant contaminants (like halogen/carbon). The precursors ideal for this range are alkyl amide precursors and hence Tetrakis-dimethyl amido Hafnium (TDMA-Hf) and tetrakis-dimethyl amido Zirconium (TDMA-Zr) will be studied extensively in this work. The prevention of non-ferroelectric monoclinic phase formation in the film can significantly improve the device reliability. It is important to realize fully -O phase crystallization both on metal electrodes and silicon substrates for practical applications like FeRAMs and FeFETs.

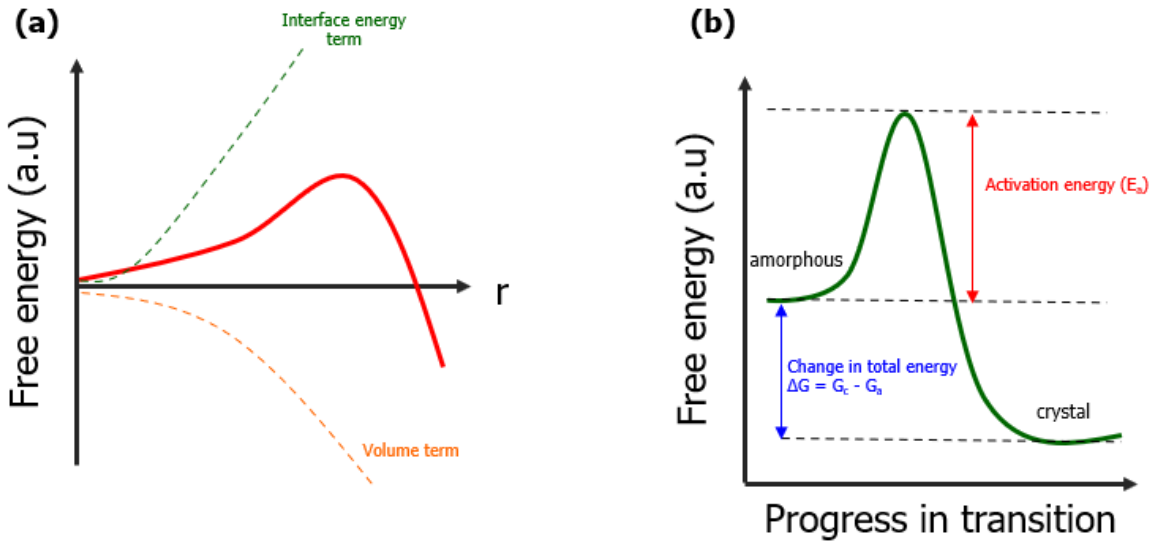

Figure 1.9: (a) the critical radius above which grain nucleation can occur in an amorphous film, and (b) a schematic of the activation energy required for amorphous to crystalline phase transition to occur.

Additionally, to realize low voltage operation, it is crucial to scale the ferroelectric layer thickness down, while maintaining the -O phase crystallization with similar ferroelectric properties. The influence of the HZO-electrode interface energy becomes more prominent when the film thickness decreases. For the crystallization process to occur, the activation energy/ energy barrier to crystalline the thin films should be overcome as shown in the Figure 1.9.

Another key challenge regarding ferroelectric HfO_2 memories is its reliability. Since Titanium Nitride (TiN) is the most commonly used electrode material for the formation of ferroelectric HfO_2, because of its thermal expansion coefficient and TiN is also considered very suitable for CMOS processing because of its thermal and chemical stability.[58-60] The main drawback of this however is its oxygen scavenging nature. TiN integrated directly on top of HfO_2 based high-k materials is well known to scavenge the HfO_2 of its oxygen during its annealing process, resulting in a defect rich HfO_2 film. Additionally, the scavenged O binds with the TiN film to form a TiO_xN_y interface. This TiO_xN_y interface (also called a non-ferroelectric dead layer) is usually rich in defects and oxygen vacancies, given its stoichiometry.[61,62]

The polarization-electric field (P-E) loop of a ferroelectric HfO_2 material usually shows a "pinched" hysteresis loop in its pristine state. This characteristic is mainly attributed to the presence and accumulation of defects at the HZO layer and interface.[63-67] These defects are caused because of the scavenging nature of the TiN electrodes and from the fabrication process. Hence, these defects are almost unavoidable in ferroelectric HZO.[68] Moreover, the presence of defects and oxygen vacancies at the ferroelectric layer and the electrode interface can significantly degrade the reliability properties of a ferroelectric like endurance and data retention [69-76]. Hence, engineering the HZO ferroelectrics to achieve a lower defect concentration both in the layer and at the electrode is crucial. In commercialized PZT ferroelectrics, it was reported that using a conductive oxide electrode (RuO_2 or IrO_2) reduces the oxygen vacancy formation at the PZT layer and at the electrode-PZT interface.[77-79] However, using a conductive electrode as the top electrode in ferroelectric HZO crystallization did not aid the -O phase formation because of its thermal expansion and the low stress received by the HZO layer. It is also shown

theoretically that an increase in oxygen vacancy concentration in HfO_2 also reduces the free energy for the crystallization of the -o phase.[58] Too many oxygen vacancies lead to reliability issues and too little oxygen vacancies can lead to the formation of the undesirable -m phase. Hence, a delicate equilibrium has to be achieved to obtain reliable ferroelectric properties.

Additionally, during integration of the ferroelectric HZO layer on top of 1 nm SiO_x (this 1 nm SiO_x is inevitable during the integration of high-k dielectrics on a silicon substrate), the polarization switching from the ferroelectric is compensated by a dielectric layer instead of a metal electrode. This charge compensation between HZO and the SiO_x layer (dead layer) leads to the generation of a depolarization field (built-in field) in both the layers.[80-82] This built-in field can lead to drastic reliability issues in ferroelectric device performances on top of silicon substrate. Some additional negative effects of this non-ferroelectric dead layer are the reduction in polarization, drastic fatigue, increased ferroelectric coercive fields and generation of built-in fields.[83-85] Hence, it is crucial to properly understand the charge matching between the two layers and to minimize the thickness of the interface SiO_x.

1.7 Dissertation Outline

This dissertation considers some of the challenges and issues illuminated in the above section and aims to push the understanding and commercialization of ferroelectric HfO_2 one small step further. This dissertation mainly focuses on three areas:

(1) crystallization of the ferroelectric -O phase in HZO at low temperatures (<400 °C) and scaling the HZO layer for low voltage operation is discussed and the ALD scaling of HZO in MFM capacitor structures in CHAPTER 3, (2) the reliability issues (data retention, imprint, fatigue and time-dependent-dielectric-breakdown) of 10-nm HZO films on metal-ferroelectric-

metal structures in CHAPTER 4, and (3) the effect of scaling ferroelectric HZO films on silicon substrates on the reliability and built-in fields in CHAPTER 5,

The first part of CHAPTER 3 focusses on uniform -O phase crystallization in thin HZO films at low process temperatures (<400°C) and proper understanding of the role of the TiN electrodes and the crystallization annealing in the crystallization of the ferroelectric -O phase. The second part of CHAPTER 3 focuses on scaling the thickness of the HZO layer on metal-ferroelectric-metal structures to realize low voltage operation and the effect of TiO_xN_y interfaces and annealing temperatures on scaling,

CHAPTER 4 focusses on the reliability issues in 10 nm HZO ferroelectric thin films and efforts to understand the reliability mechanisms and failure lifetime of ferroelectric MFM capacitors. In particular, the ferroelectric data-retention/ imprint studies and its failure mechanisms are clearly studied in HZO thin films.

CHAPTER 5 focusses on the scaling of HZO thin films on silicon substrates and reducing the effective EOT of these MFIS capacitors to achieve low voltage operation. Additionally, the effects of interface SiO_x on the ferroelectric reliability and built-in field are studied.

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CHAPTER 2

EXPERIMENTAL METHODS

2.1 Deposition Techniques and annealing tools

2.1.1 Atomic Layer Deposition (ALD)

ALD is a thin film deposition technique and is very popular in the semiconductor industry because of its precise thickness control, conformality and uniformity[1]. ALD enables the deposition of a wide variety of oxides, nitrides and even some metals with high conformality, even on high aspect ratio trenches due to its surface limited chemical reaction[2].

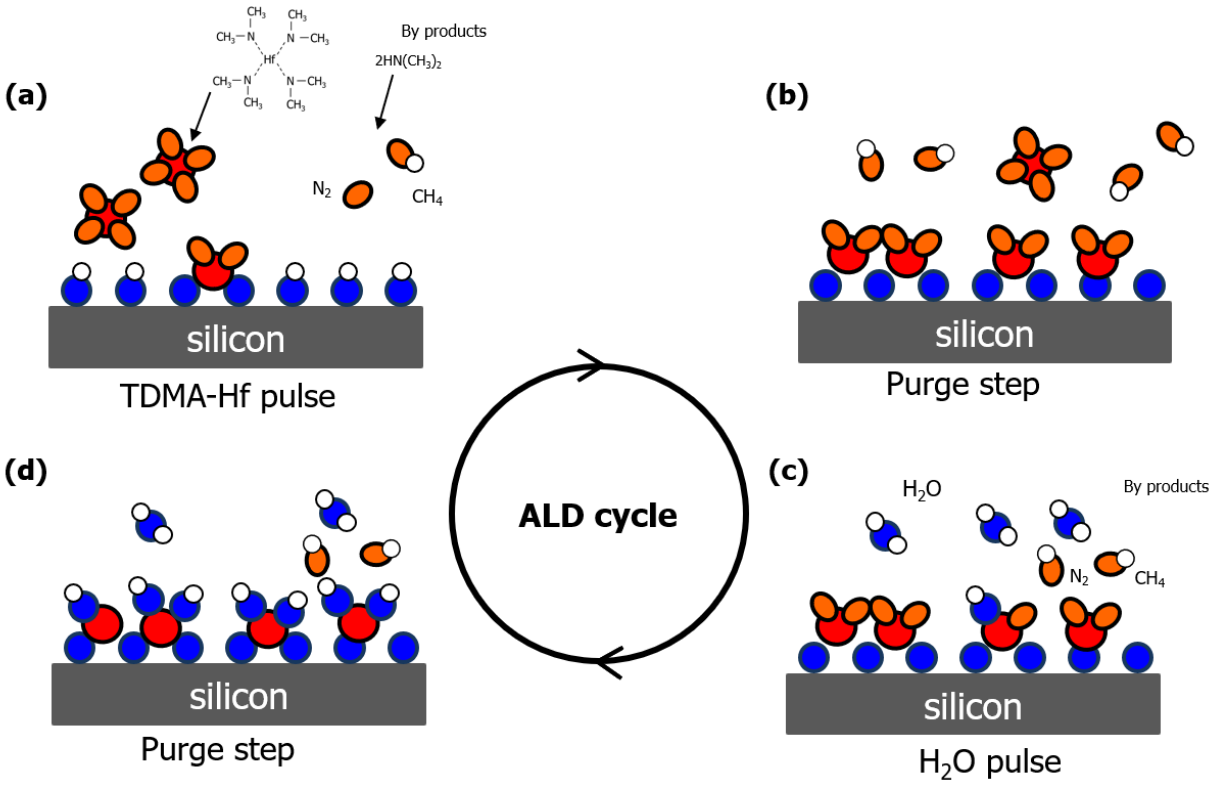

Figure 2.1: A schematic diagram of the surface reactions in one cycle of ALD deposition using TDMA-Hf and H_2O as the metal precursor and oxidant respectively.

To deposit a metal oxide using ALD, a minimum of two precursors are required: a metal precursor and an oxidant. Metal halogen (like $HfCl_4$) and metal organic (like TDMA-Hf) precursors are commonly used because of their self-limiting non-reactivity with themselves. Typical oxidants used are O_3 and H_2O, but oxygen plasma is also used in plasma enhanced ALD depositions, but in this work only thermal ALD of $Hf_{0.5}Zr_{0.5}O_2$ films will be discussed. The deposition chamber is heated up (250°C for HfO_2 deposition using TDMA-Hf) to ensure self-limiting saturated deposition takes place within the ALD window of the precursor. One full ALD cycle for HfO_2 deposition involves 4 steps as shown in Figure 2.1.

(i) 1st precursor (TDMA-Hf) pulse : In this step TDMA-Hf is pulsed into the chamber. Since the vapor pressure of the precursor very low at room temperature, the precursor must be heated (65 °C) to ensure the proper delivery of the precursor gas to the reaction chamber. The TDMA-Hf vapors are delivered using an inert Argon carrier gas. Once the TDMA-Hf vapors enter the chamber, a surface reaction with the existing -OH bonds (surface active sites) takes place to form Hf-O bonds, and the reaction stops once reaction has occurred on all the -OH bonds on the surface.

(ii) 1st inert gas purge: In this step, the by-products of the surface chemical reaction and the remaining TDMA-Hf precursor in the chamber are flushed out by purging the chamber with the Ar inert gas to avoid any gas phase chemical vapor deposition (CVD) on the surface.

(iii) 2nd precursor pulse (H_2O) pulse : H_2O molecules are pulsed into the chamber and these molecules react with the TDMA-Hf molecules chemisorbed on the surface. This reaction occurs until the reaction happens on all the chemisorbed TDMA-Hf surfaces to form HfO_2.

(iv) 2nd inert gas purge: Similar to step 2, both the by-products of the chemical reaction and the residual H_2O molecules are completely purged out of the chamber by using inert gas to avoid any contaminants or CVD type reactions.

Similar to the above technique, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) is deposited using a super cycle of TDMA-Hf, purge, oxidant pulse, purge, TDMA-Zr pulse, purge, oxidant pulse and purging steps for multiple cycles. These steps can be repeated continuously until the desired thickness is achieved. In this work, high purity, high concentration O_3 generated (400 g/m^3) using a TMEIC ozone generator is used as the oxidant because it has a much higher reactivity compared to H_2O. The growth per cycle (GPC) for the super cycle of HZO is ~0.2nm. Hence the deposition of 10 nm of HZO needs 50 supercycles. To ensure proper ALD reaction, TDMA-Hf/TDMA-Zr pulse time of 0.2 seconds, purge time 20 seconds and a O_3 pulse time of 0.03s and purge time of 10 seconds was used in this study.(the ALD valve tool specification says the shortest possible open/close time is 0.03s, but practically the communication delay between the controller and the ALD valve can result in the pulse time being a little longer). The deposition temperature was set to 250 °C to ensure minimized carbon contamination from the TDMA-Hf precursor and to make sure the ALD reaction is within the ALD window for the precursor reaction on the surface. Figure 2.2 shows the photograph of the Cambridge Nano-Tech system (CNT) used to deposition $Hf_{0.5}Zr_{0.5}O_2$ thin films.

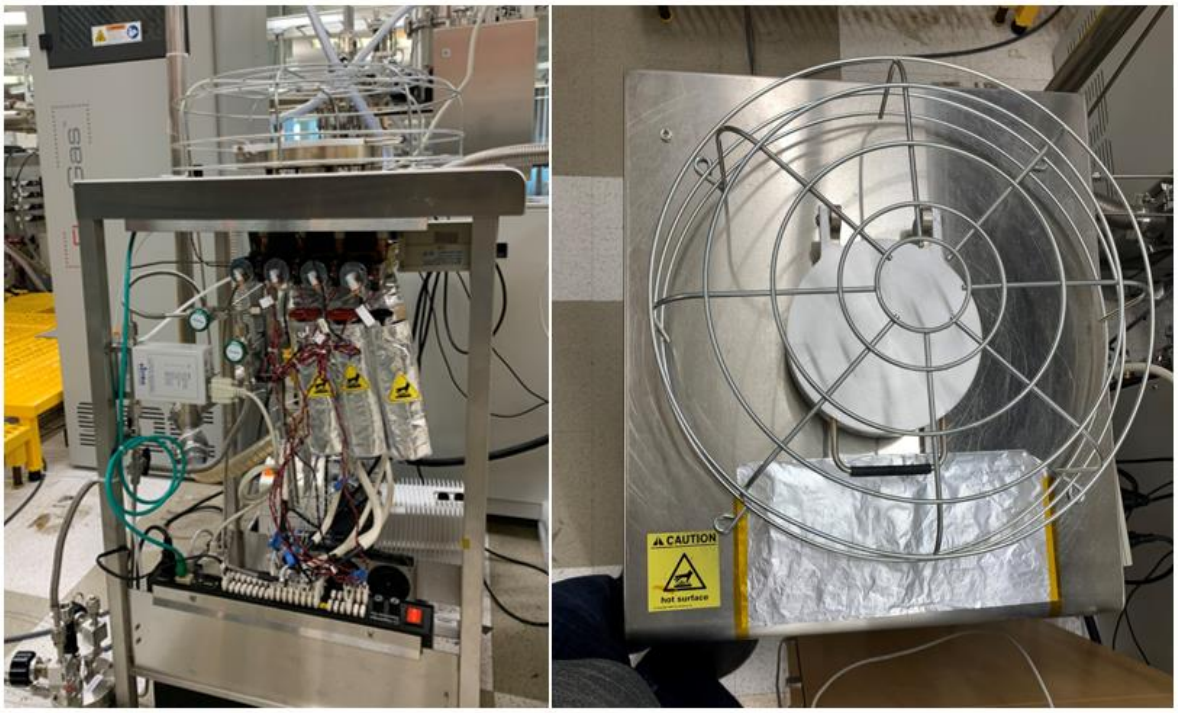

Figure 2.2: A photograph of the ALD cross-flow reactor chamber (Cambridge Nano Tech Savannah S100) with 4 precursor manifolds which can accommodate a 4" (100mm) wafer.

Although the ALD process has various advantages, its limitation is that it is very time-consuming deposition process.

2.1.2 RF Magnetron Sputtering

Unlike the ALD process in which the deposition is due to a chemical reaction, sputtering is a physical vapor deposition (PVD) process. In sputtering, the target material to be deposited is bombarded with energetic ions of a gas (Argon in this study). These energetic ions are a consequence of the plasma on the target surface. The forceful collision of the energetic Ar^+ gas with the target material ejects the target material into the chamber leading to film deposition.[3]

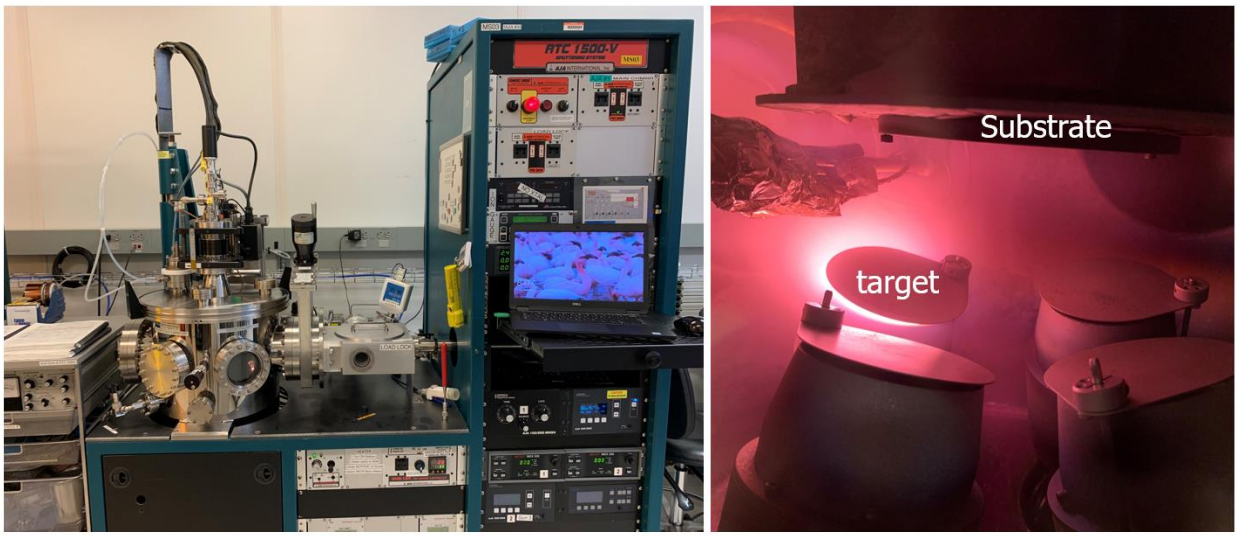

Figure 2.3: AJA 1500V sputtering tool common user facility in the UTD cleanroom with 4 installable targets at one time.

Figure 2.3 shows the AJA 1500V sputtering tool used in this study which is housed at the Cleanroom Laboratory (CRL). Traditional DC sputtering is commonly employed to deposit pure metals (Like Au, Pt etc.). However, for depositing materials that are not as conductive as pure metals, radio frequency (RF) sputtering is a commonly employed technique, as it prevents charge build up in the target materials. RF sputtering involves an alternating potential (usually at a frequency of 13.56MHz) between the cathode (target material) and the anode (substrate) to prevent a charge build up in the film which can over-time lead to plasma-arcing, which spews out droplets of metal causing film uniformity, thickness, and quality issues.[3-4]

To initiate a plasma, a high voltage is applied between the target and the substrate with the chamber at a higher base pressure compared to the working pressure (a greater number of gas molecules is needed to ignite the plasma). The electrons present in the gas are accelerated due to the applied voltage and cause collisions between the gas molecules, thereby knocking off

electrons from the sputtering gas atoms (Ar gas becomes Ar^+ ions). These Ar+ ions are accelerated towards the cathode (target material) leading to sputter deposition of the film. Using magnets under the target surface confines the electrons in the plasma at or near the surface leading to a higher density plasma and increased deposition rates (called magnetron sputtering).

Introducing a reactive gas (such as oxygen or nitrogen) in the chamber in the sputtering environment can permit deposition of oxide or nitride films. By using reactive sputtering, stoichiometry control can be achieved in the deposited film. In this work, the sputtering process was used to deposit the metal electrode and most of the work done was using titanium nitride (TiN) as the electrode. By introducing nitrogen gas in the sputtering chamber and using a titanium target, TiN deposition can be achieved. During reactive sputtering, it is critical to control the partial pressure of the reactive gas introduced in the chamber. Increasing the reactive gas flow rate will transition the outermost surface of the metal target from a metal to a "poisoned" state (surface oxidation/nitridation).[5-6] The poisoned state can lead to plasma stability issues and plasma arcing, leading to reduced quality of the deposited film. If the surface is pure metal (very low gas flow rate), then the result will be the deposition of a sub-stochiometric film. Hence, proper control of the reactive gas flow rate and chamber pressure is critical to ensure that the target surface is kept in a transition state between metallic and poisoned state for the deposition of a stochiometric film.

Additionally, for the deposition of TiN which is conductive, it is crucial that the oxygen partial pressure in the chamber remain as low as possible (to prevent the deposition of TiO_xN_y). Hence, before every sputtering of TiN, the empty chamber is sputtered with titanium to getter all

the oxygen present in the chamber. This process is repeated until the base pressure of the sputtering chamber is below 10^{-7} Torres.

2.1.3 Rapid Thermal Annealing (RTA) System

RTA systems are based on lamp-based radiation heating and these systems are very useful in short duration fast annealing processes at high temperatures (up to 1000°C).

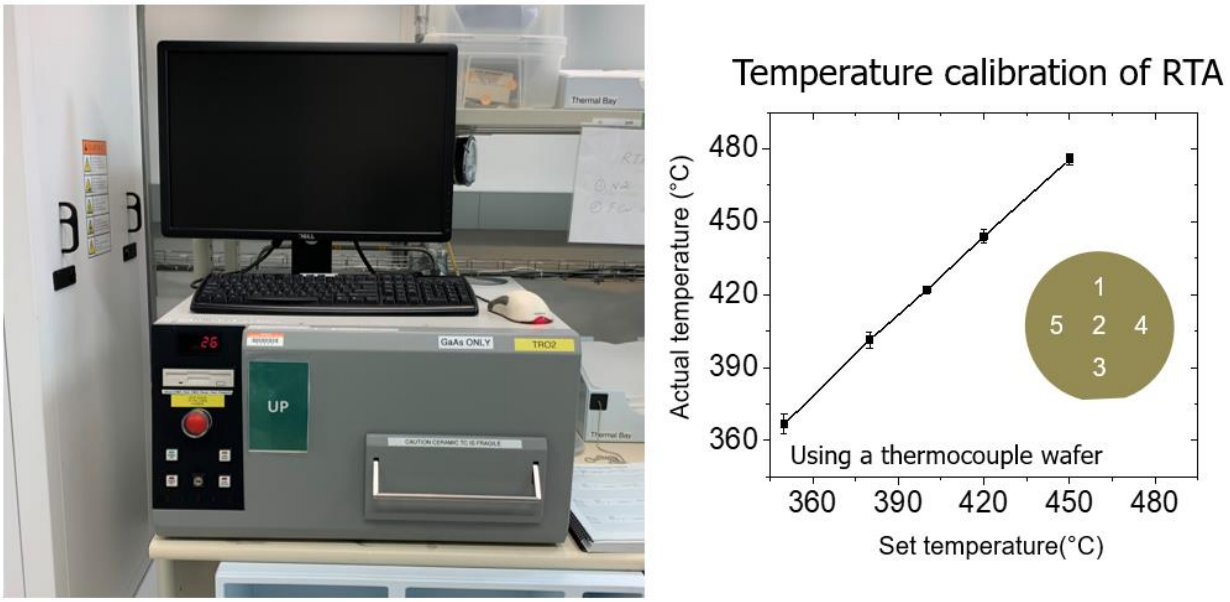

Figure 2.4: The MPTC RTP-600xp Rapid thermal processing system, can anneal up to 1000°C. The temperature calibration using a thermocouple wafer shows a ~20°C higher temperature compared to the setpoint with ~5°C variation across the 100mm wafer.

Figure 2.4 shows the photograph of the RTA system and the actual temperature vs set point between 350 °C and 450 °C. Standard RTA systems have a process chamber, gas inlet valves, heating lamps, an exhaust and a PID controller to control the temperature with temperature sensors. The annealing process performed in this work is usually on a structure with HZO and TiN layers.

RTA is very useful as TiN is very sensitive to O_2 and H_2O even in the ppm levels.[7] Using a furnace at atmospheric pressure (even at vacuum) for longer times can lead to oxidation of the TiN, making the electrodes insulating in nature. Using the RTA can control the annealing time to less than a minute, with high ramping and cooling rates up to a 100°C/sec to reduce the entire duration of the annealing process. Since the chamber is also equipped with N_2 gas, annealing the TiN films in N_2 ambient can significantly reduce the oxidation of the TiN films.

The problem with the RTA system however is the temperature controllability and uniformity across the wafer. Higher temperature (>600°C) annealing processes can lead to >10°C non-uniformity across the 100mm wafer.

2.2 Materials characterization tools

2.2.1 Grazing Incidence X-Ray Diffraction (GI-XRD)

X-ray diffraction (XRD) is the most effective tool to determine the long-range crystallographic orientation of materials at atomic resolution. Since the spacing of atoms in a lattice is higher than the wavelength of X-rays (Cu-Kα wavelength is 1.54Å), X-rays can be used to probe the interatomic spacing in the lattice, and based on the spacing of the material, information about the chemical composition and crystallographic nature (single crystal, poly-crystal or amorphous) of the species can be obtained. Based on Bragg's law, $n\lambda = 2d\sin\theta$, (where n is an integer, λ is the wavelength of the incident X-ray, d is the interatomic spacing, θ is the incident X-ray angle), when X-ray beam is incident on the material, constructive or destructive interference occurs due to the d-spacing of the planes and the structure factor of the material so that diffracted beams are obtained at different detector angles.[8]

Figure 2.5: An image of the Rigaku smart lab XRD system.

However, the penetration depth of X-ray is strongly dependent on the incident angle and moving the source to higher angles can lead to deeper penetration of the X-rays, and loss of information from the surface. Grazing Incidence XRD is commonly employed to measure thin films of <100 nm in thickness, where the incidence angle is kept fixed, and the detector is moved to collect diffraction information at different angles. Since the HZO film of interest is <20 nm in thickness, an incident angle of 0.2° is required to minimize the effect from the substrate but smaller incident angle lead to lower detector signal. Hence, an optimized incidence angle of 0.5° was used to detect the ordering in the near surface. The TiN top electrode is chemically removed using an etchant called SC1 (which contains NH_4OH and H_2O_2 in 1:1 ratio) and the crystallinity

of underlying HZO layer was studied using GI-XRD. Figure 2.5 shows a photograph of the Rigaku smart lab XRD system used for this study.

2.2.2 Transmission electron microscopy (TEM)

The TEM is a very powerful tool for the characterization of nanomaterials because of its high-resolution imaging and chemical analysis capabilities.

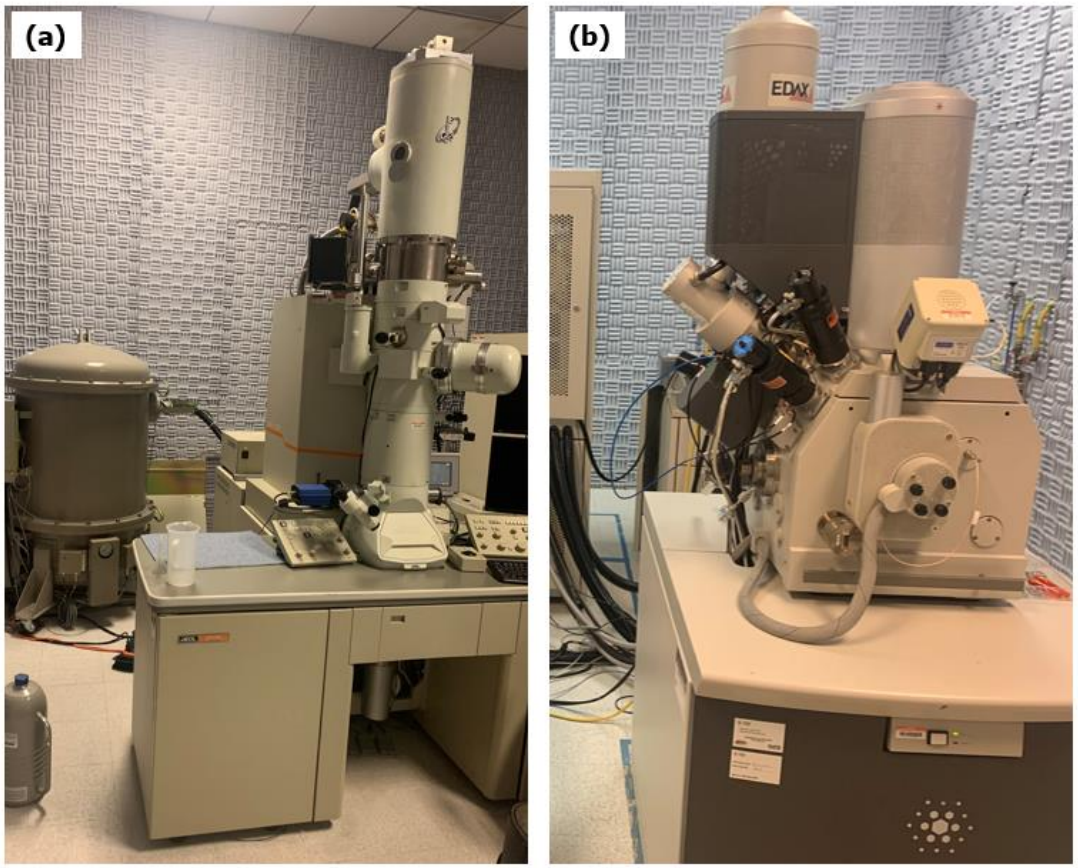

Figure 2.6: (a) an image of the JEOL-2100F transmission electron microscope with a resolution of 1.9Å and (b) an image of the FEI-focused ion beam/Scanning electron microscope tool used for TEM sample preparation.

High resolution imaging can be done using TEM using atomic resolution of ~0.2nm by using a very high energy (200kV) electron beam and aberration corrected electromagnetic lens.[9,10] According to de Broglie's relation,

$$\lambda = {}^{h}/_{(2mqV)^{1/2}}$$

where m and q are the mass and charge of the electron, h is planks constant and V is the accelerating voltage. Using a 200kV electron beam, the wavelength is 0.00251 nm corresponding to a spatial resolution of ~0.2 nm.

In TEM, the high energy electron beam is transmitted through a sample with electron transparent thickness (for inorganic oxide materials, the thickness should be <100 nm). In addition to a high-resolution measurement of thickness, the d-spacing of crystalline films can be physically observed since the resolution of the TEM is ~0.2 nm (which is lower than the d-spacing of lattices). In addition to this, because of the nature of electron interaction with materials (energy loss and X-ray generation), chemical analysis can also be done using TEM such as electron energy loss spectroscopy (EELS) and energy dispersive X-ray spectroscopy (EDS).

In this dissertation, HR-TEM is used mainly to observe structural and atomic resolution lattice imaging, as well as thickness measurements. Cross-sectional TEM samples with less than 100 nm thickness are prepared using the FEI-focused ion beam (FIB) lift-out technique. A protective platinum layer is deposited on top of the sample to prevent FIB damage and the captured images from the TEM are analyzed using the Gatan GMS 3 software.

2.2.3 Thin film stress measurement

Based on the change in curvature of the wafer before and after thin film deposition, the stress developed in the film can be calculated using Stoney's equation.[11]

$$\sigma_f = \left(\frac{Y}{1-\upsilon}\right)\frac{t_s^2}{6rt_f}$$

where, σ_f is the stress generated in the deposited thin film, t_s is the thickness of substrate, t_f is the thickness of the deposited film, r is the radius of curvature change in the wafer after the thin film deposition, Y is the young's modulus of elasticity of the substrate and υ is Poisson's ratio.

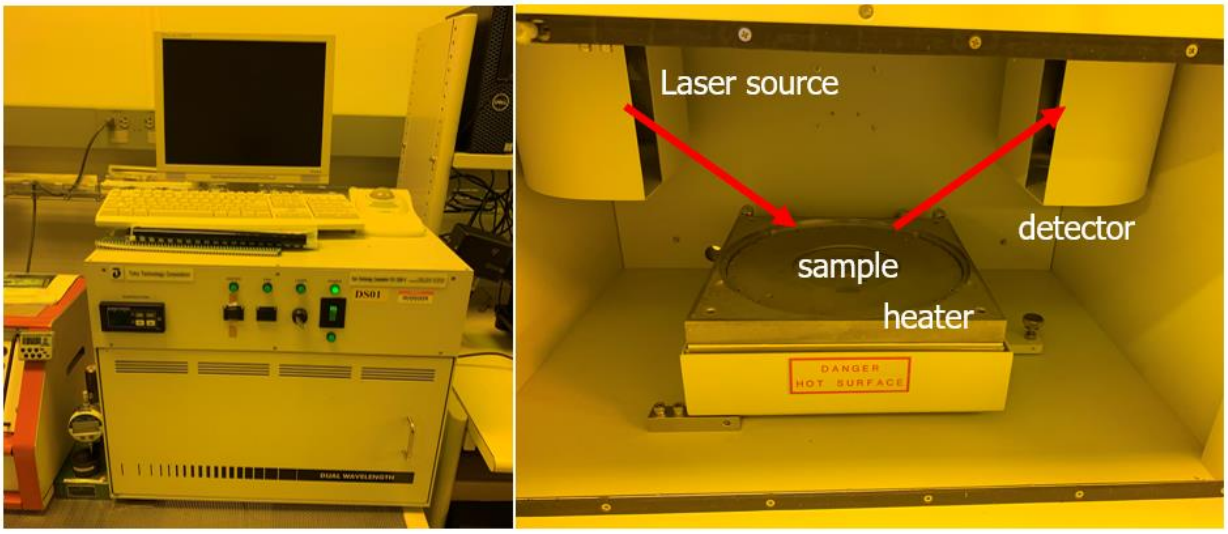

Figure 2.7: The toho FLX-2320 thin film stress measurement tool. The tool is equipped with a heater that has heating capability up to 500°C.

Figure 2.7 shows the photograph of the toho thin film stress measurement tool housed at the CRL laboratory used in this study. Laser light of wavelength of 680 nm is used to measure the amount of deflection change based on thin film deposition. Based on the change in curvature, the type and amount of stress generated in the wafer can be determined (concave change in curvature

means a tensile stress is present in the film and convex change in curvature means a compressive stress is present in the film). The key requirements for calculation of stress from Stoney's equation are:

(i) Blank wafers must be used, and the thin film should be deposited on the entire blank wafer (patterned wafer cannot be used).

(ii) The thickness of substrate must be very large compared to the thickness of film.

(iii) The wafer or film must be reflective to allow the laser to bounce back from the surface. Rough surfaces can lead to scattering and affect the measurement.

Additionally, the toho FLX-2320 thin film stress measurement tool also has a heating capability up to 500°C, and hence the stress evolution in the wafer can be studied based on temperature.

2.3 Device Fabrication

2.3.1 Metal-ferroelectric-metal (MFM) capacitor fabrication

The schematic of the MFM capacitor fabrication using TiN electrodes is shown in Figure 2.8. Thermally grown 300 nm SiO_2 (grown using wet oxidation) was used as a substrate to prevent parasitic resistance and capacitance components from the p-type silicon substrate and to isolate the MFM capacitor from the semiconducting substrate. A 90 nm thick TiN bottom electrode (BE) is deposited using room temperature RF magnetron sputtering. In most cases of the MFM fabrication process (unless mentioned otherwise), the fabrication process up to this step is the same. On top of 90 nm TiN BE, HZO was deposited using Tetrakis-dimethlyamido-hafnium ($Hf[N(CH_3)_2]_4$, TDMA-Hf), tetrakis-dimethylamido-zirconium ($Zr[N(CH_3)_2]_4$, TDMA-

Zr), and O_3 as the Hf-precursor, Zr-precursor, and oxygen source, respectively. The thickness of the HZO layer for the standard device was ~10nm and the variation in ferroelectric properties based on HZO thickness was also studied in this work. High concentration O_3 (400 g/m^3) used in this work was formed by an O_3 generator (OP-250H, Toshiba-Mitsubishi-Electric Industrial Systems Corporation (TMEIC)). The wafer temperature was set to 250 °C during HZO deposition and the growth per super cycle of HfO_2 and ZrO_2 was ~0.2 nm/super cycle. After the deposition of HZO, a 90 nm TiN top electrode (TE) was again deposited on top of the HZO layer using room temperature RF magnetron sputtering to form MFM capacitor stack. Two types of crystallization annealing processes were performed to study the role of the TiN top electrode; (i) Post deposition annealing (PDA), and (ii) Post metallization anneal (PMA). The PDA process was performed using the rapid thermal annealing (RTA) system immediately after HZO deposition and the PMA process was performed using RTA annealing after the TiN top electrode deposition. The RTA process was done between 300-500 °C in N_2 ambient. An E-beam evaporator was used to deposit Pd/Au (10nm/200nm) as a hard mask for a conventional lithography process. Wet-etching using SC1 etchant (NH_4OH:H_2O_2 in the ratio 1:1) was done to remove excess TiN and isolated capacitor structures with the global bottom electrode, as shown in Figure 2.8. Wet etching of the TE leads to the formation of undercut and hence the real area of the capacitor structures should be calculated.

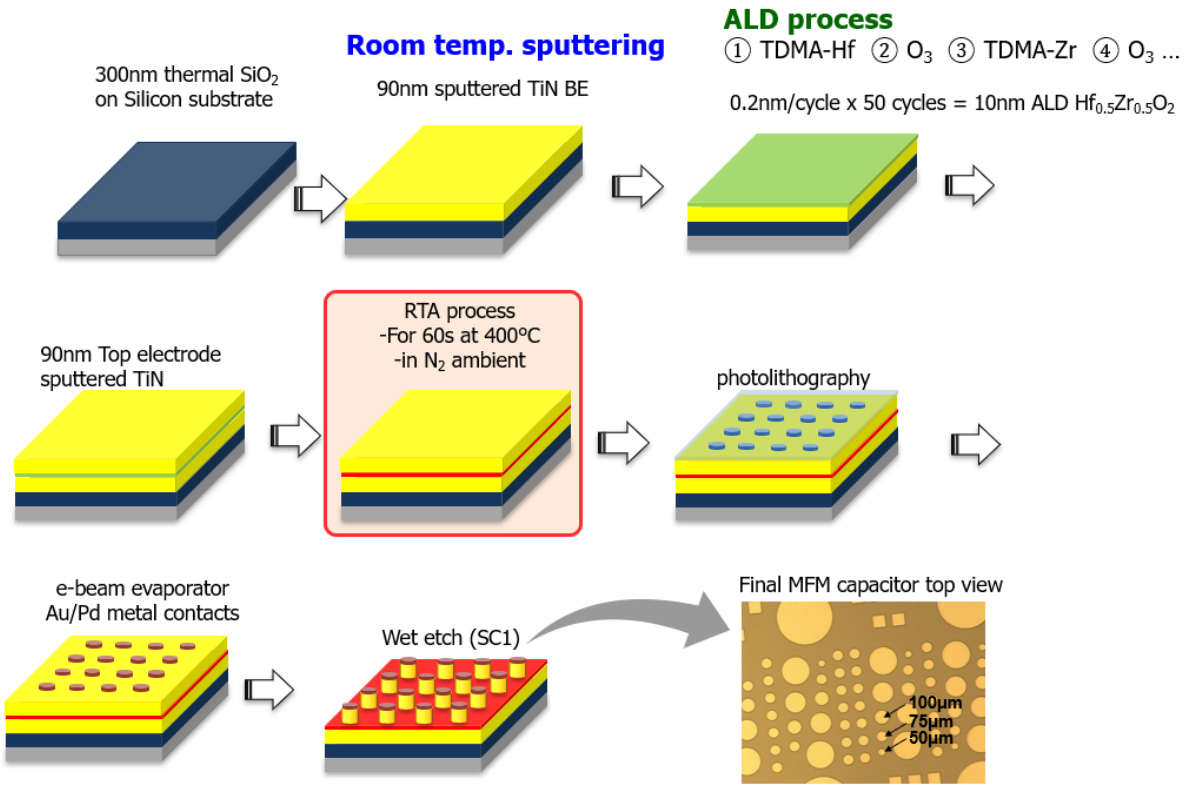

Figure 2.8: Process flow chart for the fabrication of MFM ferroelectric capacitors.

2.3.2 Metal- ferroelectric-insulator-semiconductor (MFIS) capacitor fabrication

The schematic of the MFIS capacitor fabrication is shown in Figure 2.9. p-type or n-degenerate silicon substrates were used as the semiconductor. The surface of the silicon wafer is cleaned using RCA cleaning procedure (mentioned in detail in chapter 5). Two types of processes including the HF last and the SC1 last process (forming 1 nm chemical oxide on the silicon surface) were used. The HZO was deposited using TDMA-Hf, TDMA-Zr and O_3 as the Hf-precursor, Zr-precursor, and oxygen source, respectively. The thickness of the HZO layer was studied scaling down to 2nm and the variation in ferroelectric properties based on HZO thickness was studied in this work.

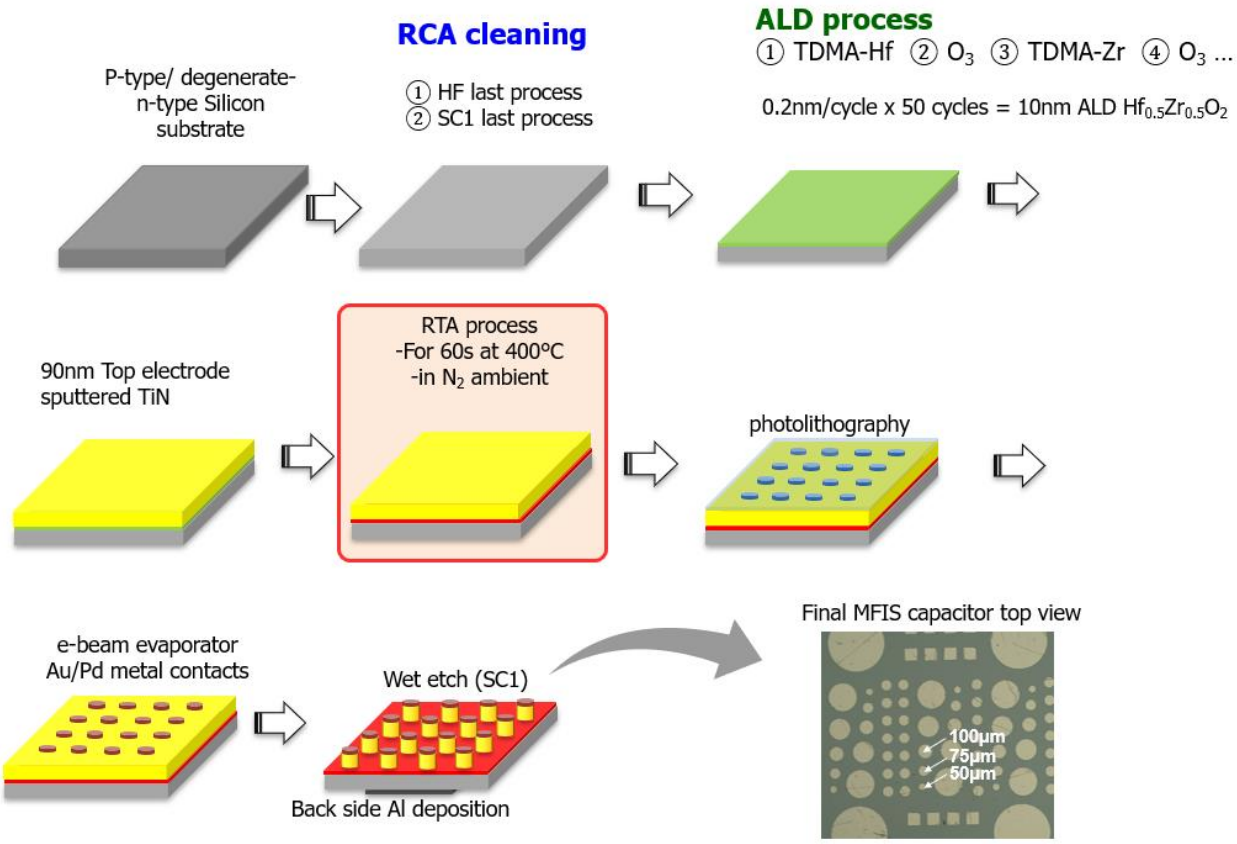

Figure 2.9: Process flow chart for the fabrication of MFIS ferroelectric capacitors.

The other steps, including 90 nm top electrode deposition, RTA process (300-600 °C in N_2 ambient), photolithography, hard mask deposition and etching are like the fabrication process of MFM capacitors. Aluminum is deposited on the back side of the silicon substrate so as to use the substrate to apply electrical bias/ground.

2.4 Electrical Characterization

2.4.1 Calculation of real capacitor area

After the wet etching process of the 90 nm TiN to form the capacitor structures, the formation of an undercut is unavoidable as shown in Figure 2.10. Hence, for accurate

measurement of ferroelectric properties in the capacitor structures, the real area must be calculated.

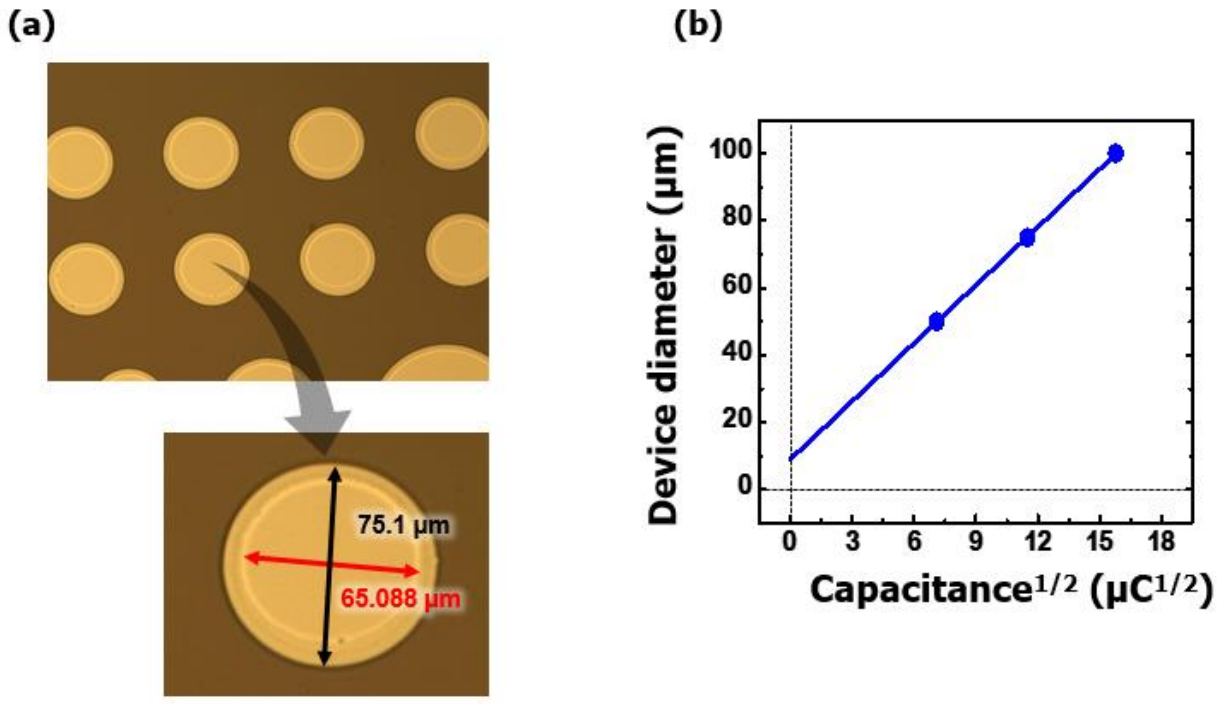

Figure 2.10: (a) optical microscopy image showing the formation of undercut (b) real area calculation to find the amount of over-etching.

The capacitance across a parallel plate capacitor filled with a dielectric material is given by,

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

$A = \pi r^2$ (for a circular capacitor)

where ε_0 is the relative permittivity in vacuum, ε_r is the relative permittivity in free space for the dielectric material used, A is the area of the capacitor metal pads (circular pads are used in this study) and d is the thickness of dielectric.

From this,

$$C = {\pi(real\ diameter - undercut)^2 \varepsilon_0 \varepsilon_r}/{4 \cdot d}$$

$$\text{device diameter} - \text{undercut} \propto \sqrt{C}$$

by plotting and linear extrapolation of $\sqrt{Capacitance}$ vs. device diameter obtained for three different device sizes as shown in figure 2.10 (the capacitance can be measured by small signal CV or large signal pulse measurements), the value of the real capacitor area (undercut value) can be found from the intercept of the plot.

2.4.2 Pulse measurements for the ferroelectric characterization

In this dissertation, the dynamic ferroelectric properties were analyzed using pulsed I-V measurements using a Keithley 4200 SCS semiconductor parameter analyzer and a pulse generator/oscilloscope setup. The pulse generator/ oscilloscope setup will be explained in detail in CHAPTER 4. The Keithley 4200 SCS has a model-4255 pulse measurement unit (PMU) module with two 4255- remote amplifier/switch RPMs. The RPM modules are designed to be located close (<30cm) to the device under test (DUT), minimizing cabling effects to provide improved high-speed measurements. Two of the most used program modules for the measurement of ferroelectric properties are shown in Figure 2.11.

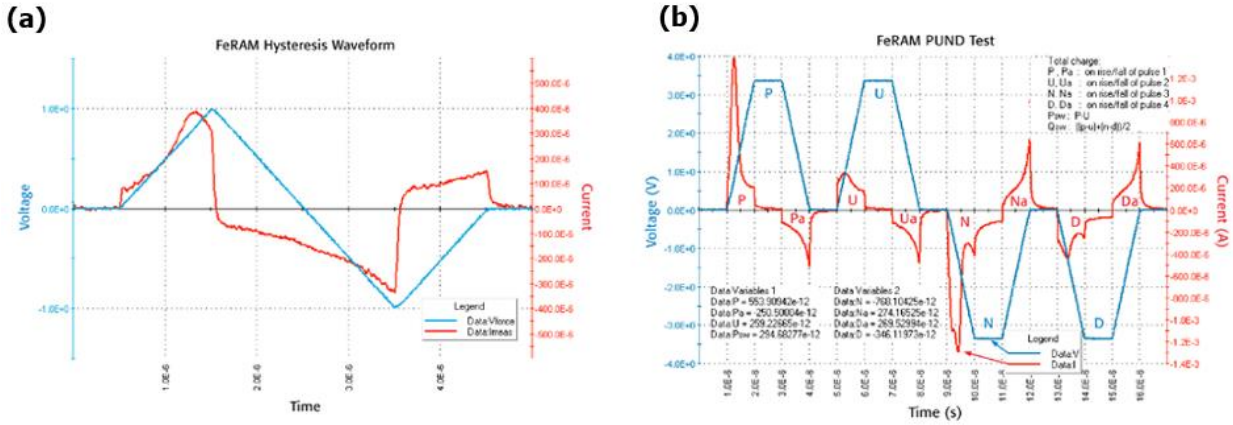

Figure 2.11: (a) FeRAM hysteresis waveform module, and (b) positive-up-negative-down (PUND) module of the Keithley 4200 SCS pulse measurement unit.

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CHAPTER 3

REALIZATION OF LOW VOLTAGE OPERATION FERROELECTRIC METAL-FERROELECTRIC -METAL CAPACITORS AT LOW PROCESSING TEMPERATURES (400°C)

3.1 Preface

The discovery of ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ (HZO)[1,2] thin films has paved the way to realize integration of ferroelectrics in current technology nodes and trench structures. However, in most cases, the crystallized HZO films have a small fraction of the equilibrium non-ferroelectric monoclinic (-M) phase that crystallizes along with the ferroelectric orthorhombic phase.[3-5] Careful systematic study is required to understand the parameters responsible for the complete stabilization of this meta-stable ferroelectric phase for scaled ferroelectric films to realize low-voltage operation.

CHAPTER 3 will primarily focus on the role of the TiN electrode as a stressor during the crystallization process of HZO and the effects of scaling HZO to 5 nm in metal-ferroelectric-metal (MFM) structures to enable low voltage ferroelectric operation. I would like to acknowledge Dr. Sijoon Kim, Dr. Jae-Gil Lee and Dushyant Narayanan for development of ferroelectric fabrication process and pulse measurement setup at UTD. This chapter includes some contents from three previously published work and some unpublished work. The three manuscripts are entitled (i) "*Effect of film thickness on the ferroelectric and dielectric properties of low-temperature (400°C) $Hf_{0.5}Zr_{0.5}O_2$ films*" in *Applied physics Letters*, adapted from Ref [6], Copyright (2018) AIP publishing. The authors are Si Joon Kim, Jaidah Mohan, Jaebeom Lee, Joy S Lee, Antonio T Lucero, Chadwin D Young, Luigi Colombo, Scott R Summerfelt, Tamer

San and Jiyoung Kim. (ii) "*Large ferroelectric polarization of TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors due to stress induced crystallization at low thermal budget* " in *Applied physics Letters*, adapted from Ref [9], Copyright (2017) AIP publishing. The authors are Si Joon Kim, Dushyant Narayan, Jae-Gil Lee, Jaidah Mohan, Joy. S. Lee, Jaebeom Lee, Harrison S. Kim, Young-Chul Byun, Antonio T. Lucero, Chadwin D Young, Luigi Colombo, Scott R Summerfelt, Tamer San and Jiyoung Kim. (iii) "*A comprehensive study on the effect of TiN top and bottom electrodes on atomic layer deposited ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films*" in Materials, adapted from Ref [8], Copyright (2020) MDPI publishing. The authors are Si Joon Kim, Jaidah Mohan, Harrison Sejoon Kim, Su Min Hwang, Namhun Kim, Yong Chan Jung, Akshay Sahota, Kihyun Kim, Hyung-Yong Yu, Pil-Ryung Cha, Chadwin D Young, Rino Choi, Jinho Ahn, and Jiyoung Kim.

In work discussed in this chapter, my contribution was to assist in designing experiments, performing the experiments, analyzing data, and participating in the discussions during the preparation of the above manuscripts. Dr. Su Min Hwang performed the X-ray photoelectron spectroscopy measurements and Dr. Harrison Sejoon Kim assisted with some of the X-ray diffraction measurements presented in this chapter.

Texas Instruments Incorporated funded this work.

3.2 Introduction

In recent years, ferroelectricity in HfO_2 thin films has been extensively studied for various applications including non-volatile memory and high-k DRAM structures. As already explained in the introduction section (CHAPTER 1), ferroelectric (FE) HfO_2 offers superior scaling and integration feasibility compared to traditional ferroelectrics like PZT and SBT.[9-12] The FE behavior for doped HfO_2 thin films is believed to originate from a non-centrosymmetric

orthorhombic phase and various theoretical investigations have shown that this phase in HfO_2 thin films can be stabilized in the presence of huge tensile strain (around 3-5 GPa)[13]. Essentially, several dopants like Si, Gd, Y, Sr, and La [14-16] have been studied for forming the ferroelectric phase in HfO_2 thin films, and most of the dopants require careful control of concentration and a higher thermal budget for the crystallization of the ferroelectric phase (>650°C). However, Zr doped HfO_2 i.e., $Hf_{0.5}Zr_{0.5}O_2$, offers good ferroelectric properties without precise composition control, and HZO can be deposited easily using ALD processes.[17-19] Additionally, ZrO_2 has a very low crystallization temperature compared to HfO_2, and alloying HfO_2 films with ZrO_2 (HZO) is shown to reduce the crystallization temperature to 400 or 450 °C.[1,19] This low-temperature processing could be of merit, particularly in the integration of ferroelectric materials in the back end of line (BEOL) processes. In most of the reports, the deposition of the TiN top electrode is done using an ALD or CVD process (at 400 – 500 °C) which also results in the crystallization of the HZO films. In these cases, ~20 to 60% of the crystallized HZO has the monoclinic phase (which is non-ferroelectric). [3-5] Hence, the factors responsible for the crystallization of pure ferroelectric -O phase must be thoroughly studied. To systematically isolate the role of the crystallization annealing step from the role of the TiN electrode capping layer effect, a room temperature sputtering process for TiN deposition was used in this work (instead of a high-temperature processes). The HZO MFM capacitors were then studied up to the scalability thickness limit to understand the thin film crystallization process and low voltage operation capability.

3.3 Effect of post-deposition annealing of 10nm HZO thin films

3.3.1 Experimental Procedures

On 100 mm p-type Si wafers with 300 nm thermally grown SiO_2, 90 nm TiN bottom electrode was deposited using room temperature radio frequency (RF) sputtering with an Ar:N_2 ratio of 20:1 using a power of 250 W. On top of this 10 nm thick HZO was deposited using TDMA-Hf, TDMA-Zr and O_3 as the Hf precursor, Zr precursor and oxidant respectively. The deposition temperature of HZO was 250°C, and the growth rate of HZO was ~0.2 nm/supercycle. Immediately after deposition of HZO, a post-deposition anneal (PDA) process was performed at different annealing temperatures (between 300°C - 700°C). After the PDA process, a 90 nm TiN top electrode was deposited using room temperature RF sputtering. A photolithograpic/wet etching process, as described in chapter 2 (section 2.3.1) was used to isolate the capacitor top electrodes.

3.3.2 Results and Discussions

Figure 3.1 shows the polarization-electric field (P-E) hysteresis characteristics of 10 nm HZO MFM capacitors performed at 10 kHz after the PDA annealing process was performed between 300 to 500 °C. The as-deposited films (no annealing process) and the 300 °C PDA annealed samples show pure dielectric response (linear polarization-voltage characteristics). In comparison, the samples annealed to temperatures between 400 °C and 500 °C show small ferroelectric behavior of ~3 μC/cm^2 even when the annealing process was performed before the TiN capping TE layer was deposited. All the measurements were performed after wakeup field cycling of 10^5 cycles at 2.5 MV/cm. The reduced P_r of the initial device and improved properties

during the initial wakeup cycles is a little analogous to silicon devices' “burn-in” failure, and the term “wakeup” is more often used by the ferroelectric community.[35] During wakeup field cycling, redistribution of defects and oxygen vacancies occurs, leading to un-pinning of some ferroelectric domains, causing more significant ferroelectric polarization.

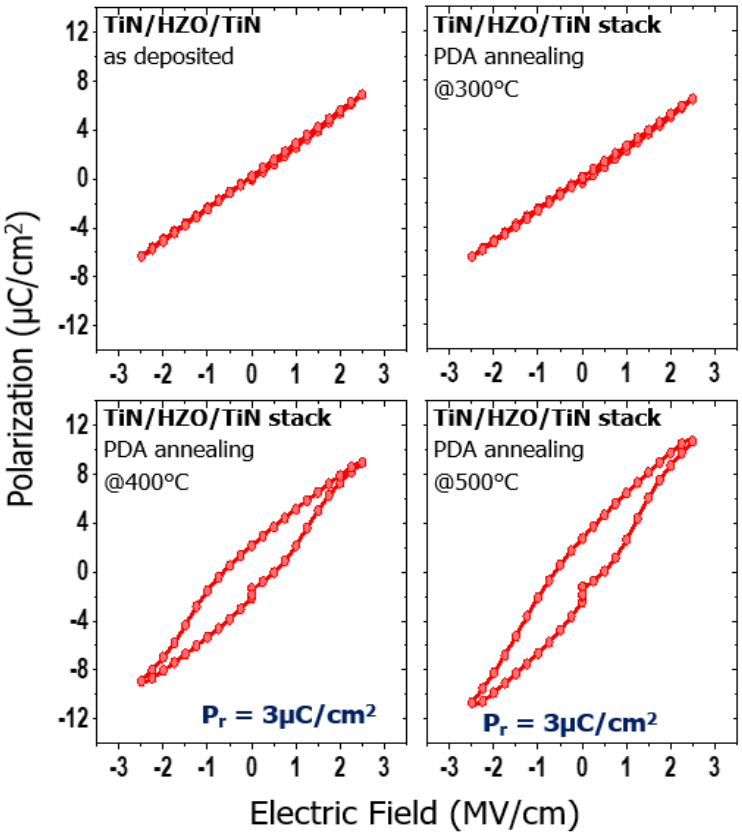


Figure 3.1: Effect of post-deposition annealing (300-500°C) on the ferroelectric properties of 10 nm HZO MFM capacitors.

The resulting crystal structure of the HZO films annealed before TiN TE deposition was measured using grazing-incidence X-ray diffraction (GI-XRD) in the 2θ range between 26° - 40° with an incident angle of 0.5°. Because of structural similarity between the ferroelectric -o phase and the -t phase in HZO films, the peaks centered at 30.5° and 35.5° are assigned to the -o phase

of HZO films. The peaks centered at 28.5° and 31.5° correspond to the diffraction from the -m phase of HZO films. Table 3.1 summarizes the various diffraction peaks between 26° - 40°, their (h k l) values and corresponding d- spacing.

Table 3.1: A table showing the various d-spacings between 2θ range of 26° to 40° adapted from Ref[5].

GIXRD	■	●	▲	▼	▽
θ (°)	~28.5	~30.5	~31.5	~35.5	~36.5
Phase	m-phase	o-phase	m-phase	o-phase	TiN
	(-1 1 1)	(1 1 1)	(1 1 1)	(2 0 0)	(1 1 1)
d (Å)	~3.13	~2.94	~2.83	~2.54	~2.44

Both the as-deposited films (the films are deposited at 250 °C) and the 300 °C PDA annealed samples show a lack of long-range ordering in the films. This can be interpreted as having an amorphous or nano-crystalline structure. The HZO films after PDA annealed to 400 °C or higher show both the -o phase and -m phase characteristics.

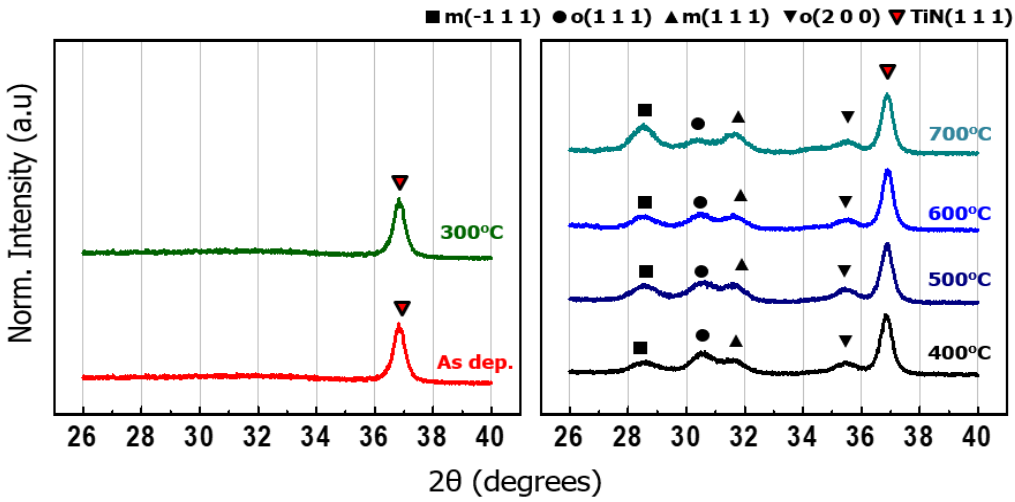


Figure 3.2: GI-XRD based on different PDA annealing temperatures for 10nm HZO film.

Based on theoretical XRD peak intensities from the structure factor calculations of the crystal structure, the relative ratio of the peaks of highest intensities m(-1 1 1) and o(1 1 1) was used to quantify the relative % of crystallized -o phase. The % of – o phase was highest after the 400 °C PDA annealing process with ~61%, but after annealing to higher temperatures, the % of -o phase sequentially decreases to 51% after 500 °C anneal, 51% after 600 °C anneal, and 40% after 700 °C anneal. Annealing to higher temperatures without top electrode deposition promotes the formation of the equilibrium non-ferroelectric -m phase.

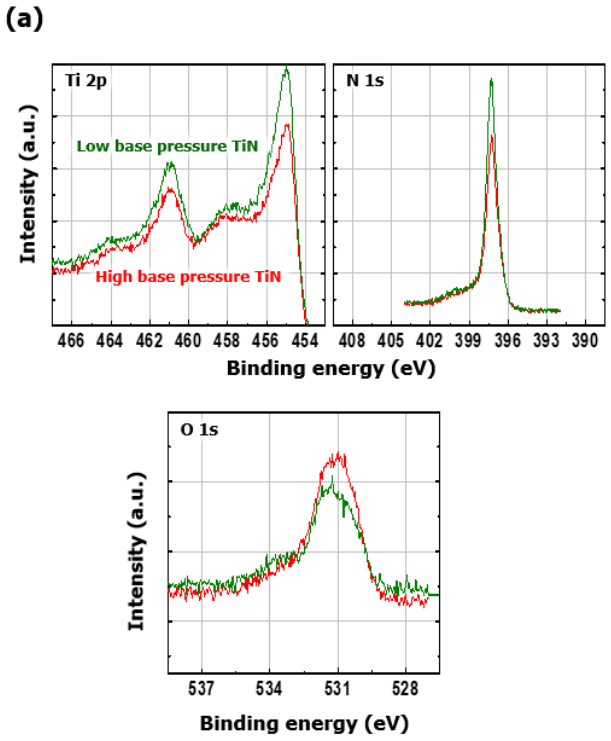
3.4 Effect of post-metallization annealing of 10 nm HZO thin films (annealing after TiN capping)

3.4.1 Effect of sputtering base pressure during TiN TE deposition

The capping of HfO_2 with the electrode before the annealing process is known to affect the ferroelectric properties critically. Si-doped HfO_2 was studied before and after the capping layer, and the TiN capping layer was shown to have an important role in inhibiting -M phase formation.[1] It was reported that the TiN capping layer acts as mechanical confinement which is necessary to prevent the volume expansion of the -M phase. It is also believed that the oxygen scavenging nature of TiN TE also creates tensile stress in the HZO layer to promote the crystallization of -o phase.[20-22] Hence, based on the base pressure of the sputtering chamber, the amount of oxygen in the TiN TE is controlled to study the effect of scavenging from the TiN top electrode.

Figure 3.3 gives the comparison of the X-ray photoelectron spectrum (XPS) of TiN deposited in $7x10^{-7}$ Torr (high vacuum pressure) and $<1x10^{-7}$ Torres (low vacuum pressure). The

XPS was performed using the PHI VersaProbe II using an Al Kα X-ray source with an incident angle of 54°. After 5 minutes of sputtering using a 1kV Ar+ gun to clean the TiN surface from contaminants, the XPS measurements were done using a pass energy of 23.5 eV. It can be seen that the N 1*s* to O 1*s* peak ratio for the TiN with low base pressure is higher, indicating lower oxygen contamination in TiN films. Based on peak area calculation and the atomic sensitivity factor, ~12% of oxygen was calculated for TiN deposition with high base pressure ($7x10^{-7}$ Torr) and ~ 6% of oxygen was calculated for TiN deposited with low sputtering chamber base pressure ($<1x10^{-7}$ Torr).



(b)

	peaks	Binding Energy (eV)
1	$Ti2p_{3/2}$ from TiN	455.5 ~ 456.0
	$Ti2p_{3/2}$ from TiO	454.5 ~ 455.5
	$Ti2p_{3/2}$ from TiO_2	458.5 ~ 459.5
2	N 1s	396.5 ~ 398.5
3	O 1s	528 ~ 537

Figure 3.3: (a) Ti 2p, N 1s, and O 1s core level spectra obtained from sputtered TiN with different chamber base pressure, and (b) binding energy ranges for Ti 2p, N 1s and O 1s core levels[49]

Based on the different TiN films deposited using room temperature sputtering on HZO, a post metallization annealing process was performed at 400 °C and MFM capacitors were

fabricated. From Figure 3.4(a), the amount of remnant polarization is similar for HZO capacitors fabricated using different oxygen concentration TiN films (16 μC/cm^2 for films fabricated using 12% oxygen TiN and 20 μC/cm^2 for films fabricated using 6% oxygen). The amount of P_r is usually a representation of the amount of ferroelectric phase concentration. However, the ferroelectric coercive field (E_c) is larger for the HZO films fabricated using TiN with higher oxygen concentration. This scenario with higher E_c with more skewed hysteresis has been mathematically modeled by a dielectric layer in series with the ferroelectric (demonstrated and called the dead layer effect).[23-27] Based on the parasitic capacitance of the material in series and the thickness of the material, the voltage is divided among the ferroelectric and the parasitic series capacitance. This leads to a much larger applied voltage requirement to the entire stack for the ferroelectric switching process to occur.

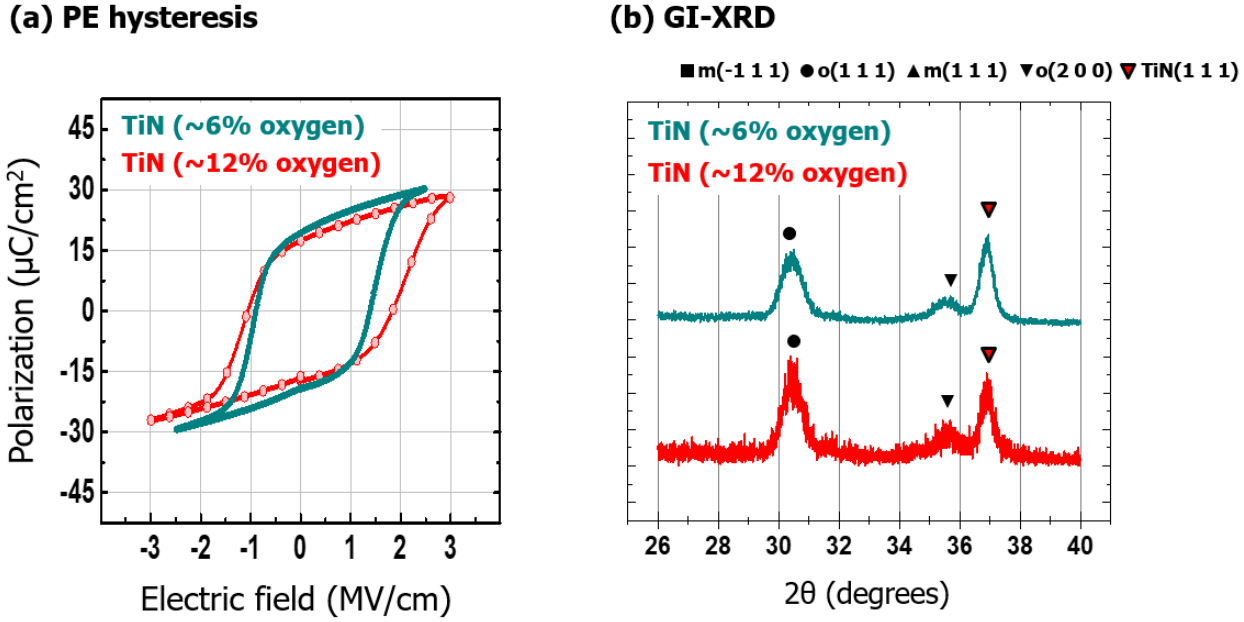


Figure 3.4: (a) PE hysteresis measurements for MFM capacitors with TiN with different oxygen impurity concentration and (b) GI-XRD showing the crystallinity of the underlying HZO film based on TiN TE with different oxygen concentration.

Also, from GI-XRD results shown in Figure 3.4 (b), it is evident that the crystallinity of the HZO films deposited using TiN with different oxygen concertation (Up to 12% oxygen) was not affected drastically (no significant monoclinic phase concentration in the HZO film). However, the effects of series capacitance due to the TiO_xN_y layer cannot be ignored during the deposition of TiN films and the fabrication of MFM capacitors.

3.4.2 Effect of PMA annealing temperature

Experimental procedures

On 100 mm p-type Si wafers with 300nm thermally grown SiO_2, a 90 nm TiN bottom electrode was deposited using room temperature radio frequency (RF) sputtering with an $Ar:N_2$ ratio of 20:1 using a power of 250 W. On top of this, a 10 nm thick HZO was deposited using TDMA-Hf, TDMA-Zr and O_3 as the Hf precursor, Zr precursor and oxidant respectively followed by subsequent room temperature sputtered 90 nm TiN deposition. After the deposition of the TiN top electrode, a post-metallization anneal (PMA) process was performed at different annealing temperatures (between 300°C - 700°C). A photolithograpic/wet etching process, as described in chapter 2 (section 2.3.1), was used to isolate the capacitor top electrodes.

Results and discussions

Figure 3.1 shows the polarization-electric field (P-E) hysteresis characteristics of 10 nm HZO MFM capacitors performed at 10 kHz after the PMA annealing process was performed between 300 to 500 °C. The 300 °C PMA annealed samples show very small ferroelectric response (almost linear P-E response) with P_r of 0.4 μC/cm^2. After 10^5 wakeup cycles at 2.5V, the HZO samples annealed to 400 °C after the TiN top electrode deposition show large P_r (24 μC/cm^2) and ferroelectric Ec of ~1.2 MV/cm. The HZO stack annealed to 500 °C after the TiN

top electrode deposition also show large P_r (26 µC/cm^2), however the E_c of the devices increases to ~1.5 MV/cm also accompanied by an increase in leakage current. As discussed in the previous section, an increase in the E_c while maintaining similar P_r values is a consequence of the dead layer effect and annealing the HZO samples to higher temperatures (>400 °C) can have a detrimental effect to the ferroelectric Ec. On comparing the results from Figure 3.4(a), this increase in E_c can be justified by the partial oxidation of TiN electrodes during the annealing process at higher process temperatures.

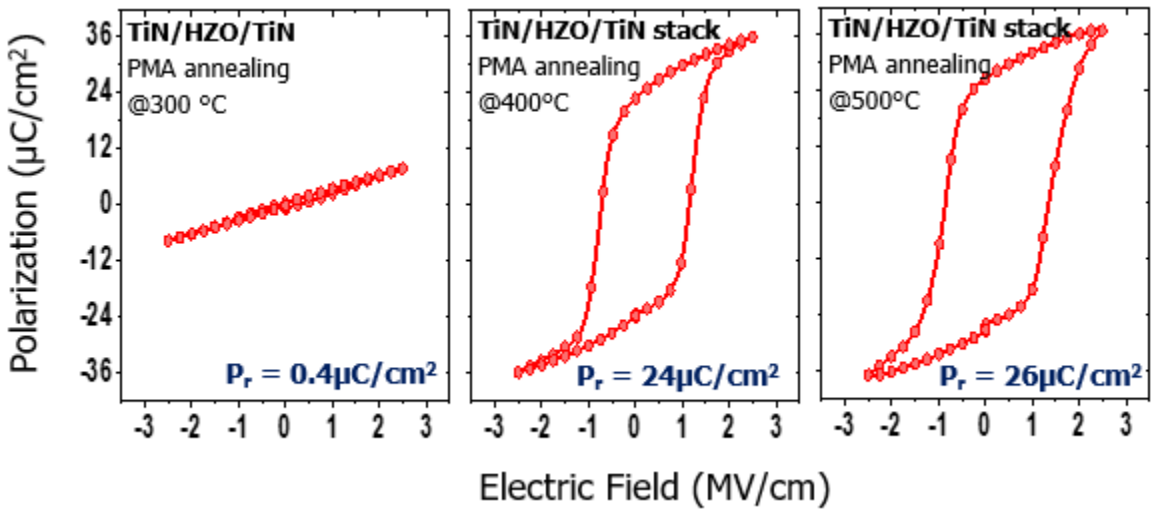


Figure 3.5: Effect of PMA annealing temperature on the ferroelectric properties of HZO films.

GI-XRD measurements were also performed as shown in Figure 3.6, from the 2θ range of 26° - 40° with an incident angle of 0.5°. 2x2 cm MFM stack (Si/SiO_2/TiN/HZO/TiN) wafer pieces were annealed at different temperatures from 300 °C to 700 °C using the RTA system. Before the GI-XRD measurements, the TiN TE on top of all HZO samples was chemically removed using the SC-1 wet etchant (NH_4OH:H_2O_2 1:1 ratio). It can be seen from Figure 3.6 that for the 300 °C annealing process, there is no crystallinity observed in the HZO films (the films

show amorphous or nano-crystalline short-range ordering). However, the HZO films annealed at 400 °C or higher after the TiN top electrode deposition shows the -o phase formation with the complete inhibition of the equilibrium monoclinic phase. The percentage of -o phase based on the relative ratio of o (1 1 1) diffraction peaks to the m (-1 1 1) peaks was 100%. It can also be seen that annealing to higher temperatures (up to 700 °C) in the presence of TiN TE still shows stable -o phase diffraction peaks and the inhibition of the -m phases.

Additionally, annealing the samples to higher temperatures increases the peak maximum based on the position of the -o (1 1 1) peak to higher 2θ degrees. It was seen that when the annealing process temperature was increased from 400 °C to 700 °C, the -o (1 1 1) peak maximum position increased from 30.44° to 30.5°.

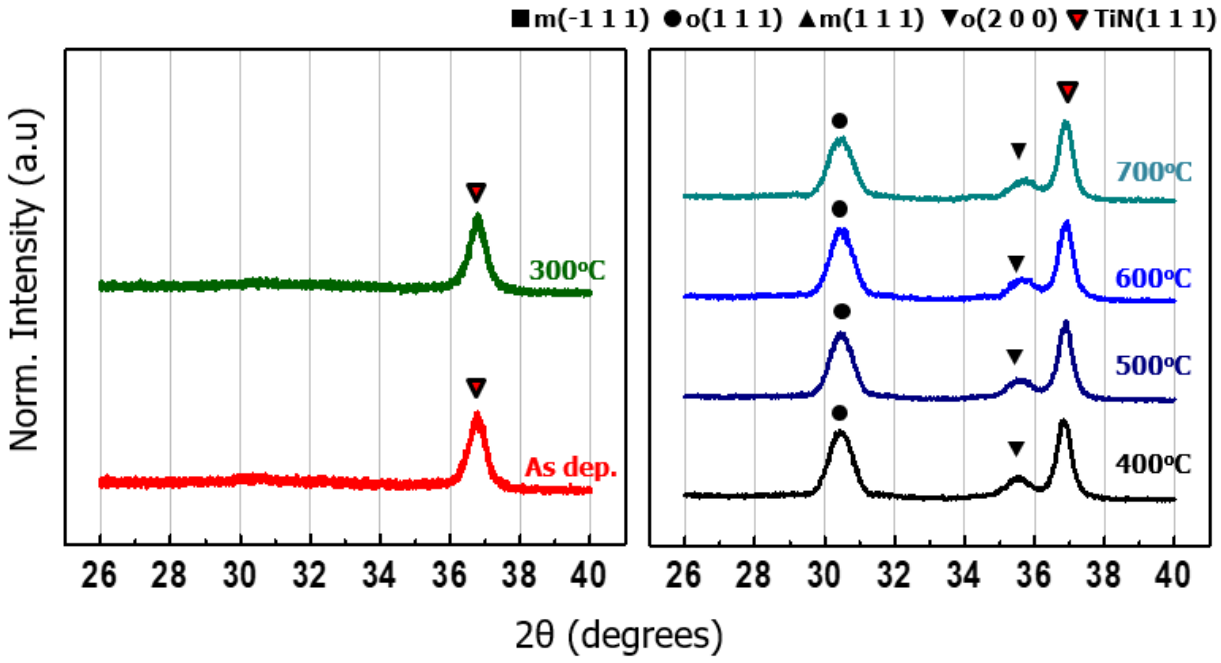


Figure 3.6: GI-XRD measurements of HZO films with different PMA annealing temperatures.

Since from Bragg's law, $n\lambda = 2d \sin\theta$, an increase in the 2θ peak maximum signifies a smaller d-spacing which means that the films experience a compressive stress as the annealing process is increased to higher temperatures.

The DC current-voltage (I-V) response of the MFM capacitors annealed at 300 °C, 400 °C and 500 °C was analyzed and it can be seen from Figure 3.7 that as the annealing temperature increases from 300 °C to 500 °C, the leakage current increases from $1x10^{-8}$ A/cm^2 to $1x10^{-4}$ A/cm^2. The increase in leakage currents with increase in annealing temperatures can be explained by the increase in grain size in the thin film and leakage current paths through the grain boundaries.[28,29] Hence, to ensure reduced leakage current and reduce the effect of dead layer effect due to the oxidation of the TiN electrodes, it is critical to reduce the thermal budget.

Leakage current measurements for HZO films annealed at different temperatures after TiN TE deposition is shown in Figure 3.7.

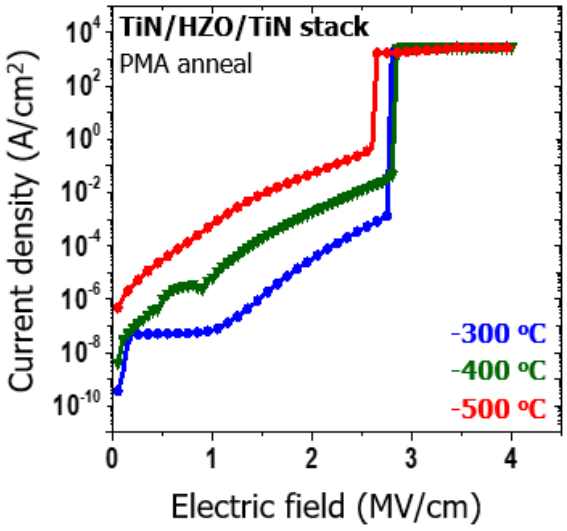


Figure 3.7: Leakage current measurements for HZO films annealed at different temperatures after TiN TE deposition.

However, the thermal budget for the crystallization of most HfO_2 thin films is >600 °C which can lead to oxidation of the TiN electrodes, causing the dead layer effect. This dead layer effect leads to a much higher voltage operation due to the voltage dividing between the parasitic capacitance components of the electrodes. Using ZrO_2 as the dopant can significantly reduce the annealing temperature (to <450 °C) and hence reduce the ferroelectric E_c of the material. Reduction in E_c can facilitate low voltage operation of ferroelectrics. Additionally, using room temperature sputtering for the TiN TE can significantly inhibit the formation of -M phase in the HZO film when the annealing process is performed after the TiN top electrode is deposited. The meta-stable phase can be observed when the annealing process is performed up to 700 °C after TiN top electrode deposition, indicating very good stability of the meta-stable phase in the presence of TiN stressor.

3.4.3 Effect of TiN TE thickness on the ferroelectric properties

Experimental procedures

On 100 mm p-type Si wafers with 300 nm thermally grown SiO_2, 90 nm TiN bottom electrode was deposited using room temperature radio frequency (RF) sputtering with an $Ar:N_2$ ratio of 20:1 and a power of 250 W. On top of this, 10 nm thick HZO was deposited using TDMA-Hf, TDMA-Zr and O_3 as the Hf precursor, Zr precursor and oxidant respectively followed by subsequent room temperature sputtered 90 nm TiN deposition. After the TiN top electrode deposition of different thickness (45 nm, 90 nm and 180 nm), a post-metallization anneal (PMA) process was performed at 400 °C. A photolithographic/wet etching process, as described in CHAPTER 2 (section 2.3.1) was used to isolate the capacitor top electrodes.

Results and discussions

Figure 3.8 shows the P-E hysteresis curves of the TiN-10 nm HZO-TiN stack with TiN top electrodes of different thicknesses (45 nm, 90 nm and 180 nm). The annealing process was performed at 400 °C after the TiN top electrode deposition in all these cases. It can be seen from Figure 3.8 that as the TiN top electrode thickness increases from 45 nm to 90 nm, an increase in P_r from 17 μC/cm^2 to 24 μC/cm^2 was observed. Further increase in the thickness of the TiN electrode to 180 nm shows a saturation in P_r at 24 μC/cm^2. The ferroelectric E_c was ~1.2 MV/cm in all these cases. This shows that in the presence of a thicker TiN TE stressor layer, the crystallization of the HZO films at 400 °C are even more favorable, and a thickness of >90 nm for the TiN electrode aids in the complete crystallization of the ferroelectric -o phase.

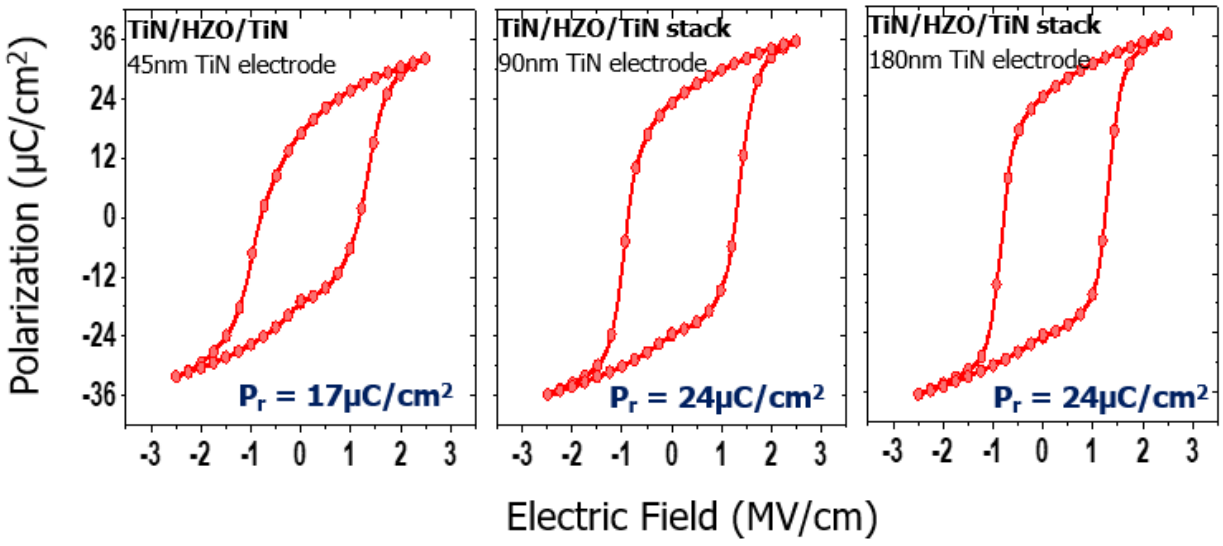


Figure 3.8: P-E hysteresis measurements of HZO films annealed at 400 °C using TiN TE of different thickness

Based on theoretical calculations using only the effects of stress (ignoring surface energy effect of HZO layer), a stress of ~10 GPa is required for the stabilization of -o phase at low processing temperatures (<500 °C).

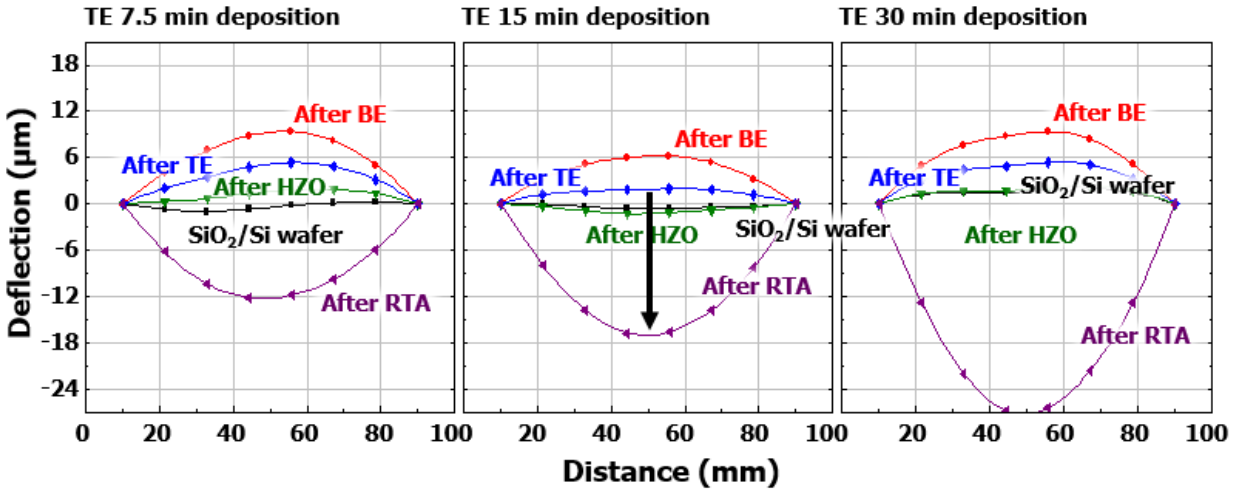


Figure 3.9: Thin film wafer bowing measurements performed after TiN electrode deposition of different thickness (45 nm, 90 nm and 180 nm).

Using the Toho thin film stress measurement tool, the amount of bending caused in the wafer due to thin film deposition is monitored. Based on this, the amount of bending generated in the stack after TiN deposition, and after the annealing process, an estimate of the amount of stress in the stack can be obtained from Stoney's equation. Based on the amount of deflection from the wafer after the TiN top electrode deposition of different thickness, it can be observed that a TiN deposition of 45 nm (7.5min sputtering deposition) can cause a deflection of -12 μm. The negative deflection indicates that the entire stack experiences a tensile stress after the annealing process. After 180 nm of TiN deposition, a deflection of -26 μm was obtained. This deflection corresponds to a tensile stress of ~3GPa in the entire stack. However, separating the amount of stress experienced by only the HZO layer is very difficult because of the complex stresses generated in stacked structures.[30-33] However, it is clear that a large tensile stress is generated in the stack after the RTA process with a TiN electrode of >90 nm thickness, which signifies the importance of TiN stressor in generating the stress.

Additionally, as shown in Figure 3.10, the effect of re-annealing a PDA annealed HZO sample (which has both -o and -m phases) was studied. TiN TE was deposited on the already PDA annealed samples, and a re-annealing (a post metallization annealing) process was performed at 500 °C and 600 °C. It can be seen from Figure 3.10 that once the equilibrium -M phase has been crystallized, even PMA processes at higher temperatures cannot phase transform -M phase to -O phase. Hence, it is crucial for the TiN top electrode to be deposited when the HZO films are still amorphous. The TiN top electrode can aid the amorphous -> ferroelectric -O phase formation, but once the equilibrium -M phase has been stabilized, it is very difficult for the phase transformation from -m phase to the -O phase to take place. Deposition of room temperature sputtered TiN TE films also aids in preventing premature crystallization of HZO films.

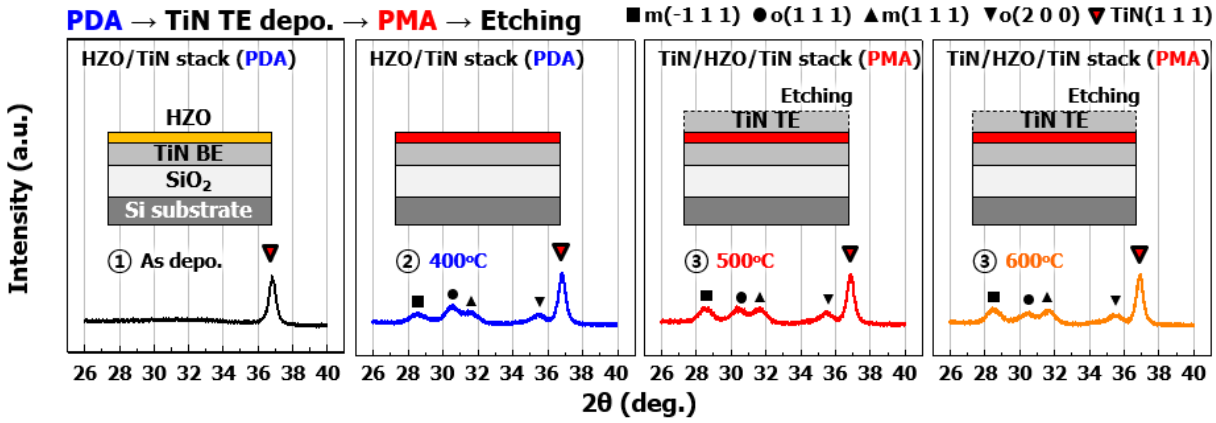


Figure 3.10: Effect of a PMA re-anneal at higher temperatures (500 °C, and 600 °C) after the PDA annealing process

Some of the HZO films reported in the literature use a CVD or ALD process for the deposition of TiN films[3-5,19] at temperatures >300 °C, which can lead to premature crystallization of the -m phase in the films.

3.5 The wake-up effect in 10 nm ferroelectric HZO

The reported ferroelectric properties in HZO films become more evident as the number of switching cycles increases. This observation is similar to most of the reports on HfO_2 based ferroelectric materials in the literature improved properties during the initial wakeup cycles is analogous to "burn-in" effects in silicon devices/transistors, but the term "wakeup" is more often used by the ferroelectric community.[34-36] The amount of polarization shown in 10 nm ferroelectric HZO increases from 11 $\mu C/cm^2$ to 24 $\mu C/cm^2$ after 10^5 switching cycles at 2.5 MV/cm as shown in Figure 3.11(a). This wake-up effect is usually an indication that some of the ferroelectric domains are pinned by defects and traps within the film or the electrode interface, leading to a much higher energy requirement for the complete ferroelectric switching process to occur.[39-42] It can be seen from Figure 3.11(b) that the complete ferroelectric switching process (switching current peak) occurs at a much lower voltage after the wakeup effect. Repeated cycling of the ferroelectric is believed to cause un-pinning of the pinned domains from the traps/defects, leading to a facile ferroelectric switching process. In HZO films, the formation of a defect-rich TiO_xN_y interface during the deposition and annealing process of TiN on top of HZO is believed to be an important reason for the observed wake-up effect.[26,36] Additionally, redistribution of the oxygen vacancies/defects in the HZO layer is also thought to affect the wake-up cycling effects.[36,37] In Figure 3.11, it can be seen that an anti-ferroelectric to ferroelectric transition occurs after the wake-up effect takes place. This observation is similar to most of the reports in the literature.[5,18,19]

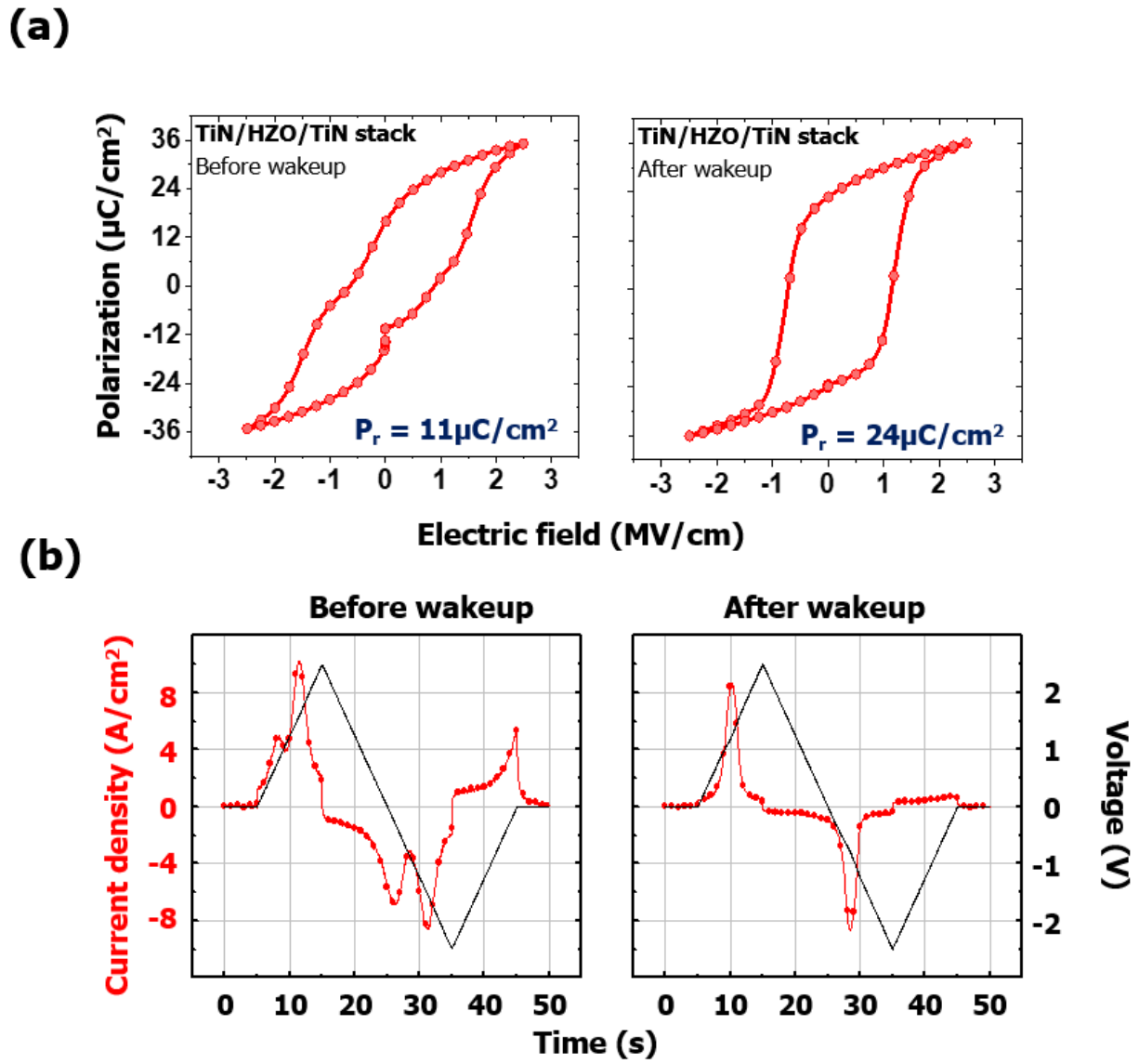


Figure 3.11: Figure showing the pulse I-V and PE hysteresis curves for 10 nm HZO ferroelectric films before and after the wakeup process (10^5 switching cycles at 2.5MV/cm)

To summarize the role of TiN top electrode, annealing before the TiN top electrode deposition is performed results in a very small portion of the ferroelectric -O phase. Annealing to 400 °C results in a P_r of ~3 μC/cm^2. It was observed that the quality of TiN electrode (oxygen contamination) plays an important role in the ferroelectric E_c because of parasitic components.

Reducing the base-pressure of the sputtering chamber also reduces the oxygen contamination in the chamber to reduce the E_c of ferroelectric HZO. Also, the effect of TiN stress was systematically studied, and it was seen that a TiN thickness of >90 nm and a PMA process of 400 °C is required to obtain large P_r and for the complete crystallization of the -o phase in HZO films. The results are summarized in Table 3.2.

Table 3.2: Summary of the ferroelectric properties obtained using different process conditions.

Process		Process temperature (°C)	TiN TE thickness (nm)	P_r (μC/cm²)	Ec (MV/cm)
Annealing before TiN deposition		300	90	-	-
		400	90	3	~1.5
		500	90	3	~1.5
Effect of sputtering base pressure	>$7x10^{-7}$ Torr	400	90	16	1.5
	<$8x10^{-8}$ Torr	400	90	20	1.2
Annealing after TiN deposition		300	90	0.4	-
		400	45	17	~1.2
		400	90	24	~1.2
		400	180	24	~1.2
		500	90	25	~1.5

3.6 Effect of Film Thickness on The Ferroelectric Properties of HZO Films

3.6.1 Introduction

With the discovery of ferroelectricity in doped HfO_2, a light has been brought to various new applications of ferroelectricity. Since an ALD process for HfO_2 (and HZO) is currently well developed, uniform and conformal deposition on trench structures can be precisely performed. Scaling the ferroelectric is key in most of these new applications. For example, in the case of

Ferroelectric Random-Access Memory (FRAMS) or Non-Volatile Dynamic Random-Access Memories (NV-DRAMs) scaling the thickness of the ferroelectric can help in achieving low voltage operation and sometimes aid in increasing the endurance cycles.[38] Ferroelectric tunnel junctions (FTJs) and Synapse devices which work on the principle of resistance difference during the switching and non-switching process requires ferroelectrics in sub-2 nm thickness range, as it provides more tunneling current.[39-41] Also, a new interest has developed in Negative-Capacitance Field Effect Transistors (NC-FETs) for logic transistor applications, as it is expected to produce hysteresis free sub-60 mV/decade sub-threshold swing.[42-46] Although there are different schools of thought on the origins of these effects [47-48], scaling ferroelectrics and understanding the scalability limit is crucial. The main problem with scaling conventional ferroelectrics, was that the effect of the interface dead layer becomes more prominent. Hence, proper analysis of the ferroelectric properties, domain sizes and interfacial dead layers due to annealing temperatures, crystal strain, and electrodes is essential in sub-10 nm thickness.

3.6.2 Fabrication Procedure

On 100 mm p-type Si wafers with 300 nm thermally grown SiO_2, 90 nm TiN bottom electrode was deposited using room temperature radio frequency (RF) sputtering with an $Ar:N_2$ ratio of 20:1 using a power of 250 W. On top of this HZO films of different thickness (20 nm, 10 nm, 7 nm and 5 nm) were deposited using TDMA-Hf, TDMA-Zr and O_3 as the Hf precursor, Zr precursor and oxidant respectively. The deposition temperature of HZO was 250 °C, and the growth rate of HZO was ~0.2 nm/supercycle. After deposition of HZO, a 90 nm thick TiN top electrode was deposited using room temperature RF sputtering. A post metallization annealing process was performed at 400 °C after top electrode deposition. A photolithography/wet etching

process, as described in CHAPTER 2 (section 2.3.1) was used to isolate the capacitor top electrodes.

3.6.3 Results and Discussion

Figure 3.12 shows the P-E hysteresis curves measured at 10 kHz from HZO films of different thickness (20 nm, 10 nm, 7 nm and 5 nm) annealed after the TiN top electrode deposition at 400 °C (for 60 seconds) after 10^5 wake-up cycles at 2.5 MV/cm.

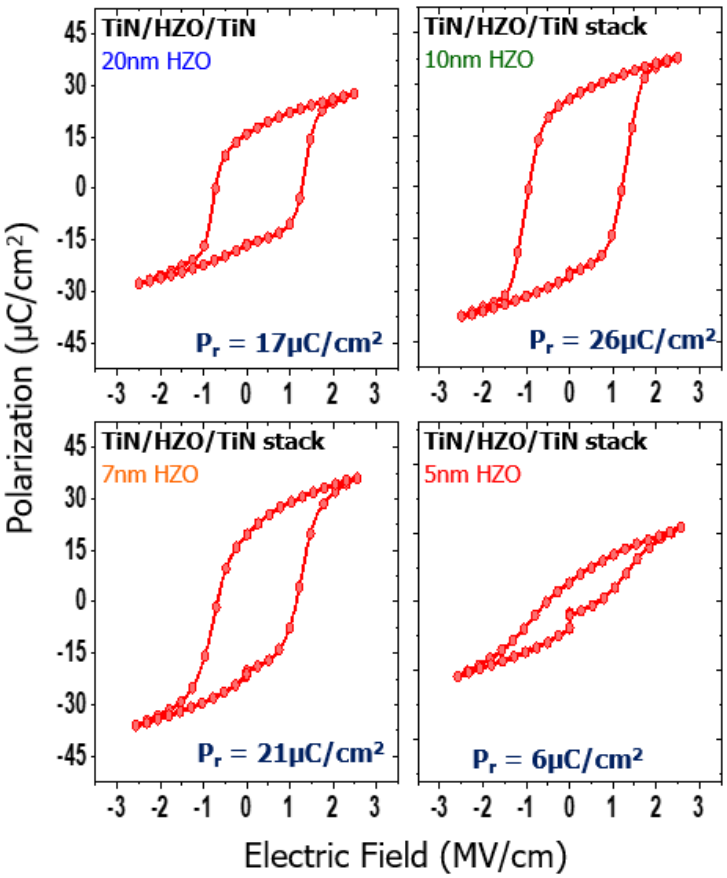


Figure 3.12: PE hysteresis loops from the MFM capacitors obtained from HZO deposited with different thickness (scaling down to 5nm) and a PMA anneal of 400 °C

From the P-E hysteresis curves, it can be observed that the 10 nm HZO films show the largest Pr of ~26 μC/cm^2. Scaling down in thickness to 7 nm and 5 nm shows a reduction in P_r to ~21 μC/cm^2 for 7 nm HZO and ~6 μC/cm^2 for 5 nm HZO films. Additionally, an increase in the thickness to 20 nm HZO also shows a decrease in P_r to 17 μC/cm^2. However, the operating voltage reduction due to scaling is very advantageous for practical applications and commercialization. The reduction in P_r from 10 nm to 5 nm can due to the smaller ferroelectric grain size. The grain nucleation and growth of the crystalline grains are restricted due to the lateral limit of the HZO thin films. The grain size based on the film thicknesses and increasing the grain size based on annealing temperatures are a direction of future study. The amorphous → crystalline phase transformation is driven by the free energy minimization of the material.

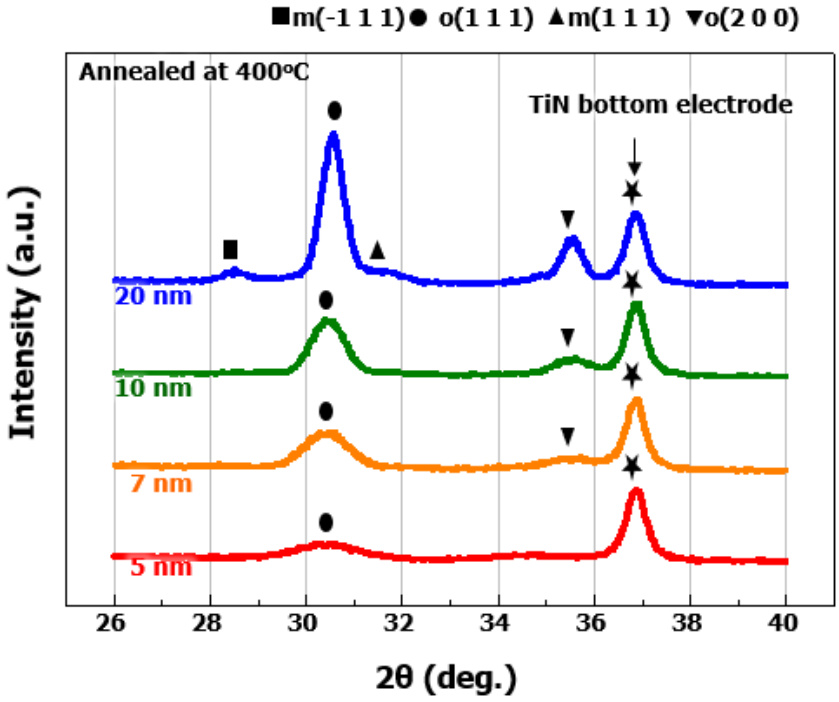


Figure 3.13: GI-XRD results showing the crystallinity of HZO films scaled from 20 nm to 5 nm. 20 nm shows the presence of the equilibrium -m phase in addition to the ferroelectric -O phase.

The GI-XRD results show the -O phase peaks at ~30.5° and 35.5° in all the HZO films, scaling down to 5 nm thickness. In the case of 10, 7 and 5 nm HZO, the complete inhibition of the equilibrium -M phase was observed, however in the case of 20 nm HZO, a small fraction of –m phase nucleation was also observed. Hence, once the volume energy of the thin film increases, the stabilization of the equilibrium – M phase starts to become more favorable.

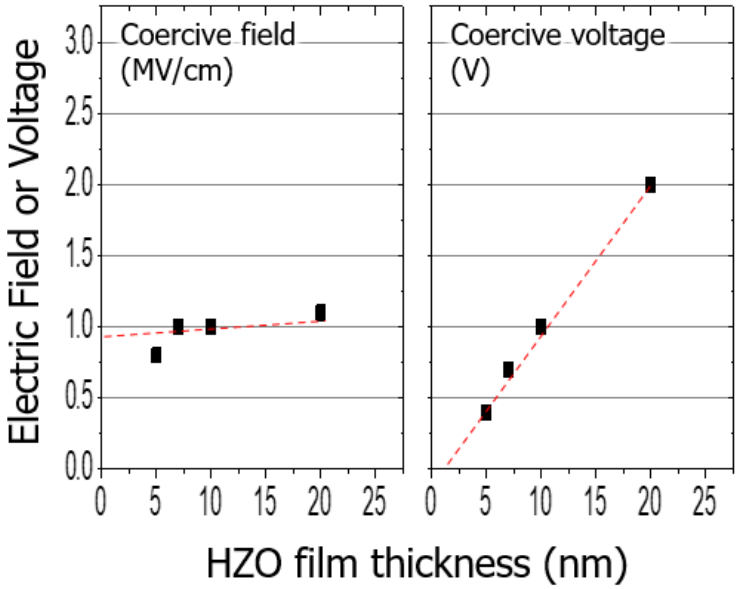


Figure 3.14: Summary of scaling down the ferroelectric E_c and operating voltages in HZO thin films.

From Figure 3.14, the scalability on HZO in terms of voltage operation has very minimal impact. This is because of the expected relatively high dielectric constant for the interface TiO_xN_y layer compared to the conventional PZT films.[50] Based on this, low voltage operation (~1 V operation) can be achieved in 5 nm ferroelectric HZO films, but the small grain size limits the remnant polarization for such thicknesses.

3.7 Conclusions

To summarize the role of the TiN top electrode, annealing before the TiN top electrode deposition is performed results in a very small portion of the ferroelectric -o phase. Annealing to 400 °C results in a P_r of ~3 μC/cm^2. It was observed that the quality of the TiN electrode (oxygen contamination) plays an important role in the ferroelectric E_c because of parasitic components. Reducing the base-pressure of the sputtering chamber also reduces the oxygen contamination in the chamber leading to a higher voltage requirement for the ferroelectric switching process to compensate for the voltage drop across the dead layer. Also, the effect of TiN stress was systematically studied, and it was seen that a TiN thickness of >90 nm and a PMA process of 400 °C is required to obtain large P_r and for the complete crystallization of the -O phase in HZO films. Additionally, scaling the HZO films to 5 nm can provide low voltage operation of the ferroelectric (~1 Volt). This can aid advances in various applications that require thin ferroelectric films such as ferroelectric tunnel junctions.

3.8 References

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CHAPTER 4

RELIABILITY PROPERTIES OF LOW-TEMPERATURE (400 °C) HZO METAL-FERROELECTRIC-METAL CAPACITORS

4.1 Preface

Although ferroelectrics HfO_2 thin films have shown significant promise as a prospective candidate for future ferroelectric-random-access memories due to their scalability and integration capabilities, the reliability of these devices still hinders commercialization. HfO_2 based ferroelectrics show an endurance that is significantly lower than state-of-the-art commercialized FeRAM devices using PZT. Additionally, since the operating voltage is very close to the breakdown voltage of the ferroelectrics (operating voltage of ~3 Volt with a breakdown voltage of ~3.5 Volt), there is a severe risk of premature failure of these devices. There has been extensive study on the ferroelectric properties of different doped HfO_2 films. However, there is still a lack of literature on comprehensive ferroelectric reliability characterization of these materials (particularly HZO) films. To realize commercialized low temperature ferroelectric HZO MFM capacitors, it is crucial to study and correlate the various reliability properties. Four primary failure mechanisms are responsible for limiting ferroelectric devices' lifetime: breakdown (voltage/time dependent breakdown), endurance, data retention, and imprint.

CHAPTER 4 will primarily focus on discussing the various reliability issues in 10 nm ferroelectric HZO MFM capacitors, particularly the imprint and data-retention properties, and the correlation between operation voltage and pulse widths for various reliability issues.

In the work discussed in this chapter, which is under preparation for submission in a peer-reviewed journal, my contribution was designing the experiments, performing the reliability

studies, and analyzing and interpreting data. Dr. Si Joon Kim, Dr. Yong Chan Jung, Dr. Heber-Hernandez Arriaga and Jinhyun Kim participated in discussions and data interpretation of the results. Dr. Scott Summerfelt guided the measurement setup, and Prof. Jiyoung Kim guided the experiments, reviewed the results, and contributed to the data interpretation and preparation of the manuscript.

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4.2 Introduction

The discovery of the ferroelectric phase (orthorhombic, space group – $Pca2_1$) in doped HfO_2 thin films has been a breakthrough for ferroelectric (FE) technology. This is because HfO_2 is a material that is fully compatible with current complementary metal-oxide-semiconductor (CMOS) technology, making ferroelectricity one of the most promising emerging memories.[1-4] Additionally, the FE properties in thin doped HfO_2 films can be easily obtained using atomic layer deposition (ALD), a technique that enables precise control of film thickness and 3-D conformality.[3-7] In this regard, there has been a growing interest in investigating these materials for a wide range of device applications like ferroelectric random-access memory (FeRAMs),[6,8-9] ferroelectric field-effect transistors (FeFETs),[10,11] energy storage[12,13], and even neuromorphic applications[14,15]. Among various doped HfO_2 films, Zr-doped HfO_2, i.e., $Hf_{0.5}Zr_{0.5}O_2$ (HZO), is one of the most promising candidates because of its low crystallization temperature ($\leq$400°C), stable FE properties for a wide range of compositions, and back end of line (BEOL)

compatibility.[1,3,7] Although HZO films have shown promising performance, such as suitable remnant polarization (P_r ~25 μC/cm^2), low voltage operation (2.5 V) and nano-second switching,[16] careful assessment of the reliability properties is needed to ensure the practical realization of these FE films.

Three primary failure mechanisms are responsible for limiting the lifetime of FE devices, namely: endurance, data retention and imprint.[17-19] The endurance properties of HZO films have been studied extensively and various mechanisms were studied to understand and mitigate the effects of field cycling on the FE performance and fatigue.[20-22] However, the imprint failures are often overlooked and from studying conventional FE films like $PbZrTiO_x$ (PZT), $SrBiTaO_x$ (SBT) etc., it is well known that they pose more severe problems to the memory operation.[17,19] Additionally, for neuromorphic applications, the stability and retention of polarization in the sub-polarization states are also crucial and need to be investigated carefully.

Among the data retention and imprint studies in the literature, the shift in the polarization-voltage hysteresis loops is often studied.[20-22] Although this effect can cause an increase in the operating voltage, this effect is not as detrimental as compared to opposite state imprint effects.

The increase in the imprint and data retention time-to-failure (TTF) based on increasing annealing temperatures of Si-doped HfO_2 was reported.[25] There have been other reports on the data retention properties of MFM capacitors as well,[26-28], but there is limited insight on the mechanism of data retention in HZO based MFM capacitors. Additionally, it is to be noted that some retention tests in the literature use large pulse widths (~1ms) for their retention and imprint tests,[23,25-26,] which can significantly exaggerate the lifetime of ferroelectric devices. This chapter

sheds more light on the data retention and imprint degradation mechanisms of 10 nm HZO MFM structures. To the author's knowledge, the data retention and imprint properties of HZO based MFM capacitors were studied systematically based on applied voltages, baking temperatures, write pulse widths, and switching cycles for the first time. Based on the electrical characterization, a strong recovery effect on the imprint and data retention degradation was observed when subjected to extended switching pulse width and switching cycles. Although the use of large pulse width is impractical, the long-term operation of FE HZO devices can be stabilized even further by using a periodic refresh based on a long switching pulse or a large number of switching cycles.

There have been a few studies regarding the data retention and imprint properties of doped HfO_2 thin films.[23-28,37] The effects of imprint and data retention by increasing a physically deposited Al_2O_3 dielectric layer on top of HZO films were studied to give an insight into capacitance matching and bulk screening on the data retention properties.[23] The effects of scaling FE film thickness on the data retention properties when HZO was integrated on silicon were also studied, and the results were explained due to generated built-in fields.[24] In these cases, where the FE films are integrated on dielectric/semiconductor (interface) layers, the mechanism of retention is based on the capacitance matching between the interface and the FE layer, and based on the capacitance of the interface. This effect can be more drastic compared to metal-ferroelectric-metal (MFM) capacitors.[23]

4.3 Experimental Details

4.3.1 Fabrication Procedure

The fabrication processes of 90 nm TiN/10 nm HZO/90 nm TiN MFM capacitors are as follows. The TiN bottom electrode was deposited on top of p-silicon substrates with 300 nm thermally grown SiO_2. At room temperature, radio frequency (RF) sputtering using a Ti target in an Ar : N_2 environment with a ratio of 20:1 was performed. After this, 10 nm ALD HZO films were deposited using TDMA-Hf, TDMA-Zr, and ozone (O_3) as the Hf precursor, Zr precursor, and oxygen source, respectively. During ALD deposition, the wafer temperature was set to 250°C for a growth per cycle of HfO_2 and ZrO_2 of ~0.2 nm/cycle. The final thicknesses of HZO films were approximately 10 nm, as verified by spectroscopic ellipsometry and HR-TEM. A 90 nm TiN top electrode was deposited at room temperature using RF sputtering to encapsulate the HZO films. The stack was then subjected to rapid thermal annealing (RTA) process for 60 s at 400 °C in an N_2 environment. The RTA process was done after the TiN top electrode deposition to ensure sufficient stress was given to the film for the -O phase crystallization.[29,30] The MFM structures were then defined using a photolithography and etching process. Negative photoresist (nLOF2020) was spin-coated on top of the MFM stack and pre-baked at 115 °C for 60 s on a hot plate to remove the excess solvent. The photoresist was subsequently exposed to ultraviolet light through a mask having hole diameters of 50, 75, and 100 μm with a post-exposure bake at 115 °C for 60 s on a hot plate. The photoresist development step was carried out for 75 seconds using the AZ300-MIF developer. An Au/Pd hard mask with a thickness of 85/3 nm was deposited using an electron-beam evaporator, and then the lift-off process was carried out using AZ400T stripper using a hot plate at 75 °C for 15 mins. The wet-etching process of TiN was carried out

using SC-1 (1:1 ratio of NH_4OH: H_2O_2) to remove the TiN and isolate the capacitor structures. For the electrical characterization, circular pads with a diameter of 75 μm were probed. Polarization-voltage (P-V) hysteresis measurements were conducted at 10 kHz using the pulse measuring unit (PMU) of the semiconductor parameter analyzer (Keithley 4200-SCS), and the output characteristics were measured using the virtual ground method. The baking process was done in box-type ovens, restricted to particular temperatures only (i.e., separate dedicated ovens for 65 °C, 95 °C and 110 °C bake). In all the electrical measurements performed, the voltage was applied to the top electrode and the bottom electrode is grounded.

4.3.2 Pulse Measurement Setup

The pulse read/write measurements were performed similar to the previous reported studies[24,29,30]. Using a pulse generator (Agilent 81110A) and an oscilloscope (Tektronix DPO7104) and shown in Figure 4.1, the subsequent voltage drop across an internal resistor of 50Ω (shunt resistor) was measured using an oscilloscope. The load current was calculated from the measured load current which was then integrated over time to extract the polarization response of the material.

The pulse read/write measurement sequence is sent such that both the switching and non-switching responses can be extracted from the read pulses at different voltages.

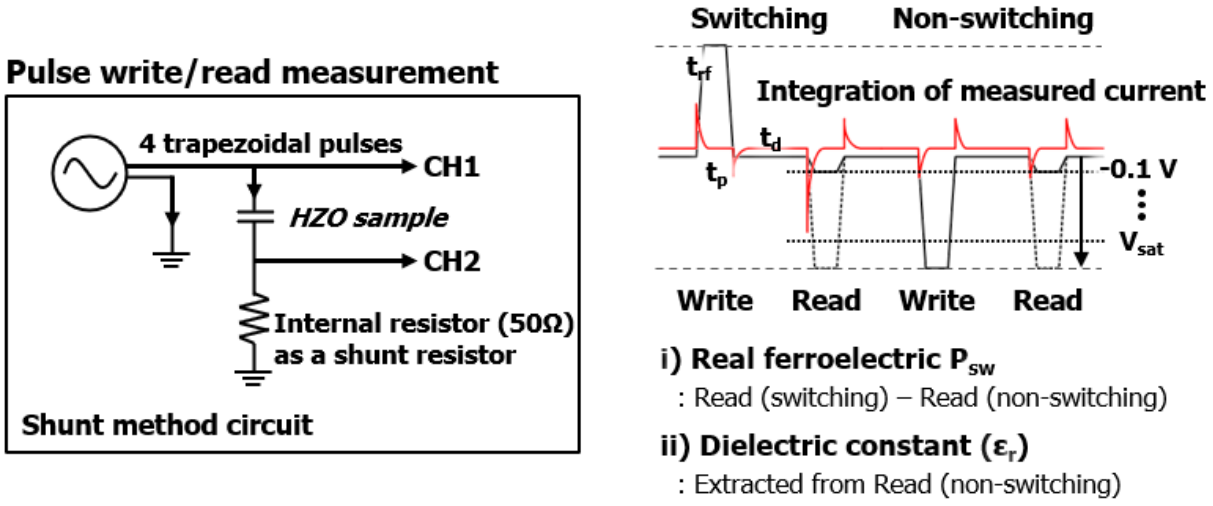

Figure 4.1: A schematic diagram of the pulse read/write measurements and a sequence of write/read pulses using a fixed write voltage at ±2.5 V and the read voltage was varied in 0.1 V steps from -2.5 V to 2.5 V.

By subtracting the integrated current values for the switching and the non-switching operation, the real ferroelectric switching (P_{FE}) was extracted. The slope of the polarization voltage responses during non-switching operation can be used to extract the material dielectric constant values.

4.4 Results and discussions

4.4.1 Ferroelectric property measurements in 10-nm HZO films

Figure 4.2(a) shows the standard P-V hysteresis curves measured from bipolar triangular pulses from the 10 nm HZO MFM capacitor after being subjected to a 10^5 wake-up cycle at 2.5 V. This wakeup effect, where the P_r increases with a certain number of field cycles, is observed in most of the HZO based FE reports in the literature.[9,21,29]

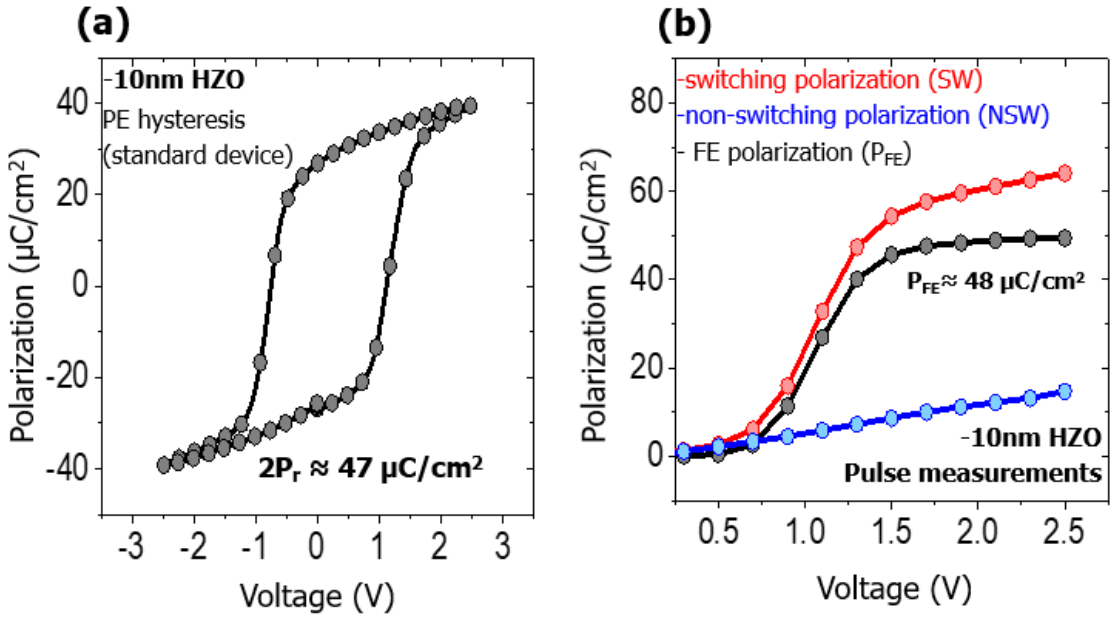

Figure 4.2: (a) P-V hysteresis measurements of the HZO MFM capacitors after wakeup cycling (10^5 cycles at 2.5 V), (b) Pulse measurements to extract SW, NSW, and FE polarization at various applied voltages after 6s of delay time.

From the P-V hysteresis results, the devices showed a P_r of 24±0.7 μC/cm^2 with a coercive voltage V_c of 1.25±0.03 V. The pulse write/read measurements were also performed similar to our previous studies[9,29]. The comparison of P_{FE} properties from pulse measurements, measured at room temperature (RT) up to 125 °C between 10 μs delay between pulses and 6 s delay between pulses is shown in Figure 4.3. At saturation polarization, there is no significant difference between the two delay times. This time of less than 6s is sufficient for charge trapping/de-trapping responses to affect the FE polarization.[24,29]

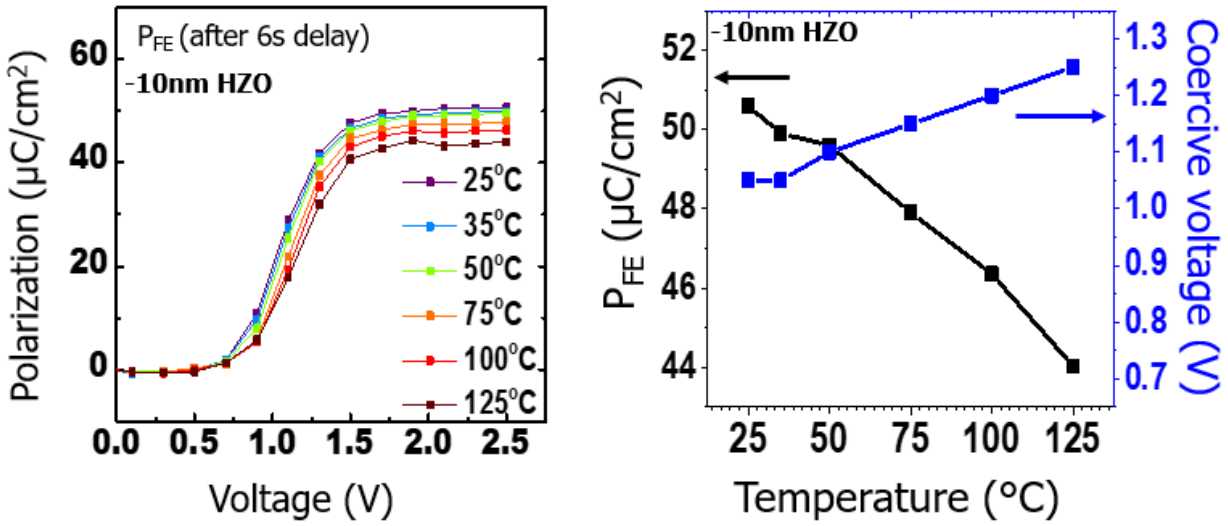

Figure 4.3: (a) Temperature dependence on the FE polarization extracted using pulse write/read measurements using 6s delay time between pulses, (b) Saturation polarization and coercive voltage dependence on temperature.

A 6 s delay time between pulses ensures sufficient relaxation time.[29] Figure 4.2(b) shows the pulse measurements done after the device is subjected to the wakeup cycles. The real FE polarization (P_{FE}) of 48±1.5 μC/cm^2 was calculated by subtracting the switching (SW) and NSW polarization. These values were similar to the reports done in our previous studies.[9,29] Additionally, the pulse measurements done at high temperature using a hot chuck show stable FE properties from room temperature (RT) to 125 °C (see Figure 4.3), indicating the metastable orthorhombic phase is stable even at elevated temperatures.

4.4.2 Statistical variation and Lot-to -Lot dependence

The batch-to-batch variation of ferroelectric properties of 10 nm HZO fabricated using the post metallization annealing process at 400 °C using ozone was verified extensively. This device was used as a control sample in all the device fabrication splits (called a batch). Figure

4.4 shows the batch-to-batch variation fabricated from almost 50 10 nm MFM capacitors. The reference devices without any special causes showed a P_r of 25 ±5 μC/cm^2 and a coercive field E_c of 1.2 ±0.2 MV/cm. When the fabricated devices do not follow the statistical distribution, some tool issues or fabrication processing issues are identified .

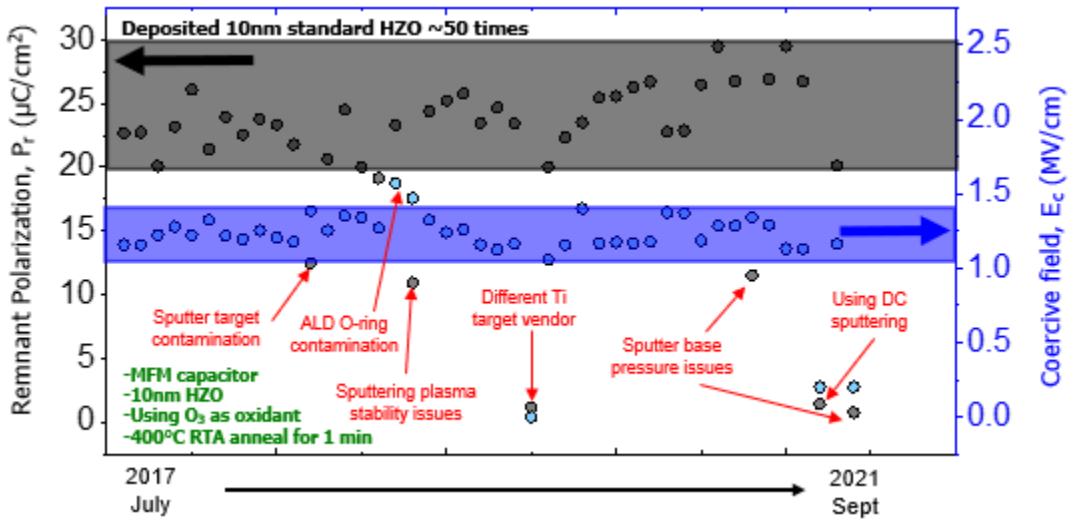

Figure 4.4: The batch-to-batch variation of the ferroelectric properties of 10 nm HZO MFM capacitors

As shown in Figure 4.5, within the same fabrication batch (around 2x2 cm^2 sample) , the 10nm MFM capacitors measured across 25 devices show an even tighter distribution of 23±0.7 μC/cm^2 (which is a standard deviation of 0.4σ) and E_c variation of 1.25 ±0.03 MV/cm.

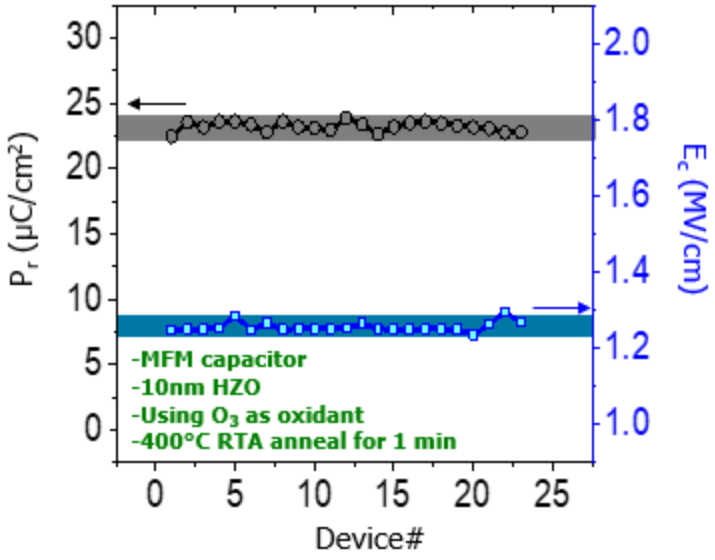

Figure 4.5: Device-to-device variation of the various capacitors in the same fabrication batch.

4.4.3 Fatigue and TDDB tests

Ferroelectrics are expected to degrade under the influence of repeated switching cycles, and this degradation is attributed to the generation, redistribution, and migration of oxygen vacancies in the HZO layer and at the interfaces. It can be seen from Figure 4.6 (b) that using a higher voltage for the ferroelectric operation leads to a much faster degradation. For example, using 4 Volt switching pulses show ~10^4 cycles of stable ferroelectric memory operation, while using 2.5 V shows 10^9 cycles of stable ferroelectric endurance operation. From Figure 4.6(a), it can be observed that using a 2.5 V cycling leads to a continuous increase in polarization followed by a hard breakdown after 10^9 cycles. Breakdown is defined as the point at which the ferroelectric(dielectric) shows conductive I-V behavior because of a conductive filament formation. As the breakdown voltage of HZO films is ~3 V, hard breakdown is more common endurance failure. However, cycling at 2 Volts shows a standard ferroelectric fatigue

measurement with wake-up, stabilized, and fatigued (degradation in polarization with time) regions clearly obervable. The wake-up effect is attributed to redistribution of oxygen vacancies in HZO, and fatigue is due to defect generation and ferroelectric domain pinning.[19-22] The polarization fatigue tests were performed using trapezoidal voltage pulses with 5 µs width, 10 µs delay time and 600 ns rise/fall time.

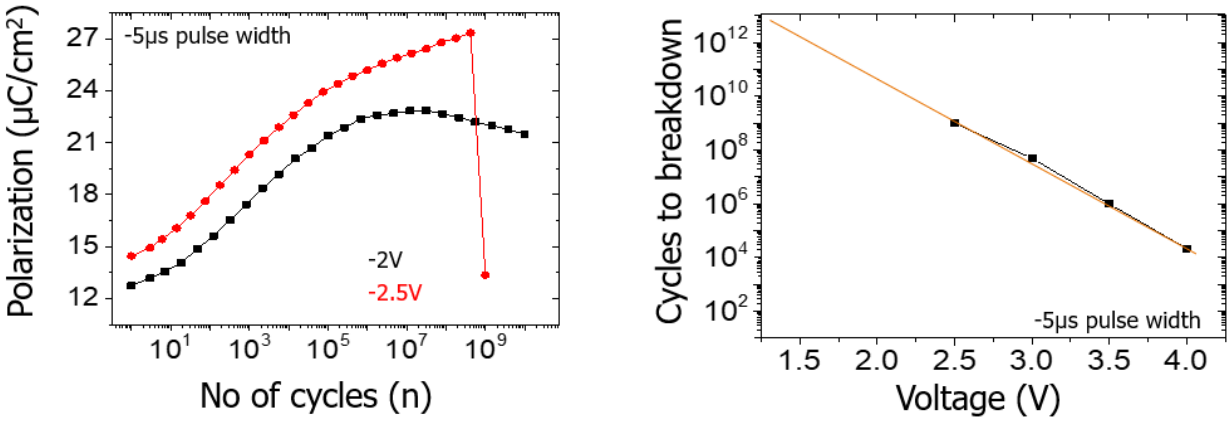

Figure 4.6: The ferroelectric polarization fatigue measurements of 10 nm HZO MFM capacitors showing stable operation for 10^{10} cycles under 2V operation.

From the time dependent dielectric breakdown (TDDB) measurements shown in Figure 4.7, it is also clear that a lower voltage operation leads to a more reliable long term ferroelectric property in the HZO films. The TDDB measurements shown in Figure 4.7(a) show 3 regions. Initially, the current decreases due to electron trapping until a soft breakdown occurs which eventually leads to hard breakdown.

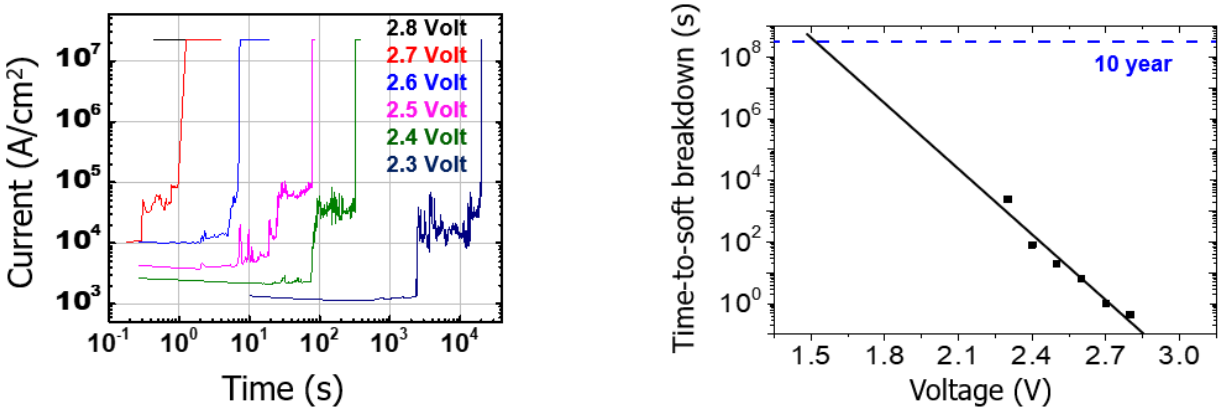

Figure 4.7: time dependent dielectric breakdown characteristics of 10 nm ferroelectric HZO MFM capacitors

4.4.4 Retention tests after baking

Retention tests measure the loss of switchable polarization over time. To do an accelerated aging test, a baking process was performed at different temperatures. Additionally, measurement of polarization at different applied voltages immediately after baking using the same device is unfeasible because of the varied applied voltage history it has experienced. Hence, to perform systematic retention and imprint tests, different devices have to be used to measure polarization at different voltages immediately after baking. Consequently, it is crucial that the device-to-device variation within the sample must be minimal. As shown in Figure 4.2, the average P_r and V_c measured across 25 devices shows a very tight distribution with P_r ~23 ± 0.7 μC/cm^2 and V_c ~ 1.25± 0.03 V. Hence, a total of 16 devices within the same wafer were used to do the retention tests; 8 devices were initiated (write) in the $+P_r$ state and 8 in the $-P_r$ state before baking, so that the polarization after long term baking can be extracted at different voltages (±2.5, ±2.0, ±1.5, ±1.0) for both SW and NSW operation.

The schematic of the measurement pulse sequence for retention tests is shown in Figure 4.8. Pulse measurements were chosen because it is easier to separate the SW and NSW components and replicate actual memory operation. Prior to the retention and imprint tests, all the devices were subjected to the wakeup effect (10^5 cycles at 2.5V).

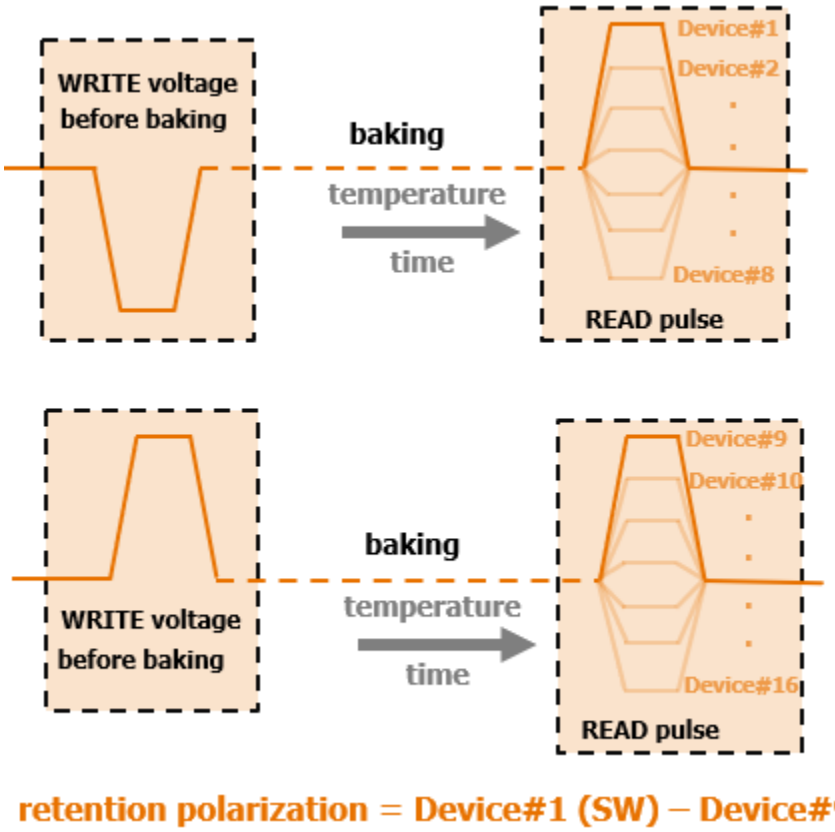

Figure 4.8: Measurement setup for the retention tests after baking. The baking process was performed to accelerate the aging process.

Figure 4.9(a) shows the retention polarization ($P_{retention}$) extracted using the setup shown in Figure 4.8. After long baking hours, the total amount of switchable polarization does not change significantly, but a systematic shift in the V_c is observed. Hence, long term baking does not result in the permanent pinning of FE dipoles as seen during the fatigue measurements, but causes a high voltage requirement for the ferroelectric switching process. The horizontal shift in

the V_c implies that there is a built-in voltage (V_{BI}) that is developed in the FE layer. By subtracting the V_c for a standard device with the V_c of the device after baking, the amount of V_{BI} can be extracted as shown in Figure 4 9(b). The V_{BI} calculated after annealing the -P_r state devices to 95 °C and 110 °C for extended hours are very close to the -V_c of 10 nm HZO FE capacitors and can cause back switching without the presence of an applied bias. Hence, the stability of a re-write after the retention tests is one of the crucial problems in FE reliability (commonly called opposite state failure).[18,31]

Based on the amount of time required for generating a V_{BI} of 0.7 Volt during different temperature baking process, the slope of the log-time vs 1/kT graph was used to calculate the activation energy of the V_{BI} shift. Two different slopes were extracted, baking above 85 °C shows a slope of 0.65 eV, which is the activation of energy of oxygen vacancy migration in HfO_2 films, while the activation energy below 85 °C shows a slope of 0.3 eV which is the activation energy of electron trapping through defect sites.[38]

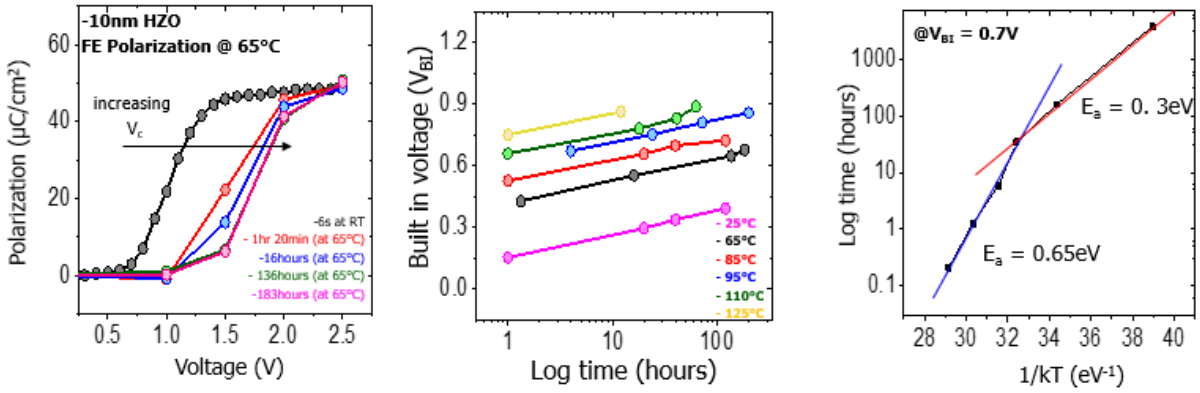

Figure 4.9: $P_{retention}$ obtained after baking the -P_r state devices at 65°C, for different baking time (b) V_{BI} developed in the film due to baking for long periods at higher temperatures. (c) based on the amount of time required to generate a V_{BI} of 0.7 V at different baking temperatures, two different activation energies were calculated.

Hence, based on the requirement of the ferroelectric operation i.e, <85 °C for consumer electronics and the 125 °C requirements for memory devices for automotive industry, the accelerated tests in ferroelectric HZO can be conducted and the reliability properties can be studied.

4.4.5 Imprint tests in HZO films

The imprint tests are reliability tests specific to ferroelectrics. As discussed in the previous section, when the V_{BI} generated in the HZO film is greater than the ferroelectric E_c, back-switching and polarization orientation preference of the ferroelectric domains lead to imprint failures.

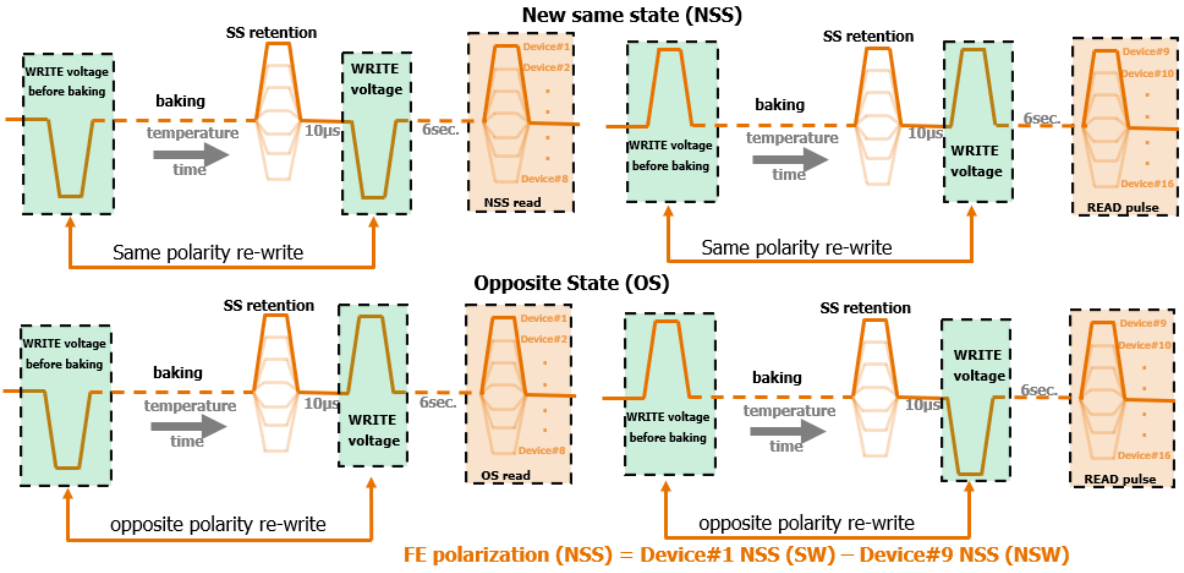

Figure 4.10: A schematic of the new same state and opposite state imprint measurement pulse sequences.

The effect of this imprint in the FE behavior is also carefully studied using subsequent re-write pulses with the same polarity and opposite polarity as the polarization before baking. The ability

to retain the same/opposite polarization (P_{SS}, P_{OS}) state after a re-write to the same/opposite state (called SS/OS imprint) is measured using different voltage read pulses (±2.5, ±2.0, ±1.5, ±1.0) after 6 s as shown in Figure 4.10.

Figure 4.11 (a) shows the comparison of the FE polarization extracted from retention, SS and OS imprint measurements after a 136 hour bake at 65°C.

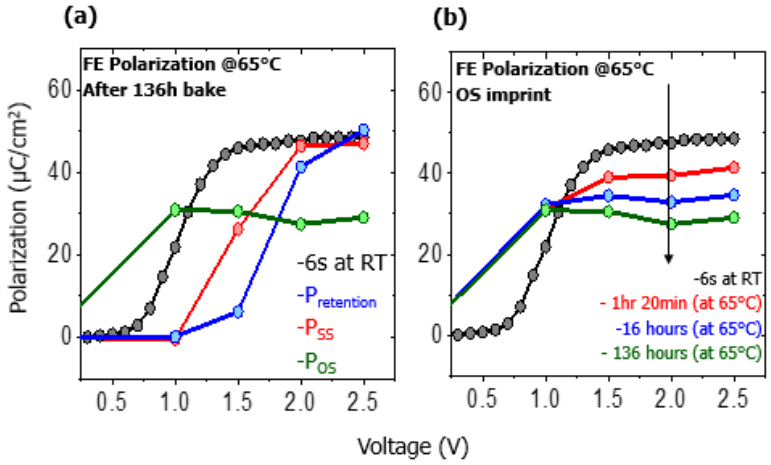

Figure 4.11: (a) Comparison of the $P_{retention}$, P_{SS} and P_{OS} after a 136 hour bake at 65 °C (b) Comparison of the P_{OS} obtained from the OS imprint measurements at 65 °C after different baking times.

The SS imprint shows a reduction in the V_c compared the retention after baking measurements while maintaining the same amount of saturation P_{FE} compared to the standard write/read measurements after 6 s delay at RT. This difference in V_c is believed to be due to the generation of a thermal depolarization field.[18,23] In the case of OS imprint measurements, a reduction in P_{FE} is observed but the FE switching process happens at a much lower voltage (even at ±1V) compared to the standard write/read measurements. This implies that during the OS imprint measurements, the FE switching process has lower voltage requirements, but the number of switchable dipoles is lower. Since the total number of switchable FE domains does not

change, this reduction in P_{FE} means that some of the FE domains back switch during the 6 s relaxation time after the re-write in the OS. Figure 4.11(b) shows a systematic reduction in the amount of P_{FE} during the OS imprint measurements. After 136 hours at 65 °C, almost 40% of the stored polarization is lost during the 6 s relaxation time.

Several mechanisms explaining the reasons for the formation of such V_{BI} have been extensively discussed in conventional FE materials like PZT, SBT, etc.[32-34] One of the commonly used mechanisms to describe this effect is the bulk screening model, where charge matching between the dead interface layer and the FE results in the formation of such depolarization fields. In PZT and SBT, the coercive field (E_c) is very less (~100 kV/cm), making the role of the interface layer capacitance significant.[32,35] However, in the case of HZO films (E_c of 1.2 MV/cm), if we assume a 2 nm TiO_x interface, with a dielectric constant of 70,[39] the internal depolarization field extracted based on Gong et al.'s equation[35] was approximately 0.2 MV/cm, which was very minimal compared to the E_c of HZO. Hence the effect of bulk screening in HZO based MFM capacitors is very minimal. Research in FE $BaTiO_3$ (BTO) has pointed out that the defect dipole alignment mechanism could be responsible for the formation of built-in fields.[33,36] Based on this model, the alignment of FE domains after the FE switching process creates a field due to the trapped charges, defects, and oxygen vacancies in the film, making them move towards the interface. Although this effect is not as drastic as bulk screening in MFIS capacitors,[24] the presence of trapped charges can severely deteriorate the device performance. Based on this mechanism, the reduction in V_c after a re-write to the SS can be validated due to the de-trapping of charges from the $TiON_x$ interface. Figure 4.12 shows the mechanism of V_{BI} generation and charge trapping/de-trapping leading to OS imprint loss in FE HZO films. When

combined with a high temperature baking, the built-in field leads to more facile migration of defects and vacancies.

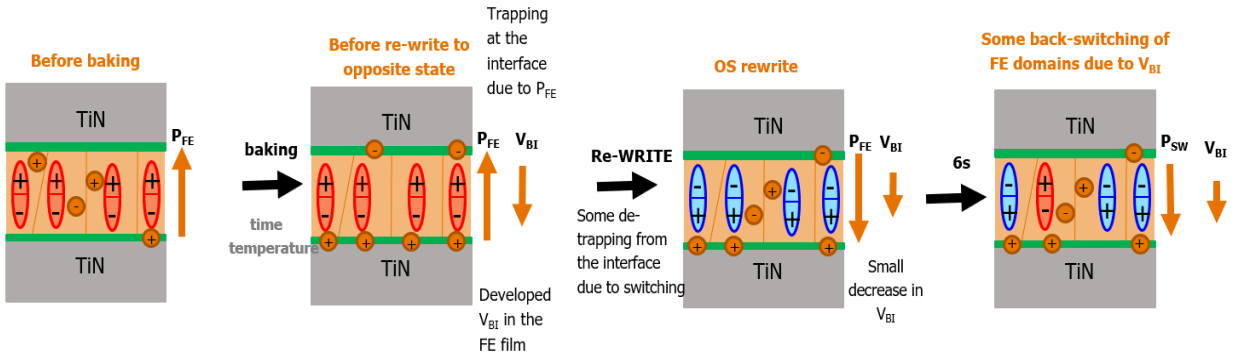

Figure 4.12: V_{BI} generation and charge trapping mechanism leading to OS imprint loss in HZO FE films.

Based on the amount of V_{BI} developed, as obtained from the retention measurements, using charge neutrality conditions,

$$Q_{interface} = n_{dets} * e = C_{FE} \cdot V_{BI} \quad (1)$$

From the V_{BI} extracted from the V_c shifts and the NSW capacitance of the HZO film, if we assume that all charges are trapped at a 2-D interface, then the number of defects/cm^2 is of the order of 10^{13}. This number may seem very high for a 2-D surface, but, in reality, the interface has some thickness to it as well. Hence, reducing the trapped charge density in the film and the thickness of the interface will be the key to realizing stable FE properties.

Established on the retention properties and P_{FE} extracted after different baking times at various temperatures, the lifetimes of the devices for read pulse amplitudes of ±2.5V and ±2V was extrapolated for $P_{retention}$, P_{SS} and P_{OS} are shown in Figure 4.13(a). In this study, 80 % P_{FE} degradation is considered as the time to failure (TTF). As expected, the P_{OS} shows more severe failure, compared to $P_{retention}$ and P_{SS}. At 65°C, a lifetime of >10 years was extracted based on the

5 µs pulse used at 2.5 V. For 2.0 V operation with the same pulse width at 65°C, a lifetime of the 0.6 years was extracted. In the case of 95 °C and 110 °C, drastic failure was observed, and a lifetime of less than 20 hours was extracted.

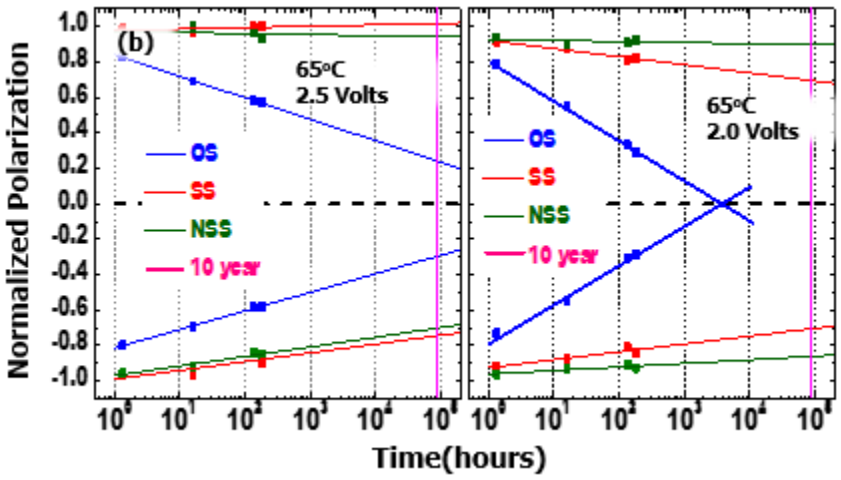

Figure 4.13: (a) Lifetime extraction for $P_{retention}$, P_{SS}, and P_{OS} at 65 °C after different baking times. OS shows the most drastic degradation in the retention properties

Based on the understanding of charge trapping at the interface due to P_{FE}, a long re-write voltage pulse can cause de-trapping of the charges at the interface and reduce the amount of P_{OS}. Hence, the effect of pulse width was studied systematically using 16 different devices. The P_{OS} measurements were performed at ±2.5 V after a ±2.5 V re-write for different pulse widths (5µs, 10 µs, 100 µs, and 1 ms) as shown in Figure 4.14(a). 5µs was chosen as the lower limit because of RC delay issues due to device size and capacitance. As shown in Figure 4.14(b), the P_{OS} value increases with increase in the re-write pulse width. After a 24 hour bake at 95 °C, the P_{OS} increases from 6 µC/cm^2 for 5 µs to 40 µC/cm^2 when using 1 ms pulse width. This ~80% increase in polarization cannot be neglected and hence the effect of pulse width for the retention and imprint measurements is very crucial. Also, after a 72 hour bake at 95 °C using 5 µs, the P_{OS}

value is less than 0 μC/cm^2 (which is a negative value indicating failure) but using a 1 ms pulse width shows polarization of ~34 μC/cm^2. The effect of failure lifetime based on the re-write pulse widths was studied as shown in Figure 4.14(c). It can be seen that using a 1 ms pulse shows close to 10-year lifetime for operation at 95 °C and 110 °C, compared to the less than 20 hours lifetime using 5 μs pulses. Several reports in the literature use large pulse widths (~ms range) for the retention and imprint tests[23,25-26], which can over-estimate the lifetime. The actual operation of ferroelectric devices is in the range of a few ns, and proper studies must be done to ensure a stable lifetime in that regime.

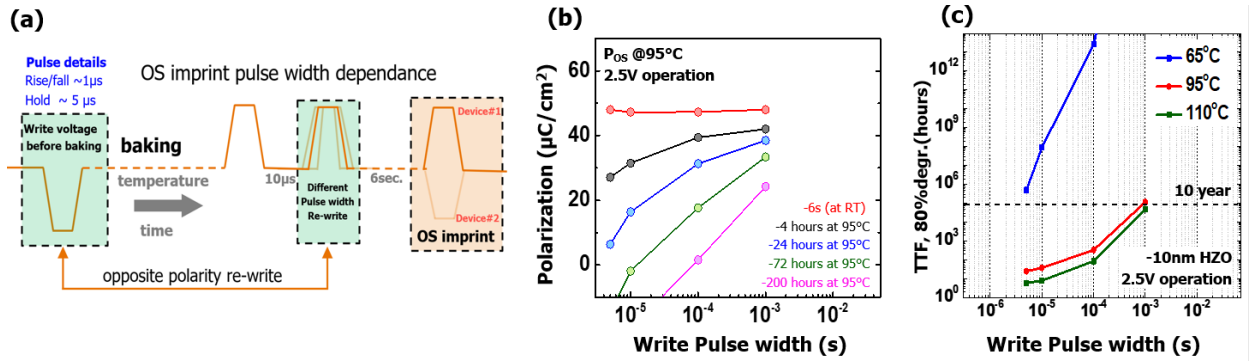

Figure 4.14: (a) pulse sequence to measure OS imprint with different re-write pulse widths, (b) P_{OS} at 95 °C for various write pulse widths extracted at different baking times (c) lifetime extraction based on different write pulse widths for 65 °C, 95 °C, and 110 °C.

In addition, the asymmetric shift in the V_c based on baking time and temperature was studied using P-V hysteresis measurements. After a 200 hour anneal at 95 °C, a 0.9 V shift in the hysteresis was observed, similar to the pulse measurements. This shift in hysteresis was explained due to charge trapping at the interface. A complete recovery effect was observed after field cycling at 2.5 V for 10^5 cycles using 5 μs wide pulses, as shown in Figure 4.15(a). The effect of V_c recovery after field cycling is consistent with other reports for HfO_2 based FE

films.[37] Redistribution of defects and vacancies during field cycling is an accepted mechanism for endurance FE HZO films[20-22]. As shown in Figure 4.15(b), the redistribution of defects trapped at the interface after long baking at higher temperatures with field cycling can explain the recovery effect. Hence, the defect dipole alignment model perfectly explains retention and imprint behaviors in FE HZO films and reducing defects and trap charges in the HZO film will be key to realizing reliable FE properties.

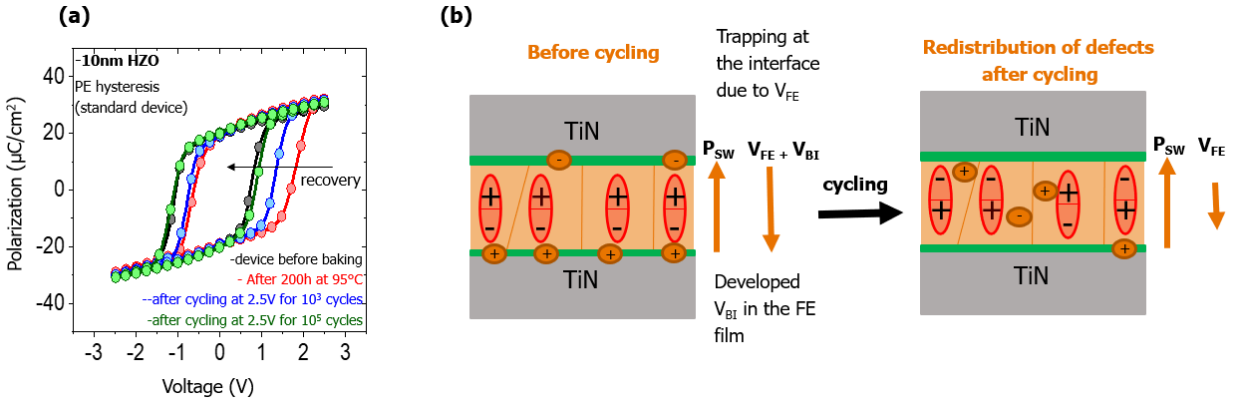

Figure 4.15: (a) Recovery of imprint effects after cycling, and (b) mechanism of redistribution of defects after cycling.

4.5 Conclusions

In summary, we have investigated the data retention and imprint characteristics of 10 nm-HZO films accelerated by temperature. Shifts in the polarization-voltage hysteresis were observed in a pre-poled ferroelectric based on baking temperature (65 °C ~ 110 °C) and time (1 hour to 200 hours). After baking to 95 °C, this shift is close to the coercive voltage of the ferroelectric, and the stability of polarization is degraded due to back-switching. The amount of voltage shift corresponds to the defects accumulating at the interface and using longer switching pulses or switching cycles can de-trap these charges from the interface. It was seen that the

devices that were baked at 95 °C and 110 °C, show less than 20 hours lifetime when 5 µs pulses were used. Increasing the pulse width to 1 ms showed a strong recovery effect, demonstrating a stable operation for close to 10 years. Some of the retention tests in the literature use long write-pulse widths (~1 ms) for their retention and imprint tests[23,25-26], which are impractical and may show optimistic ferroelectric device lifetime. Additionally, after 10^5 switching cycles at 2.5 V, the devices degraded by a 95 °C baking for 200 hours, showed almost complete recovery.

4.6 References

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CHAPTER 5

SCALING FERROELECTRIC HZO ON SILICON TO REDUCE THE EOT TO LESS THAN 1 nm AND THE EFFECTS OF BUILT-IN FIELD

5.1 Preface

To realize ferroelectric devices for FET applications, reducing the EOT of the gate oxide, while maintaining the ferroelectric properties of the oxide is crucial. In this work, the key focus is to investigate scalability of ferroelectric HZO films as a gate dielectric by reduction in the thickness of the ferroelectric films and reduction in the thickness of the interfacial SiO_x formed due to integration with silicon. The direct integration of ferroelectric HZO ($Hf_{0.5}Zr_{0.5}O_2$) on silicon, and achieving ferroelectric properties in HZO thickness less than 5 nm thick was studied. By correlating the electrical measurements to high energy synchrotron Grazing Incidence X-ray diffraction (GI-XRD) and high-resolution transmission electron microscope (HR-TEM), the lowest EOT of 0.9 nm was extracted using 5 nm HZO, while confirming the presence of the ferroelectric phase. A direct observation of oxygen scavenging from the bottom SiO_x interfacial layer was also observed in 3 nm HZO after the 400 °C annealing process. 4 nm or thinner HZO, however, shows amorphous phase with 400 °C PMA annealing. The effects of re-annealing to higher temperatures on the ferroelectric phase crystallization in HZO thin films was also studied. Also, the effect of voltage dividing and the built-in field generated due to integration of ferroelectric films on silicon substrates was studied carefully using degenerate silicon substrates.

The contents of this chapter are mainly divided into two sub-sections, (i) focusing on scaling and reducing the EOT of the ferroelectric/dielectric, and (ii) study of the built-in field issues of ferroelectric devices integrated on silicon. The first section includes contents which is

unpublished, and the manuscript is under preparation for a peer reviewed journal. The second section includes the published material entitled "*ferroelectric polarization retention with scaling of $Hf_{0.5}Zr_{0.5}O_2$ on silicon*" by *Applied Physics Letters* and is reprinted from Ref [33]. Copyright (2021) AIP Publishing. The authors are Jaidah Mohan, Heber Hernandez-Arriaga, Yong Chan Jung, Takashi Onaya, Chang-Yong Nam, Esther H. R. Tsai, Si Joon Kim and Jiyoung Kim. In this work, my contribution was to design the experiments, perform the fabrication, characterization, data analysis, TEM imaging and preparation of the manuscript. Dr. H. H. Arriaga, Y. C. Jung, T. Onaya helped with the fabrication and Prof. Sijoon Kim gave valuable inputs in preparing the manuscript. C. Y. Nam and E. Tsai helped in performing beamline experiments at Brookhaven National Laboratory. Prof. Jiyoung Kim guided the experiments and contributed to the manuscript.

This work was supported by Samsung Advanced Institute of Technology (SAIT).

5.2 Scaling ferroelectric HZO on silicon and reducing the EOT to less than 1nm

5.2.1 Introduction

To realize ferroelectric (FE) $Hf_xZr_{1-x}O_2$ (HZO) as a gate dielectric for logic devices, scaling the equivalent oxide thickness (EOT) to less than 1 nm while maintaining the orthorhombic phase is a crucial step. In this study, we will employ two different strategies to reduce the EOT. Firstly, we scaled HZO thickness on SC-1 and HF last processes on silicon. (O_3 was used as an oxidant for the deposition of HZO films) Secondly, the role of TiN electrode in scavenging effects[1] with reducing thickness of HZO has to be studied.

There could be several challenges for this study. (i) Maintaining the orthorhombic phase of the FE layer for HZO for thickness less than 4 nm. (ii) Also, it is not clear if scavenging effects of TiN can affect the ferroelectric phase stability of the HZO layer.

From the list of oxides which are energetically more favorable than SiO_x, metal electrodes will be deposited such that the interfacial SiO_x layer thickness can be reduced. Based on the reaction equilibrium in equation 1, if ΔG is positive, reduction of SiO_2 is more favorable. The list of all oxides which are energetically more favorable than SiO_2 is shown in Table 1.

$$Si + MO_x \rightarrow M + SiO_2 \text{ ---------- (1)}$$

Table 5.1: List of oxides that are energetically less favorable for the forward reaction of equation (1) [2]

MO_x	ΔG^o1000K
La_2O_3	-98.48
Nd_2O_3	-101.692
Gd_2O_3	-101.549
TiO	-17.849
Ti_2O_3	-35.432
TiO_2	-7.527
ZrO_2	-42.326
HfO_2	-47.648

Furthermore, extracting the capacitance oxide thickness (CET) and equivalent oxide thickness (EOT) of scaled devices could be tricky due to the leakage currents and parasitic capacitances. CVC modeling[34] was used to extract the EOT carefully.

5.2.2 Experimental : HF last and SC-1 last processes

The low doped p-Si ($10^{15}/cm^3$) was used as the substrate for the EOT scaling study. The standard RCA cleaning procedure[35] is done at UTD cleanroom. The steps for the RCA cleaning procedure are shown in Figure 5.1.

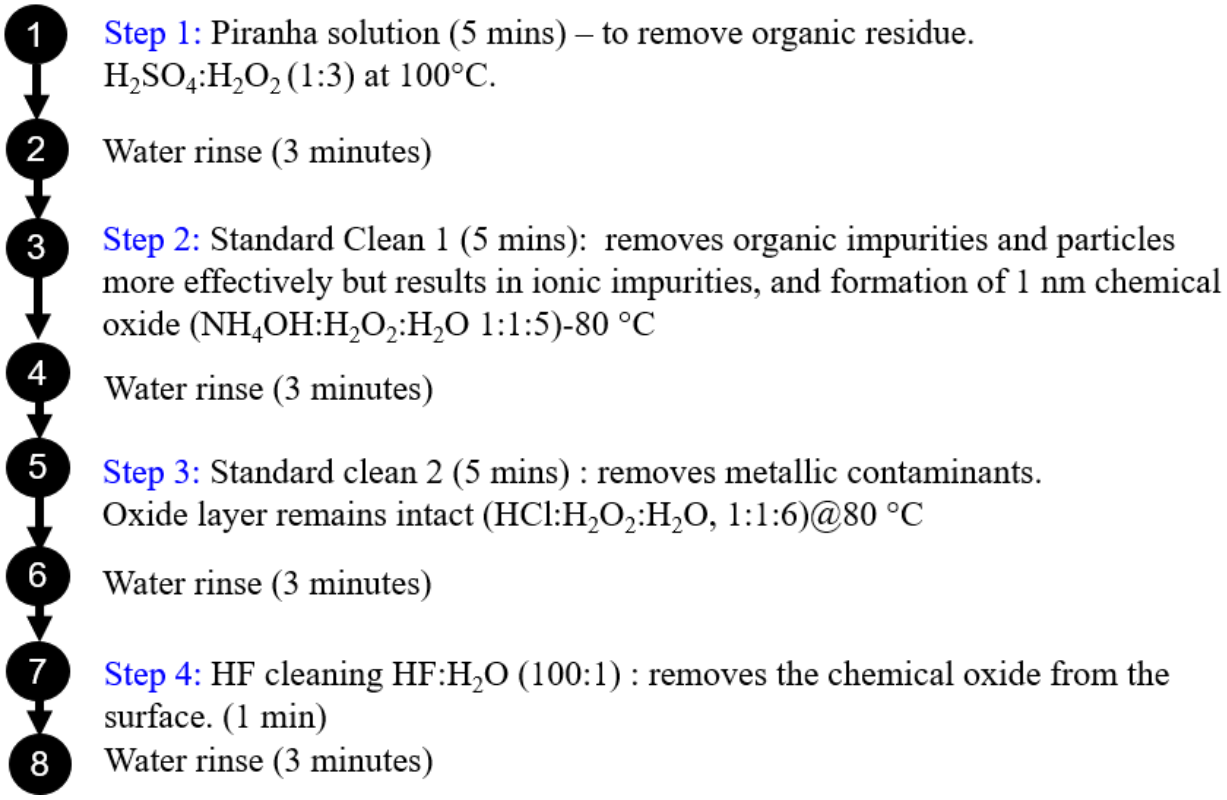

Figure 5.1: Standard RCA cleaning procedures done at the UT Dallas cleanroom

Each of the RCA cleaning steps is done using individual quartz baths reserved for only that chemical so that there is no presence of unwanted impurities from the container. After RCA cleaning, the silicon surface was hydrophobic, indicating that all the SiO_2 is removed, and Si-H bonds have been formed.[3-5] Two types of processes have been used, the first process, called the "HF last process" involves RCA cleaning with HF cleaning as the last step and the other process

called the “SC1 last process” which involves RCA cleaning and then further treatment with SC1, i.e., $NH_4OH:H_2O_2:H_2O$ in the ratio 1:1:5 at 80°C. SC1 treatment for 5 mins results in a saturated 1.2 nm Chemical SiO_2 on the silicon surface.[35] This process is done because direct deposition of HZO on silicon results in the formation of silicate which can be the source of interface traps in the gate oxide. The ellipsometry measurements done after the SC-1 last process (shown in Figure 5.2) shows 1.23 nm of chemical SiO_x formation after SC-1 last process.

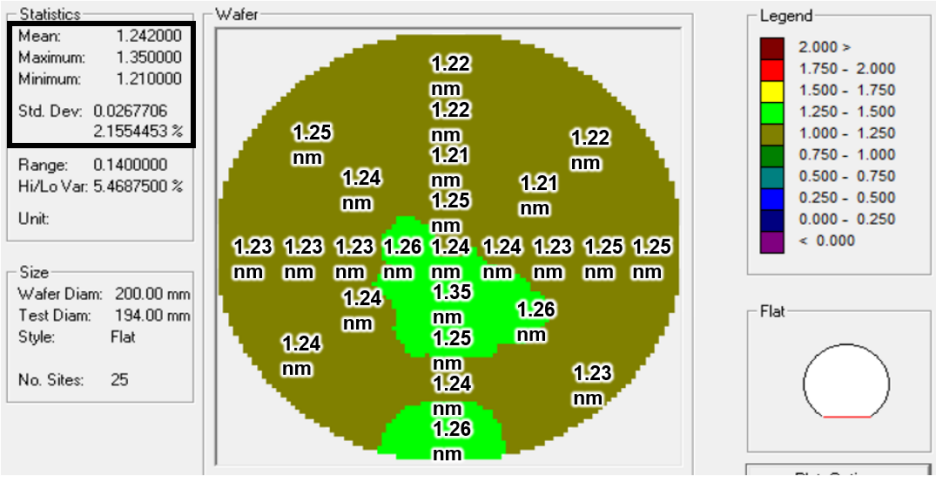

Figure 5.2: Ellipsometry showing wafer uniformity of chemical SiO_2 grown on silicon substrate using SC-1 last process after RCA cleaning procedures.

The fabrication process is shown in Figure 4. After RCA cleaning, HZO is deposited using thermal ALD at 250 °C using TDMA-Hafnium, TDMA-Zirconium or O_3 as the Hf-precursor, Zr-precursor and oxidant source respectively. 90 nm TiN is deposited using RF magnetron sputtering using a titanium target Ar and N_2 gas at 250 W. After TiN deposition, Rapid thermal annealing (RTA) is done at 400 °C for 60 s in N_2 ambient. A standard photolithographic/etching process is done and Au/Pd is used as a hard mask for the TiN etching process to form capacitors.

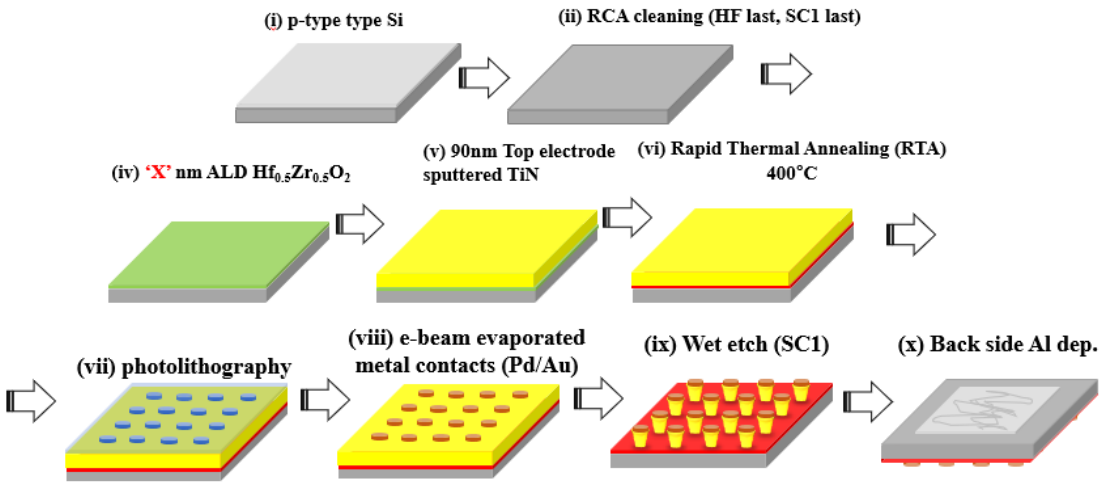

Figure 5.3 : shows the detailed fabrication process flow for making MFIS capacitors

5.2.3 Results and Discussions

Using the HF last process and O_3 as oxidant for the ALD deposition, $Hf_{0.5}Zr_{0.5}O_2$ of various thickness (10 nm, 7 nm, 6 nm, 5 nm, 4 nm and 3 nm) were deposited on the RCA cleaned silicon surface. Capacitors of 50 µm, 75 µm and 100 µm were fabricated. The Capacitance Voltage (C-V) curves at 10 kHz and 100 kHz annealed at 400 °C are shown in Figure 5.4. As the HZO thickness decreases, the observed hysteresis in the CV curves also decreases, because of a decrease in fixed oxide charges. The presence of "humps" in the CV curves indicate the presence of interface trapped charges. The amount of frequency dispersion between 10 kHz and 100 kHz CV curves was almost 5% for various thickness of deposited HZO, indicating lower impact of parasitic and leakage current components in the measurements (parasitic components can arise from the measurement circuit).

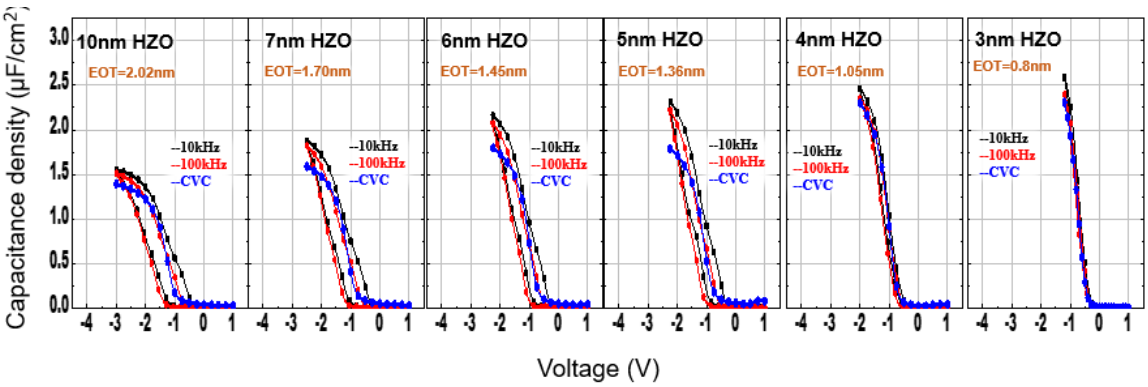

Figure 5.4 : Capacitance-voltage curves for HF last process for various thickness of $Hf_{0.5}Zr_{0.5}O_2$ annealed at 400°C at 10 kHz and 100 kHz frequencies.

4-5 nm HZO was found to be the region of phase-transition from ferroelectric to amorphous at 400°C. EOT was extracted from the CVC analysis of the CV curves. The slope of EOT vs HZO thickness can be used to extract the dielectric constant of the HZO layer, and the intercept can be used to estimate the thickness of the interface SiO_x/silicate. From the CVC fitting, as shown in Figure 5.5, a dielectric constant of 35 was extracted between HZO thickness of 10 nm to 5 nm for HF last process. This agrees with the dielectric constant of -O phase HZO reported in the literature.[5,9,10] Below 5 nm, a different slope of dielectric constant of 18 was extracted.

$$EOT = 3.9 \times {}^{t_{HZO}}/_{\varepsilon_{HZO}}$$

The dielectric constant of 35, corresponds to the dielectric constant of the ferroelectric o-phase HZO. The films below 4 nm can be expected to be amorphous with a dielectric constant of 18. It is also to be noted that below 4 nm HZO there is a possibility of SiO_x scavenging at 400°C by the TiN electrode. This could be the reason for lower extracted dielectric constant than the theoretical (~22-24) dielectric constant of amorphous HZO.

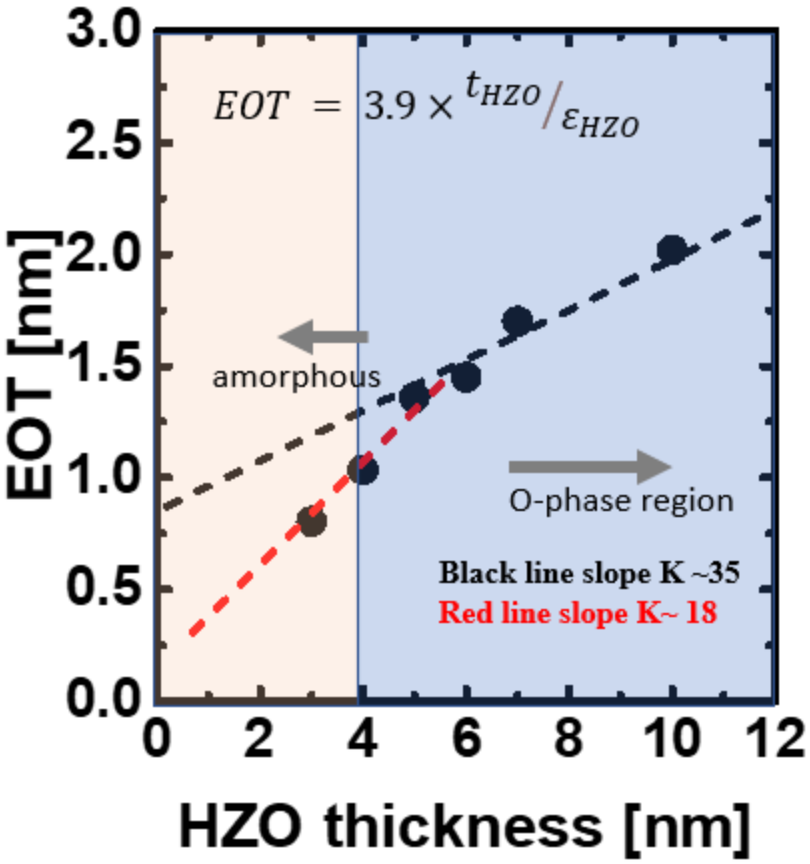

Figure 5.5: EOT extracted from C-V curves for different thickness of HZO annealed at 400°C using H_2O as oxidant for HF last process. Blue dot shows the 5 nm HZO fabricated during a different batch with high EOT of 0.9 nm.

Additionally, it can be seen from Figure 5.6 that as the thickness of HZO decreases, there is an increase in leakage current, and a decrease in breakdown voltage in the accumulation region (negative applied voltage) as expected. The leakage current in the depletion region (positive applied voltage region) also increases as HZO thickness decreases.

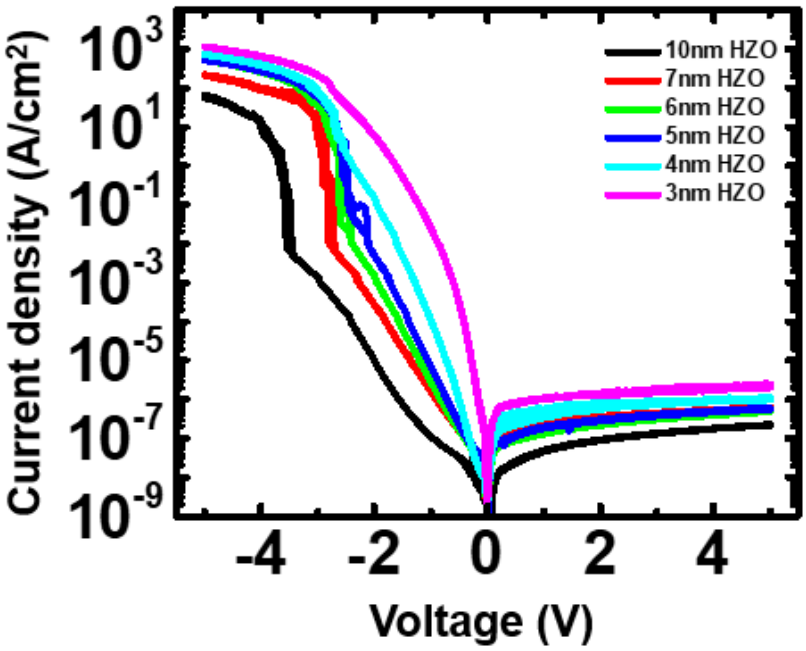

Figure 5.6: Leakage currents for HF last process for various thickness of $Hf_{0.5}Zr_{0.5}O_2$ annealed at 400°C

Similarly, when using SC1 last process, as the HZO thickness decreases, the observed hysteresis in the CV curves also decreases, because of decrease in fixed oxide charges. The amount of frequency dispersion between 10 kHz and 100 kHz CV curves was almost 10% for various thicknesses of deposited HZO, indicating that the interface is thickness reduces, leading to higher leakage current during measurements. The EOT was also extracted from the CVC analysis of the CV curves. From the CVC fitting as shown in Figure 5.7, the dielectric constant of 35 was extracted between HZO thicknesses of 10 nm to 5 nm using SC1 last process. Below 5 nm, a different slope of dielectric constant of 20 was extracted.

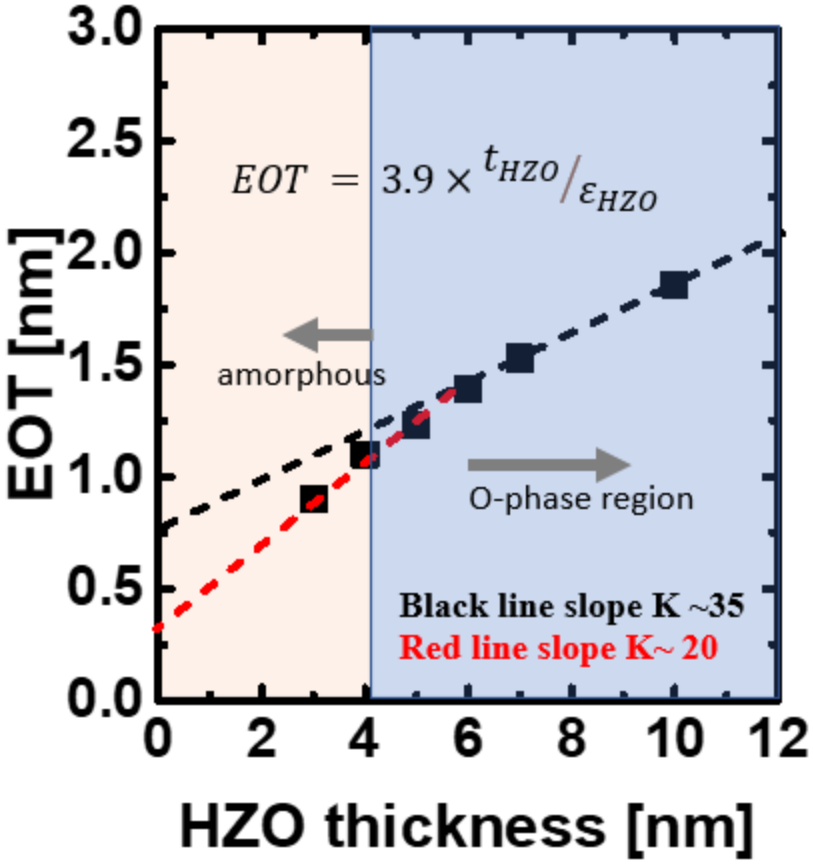

Figure 5.7: EOT extracted from C-V curves for different thickness of HZO annealed at 400°C using H_2O as oxidant for SC1 last process.

High resolution transmission electron microscopy (HR-TEM) was used to measure the thickness of the interfacial SiO_x/silicate layer, and to confirm the presence of the ferroelectric o-phase in the HZO layer. Crystalline grains with d-spacing of 2.94Å, which is the d-spacing of orthorhombic (111) phase was observed in the TEM images of 5 nm HZO on HF last silicon using O_3 as oxidant, annealed at 400 °C as shown in Figure 5.8. 1nm interfacial silicate/ SiO_x layer was observed at the interface of HZO and silicon.

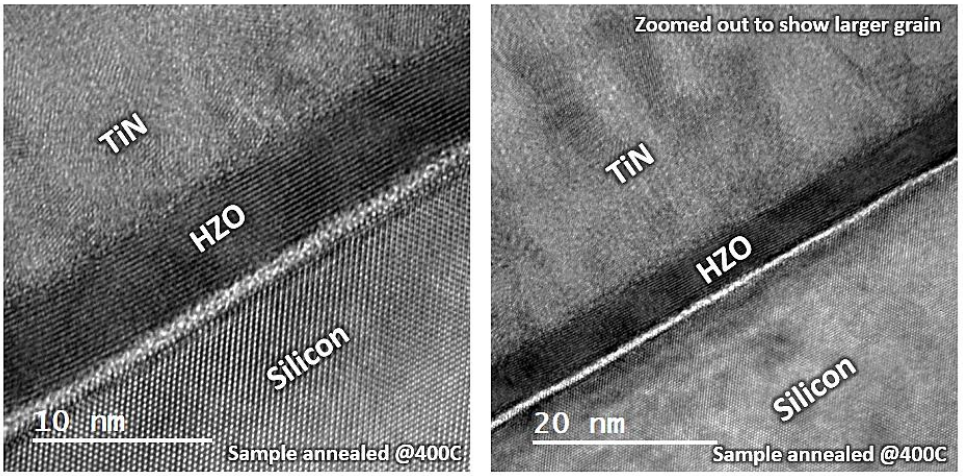

Figure 5.8: TEM images showing uniform crystalline orthorhombic grains of 5 nm HZO using O_3 on HF-last silicon.

Also, from the HR-TEM images of HZO on SC1 last silicon, when the thickness of HZO is decreased to 3 nm, and the annealing process is performed at 400 °C after the TiN top electrode deposition, a decrease in the bottom interfacial SiO_x layer thickness from 1.3 nm to less than 0.7 nm was observed as shown in Figure 5.9. This effect can be explained because of the scavenging of SiO_x to the TiN electrode.

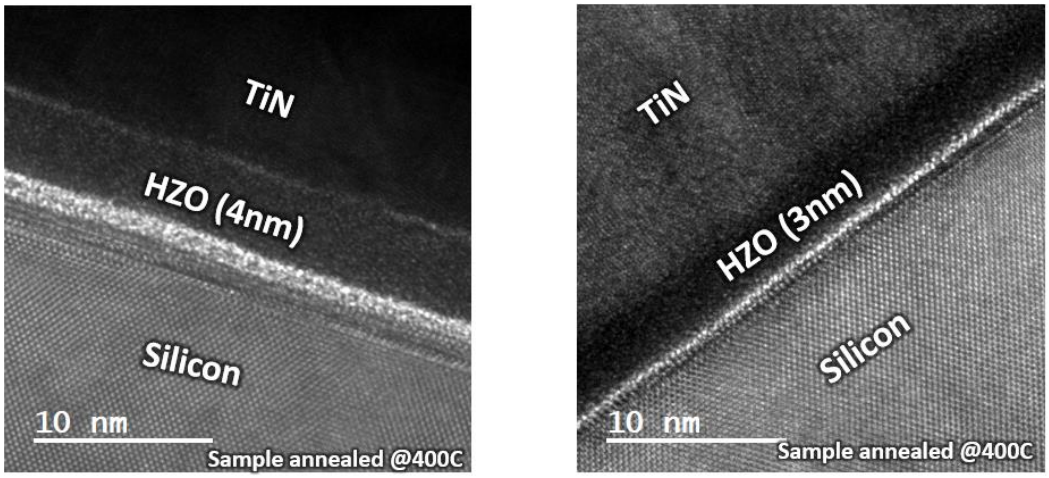

Figure 5.9: HR-TEM images of 4 nm and 3 nm HZO using O_3 on SC1 last process.

At thickness below 5 nm HZO, laboratory-based GI-XRD cannot provide the resolution to identify the o-phase peaks (the X-ray beam intensities are too small to get detectable diffraction resolution). Hence, The X-ray analysis was conducted at 12-ID beamline at the National Synchrotron Light Source-II (NSLS-II) located in Brookhaven National Laboratory, NY. The incident angle was set at 0.15°. This angle was chosen such that there is minimum intensity from the background Si peaks and maximum intensity from the HZO layer. Based on the X-ray intensity, the depth of penetration of the X-rays for the incident angle of 0.15° is approximately 7 nm. The samples were characterized under dynamic vacuum environment (<1 mTorr) to minimize non-sample scattering intensities. A background scattering pattern is also subtracted from the scattering patterns to reduce instrument originated contributions.

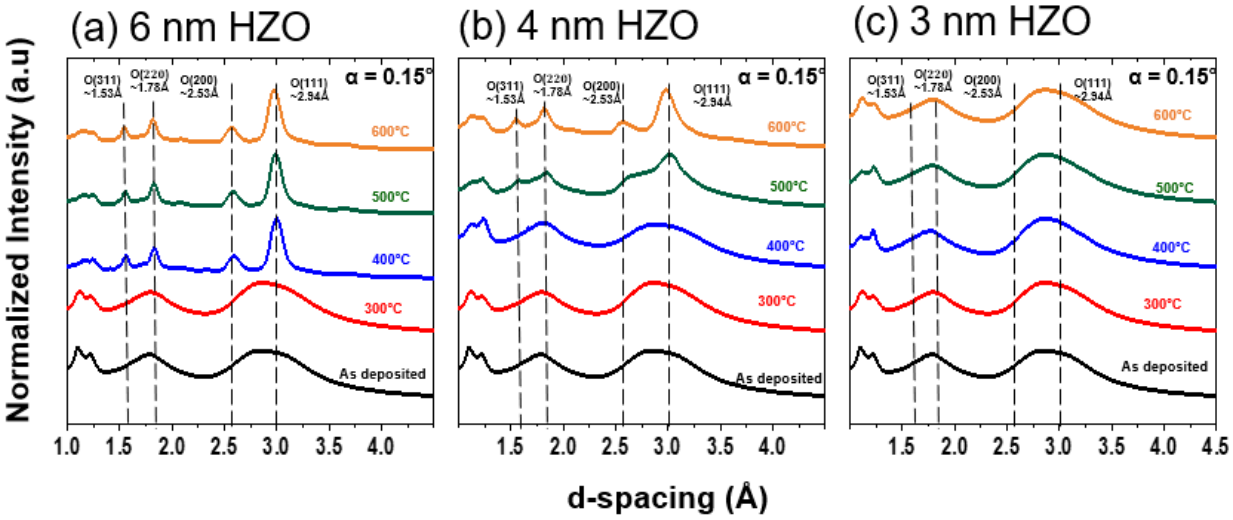

Figure 5.10: GI-WAXS on 6 nm, 4 nm and 3 nm HZO deposited using O_3 on SC1 last silicon annealed at different temperatures.

It is seen from Figure. 5.10, that 6 nm HZO films can be crystallized to the ferroelectric phase by rapid annealing at 400 °C for 1 min but 4 nm HZO requires 600 °C for complete film crystallization. At 500 °C, partial crystallization was observed, which is indicated by a lower

peak intensity. Annealing 3 nm HZO even to 600 °C does not show the desired -O phase for HZO, as confirmed by GI-WAXS.

To compare the EOT of o-phase HZO, and the EOT of films which are amorphous, MOSCAPs were fabricated using amorphous HZO without any annealing process. As shown in Figure 5.11, without the annealing process, the dielectric constant for HZO was 24 and 26 for HZO deposited on HF last and SC1 last silicon, using O_3 as oxidant. It should also be noted that without the annealing process, the scavenging effects of the SiO_x interface will not be significant.

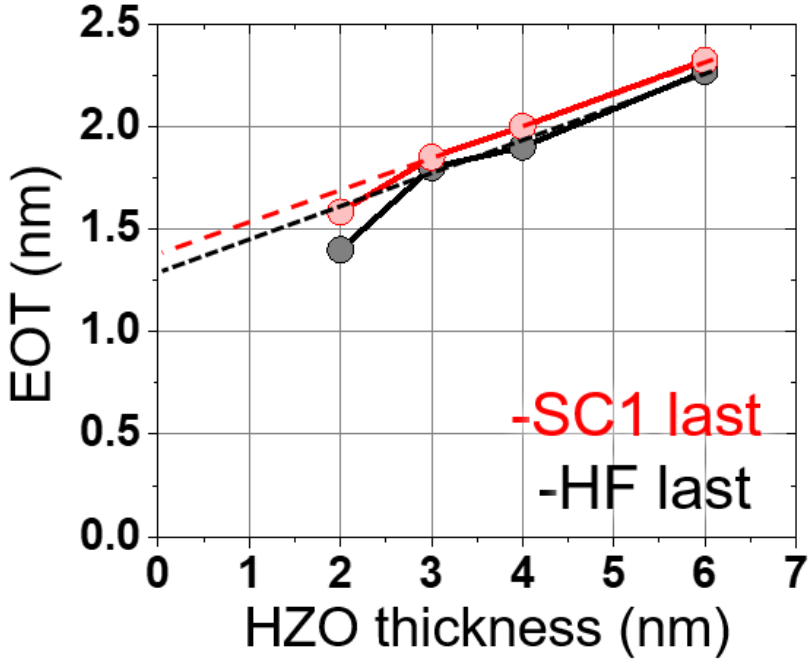

Figure 5.11: EOT extracted for non-annealed $Hf_{0.5}Zr_{0.5}O_2$ on HF last and SC1 last silicon using O_3 as the oxidant.

At 400 °C annealing, the EOT extracted for 5 nm HZO using O_3 on SC1 last silicon showed the lowest EOT of 0.9 nm while maintaining the desired ferroelectric o-phase. The 3 nm HZO using HF/SC1 last has an EOT of 0.8 nm, but the films are amorphous in nature. Further annealing to higher temperatures (500 °C) can help in obtaining the ferroelectric phase in 4 nm

and below but there could be a trade-off between the device leakage currents at higher temperatures which need to be studied extensively.

5.3 Ferroelectric polarization retention with scaling of $Hf_{0.5}Zr_{0.5}O_2$ thickness on silicon

5.3.1 Introduction

Over the past few decades, ferroelectricity has been extensively studied for non-volatile memory (NVM) and ferroelectric field-effect transistor (FeFET) applications.[5–8] Since the recent discovery of ferroelectricity in very thin doped-HfO_2 films[5,6], a great deal of interest has been kindled in the semiconductor community because ferroelectric HfO_2 can be readily integrated with complementary-metal-oxide-semiconductor (CMOS) without concern about material compatibility issues faced by conventional FEs like $Pb(Zr,Ti)O_3$ (PZT) and $SrBi_2Ta_2O_9$ (SBT).[11-14.] In particular, there has been a focus on the interactions between ferroelectric/dielectric (FE/DE) bilayers and metal-ferroelectric-insulator-Si (MFIS) structures. These stacks are of great interest because of the predicted and observed "charge boosting" that renders the semiconductor surface potential higher than the applied voltage.[15,16] Also, understanding MFIS structures is of high importance for FeFETs ,which have been investigated for the fabrication of analog type non-volatile memristors for neuromorphic and steep slope device applications.[17-20]

It has been discussed in the literature that the presence of depolarization fields in a FE/DE/semiconductor heterostructure leads to the reduction in the measured remnant polarization (P_r) values.[6,21,22] Meanwhile, it is also expected that capacitance matching between the FE and interface layers lead to the formation of a built-in potential due to the charge continuity between FE polarization (P_{FE}) and charge of the interface layer, without the presence

of an external bias.[23] There are, however, not many experimental reports discussing the effects of the built-in potential on FE characteristics in MFIS structures. In this section, the FE polarization retention for 6 sec, as a function of FE thickness in MFIS capacitors using degenerate Si as a conducting bottom electrode was investigated, in order to avoid significant Si depletion effects. Using a series connection between a 7 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) metal-FE-metal (MFM) capacitor and a 5 nm HfO_2 metal-oxide-semiconductor (MOS) capacitor with degenerate n-Si as the bottom electrode, we have also directly measured a residual voltage at the MFM and MOS interface node after the FE switching process at the ground state (at $0V_{appl}$).

5.3.2 Experimental Methods

HZO thicknesses of 20, 10, 7, and 5 nm were deposited directly on top of HF treated n-type degenerate Si substrate (10^{20} /cm^3 doping density and a resistivity of ~0.001 Ω•cm). Degenerate Si was used to circumvent the effects of voltage dividing and depletion capacitance in the semiconductor layer. HZO was deposited with a Hf:Zr ratio of 1:1 using atomic layer deposition (ALD, Cambridge Nanotech Savannah S100). Tetrakis-dimethylamido-hafnium ($Hf[N(CH_3)_2]_4$, TDMA-Hf, Aldrich), tetrakis-dimethylamido-zirconium ($Zr[N(CH_3)_2]_4$, TDMA-Zr, Aldrich), and O_3 were used as the Hf-precursor, Zr-precursor, and oxygen source, respectively. High concentration O_3 (400 g/m^3) used in this work was formed by an O_3 generator (OP-250H, Toshiba-Mitsubishi-Electric Industrial Systems Corporation (TMEIC)). The wafer temperature was set to 250 °C during HZO deposition and the growth rate per supercycle of HfO_2 and ZrO_2 was ~0.2 nm/supercycle. RF magnetron sputtering was used to deposit 70 nm TiN as a top electrode (TE). Rapid thermal annealing (RTA) at 450 °C was done for 60 s in N_2 ambient. MFIS capacitors were fabricated using a conventional photolithography and etching

using a Pd/Au hard mask. The over-etching values are estimated by linear extrapolation of device diameter as a function of the square root of the capacitance. To corroborate the presence of FE orthorhombic phase (O-phase), grazing incidence-wide angle X-ray scattering (GI-WAXS) was performed at 12-ID SMI beamline at the National Synchrotron Light Source-II (NSLS-II) at Brookhaven National Laboratory.

5.3.3 Results and Discussions

The incident angle was set at a low angle of 0.15°, such that there is minimized intensity from the background Si peaks, and the intensity from the HZO layer is maximized. Based on the X-ray intensity, the X-ray penetration depth at 0.15° incidence angle is approximately 7 nm.[20] Figure 5.12(a) shows the GI-WAXS spectra of HZO films of various thicknesses. The diffraction peaks in the spectra are identified to be originating from a polycrystalline O-phase HZO. Even the 5 nm HZO annealed at 450 °C shows good O-phase formation without the observation of the equilibrium non-polar monoclinic phase (M-phase). It can also be observed that the O(111) peak maximum of 20 nm HZO (d-spacing ~2.93 Å) does not exactly overlap with those of 10, 7 and 5 nm HZO (d-spacing ~2.96 Å). This observation can be attributed to the presence of a less tensile strained 20 nm HZO poly-crystalline film[9]. Also, a broader O(111) peak can be observed in the 20 nm HZO sample. This peak can be deconvoluted to the M(111) phase with d-spacing 2.84 Å. M($11\bar{1}$) peaks with d-spacing of 3.15 Å can also be observed in the 20 nm HZO sample. These results indicate that for HZO thickness of 20 nm HZO and above, the tensile stress generated from the TiN top electrode is insufficient for complete O-phase crystallization and the equilibrium m-phase of HZO can also be observed.[7,25]

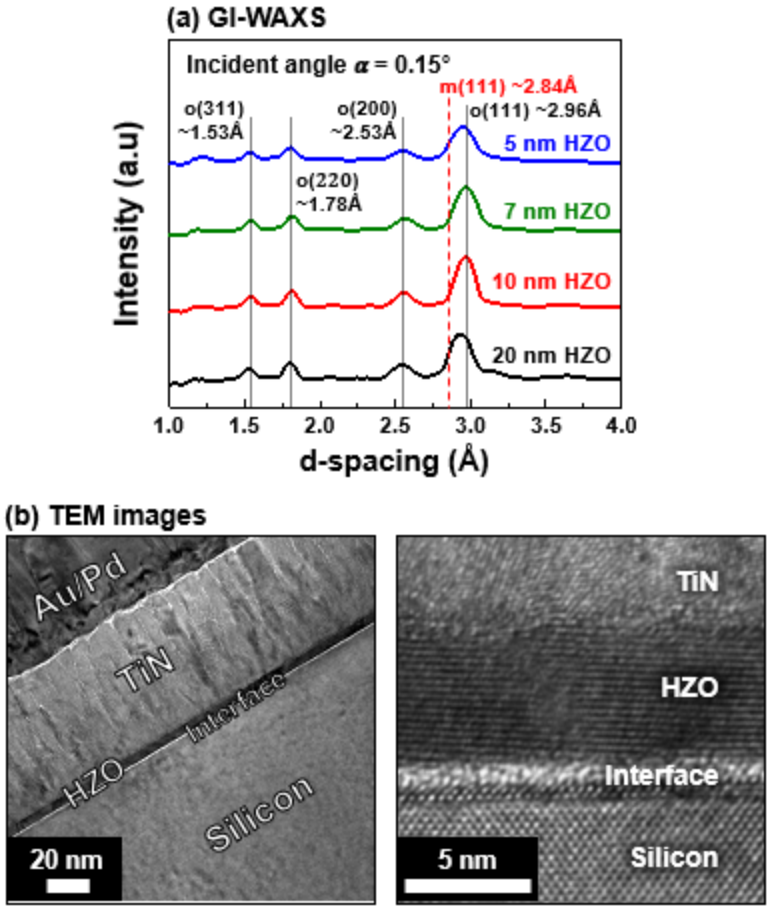

Figure 5.12: (a) GI-WAXS spectra showing the diffraction peaks of HZO films with different thickness using an incidence angle of 0.15°. (b) Low magnification TEM image of 5 nm HZO based MFIS structure and cross-sectional HR-TEM image of 5 nm HZO showing crystalline behavior.

Figure 5.12(b) shows the cross-sectional high-resolution transmission electron microscopy (HR-TEM, JEOL JEM-2100F) images of the 5 nm HZO-based MFIS capacitor that was annealed at 450 °C after TiN TE deposition. Using the electron diffraction patterns obtained by using the fast Fourier transformation (FFT), the interplanar distance (*d*) of the HZO layer was calculated to be 2.96 Å. This spacing is consistent with the d-spacing of O(111) using Bragg's law and is also consistent with the GI-WAXS results. The o-phase polycrystalline grains with

sizes up to 30 nm were observed. The thickness of the interfacial layer obtained from the 5 nm MFIS capacitors was 1 nm, as measured by HR-TEM.

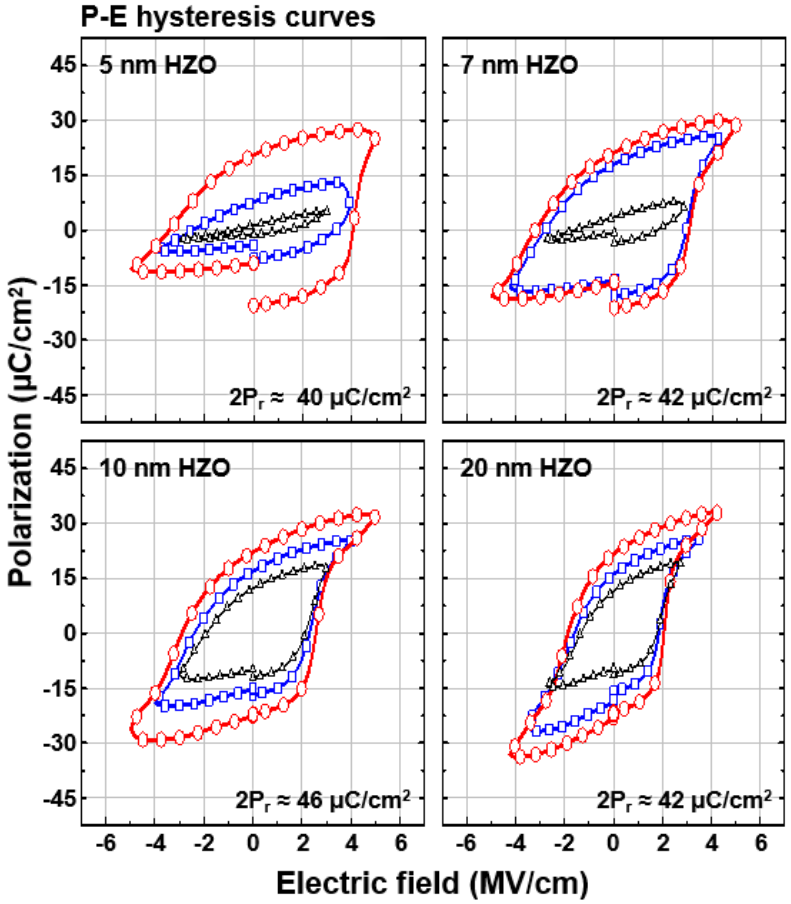

Figure 5.13: P-E hysteresis results showing the FE properties of HZO based MFIS capacitors of various thicknesses (5, 7, 10, and 20 nm) measured at different applied electric fields (red, blue and black curves represent different applied electric fields).

Figure 5.13 shows the polarization-electric field (P-E) hysteresis curves of HZO-based MFIS capacitors measured using a semiconductor parameter analyzer (Keithley 4200-SCS). The P-E hysteresis loops were measured at 25 kHz as this frequency has minimal effects on leakage current and RC delay. The electric fields of MFIS capacitors were calculated using E=V/d, where d is the total thickness of the FE and DE stack, and V is the applied voltage All electrical

measurements were performed on circular device pads with 75 μm diameter. No wake-up type behavior is observed in MFIS capacitors using FE HZO. The 10 nm HZO sample annealed at 450 °C after TiN TE deposition exhibits the largest $+P_r$ of 23 μC/cm^2 without any relaxation. The P_r for 20, 7, and 5 nm HZO were 21, 21 and 20 μC/cm^2 respectively (10% change in $+P_r$). The slightly decreasing P_r with decreasing thickness of HZO is due to the smaller grain size of HZO. This trend is similar in all FE materials and arises as an increase in grain boundaries can hinder the motion of domains[22]. For thickness of 20 nm, the presence of an additional non-FE m-phase reduces the P_r, as confirmed by the GI-WAXS results. This trend is similar to the observations in HZO-based MFM capacitors[14,28]. It can also be seen from Figure. 5.13 that, the P-E hysteresis curves do not form a closed loop. This is possibly due to n-degenerate Si as a bottom electrode[23].The FE coercive field (E_c) for the 20, 10, 7, and 5 nm HZO MFIS capacitors was observed to be 2.0, 2.7, 3.0 and 4.0 MV/cm respectively. This increase in E_c with decrease in FE thickness, can be attributed to the role of the interfacial layer. This indicates that with decreasing FE thickness and for a fixed interface layer thickness, the interface plays a more prominent role in the applied voltage dividing. By simple capacitor-based voltage dividing (using the capacitances of HZO and interface layer), the net electric field to the FE layer, for FE saturation is between 2 to 2.5 MV/cm for all thicknesses of HZO. These values are consistent with the values obtained for MFM capacitors[27]. The breakdown field also increases as HZO is scaled down because of the relatively higher breakdown field for the interfacial layer compared to the HZO layer. The leakage current and breakdown field data are summarized in Figure 5.14.

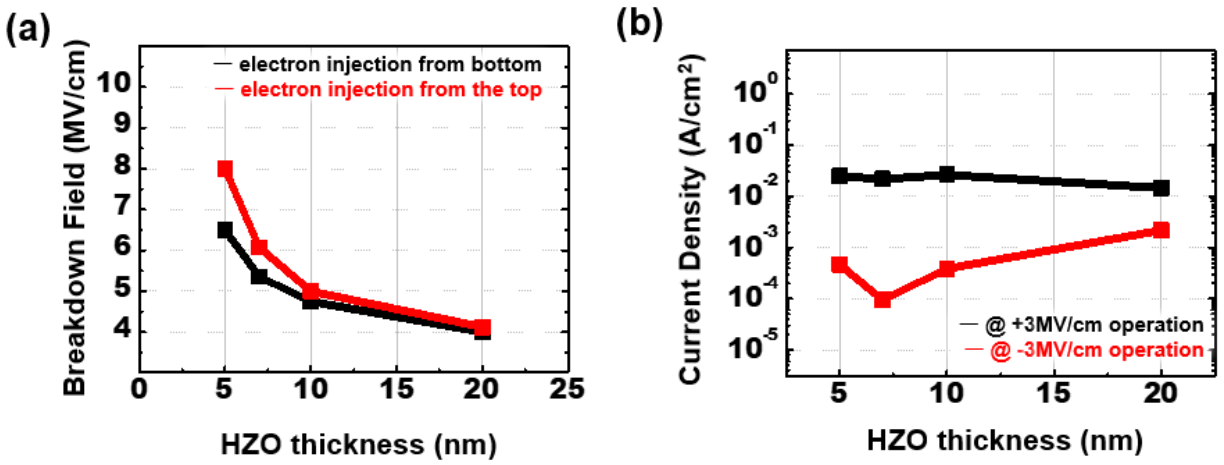

Figure 5.14: (a) Plot of effective breakdown field vs. HZO thickness, and (b) plot of current density at ±3 MV/cm operation for different thickness of HZO.

The trapezoidal WRITE/READ voltage-time pulses were applied to the MFIS capacitors. The pulse details and the measurement setup is similar to our previous studies.[14,27] The pulse timing parameters were chosen such that a fast measurement is used with minimal RC delay effects. The first pulse in a measurement pulse train is used as a conditioning pulse (WRITE) to polarize the FE in one direction at the saturation field of approximately ±5 MV/cm. The second pulse (READ) is applied after 10 μs (i.e., immediate READ) or after 6 s (i.e., delayed READ). The delay time of 10 μs for immediate read was chosen as the shortest limit, as this is long enough circumvent the effects of RC delay and slow domain switching. 6 s was chosen because of programing limitation between subsequent oscilloscope capture windows. It is also expected that this delay time is long enough to observe drastic retention effects, since the delayed READ 10^6 times longer delay time than an immediate READ. By subtracting these integrated current values during switching (P_{sw}) and non-switching (P_{nsw}) pulses, the net FE polarization (P_{FE}) is extracted for different READ voltages.

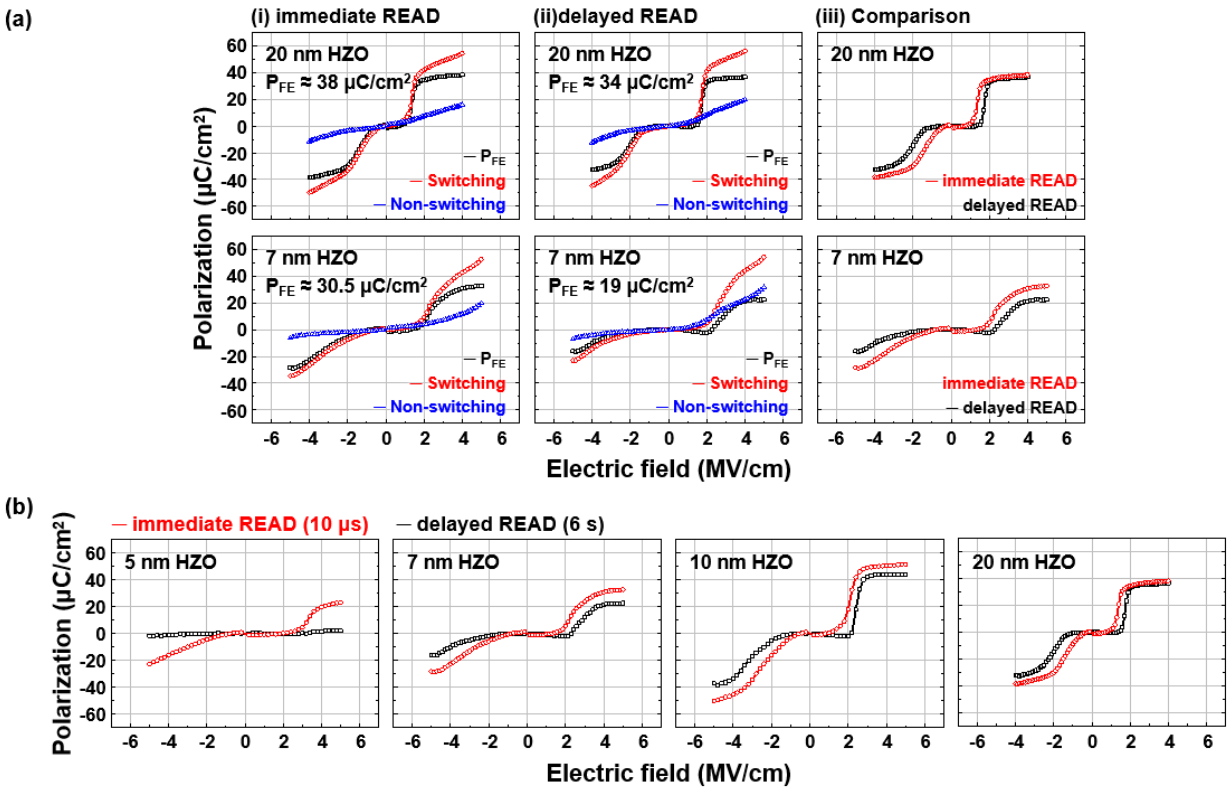

Figure 5.15: (a) Comparison of the FE switching, and non-switching properties measured using WRITE immediate READ and WRITE delayed READ for 20 nm and 7 nm MFIS capacitors. (b) Comparison of the FE polarization (P_{FE}) for HZO based MFIS capacitors of different thickness (5, 7, 10, and 20 nm).

Figure 5.15(a-i) and (a-ii) show the comparison of the individual switching, non-switching, and P_{FE} values for 20 nm HZO and 7 nm HZO MFIS capacitors. There is a decrease in polarization for delayed READ, when compared to immediate READ due to FE polarization loss. In the case of 7 nm HZO, this polarization decrease is more drastic compared to 20 nm HZO as shown in Figure 5.15(a-iii). There is also a distortion in the FE behavior and a shift in E_c (~0.5 MV/cm) when comparing immediate READ and delayed READ. This shift has been observed in MF(I)S capacitors with PZT/Si or HZO/Ge as FE/semiconductor layers[24,29]. From Figure 5.15(b) we find that, with decreasing thickness of the FE layer, there is a much larger

decrease in FE polarization for delayed READ, when compared to immediate READ. Hence, the amount of polarization loss is larger for thinner films (5, 7 nm HZO).

The P_{FE} loss in MFIS capacitors can be attributed to the built-in field generated in the FE layer due to charge continuity between the ferroelectric, and the interface layer. The interface layer here, is defined as the series combination of the interface silicate (SiO_x) and the silicon space charge layer. To estimate the amount of FE built-in field, a simplified series-capacitor model was assumed without considerations for leakage currents and trapped charges as shown in Figure 5.16(a). The potential generated due to the P_{FE} should match the charge of interface layer in contact with the FE.

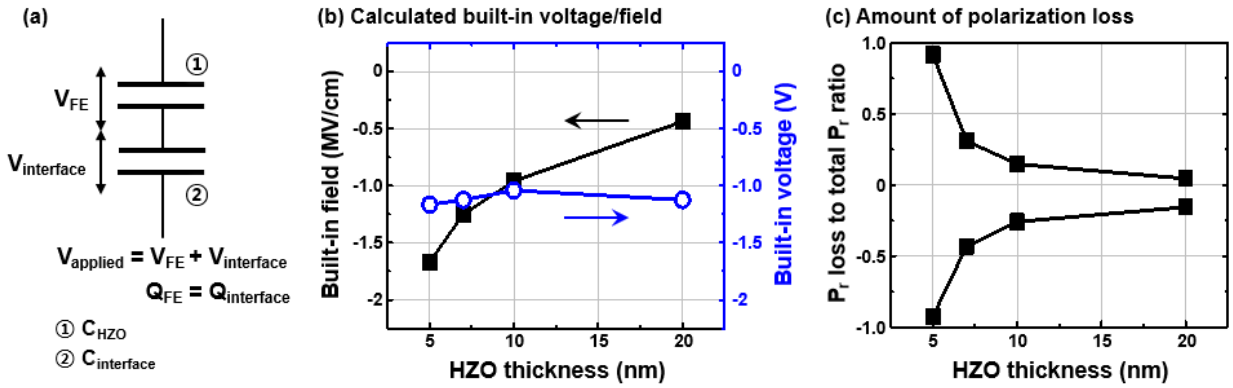

Figure 5.16: (a) Equivalent circuit diagram of the MFIS capacitor structure. (b) Calculated built-in voltage/field in the FE layer based on different HZO thicknesses for the MFIS capacitors. (c) Amount of polarization loss observed as the HZO scales in the MFIS capacitor.

Based on the capacitance of the interface layer and the amount of P_r, the built-in voltage (V_{bi}) at the interface layer and FE layers (at zero applied voltage) can be calculated using,

$$Q_{interface} = C_{interface} V_{interface} = P_r$$

Where, $\frac{1}{C_{interface}} = \frac{1}{C_{SiO_x}} + \frac{1}{C_{SCL}}$. Linear extrapolation of $1/C_{eff}$ versus HZO thickness plot , extracted using the non-switching pulses for different thickness of HZO was used (as shown in Figure 5.17) to extract the capacitance density of the interface ($C_{interface}$ ~ 24 μF/cm^2).

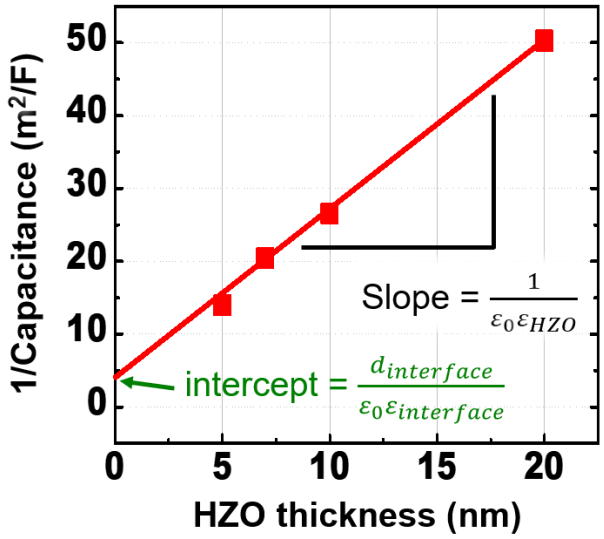

Figure 5.17: Plot of 1/effective capacitance vs. thickness of HZO. The slope can be used to extract the dielectric constant of the HZO layer, and the intercept can be used to extract the dielectric constant of the interface layer.

At ground state without any external applied voltage (V_{appl}),

$$V_{appl} = 0 = V_{FE} + V_{DE}, \qquad -V_{FE} = V_{interface} = V_{bi}$$

Based on this calculation, the built-in field in the FE layer, $E_{FE} = V_{FE}/d_{HZO}$ is calculated as shown in Figure 5.16(b). It can also be seen from Figure 5.16(c) that the amount of polarization loss increases as the FE thickness scales down. It is known that for HZO based MFM capacitors, the FE E_c is constant (~1-1.5 MV/cm) for various thicknesses of HZO[28]. As shown in Figure 5.18, the charge continuity in FE and interface layers creates a V_{bi} and the FE built-in field acts in a direction opposite to P_{FE}. Although the calculated V_{bi} is similar (~0.9 V)

for various thickness of HZO, the built-in field in the FE layer for 5 nm and 7 nm films is near the FE E_c of MFM HZO devices. This high FE built-in field (for example, higher than E_c) leads to accelerated immediate FE polarization loss through the ferroelectric switching process. FE domain switching due to the built-in field happens fast (<10 µs), whereas after longer time (>10 µs) trapping/de-trapping, oxygen vacancy and interface trapped charge responses, due to the built-in field can dominate the P_{FE} retention loss process.[7,24,29] The built-in field also reduces with time through space charge redistribution as shown in Figure 5.18.

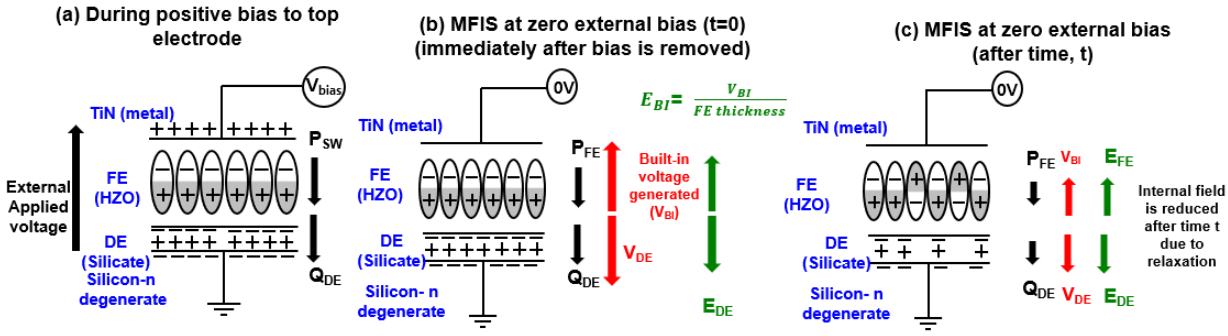

Figure 5.18: Charge distribution and built-in voltage/ built-in field for the MFIS capacitors (a) during bias, (b) immediately after the applied bias is removed (t=0), and (c) time t after the applied bias is removed.

It is also observed that the trend in FE polarization loss was similar in the case of degenerate p-type and n-type substrates. It is noteworthy to mention that the direction of asymmetry is also the same for both cases (pulse measurements on degenerate p- Si substrate). This could lead to the conclusion that the work function difference between asymmetric electrodes, such as TiN (~4.5 eV) and Si (degenerate n-type ~ 4.05 eV and degenerate p-type ~5.15 eV) is not the only contributing factor for the observed asymmetry. Other possible reasons for the generated asymmetry include interfacial polarization caused by interface trapped charge and disproportionate strain originating from the crystallization annealing.[30,31]

In order to understand built-in voltage at the interface of the FE and interface layer, a series connection was made using a 7 nm HZO ferroelectric MFM capacitor and a 5nm HfO_2 MOS capacitor with degenerate Si. The voltage at the interface node between the MFM and the MOS capacitors was monitored using an oscilloscope. The role of this experiment is to show indirect evidence of built-in voltage generated in the MFIS interface due to FE polarization switching between the FE layer and the interface layer using an equivalent circuit of MFM and MOS capacitors in series.

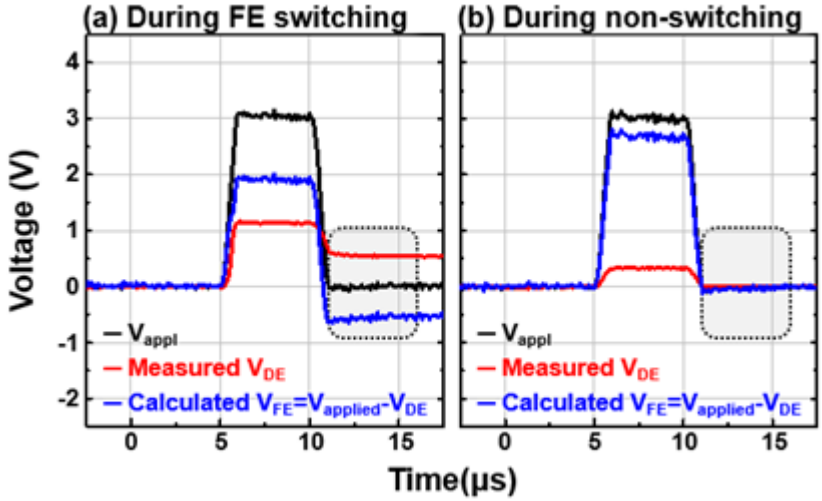

Figure 5.19: Direct measurement of an apparent remnant voltage in the 7 nm MFM + 5 nm HfO_2 MOS capacitor (degenerate n-silicon) series connection using an oscilloscope (a) during ferroelectric switching operation (b) during non-switching operation.

A residual voltage at the node was directly observed at a ground state (0 V_{appl}) after the FE switching process, as shown in Figure 5.19(a). But for non-switching, there is no residual voltage after the applied voltage pulse goes to 0 V. This residual voltage developed in the series connection due to charge continuity can be correlated to the built-in voltage in the MFIS stack. The observation of a residual voltage at 0 V_{appl} has been well-aligned with depolarization field effects discussed by Black et al.[32] Still, further systematic study is required to properly

understand the built-in potential generated between ferroelectric HZO and interface layers, and their impact on ferroelectric device reliability.

5.4 Conclusions

(i) The direct integration of ferroelectric HZO ($Hf_{0.5}Zr_{0.5}O_2$) on silicon, achieving ferroelectric properties on HZO thickness less than 5 nm was studied. By correlating the electrical measurements to high energy synchrotron Grazing Incidence X-ray diffraction (GI-XRD) and high-resolution transmission electron microscope (HR-TEM), the lowest EOT of 0.9 nm was extracted using 5 nm HZO, while confirming the presence of the ferroelectric phase. A direct observation of scavenging of the bottom SiO_x interfacial layer was also observed in 3 nm HZO after the 400 °C annealing process. 4 nm or thinner HZO, however, shows amorphous phase with 400 °C PMA annealing. The effects of re-annealing to higher temperatures on the ferroelectric phase crystallization in HZO thin films was also studied.

(ii) The FE polarization loss of HZO- based MFIS capacitors was investigated with scaling down of FE layers from 20 to 5 nm. 20 nm HZO films show a small change (~5%) in P_{FE} between short (10 μs) and long (6 s) retention time while 5 nm thick films exhibit a large difference (~90%). The dependence of FE polarization loss on FE thickness is attributed to a built-in potential developed in the MFIS stack due to charge continuity between P_{FE} in the FE and the interface charge at ground state without external bias. A direct experimental observation confirmed that a residual voltage is developed at the node between the MFM and MOS capacitors connected in series at a ground state after the ferroelectric switching process. Proper understanding of the built-in field developed at the FE layer in an MFIS stack is crucial to enhance ferroelectric memory retention properties.

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CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusions

In CHAPTER 3, the factors responsible for the crystallization of pure ferroelectric -O phase in HZO thin films was reported. To systematically isolate the role of the crystallization annealing step from the role of the TiN electrode capping layer effect, a room temperature sputtering process for TiN deposition was used in this work (instead of high-temperature TiN deposition processes) and the effects of annealing the HZO films before and after the TiN top electrode deposition was studied. Additionally, the role of oxygen concentration in TiN films on the ferroelectric properties of 10 nm HZO films was studied. The HZO MFM capacitors were then studied to the scalability thickness limit to understand the thin film crystallization process and low voltage operation capability. However, the phase transformation in thin films is limited to the surface to volume energy ratios.

In CHAPTER 4, the reliability properties of the low temperature (400 °C) fabricated MFM capacitors were studied. The trade-off between different reliability issues is studied for the low voltage operation. The mechanisms of failure were elucidated, and it was seen that at 2 V operation at 65 °C, the stability of the devices does not reach the desired 10- year lifetime. Additionally, at 2 V operation, the endurance of the films is expected to be around 10^{11} cycles.

CHAPTER 5 focusses on the scaling of HZO thin films on silicon substrates and reducing the effective EOT of these MFIS capacitors to achieve low voltage operation. Additionally, the effects of interface SiO_x on the ferroelectric reliability and built-in field were studied.

6.2 Future Work

The ALD deposition of HZO films with different metal precursors and oxidants needs to be studied extensively to realize fully crystalline ferroelectric thin films at low temperatures. Additionally, since the -O phase formation is due to a homogeneous nucleation/growth mechanism on top of poly-crystalline TiN electrodes, studies with textured TiN films should be performed to realize ferroelectric HZO films with a preferential growth direction that increases the measured amount of polarization and reduces the operating voltages.

In conventional ferroelectric materials, the reliability issues were solved by using a conductive oxide electrode (RuO_2/IrO_2) to reduce the amount of defects/oxygen vacancies at the interfaces. A similar approach can be used in the case of HZO films, but the crystallization of HZO films requires the presence of the TiN stressor layer. Hence, after phase transformation of the HZO layer in the presence of TiN top electrode, the electrode can be chemically removed (etched) and a conductive oxide electrode replacement can be studied to improve reliability. Band gap and work-function engineering of electrodes is key in realizing this study.

The key to realize reliable ferroelectric polarization for scaled HZO films in silicon is the reduction of interfacial SiO_x layer. The effects of integrating HZO on top of ozonated water treated silicon surface (which leads to the formation of a thinner higher quality chemical oxide) must be studied to realize reliable ferroelectrics for scaled thicknesses on silicon.

BIOGRAPHICAL SKETCH

Jaidah Mohan was born in Doha, Qatar in 1995. He received his bachelor's degree in Materials Science and Engineering from Anna University, Chennai, India in 2016. He then joined the master's program in Materials Science and Engineering at UT Dallas in Fall 2016 and enrolled in the PhD program in Materials Science and Engineering in Spring 2017. He has been working since on ferroelectric $Hf_xZr_{1-x}O_2$ thin films under the supervision of Dr. Jiyoung Kim. He received his master's degree in Materials Science and Engineering from UT Dallas in Spring 2019.

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17. S. J Kim, **Jaidah Mohan**, C. D. Young, S. R. Summerfelt, L. Colombo, J. Kim, T. San, "*Ferroelectric TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN capacitors with low voltage operation and high reliability for next-generation FRAM applications*" IEEE International Memory Workshop (IMW), 1-4 (2018)
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ORAL PRESENTATION:

1. Jaidah Mohan *et. al "Ferroelectricity in low temperature $Hf_{0.5}Zr_{0.5}O_2$ using H_2O_2 as oxidant" presented at annual review meeting, Semiconductor Research Corporation, SRC-LMD, (Poster presentation, Nov 10,2020)*
2. Jaidah Mohan *et. al "Effect of write pulse width on the data retention properties of 10nm $Hf_{0.5}Zr_{0.5}O_2$ MIM capacitors " (Poster Presentation, SISC 2020, San Diego, California)*
3. Jaidah Mohan *et. al "Ferroelectric dipole relaxation with scaling of $Hf_{0.5}Zr_{0.5}O_2$ on silicon" (Poster Presentation, SISC 2019, San Diego, California)*
4. Jaidah Mohan *et. al "Scaling ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ on MFM and MFIS structures" (Conference Presentation, ALD 2019, Bellevue, Washington)*
5. Jaidah Mohan *et. al "Ferroelectricity in Hafnium Zirconate using Tungsten capping Layer" (Conference Presentation, TMS 2019, San Antonio, Texas)*
6. Jaidah Mohan *et. al "Study on the Stress Induced Ferroelectric Polarization of $Hf_{0.5}Zr_{0.5}O_2$ thin films realized at low temperature" (Conference Presentation, TMS 2018, Phoenix, Arizona).*
7. Jaidah Mohan *et. al "A study on the Oxygen Source and Annealing Temperature Effects on Atomic Layer Deposited ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ thin films" (Conference Presentation, ALD 2017, Denver, Colorado).*
8. Jaidah Mohan *et. al "Low Velocity Impact and Axial Loading Response of Hybrid Fiber Metal Laminates" (Conference Presentation, ICMDM'16, Chennai, India)*

AWARDS AND DISTINCTIONS:

1. Dissertation research scholarship, College of Engineering Guindy, Chennai - Rs.25000 for undergraduate research based on written submitted project proposal. 10 applications were selected from a pool of 100. (Jan 2016)