HIGH MOBILITY III-V SEMICONDUCTOR DEVICES WITH GATE DIELECTRICS AND PASSIVATION LAYERS GROWN BY ATOMIC LAYER DEPOSITION

by

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To my family

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by

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HIGH MOBILITY III-V SEMICONDUCTOR DEVICES WITH GATE DIELECTRICS AND PASSIVATION LAYERS GROWN BY ATOMIC LAYER DEPOSITION

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This dissertation focuses on the applications of atomic layer deposition (ALD) to high mobility III-V semiconductor devices. The first study is an in situ ALD-based interface passivation technique using ALD diethylzinc (DEZ) treatment on n-type and p-type $In_{0.53}Ga_{0.47}As$ substrate. The capacitance-voltage (C-V) characteristics of metal-oxide-semiconductor capacitors (MOSCAPs) were studied for a variety of ALD DEZ treatment cycles, different measurement temperatures, and different thickness of ALD-grown high-k gate insulators. The reasons for the presence of inversion-like C-V characteristics shown on n-type substrates are discussed. In addition to ALD DEZ passivation, two alternative ALD-based interface passivation techniques were studied. Furthermore, inversion-type enhancement-mode n-channel and p-channel $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistors (MOSFETs) were demonstrated using in situ ALD DEZ-based interface passivation techniques.

The second part of this dissertation is the fabrication and characterization of AlGaN/GaN MIS-HEMTs. Silicon nitride (SiN_x), grown by low-temperature hollow cathode plasma-enhanced ALD (PEALD), served as a gate dielectric and a surface passivation layer for MIS-HEMTs. Extensive

characterization of the devices was done by high-resolution transmission electron microscopy (HRTEM), current-voltage (I-V) measurement, C-V measurement, gate bias stress measurement, and pulsed I-V measurement. The SiN_x/GaN MIS-HEMTs not only showed a crystalline interfacial layer in the HRTEM images of gate stack, but also demonstrated excellent threshold voltage stability and a mitigated current collapse. Clearly, the effective passivation of surface/interface defects (e.g., nitrogen vacancies and dangling bonds) by the crystalline interfacial layer and the low bulk trap density of PEALD SiN_x are highly beneficial to the reliability of GaN devices.

The last part of this dissertation mainly focuses on the electrical characteristics of AlGaN/GaN heterostructure with ALD-grown epitaxial ZnO cap layer. Theoretically, it was predicted that the piezoelectric polarization of epitaxial ZnO cap layer should have a direction opposite to that in the underlying AlGaN/GaN substrate. As a result, resembling the effect of an InGaN cap layer, a ZnO cap layer may deplete the two-dimensional electron gas (2DEG) near the AlGaN/GaN interface. Experimentally, HRTEM confirmed the epitaxial growth of single-crystalline ZnO cap layer on AlGaN/GaN heterostructure by thermal ALD at 300 °C. The I_{ds}-V_g transfer curve and C-V curve showed a significant positive shift (~1 V) for devices with an O_3-based epitaxial ZnO cap layer, compared to those of Schottky gate devices and devices with a highly conductive H_2O-based epitaxial ZnO cap layer.

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Introduction

The past two decades have witnessed revolutionary progress of the silicon metal-oxide-semiconductor field-effect transistor (Si MOSFET) technology and continuous scaling of device dimension, owing to the introduction of a series of innovative techniques such as strained-silicon, high-k/metal gate, multiple patterning, fin or gate-all-around (GAA) channel structure [1]. Although the efforts to further explore the limit of Si MOSFET technology never cease, researchers have realized the inevitable limitation (e.g., mobility and thermal conductivity) from channel material silicon itself. A high field-effect mobility is extremely critical to obtain high-performance MOSFETs for the applications in high-speed logic circuits. The high-performance and low-power-consumption logic computing will accelerate the development of machine learning, robotics, cloud computing, and internet of things (IoT). Fundamentally, the use of alternative high-mobility channel material in MOSFETs can result in a higher field-effect mobility. This triggered the need to investigate alternative high-mobility channel materials such as the III-V compound semiconductors [2], germanium (Ge), graphene, two-dimensional transition metal dichalcogenides (2D TMDs), and black phosphorus (BP) [3]. Among these novel channel materials, InGaAs has been considered a promising channel material of n-channel MOSFET (NMOS) in sub-7 nm technology node owing to the high electron mobility and appropriate band gap [4].

In addition, there is an ever-increasing demand for devices used in next generation high-frequency and high-power applications, such as radar system, satellite communication, mobile

station, power switch, power amplifier, and power converter. Gallium nitride (GaN) has emerged as the material of choice for the next generation high-performance radio-frequency (RF) device and power devices, competing with the state-of-art devices using conventional semiconductor materials such as the silicon (Si), silicon carbide (SiC), and gallium arsenide (GaAs) [5, 6]. GaN is a wide band gap semiconductor with high critical electric field and high thermal conductivity, which are attractive material properties for power devices. Furthermore, GaN-based high electron mobility transistors (GaN HEMTs) using AlGaN/GaN and InAlN/GaN heterostructures exhibit high electron mobility and electron sheet density owing to the existence of two-dimensional electron gas (2DEG). Over more than 20 years of development, commercial available GaN HEMT products have demonstrated superior performance, including a high power density, high switching speed, high frequency, high working temperature, high breakdown voltage, low power-loss, low noise, and low on-resistance. Therefore, they are very suitable for the next generation high-frequency and high-power applications.

1.2 High Mobility III-V Compound Semiconductor Devices

1.2.1 Overview of InGaAs MOS Devices and Present Issues

The III-V compound semiconductors are referred as a family of semiconductors consisted of the elements in columns III and V of the periodic table, like GaAs, InAs, GaSb, and InP. In addition, ternary and quaternary alloys are attractive owing to the tunable properties. The basic material properties of Si, Ge, and the representative III-V semiconductor materials are tabulated in Table 1.1.

Table 1.1. The material properties of Si, Ge, and the representative III-V semiconductors [7-9].

Properties	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	GaSb	InSb	InP
Band gap	Indirect	Indirect	Direct	Direct	Direct	Direct	Direct	Direct
Structure	DC	DC	ZB	ZB	ZB	ZB	ZB	ZB
χ (eV)	4.05	4.0	4.07	4.5	4.9	4.06	4.38	4.38
E_g (eV)	1.12	0.66	1.42	0.74	0.36	0.73	0.17	1.35
μ_e (cm^2/Vs)	1350	3900	8500	13000	33000	3750	77000	4000
μ_h (cm^2/Vs)	450	1900	400	400	460	680	850	100
$v_{e,sat}$ (10^7cm/s)	1.0	0.7	1.2	3	3.5	-	5.0	0.67
ε_r	11.7	16	13.2	13.9	15.1	15.7	12.5	12.4

DC is diamond cubic, ZB is zinc blende, χ is electron affinity. μ_e is electron mobility, μ_e is hole mobility, $v_{e,sat}$ is electron saturation velocity, and ε_r is relative permittivity (i.e. dielectric constant κ).

Unlike Si and Ge with an indirect band gap and a diamond cubic crystal structure, GaAs and InGaAs are both direct bandgap semiconductor with a zinc blende crystal structure. The adjustable direct band gap of III-V alloys made them a research focus for optical applications such as infrared lasers and photonic detectors. More importantly, the high electron mobility of GaAs and $In_xGa_{1-x}As$ provides them a wider platform in the applications of high-performance NMOS devices. Particularly, a mid-range ternary composition of $In_xGa_{1-x}As$ (x=0.53) can be grown an InP substrate with precise lattice matching to obtain a high-quality single crystal. With higher electron mobility and narrower band gap, $In_{0.53}Ga_{0.47}As$ has surpassed GaAs to be a better candidate for fabricating high-performance n-channel MOSFETs to deliver a high computing speed and a low operation voltage.

Although $In_xGa_{1-x}As$ possesses excellent materials properties, silicon MOSFETs are still playing a dominant role in ultra-large scale integration (ULSI). One important reason for the lag of progress in developing high-performance $In_xGa_{1-x}As$ MOSFETs is the difficulty to obtain high-quality gate dielectric/$In_xGa_{1-x}As$ interface [10]. Unlike silicon with high-quality native oxide, III-V semiconductors and Ge are lacking a high-quality native oxide as the gate dielectric. Attempts to grow non-native oxides such as high-k dielectrics on $In_xGa_{1-x}As$ failed to obtain a high-quality interface due to the formation of a detrimental interfacial layer [11]. The interfacial layer consists a variety of complex electronic defects, including Ga-O bonds, As-O bonds, In-O bonds, elemental As, As-As dimer, vacancies, dangling bonds, and anti-sites. These interface imperfections are believed to cause a high interface trap density (D_{it}), which induces a large frequency dispersion and a failure to effectively modulate the electrostatic potential inside the III-V semiconductors, i.e. Fermi level pinning. Since the Fermi level typically moves between the conduction band edge and valence band edge, a defect state normally originates from an interface state with its energy level located within the band gap. For example, a hump-like feature shown in a capacitance-voltage (C-V) curve usually corresponds to the response of mid-gap interface traps of III-V semiconductors. The frequency dispersion of accumulation capacitance usually corresponds to the interface/border traps near the conduction band edge of the III-V semiconductors.

To remove the defective interfacial layer and passivate the III-V semiconductor surface without further oxidation during growing the gate dielectrics, many ex situ or in situ cleaning and passivation techniques have been investigated. Ex situ wet cleaning with solutions such as buffered oxide etch (BOE), hydrochloric acid (HCl), hydrofluoric acid (HF), ammonium hydroxide (NH_4OH), and ammonium sulfide $(NH_4)_2S$ are widely used to remove the surface oxides and

passivate the surface [12, 13]. However, the surface can be immediately re-oxidized upon exposure to oxygen and moisture in the ambient air.

This problem was effectively addressed by growing thin interfacial passivation layer (IPL) or Si precursor treatment including amorphous Si [14], Ge [15], SiH_4 treatment [16], Si_2H_6 treatment [17], SiH_4/NH_3 treatment [18], AlN IPL[19], AlON IPL [20], and ZnO IPL [21]. By depositing a thin IPL (0.5−1.5 nm) to passivate the surface, the oxidation of III-V semiconductor surface was greatly suppressed and D_{it} was noticeably reduced. For example, the Si or Ge IPL allows oxygen gettering from the III-V semiconductor surface and reduces the high oxidization states of III-V semiconductor. However, it is difficult to precisely control the uniform coverage of thin IPL on the surface. Also, the formation of low dielectric constant (κ) interfacial silicon oxide or germanium oxide forbids the continuous scaling of effective oxide thickness (EOT).

As the device fabrication approaches atomic-scale dimensions, interface passivation at atomic-scale dimensions are preferred. To prepare only a few angstroms (Å) of the interfacial layer, atomic layer deposition (ALD) is a very promising technique to meet this requirement [22]. In addition, ALD is also considered a suitable method to grow highly uniform gate dielectrics with atomic scale precision. The detailed description about ALD will be presented in section 1.3.

1.2.2 Overview of AlGaN/GaN HEMTs and Present Issues

AlN, GaN, and InN belong to III-V semiconductors, and they are usually referred as III-nitride (III-N) semiconductors [23]. Simply by replacing As atom with N atom, the materials properties of III-N semiconductors totally differ from those of their counterparts

(AlAs/GaAs/InAs). The basic material properties of Si, Ge, and the representative III-N semiconductors are tabulated in Table 1.2.

Table 1.2. The material properties of Si, Ge, and the representative III-N semiconductors [7-9].

Properties	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	AlN	GaN	InN
Band gap	Indirect	Indirect	Direct	Direct	Direct	Direct	Direct
Structure	DC	DC	ZB	ZB	WZ	WZ	WZ
χ (eV)	4.05	4.0	4.07	4.5	0.6	4.1	5.8
E_g (eV)	1.12	0.66	1.42	0.74	6.2	3.4	0.7
μ_e (cm^2/Vs)	1350	3900	8500	13000	1100	400 (bulk) 1500 (2DEG)	3600
μ_h (cm^2/Vs)	450	1900	400	400	14	10	30
$v_{e,sat}$ (10^7 cm/s)	1.0	0.7	1.2	3	1.5	1.5-2	1.0
ε_r	11.7	16	13.2	13.9	8.5	8.9	15.3

DC is diamond cubic, ZB is zinc blende, WZ is wurtzite, χ is electron affinity. μ_e is electron mobility, μ_e is hole mobility, $v_{e,sat}$ is electron saturation velocity, and ε_r is relative permittivity (i.e. dielectric constant κ).

Although the III-N semiconductors can exist in both the zinc blende and wurtzite crystal structure, the wurtzite form with noncentrosymmetric (lacking inversion symmetry) crystal structure along the [0001] c-axis has been mainly investigated. There is a strong spontaneous polarization (P_{SP}) present in the wurtzite crystal structure owing to the cation-anion (metal-nitrogen) dipole moment. The direction (polarity) of P_{SP} depends on the crystal orientation relative to the substrate. As shown in Figure 1.1, there are two types of polarity in the wurtzite GaN crystal structure: Ga-face and N-face polarity [24]. The direction of P_{SP} is parallel to the [0001]

orientation: pointing towards (down direction) the substrate for the Ga-face crystal whereas pointing opposite to (up direction) the substrate for the N-face crystal.

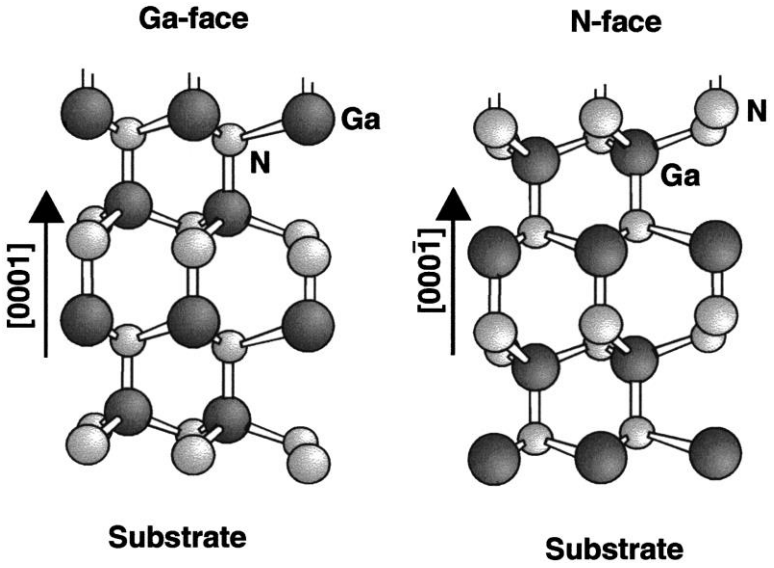


Figure 1.1. Schematic diagram of the crystal structure of wurtzite GaN with Ga-face and N-face polarity [24]. Reprinted from Ambacher et al., Journal of Applied Physics 85, 3222 (1999), with the permission of AIP Publishing.

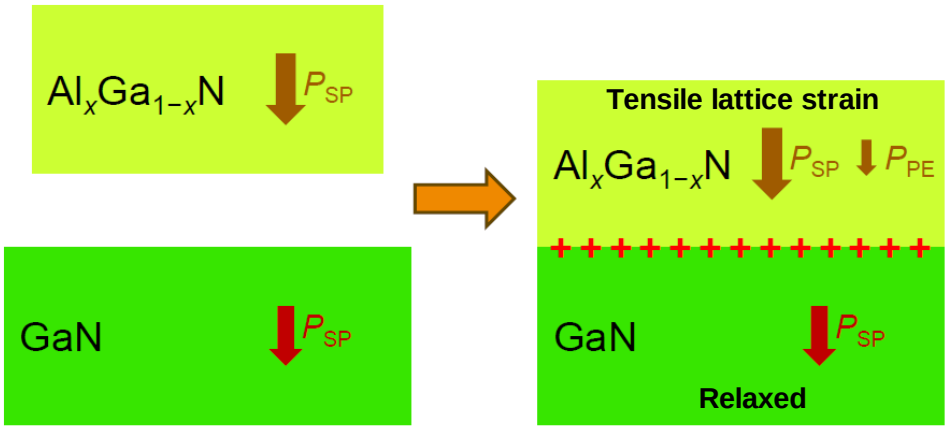


Figure 1.2. Schematic diagram of the spontaneous polarization and piezoelectric polarization existing in an $Al_xGa_{1-x}N$/GaN heterostructure, Ga-face polarity is assumed [25]. Adapted from ESSDERC 2013 tutorial, "High Voltage GaN HEMT devices and modelling" by Dr. Stephen Sque.

When lattice strain is present due to the lattice mismatch, a piezoelectric polarization (P_{PE}) will be induced in wurtzite III-N semiconductors. The direction of P_{PE} not only depends on the crystal orientation (Ga-face or N-face), but also depends on the nature of the strain (compressive or tensile). One important application of the inherent polarization behavior is to form the heterostructures such as $Al_xGa_{1-x}N/GaN$ and $In_xAl_{1-x}N/GaN$. As shown in Figure 1.2, in the case of an $Al_xGa_{1-x}N/GaN$ heterostructure (Ga-face polarity is assumed), the direction of spontaneous polarization (P_{SP}) is pointing to the substrate. When an $Al_xGa_{1-x}N$ layer is epitaxially grown on a GaN substrate, due to the presence of a tensile lattice strain (lattice constant: AlN < GaN), there is additional piezoelectric polarization induced in the $Al_xGa_{1-x}N$ layer with the same direction. In the case of the GaN substrate, the lattice is relaxed (strain-free) and the piezoelectric polarization does not exist.

As illustrated in Figure 1.3, the strong polarization induces the band bending, and the Fermi level moves above the conduction band edge of GaN at the heterointerface. Electrons will populate near the interface and form two-dimensional electron gas (2DEG). The 2DEG can be confined by the energy barrier near the $Al_xGa_{1-x}N/GaN$ interface due to presence of the conduction band offset between $Al_xGa_{1-x}N$ and GaN. Interestingly, the lattice-matched $In_xAl_{1-x}N/GaN$ heterostructures are currently investigated as the alternatives to the conventional $Al_xGa_{1-x}N/GaN$ heterostructures [26]. There is a larger spontaneous polarization while no strain-induced piezoelectric polarization present in an $In_xAl_{1-x}N/GaN$ heterostructure. The mobility degradation related to lattice strain is expected to be effectively suppressed.

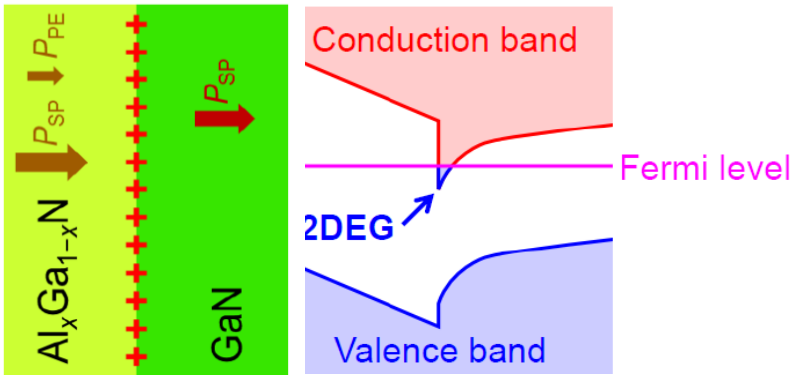


Figure 1.3. Schematic diagram of the spontaneous polarization and piezoelectric polarization existing in an $Al_xGa_{1-x}N$/GaN heterostructure and the corresponding energy band diagram [25]. Adapted from ESSDERC 2013 tutorial, "High Voltage GaN HEMT devices and modelling" by Dr. Stephen Sque.

Without any intentional doping, the $Al_xGa_{1-x}N$/GaN channel (2DEG) shows high sheet carrier density (~10^{13} cm^{-2}), high electron mobility (~1500 cm^2/Vs), and high electron saturation velocity (~2.5×10^7 cm/s vs. 1.0×10^7 cm/s for Si), which are attributed to the effective suppression of mobility degradation by surface roughness scattering and impurity scattering. These exceptional electron transport characteristics make way for the development of high electron mobility transistors (HEMTs) operated at high frequencies. In addition, the excellent chemical/thermal stability, the high critical electric field (E_c~3 MV/cm vs. 0.3 MV/cm for Si), and the wide band gap (3.4 eV vs. 1.12 eV for Si) allow GaN HEMTs to operate at high-temperature (>250 °C) and high-voltage conditions (>600 V). Regarding the limitation from the lateral device structure, the vertical GaN power devices have been investigated for a higher voltage conditions (>1000 V) [27].

Three mainstream substrates for AlGaN/GaN HEMTs are sapphire (Al_2O_3), SiC, and silicon (111). Al_2O_3 substrate is inexpensive, but it suffers from poor epitaxy quality (a large dislocation density due to a large lattice mismatch with GaN) and poor thermal conductivity. SiC

substrate provides a high epitaxy quality and a high thermal conductivity, but the manufacturing cost is very high. GaN HEMTs on SiC are targeted at the performance-oriented applications. Compared to the Al_2O_3 and the SiC substrate, the Si substrate can offer a larger wafer size (cost-effective) and is compatible with the mainstream CMOS production lines in the semiconductor fabs. Therefore, the industrial community has devoted tremendous efforts to developing CMOS-compatible technology (e.g., gold-free ohmic contact, Ga contamination prevention) to fabricate GaN HEMTs on Si substrate [28].

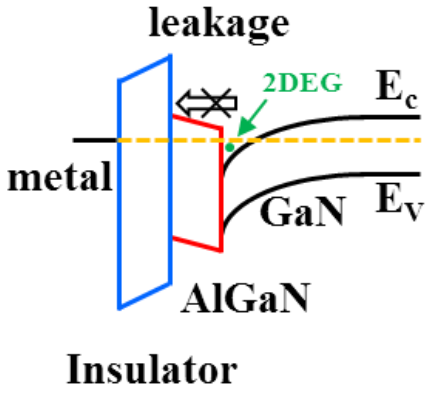


Figure 1.4. Schematic band diagram of a GaN MIS-HEMT structure using a gate insulator to reduce the gate leakage current.

In addition, a low gate leakage current is extremely important for power device application. The use of a metal-insulator-semiconductor (MIS) structure can reduce the gate leakage current of GaN HEMTs [29], as shown in Figure 1.4. Early attempts to grow gate dielectrics focused on using conventional deposition methods including plasma-enhanced vapor deposition (PECVD), thermal CVD, and physical vapor deposition (PVD). However, these methods suffered from poor film quality, non-uniform thickness, high thermal budget, or ion bombardment damage. Inspired by the

pioneering work using ALD Al_2O_3 as a gate dielectric on GaN HEMTs by Ye et al. [30], as well as encouraged by the successful integration of ALD high-k dielectrics into the Si CMOS platform for mass production, the GaN community has considered ALD a highly attractive method to grow high-quality gate dielectrics for AlGaN/GaN MIS-HEMTs. The past decade witnessed a boost of research efforts and an unprecedented improvement of device performance. However, people have realized that there are still many issues and challenges to address to obtain high performance and high reliability.

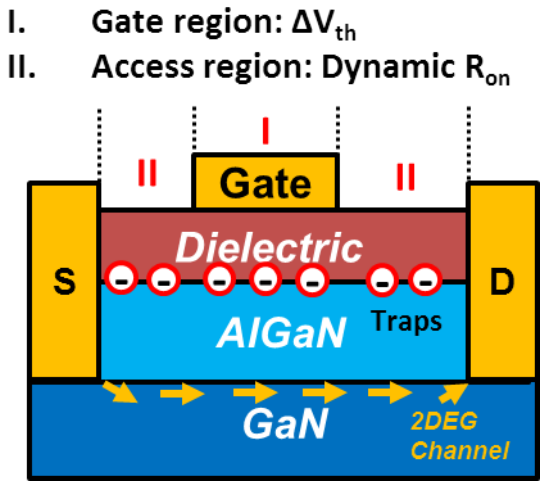


Figure 1.5. Schematic diagram of a GaN MIS-HEMT structure with the presence of traps near the dielectric/III-N interface on either (I) gate region or (II) access region.

Figure 1.5 shows a schematic diagram of a MIS-HEMT structure with the presence of traps near the dielectric/III-N interface on either gate region or access region. These traps may capture and emit electrons dynamically during the device operation. The trapping/detrapping of interface traps and border traps near the dielectric/III-N interface may induce several reliability issues [31]. One of the issues is the threshold voltage instability [32, 33]. The V_{th} instability is typically referred

as the V_{th} hysteresis and V_{th} drift under a forward or large reverse gate bias, which is because of the interface/border traps under the gate region. The traps with captured electrons act as fixed charge (usually negative charge for acceptor-like traps) and induced the change of V_{th}. Temperature also directly impact the V_{th} instability since it can change the emission time constant of traps.

On the other hand, electrons captured by the traps can induce another problem called dynamic on-resistance (R_{on}) or current collapse. Specifically, the interface/border traps and the buffer layer traps from gate-to-drain region have more influence since a high electric field exists in this region. Electrons can be injected from the gate or the substrate, and then captured by the traps. During fast switching operation, the captured electrons may not be immediately emitted. As a result, the filled trap acts as a negatively charged virtual gate, which screens (or depletes) the electrons in the 2DEG channel and causes a temporarily reduced drain current [34]. As a symptom of current collapse, the R_{on} extracted from pulsed I-V output curves increases with the increasing of quiescent drain voltage.

Figure 1.6 shows a representative C-V curve of a GaN MIS-capacitor. There are two major interfaces in a typical MIS-capacitor structure: the barrier/GaN interface and the dielectric/III-N barrier interface. First, the forward gate bias modulates the Fermi level to move above the conduction band edge of GaN. Electrons accumulate at the barrier/GaN interface to form the 2DEG channel. There will be no interaction between 2DEG and the traps near the dielectric/ III-N barrier interface because of the physical separation by the barrier. At this moment, the first slope appears in the C-V characteristics. The saturated capacitance is a total capacitance of the dielectric capacitance (C_{ox}) and the barrier capacitance ($C_{barrier}$) in series connection. The value is smaller

than that of Schottky gate structure with only the barrier capacitance ($C_{barrier}$). If the forward gate bias is large enough to allow the electrons to spill over the barrier, the electrons will populate at the dielectric/III-N barrier interface. The second slope with higher capacitance (~C_{ox}) appears in the C-V characteristics at a larger forward gate bias. At this moment, electrons can communicate with the traps near the dielectric/III-N barrier interface via trapping/detrapping process [29].

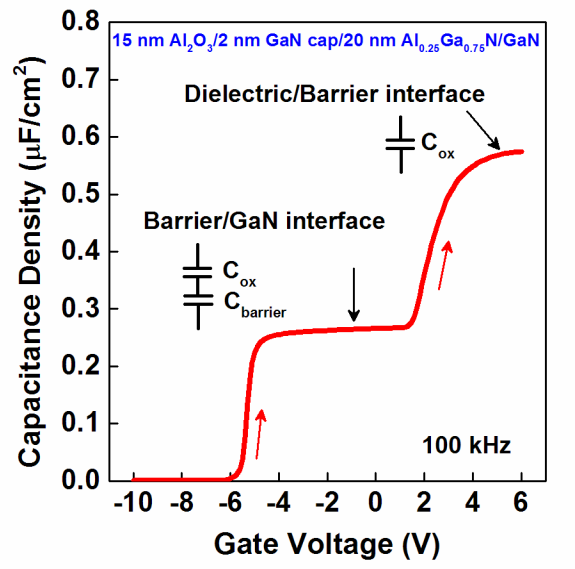


Figure 1.6. Representative C-V curve of a GaN MIS-capacitor measured at 100 kHz with Ni/Au gate electrode.

As reported in the literature, the materials utilized for the gate insulator of GaN MIS-HEMTs includes Al_2O_3 [30, 35], ZrO_2 [36, 37], HfO_2 [38], SiO_2 [39], SiON [40], SiN_x [41, 42], Sc_2O_3 [43], MgCaO [44, 45]. In addition, various dielectric/III-nitrides interface passivation techniques have been proposed, such as plasma nitridation [46, 47], ultra-thin AlN [48, 49], SiN_x [50], or crystalline oxide interlayer [51, 52]. Among the gate insulator candidates, silicon nitride (SiN_x) has a band gap of 5.3 eV and has a type II staggered band alignment with GaN (E_g=3.4 eV) and $Al_{0.3}Ga_{0.7}N$ (E_g=4.2 eV) [53]. The large conduction band offsets (2.0 eV with GaN and 2.3 eV

with $Al_{0.3}Ga_{0.7}N$, respectively) allow low gate leakage current under a forward gate bias. Furthermore, SiN_x can form a good interface with III-nitrides by passivating the nitrogen vacancies, Ga dangling bonds and suppressing the Ga−O bonds formation [42]. In addition, SiN_x is a mature dielectric material that has high breakdown field and is being widely used in Si-CMOS industry. Therefore, SiN_x gate insulator has attracted great research interests.

For example, Moens et al. have demonstrated CMOS-compatible 650 V rated depletion mode (D-mode) AlGaN/GaN MIS-HEMTs on Si using in situ metalorganic chemical vapor deposited (MOCVD) SiN_x as a gate dielectric and passivation layer on the access region [54]. The devices showed a good V_{th} stability (ΔV_{th}<400 mV) at a high working temperature of 200 ℃, as well as low dynamic R_{on} (<20%, V_{DS}=600 V) by using gate/source field plate structures and PECVD SiN_x/polyimide passivation layers. However, in situ MOCVD SiN_x cannot be utilized as a gate insulator of gate-recessed MIS-HEMTs. Hua et al. have realized high-performance and reliable enhance-mode (E-mode) GaN MIS-FETs by adopting ex situ 2-nm-thick low-temperature (300 °C) PECVD SiN_x interfacial layer and 15-nm-thick high-temperature (780 °C) low pressure chemical vapor deposited (LPCVD) SiN_x as the gate insulator stack [50]. The thin PECVD-SiN_x interfacial layer protected the etched GaN surface from Ga and N atoms out-diffusion, as well as oxidation, during the initial stage of high-temperature LPCVD process. The subsequent LPCVD-SiN_x layer ensured the high bulk quality of the gate insulator stack owing to the high process temperature. However, either in situ MOCVD approach (>1000 °C) or ex situ LPCVD (> 700 °C) approach raises the thermal budget of device fabrication. High temperature causes unwanted high thermal stress due to the difference in thermal expansion coefficient of epitaxial layers and the underlying substrate. Furthermore, high temperature is not compatible with ohmic-first process

flow, as well as indium nitride (InN)-based MIS-HEMTs fabrication due to the InN decomposition ($T_{decomposition}$>630 °C) [55].

For low-temperature SiN_x process, plasma-enhanced atomic layer deposition (PEALD) is considered the choice of method due to the ability to grow conformal film with high quality [56, 57]. In addition, the repetitive nitrogen-containing plasma exposure during the initial stage of SiN_x growth can improve the device performance by generating nitrogen-passivated insulator/III-nitride interface. The few early attempts implemented inductively coupled (ICP) PEALD SiN_x gate insulators on gate-recessed structures [58-60]. Though improved V_{th} stability was demonstrated under small gate bias stress conditions (<3 V), the performance degraded when larger stress gate bias (e.g., 7 V) was applied. On one hand, this could be related to the surface damage from the recess etch. On the other hand, indicated by a low refractive index of 1.85−1.87, the quality of low-temperature PEALD SiN_x grown by SiH_4 and N_2 plasma in these studies was inferior to that of SiN_x grown by high-temperature process. This may be ascribed to the hydrogen impurity from the SiH_4 molecule and oxygen impurity from the ceramic tube of the ICP plasma source [61]. Furthermore, the efficacy of using PEALD SiN_x passivation layer on access regions to suppress current collapse behavior was not reported.

Except the V_{th} instability and dynamic R_{on} discussed above, another problem people have been working on is normally-on operation (depletion mode or D-mode), i.e. negative threshold voltage. This is ascribed to the strong polarizations naturally existing in the AlGaN/GaN heterostructure without any externally applied electric field. However, the fail-safe system design requires normally-off devices. Equivalent normally-off operation (Enhance-mode or E-mode) can be achieved by a cascode configuration with a low-voltage normally-off Si MOSFET and a high-

voltage normally-on AlGaN/GaN HEMTs. However, this approach requires additional power supply and more complex circuit.

A direct way to obtain normally-off operation is by canceling out the strong polarization (deplete the 2DEG) of heterostructure under the gate region. 2DEG channel will not form until a positive gate voltage exceeding the V_{th} is applied. The methods include (1) MIS-FETs structure with fully recessed barrier at the gate region, (2) charge engineering technique by introducing negative charges via fluorine plasma treatment or using ferroelectric-based gate stack with a charge trapping layer, and (3) polarization engineering by adopting a new epitaxial structure (e.g., p-GaN cap, p-AlGaN cap, InGaN cap, and piezo-neutralization layer) with modified polarization fields inside the III-N heterostructure [62]. For the third method, the polarization fields are intentionally modified to lift the energy band diagram at the III-N heterointerface, where 2DEG channel will be formed. When the gate voltage is zero, the conduction band edge near the heterointerface locates at a higher potential energy above the Fermi level and 2DEG does not exist. When a positive gate voltage is applied, the Fermi level raises above the conduction band edge and 2DEG forms.

For example, introducing an i-InGaN or p-InGaN cap layer can realize normally-off operation [63-67]. Due to the presence of a compressive lattice strain in the InGaN cap layer, the direction of piezoelectric polarization in the InGaN cap layer is opposite to that in the underlying AlGaN/GaN substrate. Although a spontaneous polarization also exists in the InGaN cap layer, its value is smaller than that of the strain-induced piezoelectric polarization. Therefore, the piezoelectric polarization is dominant. As shown in Figure 1.7, with an i-InGaN or p-InGaN capping layer, the conduction band near the 2DEG channel raises above the Fermi level and 2DEG is depleted.

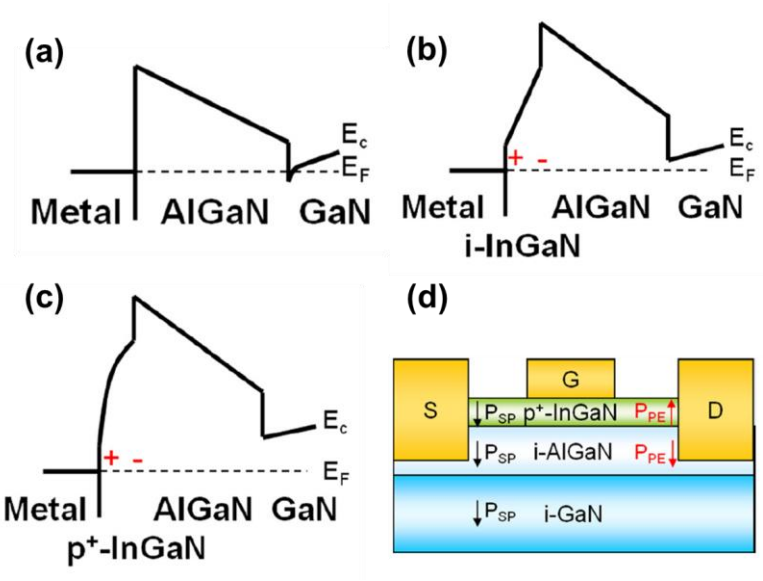


Figure 1.7. Schematic of the energy band-diagram in a Schottky gate AlGaN/GaN structure (a) without cap layer, (b) with an i-InGaN cap layer, (c) with a p-InGaN cap layer, and (d) schematic of a Schottky gate HEMT structure with a p-InGaN cap layer and the polarization direction inside [67]. Reprinted from Mizutani et al., Journal of Applied Physics 113, 034502 (2013), with the permission of AIP Publishing.

Zinx oxide (ZnO) is a group II-VI wide band gap semiconductor material. Its material properties together with those of III-N semiconductors are summarized in Table 1.3. Wurtzite structure ZnO has a band gap of 3.37 eV (vs. GaN 3.4 eV) and a small lattice mismatch with GaN (~1.9%). In addition, ZnO shows great similarity to the III-N semiconductors in terms of the existence of strong spontaneous polarization and piezoelectric polarization. The piezoelectric polarization along the c-axis can be determined by the Equation 1.1. a and a_0 is lattice constant of GaN and the strained layer in equilibrium, respectively.

$$P_{PE} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{c_{13}}{c_{33}}\right) \qquad \text{Equation 1.1.}$$

Table 1.3. Basic material properties of ZnO and the representative III-N semiconductors [68, 69].

Properties	ZnO	GaN	AlN	InN	$Al_{0.25}Ga_{0.75}N$	$In_{0.2}Ga_{0.8}N$
Lattice structure	WZ	WZ	WZ	WZ	WZ	WZ
Band gap (eV)	3.37	3.4	6.2	0.7	4.1	2.86
Electron affinity (eV)	4.35	4.1	0.6	5.8	3.23	4.44
Dielectric constant	8.5	8.5	8.9	15.3	8.6	9.9
a (Å)	3.25	3.189	3.112	3.545	3.17	3.278
c (Å)	5.204	5.182	4.982	5.703	5.132	5.312
Spontaneous polarization (c/m^2)	-0.057	-0.029	-0.081	-0.032	-0.042	-0.030
Elastic constant, c13	105.1	103	108	92	104	100.8
Elastic constant, c33	210.9	405	373	224	397	368.8
Piezoelectric constant, e31	-0.51	-0.49	-0.6	-0.57	-0.52	-0.506
Piezoelectric constant, e33	0.89	0.73	0.91	1.46	0.91	0.778

The ternary material properties are determined by Vegard's law. WZ is wurtzite.

Theoretically, as shown in Figure 1.8, that the piezoelectric polarization of epitaxial ZnO cap layer should have a direction opposite to that in the underlying AlGaN/GaN substrate. As a result, resembling the effect of an InGaN cap layer, a ZnO cap layer may deplete the two-dimensional electron gas (2DEG) near the AlGaN/GaN interface. Simulation results obtained by Dr. Jae-Gil Lee in our group also support this hypothesis. As show in Figure 1.9, the n-type ZnO cap layer can shift the V_{th} positively to realize normally-off operation and p-type ZnO cap layer can make the device have a larger positive V_{th}.

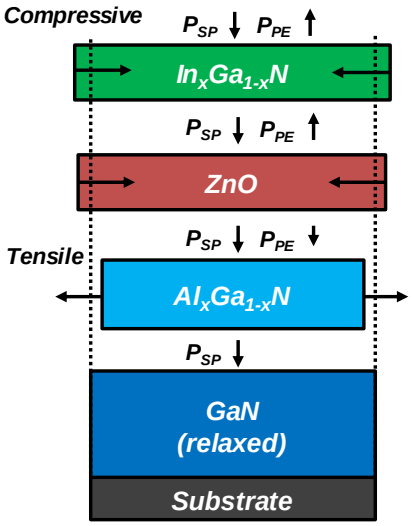


Figure 1.8. Schematic of spontaneous polarization (P_{SP}) and piezoelectric polarization (P_{PE}) present in epitaxial $Al_xGa_{1-x}N$, ZnO, and $In_xGa_{1-x}N$ on GaN.

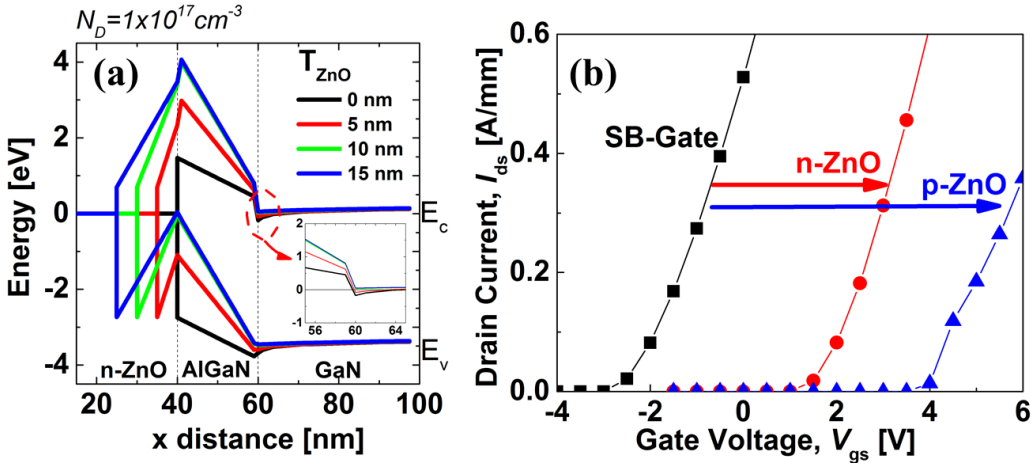


Figure 1.9. (a) Schematic of $Al_{0.25}Ga_{0.75}N$/GaN band diagram without (0 nm) and with (5 nm, 10 nm, and 15 nm) n-type ZnO cap layer, (b) V_{gs}-I_{ds} transfer curves of HEMTs without (Schottky gate) and with 15 nm n-type or p-type ZnO cap layer. The results were simulated by Dr. Jae-Gil Lee using Silvaco Atlas.

It has been reported that it is feasible to grow epitaxial oxides by ALD or so-called atomic layer epitaxy (ALE), such as La_2O_3 and $La_{2-x}Y_xO_3$ on GaAs (111), $Mg_xCa_{1-x}O$ on GaN,

$Mg_{0.25}Ca_{0.75}O$ on AlGaN/GaN or InAlGaN/GaN MIS-HEMTs [26, 44, 70-72]. These epitaxial oxide gate dielectrics improved the MOS interface quality due to the effective reduction of interfacial dangling bonds and other defects related to the lattice strain. Not surprisingly, ZnO epitaxially grown on GaN at a temperature of ~300 °C by thermal ALD (diethylzinc/H_2O) has also been demonstrated. However, the effect of ALD epitaxial grown ZnO cap layer on the electrical characteristics of AlGaN/GaN heterostructure has not been investigated. There were a few reports regarding growing ZnO on GaN HEMTs using physical deposition methods such as vapor cooling condensation [73-75], e-beam evaporation [76], and pulsed laser deposition (PLD) [77]. However, epitaxial growth of crystalline ZnO layer was not demonstrated in these studies. More importantly, the polarization effect of ZnO on AlGaN/GaN heterostructure was not considered by the authors.

1.3 Atomic Layer Deposition

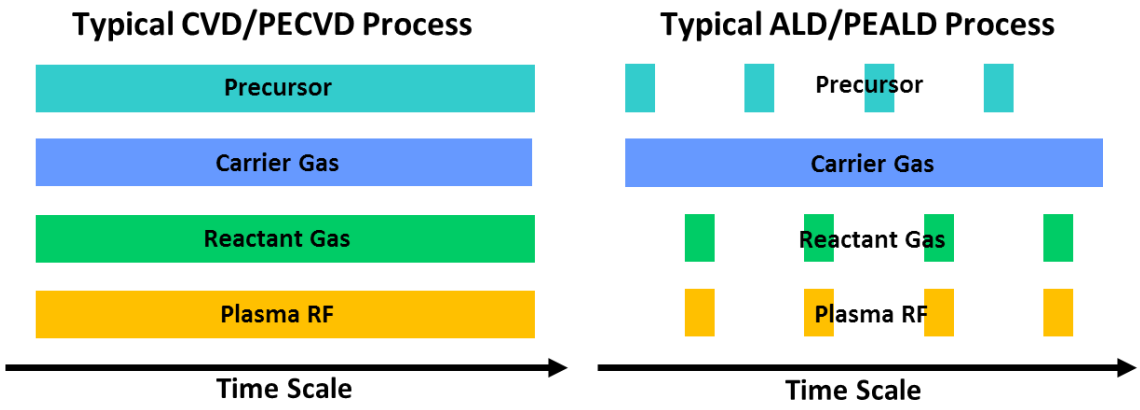


Figure 1.10. Schematic of the typical CVD/PECVD process and typical ALD/PEALD process.

Atomic layer deposition (ALD), based on the self-limiting surface chemical reactions using subsequent exposure of the gas phase reactants, is an extremely attractive thin film deposition

technique. Unlike CVD which has precursor and reactant gas reacted at the same time, ALD is a cycling deposition method with separated reactant exposure steps. As shown in Figure 1.10, each ALD cycle typically consists characteristic four process steps: (1) precursor exposure, (2) purge, (3) reactant or plasma exposure, and (4) purge.

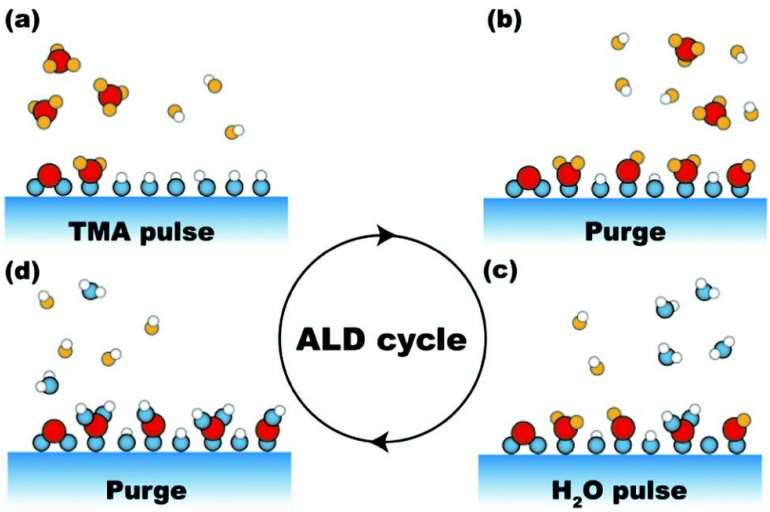


Figure 1.11. Schematic diagram of typical surface reactions of one cycle Al_2O_3 ALD process using TMA and H_2O [78]. Reproduced from H. Van Bui et al., Chem. Commun., 2017, 53, 45 with permission of The Royal Society of Chemistry.

The surface reactions of ALD can be illustrated with the classic Al_2O_3 ALD process using trimethylaluminum (TMA, $Al(CH_3)_3$) and H_2O [78]. As shown in Figure 1.11, the incoming surface is terminated with −OH groups, the first step of Al_2O_3 ALD cycle is precursor TMA pulse and one or two $-CH_3$ ligands of TMA molecules reacted with the surface −OH groups in a self-limiting fashion, releasing gas-phase CH_4 molecules as the reaction byproducts. Then, the nonreacted TMA and reaction byproducts (e.g., CH_4) are purged by inert gas (nitrogen or argon). The third step is H_2O pulse and the remaining $-CH_3$ ligands are cleaved, leaving −OH groups

terminated on the surface. Again, the nonreacted H_2O and reaction byproducts (e.g., CH_4) are purged by inert gas (nitrogen or argon). A more detailed introduction to ALD can be found in many existing review papers [22, 57, 79].

The nature of ALD allows the precise manipulation of surface reaction by simply changing the exposure of precursor and reactant. Furthermore, precise thickness control can be realized by simply tuning the cycle numbers when depositing in a saturated ALD reaction regime. These features are extremely desired when the dimensions of transistors in integrated circuits continue to scale down. In addition, the outstanding features of ALD have been further extended by using plasma to enhance the reactivity of reactants. Plasma-enhanced ALD (PEALD) can allow a lower deposition temperature, a higher growth per cycle (GPC) while obtaining an improved film quality [57]. Furthermore, in situ plasma pre-deposition treatment or post-deposition treatment can be combined with ALD film growth.

1.3.1 ALD of Silicon Nitride (SiN_x)

Silicon nitride (SiN_x) is one of the most extensively used silicon-based thin film materials. Several deposition techniques including plasma-enhanced chemical vapor deposition (PECVD), low-pressure chemical vapor deposition (LPCVD), hot-filament chemical vapor deposition (HF-CVD), and atomic layer deposition (ALD) have been employed for SiN_x growth. Particularly, ALD has been considered a suitable technique to grow conformal SiN_x films with atomic-scale precision of thickness control. During my PhD research, I have studied SiN_x thin film growth for more than 3 years by thermal ALD using ammonia (NH_3) (≥500 °C) or hydrazine (N_2H_4) (<450 °C), as well as hollow cathode PEALD using NH_3 plasma, N_2-H_2 plasma, and N_2 plasma at low

temperatures (≤400 °C). I have also performed comprehensive literature review regarding SiN_x ALD research in the past two decades, and published one review paper, entitled "Atomic layer deposition of silicon nitride thin films: A review of recent progress, challenges, and outlooks" by Xin Meng, Young-Chul Byun, Harrison S. Kim, Joy S. Lee, Antonio Lucero, Lanxia Cheng, and Jiyoung Kim (*Materials* **2016**, 9, 1007) [56]. Additionally, I have submitted several original research papers on this topic. Although a discussion on these works is not covered in this dissertation, study on SiN_x ALD is still an importance part of my PhD research.

1.4 Dissertation Outline

Chapter 1 introduces this work and provides a research background overview of InGaAs MOS devices and AlGaN/GaN HEMTs. Additionally, the principle of ALD technique is discussed.

Chapter 2 provides the experimental procedure of this dissertation, including ALD reactors, facilities and methodology for material characterization, electrical characterization, and device fabrication.

Chapter 3 focuses on the study of high-k/$In_{0.53}Ga_{0.47}As$ interface passivation using ALD-based passivation techniques. By examining the C-V characteristics of MOSCAPs fabricated on n-type and p-type substrates at various conditions, the effect of in situ ALD diethylzinc (DEZ) treatment is determined. The absence of a hump-like response, the presence of inversion-like C-V characteristics on an n-type substrate, as well as the first principle DFT simulation results, all suggest that ALD DEZ treatment effectively passivates the defects near the mid gap and the valence band edge of $In_{0.53}Ga_{0.47}As$. Additionally, the efficacy of in situ ALD DEZ-based interface passivation is demonstrated on inversion-type n-channel MOSFETs and p-channel MOSFETs. Particularly, the first demonstration of p-channel MOSFETs makes the in situ ALD DEZ-based

interface passivation techniques highly promising to be implemented in InGaAs CMOS technology.

Chapter 4 discusses the results of SiN_x/GaN MIS-HEMTs with a crystalline interfacial layer. The SiN_x layer grown by hollow cathode PEALD serves as not only a gate dielectric for a lower leakage current, but also a surface passivation layer on access region to reduce the current collapse. The reliability of MIS-HEMTs is examined using gate bias stress measurement and pulsed I-V measurement. It is suggested that the excellent reliability is attributed to the effective passivation of surface/interface traps by PEALD-grown crystalline interfacial layer, as well the negligible bulk traps in the PEALD SiN_x layer.

Chapter 5 presents a study of the effect of ALD-grown epitaxial ZnO cap layer on the electrical characteristics of AlGaN/GaN heterostructure. According to HRTEM, epitaxial ZnO layer has an atomic sharp interface with GaN. Hall effect measurement determines a significant difference (2-3 orders of magnitude) in the electron density of H_2O-based ZnO and O_3-based ZnO. Compared to Schottky gate device, the devices with O_3-based ZnO cap layer show a significant positive shift of V_{th} (~1 V) while the devices with H_2O-based ZnO cap layer show a negligible shift of V_{th}.

Chapter 6 concludes this dissertation and discusses the ideas worthwhile for future study.

CHAPTER 2

EXPERIMENTAL

2.1 Introduction

This chapter describes the experimental procedure of this dissertation, including ALD reactors, facilities and methodology for material characterization, electrical characterization, and device fabrication.

2.2 ALD Reactors

2.2.1 Cambridge Nanotech Thermal ALD

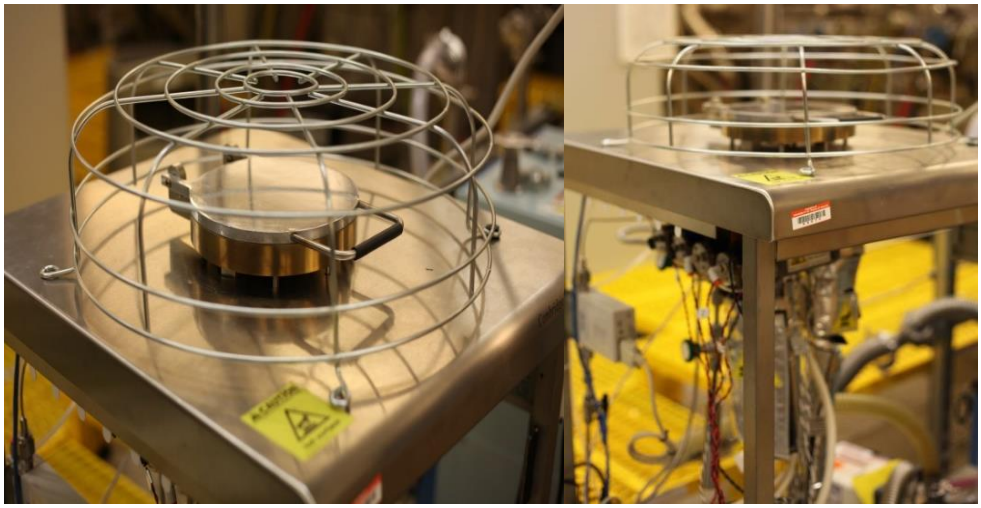


Figure 2.1. Cambridge Nanotech/Ultratech Savannah S100 (CNT) ALD reactor.

Figure 2.1 shows the Cambridge Nanotech/Ultratech Savannah S100 (CNT), which is a cross-flow type of thermal ALD reactor using metal-organic precursors to grow various films, especially metal oxides such as Al_2O_3, HfO_2, ZrO_2, ZnO. Deionized water (DI H_2O) or high-concentration ozone (O_3, 400 g/m^3) is used as an oxidant. O_3 generator (OP-250H) is provided by

Toshiba-Mitsubishi-Electric Industrial Systems Corporation (TMEIC). High purity inert gas (argon or nitrogen, BIP grade, 99.9999%) is used as a carrier gas and a purge gas, respectively. Under a constant flow of 20 sccm inert gas, the chamber maintains at a pressure of 0.4-0.5 Torr with a rotary vane pump.

2.2.2 Hollow Cathode Plasma-Enhanced ALD

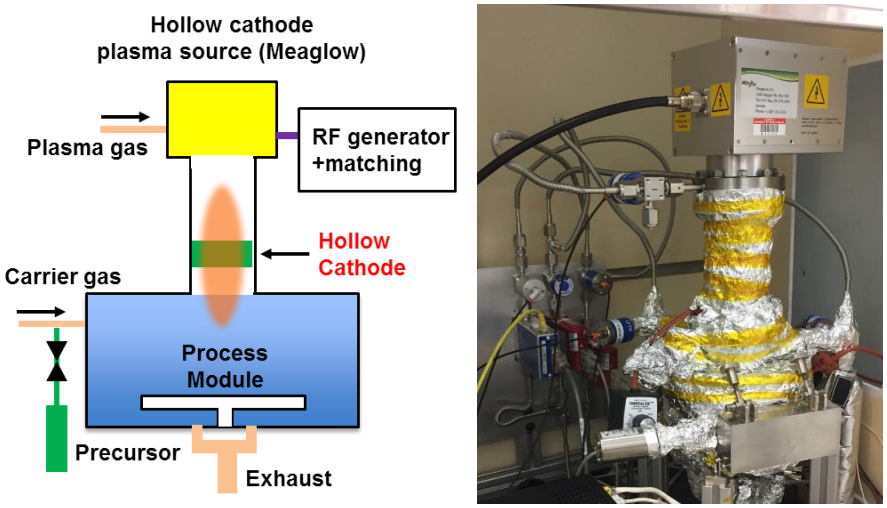
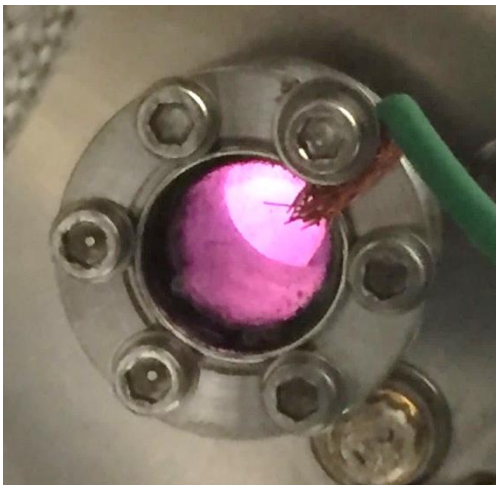


Figure 2.2. Schematic diagram and image of hollow cathode plasma-enhanced ALD reactor.

As shown in Figure 2.2 and 2.3, the hollow cathode plasma-enhanced ALD reactor is a customized ALD system equipped with a custom-built hollow cathode plasma source (Meaglow Ltd.). The reactor has a remote plasma configuration with a distance of ~5 inches between the hollow cathode and the wafer substrate. The plasma operates at a radio frequency of 13.56 MHz. The stainless-steel chamber wall and the exhaust tube are heated to ~120 °C. The precursor delivery lines are heated to 90 °C to prevent condensation of precursors. As shown in Figure 2.3, the unique features of a hollow cathode plasma source include high plasma density, low oxygen contamination, improved film crystallinity, and low plasma damage.



Plasma Type	CCP	ICP	MP	HC
Plasma Density	Low	High ✓	High ✓	High ✓
Oxygen Contamination	Low ✓	High	High	Low ✓
Crystallinity	Average	Average	Average	Exceptional ✓
Plasma Damage	High	High	Low ✓	Low ✓
Growth Rates	Low	Medium	Medium	High ✓
Scalability	High ✓	Medium	Low	High ✓

Figure 2.3. A hollow cathode plasma source, a view of plasma inside the reactor, and the unique features compared to other plasma sources (adapted from www.meaglow.com). CCP is capacitive coupled plasma (CCP), ICP is inductively coupled plasma, MP is microwave plasma.

The standard operating procedure of PEALD process is described as follows. A sample is dipped into dilute HF solution (100:1) for 3 min, rinsed with DI H_2O for 1 min, and dried by compressed N_2. The sample is then immediately loaded into the chamber at 100 °C, which will be pumped to a base pressure of ~10^{-6} Torr using a turbo pump. A long purging time (e.g., >2 hours) is typically used to make sure the oxygen and moisture content is as low as possible.

2.3 Material Characterization Facility

2.3.1 Spectroscopic Ellipsometer

Figure 2.4. J. A. Woolam M-2000DI spectroscopic ellipsometer.

Figure 2.4 shows the J. A. Woolam M-2000DI spectroscopic ellipsometer, which was used to characterize the film thickness and the refractive index (RI). The sample was clamped on the stage by vacuum. The spectra were collected at three different incident angles (55°, 65°, and 75°). The RI was reported at a wavelength of 633 nm.

2.3.2 X-ray Photoelectron Spectroscopy

Figure 2.5 shows the PHI VersaProbe II X-ray photoelectron spectroscopy (XPS) system with a monochromatic Al Kα X-ray source (E=1486.6 eV). It was used for characterizing the chemical state and composition. It has many useful features including charge neutralization, sputter depth profiling, and fully automated unattended analysis. Prior to scanning the spectra, the

film surface was sputtered with argon ions to remove the surface contamination layer. The atomic percentage of each element was estimated using peak area and atomic sensitivity factor.

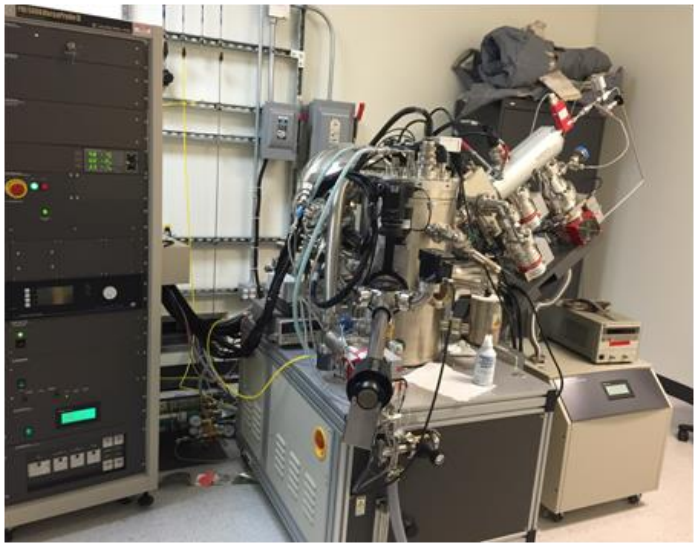


Figure 2.5. PHI VersaProbe II XPS system.

2.3.3 Atomic Force Microscopy

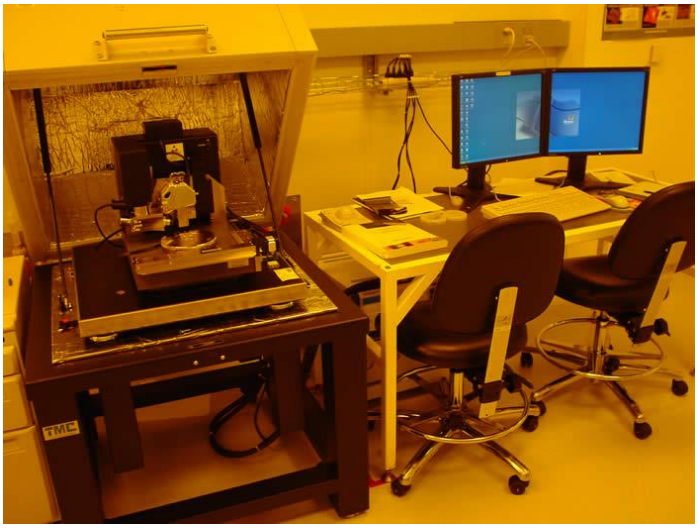


Figure 2.6. Veeco 5000 AFM located in UTD NSERL cleanroom.

The surface morphology of materials and the profile of nanoscale device features were characterized by atomic force microscopy (AFM). Figure 2.6 shows the Veeco 5000 AFM which locates in UTD NSERL cleanroom. The representative applications include evaluating the film surface roughness or the etching profile, inspecting photoresist (PR) or etching residues. AFM measurement is usually performed under tapping mode with a scan rate of 0.5-0.8 Hz, on an area ranging from 1 μm×1 μm to 10 μm×10 μm. The shield is closed during the measurement to minimize any mechanical noise interference.

2.3.4 Profilometer

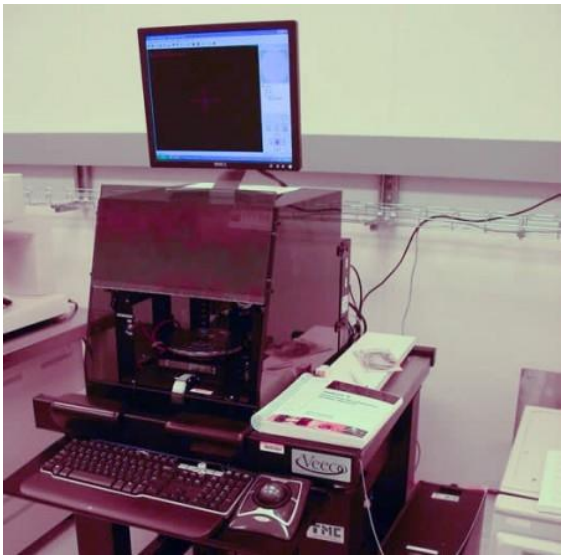


Figure 2.7. Veeco Dektak VIII profilometer located in UTD NSERL cleanroom.

Figure 2.7 shows the Veeco Dektak VIII profilometer, which can measure the profile of a pattern on the sample surface. For example, the step height of mesa isolation and the ohmic metal stack thickness of AlGaN/GaN HEMTs were determined via the profilometer. It is also widely being used to measure the photoresist thickness.

2.3.5 High-Resolution Transmission Electron Microscopy

High-resolution transmission electron microscopy (HRTEM) images were captured using JEOL 2100F analytical TEM or JEM-ARM200F atomic resolution analytical microscope in UTD NSERL. Samples were prepared using FEI Nova 2000 focused ion beam (FIB).

2.4 Electrical Characterization Facility

2.4.1 Cascade Probe Station

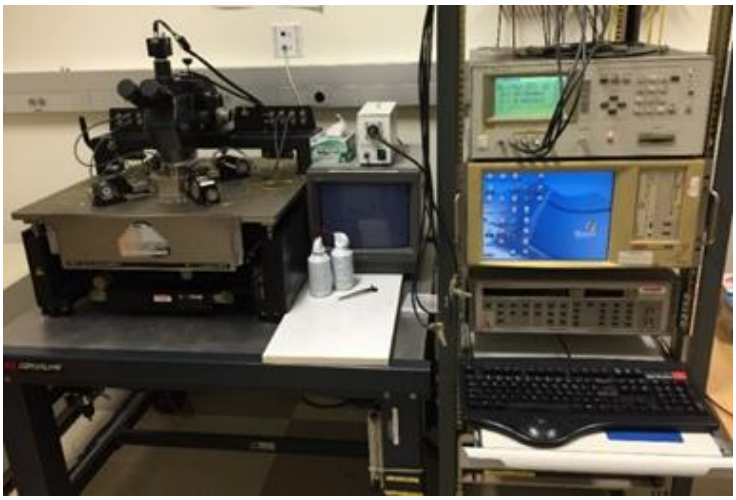


Figure 2.8. The Cascade probe station, HP 4284 LCR meter and Keithley 4200 semiconductor parameter analyzer.

Figure 2.8 shows a Cascade probe station which is connected to a HP 4284 LCR meter and a Keithley 4200 semiconductor parameter analyzer. After contacting the metal electrodes with replaceable coaxial probes, the capacitance-voltage (C-V) and current-voltage characteristics (I-V) of devices were measured in a dark environment. The samples were clamped on the chuck by vacuum. The measurements were typically done at room temperature (25 °C). The chuck can be heated up to 200 °C for temperature-dependent measurement.

2.4.2 Cryogenic Probe Station

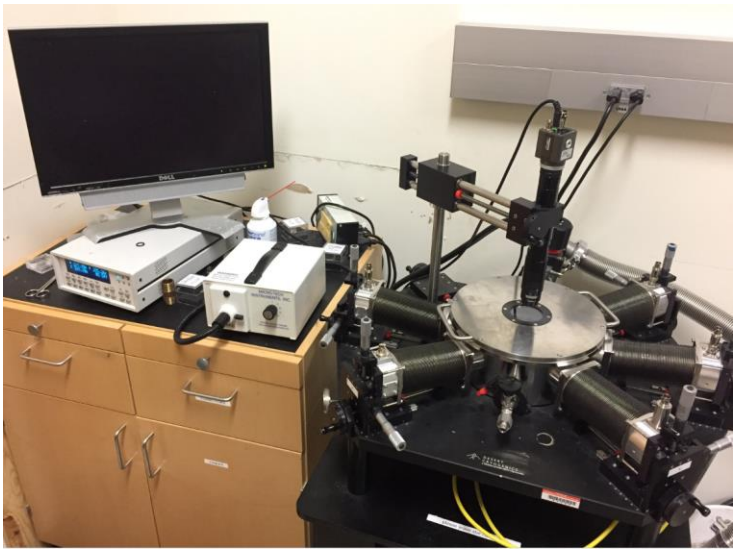


Figure 2.9. Cryogenic probe station, model TTPX, Lake Shore Cryotronics, Inc.

Figure 2.9 shows the cryogenic probe station (Lake Shore, model TTPX), which is capable to measure the I-V and C-V characteristics of devices at a substrate temperature between 4.2 K and 475 K under a high vacuum condition (~10^{-6} Torr). The samples were attached to the chuck by coating a small amount of conductive silver paste on the backside. Therefore, the samples could maintain a good electrical contact with the chuck (grounding) and be invulnerable to position shift during pumping, venting, and measurement. At the end of the measurements, the samples should be carefully removed after spraying acetone to soften the silver paste.

In this work, the cryogenic probe station was used to measure InGaAs MOS devices at low temperature (e.g., 100 K). The chuck was cooled by liquid nitrogen. HP 4284 LCR meter was used for C-V measurement controlled by a Labview program. HP 4155A semiconductor parameter analyzer was used for I-V measurement.

2.4.3 Hall Effect Measurement

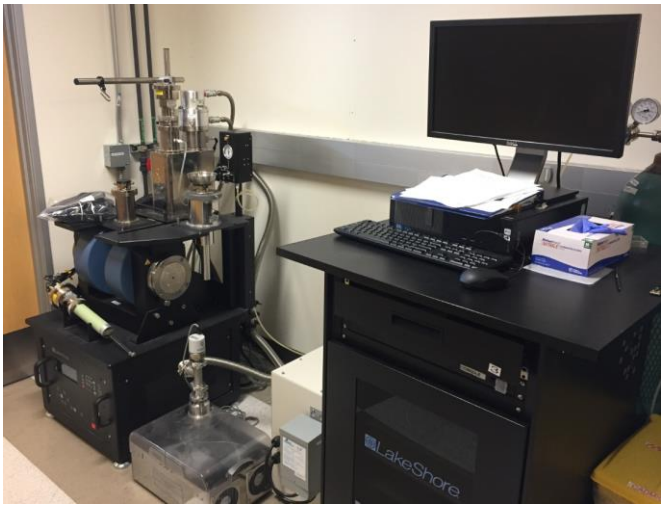


Figure 2.10. Lake Shore 8400 series Hall measurement system.

Figure 2.10 shows the Lake Shore 8400 series Hall measurement system. Under AC field setup, the system can measure mobility from 1×10^{-3} to 1×10^{6} $cm^2/V\cdot s$, carrier concentration from 8×10^{2} to 8×10^{23} cm^{-3}, and resistivity from 1×10^{-5} to 1×10^{5} $\Omega\cdot cm$, respectively. In this work, van der Pauw four-point configuration (1 cm×1 cm) was used. The mobility, resistivity, carrier concentration, and type of carrier were determined at room temperature.

2.5 Device Fabrication and Mask Layout

All the devices in this work were fabricated in UTD cleanroom located at Natural Science and Engineering Research Laboratory (NSERL). The cleanroom includes facilities for device fabrication and characterization, such as PECVD, LPCVD, ICP/RIE plasma etcher, metallization tools (e.g., sputter, e-beam, and thermal evaporation), acid/base/solvent chemical hoods, thermal processing tools (e.g., oxidation/diffusion, furnace tube annealing, rapid thermal annealing),

lithography tools (e.g., Karl Suss MA6 BA6 contact aligner and Raith 150 two e-beam lithography system), and characterization tools (e.g., SEM, optical microscope, and ellipsometer).

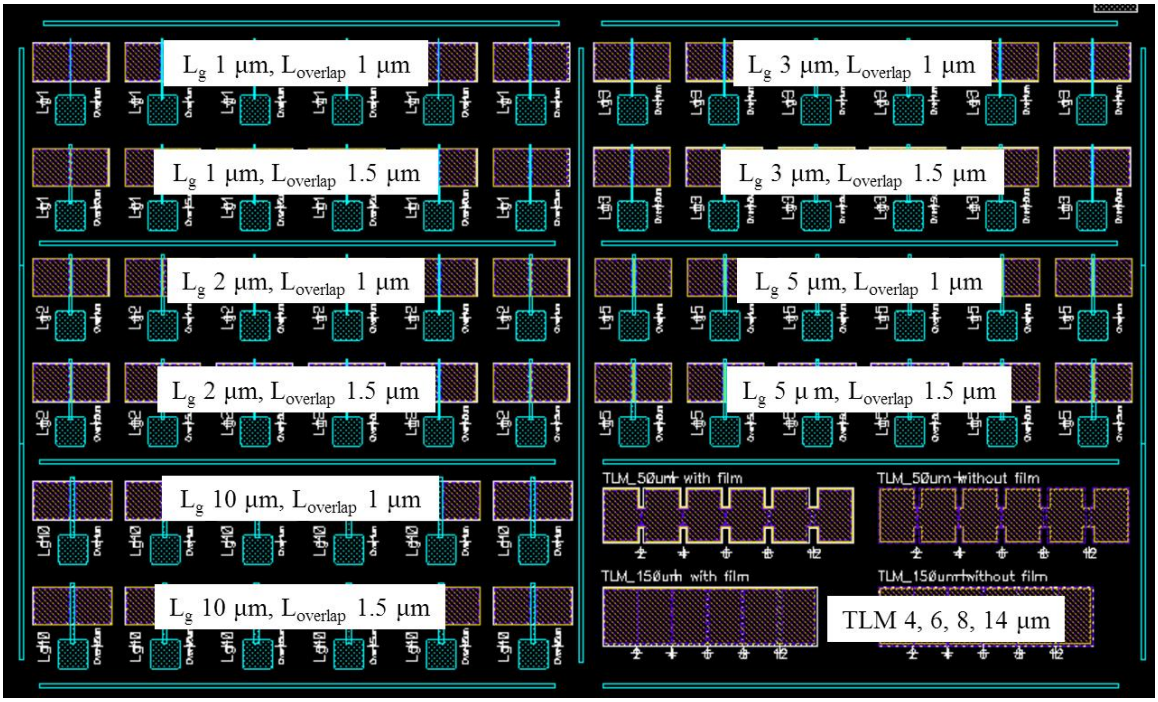


Figure 2.11. Mask layout designed by Dr. Jae-Gil Lee for InGaAs MOSFETs fabrication.

Figure 2.11 shows the mask layout designed by Dr. Jae-Gil Lee for InGaAs MOSFETs fabrication. The MOSFETs have various channel length (L_g) from 2 μm to 10 μm. There are also a few long-channel (L_g=40 μm) MOSFETs, which are not shown in Figure 2.11. All the measured devices have an overlap length ($L_{overlap}$) of 1.5 μm with the implanted source and drain region, i.e. actual metal gate length (L_G) is L_g+2$L_{overlap}$. For MOSFET with a channel length of L_g=3 μm, actual L_G is 6 μm. The transmission line measurement (TLM) structures have a distance of 4 μm, 6 μm, 8 μm, and 12 μm and a width of 150 μm. The ion implantation was performed by CuttingEdge Ions, LLC (California, US).

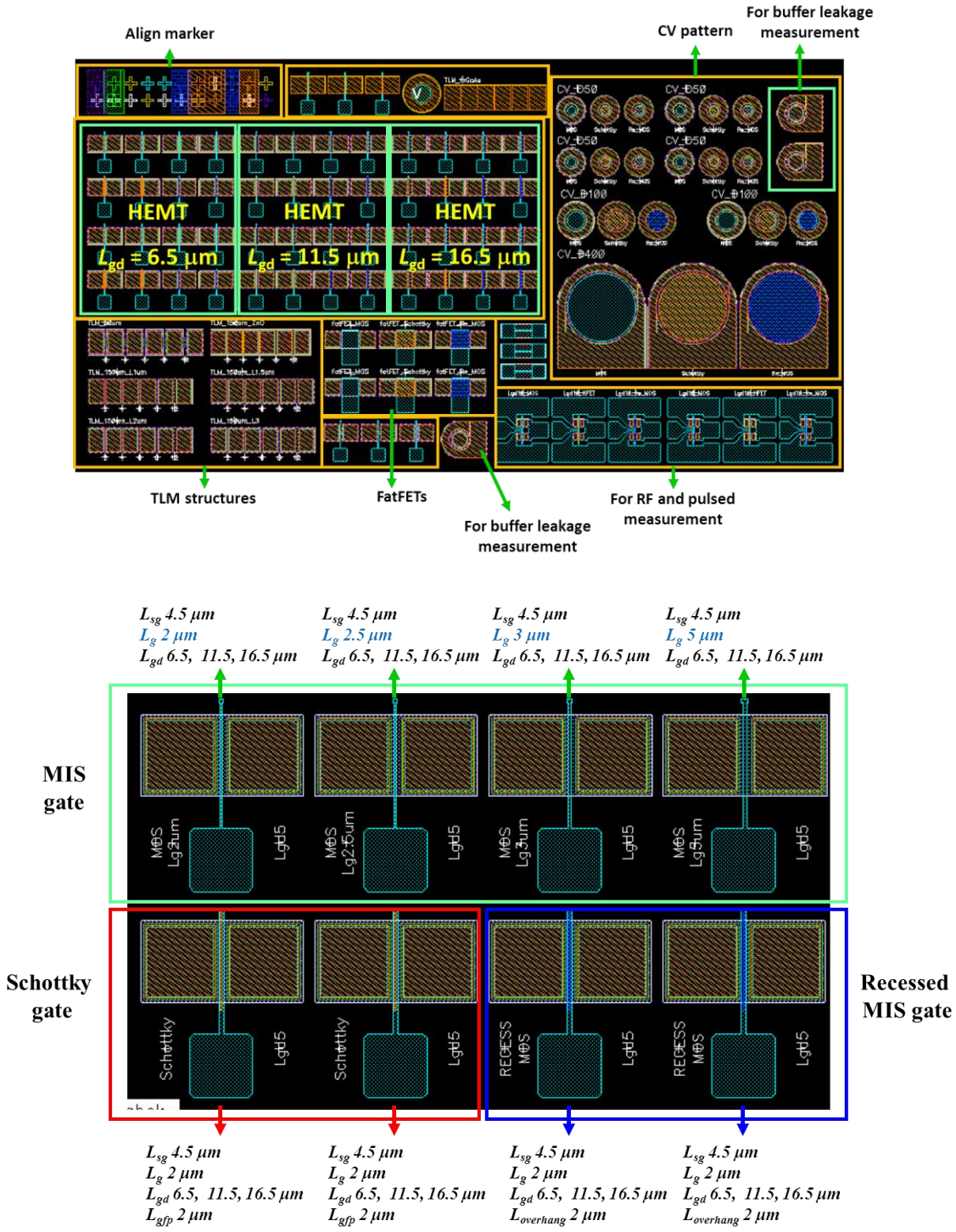


Figure 2.12. Mask layout designed by Dr. Jae-Gil Lee for GaN HEMTs fabrication.

Figure 2.12 shows the mask layout designed by Dr. Jae-Gil Lee for GaN HEMTs fabrication. The MOSFETs have various channel length (L_g) from 2 μm to 5 μm. There are also a few long-channel (100 μm) devices (FatFETs). The MIS-gate structures were selected for measurement in this work. The TLM structures for measurement in this dissertation have a distance of 4 μm, 6 μm, 8 μm, 10 μm, and 14 μm and a width of 150 μm.

The detailed device fabrication procedure will be discussed separately in chapter 3, chapter 4, and chapter 5. Additionally, the general process flows of InGaAs MOSFET and GaN HEMT are provided in Appendix A and Appendix B.

2.6 Device Characterization Methods

2.6.1 Transmission Line Measurement

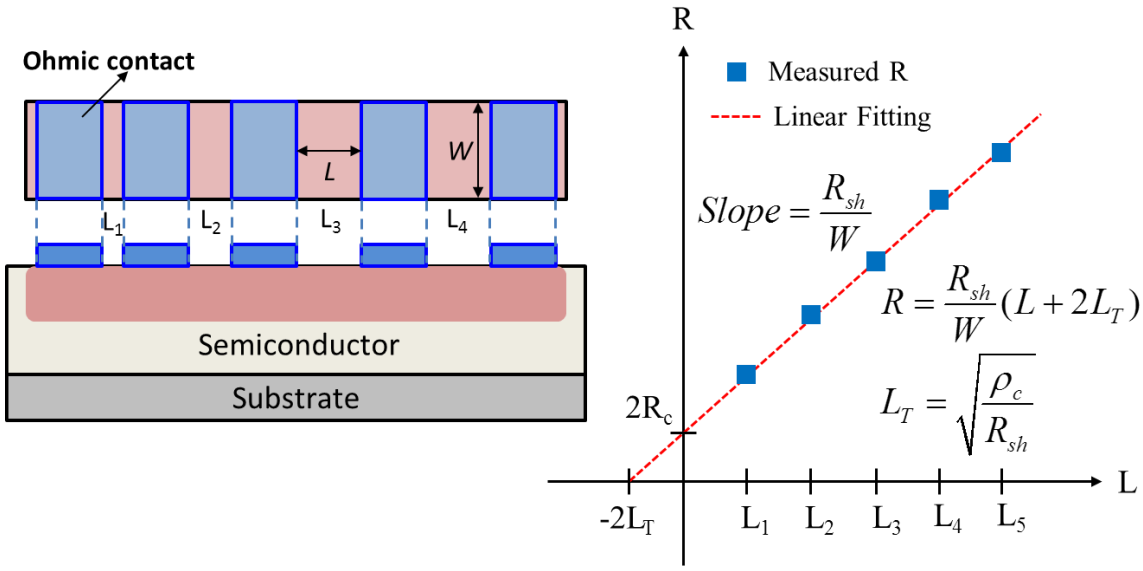


Figure 2.13. Schematic of contact resistance (R_c), sheet resistance (R_{sh}), and specific contact resistivity (ρ_c) calculation using TLM.

Transmission line measurement (TLM) is widely used to extract the contact resistance (R_c), the sheet resistance (R_{sh}), and the specific contact resistivity (ρ_c) of ohmic contact on semiconductor. As shown in Figure 2.13, TLM structure is fabricated on an isolated area that consists several contact pads with a varied distance (L) and a fixed width (W). By measuring the linear I-V characteristics of two adjacent pads, the total resistance (R_T) can be extracted as a function of L. Using a linear fitting line, twice of the contact resistance ($2R_c$, ohm) and twice of the transfer length ($2L_T$) from the intersections on vertical and horizonal axis can be obtained, respectively. According to the equation shown in Figure 2.13, R_{sh} can be extracted using the slope of the linear fitting line and ρ_c can be extracted using the L_T and R_{sh}. The typical units for R_c, R_{sh}, and ρ_c are ohm·mm, ohm/sq, and ohm·cm^2.

2.6.2 Positive/Negative Bias Instability (PBI or NBI) Stress Measurement

The stress measurement was used to evaluate the threshold voltage (V_{th}) instability of GaN MIS-HEMTs under a positive or negative gate bias stress. The instability is ascribed to the electron trapping in the gate insulator and near the insulator/III-N interface. The procedure was similar to the method described by P. Lagger et al. [80], as shown in Figure 2.14. First, a measurement of fresh device was performed. Then, the bias stress ($V_{g,stress}$) was only applied on gate terminal while source and drain terminals were grounded (V_d=V_s=0 V). At selected time intervals, I_{ds}-V_g transfer curve measurement temporarily interrupted the stress. The stress time (t_{stress}) started from 1 s up to 10000 s. Therefore, the drift of V_{th} (ΔV_{th}) as a function of the t_{stress} was determined. Keithley 4200-SCS was used for the measurement. The software can define the measurement conditions (e.g., stress time and stress-to-measure delay time) for automatic execution, as shown in Figure 2.15.

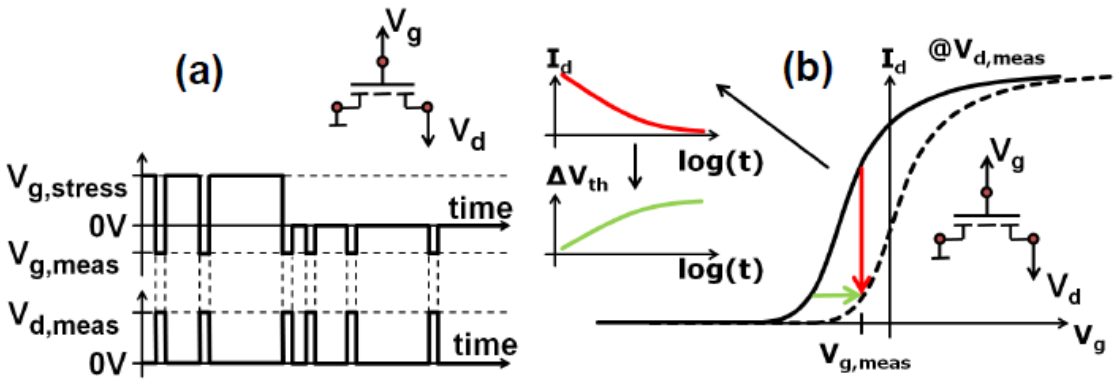


Figure 2.14. An example of the method for characterizing the V_{th} instability of GaN MIS-HEMTs described by P. Lagger et al. [80]. Adapted from P. Lagger, et al., IEEE International Electron Devices Meeting (IEDM 12), pp. 13-1, with permission. Copyright 2012, IEEE.

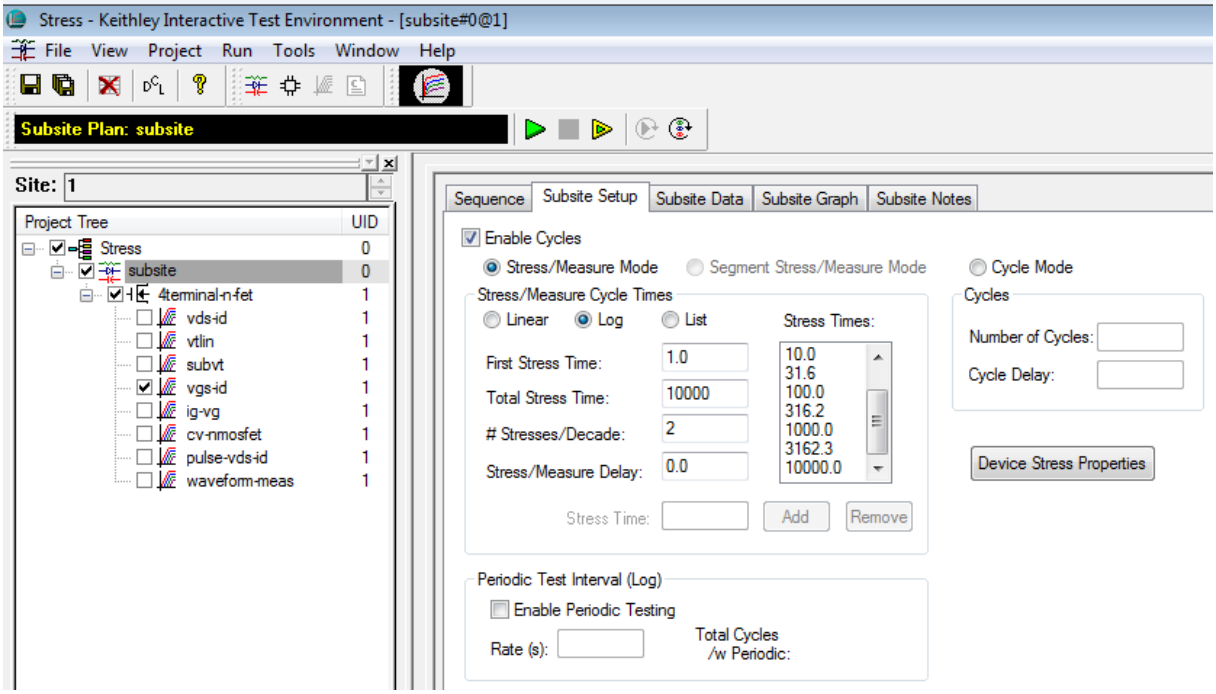


Figure 2.15. Snapshot of the stress measurement program of Keithley 4200-SCS.

2.6.3 Pulsed I-V Measurement

Figure 2.16 shows a basic comparison between direct current (DC) I-V measurement and pulsed I-V measurement [81]. In this dissertation, the dynamic electrical properties of GaN MIS-HEMTs was analyzed using pulsed I-V measurement, which can characterize dynamic R_{on} (current collapse) behavior to examine the quality of surface passivation [82]. Two Keithley 4225-RPM units were connected to the gate terminal and drain terminal, respectively, while the source terminal was grounded. Pulsed waveforms were applied for fast I-V measurement. As shown in Figure 2.17, user can define the pulse timing in the program of Keithley 4200 SCS. A low duty cycle (stress time/period time in a single pulse waveform) of 0.1% was used. The period of the waveform was 10^{-3} s (1 ms), the pulse width was 8×10^{-7} s (800 ns), and the rise/fall time of the pulse waveform was 2×10^{-7} s (200 ns).

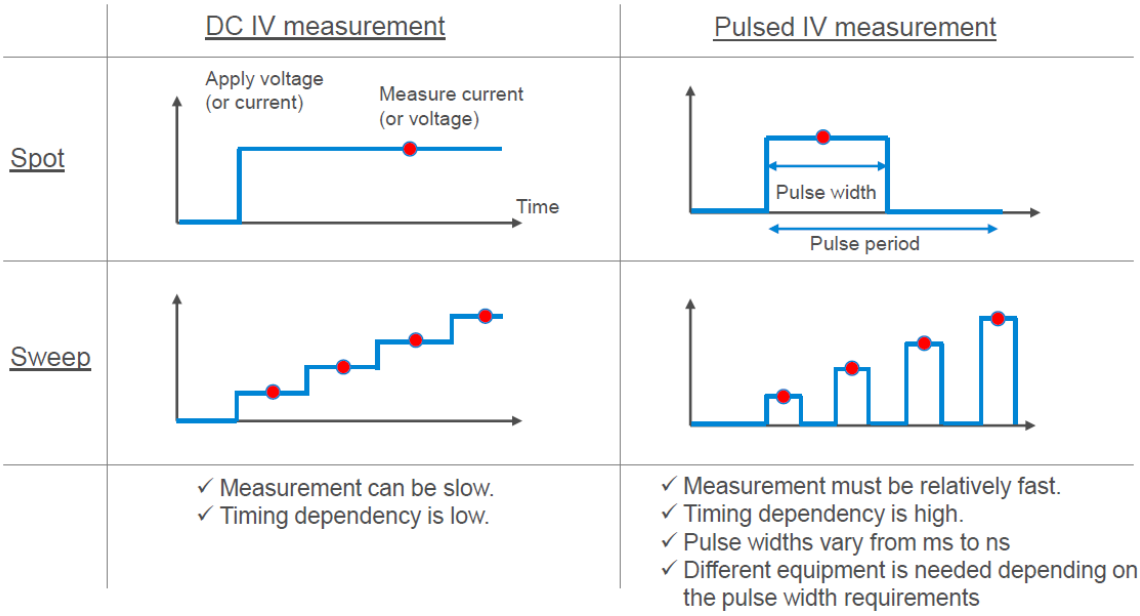


Figure 2.16. Comparison between DC I-V measurement and Pulsed I-V measurement. Source: "Fundamentals of fast pulsed IV measurement" by Alan Wadsworth, Agilent Technologies [81].

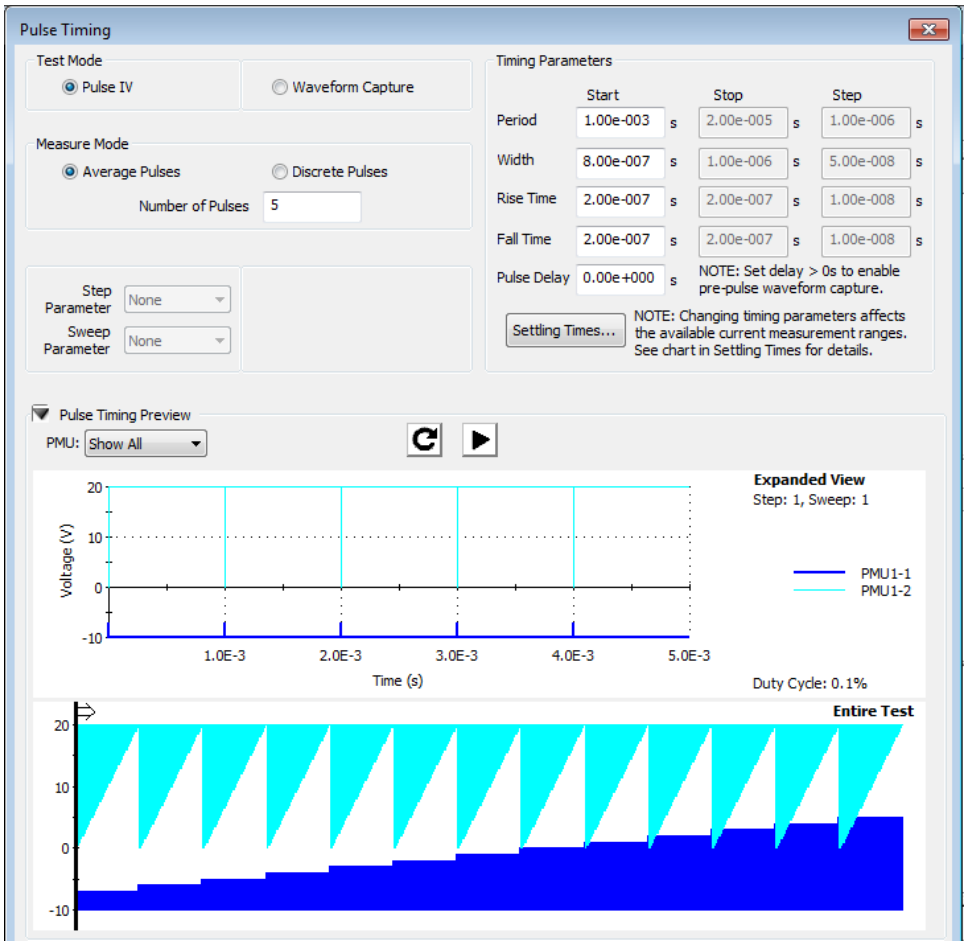


Figure 2.17. A snapshot of pulse timing window in the pulsed I-V measurement program of Keithley 4200-SCS.

CHAPTER 3

$IN_{0.53}GA_{0.47}AS$ MOS DEVICES USING ALD-BASED INTERFACIAL PASSIVATION LAYER AND HIGH-K GATE DIELECTRIC STACKS

3.1 Introduction

High-k/metal gate technology allows the scaling of Si CMOS technology to sub-7 nm node [83]. There have been long efforts to develop and optimize high-k gate dielectric stacks on silicon. However, the development of high-k gate stacks on III-V semiconductors is far more challenging because of the complex chemical composition on the surface of III-V semiconductors. The surface channel MOS devices suffer from Fermi level pinning due to the formation of defective interfacial layers on high-k/InGaAs interface. Therefore, the development of an effective interface passivation technique will be critical to obtain high-performance and highly reliable devices.

Chapter 3 will focus on ALD-based interfacial passivation layer and high-k gate dielectric stacks on n-type and p-type $In_{0.53}Ga_{0.47}As$ MOS devices, which include MOS capacitors (MOSCAPs) and MOS field-effect transistors (MOSFETs). The structures include ultra-thin (a few angstroms) interfacial passivation layer and 3-5 nm-thick insulating high-k oxide grown by ALD. Particularly, ALD diethylzinc (DEZ) based interface passivation will be extensively discussed in this work. Besides, alternative ALD-based interface passivation techniques including magnesium-containing ALD precursor treatment and hollow cathode PEALD-AlN interlayer will be discussed. To demonstrate the efficacy of ALD DEZ-based interface passivation on MOSFETs, both inversion-type n-channel MOSFETs and p-channel MOSFETs were fabricated on $In_{0.53}Ga_{0.47}As$ substrate. I would like to acknowledge Dr. Jae-Gil Lee, Dr. Antonio T. Lucero, and

Dr. Young-Chul Byun for their contributions to the early development of MOSCAP and MOSFET fabrication process in UTD.

3.2 $NH_4OH/(NH_4)_2S$ Treated $In_{0.53}Ga_{0.47}As$ MOSCAPs using ALD-Grown High-k Gate Dielectric Stacks without ALD-Based Interface Passivation

3.2.1 Experimental

The $In_{0.53}Ga_{0.47}As$ wafers purchased from IntelliEpi (Richardson, TX, USA) was used for device fabrication. The epitaxial structure information is listed in Table 3.1 and 3.2. The schematic of the $In_{0.53}Ga_{0.47}As$ MOSCAP fabrication process flow is illustrated in Figure 3.1.

Table 3.1. The epitaxial structure information of n-type $In_{0.53}Ga_{0.47}As$ wafer.

Layer	Material	Thickness (nm)	Dopant	Level ($/cm^3$)	Type	Notes
2	$In_{0.53}Ga_{0.47}As$	300	Si	1×10^{17}	n	-
1	$In_{0.53}Ga_{0.47}As$	500	Si	4×10^{17}	n	-
Substrate	n+ InP	-	-	-	n	4-inch

Table 3.2. The epitaxial structure information of p-type $In_{0.53}Ga_{0.47}As$ wafer.

Layer	Material	Thickness (nm)	Dopant	Level ($/cm^3$)	Type	Notes
2	$In_{0.53}Ga_{0.47}As$	300	Be	1×10^{17}	p	-
1	$In_{0.53}Ga_{0.47}As$	500	Be	4×10^{17}	p	-
Substrate	p+ InP	-	-	-	p	3-inch

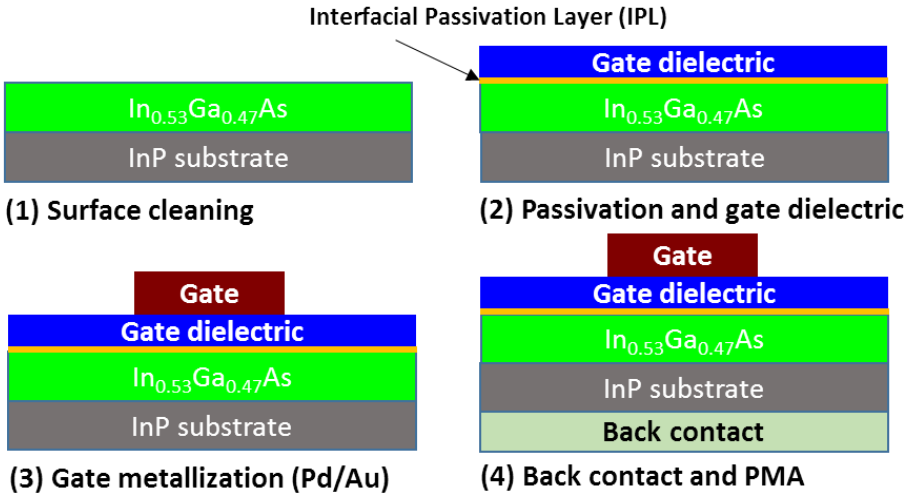


Figure 3.1. Schematic of the $In_{0.53}Ga_{0.47}As$ MOSCAP fabrication process flow.

The substrate was diced into small samples carefully by hand using a diamond scribe. After the surface particles were removed with a nitrogen gun, the samples were cleaned with acetone using an airbrush. Then, a standard solvent cleaning procedure was performed to remove organic contamination: rinse in acetone, methanol, isopropanol alcohol (IPA) and de-ionized (DI) water (optional) for 3 min, 1 min, 1 min, and 1 min, respectively. Handling the samples should be very careful since the InP substrate is extremely fragile. Finally, the samples were blown dry with a nitrogen gun.

Next, the samples were cleaned in 29% NH_4OH solution for 1 min, rinsed thoroughly with DI H_2O (30 s) and blown dry quickly with an N_2 gun. Then, the samples were immediately transferred to a ~10% $(NH_4)_2S$ solution for 20 min sulfur passivation and given a thorough a continuous clean DI H_2O flow rinse (30−60 s) followed by N_2 dry. The $(NH_4)_2S$ cleaning conditions were selected based on the paper published by B. Brennan et al. from UTD [12]. To

suppress the degradation of passivation due to the re-oxidation in the air, it is critical to minimize the sample loading time (usually <60 s) in the ALD reactor after wet-cleaning treatment.

The ALD gate insulators were grown in the Cambridge Nanotech S100 thermal ALD reactor. Tetrakis(dimethylamido)hafnium (TDMA-Hf, heated at 75 °C, Sigma-Aldrich) and DI H_2O (room temperature) were used for HfO_2 deposition. HfO_2 was grown at 200 °C using a TDMA-Hf/purge/H_2O/purge of 0.2/10/0.03/10 s. Likewise, tetrakis(dimethylamido)Zicornium (TDMA-Zr, heated at 75 °C, Sigma-Aldrich) and DI H_2O were used for ZrO_2 deposition. To grow $Hf_{0.5}Zr_{0.5}O_2$, a super-cycle recipe containing a TDMA-Hf/purge/H_2O/purge of 0.2/20/0.03/10 s and a TDMA-Zr/purge/H_2O/purge of 0.2/20/0.03/10 s was used at 200 °C. Recently, there have been great interests to use ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for the application of negative capacitance FETs (NC-FETs) [84] and ferroelectric FETs (FeFETs) [85]. Four samples were fabricated on either n-type or p-type substrate, as shown in Table 3.3. After $NH_4OH/(NH_4)_2S$ cleaning, ~4 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) was grown by repeating 20 super-cycles (total 40 sub-cycles) of ALD process and ~4 nm HfO_2 was grown by repeating 40 cycles of ALD process.

Table 3.3. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples with ALD-grown $Hf_{0.5}Zr_{0.5}O_2$ and HfO_2 gate insulators.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	No	4 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	No	4 nm HfO_2
(c)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	No	4 nm $Hf_{0.5}Zr_{0.5}O_2$
(d)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	No	4 nm HfO_2

Subsequently in the cleanroom, a negative photoresist (PR, NLOF 2020) was spin-coated and MOSCAPs PR pattern was formed using Karl Suss MA6 BA6 contact aligner and AZ300 MIF developer (60 s). A Pd/Au (20 nm/100 nm) gate electrode was deposited using e-beam evaporator and patterned with a lift-off process. The InP substrate backside was gently scratched by a diamond scribe and immediately loaded into e-beam evaporator for backside ohmic contact deposition (Ti/Au 20 nm/200 nm). Finally, the sample was annealed in a rapid thermal processing (RTP) chamber at 300 °C in a forming gas (95% N_2/5% H_2) ambient for 5 min and ready for electrical characterization. Devices with a gate electrode diameter of 75 μm were measured (Figure 3.2).

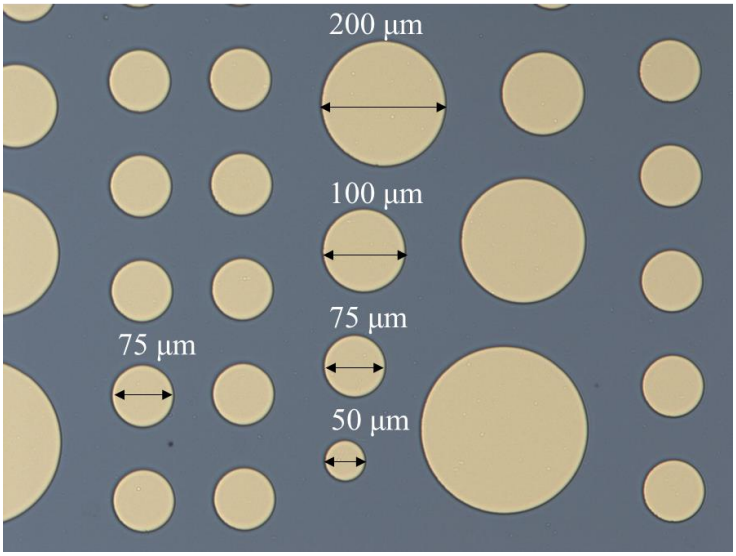


Figure 3.2. Optical microscope image of the $In_{0.53}Ga_{0.47}As$ MOSCAPs.

3.2.2 Results and Discussions

Figure 3.3 shows the capacitance-voltage (C-V) characteristics of $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAPs on n-type and p-type substrates side by side. The C-V measurement was performed at room temperature (295 K) from 1 kHz to 1 MHz (total 31 scans, from depletion to

accumulation). In the case of MOSCAPs on n-type substrate, both ~4 nm $Hf_{0.5}Zr_{0.5}O_2$ sample (a) and ~4 nm HfO_2 samples (b) show a pronounced frequency dispersion with a "hump-like" feature at the negative voltage region of the C-V curves (depletion or weak inversion region for an n-type substrate). Furthermore, for sample (c) and (d) on p-type substrate, we observed a pronounced frequency dispersion at the negative voltage region of the C-V curves (accumulation region for a p-type substrate). The curves are significantly stretched out because of the contribution of interface trap capacitance (C_{it}). This phenomenon clearly indicates the Fermi levels were pinned for $In_{0.53}Ga_{0.47}As$ samples with only $NH_4OH/(NH_4)_2S$ surface treatment, ascribed to a high interface trap density (D_{it}) existing near the lower half of the band gap (between mid-gap and the edge of valance band).

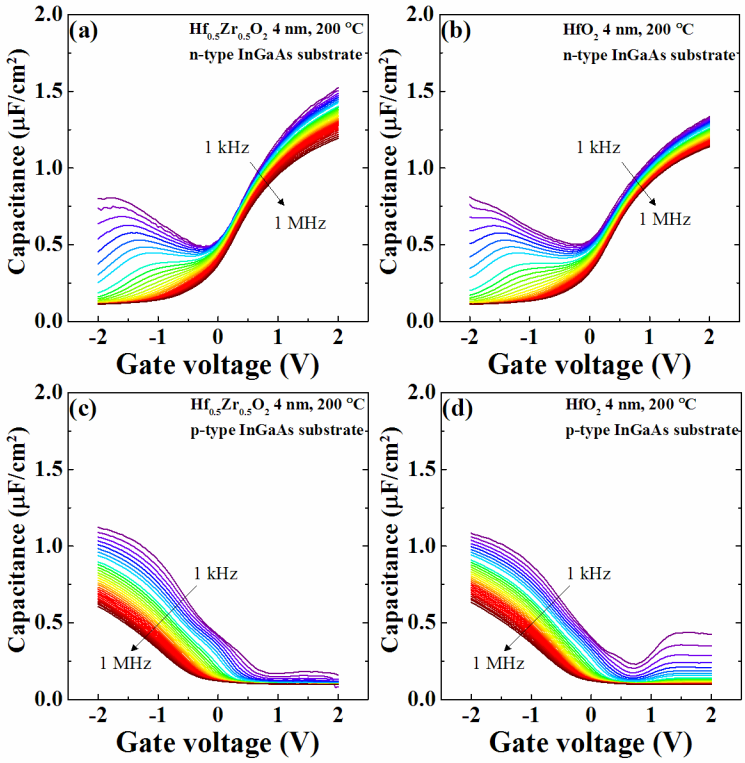


Figure 3.3. C-V frequency dispersion characteristics for $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAPs with (a, c) 4 nm $Hf_{0.5}Zr_{0.5}O_2$ and (b, d) 4 nm HfO_2 ALD-grown gate insulator.

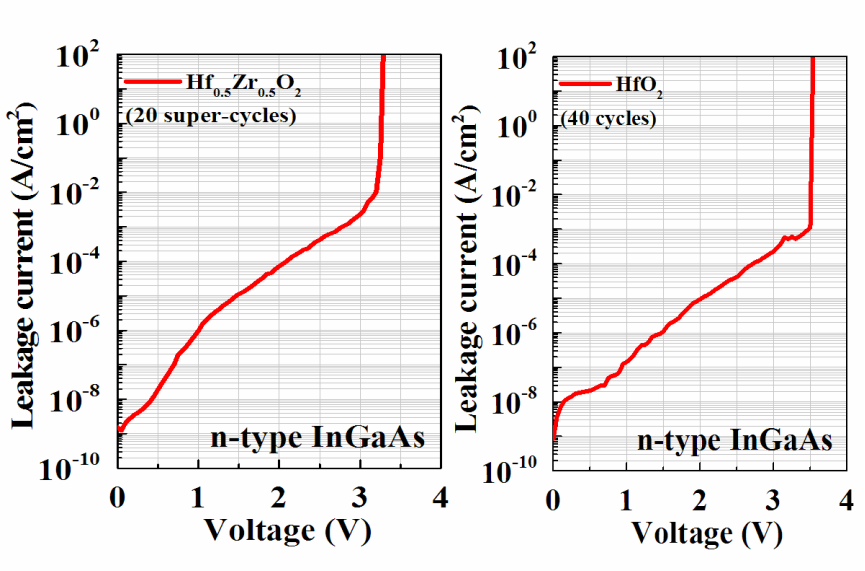


Figure 3.4. Breakdown characteristics for $NH_4OH/(NH_4)_2S$ treated MOSCAPs on n-type $In_{0.53}Ga_{0.47}As$ substrate with 4 nm $Hf_{0.5}Zr_{0.5}O_2$ and 4 nm HfO_2 gate insulator.

Figure 3.4 shows the breakdown characteristics of the ~4 nm $Hf_{0.5}Zr_{0.5}O_2$ and ~4 nm HfO_2 samples on n-type substrate. The ~4 nm $Hf_{0.5}Zr_{0.5}O_2$ sample and ~4 nm HfO_2 sample both show a low leakage current ($<10^{-4}$–10^{-5} A/cm^2) within the C-V measurement voltage range (2 V) with a reasonable breakdown voltage of 3.2 V-3.5 V.

Figure 3.5 and Figure 3.6 show the C-V double-sweep hysteresis characteristics of ~4 nm $Hf_{0.5}Zr_{0.5}O_2$ and ~4 nm HfO_2 samples on n-type substrate at different maximum voltage (1.0 V, 1.5V, and 2.0V) during the measurement (100 kHz). The extracted hysteresis value is shown as a function of the maximum measurement voltage. Both samples exhibit comparable performance: a small hysteresis of ~50 mV at a maximum voltage of 1.0 V and a higher hysteresis of 80−100 mV at a maximum voltage of 2.0 V.

The results suggest that the $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAPs using $Hf_{0.5}Zr_{0.5}O_2$ and HfO_2 gate insulators shows similar C-V characteristics. The stretch-out of C-V curves and large frequency dispersion were observed on all the samples due to the Fermi level pinning and the contribution of C_{it}. Therefore, an interface passivation technique must be explored to improve the interface quality of high-k gate dielectric stack to obtain better C-V characteristics.

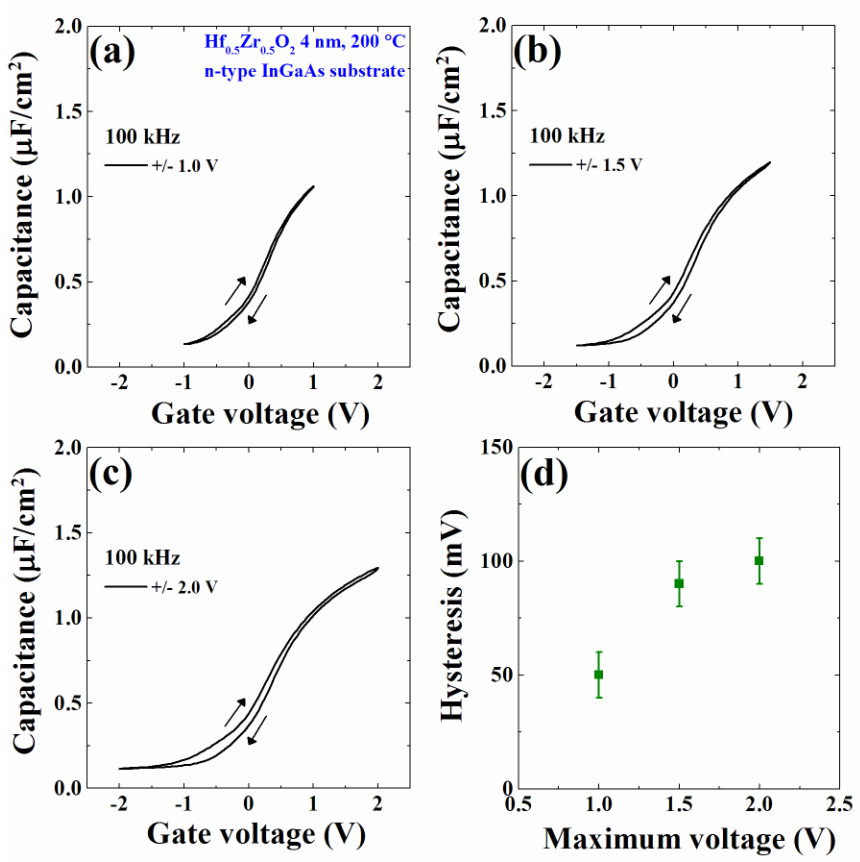


Figure 3.5. C-V hysteresis characteristics of $NH_4OH/(NH_4)_2S$ treated MOSCAPs on n-type $In_{0.53}Ga_{0.47}As$ substrate with 4 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulator as a function of maximum measurement voltage (a) 1.0 V, (b) 1.5 V, (c) 2.0 V, and (d) the corresponding hysteresis.

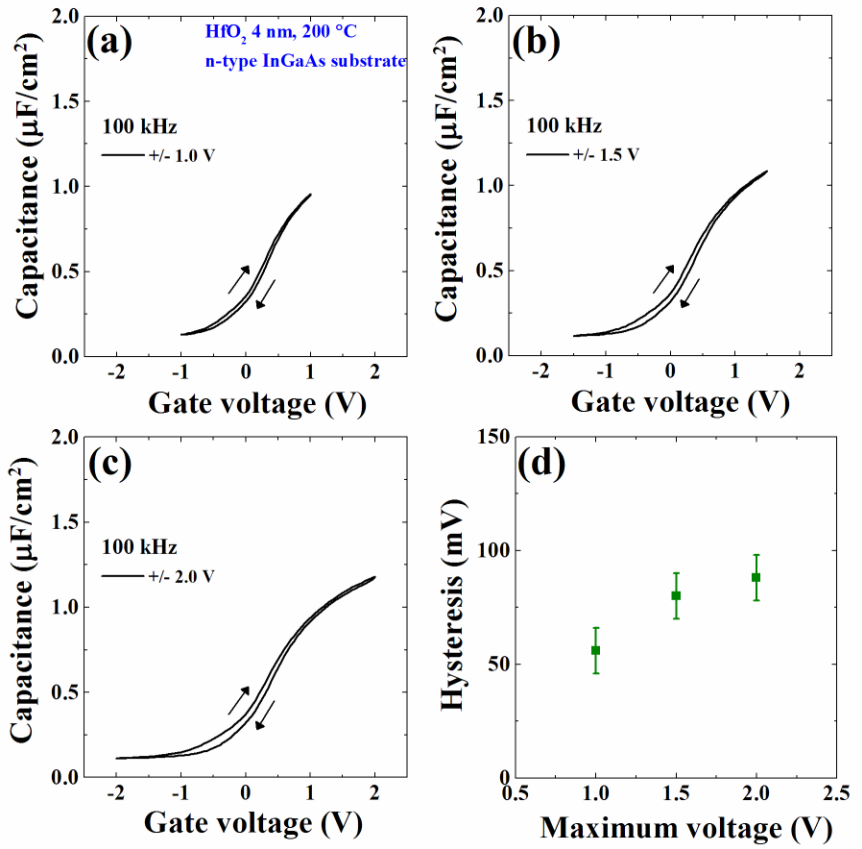


Figure 3.6. C-V hysteresis characteristics of $NH_4OH/(NH_4)_2S$ treated MOSCAPs on n-type $In_{0.53}Ga_{0.47}As$ substrate with 4 nm HfO_2 gate insulator as a function of maximum measurement voltage (a) 1.0 V, (b) 1.5 V, (c) 2.0 V, and (d) the corresponding hysteresis.

3.3 In situ ALD DEZ-Based Interface Passivation on $In_{0.53}Ga_{0.47}As$

3.3.1 Introduction

Previous studies have found that several ALD precursors including trimethylaluminum (TMA), tetrakis(ethylmethylamino)hafnium (TEMA-Hf) exhibited "self-cleaning effect" on GaAs, InGaAs substrate. The self-cleaning process was determined by the reduction and removal of native oxide via in situ XPS analysis [86-88]. The effective self-cleaning of surface oxides

successfully reduced the D_{it}. On the other hand, previous work done by Byun et al. and Lucero et al. have shown that the in situ ALD ZnO passivation (10 cycles of DEZ and H_2O pulse at 150 °C) prior to growing ALD-HfO_2 gate insulator can dramatically reduce the accumulation frequency dispersion and hysteresis in the C-V characteristics of MOSCAPs on p-type GaAs [89] and p-type $In_{0.53}Ga_{0.47}As$ substrate [90, 91]. This can be attributed to effective passivation of interface traps near the valance band edge by ZnO/ZnS interfacial passivation layer (IPL). In situ XPS study by Lucero et al. suggested that DEZ has weak "clean-up" effect on native oxide, but a ZnO/ZnS IPL can be formed in combination with the $(NH_4)_2S$ pretreatment. Improvement in C-V characteristics was also demonstrated on InP substrate by Kim et al. using ALD-grown 1.5-nm-thick ZnS and ZnO IPLs [92].

According to Byun et al., the ALD ZnO passivation was performed for only 10 cycles at 150 °C. The IPL layer should be very thin due to the incubation time of initial growth. However, the physical presence of ZnO/ZnS IPL, which has a lower dielectric constant than high-k insulator, is not desired from the perspective of equivalent oxide thickness (EOT) scaling. Furthermore, the introduction of H_2O during the ALD ZnO treatment may oxidize the fresh $NH_4OH/(NH_4)_2S$ treated surface, preventing the effective reduction of oxidation states by ALD precursors. Additionally, although ALD reaction is well known as a self-limiting surface reaction (saturated growth), increasing the number of DEZ/H_2O pulse cycle does not follow a saturated growth of the IPL. Therefore, a precise control of the number of ALD ZnO treatment cycle is required to avoid the growth of thick IPL (e.g., >1 nm).

This subsection will discuss a novel interface passivation technique using in situ ALD DEZ treatment without H_2O exposure on both n-type and p-type $In_{0.53}Ga_{0.47}As$ substrate. Using room

temperature (295 K) and low-temperature measurement (100 K), the saturation behavior in C-V characteristics on n-type $In_{0.53}Ga_{0.47}As$ substrate will be evaluated as a function of the number of ALD DEZ treatment cycle.

3.3.2 Experimental, Results, and Discussion

Table 3.4. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples without and with interface passivation by in situ ALD DEZ and ALD DEZ/H_2O surface treatment.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD Passivation	ALD Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	No	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(c)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ/H_2O 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(d)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	No	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(e)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	DEZ 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(f)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	DEZ/H_2O 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$

As shown in Table 3.4, $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples without and with interface passivation by in situ ALD DEZ (10 cycles) and ALD DEZ/H_2O (10 cycles) treatment were fabricated. After $NH_4OH/(NH_4)_2S$ treatment, samples were immediately loaded into Cambridge Nanotech S100 thermal ALD reactor at 150 °C. The ALD DEZ interface passivation was performed using a DEZ pulse/purge of 0.1/10 s for 10 cycles at 150 °C. The ALD DEZ/H_2O interface passivation was performed using a DEZ pulse/purge/DI H_2O pulse/purge of 0.1/10/0.05/10 s for 10 cycles at 150 °C. Subsequently, the samples were heated up to 200 °C in 10 min and deposited with the $Hf_{0.5}Zr_{0.5}O_2$ film (25 super-cycles) using the process as described

before. After post metallization annealing (PMA) at 300 °C in a forming gas (95% N_2/5% H_2) ambient for 5 min, C-V measurement was performed at room temperature (295 K) from 1 kHz to 1 MHz (total 31 scans). The results are shown in Figure 3.7.

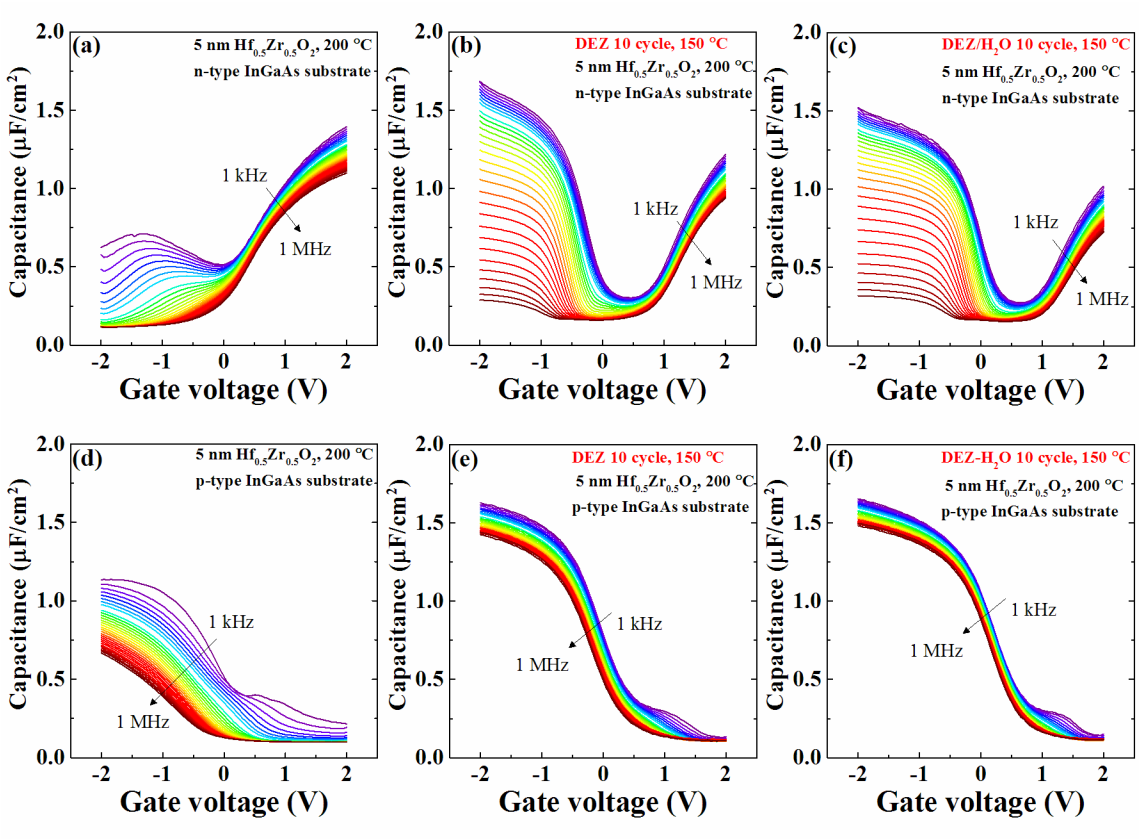


Figure 3.7. C-V frequency dispersion (from 1 kHz to 1 MHz) characteristics for $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples (a, d) without and with interface passivation by (b, e) in situ ALD DEZ and (c, f) ALD DEZ/H_2O surface treatment.

First, on n-type $In_{0.53}Ga_{0.47}As$ substrate, remarkable inversion-like behavior is shown at the negative voltage region of the C-V curves (depletion or weak inversion region for n-type substrate) for either (b) 10 cycles of DEZ or (c) 10 cycles of DEZ/H_2O treated sample. Whereas for sample (a) without ALD interface passivation, the C-V curves show a pronounced frequency dispersion

with a "hump-like" feature. Second, on p-type $In_{0.53}Ga_{0.47}As$ substrate, the frequency dispersion at the negative voltage region (accumulation region) is greatly reduced and the C_{max} at a gate voltage of -2 V significantly increases. Furthermore, the C-V curves are steeper (less stretch-out) during transition from depletion region to accumulation region both on p-type and n-type substrate. The inversion-like behavior on n-type substrate, the reduced accumulation frequency dispersion on p-type substrate, and the steeper C-V curves all suggest that the D_{it} near the mid-gap and valance band edge is reduced, and the unpinned Fermi level can move from the mid-gap to the valance band edge of $In_{0.53}Ga_{0.47}As$. The inversion-like behavior n-type substrate should be due to the minority carrier (hole) response.

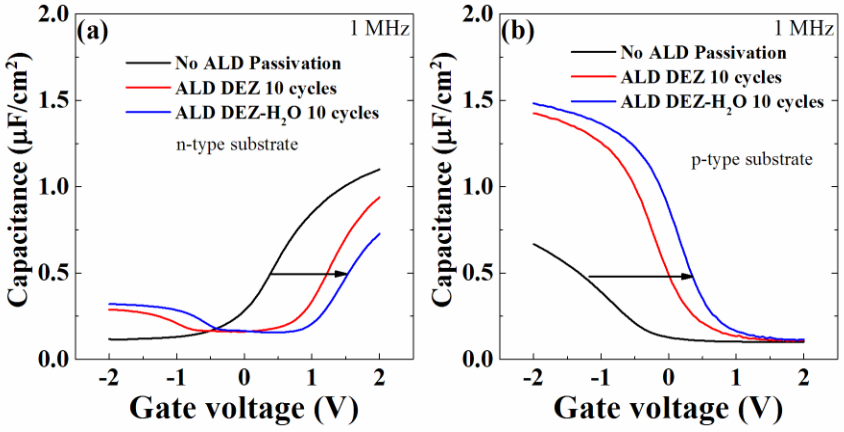


Figure 3.8. Comparison of C-V curves at 1 MHz for $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples on (a) n-type substrate (b) p-type substrate, without and with interface passivation by in situ ALD DEZ and ALD DEZ/H_2O surface treatment.

The high frequency (1 MHz) C-V curves are shown in Figure 3.8. Compared to the sample without ALD passivation, a positive shift is clearly observed for samples with ALD DEZ or DEZ/H_2O interface passivation. The exact reason for this phenomenon is still not clear. It may

relate to a reduction of positively charged traps that shifted the flat band voltage. Additionally, it has been suggested that a Si or Ge IPL may unintentionally incorporate n-type dopants that can change the surface doping concentration (e.g., counter dope p-$In_xGa_{1-x}As$) [93]. If it is true, the p-type doping effect of Zn on $In_{0.53}Ga_{0.47}As$ also seems to be plausible.

Table 3.5. Summary of the representative dopants of $In_{0.53}Ga_{0.47}As$ and the corresponding ionization energy [94].

Element	Dopant type	Ionization Energy (meV)
Si	n	~5
Ge	n	~5
Sn	n	~5
Zn	p	~20
Mg	p	~25
Be	p	~25

The representative dopants of $In_{0.53}Ga_{0.47}As$ and the corresponding ionization energy are summarized in Table 3.5. Si, Ge, and Sn are shallow donors of $In_{0.53}Ga_{0.47}As$ with an ionization energy ~5 meV. In contrast, Zn, Mg, and Be are shallow acceptors of $In_{0.53}Ga_{0.47}As$ with an ionization energy ~20−25 meV. In fact, the ionization energy of these dopants not high compared to the room temperature thermal energy 25.9 meV at 300 K and the ionization energies of shallow impurities in silicon [9]. From this perspective, the ALD DEZ treatment can potentially incorporate p-type dopant Zn via ALD surface reactions, resulting in counter doping the surface of the n-type

$In_{0.53}Ga_{0.47}As$ substrate. Therefore, an ultra-thin counter doping layer (CDL) can be formed. If CDL is completed inverted to p-type, a thin p-n junction is obtained. This structure is an analogy of the buried channel Si MOS structure with inverted surface doping [95].

In fact, ALD DEZ interface passivation only employs the first half cycle reaction of standard ALD ZnO process, without exposing H_2O as co-reactant. Owing to the self-limiting surface chemical reactions, the growth per cycle (GPC) of ALD film does not directly depend on the exposure of precursors once the process takes place in a saturated growth regime. However, the initial reactions on $NH_4OH/(NH_4)_2S$ treated InGaAs surface may rely on the exposure of DEZ due to the complex surface termination and unwanted incubation period. Therefore, the following experiments were designed to study the incubation and saturation behavior of DEZ exposure by analyzing the C-V characteristics.

Table 3.6. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples with 0, 10, 50, and 100 cycles of in situ ALD DEZ interface passivation.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 0 cycle	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(c)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 50 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(d)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 100 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$

As shown in Table 3.6, four $NH_4OH/(NH_4)_2S$ treated n-type $In_{0.53}Ga_{0.47}As$ samples with (a) 0 cycle, (b) 10 cycles, (c) 50 cycles, and (d) 100 cycles of in situ ALD DEZ interface passivation

were studied. Figure 3.9 and Figure 3.10 show that there is no significant difference in the C-V characteristics among the three ALD DEZ treated samples (b-d). This suggests that, by taking the use of first half-cycle reaction in ALD ZnO process, ALD DEZ passivation exhibits a nearly saturated behavior regardless of the number of DEZ cycle ranging from 10 cycles to 100 cycles.

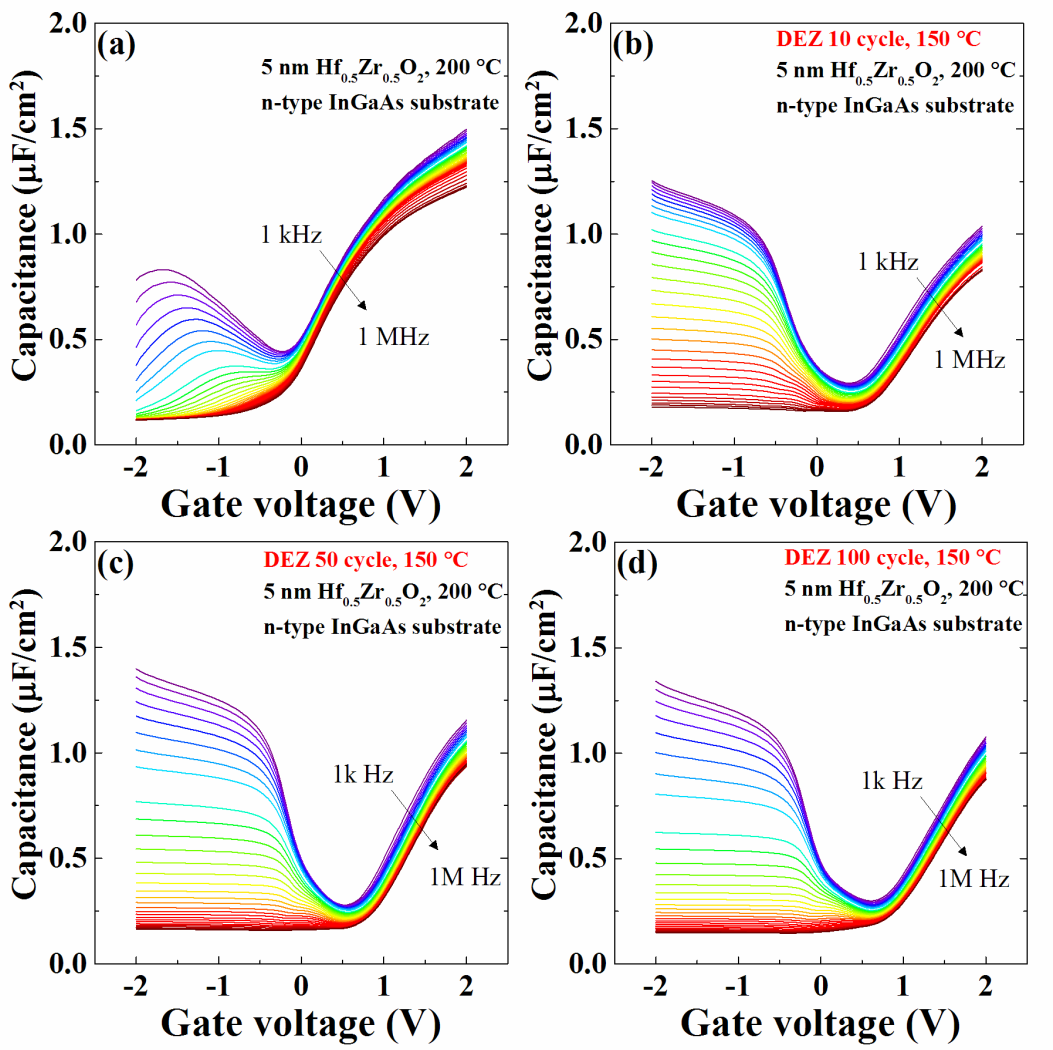


Figure 3.9. C-V frequency dispersion (from 1 kHz to 1 MHz) characteristics for $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples on n-type substrate with (a) 0 cycle, (b) 10 cycles, (c) 50 cycles, and (d) 100 cycles of in situ ALD DEZ interface passivation.

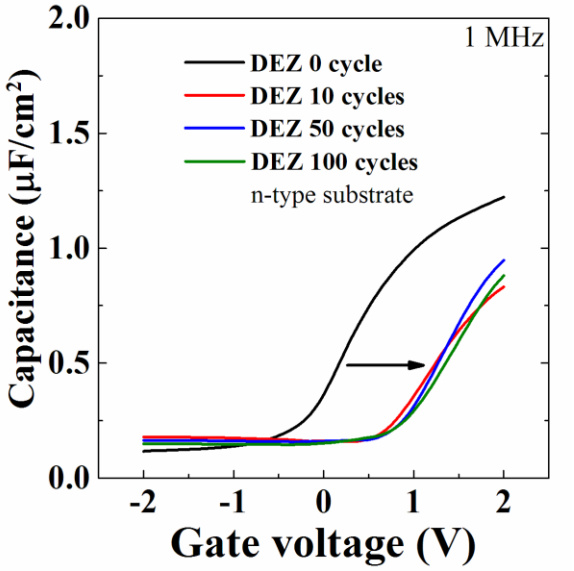


Figure 3.10. Comparison of C-V curves at 1 MHz for $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples on n-type substrate with 0 cycle, 10 cycles, 50 cycles, and 100 cycles of in situ ALD DEZ interface passivation.

Table 3.7. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples with 0, 1, 2, 10, and 20 cycles of in situ ALD DEZ interface passivation.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 0 cycle	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 1 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(c)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 2 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(d)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(e)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 20 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$

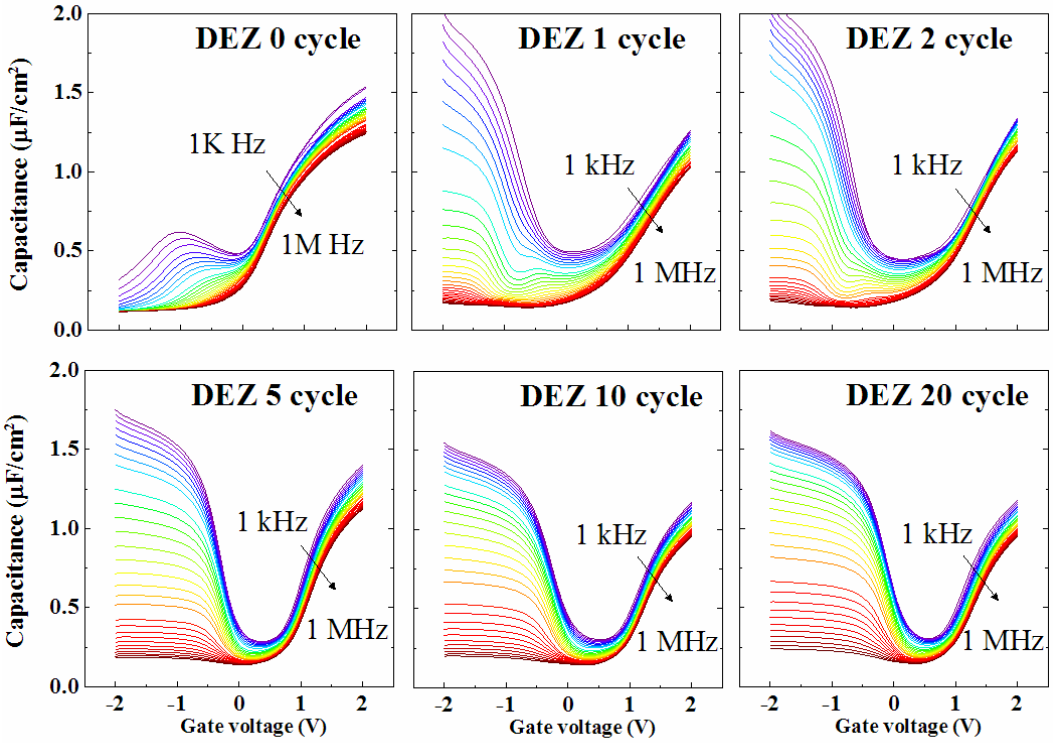


Figure 3.11. C-V frequency dispersion characteristics (from 1 kHz to 1 MHz) for n-type $In_{0.53}Ga_{0.47}As$ MOSCAP with 5 nm $Hf_{0.5}Zr_{0.5}O_2$ as a function of the cycle number of in situ ALD DEZ treatment. Measurements were done at room temperature 295 K.

To further understand the evolvement of C-V characteristics with increasing the number of ALD DEZ cycle, we studied MOSCAPs on $NH_4OH/(NH_4)_2S$ treated n-type $In_{0.53}Ga_{0.47}As$ substrate with 0, 1, 2, 5, 10, and 20 cycles of DEZ pulse, as listed in the Table 3.7. In addition to the standard measurements at room temperature (295 K), to freeze out the trap response, low-temperature (100 K) electrical measurements using a cryogenic probe station were also performed.

Figure 3.11 shows the C-V characteristics measured at room temperature. With only 1 cycle or 2 cycles of DEZ exposure, the inversion-like feature starts to appear at the negative voltage region, even though small hump-like feature can be still distinguishable between 0 V and -1 V gate

voltage. With 5 cycles of DEZ exposure, the C-V characteristics are quite similar to that of samples with 10 cycles or 20 cycles of DEZ exposure. This suggests that an incubation period exists in the initial surface reactions, and the passivation of high-k/InGaAs interface needs a few cycles (5 or more) of DEZ exposure to take full effect.

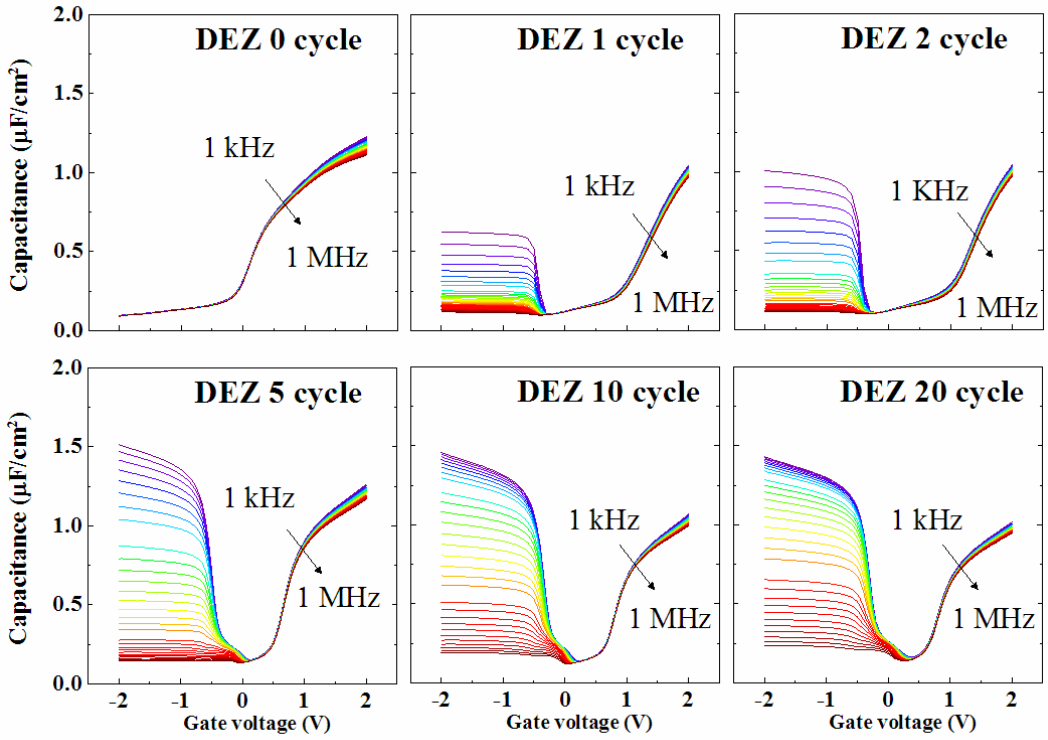


Figure 3.12. C-V frequency dispersion characteristics (from 1 kHz to 1 MHz) for n-type $In_{0.53}Ga_{0.47}As$ MOSCAP with 5 nm $Hf_{0.5}Zr_{0.5}O_2$ as a function of the cycle number of in situ ALD DEZ treatment. Measurements were done at low temperature 100 K.

When it comes to the C-V characteristics measured at low temperature (100 K), the contribution of C_{it} to the total capacitance is minimal. As shown in Figure 3.12, for samples (a) without ALD DEZ passivation, the hump-like feature disappears and the frequency dispersion is reduced. In contrast, for samples (b) with only 1 cycle of DEZ exposure, the inversion-like feature

does not disappear. With an exposure of DEZ up to 5 cycles, the inversion capacitance gradually increases to maximum. Furthermore, the threshold of the appearance of inversion capacitance starts at a higher frequency, which indicates the slightly change of time constant for minority carrier (hole) response. Although it seems that more than 5 cycles of DEZ treatment is required in this experiment, it is possible that a less number of cycle may also work if the exposure time (e.g., 1 s) is longer or the dosage (Torr·s) is larger in each DEZ treatment cycle.

As suggested in the previous in situ XPS half cycle study using DEZ/H_2O treatment by Lucero et al. [90, 91], the reduction of oxidation state on the surface by DEZ exposure is not significant, indicating that the inversion-like response was not simply due to the reduction of oxidization states. Zn2p XPS signal suggested that Zn incorporation immediately occurred at the first DEZ pulse and more Zn was incorporated at the tenth DEZ pulse. Therefore, the interface passivation is more likely concurrent with the Zn incorporation, either by forming the ZnO/ZnS IPL or counter doping n-type $In_{0.53}Ga_{0.47}As$ surface by p-type dopant Zn.

Table 3.8. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples with 10 cycles of in situ ALD DEZ treatment and ~3 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulator.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 10 cycles	~3 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	p	1 min/20 min	DEZ 10 cycles	~3 nm $Hf_{0.5}Zr_{0.5}O_2$

To obtain a smaller EOT (or capacitance equivalent thickness, CET), the gate insulator thickness was scaled down from ~5 nm to ~3 nm using 15 super-cycles of ALD $Hf_{0.5}Zr_{0.5}O_2$ process. As shown in Table 3.8, MOSCAP samples were fabricated both on n-type and p-type

substrate with 10 cycles of DEZ treatment. As shown in Figure 3.13, the C-V characteristics are similar to the standard samples with ~5 nm ALD $Hf_{0.5}Zr_{0.5}O_2$, while the curves are steeper because of a smaller gate insulator thickness. For p-type substrate, the maximum capacitance density (C_{max}) at 100 kHz in the C-V curves is 1.5 μF/cm^2, the corresponding to a CET of 2.3 nm. If we assume the dielectric constant for ALD-$Hf_{0.5}Zr_{0.5}O_2$ is similar to that of ALD-HfO_2 (~17) and t_{ox} is 3 nm, then the C_{ox} is estimated to be 5 μF/cm^2. A much lower C_{max} than the capacitance of gate dielectric (C_{ox}) was suggested due to the low effective density of states (DOS) in the conduction band of $In_{0.53}Ga_{0.47}As$ [96], quantum-mechanical correction, charge quantization effect [97], as well as the presence of a low-κ interfacial layer. To calculate the EOT (EOT=CET-$EOT_{correction}$) of high-k/$In_{0.53}Ga_{0.47}As$/InP system, $EOT_{correction}$ (~0.8 nm) needs to be considered [97, 98].

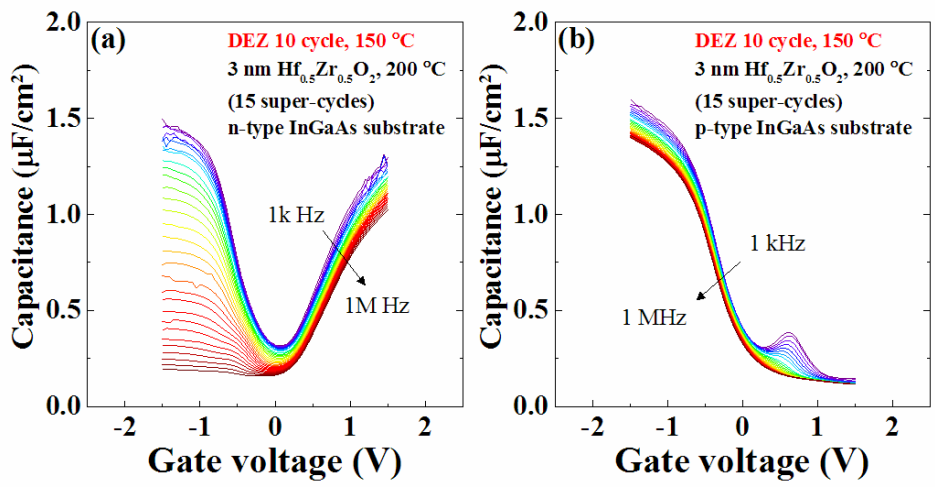


Figure 3.13. C-V frequency dispersion (from 1 kHz to 1 MHz) characteristics for (a) n-type and (b) p-type $In_{0.53}Ga_{0.47}As$ MOSCAP with 10 cycles of in situ ALD DEZ treatment and ~3 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulator.

Figure 3.14 shows the C-V double-sweep hysteresis characteristics (100 kHz) of ~3 nm ALD $Hf_{0.5}Zr_{0.5}O_2$ on p-type substrate MOSCAP samples at different maximum measurement

voltage (0.5 V, 0.8V, and 1.0V). The extracted hysteresis value is shown as a function of the maximum measurement voltage. The samples exhibit a small hysteresis of below 50 mV at a maximum voltage of 1.0 V. However, further scaling down the gate insulator thickness to ~ 2 nm using 10 super-cycles of ALD $Hf_{0.5}Zr_{0.5}O_2$ process was not successful because of a high gate leakage current. The actual film thickness may be thinner than 2 nm because that the growth of $Hf_{0.5}Zr_{0.5}O_2$ on InGaAs may need a few cycles period for nucleation to form a continuous film.

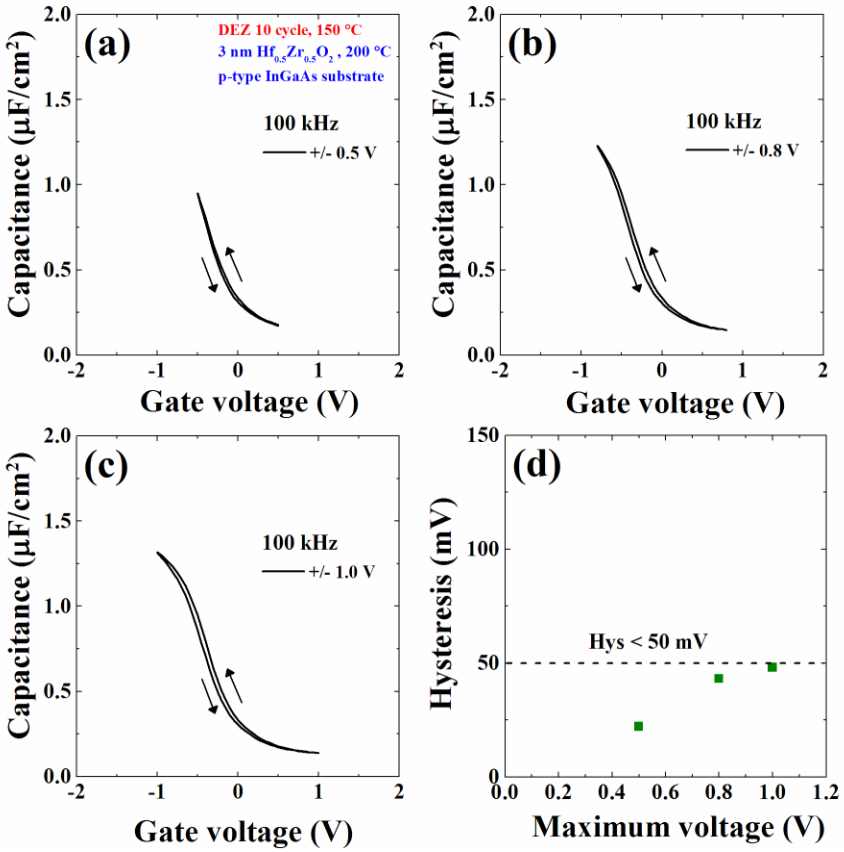


Figure 3.14. C-V hysteresis characteristics of p-type $In_{0.53}Ga_{0.47}As$ MOSCAP with 10 cycles of in situ ALD DEZ treatment and ~3 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulator as a function of the maximum measurement voltage (a) 1.0 V, (b) 1.5 V, (c) 2.0 V, and (d) the corresponding hysteresis.

To understand the passivation mechanism of Zn on high-k/InGaAs interface, Dr. Young Jun Oh in UTD did first-principle calculation using density functional theory (DFT). A shown in Figure 3.15 (a), due to the presence of a gallium vacancy (V_{Ga}), two As dangling bonds (DBs) exist on the HfO_2/InGaAs interface. In contrast, as shown in Figure 3.15 (b), a Zn atom occupy the V_{Ga} and is bonded with the As dangling bonds. The passivation of As dangling bonds by Zn is predicted to effectively reduce the trap states near the valence band edge of InGaAs, as shown in Figure 3.15 (c). This prediction is also consistent with the report that As dangling bonds can introduce gap states close to the valence band edge of GaAs and InAs [10].

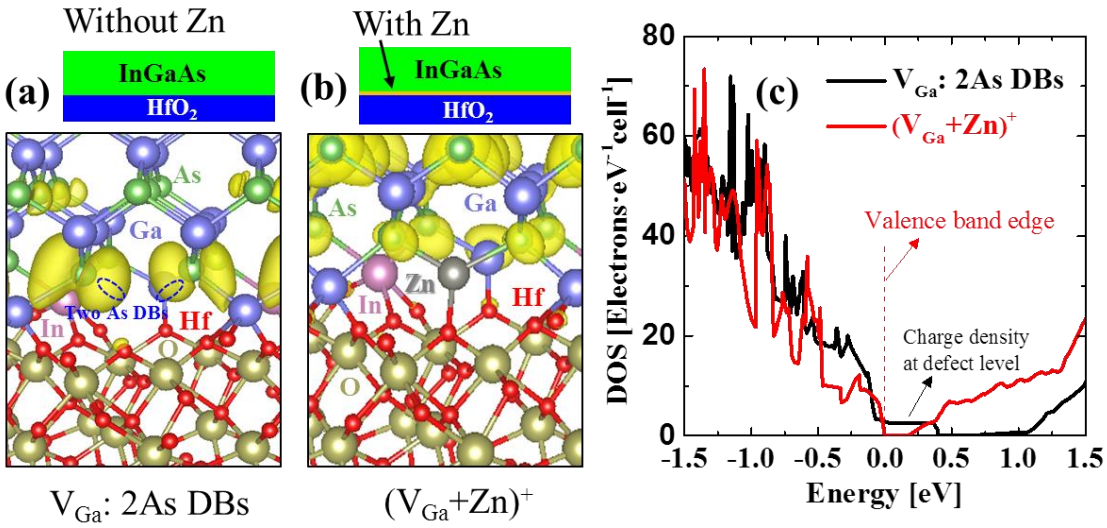


Figure 3.15. First-principle calculation using DFT in the case of (a) without a Zn atom, (b) with a Zn atom to passivate two As dangling bonds generated by Ga vacancy at the HfO_2/InGaAs interface, and (c) the corresponding density of states for each cases.

3.4 Alternative ALD-based Interface Passivation on $In_{0.53}Ga_{0.47}As$

This subsection describes two alternative ALD-based interface passivation techniques explored in this work. As discussed previously, Zn is a p-type dopant of $In_{0.53}Ga_{0.47}As$. In fact, Mg

is also a p-type shallow dopant of $In_{0.53}Ga_{0.47}As$. Surface treatment with a magnesium-containing ALD precursor will be interesting to compare with DEZ treatment. Burton et al. reported that MgO can be grown by ALD using Bis(ethylcyclopentadienyl)magnesium ($Mg(CpEt)_2$) and H_2O at a temperature between 125 °C and 400 °C [99]. Therefore, like the ALD DEZ treatment study, MOSCAPs with different $Mg(CpEt)_2$ treatment conditions were prepared, as show in Table 3.9.

Table 3.9. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples without and with 10, 100 cycles of in situ ALD-$Mg(CpEt)_2$ treatment at either 150 °C or 200 °C.

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-$Mg(CpEt)_2$	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	No	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	10 cycles, 150 °C	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(c)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	100 cycles, 150 °C	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(d)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	10 cycles, 200 °C	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(e)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	100 cycles, 200 °C	5 nm $Hf_{0.5}Zr_{0.5}O_2$

Figure 3.16 shows the room temperature C-V characteristics of these samples. Compared to the sample without with $Mg(CpEt)_2$ treatment, smaller frequency dispersion can be observed for the samples with $Mg(CpEt)_2$ treatment, regardless the temperature (150 °C or 200 °C) and the number of cycles (10 cycles or 100 cycles). Overall, the samples (b) and (c) treated at 150 °C shows slightly better performance than the samples (d) and (e) treated at 200 °C. However, the presence of hump-like features suggests that ALD-$Mg(CpEt)_2$ treatment is not as effective as ALD DEZ treatment for interface passivation on high-k/$In_{0.53}Ga_{0.47}As$. This could be due to a low

reactivity of $Mg(CpEt)_2$ on $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ surface and the bulkiness of $Mg(CpEt)_2$ molecule which causes steric hindrance effect during the surface reactions.

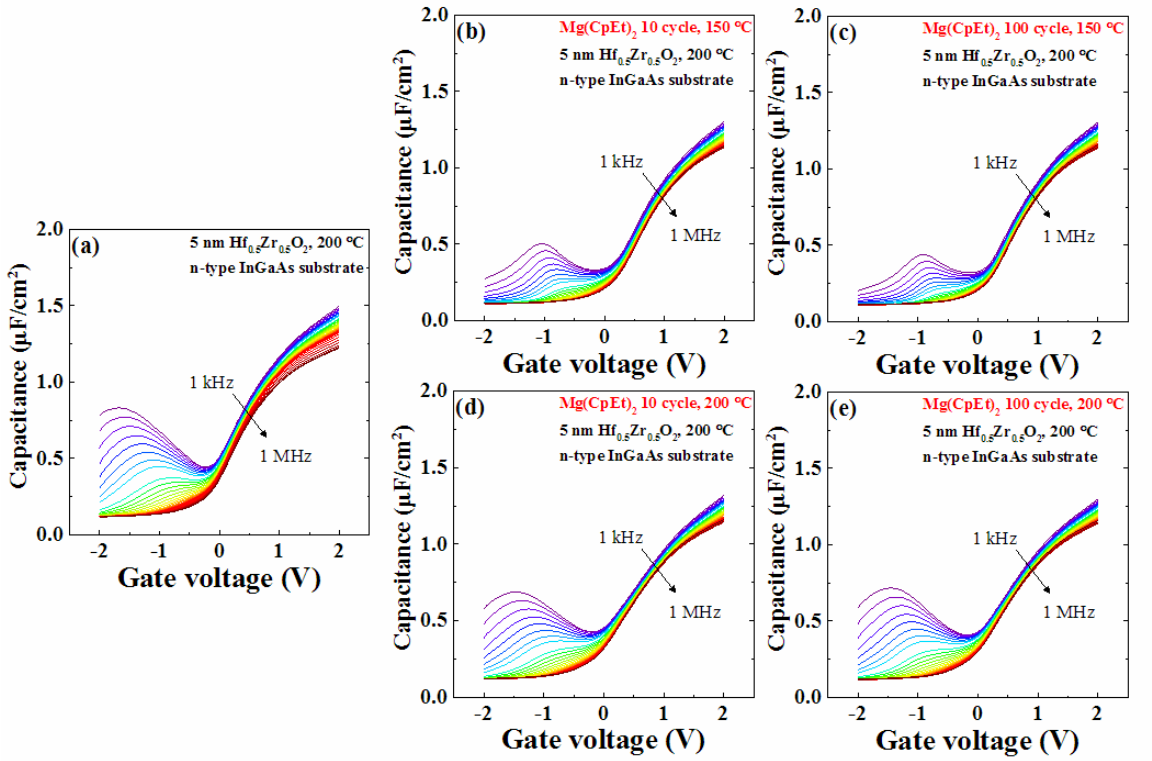


Figure 3.16. C-V frequency dispersion (from 1 kHz to 1 MHz) characteristics for $NH_4OH/(NH_4)_2S$ treated n-type $In_{0.53}Ga_{0.47}As$ MOSCAP samples (a) without and (b-e) with 10, 100 cycles of in situ ALD-$Mg(CpEt)_2$ treatment at either 150 °C or 200 °C.

Another passivation technique studied in this work utilized an ex situ PEALD-AlN interlayer grown in a hollow-cathode PEALD reactor. Nitrogen (N) and arsenic (As) are both in column V of the element periodic table and have five valence electrons. N has a smaller atomic radius than As. The smaller-sized N atoms can substitute As, occupy anion vacancies (e.g., N_{As}) or be bonded to Ga/In/As dangling bonds (DBs) on the $In_xGa_{1-x}As$ surface. Consequently, a nitrogen-passivated surface composed of Ga-N, In-N, As-N, or N DBs can be constructed. F.

Capasso et al. proposed a nitrogen-passivation technique on GaAs, $In_xGa_{1-x}As$ and the other III-V semiconductor devices [100]. The basic concept is removing As oxide, elemental As and In oxide from the surface via hydrogen plasma treatment, as well as growing ultrathin GaN/InN surface passivation layer via nitrogen plasma treatment. Using this passivation technique, A. Callegari et al. demonstrated unpinned Ga_2O_3/GaAs interface with a low D_{it} ~10^{11} $eV^{-1}cm^{-2}$ [101]. Keeping pace with the unceasing attempts to obtain high-performance III-V semiconductor MOSCAPs/MOSFETs, the interest in nitrogen surface passivation (plasma or thermal) continues. Particularly, in combined with some new techniques such as ALD, nitrogen-passivated high-k/III-V interface has demonstrated a low interface trap density (D_{it} <10^{12} $eV^{-1}cm^{-2}$) [96, 102-107].

It has been reported that high-purity crystalline AlN and GaN films could be grown at low temperatures in a modified commercial PEALD reactor with a hollow cathode plasma source [108]. In contrast, by using an ICP plasma source, the deposited films had a much higher O impurity content because of the oxygen contamination from the ICP plasma source. Since the reactive oxygen species in the nitrogen plasma could unintentionally induce the growth of detrimental interfacial oxides, the previous reports using an ICP plasma ALD system might underestimate the benefits of nitrogen-passivation [96, 104]. It will be of great interest to study nitrogen-passivation on $In_xGa_{1-x}As$ using hollow cathode PEALD reactor. Compared to conventional CCP or ICP plasma source, the advantages of this hollow cathode plasma source (Meaglow) include high plasma density, improved film crystallinity, low damage (remote plasma), and low oxygen contamination. TMA and nitrogen containing plasma (NH_3 or 10% H_2 balanced N_2) were used for AlN process development. Argon (Ar) was used as carrier gas during the process.

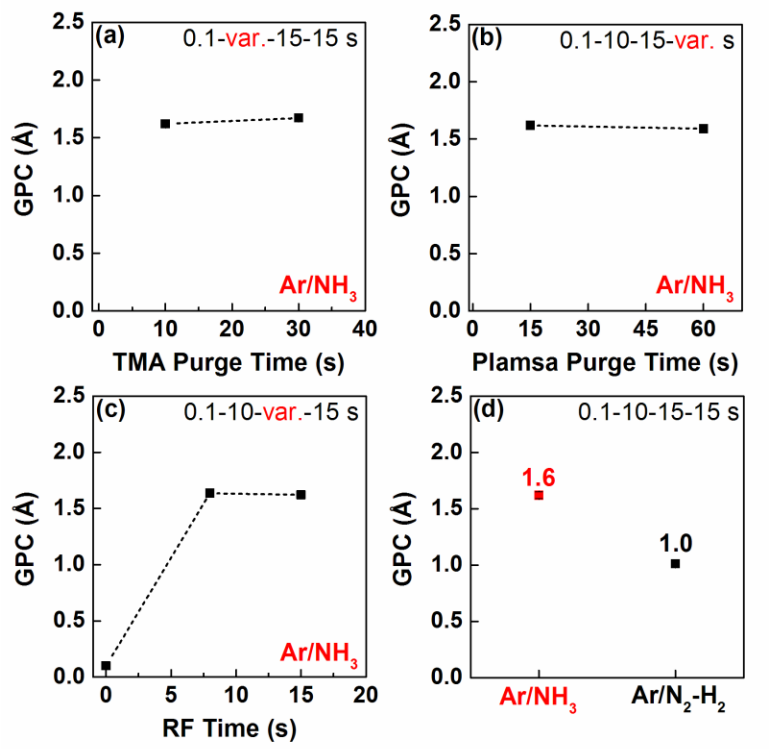


Figure 3.17. Growth per cycle (GPC, Å) of hollow cathode PEALD-AlN grown at 250 °C as a function of (a) TMA purge time (b) plasma purge time (c) RF time and (d) plasma gas.

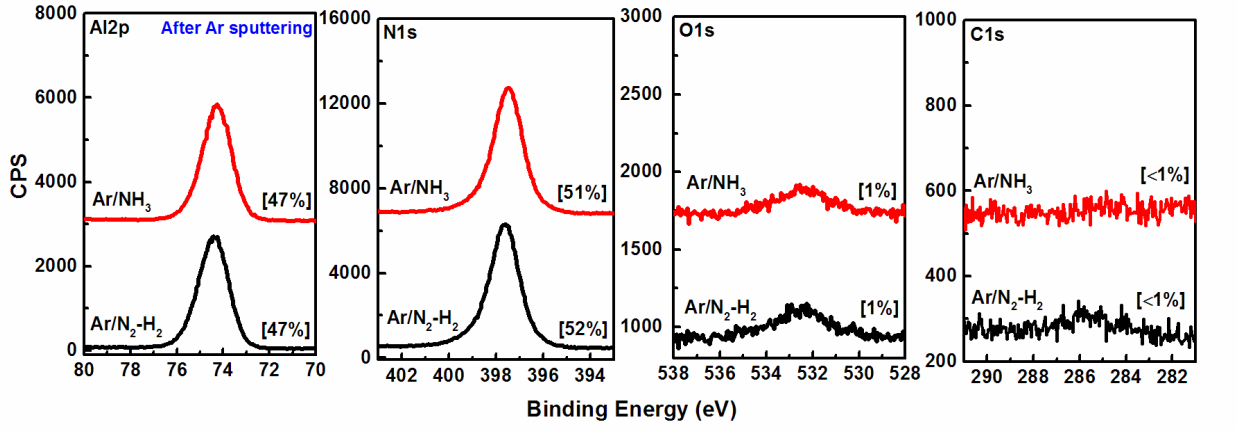


Figure 3.18. XPS spectra of hollow cathode PEALD-AlN grown at 250 °C using Ar/NH_3 plasma or Ar/N_2-H_2 (10%) plasma. Calculated atomic composition of each element is also provided.

As shown in Figure 3.17, the GPC is independent of the TMA purge time and plasma purge time, suggesting a sufficient purge time of the precursor and the plasma. Furthermore, the GPC saturates at ~1.6 Å with 8 s plasma RF time. Compared to AlN grown using Ar/N_2-H_2 plasma (GPC~1 Å), AlN grown using Ar/NH_3 plasma shows a higher GPC (~1.6 Å). According to the ex situ XPS analysis of the AlN films in Figure 3.18, both samples shows a low oxygen content [O] of ~1 at.% and carbon content [C] of ~1 at.%, close to the detection limit of XPS. The ratio of [Al]/[N] is approximately 0.92:1.

As shown in Table 3.10, two samples with ex situ grown ~3 nm hollow cathode PEALD-AlN (10 cycles, 0.1-10-8-15 s, 250 °C) interlayer were fabricated on n-type and p-type $In_{0.53}Ga_{0.47}As$ substrate. Prior to loading into PEALD reactor, the samples were performed with $NH_4OH/(NH_4)_2S$ treatment. Additionally, 4 nm $Hf_{0.5}Zr_{0.5}O_2$ (20 super-cycles, 200 °C) was grown on top of AlN interlayer.

Table 3.10. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAP samples using ex situ grown ~3 nm hollow cathode PEALD-AlN interlayer on (a) n-type and (b) p-type substrate.

Sample	Substrate	Type	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	PEALD-AlN 10 cycles	4 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	p	PEALD-AlN 10 cycles	4 nm $Hf_{0.5}Zr_{0.5}O_2$

As shown in Figure 3.19 (a), near the accumulation region (positive voltage) of n-type MOSCAP, the frequency dispersion is suppressed. However, near the depletion or weak inversion region (negative voltage) of n-type MOSCAP, the C-V curves are completely stretched out,

suggesting the pinning of Fermi level. Consistently, as shown in Figure 3.19 (b), near the accumulation region (negative voltage) of p-type MOSCAP, the frequency dispersion is pronounced. In contrast, inversion-like feature occurs near the weak inversion region (positive voltage) of p-type MOSCAP. The results suggest the D_{it} near the mid-gap and the valance band edge of $In_{0.53}Ga_{0.47}As$ is still high while the D_{it} near the conduction band edge of $In_{0.53}Ga_{0.47}As$ is greatly reduced. This result shows that the hollow cathode PEALD-AlN interlayer only passivates the defects near the conduction band edge, while introducing additional traps near the mid gap and valence band edge.

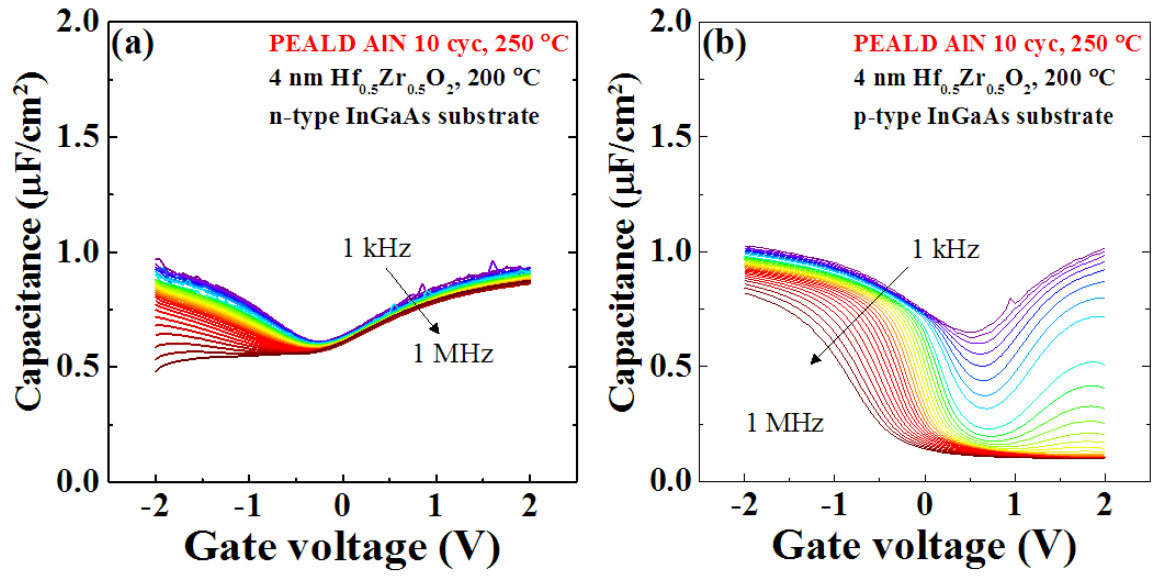


Figure 3.19. C-V frequency-dispersion (from 1 kHz to 1 MHz) characteristics for $In_{0.53}Ga_{0.47}As$ MOSCAP samples using ex situ grown ~3 nm hollow cathode PEALD-AlN interlayer on (a) n-type and (b) p-type substrate.

3.5 Inversion-Type Enhancement-Mode n-channel and p-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using in situ ALD DEZ-Based Interface Passivation Techniques

3.5.1 Introduction

The ultimate application of ALD-based IPL and high-k gate dielectric stacks on $In_{0.53}Ga_{0.47}As$ is to fabricate metal-oxide-semiconductor field effect transistors (MOSFETs). Unlike MOSCAPs, which typically have gate dielectric stacks grown on freshly cleaned blank substrates, MOSFETs have more complicated fabrication process flow. There are commonly two process integration options to make $In_{0.53}Ga_{0.47}As$ MOSFETs: (a) gate-first process and (b) gate-last process. The use of terminology 'first' or 'last' depends on whether the metal gate electrode is deposited before or after the high temperature activation annealing of the source/drain dopants.

As shown in Figure 3.20, the gate-first process flow starts with the growth of gate dielectric stacks on freshly cleaned blank substrate, followed by the metal gate deposition. Then, the dopants are implanted in the source/drain well regions while the gate region is physically blocked by the metal gate. Therefore, the implantation is done in a self-aligned fashion. To activate the dopants to form P/N junctions, high temperature (typically ≥ 600 °C) activation annealing is performed in a rapid thermal processing (RTP) or laser spike annealing (LSA) chamber in an inert ambient. Metal gate materials, such as Pd/Au in this work, do not allow such a high thermal budget. To solve this problem, a dummy gate or the so-called "replacement metal gate (RMG)" technique has been widely adopted in the Si CMOS high-k/metal gate platform. However, the poor thermal stability of $(NH_4)_2S$ treated surface remains an unsolved problem for gate-first $In_{0.53}Ga_{0.47}As$ MOSFETs process flow [109, 110]. Therefore, from the perspective of process integration, our

ALD DEZ-based interface passivation on $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ substrate is not compatible with the gate-first self-aligned process flow.

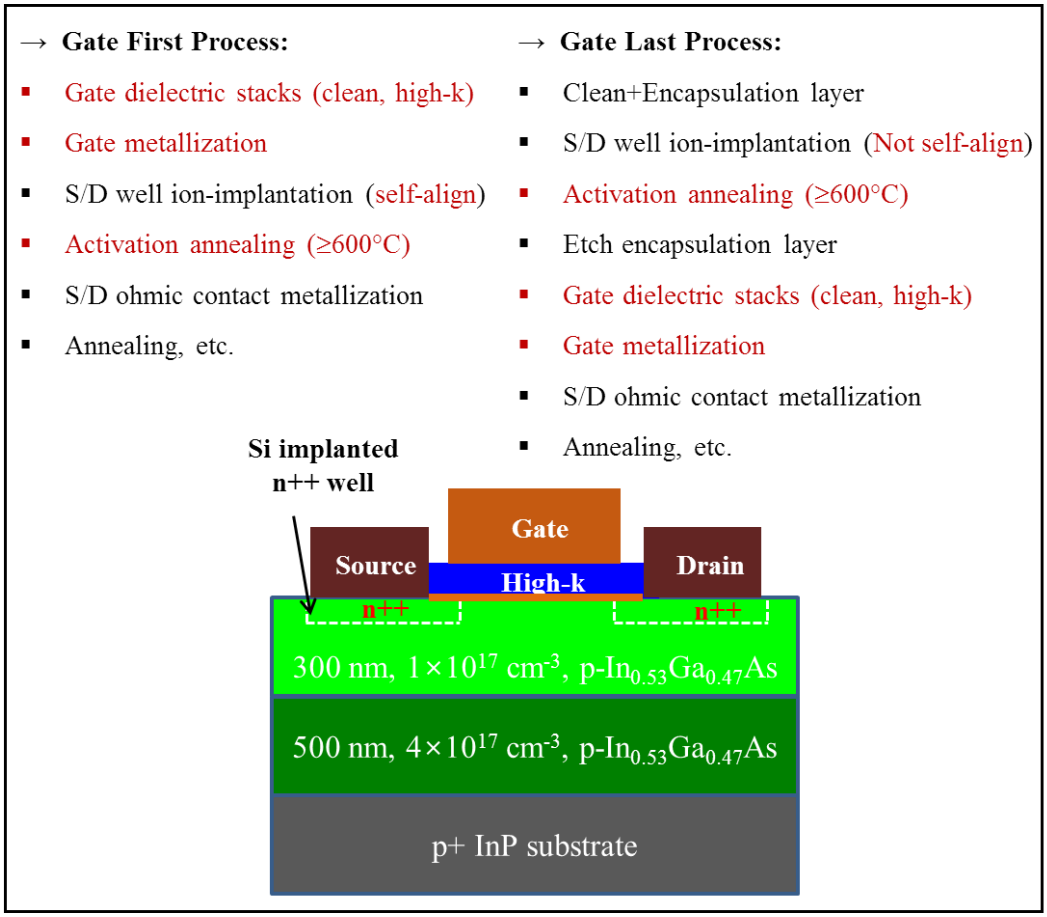


Figure 3.20. Basic flow of gate-first and gate-last process for high-k/metal gate based inversion-type n-channel MOSFETs fabrication.

In contrast, the gate-last process flow can avoid the high thermal budget for gate dielectric stacks and metal gate. As shown in Figure 3.20, the source/drain well implantation and activation annealing are performed at first on encapsulation layer protected blank substrate. Then, the gate dielectric stacks and metal gate are prepared without additional high temperature steps

subsequently. The main problem with gate-last process flow is the gate electrode is not self-aligned. Therefore, manual alignment and design of overlap margin to fully cover the channel (gate metal length L_G is slightly larger than channel length (L_{ch} or L_g, $L_G=L_g+2L_{overlap}$) are required. Additionally, since there are lithography, encapsulation layer deposition/etching, and activation annealing steps, the protection of $In_{0.53}Ga_{0.47}As$ surface from degradation prior to growing the gate dielectric stacks is also very critical and challenging.

3.5.2 Experimental

In this subsection, the development of $In_{0.53}Ga_{0.47}As$ MOSFETs using a gate-last process flow will be described. Inversion type of n-channel MOSFETs were fabricated using p-type $In_{0.53}Ga_{0.47}As$/InP substrates and inversion type of p-channel MOSFETs were fabricated using n-type $In_{0.53}Ga_{0.47}As$/InP substrates.

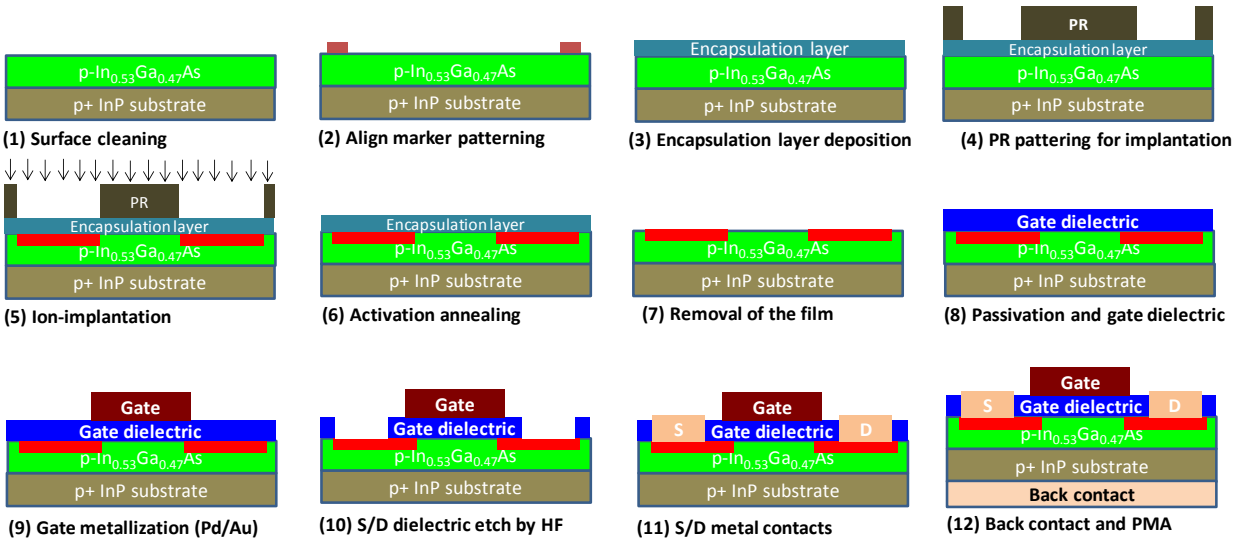


Figure 3.21. Schematic of n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs fabrication process flow.

The schematic of the baseline n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs fabrication process flow is illustrated in Figure 3.21. After the solvent cleaning by acetone/methanol/IPA, the sample was patterned with alignment marker by lifting off Ni/Au (20 nm/100 nm). PECVD SiO_2 encapsulation layer (250 °C, 30 s, ~30 nm) was deposited to protect the sample surface from damage during implantation. After the S/D implantation pattern was defined by photolithography (S1813, positive PR), a Si dose of 1×10^{14} ions/cm^2 (40 keV, tilt 7°) was selectively implanted through the 30 nm PECVD SiO_2 encapsulation layer. Activation annealing was done by rapid thermal annealing (RTA) at 600 °C for 1 min in an N_2 ambient. Encapsulation SiO_2 layer was removed by etching in 100:1 dilute HF for 5 min and N_2 dry. The relatively long etching time is ascribed to a lower wet etch rate of SiO_2 encapsulation layer densified during RTA. However, etching time should be carefully controlled since the InGaAs surface can be degraded in HF or buffered oxide etch (BOE) solution. Encapsulation layer removal was immediately followed by the same $NH_4OH/(NH_4)_2S$ cleaning step for MOSCAPs fabrication. High-k gate dielectric was grown in the Cambridge Nanotech S100 thermal ALD reactor.

Subsequently, a negative PR (NLOF 2020) was spin-coated and MOSFETs gate PR pattern was formed using Karl Suss MA6 BA6 contact aligner and AZ300 MIF developer (60 s) in the cleanroom. A Pd/Au (20 nm/100 nm) gate electrode was deposited using e-beam evaporator and patterned using a lift-off process. Then, a negative PR (NLOF 2020) was spin-coated and MOSFETs ohmic contact PR pattern was formed using Karl Suss MA6 BA6 contact aligner and AZ300 MIF developer (60 s). Dielectric at the ohmic contact regions was etched in 100:1 HF (e.g., 10 nm ALD Al_2O_3 for 30 s and 5 nm $H_{0.5}fZr_{0.5}O_2$ for 1 min 40 s−2 min) prior to S/D metallization. A Ni/Ge/Au (20 nm/20 nm/100 nm) ohmic metal stack was deposited using e-beam evaporator

and patterned using a lift-off process. The devices were not isolated with additional steps. The InP substrate backside was gently scratched by a diamond scribe and immediately loaded into e-beam evaporator for backside ohmic contact deposition (Ti/Au 20 nm/200 nm). Finally, the sample can be annealed in a rapid thermal processing (RTP) chamber at 300 °C in a forming gas (95% N_2/5% H_2) ambient for 5 min and ready for electrical characterization.

In the case of p-channel MOSFETs, the fabrication followed a similar process flow as described above. However, n-type $In_{0.53}Ga_{0.47}As$/InP substrates were used. A Be dose of 1×10^{14} ions/cm^2 (40 keV, tilt 7°) was implanted on the p^+ wells through a 30 nm PECVD SiO_2 encapsulation layer. Activation annealing was done by rapid thermal annealing (RTA) at 550 °C for 1 min in an N_2 ambient.

Figure 3.22 shows the camera and optical microscope image of the completed devices.

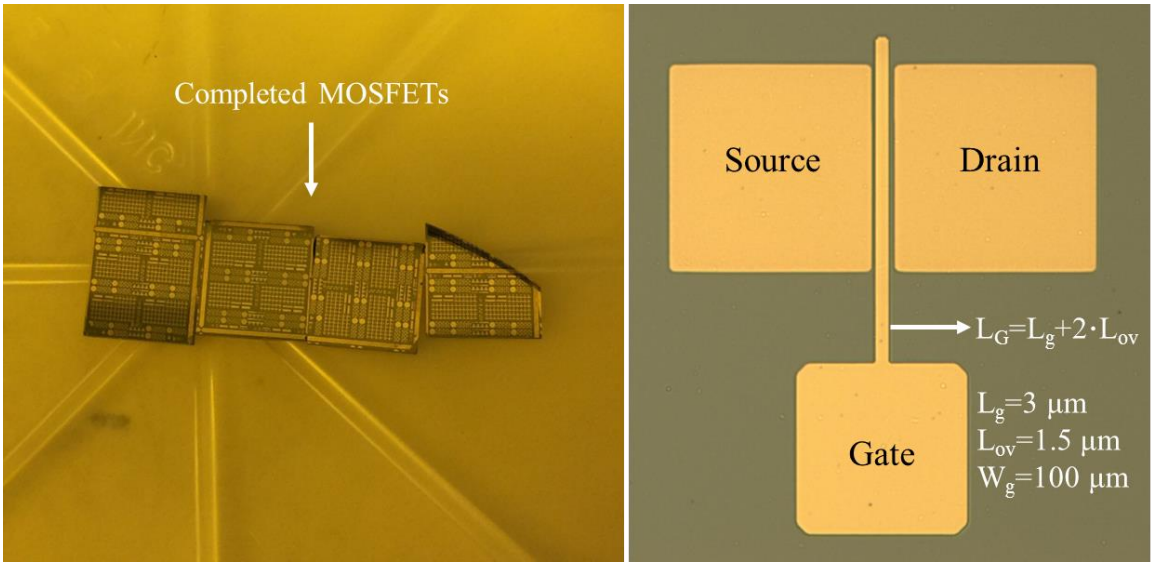


Figure 3.22. Camera and optical microscope image of the $In_{0.53}Ga_{0.47}As$ MOSFETs.

3.5.3 Results and Discussion

Figure 3.23 shows the TLM structure on the samples. To evaluate the ohmic contact using TLM structure, two samples with different activation annealing time (15 s and 60 s, 600 °C) were studied on p-type substrate for n-channel MOSFETs fabrication.

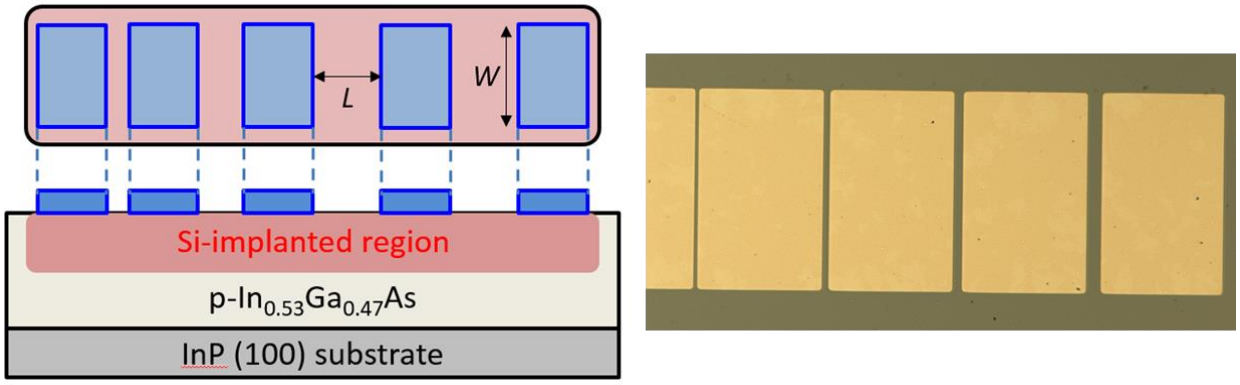


Figure 3.23. TLM structure on $In_{0.53}Ga_{0.47}As$ MOSFETs sample. Pad width (W) is 50 µm and distance (L) is 4 µm, 6 µm, 8 µm, 12 µm, respectively.

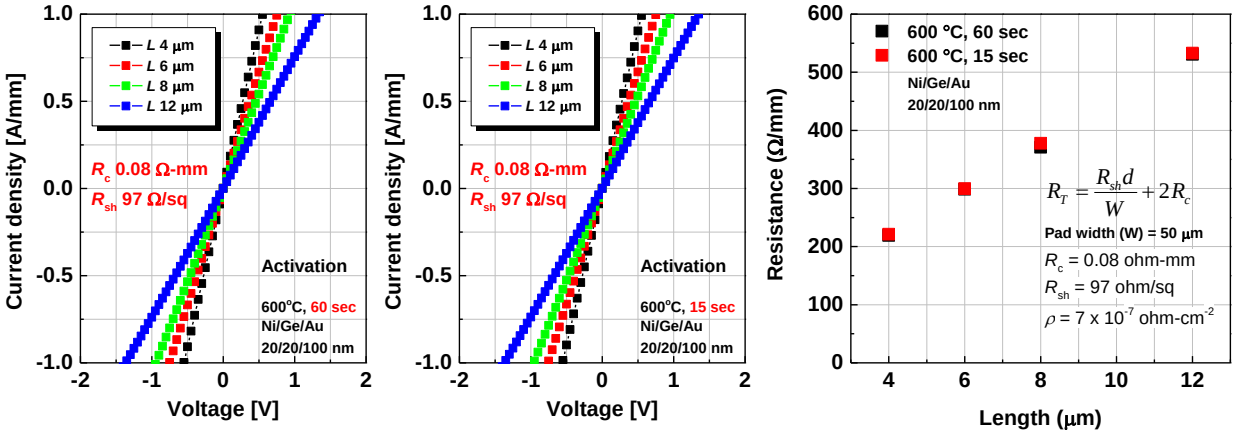


Figure 3.24. TLM results of n-channel MOSFETs with an activation annealing time of 15 s and 60 s at 600 °C in an N_2 ambient, respectively.

As shown in Figure 3.24, both samples exhibit linear I-V characteristics, without showing a rectifying Schottky contact behavior. They show comparable results: a low contact resistance (R_c) of 0.08 ohm·cm, a low sheet resistance (R_{sh}) of 97 ohm/sq, and a low specific contact resistivity (ρ_c) of 7×10^{-7} ohm·cm^2. This suggests that 15 s activation annealing time is enough to obtain a good ohmic contact.

For baseline process evaluation, $In_{0.53}Ga_{0.47}As$ n-channel MOSFETs with 10 nm ALD Al_2O_3 gate dielectric were fabricated. To grow Al_2O_3 gate dielectric on $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ samples, 10 cycles of in situ ALD TMA treatment (TMA/purge 0.03/10 s) was performed at a temperature of 200 °C, followed by Al_2O_3 growth at the same temperature (TMA/purge/H_2O/purge, 0.03/10/0.03/10 s, 100 cycles for ~10 nm).

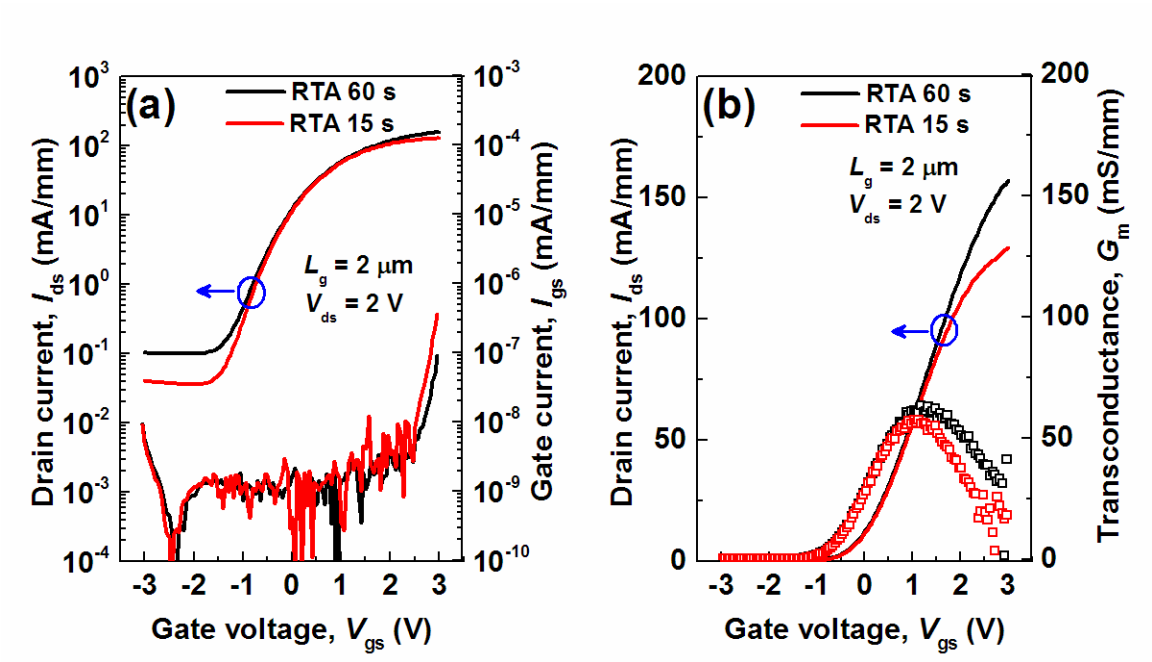


Figure 3.25. I_{ds}-V_{gs} transfer characteristics of n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with 10 nm Al_2O_3 gate dielectric, (a) log scale (b) linear scale.

The I_{ds}-V_{gs} transfer characteristics (log scale and linear scale) without PMA are shown in Figure 3.25. The channel length (L_g) is 2 µm and V_{ds} is 2 V. The sample with 60 s activation annealing shows a higher maximum drain current but a higher off-state drain current. The I_{ds} on/off ratio is approximate 10^3. The gate leakage current is comparable and much lower than off-state I_{ds}, indicating the S/D junction leakage current is dominant at off-state. The I_{ds}-V_{ds} output characteristics of 10 nm Al_2O_3 n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs are shown in Figure 3.26. The maximum I_{ds} of two samples are 173 mA/mm (RTA 60 s) and 136 mA/mm (RTA 15 s), respectively. The results suggest that the process flow is working well to fabricate MOSFETs.

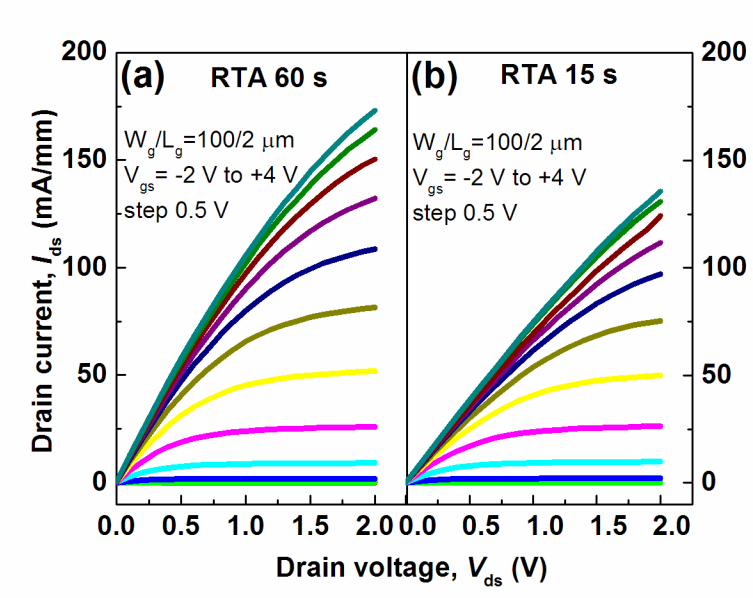


Figure 3.26. I_{ds}-V_{ds} output characteristics of n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with 10 nm Al_2O_3 gate dielectric, (a) RTA 60 s at 600 °C (b) RTA 15 s at 600 °C.

According to the results of MOSCAPs shown previously, ALD DEZ based interface passivation technique has been proved effective to reduce the D_{it} near the mid-gap and the edge of valance band of $In_{0.53}Ga_{0.47}As$. Minority carriers (holes) can be generated on n-type substrates

when the gate bias moves the fermi-level towards inversion region (negative bias). Also, a small frequency dispersion and a small hump-like feature can be obtained in the C-V curves of MOSCAPs on p-type substrates. However, it is still questionable whether this interface passivation technique will be effective on inversion-type of MOSFETs or not.

Figure 3.27 shows the electrical results an n-channel MOSFETs using 10 cycles of ALD DEZ treatment and 5 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulators. The devices are enhancement-mode with a positive threshold voltage (V_{th}) of ~2.2 V, high ON/OFF drain current ratio of 10^3–10^4, and subthreshold swing (SS) of ~280 mV/dec. PMA caused a positive shift of threshold voltage from ~1.3 V because of the reduction of positive fixed charge. Therefore, the ALD DEZ-based interface passivation can be integrated to MOSFETs fabrication.

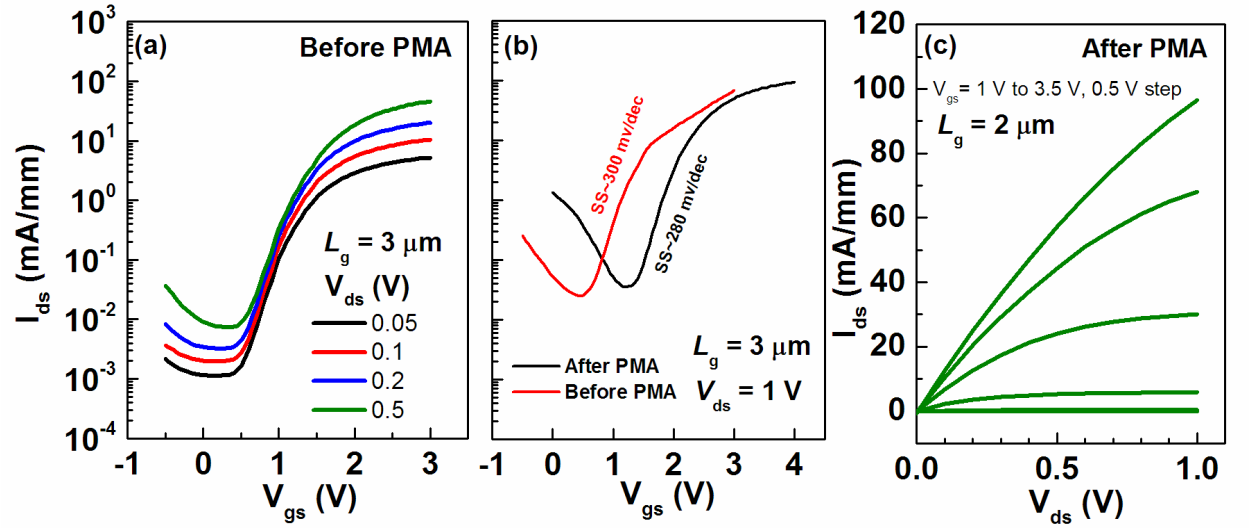


Figure 3.27. (a) (b) I_{ds}-V_{gs} transfer characteristics and (c) I_{ds}-V_{ds} output characteristics of n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs with 10 cycles of in situ ALD DEZ treatment and 5 nm $Hf_{0.5}Zr_{0.5}O_2$ gate insulator.

For n-channel $In_{0.53}Ga_{0.47}As$ MOSFET, there have been innumerable published papers available. However, except a few attempts using strained channel quantum well structure [111], the feasibility of $In_{0.53}Ga_{0.47}As$ inversion-type p-channel MOSFET fabrication on n-type substrate was seldom explored. Compared to its electron mobility (~10000 $cm^2/V \cdot s$), the hole mobility (~400 $cm^2/V \cdot s$) of $In_{0.53}Ga_{0.47}As$ is not considered attractive. Nevertheless, it is still comparable to the hole mobility of Si (~450 $cm^2/V \cdot s$). The realization of p-channel MOSFET can make $In_{0.53}Ga_{0.47}As$ CMOS possible.

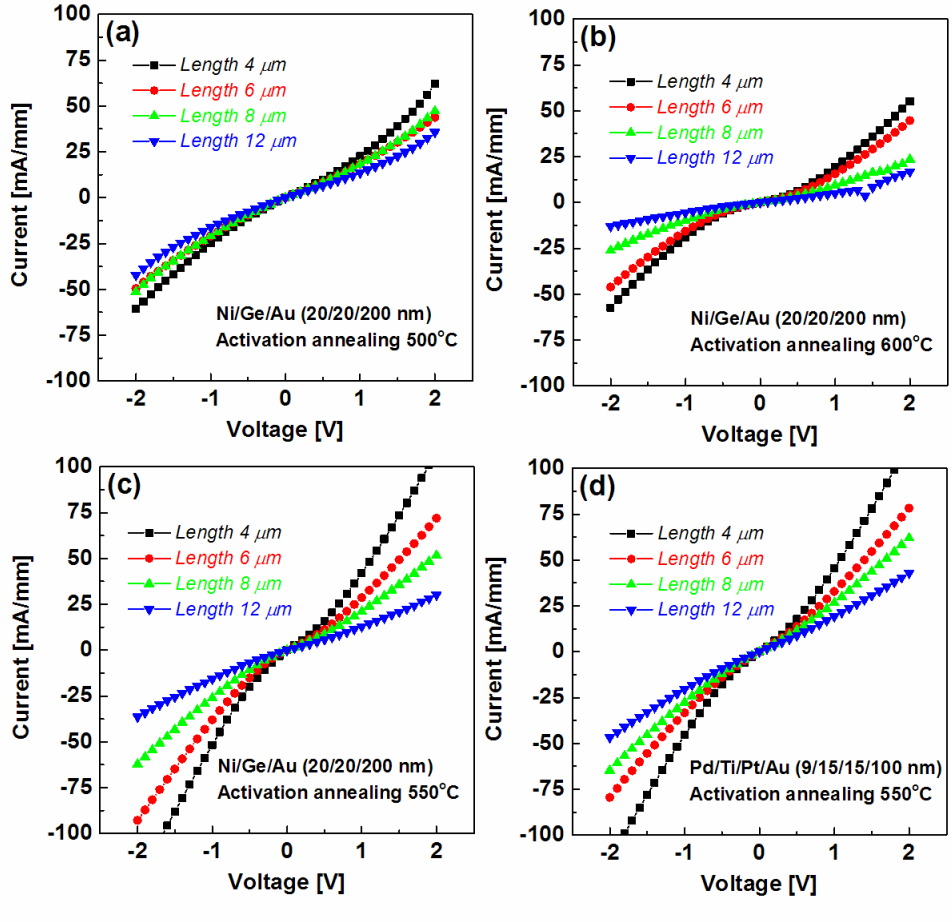


Figure 3.28. I-V characteristics of TLM structures on p-channel MOSFETs with an activation annealing time of 60 s in an N_2 ambient at (a) 500 °C, (b) 600 °C (c) 500 °C using Ni/Ge/Au stacks, and (d) at 550 °C using Pd/Ti/Pt/Au stacks, respectively.

First, the same metal stack (Ni/Ge/Au) was tested on the TLM structures of p-channel MOSFETs on n-type substrate. The activation annealing temperatures were 500 °C, 550 °C, and 600 °C, respectively. As shown in Figure 3.28, unlike the linear I-V characteristic shown in the TLM results of n-channel MOSFETs previously in Figure 3.24, the TLM results of p-channel MOSFETs show rectifying non-linear I-V characteristics. It has been reported that a low contact resistivity below 10^{-7} ohm·cm^2 was obtained on an n^+ and p^+ $In_xGa_{1-x}As$ substrate using Pd/Ti/Pt/Au (9/15/15/100 nm) non-alloyed metal stacks, respectively [112]. However, the alternative metal stack using Pd/Ti/Pt/Au showed similar results in Figure 3.28 (d). This suggests that the optimization should more focus on the implantation conditions and the activation annealing conditions. Nevertheless, it is still acceptable to investigate the efficacy of in situ ALD DEZ interface passivation on inversion-type p-channel MOSFETs. In this work, an annealing temperature of 550 °C was selected due to a better ohmic contact result.

Table 3.11. $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ p-channel MOSFETs samples (no PMA).

Sample	Substrate	Type	$NH_4OH/(NH_4)_2S$	ALD-Passivation	ALD-Insulator
(a)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	No	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(b)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$
(c)	$In_{0.53}Ga_{0.47}As$	n	1 min/20 min	DEZ/H_2O 10 cycles	5 nm $Hf_{0.5}Zr_{0.5}O_2$

As listed in Table 3.11, three p-channel MOSFET samples were fabricated without PMA. Figure 3.29 shows the I_{ds}-V_{gs} transfer characteristics. Sample (a) without ALD DEZ treatment does not show effective modulation of the drain current (I_{ds}) by the gate voltage (V_{gs}). This can be

directly correlated to the Fermi level pinning due to the high D_{it} without ALD DEZ treatment. The Fermi level pinning makes the band bending ineffective to form inversion layer as channel (minority carrier generation). In contrast, sample (b) and sample (c) with either in situ ALD DEZ treatment (10 cycles) or in situ ALD DEZ/H_2O treatment (10 cycles) both demonstrate distinct modulation of drain current (I_{ds}) by the gate voltage (V_{gs}). It is attributed to a significantly reduced D_{it} compared to sample (a) without ALD DEZ treatment. Consequently, the gate voltage can more effectively modulate the Fermi level to form an inverted channel layer. This is consistent with the observation we have shown in the C-V characteristics of MOSCAPs. All three devices have a comparable off-state current in the order of ~10^{-1} mA/mm at a V_{ds}=0.5 V. The ON/OFF Ratios are 10^1–10^2. The I_{ds}-V_{ds} output characteristics are shown in Figure 3.30.

This is the first demonstration of p-channel InGaAs MOSFETs as far as we know, though the devices do not show good performance. Nevertheless, ALD DEZ based interface passivation technique is still highly promising for inversion-type InGaAs p-MOSFETs applications.

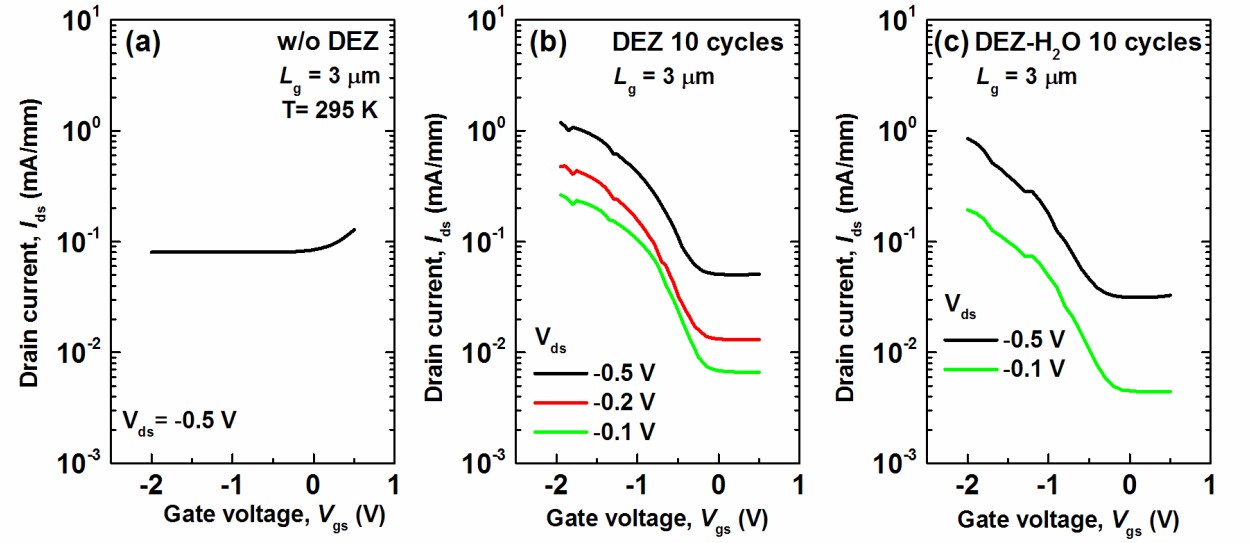


Figure 3.29. I_{ds}-V_{gs} transfer characteristics of p-channel $In_{0.53}Ga_{0.47}As$ MOSFETs (a) without DEZ treatment (b) with DEZ 10 cycles (c) with DEZ-H_2O 10 cycles of treatment.

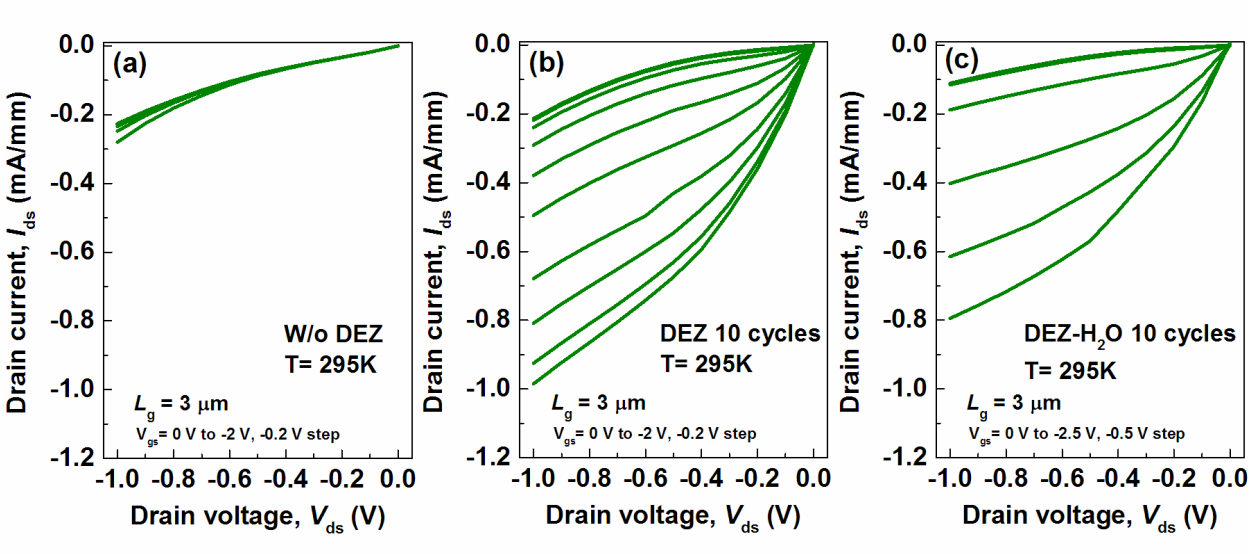


Figure 3.30. (a) I_{ds}-V_{ds} output characteristics of p-channel $In_{0.53}Ga_{0.47}As$ MOSFETs (a) without DEZ treatment (b) with DEZ 10 cycles (c) with DEZ-H_2O 10 cycles of treatment.

3.6 Summary

In chapter 3, we have compared the electrical properties of $NH_4OH/(NH_4)_2S$ treated $In_{0.53}Ga_{0.47}As$ MOSCAPs using ALD $Hf_{0.5}Zr_{0.5}O_2$ and ALD HfO_2 high-k insulators. Both the hump-like features and the large frequency dispersion suggest that an effective interface passivation of high-k/$In_{0.53}Ga_{0.47}As$ is required to reduce D_{it} and mitigate Fermi level pinning. We have shown that in situ diethylzinc (DEZ) treatment can effectively passivate the traps near the mid-gap and valence band edge of $In_{0.53}Ga_{0.47}As$. With in situ DEZ surface treatment, remarkable inversion-like C-V characteristics were observed in MOSCAPs on the n-type $In_{0.53}Ga_{0.47}As$ substrates. This behavior was still present even when the devices were measured at low temperature (100 K). With a few DEZ pulse cycles of incubation period during the initial surface reactions, the interface passivation takes full effect approximately from 5-10 cycles and shows

saturation behavior up to 100 cycles. DFT calculation has shown that the reduction of trap states of InGaAs near the valence band edge can be attributed to the effective passivation of As dangling bonds by Zn atoms. We have also proposed that the minority carrier response on n-type $In_{0.53}Ga_{0.47}As$ substrate may be due to the surface counter doping by p-type dopant Zn via ALD surface reactions. In addition, alternative ALD-based interface passivation techniques using ALD-$Mg(CpEt)_2$ treatment and hollow PEALD-AlN interlayer have been studied. At last, we have demonstrated both inversion-type enhancement-mode n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs and p-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD DEZ-based interface passivation technique. This work shows that the ALD-based interface passivation technique using in situ DEZ treatment is highly promising to be implemented in future $In_{0.53}Ga_{0.47}As$ CMOS technology by making p-channel MOSFET feasible.

CHAPTER 4

SIN_X/GAN MIS-HEMTS WITH CRYSTALLINE INTERFACIAL LAYER USING HOLLOW CATHODE PEALD

The contents of this chapter are partially adapted from a recently submitted manuscript to *IEEE Electron Device Letters*, entitled "Robust SiN_x/GaN MIS-HEMTs With Crystalline Interfacial Layer Using Hollow Cathode PEALD". The authors are Xin Meng, Jaebeom Lee, Arul Vigneswar Ravichandran, Young-Chul Byun, Jae-Gil Lee, Antonio T. Lucero, Si Joon Kim, Min-Woo Ha, Chadwin D. Young, and Jiyoung Kim. My contribution was the design and execution of experiments, as well as the preparation of the manuscript. Jaebeom Lee performed the TEM inspection of the gate stack. Arul Vigneswar Ravichandran prepared the TEM sample using FIB. Dr. Young-Chul Byun and Dr. Jae-Gil Lee assisted the mask design, process development, and electrical characterization. Dr. Antonio T. Lucero, Dr. Si Joon Kim, and Dr. Min-Woo Ha provided useful suggestion to analyze the data and revise the manuscript. Dr. Chadwin D. Young provided the pulsed I-V measurement capability in his advanced electrical characterization lab. Dr. Jiyoung Kim provided the valuable guidance of the experiments and input to prepare the manuscript.

4.1 Abstract

In this chapter, we report GaN MIS-HEMTs with a 16-nm-thick silicon nitride (SiN_x) gate insulator and surface passivation layer grown using low-temperature (300 °C) hollow cathode plasma-enhanced atomic layer deposition. Tris(dimethylamino)silane (3DMAS) and a remote N_2 plasma were used as the silicon precursor and the nitrogen co-reactant, respectively. Though the growth temperature was as low as 300 °C, we obtained excellent film properties comparable to

those of high-quality thermal SiN_x films grown at a temperature above 700 °C. High-resolution transmission electron microscopy images of the gate stacks showed high-quality SiN_x/GaN interface with ~1.5 nm β-phase Si_3N_4 crystalline interfacial layer. Furthermore, the devices showed a negligible hysteresis of ~50 mV, a steep subthreshold slope of 72 mV/dec, and a high ON/OFF drain current ratio of ~10^9. Additionally, the devices demonstrated a negligible bias-induced threshold voltage (V_{th}) instability (ΔV_{th}<0.3 V up to $V_{G,stress}$= +8 V for > 3000 s) as well as a mitigated current collapse.

4.2 Introduction

Gallium nitride (GaN)-based metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs) have emerged as the front-runner for next generation high-efficiency power switching devices owing to the high breakdown voltage, low on-resistance, high switching speed, and high power density [29, 113]. However, the GaN MIS-HEMTs technology suffer several critical reliability issues ascribed to the trapping process near the dielectric/III-nitrides interface [31, 114]. For example, the threshold voltage (V_{th}) instability [32, 80], such as a forward-reverse sweep hysteresis of V_{th} and a V_{th} shift (ΔV_{th}) under a positive/negative bias gate stress, poses a significant challenge for the reliable operation in commercial products. Furthermore, the increase of the dynamic on-resistance (R_{on}) [115], or the so-called current collapse [34], induces the unwanted switching loss and therefore deteriorates the performance of power switching devices. Unlike other dielectrics, silicon nitride (SiN_x) is able to form a good interface on III-nitrides with a lower density of trap states, by passivating the nitrogen vacancies, Ga dangling bonds and suppressing the Ga−O bonds formation [42]. Furthermore, SiN_x has a large conduction

band offsets with III-nitrides (2.0-2.3 eV) [53] and it is a mature dielectric material that is being widely used in semiconductor industry. Thus, SiN_x has been extensively studied as gate insulator and passivation layer in GaN HEMTs [41, 42, 50, 54].

Recently, plasma-enhanced atomic layer deposition (PEALD) becomes highly attractive for SiNx growth due to the ability to grow conformal film with high quality and precise thickness control at low temperatures [56]. There are a few attempts to use inductively coupled (ICP) PEALD SiN_x gate insulators on recessed gate GaN MIS-HEMT structures [58-60, 116-118]. Though improved V_{th} stability was demonstrated under a small gate bias stress (< 3 V), the performance degraded when a larger stress gate bias (e.g., 7 V) was applied. This could be related to a surface damage from recess etch and a low film quality (e.g., a low refractive index of 1.85-1.87) of PEALD SiN_x grown by SiH_4 and N_2 plasma. Furthermore, the efficacy of using PEALD SiN_x passivation layer on access regions to suppress current collapse was not studied. In this work, we demonstrate GaN MIS-HEMTs on Si with an excellent V_{th} stability and a mitigated current collapse using a high-quality SiN_x gate insulator and surface passivation layer grown by low temperature (300 °C) hollow cathode PEALD.

4.3 Experimental

The substrate for fabricating AlGaN/GaN HEMTs is a commercial 6-inch AlGaN/GaN on Si wafer purchased from DOWA Electronic Materials Co., Ltd (Tokyo, Japan). The epitaxial structure is shown in Table 4.1. The wafer consists of a p-type Si (111) substrate with a resistivity of <0.1 Ω ·cm, a 2.4 µm buffer layer, a 1.2 µm GaN layer, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 2 nm GaN cap layer. The epitaxial layers were grown by metal-organic chemical vapor deposition (MOCVD). The mobility, carrier density, and sheet resistivity determined by Hall effect

measurement (Van der Pauw structure) are 1382 $cm^2/V \cdot s$, 1.02×10^{13} cm^{-2}, 442 ohm/sq, respectively.

Table 4.1. The wafer epitaxial structure information of 6-inch AlGaN/GaN on Si wafer purchased from DOWA Electronic Materials Co., Ltd. (Tokyo, Japan).

Layer	Material	Thickness (nm)	Notes
4	GaN	2	cap
3	$Al_xGa_{1-x}N$	20	x=0.25
2	GaN	1200	-
1	Buffer	2400	-
Substrate	6-inch p-Si (111)	-	$r < 0.1\ \Omega \cdot cm$

Figure 4.1 illustrates a schematic of the AlGaN/GaN MIS-HEMTs fabrication process flow. As shown in Figure 4.2, the wafer was diced into 1 cm×1.5 cm sized coupons by a wafer dicing service company. After cleaning the surface particles with compressed N_2 gas, the samples were further cleaned with acetone using an airbrush. Then, standard solvent cleaning to remove organic contamination was performed: rinse in acetone, methanol, isopropanol alcohol (IPA) and DI water (optional) for 3 min, 1 min, 1 min, and 1 min, respectively. The sample was blown dry with a nitrogen gun. Then, the sample was cleaned in 10:1 HF for 5 min to remove the oxidized surface layer and rinsed in DI H_2O for 3 min.

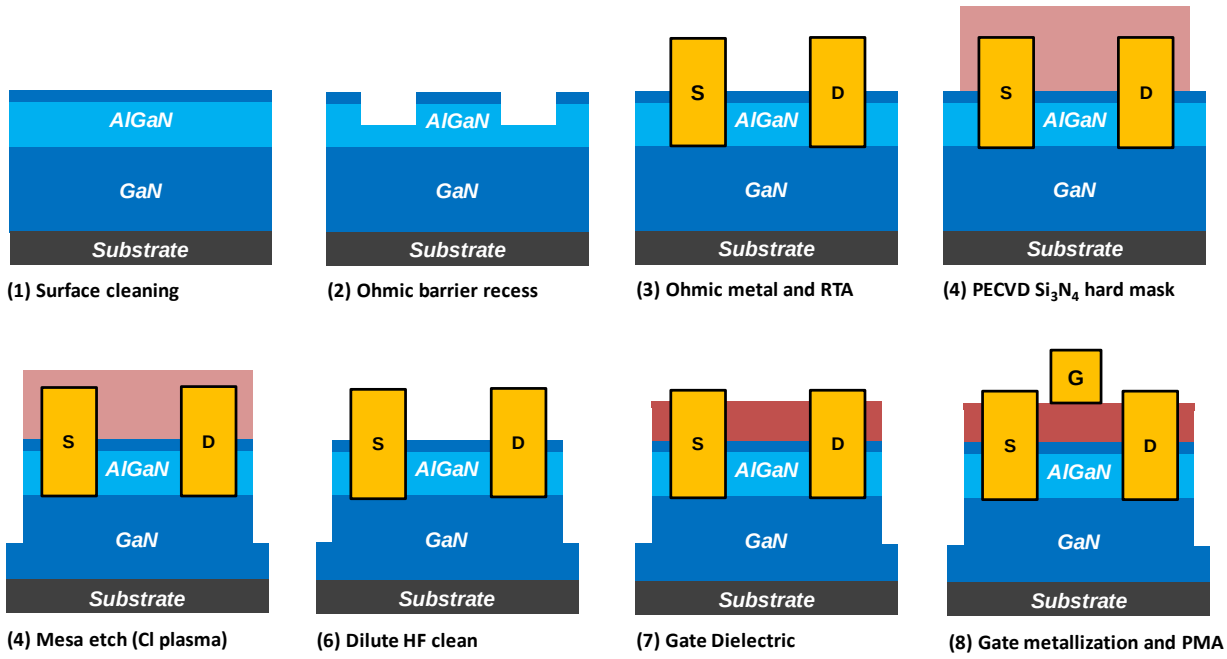


Figure 4.1. Schematic of the AlGaN/GaN MIS-HEMTs fabrication process flow.

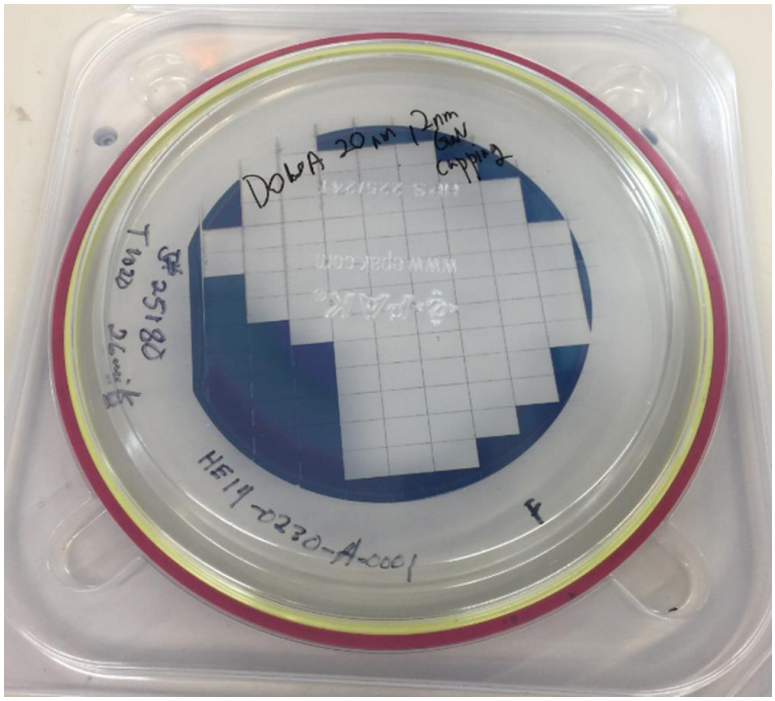


Figure 4.2. Coupons diced from 6-inch wafer used for AlGaN/GaN MIS-HEMTs fabrication.

A negative PR (NLOF 2020) was spin-coated and GaN HEMT ohmic contact PR pattern was formed using Karl Suss MA6 BA6 contact aligner and AZ300 MIF developer (60 s). Then, ~14 nm barrier recess was realized using ICP plasma etching (50 s, Cl_2/BCl_3 18 sccm/2 sccm, 5 mTorr, RF/bias power 300 W/5 W). The recess profile and the depth were confirmed by AFM, as shown in Figure 4.3. After cleaning in 1:1 H_2O/HCl (37%) for 1 min, DI H_2O rinse 1 min and N_2 dry, the sample was immediately loading into e-beam evaporator to avoid re-oxidation. A metal stack of Ti/Al/Ni/Au (20/100/25/50 nm) was deposited using e-beam evaporation, followed by lift-off. Finally, the alloyed ohmic contact was formed by rapid thermal annealing (RTA) at 830 °C for 30 s in an N_2 ambient.

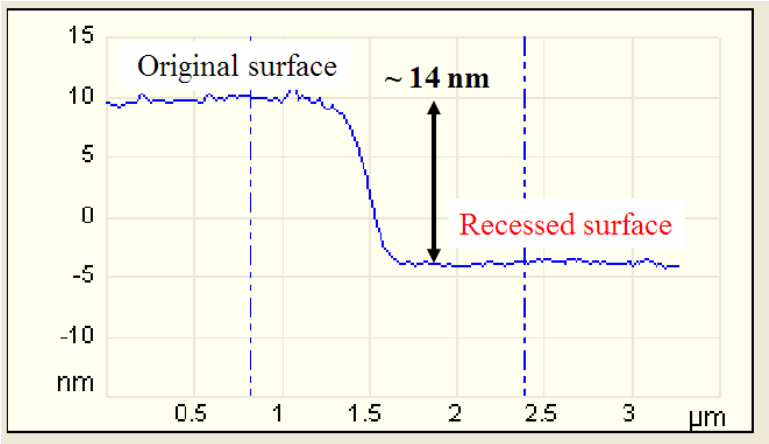


Figure 4.3. AFM line profile of a barrier recess step height of ~14 nm.

Next, mesa isolation was performed. 300−350 nm PECVD SiN_x (250 °C, 30 min) hard mask was deposited on the sample to ensure a sufficient protection of the sample during the plasma etching. A positive PR (S1813) was spin-coated and GaN HEMT MESA PR pattern was formed using Karl Suss MA6 BA6 contact aligner and MIF 319 developer (60 s). With the active regions

protected by the positive PR, the silicon nitride hard mask was selectively removed using F-plasma etching (dry etch rate 80−100 nm/min, 5 mTorr using SF_6 or CHF_3/O_2) for 5 min. Then, the sample was dipped into heated AZ400T PR stripper solution and rinsed with acetone/IPA to remove the PR. With the patterned PECVD SiN_x hard mask layer, 400−500 nm AlGaN/GaN layer was etched away by ICP plasma (750−900 s, Cl_2/BCl_3 18 sccm/2 sccm, 5 mTorr, RF/bias power 350 W/10 W). Finally, the sample was subject to acetone/IPA cleaning for 1 min and PECVD SiN_x hard mask removal by 100:1 dilute HF for 5 min. By this step, the sample is ready for preliminary characterization, such as mesa isolation plasma etching step height measurement by profilometer, buffer leakage measurement, and transmission line measurement (TLM).

Prior to gate dielectric growth, a cleaning step was performed in 100:1 dilute HF for 3 min to remove the surface oxides. Thermal ALD gate dielectrics (15 nm Al_2O_3) was deposited in the Cambridge Nanotech S100 thermal ALD reactor. The process repeated 150 cycles of TMA pulse/purge/H_2O pulse/purge of 0.03/10/0.03/10 s respectively at 300 °C. 16 nm PEALD SiN_x was performed in the hollow cathode plasma-enhanced ALD reactor, which is equipped with a commercial hollow cathode plasma source (Meaglow Ltd.). The schematic of the reactor and the PEALD SiN_x process sequence are illustrated in Figure 4.4 (a) and (b). Hollow cathode plasma source has been investigated to grow III-nitrides by PEALD due to the beneficial low oxygen contamination and high film crystallinity, which are not usually obtained using ICP plasma sources. Tris(dimethylamino)silane (3DMAS or TDMAS) and a remote N_2 plasma were used as the silicon precursor and the nitrogen co-reactant, respectively. The growth process consisted 1500 cycles (1/15/15/10 s) at 300 °C. The chamber was maintained at ~ 300 mTorr with a constant N_2 flow. The plasma RF power was 100 W.

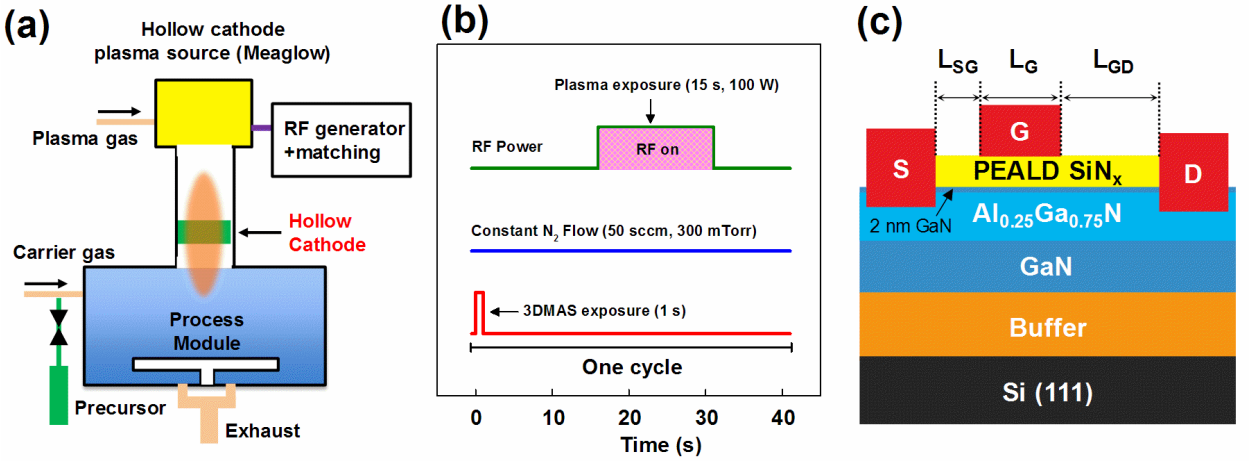


Figure 4.4. (a) Schematic of the hollow cathode PEALD reactor, (b) PEALD SiN_x process sequence, and (c) schematic cross-sectional structure of SiN_x/GaN MIS-HEMT.

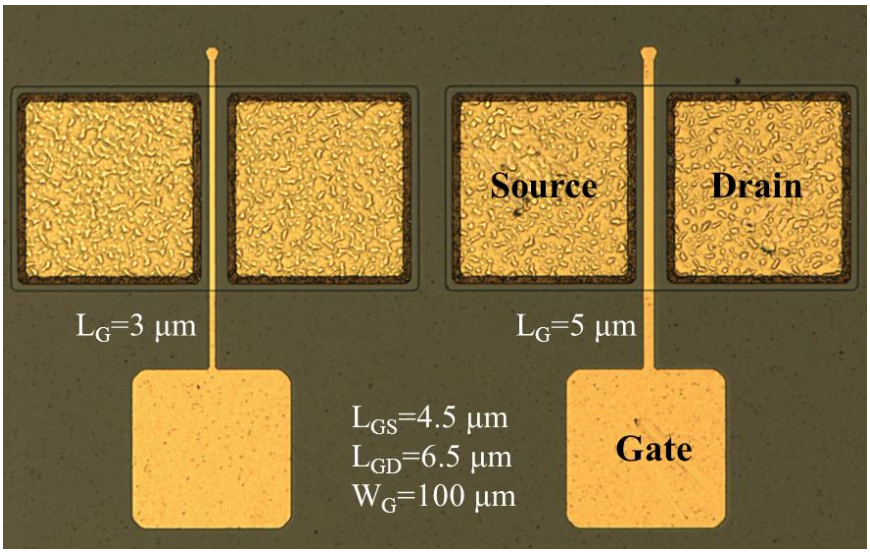


Figure 4.5. Optical microscope image of the completed GaN MIS-HEMTs.

To fabricate Schottky-barrier (SB) HEMTs, the gate dielectric deposition step was skipped. Next, a negative PR (NLOF 2020) was spin-coated and GaN HEMT gate PR pattern was formed

using Karl Suss MA6 BA6 contact aligner and AZ300 MIF developer (60 s). A Ni/Au (20 nm/100 nm) gate electrodes were deposited using e-beam evaporation, followed by lift-off and post metallization annealing (PMA) at 400 ℃ for 15 min in an N_2 ambient. As shown in Figure 4.4 (c), the device dimensions are specified as the gate length (L_G), the gate width (W_G), the gate-to-source distance (L_{GS}), and the gate-to-drain distance (L_{GD}). Figure 4.5 shows the optical microscope image of the completed GaN MIS-HEMTs.

4.4 Results and Discussion

4.4.1 Contact Resistance and Buffer Leakage

Figure 4.6 (a) shows the I-V characteristics of TLM structure after mesa isolation without growing any films. The linear dependence of the current density on the voltage suggests an ohmic contact behavior, instead of a rectifying behavior of Schottky contact. The resistance extracted from the slope of I-V characteristics is plotted as a function of distance between etch pad, as shown in Figure 4.6 (b). Using the method described in chapter 2, the contact resistance (R_c) was determined to be 0.8 ohm·mm and sheet resistance was determined to be 536 ohm/sq.

Figure 4.7 shows the I-V breakdown characteristics of buffer leakage test structure after mesa isolation using (a) current (A) and (b) current density (A/cm^2) as the unit. The test structure consists an inner circle pad with a diameter of 100 μm, which is physically isolated from the larger pad by plasma etching with a gap of 10 μm. The low leakage current density below 10^{-7} A/cm^2 up to 200 V (limitation of the tool) suggests the excellent isolation of devices by plasma etching. It ensures a low off-state current for HEMTs without interference from the peripheral devices.

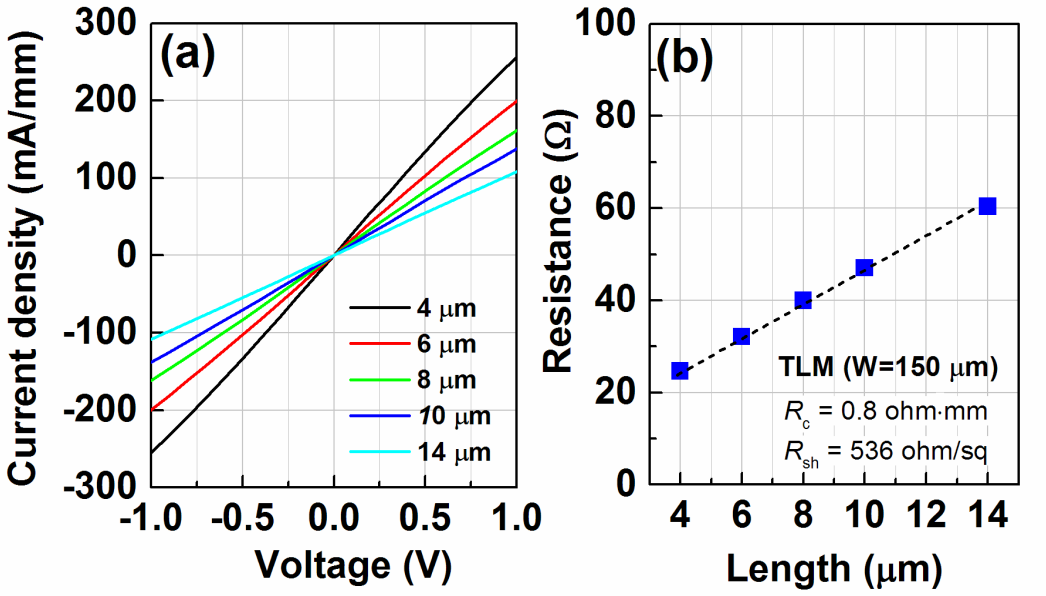


Figure 4.6. (a) I-V characteristics and (b) resistance of TLM structure after mesa isolation as a function of the distance (4 μm, 6 μm, 8 μm, 10 μm, and 14 μm) between each pad.

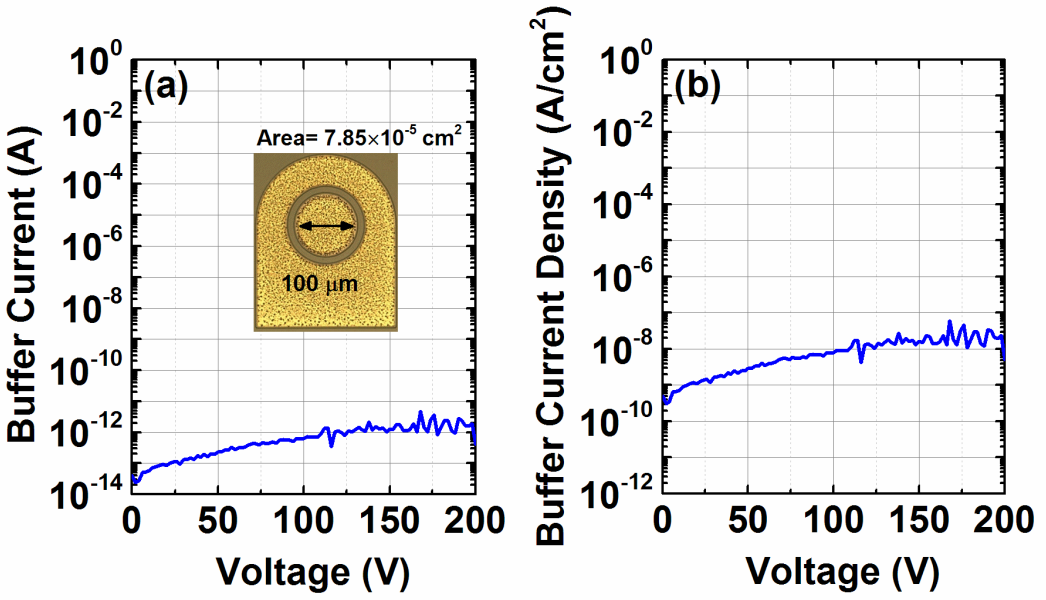


Figure 4.7. I-V breakdown characteristics of buffer leakage test structure after mesa isolation using (a) current (A) and (b) current density (A/cm^2) as the unit.

4.4.2 Characterization of Hollow Cathode PEALD SiN_x Film

Table 4.2. Summary of the properties of the PEALD SiN_x film.

Film	Thickness (nm)	Refractive Index (RI)	Growth Per Cycle (GPC, Å)	Density (g/cm^3)	Wet Etch Rate (nm/min, 100:1 HF)
SiN_x	16.6	2.00	0.11	2.9	0.8

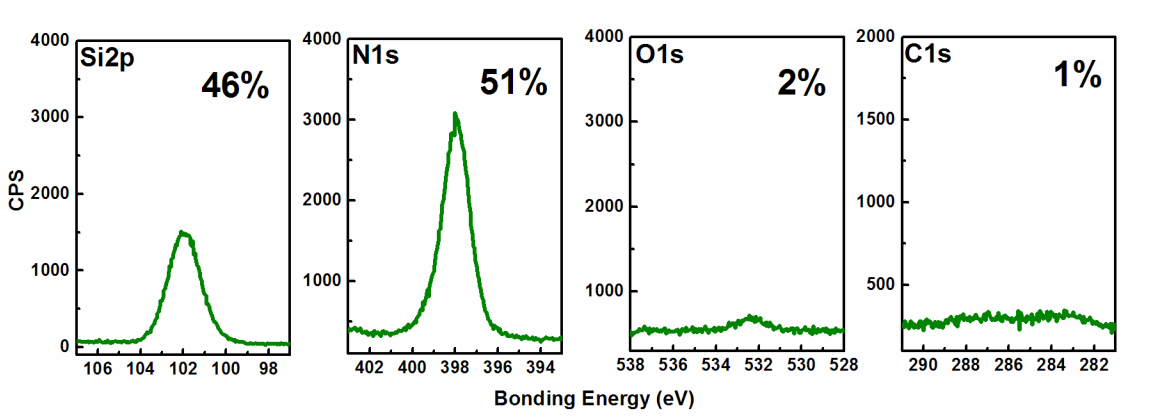


Figure 4.8. Ex situ XPS analysis of the PEALD SiN_x film after 2 min argon sputtering.

Table 4.2 summarizes the properties of SiN_x grown by 1500 cycles of PEALD process. The film thickness on Si determined by spectroscopic ellipsometry is ~16 nm. The refractive index is 2.00, close to that of the stoichiometric Si_3N_4 (2.01). The film density is 2.9 g/cm^3 and the wet etch rate in 100:1 hydrofluoric acid (HF) is 0.8 nm/min. These properties are comparable to those of high-quality thermal SiN_x grown by low-pressure chemical vapor deposition (LPCVD) at a temperature >700 °C. The growth per cycle (GPC) is approximately 0.11 Å, which is comparable to the results reported by Stanford in ICP PEALD reactors [119]. As shown in Figure 4.8, ex situ

XPS analysis indicates a low oxygen content (2 at. %) and a negligible carbon content (≤1 at. %) in the bulk film. The calculated N/Si ratio is 1.1.

4.4.3 Device Characterization

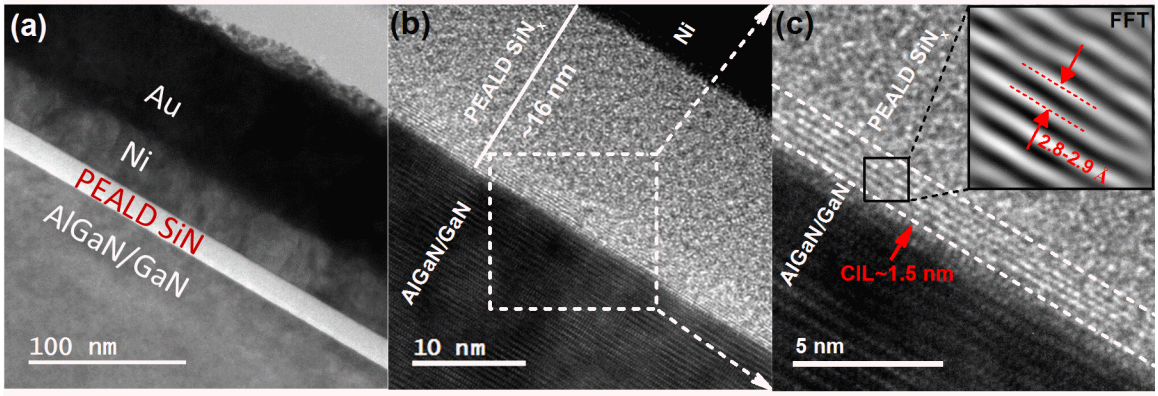


Figure 4.9. (a) (b) Cross-sectional HRTEM images of the gate stack of SiN_x/GaN MIS-HEMT. (c) A higher magnification view of ~1.5 nm crystalline interfacial layer (CIL). The inset FFT image shows the d-spacing is 2.8-2.9 Å, indicating that the CIL is β-phase Si_3N_4.

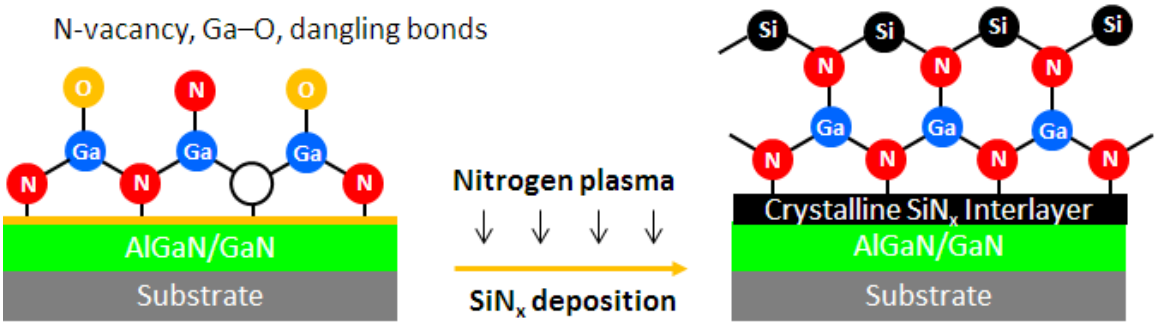


Figure 4.10. Schematic of a PEALD SiN_x crystalline interfacial layer, which passivates the nitrogen vacancies and the dangling bonds terminated on the III-nitrides surface.

Figure 4.9 shows the cross-sectional high-resolution transmission electron microscopy (HRTEM) images of the gate stack of MIS-HEMT. Underneath the Ni/Au stack, uniform PEALD SiN_x layer can be clearly observed on top of the bottom AlGaN/GaN substrate. The PEALD SiN_x

film thickness is ~16 nm, consistent with the result determined by spectroscopic ellipsometry. A higher magnification image in Figure 4.9 (c) indicates the presence of ~1.5 nm crystalline interfacial layer (CIL). The Fast Fourier Transform (FFT) image of CIL (inset) suggests an out-of-plane lattice constant (d-spacing) of 2.8-2.9 Å, indicating a β-phase Si_3N_4 with a hexagonal crystal structure [120]. This is the first demonstration of crystalline SiN_x layer grown on hexagonal wurtzite GaN by ex situ low-temperature PEALD. The crystalline layer is expected to provide a good passivation of the nitrogen vacancies and the dangling bonds terminated on the III-nitrides surface, as shown in Figure 4.10.

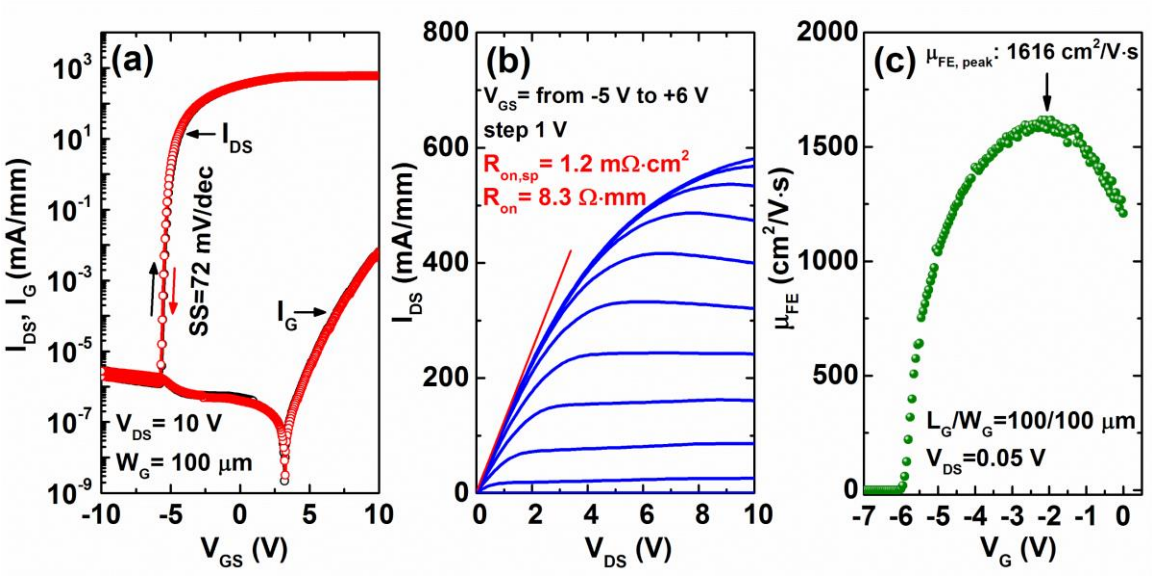


Figure 4.11. (a) DC I_{DS}/I_G-V_{GS} double sweep transfer curves and (b) I_{DS}-V_{DS} output curves. $L_{GS}/L_G/L_{GD}$=4.5/3/6.5 µm. (c) Field effective mobility extracted from a long channel device (W_G/L_G=100/100 µm).

Figure 4.11 (a) shows the DC I_{DS}/I_G-V_{GS} double sweep transfer curves of the MIS-HEMTs. The extracted V_{th} (at I_{DS}=1 mA/mm) is -5.0 V. The devices show a negligible hysteresis of ~50

mV under a $V_{G,max}$ of 10 V, a steep subthreshold slope of 72 mV/dec and a high ON/OFF drain current ratio of ~10^9. Figure 4.11 (b) shows the I_{DS}-V_{DS} output curves of the MIS-HEMTs. The maximum I_{DS} is 584 mA/mm (V_{DS}=10 V). The R_{on} extracted from the maximum slope of the output curves is 8.3 Ω·mm, corresponding to a specific on-resistance ($R_{on,sp}$) of 1.2 mΩ·cm^2. As shown in Figure 4.11 (c), the field effective mobility (μ_{FE}) extracted from a long channel device (L_G=100 μm) is as high as 1616 $cm^2/V \cdot s$.

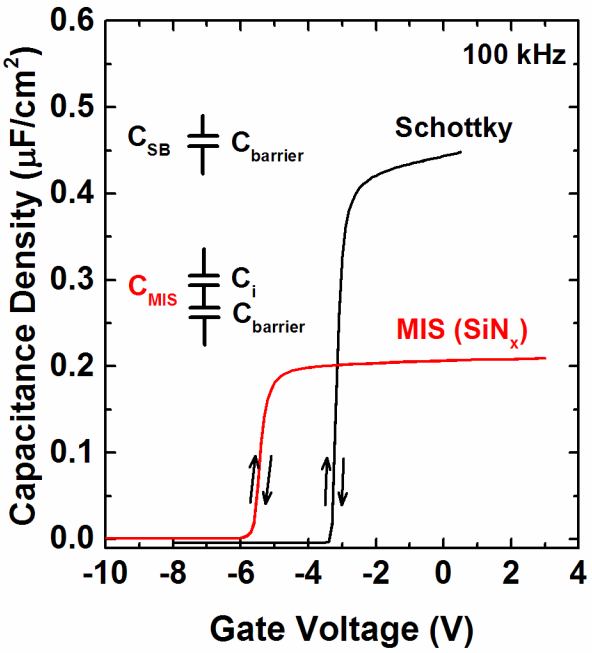


Figure 4.12. Bi-directional C-V hysteresis characteristics of a Schottky gate capacitor and a MIS-capacitor (16 nm PEALD SiN_x) measured at 100 kHz. The gate electrode diameter is 100 μm.

The dielectric constant of PEALD SiN_x can be estimated using the capacitance-voltage (C-V) curves of Schottky gate capacitor and MIS-capacitor. As shown in Figure 4.12, both samples show indistinguishable hysteresis between forward and reverse C-V sweep. The applied gate

voltage for Schottky gate capacitor could not exceed 0.5 V due to a large gate leakage current without an insulator barrier. At a gate voltage of 0 V, the capacitance density of Schottky gate capacitor (C_{SB}) is $C_{barrier}$=0.443 μF/cm^2 while the capacitance density of MIS-capacitor (C_{MIS}) is $(C_i^{-1}+C_{barrier}^{-1})^{-1}$= 0.215 μF/cm^2. Therefore, insulator capacitance density (C_i) is 0.416 μF/cm^2. Given that the dielectric constant of AlGaN barrier is 8.8 and thickness of SiN_x is 16 nm, the calculated AlGaN barrier thickness is 17.6 nm and the dielectric constant of PEALD SiN_x is 7.5.

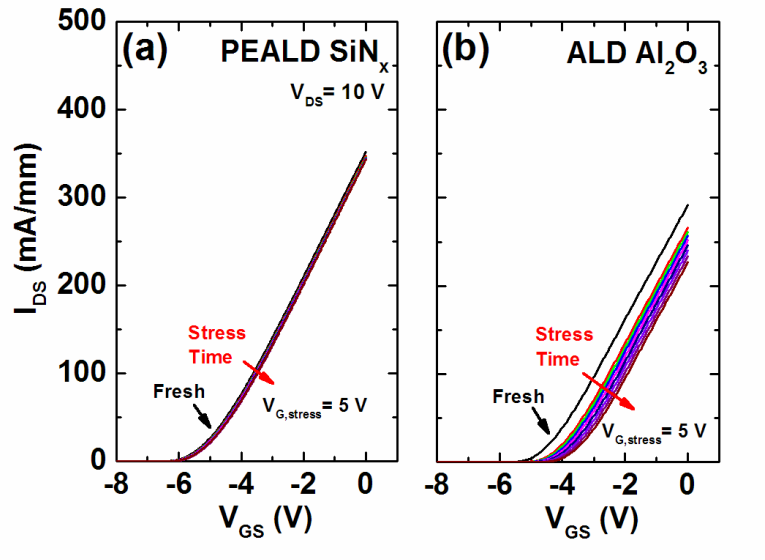


Figure 4.13. I_{DS}-V_{GS} transfer characteristics of MIS-HEMTs with (a) 16 nm PEALD SiN_x and (b) 15 nm ALD Al_2O_3 gate insulator under a constant gate bias stress of 5 V up to 3162 s. $L_{GS}/L_G/L_{GD}$=4.5/5/11.5 μm.

Figure 4.13 shows the I_{DS}-V_{GS} transfer characteristics of MIS-HEMTs with 16 nm PEALD SiN_x and 15 nm ALD Al_2O_3 gate insulator under a constant gate bias stress of 5 V up to 3162 s. The gate stress voltage was only applied to the gate while keeping the source and drain grounded. The V_{DS} during I_{DS}-V_G measurement was 10 V. The V_G during I_{DS}-V_G measurement ranged from

-8 V to 0 V with a step voltage of 20 mV. Sample (a) with 16 nm PEALD SiN_x gate insulator demonstrates stable I_{DS}-V_{GS} transfer curve without a significant positive shift. In contrast, sample (b) with 15 nm ALD Al_2O_3 gate insulator shows a significant positive shift of I_{DS}-V_{GS} transfer curve during the continuous measurement, particularly for the first measurement after a short gate bias stress for 1 s.

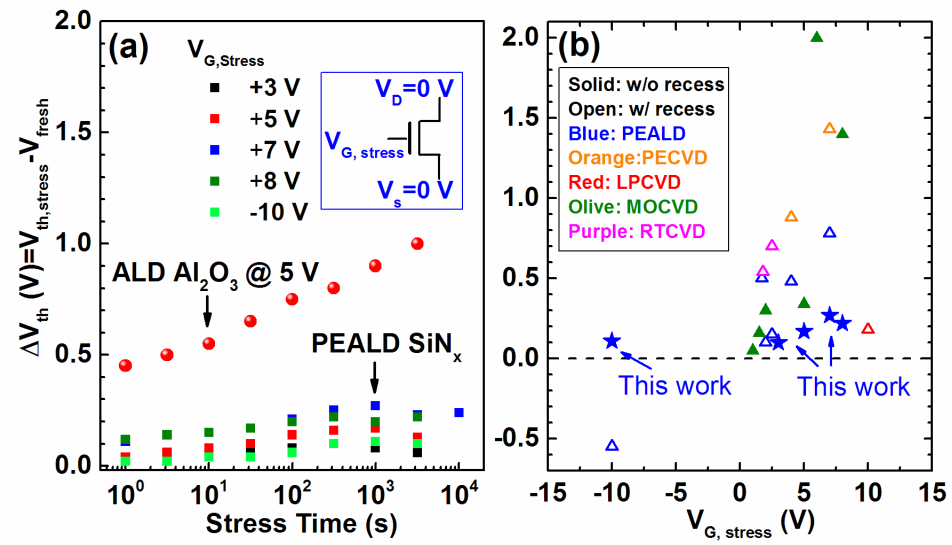


Figure 4.14. (a) Bias-induced V_{th} instability of MIS-HEMTs using gate bias stress measurement at room temperature. The ΔV_{th} values are plotted as a function of the stress time. $L_{GS}/L_G/L_{GD}$=4.5/5/11.5 μm. (b) Comparison of the ΔV_{th} values under different gate stress voltages for 10^3–10^4 s in this work with the results reported in the literatures using SiN_x gate insulators.

Figure 4.14 (a) shows the V_{th} shift (ΔV_{th}) with respect to the fresh devices as a function of the gate stress voltage ($V_{G,Stress}$) and the stress time at room temperature. After the fresh I_{DS}–V_G measurement, the subsequent measurements were performed automatically after certain stress time intervals from 1 s up to 10000 s. At each gate bias condition, the gate bias stress was applied to different devices to avoid the effect of pre-stress. Under a negative bias stress of -10 V (OFF-state)

and a moderate positive bias stress of +3 V or +5 V (ON-state), the V_{th} starts from a negligible ΔV_{th} of <60 mV to a maximum ΔV_{th} of <170 mV. Furthermore, under a large positive bias stress of +7 V or +8 V, the V_{th} starts from a small ΔV_{th} of 110-120 mV to a maximum ΔV_{th} of 220-270 mV. For all the stress conditions in this study, the ΔV_{th} reaches saturation after 1000 s stress without further positive drift. In contrast, for a reference sample with 15 nm ALD Al_2O_3 (300 °C) gate insulator, the V_{th} starts with a large ΔV_{th} of 450 mV, and continuously drifts to a maximum ΔV_{th} of 1000 mV, even under a moderate positive bias stress of +5 V. As shown in Figure 4.14 (b), the ΔV_{th} under different gate stress voltages for 10^3–10^4 s are compared with the results reported in the literature using SiN_x gate insulators. The SiN_x deposition methods include low-temperature process (PEALD and PECVD) and high-temperature process (MOCVD, LPCVD, and RTCVD). Clearly, excellent V_{th} stability has been demonstrated in this work. The outstanding performance is attributed to the use of a high-quality PEALD SiN_x gate insulator with a crystalline interfacial layer in the gate stack and a low bulk trap density.

Figure 4.15 (a) shows the I_{DS}-V_{DS} output curves of MIS-HEMTs using DC and pulsed I–V measurements. The gate bias ranged from -7 V to +5 V for all the measurements with a step voltage of 1 V. For the DC I_{DS}-V_{DS} measurement, the I_{DS} tailed off beyond certain V_{DS} because of the self-heating effect. For the pulsed I_{DS}-V_{DS} measurement, the waveform had a pulse width of 800 ns and a pulse period of 1 ms, respectively. The quiescent gate bias point ($V_{G,Q}$) was set at -10 V (OFF-state), while the quiescent drain bias point ($V_{D,Q}$) was set at 0 V and 20 V. We extracted the ratio of dynamic R_{on}/DC Statics R_{on} as a function of the off state quiescent V_{DS}. As shown in Figure 4.15 (b), the dynamic R_{on} of SiN_x/GaN MIS-HEMT sample increases by 6% at an off-state quiescent V_{DS} of 20 V whereas the dynamic R_{on} of the reference sample with 15 nm ALD Al_2O_3

gate insulator increases by 36%. In contrast, the reported MIS-HEMTs with in situ MOCVD SiN_x (14 nm) passivation in the access region showed serious current collapse behavior [41]. The low current collapse, even without introducing additional passivation layers and field plates, clearly validates the benefits from the use of PEALD SiN_x for surface passivation.

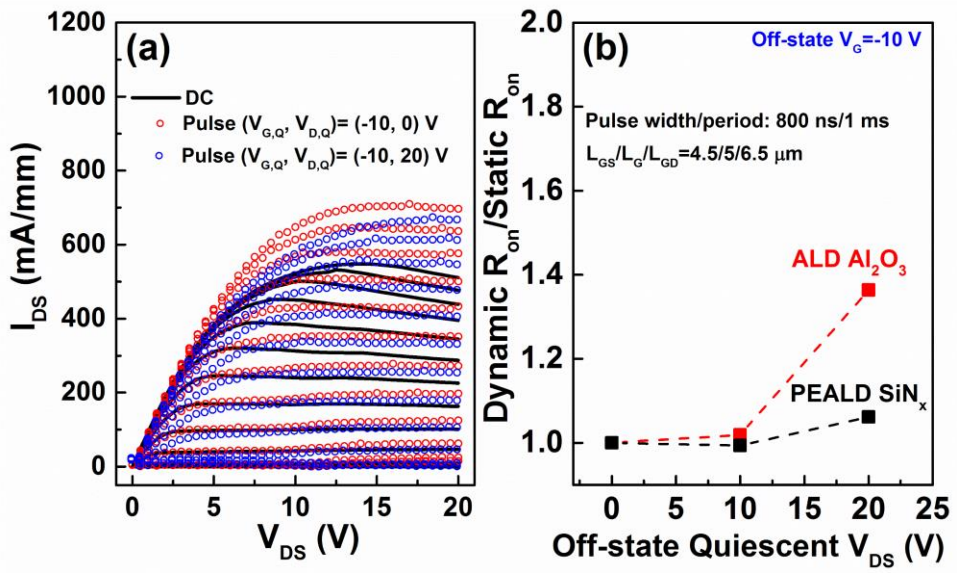


Figure 4.15. (a) I_{DS}-V_{DS} output curves of MIS-HEMTs with 16 nm PEALD SiN_x gate insulator using DC and pulsed I−V measurements. (b) The extracted ratio of dynamic R_{on}/DC static R_{on}, compared to that of a sample using 15 nm ALD Al_2O_3 gate insulator.

4.5 Summary

In Chapter 4, we have demonstrated robust GaN MIS-HEMTs adopting a 16-nm-thick low-temperature hollow cathode PEALD grown SiN_x as a gate insulator and surface passivation layer. TEM images of the gate stack showed a crystalline interfacial layer (~1.5 nm) consisting of β-phase Si_3N_4. The devices showed a negligible hysteresis (~50 mV), a steep subthreshold slope (72 mV/dec), a high ON/OFF ratio (~10^9), a high V_{th} stability (ΔV_{th}<0.3 V up to $V_{G,stress}$= +8 V for >

3000 s), and a mitigated current collapse. The excellent device performance and reliability is attributed to the passivation of surface/interface defects by the crystalline interfacial layer and high quality PEALD SiN_x with a low bulk trap density. This work suggests that the PEALD SiN_x technology is highly promising to be utilized in GaN-based power and radio-frequency devices.

CHAPTER 5

EFFECT OF ALD-GROWN EPITAXIAL ZNO CAP LAYER ON THE ELECTRICAL CHARACTERISTICS OF ALGAN/GAN HETEROSTRUCTURE

5.1 Introduction

AlGaN/GaN heterostructure exhibits high electron mobility and high carrier density. It is widely used in high electron mobility transistors (HEMTs) for high-power and high-frequency applications. As discussed in chapter 1, Zinc oxide (ZnO) can be epitaxially grown on GaN along [0001] c-axis using ALD due to small lattice mismatch (~1.9%). Theoretically, introducing an epitaxial ZnO cap layer on AlGaN/GaN heterostructure can induce a positive V_{th} shift. However, the electrical characteristics of AlGaN/GaN heterostructure with epitaxial ZnO cap layer have seldom been studied. Chapter 5 studies the effect of ALD-grown epitaxial ZnO cap layer on the electrical characteristics of AlGaN/GaN heterostructure.

5.2 Experimental

ZnO was deposited in the Cambridge Nanotech S100 thermal ALD reactor. As illustrated in Figure 5.1, metal-organic precursor diethylzinc (DEZ, $(C_2H_5)_2Zn$, Sigma-Aldrich) and DI H_2O or O_3 served as the Zn source and the oxygen source, respectively. One ALD cycle consisted a DEZ pulse/purge/oxidant pulse/purge time sequence of 0.03/10/0.03/10 s. A 500-nm GaN/Si substrate (Kyma) and a 2-nm GaN cap/20-nm $Al_{0.25}Ga_{0.75}N$/GaN/Si substrate (DOWA) grown with ALD ZnO films (300 cycles, 300 °C, DEZ and H_2O) were employed for high-resolution transmission electron microscopy (HRTEM) analysis.

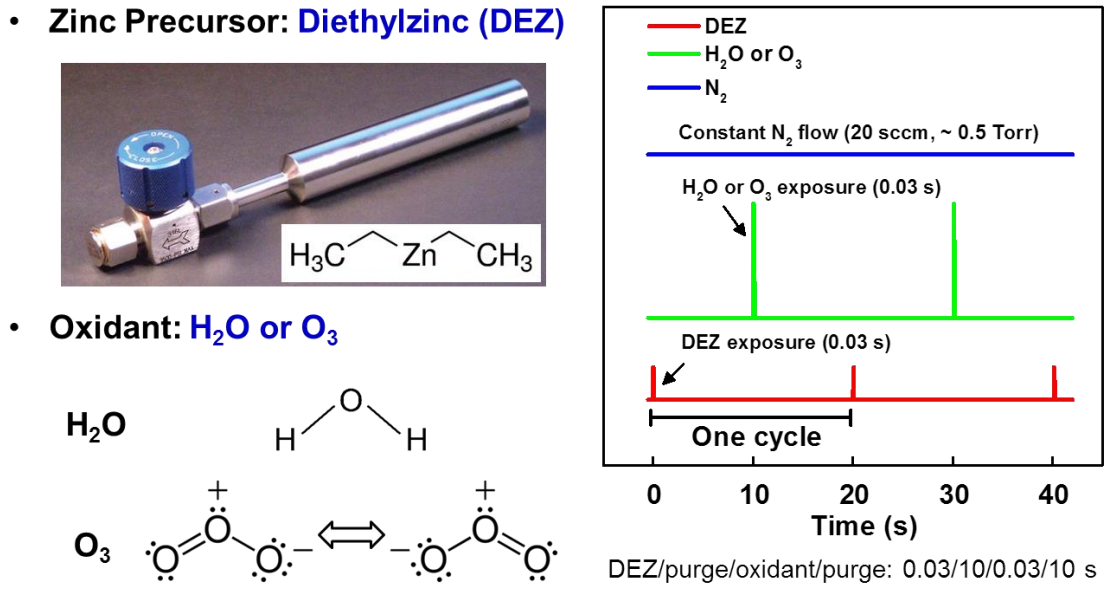


Figure 5.1. Schematic diagram of one cycle of ZnO ALD process.

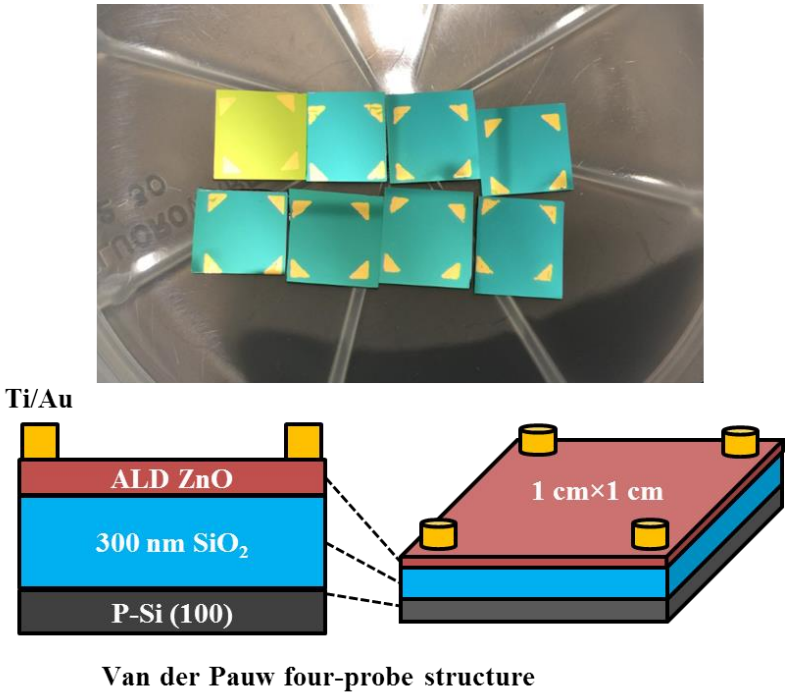


Figure 5.2. Samples for Hall effect measurement with Van der Pauw four-probe structure.

The type of carrier, carrier concentration, carrier mobility, and resistivity of ZnO films were determined by Hall effect measurement using Van der Pauw four-probe method at room temperature (Figure 5.2). To fabricate the samples, 20−30 nm ALD ZnO films were grown on 300 nm thermal SiO_2/p-Si substrates at a temperature of 320 °C. Ohmic contacts were formed at each corner (1 cm×1 cm) by evaporating Ti/Au (30 nm/100 nm) through shadow masks. Some samples with DEZ/H_2O deposited ZnO films were subject to direct oxygen plasma treatment (1−10 min, 50 W, 100 mTorr, Technics reactive ion plasma etcher) prior to depositing ohmic contacts.

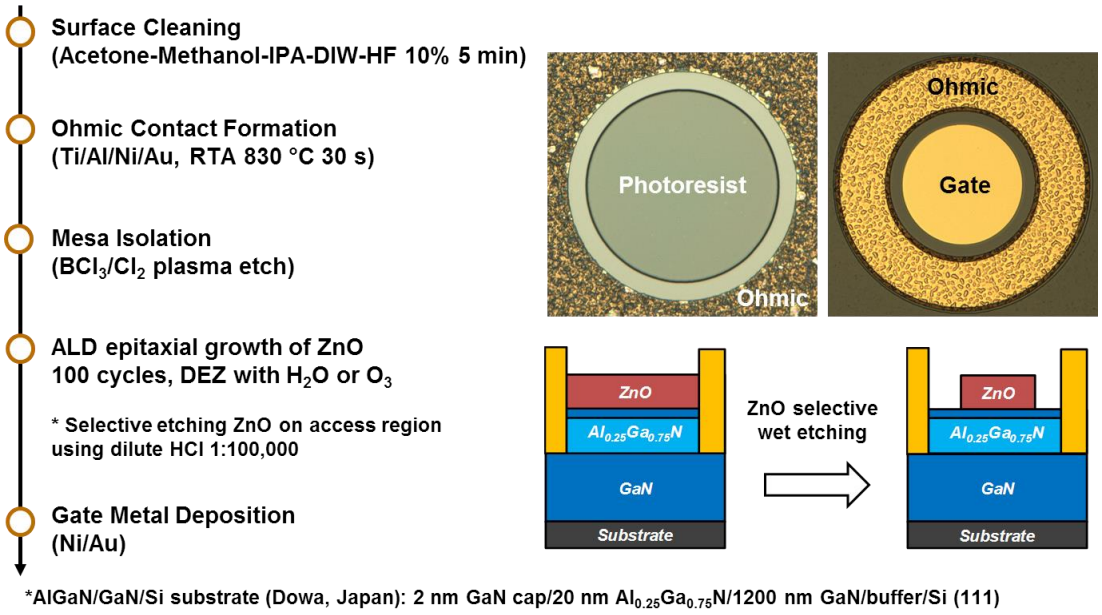


Figure 5.3. Process flow of fabricating AlGaN/GaN HEMTs with ALD-grown epitaxial ZnO cap layer. Selective etching technique was developed to define the pattern of ZnO.

As shown in Figure 5.3, the fabrication process flow was basically the same as that described in chapter 4. After 3 min 100:1 HF cleaning, ZnO films were deposited on the samples at 320 °C for 100 cycles. A slightly higher growth temperature than that used in the samples for

TEM analysis was employed to improve the crystallinity of epitaxial ZnO while to avoid the decomposition of DEZ at temperatures above 330 °C [121]. Due to the low resistivity of epitaxial ZnO films, a high off-state leakage current was observed. Therefore, a selective etching technique was developed to reduce the leakage current. The ZnO films were selectively removed by wet etching in dilute HCl solution (1:100,000) for 10−20 min, while the ZnO films on the gate region were protected by positive photoresist (S1813). The ZnO film thickness on devices and the surface morphology were determined by AFM measurement shown in Figure 5.4.

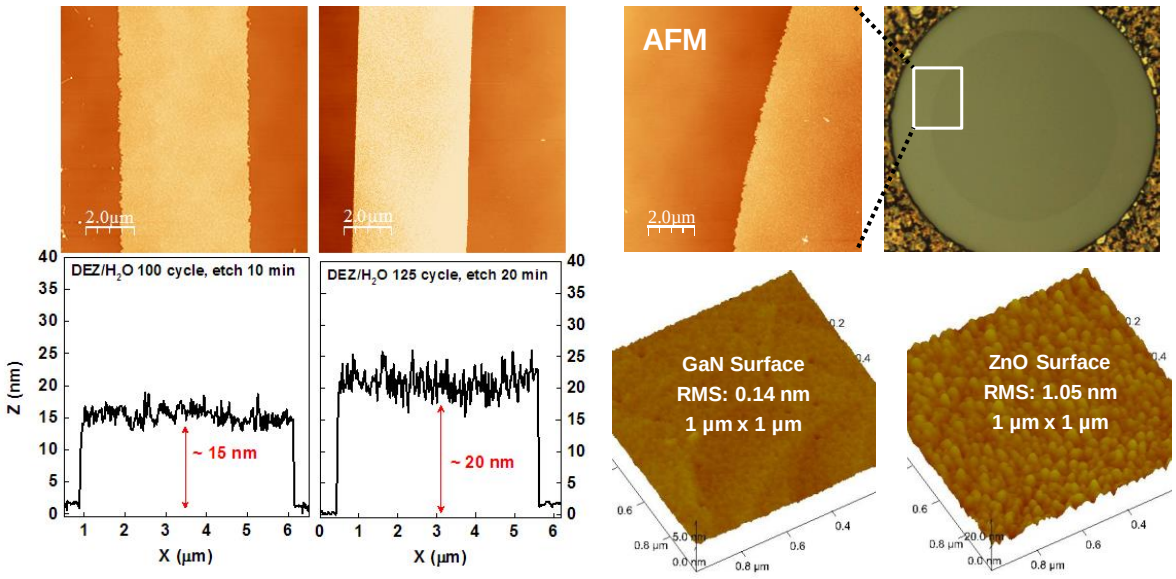


Figure 5.4. AFM characterization of ZnO step height on HEMT structures and surface morphology on a capacitor structure after ZnO cap layer was defined by selective etching.

5.3 Results and Discussion

As shown in the HRTEM images in Figure 5.5 (a) and (b), ZnO films were epitaxially grown on either GaN/Si substrate or GaN/AlGaN/GaN/Si substrate with an atomically sharp

interface and clear single-crystalline lattice structure. The corresponding energy dispersive spectroscopy (EDS) composition analysis, shown in Figure 5.5 (c) and (d), provided the elemental information across the structure. Particularly, a sharp EDS interface was obtained on the DOWA substrate without a significant inter-diffusion of elements.

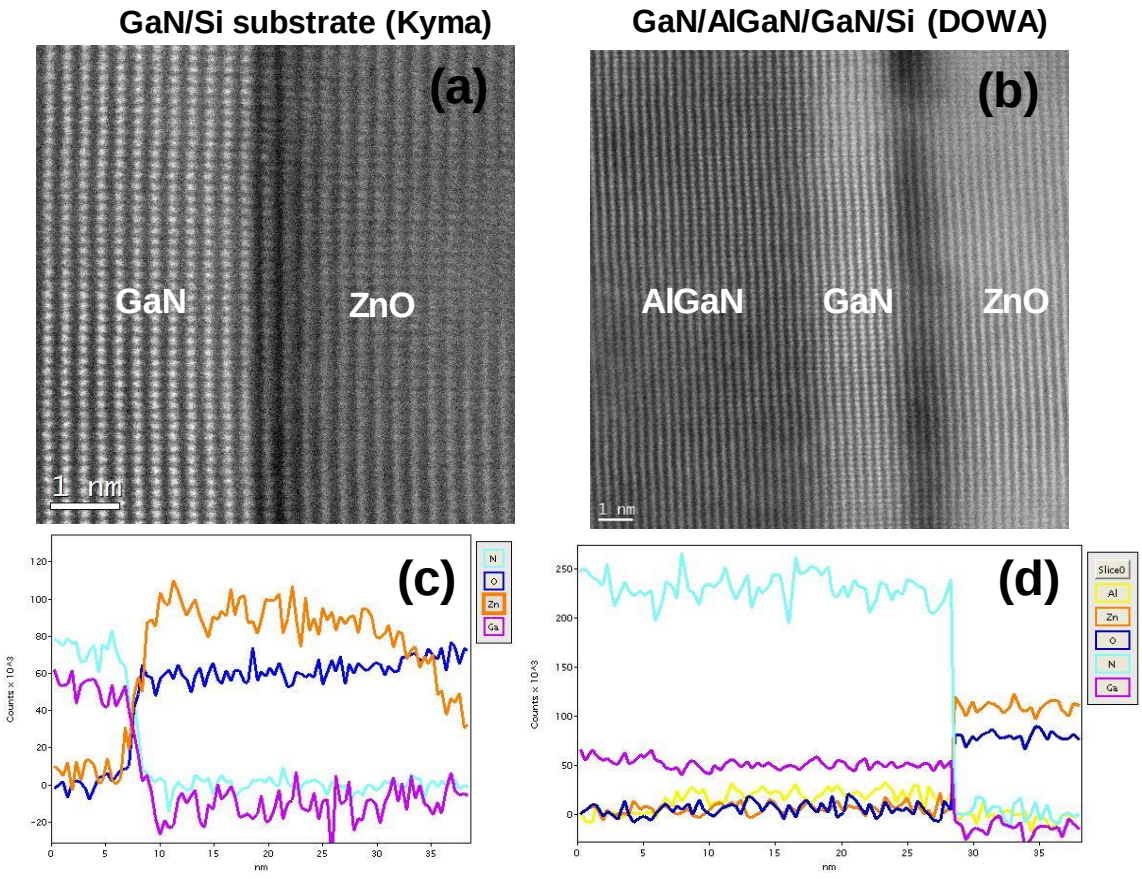


Figure 5.5. HRTEM images and corresponding energy dispersive spectroscopy (EDS) composition analysis of ALD ZnO on (a, c) GaN/Si substrate (b, d) GaN/AlGaN/GaN/Si substrate.

Figure 5.6 shows the comparison between the Schottky gate capacitor and the ZnO MOS capacitor. As mentioned earlier, the ZnO MOS capacitor showed a high off-state leakage current

when ZnO was not selectively etched. Also, the C-V curve is abnormal as shown in Figure 5.6 (b). One of the suspected reasons for this abnormality is that the ZnO films were conductive and they conducted leakage current from the gate electrode to the ohmic contacts. If this is the phenomenon behind this behavior, selective etching of ZnO might help in resolving the problem. Consistent with our expectation, in Figure 5.6 (c), the C-V curve of ZnO MOS capacitor with selective etching show normal behavior with a clear transition from accumulation to depletion. However, V_{th} was not significantly impacted with the conductive H_2O-based ZnO cap layer.

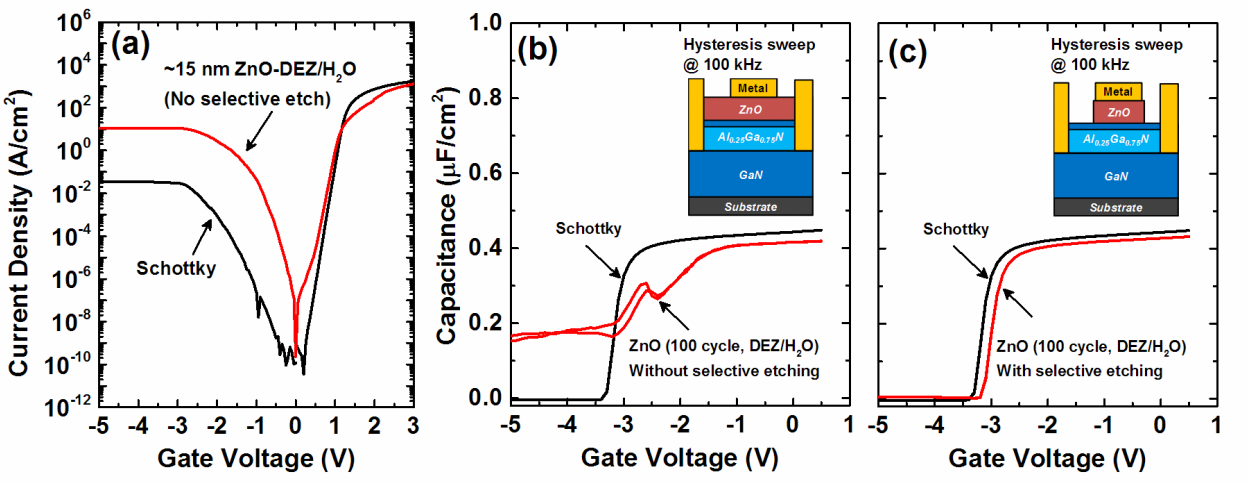


Figure 5.6. Comparison between the Schottky capacitor and the ZnO MOS capacitor. (a) I-V characteristics, (b) C-V characteristics without selective etching, and (c) C-V characteristics with selective etching. The diameter of gate electrode was 100 μm in this work.

The conductive characteristic of ZnO discussed above was also confirmed using Hall effect measurement. As shown in Figure 5.7, the ZnO films grown using DEZ and H_2O at 320 °C are n-type semiconductor, exhibiting a high carrier concentration of 2×10^{19} cm^{-3} and a low resistivity of 0.16 ohm·cm. The n-type doping characteristics of ZnO have been ascribed to the presence of

donor defects including oxygen vacancy, Zn interstitial, hydrogen impurity [122]. It was reported that O_2 plasma treatment could reduce the carrier concentration by reducing the amount of oxygen vacancy [123]. However, our results indicated that ex situ O_2 plasma post deposition treatment on ZnO films did not reduce the carrier concentration. This could be due to the difference in the plasma treatment conditions.

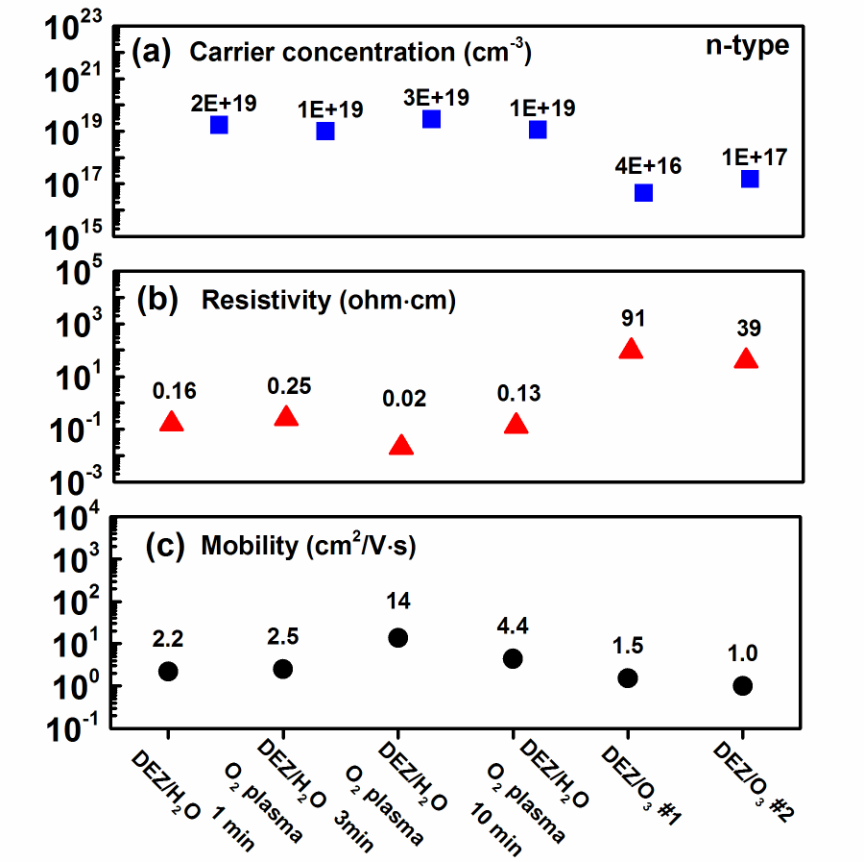


Figure 5.7. (a) Carrier concentration, (b) resistivity, and (c) mobility of the ALD ZnO films determined by Hall effect measurement.

In addition, the O_2 plasma treatment severely degraded the device performance and shifted the V_{th} to a positive direction. As shown in Figure 5.8, the two O_2 plasma (3 min) treated ZnO

HEMT samples have a lower I_{DS} and a higher I_G. In addition, a positive V_{th} shift was observed in both the V_{GS}-I_{DS} transfer characteristics and the corresponding C-V characteristics. Furthermore, additional experiment was done by fully removing the plasma treated ZnO layer prior to gate metallization. The sample also showed a degraded performance and a positive V_{th} shift (not shown). Therefore, the positive V_{th} shift could be due to the negative charge incorporated into the barrier during the plasma treatment, which is analogous to the fluorine plasma treatment technique to obtain normally-off operation.

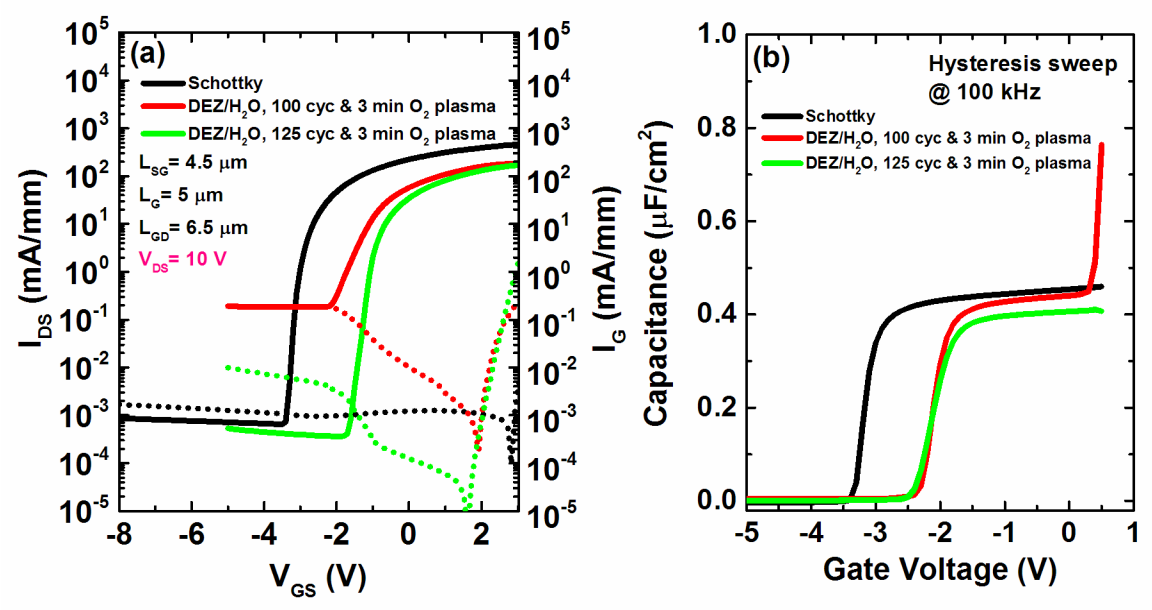


Figure 5.8. Comparison between the Schottky gate HEMT sample and the O_2 plasma treated H_2O-based ZnO cap layer HEMT samples. (a) The V_{GS}-I_{DS} transfer characteristics and (b) the corresponding C-V characteristics of capacitors.

As seen from the results of Hall effect measurement in Figure 5.7, the ZnO films grown using DEZ and O_3 have at least two orders lower carrier concentration (~1×10^{17} cm^{-3}) and two orders higher resistivity. It is consistent with a previous report that the ALD ZnO films showed a

reduced carrier concentration when H_2O was replaced by O_3 as the oxidant [124]. The distinction between the electrical properties of H_2O-based ALD ZnO and O_3-based ALD ZnO triggered our interest in further study.

As shown in Figure 5.9, there is an immediately change of source/drain two-terminal I-V curve before and after O_3-based ZnO cap layer growth. The lower current after ZnO growth suggests that available 2DEG in the channel is reduced (or depleted) due to the introduction of the ZnO cap layer. As a result, the increase of sheet resistance caused a lower current.

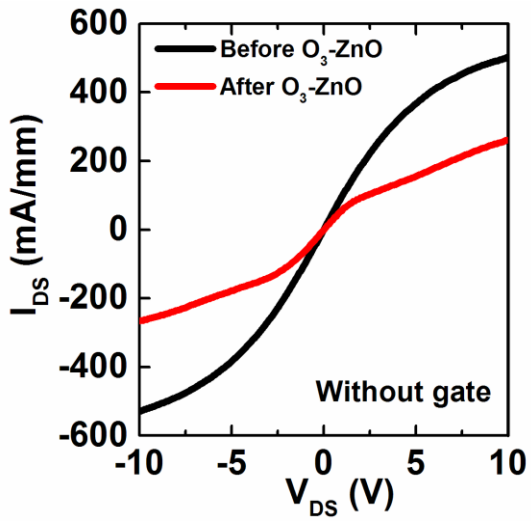


Figure 5.9. Comparison of source/drain two-terminal I-V curves before and after O_3-based ZnO cap layer growth (DEZ/O_3, 100 cycles).

As shown in Figure 5.10, compared to the Schottky gate HEMT sample, the O_3-based ZnO cap layer HEMT sample shows ~1 V positive V_{th} shift without any plasma treatment. The ability to modulate V_{th} indicates that introducing an epitaxial ZnO cap layer has potential to be a new method to realize normally-off operation. However, O_3-based ZnO cap layer HEMT sample still has a higher gate leakage current. The existence of the conductive ZnO residue or a reduced energy

barrier height for 2DEG may explain the higher gate leakage. In addition, the V_{DS}-I_{DS} output characteristics of both samples are shown in Figure 5.11, respectively.

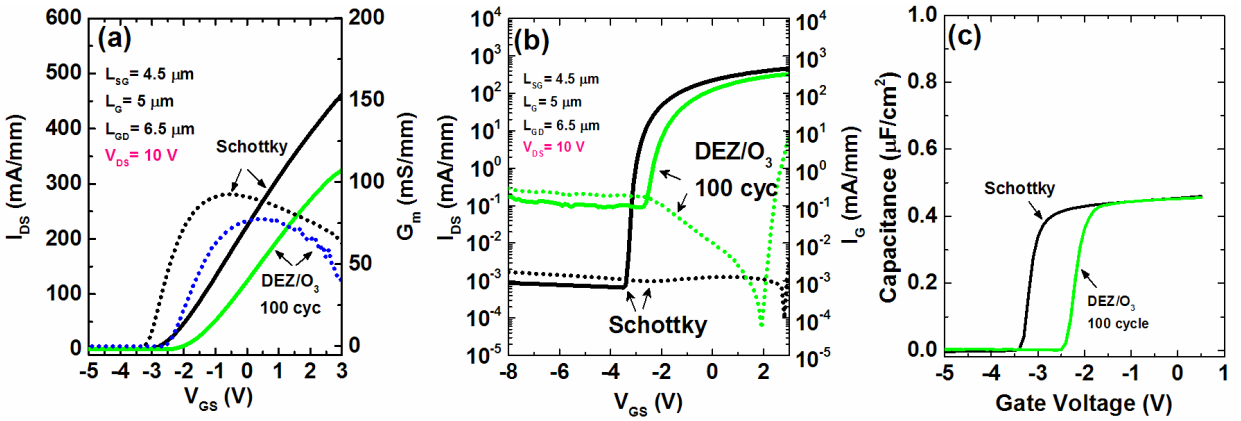


Figure 5.10. Comparison between the Schottky gate HEMT sample and the O_3-based ZnO cap layer HEMT sample. (a) Linear scale, (b) log scale of the V_{GS}-I_{DS} transfer characteristics, and (c) the corresponding C-V characteristics.

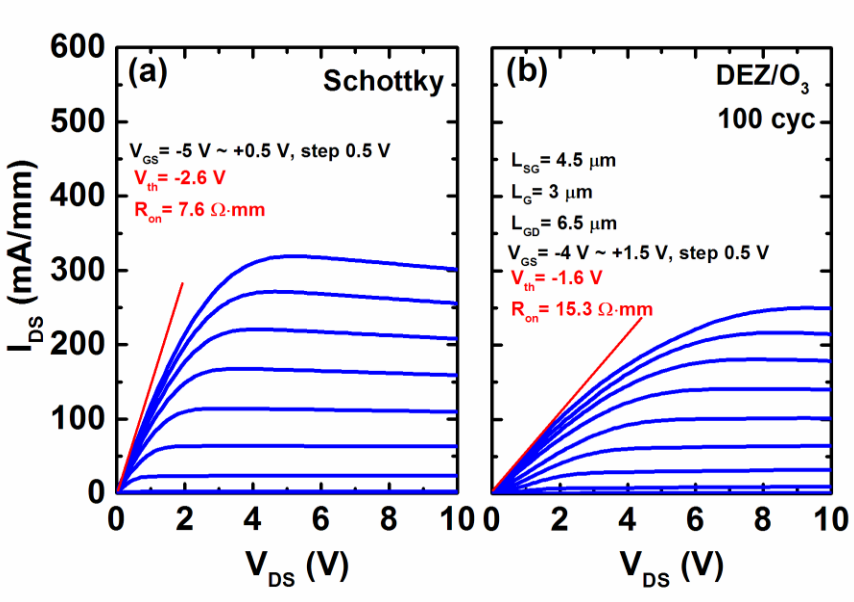


Figure 5.11. Comparison of the V_{DS}-I_{DS} output characteristics between (a) the Schottky gate HEMT sample and (b) the O_3-based ZnO cap layer HEMT sample.

The results suggest that the epitaxial ZnO cap layer could affect the V_{th} in a similar manner to the InGaN cap layer, which is discussed in chapter 1, due to the presence of piezoelectric polarization. Still in its infancy, the quality of the epitaxial ZnO grown by ALD cannot compete with those of high-quality ZnO crystals grown by MBE or MOCVD at higher temperatures. Additionally, the high carrier concentration and the poor surface morphology on GaN require further process optimization including proper surface pretreatment, long purging time to enhance nucleation and atom diffusion, and the use of oxygen plasma to assist the ZnO film growth.

5.4 Summary

Epitaxial growth of single-crystalline ZnO on AlGaN/GaN heterostructure with an atomically sharp interface has been successfully demonstrated via ALD. Hall effect measurement results showed that H_2O-based ALD ZnO films exhibited n-type behavior with a high carrier concentration (~10^{19} cm^{-3}). In the case of O_3-based ALD ZnO films (n-type), the carrier concentration was reduced by approximately 2−3 orders of magnitude to 10^{16}–10^{17} cm^{-3}. Compared to the Schottky gate HEMTs, the HEMTs with H_2O-based ZnO cap layer (DEZ/H_2O, 100 cycles) showed a similar V_{th}. Post-deposition treatment with oxygen plasma severely degraded the device performance and positively shifted the V_{th}. In contrast, the HEMTs with O_3-based ZnO cap layer (DEZ/O_3, 100 cycles) showed ~1 V positive V_{th} shift without plasma damage. Decent output characteristics were demonstrated whereas a high gate leakage current was observed. We attribute the positive V_{th} shift to the piezoelectric polarization of ZnO cap layer, resembling that of an InGaN cap layer, with a direction opposite to that in the underlying AlGaN/GaN substrate.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

The focus of this work is the application of atomic layer deposition (ALD) technique to two different types of high mobility III-V compound semiconductor devices: the $In_{0.53}Ga_{0.47}As$ MOSCAPs/MOSFETs and the AlGaN/GaN HEMTs. The ALD-grown films function as gate dielectrics and interface/surface passivation layers on the above-mentioned III-V semiconductor substrates.

Inversion-type $In_{0.53}Ga_{0.47}As$ MOSFETs, like Si MOSFETs, have an inverted surface channel consisted of minority carriers. However, the $In_{0.53}Ga_{0.47}As$ MOSCAPs without an interfacial passivation layer (IPL) suffered from high D_{it} and Fermi level pinning, which are detrimental to the formation of inversion layer. In addition to 10 cycles of in situ ALD DEZ/H_2O (ZnO) IPL passivation, we found that in situ ALD DEZ interface passivation mitigated the problem in a similar fashion and demonstrated inversion-like C-V characteristics on n-type substrates. Without the concern of non-self-limiting growth of thick ZnO IPL using ALD DEZ/H_2O >10 cycles, the ALD DEZ passivation technique have demonstrated saturated C-V characteristics as a function of the number of DEZ pulse cycle, from 5−10 cycles up to 100 cycles. Low-temperature (100 K) C-V measurement results have proved that the inversion-like behavior was not fake inversion because of the trap response but real inversion originating from the minority carrier response. Furthermore, first-principle DFT simulation have suggested that Zn atom can passivate the As dangling bonds (occupy the V_{Ga}), reducing the trap states near the valance bend edge of $In_{0.53}Ga_{0.47}As$. In addition, a hypothesis that the surface of n-type substrate was counter doped due

to the p-type dopant (Zn) incorporation was discussed. Lastly, this work has demonstrated inversion-type enhancement mode n-channel $In_{0.53}Ga_{0.47}As$ MOSFETs, and for the first time p-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using in situ ALD DEZ and ALD DEZ/H_2O (ZnO) treatment. This work suggests that the ALD DEZ-based interface passivation is highly promising to be implemented in III-V semiconductor CMOS technology using $In_{0.53}Ga_{0.47}As$ or even GaAs as the channel materials.

This work also studied AlGaN/GaN HEMTs from two perspectives. First, we employed silicon nitride (SiN_x) grown using low-temperature (300 °C) hollow cathode plasma-enhanced atomic layer deposition (PEALD) as a gate insulator and a surface passivation layer on GaN MIS-HEMTs. The SiN_x film showed excellent film properties, including a high refractive index, a high film density, and a low wet etch rate. HRTEM showed a high-quality SiN_x/GaN interface with ~1.5 nm crystalline interfacial layer (CIL). The d-spacing according to the FFT results is 2.8−2.9 Å, indicating that the CIL is β-phase Si_3N_4. The MIS-HEMTs showed a negligible hysteresis, a steep subthreshold slope, and a high ON/OFF drain current ratio. Additionally, the devices demonstrated a negligible bias-induced V_{th} instability as well as a mitigated current collapse. A theory that the excellent device performance and high reliability was attributed to the effective passivation of lattice defects (e.g., nitrogen vacancies and dangling bonds) on III-nitrides by the crystalline interfacial layer, as well as a negligible bulk trap density inside the PEALD SiN_x was proposed.

Second, epitaxial growth of ZnO cap layer on AlGaN/GaN heterostructure using ALD was studied. HRTEM indicated that the ALD-grown single-crystalline ZnO had an atomically sharp interface on GaN. Compared to Schottky gate devices, devices with a H_2O-based epitaxial ZnO

cap layer showed a similar C-V characteristic, whereas devices with an O_3-based epitaxial ZnO cap layer showed a significant positive shift of V_{th} (~1 V) both in the I-V and C-V characteristics. Hall effect measurement results suggested that O_3-based ALD ZnO had a 2−3 orders of magnitude lower electron concentration than H_2O-based ALD ZnO. A hypothesis that the positive shift of V_{th} was because of the piezoelectric polarization of ZnO cap layer, resembling that of an InGaN cap layer, with a direction opposite to that in the underlying AlGaN/GaN substrate was proposed.

6.2 Future Work

InGaAs Devices

Considering the relatively high CET (~2.3 nm) obtained in this work, it is worthwhile to further investigate how to obtain sub-nm EOT of high-k/metal gate stacks on $In_{0.53}Ga_{0.47}As$ using in situ ALD DEZ interface passivation. Future work should try to increase the dielectric constant of gate oxide and minimize the formation of low dielectric constant interfacial layer. Furthermore, the effective work function (EWF) of metal gate electrodes should be considered in the case of high-k/metal gate (HKMG) stack. It will be interesting to study alternative CMOS compatible metal gate materials (e.g., TiN, TaN) which are being widely used in the semiconductor industry. Interfacial reaction between TiN and HfO_2 may cause the Ti or nitrogen doping of HfO_2, resulting in a higher dielectric constant. Recent papers have also shown that a Pd gate electrode with a negative Gibbs free energy induced the oxidation of the InGaAs surface during the forming-gas PMA. In contrast, a TiN gate electrode with a positive Gibbs free energy caused the reduction of interfacial oxides (gathering oxygen) between HfO_2 and InGaAs. As a result, a significantly lower CET (from ~2.9 nm to ~1.2 nm using 4 nm HfO_2) was obtained using TiN gate electrode [125,

126]. The scavenging of interfacial oxide layer using direct or remote approaches has been widely investigated in Si high-k/metal gate CMOS technology [127, 128].

On the other hand, ferroelectricity (FE) can be obtained in TiN capped $Hf_{0.5}Zr_{0.5}O_2$ after annealing at ≥400 °C. Based on the study in our lab [129], ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ have shown a high dielectric constant (40−60) owing to the formation of non-centrosymmetric orthorhombic phase. The ferroelectricity together with the negative capacitance (NC) effect make a further study of TiN/$Hf_{0.5}Zr_{0.5}O_2$/$In_{0.53}Ga_{0.47}As$ devices attractive for FeFET and steep-slope NC-FET applications. Additionally, as discussed in this work, the surface doping effect of Zn, Mg, Si, and Ge containing interfacial passivation layers also deserves to be further studied.

Although this work has first demonstrated inversion-type p-channel MOSFETs, the performance is still inferior to the state of art devices on Si or Ge substrate. Further optimization on the current MOSFETs process flow should focus on the implantation (e.g., implantation and activation annealing conditions, Zn ion implantation), alternative encapsulation layers (e.g., thermal ALD Al_2O_3), and encapsulation layer etching/cleaning, etc.

SiN_x/GaN MIS-HEMTs

For GaN MIS-HEMTs, the mechanism of crystalline SiN_x interfacial layers formation is still not clear. It will be highly interesting to investigate how to precisely control the growth of crystalline SiN_x. In addition, we did a preliminary study using in situ N_2/NH_3 plasma pretreatment, followed by 15 nm PEALD SiN_x growth using chlorosilane precursors (carbon-free) and N_2/NH_3 plasma. The devices also demonstrated an extraordinary V_{th} stability (e.g., ΔV_{th} <100 mV under a gate bias stress of 6 V for 10^4 s). However, the bulk film properties were not as good as those reported in chapter 4. Therefore, the effect of plasma treatment (e.g., plasma gas composition, RF

power, time), the correlation of the PEALD process conditions and film properties with device electrical results, and the comparison with thermal ALD SiN_x film should be carefully studied in future.

Epitaxial ZnO Cap Layer on AlGaN/GaN

The rough surface morphology of epitaxial ZnO cap layer suggests that the epitaxial growth conditions on GaN were not optimized. Future study can evaluate a longer purging time or DEZ pre-exposure treatment to improve the nucleation and the surface morphology. Other growth methods including MOCVD, molecule beam epitaxy (MBE), and pulsed layer deposition (PLD) should also be considered. A study of control and characterize the polarity of ZnO on GaN will be also worthwhile. It has been reported that the polarity control of ZnO (Zn-polar or O-polar) on GaN template could be realized by initial surface engineering (Zn pre-exposure or O-plasma pre-exposure) using plasma-assisted molecular-beam epitaxy (PA-MBE). Furthermore, a plasma-assisted process (e.g., hollow cathode PEALD) should be considered for future study. It has been reported that plasma-enhanced thermal ALD can grow ZnO films exhibiting low carrier concentration and high resistivity [130]. An in situ O_2 plasma/purge step was added after each standard DEZ pulse/purge/H_2O pulse/purge cycle. The use of O_2 plasma at optimal conditions not only may reduce oxygen vacancy, interstitial Zn, and other impurities, but also may improve the crystallinity due to the benefits of plasma treatment.

Lastly, in situ material and electrical characterization studies using the cluster tool in our lab should be very interesting. For example, in situ characterizations of GaN samples (e.g., Van der Pauw, Hall bar, and TLM structure) can be performed as a function of the number of ZnO ALD cycle (or half cycle) from 0 to 1, 2, 10, 50, 100 or more. Raman spectroscopy can be used to

characterize the crystallinity and growth behavior of ZnO layer. XPS can be used to characterize the surface chemical reactions. TLM or Hall effect measurements can monitor the change of sheet resistance, electron density, and mobility of the 2DEG channel during the ALD ZnO growth.

APPENDIX A

GATE-LAST INGAAS MOSFET GENERAL PROCESS FLOW

[1] Ion Implantation → [2] Activation Annealing → [3] Gate Dielectric Stack → [4] Gate Metallization → [5] Source/Drain Contact and Backside Contact

Part I: Ion Implantation

1. Solvent Cleaning
    a) Dip into acetone for 3 min
    b) Dip into methanol for 1 min
    c) Dip into IPA for 1 min
    d) Dry with N_2 gun
2. Lithography
    a) Spin negative PR nLOF 2020 at 3000 RPM
    b) Bake at 115 ℃ for 60 s
    c) Mask set: InGaAs alignment
    d) Hard contact mode exposure with dose of 65 mJ/cm^2 using i-line
    e) Post exposure bake at 115 ℃ for 60 s
    f) Develop with AZ300 MIF developer for 60 s
    g) Rinse with DI H_2O and dry with N_2 gun
3. Optical microscope inspection
4. Alignment marker metal deposition using e-beam evaporator.
    a) e.g., Ni/Au 20 nm/100 nm or other metals

b) Base pressure below 5×10^{-6} Torr

5. Lift off
    a) Dip into acetone or heated AZ400T PR stripper (80 °C) for 15 min
    b) Spray and rinse in acetone and IPA to remove any residue
    c) Dry with N_2 gun
6. Optical microscope inspection
    a) To check alignment marker and any metal or PR residue
7. Encapsulation layer deposition
    a) 30 nm PECVD SiO_2 (or 10-30 nm thermal ALD Al_2O_3)
    b) Load "STDOX" recipe in PD01 PECVD, run at 250 °C for 30 s
    c) Check SiO_2 thickness on blank Si using ellipsometer
8. Lithography
    a) Spin positive PR S1813 at 3000 RPM
    b) Bake at 115 °C for 60 s
    c) Mask set: InGaAs Implantation
    d) Hard contact mode exposure with dose of 130 mJ/cm^2 using g-line
    e) Develop with MIF 319 developer for 60 s
    f) Rinse with DI H_2O and dry with N_2 gun
9. Optical microscope inspection
    a) To check the PR pattern alignment carefully
    b) It's a critical step and must repeat lithography if misalignment occurs
10. Ion Implantation

a) Stick the InGaAs sample safely to a 4-inch Si carrier wafer using tape at corners, keep the carrier wafer safely inside a wafer container, ship to CuttingEdge Ions, LLC (California, US) for ion implantation

b) A Si dose of 1×10^{14} ions/cm^2, 40 keV, tilt 7° for n-channel MOSFET

c) A Be dose of 1×10^{14} ions/cm^2, 40 keV, tilt 7° for p-channel MOSFET; Zn can be an alternative dopant for future implantation test

Part II: Activation Annealing

11. PR removal after ion implantation
    a) Dip into heated AZ400T PR stripper (80 °C) for 15 min
    b) Spray and rinse in acetone and IPA to remove any residue
    c) Dry with N_2 gun
12. Optical microscope inspection
    a) If needed, do acetone cleaning using an airbrush or O_2 plasma PR descum
13. Rapid thermal annealing (RTA)
    a) Use InGaAs annealing Si carrier wafer at MPTC RTP-600 (TR02)
    b) Dummy run with the process recipe for one or two times
    c) For n-channel MOSFET, baseline condition is 600 °C for 1 min in N_2 (20000 sccm)
    d) For p-channel MOSFET, baseline condition is 550 °C for 1 min in N_2 (20000 sccm)
14. Optical microscope inspection
    a) Alignment marker will be slightly damaged due to the high temperature annealing, however, it is still visible for alignment purpose

b) Can be optimized using alternative metals (e.g., TiN) or process flows (e.g., deposit encapsulation layer first → etching encapsulation layer in alignment marker region → deposit metal)

Part III: Gate Dielectric Stack

15. Encapsulation layer removal
    a) Dip into dilute HF (100:1) for 5 min to fully remove SiO_2 layer, long time etching can damage the InGaAs surface
    b) Rinse in DI H_2O for 2 min
16. Surface treatment
    a) Dip into 29% NH_4OH solution for 1 min immediately after encapsulation layer removal
    b) Rinse thoroughly in DI H_2O for 1 min
    c) Dip into 10% $(NH_4)_2S$ solution for 20 min
    d) Rinse thoroughly in DI H_2O for 1 min and flushing with flowing DI H_2O for 3 times
    e) Dry with N_2 gun
17. ALD DEZ interface passivation and gate dielectric deposition
    a) Within 3-5 min after surface treatment, load the sample into the Cambridge Nanotech S100 thermal ALD reactor
    b) In situ ALD DEZ passivation using DEZ pulse/purge sequence of 0.1/10 s for 10 cycles at 150 °C

c) Without breaking the vacuum, waiting for 10 min to heat up to 200 ℃, deposit 5 nm ALD-$Hf_{0.5}Zr_{0.5}O_2$ using 25 super-cycles (0.2/20/0.05/10 s+0.2/20/0.05/10 s)

d) Take out the sample and blow off the particles with N_2 gun

Part IV: Gate Metallization

18. Lithography

    a) Spin negative PR nLOF 2020 at 3000 RPM

    b) Bake at 115 ℃ for 60 s

    c) Mask set: InGaAs Gate

    d) Vacuum contact mode exposure with dose of 65 mJ/cm^2 using i-line

    e) Post exposure bake at 115 °C for 60 s

    f) Develop with AZ300 MIF developer for 60 s

    g) Rinse with DI H_2O and dry with N_2 gun

19. Optical microscope inspection

    a) To make sure no misalignment of the gate finger and alignment marker

20. Gate metal deposition using e-beam evaporator

    a) Pd/Au 20 nm/100 nm (or TiN for future tests)

    b) Base pressure below 5×10^{-6} Torr

21. Lift off

    a) Dip into heated AZ400T PR stripper (80 ℃) for 15 min

    b) Spray and rinse in acetone and IPA to remove any residue

    c) Dry with N_2 gun

22. Optical microscope inspection

    a) To check alignment marker and any metal or PR residue

    b) If needed, do additional acetone cleaning using an airbrush

Part V: Source/Drain Contact and Backside Contact

23. Lithography

    a) Spin negative PR nLOF 2020 at 3000 RPM

    b) Bake at 115 ℃ for 60 s

    c) Mask set: InGaAs Ohmic

    d) Hard contact mode exposure with dose of 65 mJ/cm^2 using i-line

    e) Post exposure bake at 115 °C for 60 s

    f) Develop with AZ300 MIF developer for 60 s

    g) Rinse with DI H_2O and dry with N_2 gun

24. Optical microscope inspection

    a) To make sure no misalignment with the gate finger and alignment marker

25. Contact window open

    a) Etching ALD dielectric in dilute HF (100:1) or BOE

    b) 10 nm ALD Al_2O_3 for 30 s, 5 nm $H_{0.5}fZr_{0.5}O_2$ for 1 min 40 s−2 min, please use oxide on Si monitor coupons for reference

    c) Rinse with DI H_2O and dry with N_2 gun

26. Ohmic contact metal deposition using e-beam evaporator

    a) Ni/Ge/Au 20 nm/20 nm/100 nm for n-channel or p-channel MOSFET

b) Base pressure below 5×10^{-6} Torr

27. Lift off

a) Dip into heated AZ400T PR stripper (80 °C) for 15 min

b) Spray and rinse in acetone and IPA to remove any residue

c) Dry with N_2 gun

28. Optical microscope inspection

a) To check alignment marker and any metal or PR residue

b) If needed, do additional acetone cleaning using an airbrush

29. Backside contact

a) The InP substrate backside was gently scratched by a diamond scribe, blow off the particles using N_2 gun

b) Immediately load sample into e-beam evaporator for Ti/Au 20 nm/200 nm deposition.

30. Post metallization annealing (PMA)

a) Use InGaAs annealing Si carrier wafer at MPTC RTP-600 (TR02)

b) Dummy run with the process recipe for one or two times

c) Anneal at 300 °C in a forming gas (95% N_2/5% H_2) ambient for 5 min

31. Complete fabrication and do electrical characterization

APPENDIX B

GAN HEMT GENERAL PROCESS FLOW

[1] Ohmic Contact → [2] Mesa Isolation → [3] Gate Dielectric Stack → [4] Gate Metallization

Part I: Ohmic Contact

1. Solvent Cleaning
    a) Acetone cleaning of the coupons using an airbrush
    b) Dip into acetone for 3 min
    c) Dip into methanol for 1 min
    d) Dip into IPA for 1 min
    e) Dry with N_2 gun
2. Oxide Layer Cleaning
    a) Dip into 10:1 HF for 5 min
    b) Rinse with DI H_2O for 3 min
    c) Dry with N_2 gun
3. Lithography
    a) Spin negative PR nLOF 2020 at 3000 RPM
    b) Bake at 115 °C for 60 s
    c) Mask set: GaN HEMT Ohmic
    d) Hard contact mode exposure with dose of 65 mJ/cm^2 using i-line
    e) Post exposure bake at 115 °C for 60 s
    f) Develop with AZ300 MIF developer for 60 s

g) Rinse with DI H_2O and dry with N_2 gun

4. Optical microscope inspection
5. Barrier recess
    a) PE03 Plasma-Therm Chlorine Etcher
    b) Recipe name: JG_GaN_BCl_3Cl_2_Ohmic Recess
    c) BCl_3/Cl_2=2/18 sccm, ICP RF 300 W, bias 5 W, 50 s, 5 mTorr, 20 °C
    d) Run 50 s dummy process prior to loading the samples
6. Optical microscope inspection
7. Cleaning
    a) Dip into HCl: H_2O (1:1) solution for 1 min
    b) Rinse with DI H_2O for 1 min and dry with N_2 gun
8. Ohmic metal stack deposition using e-beam evaporator (Cryo).
    a) Load the sample into the chamber immediately after HCl cleaning
    b) Deposit Ti 500 Å/Al 2000 Å/Ni 500 Å/ Au 1000 Å, monitored by QCM
    c) Base pressure below 5×10^{-6} Torr and tool factor (TF) 64%

    Note: actual thickness is about half of the target thickness by profilometer.
9. Lift off
    a) Dip into acetone or heated AZ400T PR stripper (80 °C) for 15 min
    b) Spray and rinse in acetone and IPA to remove any residue
    c) Dry with N_2 gun
10. Optical microscope inspection
    a) If needed, do acetone cleaning using an airbrush and IPA rinse

11. Rapid thermal annealing (RTA)
    a) To warm up lamp and purge moisture and O_2, run dummy process twice prior to loading samples
    b) Load samples on the GaN annealing Si carrier wafer and run the recipe named "YCByun_N_2_830 °C"
    c) Anneal at 830 °C for 30 s, N_2 20000 sccm
12. Optical microscope inspection
    a) The metal surface is rough due to the formation of alloyed metal contact
13. Check TLM and S/D current level to confirm the contact performance

Part II: Mesa Isolation

14. Solvent Cleaning (optional)
    a) Dip into acetone for 3 min
    b) Dip into methanol for 1 min
    c) Dip into IPA for 1 min
    d) Dry with N_2 gun
15. SiN hard mask deposition
    a) Load "LSNIT" recipe in PD01 PECVD, run at 250 °C for 30 min
    b) Check SiN thickness on blank Si using ellipsometer
    c) Thickness is approximately 300-350 nm and refractive index is 1.81-1.82
16. Lithography
    a) Spin positive PR S1813 at 3000 RPM

b) Bake at 115 ℃ for 60 s

c) Mask set: GaN HEMT MESA

d) Hard contact mode exposure with dose of 130 mJ/cm^2 using g-line

e) Develop with MIF 319 developer for 60 s

f) Rinse with DI H_2O and dry with N_2 gun

17. Optical microscope inspection

18. Plasma etching of SiN

a) PE05 Plasma-Therm III-V Etcher

b) Recipe "PECVD SiN Etch_Xin Meng"

c) SF_6 50 sccm, ICP RF power 500 W, bias power 50 W, 5 mTorr, 25 ℃

d) Dummy run 2 min with carrier wafer for chamber conditioning

e) Confirm etch rate (80-100 nm/min) by etching SiN/Si monitor sample for 2 min

f) Typical etching time 5 min (2+2+1) in total to ensure the complete removal of SiN

19. Optical microscope inspection

20. PR removal

a) Dip into acetone or heated AZ400T PR stripper (80 ℃) for 15 min

b) Spray and rinse in acetone and IPA to remove any residue

c) Dry with N_2 gun

21. Optical microscope inspection

a) If needed, do additional acetone/AZ400T cleaning or O_2 plasma PR descum

22. Plasma etching of AlGaN/GaN layers

a) PE03 Plasma-Therm Chlorine Etcher

b) Recipe name: JG_GaN_BCl_3Cl_2_MESA

c) BCl_3/Cl_2=2/18 sccm, ICP RF 350 W, bias 10 W, 750-900 s, 5 mTorr, 20 °C

d) Run 10 min dummy process prior to loading the samples

Note: dry etch rate of SiN hard mask layer is ~10 nm/min

23. Dip into acetone (1 min) and IPA (1 min)
24. Check etch step height using profilometer in the cleanroom Bay 5
25. Remove SiN hard mask using 100:1 HF for 5 min and rinse with DI water for 1 min
26. Check etch step height using profilometer in the cleanroom Bay 5
    a) Typical step height is 400-500 nm for 750 s etching.
27. Measure TLM, S/D I-V, and buffer leakage current.

Part III: Gate Dielectric Stack

28. Surface cleaning
    a) Dip into 100:1 HF for 3 min
    b) Rinse thoroughly in DI H_2O for 1 min and flushing with flowing DI H_2O for 3 times
    c) Dry with N_2 gun
29. Gate dielectric deposition (skip this step for Schottky gate devices)

Part IV: Gate Metallization

30. Lithography
    a) Spin negative PR nLOF 2020 at 3000 RPM
    b) Bake at 115 °C for 60 s

c) Mask set: GaN-HEMT Gate

d) Vacuum contact mode exposure with dose of 65 mJ/cm^2 using i-line

e) Post exposure bake at 115 °C for 60 s

f) Develop with AZ300 MIF developer for 60 s

g) Rinse with DI H_2O and dry with N_2 gun

31. Optical microscope inspection

    a) To make sure a clear pattern of the gate finger and no misalignment

32. Gate metal deposition using e-beam evaporator (Cryo)

    a) Ni/Au 40 nm/100 nm

    b) Base pressure below 5×10^{-6} Torr

33. Lift off

    a) Dip into heated AZ400T PR stripper (80 °C) for 15 min

    b) Spray and rinse in acetone and IPA to remove any residue

    c) Dry with N_2 gun

34. Optical microscope inspection

    a) To check alignment marker and any metal or PR residue

    b) If needed, do additional acetone cleaning using an airbrush

35. Complete fabrication and do electrical characterization

36. Post metallization annealing (PMA, optional)

    a) Load the sample into quartz boat (GaN and III-V only)

    b) Anneal the samples in the Minibrute #2 tube furnace (general purpose) at 400 °C for 15 min in N_2 ambient (4 liters).

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· Xin Meng, Si Joon Kim, Young-Chul Byun, Jae-Gil Lee, Jiyoung Kim, Epitaxial Growth of ZnO Layer on AlGaN/GaN Heterostructure via Atomic Layer Deposition, XXVI International Materials Research Congress, Cancun, Mexico, August 20-25, 2017.

· Xin Meng, Si Joon Kim, Jae-Gil Lee, Young-Chul Byun, Jiyoung Kim, In-situ ALD Diethylzinc (DEZ) surface passivation on $In_{0.53}Ga_{0.47}As$ MOS Devices, XXVI International Materials Research Congress, Cancun, Mexico, August 20-25, 2017 (poster).

· Xin Meng, Young-Chul Byun, Jae-Gil Lee, Harrison S. Kim, Joy S. Lee, Antonio T. Lucero, Lanxia Cheng, Jiyoung Kim, Investigation of High-quality Silicon Nitride (SiN_x) Thin Film Grown by Low-temperature Hollow Cathode Plasma-Enhanced ALD as a Gate Dielectric for AlGaN/GaN MIS-HEMTs, 17th International Conference on Atomic Layer Deposition, Denver, Colorado, USA, July 15-18, 2017.

· Xin Meng, Young-Chul Byun, Jae-Gil Lee, Jiyoung Kim, Effects of surface treatments on the electrical characteristics of AlGaN/GaN MOS capacitors using ALD grown epitaxial ZnO as interfacial gate dielectric, 2017 TMS Annual Meeting & Exhibition, San Diego, California, USA, Feb 26-Mar 2, 2017.

· Harrison Kim, Young-Chul Byun, Xin Meng, Jiyoung Kim, Byung Keun Hwang, FT-IR Investigation of H Content in SiN_X Thin Film Grown by PEALD Using HCDS as Precursor; Achieving Low WER, 2017 TMS Annual Meeting & Exhibition, San Diego, California, USA, Feb 26-Mar 2, 2017.

· Antonio Lucero, Lanxia Cheng, Joy S. Lee, Jaebeom Lee, Xin Meng, Arul Ravichandran, Young-Chul Byun, Jae-Gil Lee, Jiyoung Kim, Novel in Situ Electrical Characterization of the Dielectric Deposition Process on 2-D Transition Metal Dichalcogenides, 2017 TMS Annual Meeting & Exhibition, San Diego, California, USA, Feb 26-Mar 2, 2017.

· Antonio T. Lucero, Lanxia Cheng, Joy S. Lee, Jaebeom Lee, Xin Meng, Arul Ravichandran, Dushyant Narayan, Young-Chul Byun, Jaegil Lee, Jiyoung Kim, The effects of ALD and PEALD processing on 2D transition metal dichalcogenide devices: in-situ electrical characterization. 16th International Conference on Atomic Layer Deposition, Dublin, Ireland, July 24-27, 2016 (poster).

· Young-Chul Byun, Antonio T. Lucero, Xin Meng, Lanxia Cheng, Jiyoung Kim, Dipole Engineering for Controlling V_{th} on AlGaN/GaN Using ALD Metal Oxides, 15th International Conference on Atomic Layer Deposition, Portland, Oregon, USA, June 28-July 01, 2015 (poster).

· Young-Chul Byun, Antonio T. Lucero, Xin Meng, Arul Ravichandran, Lanxia Cheng, Jiyoung Kim, Low Temperature ALD-ZrO2 Films using TDMA-Zr and O_3, 2015 TMS Annual Meeting & Exhibition, Orlando, Florida, USA, March 15-19, 2015.