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Performance and stability of solution-based cadmium sulfide thin film transistors: Role of CdS cluster size and film composition

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Improved carrier mobility and threshold voltage (V_T) stability in cadmium sulfide (CdS) thin film transistors (TFTs) were studied and attributed to larger grain clusters in thicker CdS films rather than individual crystallite size. Non-zero V_T shifts (~200 mV) in thicker films are attributed to the presence of cadmium hydroxide [$Cd(OH)_2$] at the dielectric/CdS interface resulting from the chemical bath deposition process used to deposit the CdS films. V_T and mobility analyses indicate that clusters of CdS grains have a larger impact on TFT performance and stability than the presence of impurities in the bulk of the CdS. TFTs using this fabrication method achieved mobilities of ~22 cm^2/Vs with V_T of 7 V and ΔV_T of <200 mV after testing. The maximum processing temperature is 100 °C which makes this process compatible with flexible substrates. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4773184]

A relatively simple fabrication procedure, low deposition temperature, and the possibility to use virtually any substrate makes chemical bath deposited cadmium sulfide (CdS) semiconducting films attractive for the fabrication of thin film transistors (TFTs) for large area applications. Although CdS TFT performance is better than a-Si:H, its electrical stability is not well understood. However, to enable the design of stable circuits, the TFTs must be electrically stable when subjected to many operating cycles under atmospheric conditions and standard electrical bias. Several studies have reported the stability behavior of multiple types of TFTs.[1–11] In organic TFTs, a pronounced shift in the threshold voltage (V_T) under negative gate bias stress has been reported and identified as hole bipolaron formation.[2] Instabilities due to the movement of mobile ions under electrical stress have also been reported.[3,4] Variation in mobility (μ) due to the oxidation of the semiconductor layer and V_T shift induced by trap sites at grain boundaries and the interface between the semiconductor layer and the gate dielectric surface have also been reported.[5] Inorganic TFTs, such as hydrogenated amorphous Si (*a*-Si:H) TFTs, are also plagued by low electron mobility (~1 cm^2/V s) and well-known instabilities with respect to bias stressing[6] during light exposure.[7] TFTs based on amorphous oxide semiconductors, such as InGaZnO, are being used due to their higher electron mobility.[8] Accurate and repeatable control of this complex material in mass production can be difficult and requires ultra-high vacuum deposition equipment.[9] In order for ZnO-based TFTs to become pervasive, it is also crucial to overcome the problems of voltage dependent stability and reliability.[10] Previously, we reported on CdS TFTs with high mobility fabricated using a shadow mask process[11] as well as an approach to integrate CdS and pentacene transistors using photolithography to demonstrate CMOS circuits fabricated at temperatures below 100 °C.[12]

In this letter, we describe several factors that impact performance and V_T stability of CdS-based TFTs fabricated using chemical bath deposition (CBD). In particular, we studied the impact of CdS cluster size evolution and the influence of $Cd(OH)_2$ and $CdCN_2$ impurities on the stability and performance of TFTs fabricated with the resulting CdS films. The CdS clusters are made up of multiple CdS crystals agglomerating together. We determined that mobility is highly sensitive to cluster size and not directly related to individual CdS grain size. This behavior is different to other systems where an increase in grain size results in increased mobility.[13–15] Grain boundaries can act as charge traps. Typically, improved TFT performance observed in some systems is generally associated to an increase in grain size. It has been reported that when the grain size is above a critical value, the carrier mobility is relatively independent of the crystallite size.[14] No reports on the effect of cluster size in these systems were found in the literature. For the CdS films reported here, there is no change in the individual CdS crystal size as function of film thickness. However, there is an increase in the cluster size as the film thickness increases, resulting in improved carrier mobility. We also identified $Cd(OH)_2$ at the dielectric/semiconductor interface as responsible for the non-zero V_T shift observed in the CdS films. $CdCN_2$ impurities have a minimal impact on V_T instability and mobility.

The CdS-TFTs studied here were fabricated in a bottom-gate, top-contact configuration. All devices were fabricated on a heavily doped silicon wafer (p-type: boron; <0.005 Ω cm), which is also used as gate electrode. A 90-nm thick HfO_2 dielectric film was deposited using atomic layer deposition (ALD) and the CdS semiconducting active layer was immediately deposited using a cadmium chloride/sodium citrate/thiourea system at 70 °C, described elsewhere.[11,12]

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After deposition, the CdS films were cleaned in an ultrasonic bath with methanol, rinsed with distilled water, and then dried with N_2 gas. In order to grow the CdS films with different thicknesses, the deposition process was repeated five consecutive times with fresh solutions used for every deposition.[16] The deposition time was approximately 25 min for each deposition. For source/drain electrodes, 100 nm aluminum was deposited by e-beam through a shadow mask on top of the semiconductor layer. Channel width (*W*) and channel length (L) were 500 μm and 40 μm, respectively. Scanning electron microscopy (SEM) was performed to evaluate the morphological differences as a function of CdS thickness. Fourier transform infrared (FTIR) spectroscopy studies were used to investigate the chemical composition and to identify the presence of hydroxyl groups and/or any other species present in the resulting CdS films. Electrical characteristics of the TFTs were evaluated using current–voltage (*I-V*) measurements at room temperature with a 4200 Keithley semiconductor characterization system under dark conditions. The saturation and linear transfer curves were measured by applying a V_{DS} voltage of +20 V or +1 V, respectively. The gate voltage was swept from −5 V to +20 V. The electrical measurement sequence used in this letter is described as follows; first, the (I_D-V_G) characteristics were measured three consecutive times, followed by the output characteristic (I_D-V_D) measurements. Then, the same (I_D-V_G) sequence was used again to evaluate the V_T stability of the CdS-TFTs. We note that after the second I_D-V_G sweep, the threshold voltage shows no substantial changes. Although no V_T shift is observed after the 2nd swept, the V_T shift reported here is extracted from the V_T change between the 1st and 6th I_D-V_G measurement.

The evolution of the CdS surface morphology was analyzed as a function of film thickness. Figure 1 shows SEM images of the CdS films as function of thickness. There is a clear monotonic increase in cluster size as the thickness of the CdS films increases from 25 nm to 130 nm. This is expected since additional CdS growth time leads to larger clusters with the concomitant reduction in cluster boundary density.[7–9,17] SEM was used to evaluate the cluster size. We note that these clusters are constituted by CdS crystallites of ~22 nm and that the crystallite size remains constant throughout the entire CdS thickness evaluated, as shown later in this letter.

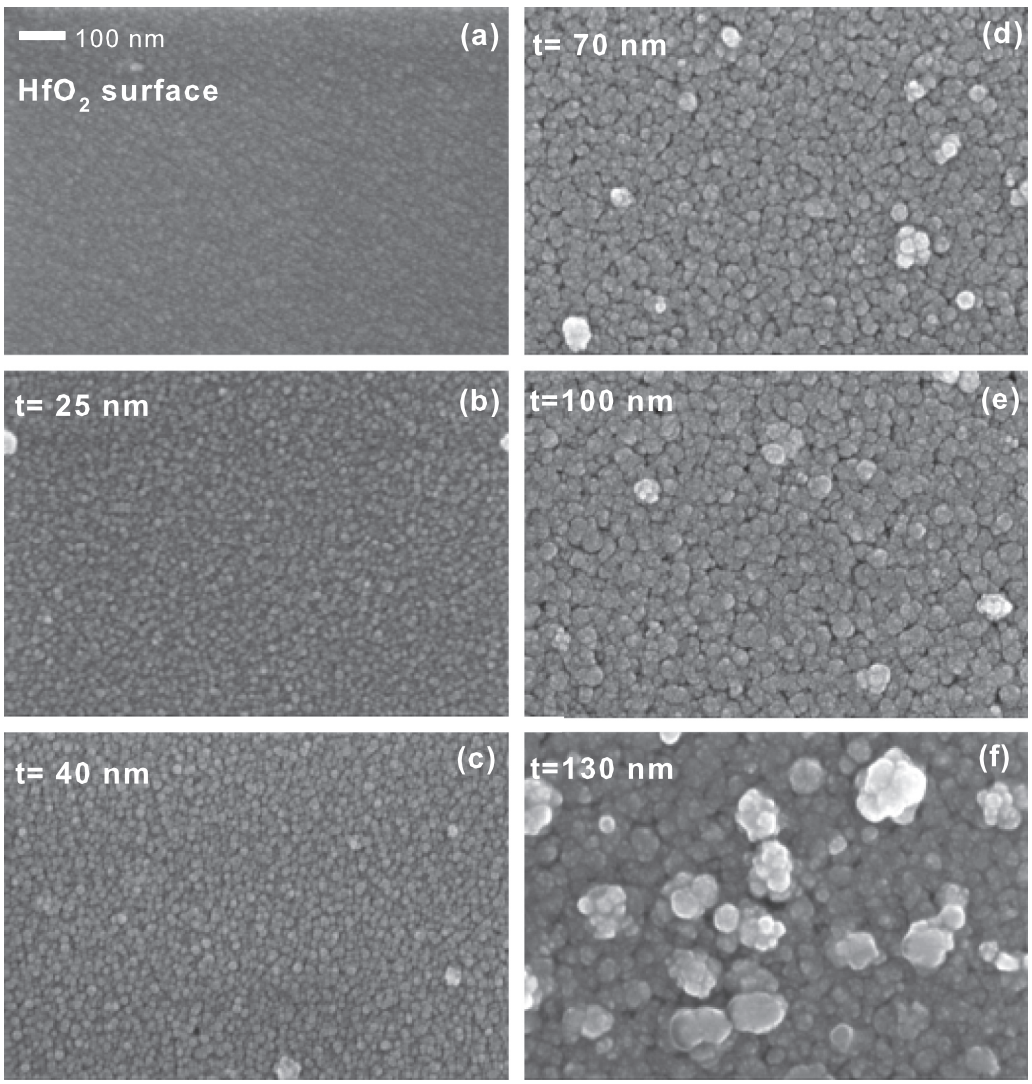

FIG. 1. SEM images of the CdS samples showing how the cluster size increases by increasing the CdS film thickness where (a) ALD HfO_2 layer, (b) t = 25 nm CdS, (c) t = 40 nm CdS, (d) t = 70 nm CdS, (e) t = 100 nm CdS, and (f) t = 130 nm CdS. t refers to CdS film thickness.

Device stability was investigated by measuring the change in V_T after consecutive I_D-V_G sweeps. The CdS-TFT structure used for these studies is shown in the inset of Figure 2(a). Figure 2(a) shows the gate current and the typical shifts observed in the transfer characteristics of the CdS–TFTs. The data shown in Figure 2(a) correspond to 100 nm thick CdS. The V_T shift was extracted between the 1st and the 6th sweep (no additional V_T shift was observed after the 6th sweep). Field-effect mobility (μ_{sat}) was calculated from the last sweep using the slope of the linear portion of the $I_D^{1/2}$ vs. V_G curve. The following equation was used for the calculations:[18]

$$I_D = \frac{W}{2L} C_i \mu_{sat} (V_G - V_T)^2, \quad (1)$$

where V_G is the gate voltage, W is the channel width, L is the channel length and C_i is the capacitance per unit area of the gate dielectric.

Leakage current remains low ($\sim 10^{-11}$A) for these devices regardless of the thickness of the CdS film (Figure 2(a)). Mobilities were as high as 22.0 cm^2/V s for the thicker films and as low as 1.2 cm^2/V s for the thinnest CdS films. Threshold voltage shifts are typical for organic and inorganic low temperature TFTs devices.[1–7,19] Gundlach[19] and Ismail[20] refer to these large initial shifts as an irreversible V_T shift because V_T does not recover to its initial value after several minutes. It is important to note that the initial V_T shift must be considered when extracting device parameters from the transfer curves. In the case of the devices described here, μ_{sat} is extracted from the last measurement, where the transfer curve remains stable.

Figure 2(b) shows the evolution of mobility, CdS cluster (■) and grain size (□) with film thickness. The inset in Figure 2(b) shows that the V_T shift decreases as the CdS thickness increases. Figure 2(b) also shows that there is a monotonic increase in cluster size with thickness. Therefore, thinner films have smaller clusters, which result in a higher density of cluster boundaries that act as charge traps. Hence, the higher V_T shift in thinner films is likely due to the higher density of cluster boundaries. The increase in mobility with CdS thickness observed in Figure 2(b) is also consistent with the increased cluster size. Cluster boundaries act as additional sites that scatter charge carriers. Larger cluster sizes result in a lower number of cluster boundaries, i.e., less scattering sites; thus, an increasing mobility is observed.[13–15] It is important to note that the CdS crystallite size, as determined using XRD, remains constant with film thickness as can shown in Figures 2(b) and 3(a). The large difference in intensity of the (002) peak is due to the thickness difference. This clearly indicates that the CdS cluster size has a larger impact on device performance and stability. Next, we evaluated the impact of impurities resulting from the CBD process.

Bulk defects in the CdS are likely to be present in the CdS films as a result of the CBD deposition process.[21–24] To study the presence of impurities in the CdS films, FTIR analyses were carried out using a Nicolet 6700: Thermo Fisher Scientific Inc., spectrometer in the range of 4000–400 cm^{-1}. Each spectrum was obtained using 500 scans with 4 cm^{-1} resolution. The FTIR spectra of the CdS thin films are shown in Figure 3(b). The broad absorption band in the range from 3600 to 3000 cm^{-1} is attributed to OH^- stretching.[21] C-H bonds are also observed at $\sim$2950 cm^{-1}. The peak at 2400 cm^{-1} is attributed to S-H stretching. This S-H bond is only observed in thicker CdS films suggesting that is likely present in the bulk of CdS film. The CBD technique is an alkaline aqueous solution; therefore, the solution contains OH^- ions. Thus, the presence of OH^- in the FTIR results is not unexpected. Since no increase in the OH^- peak with film thickness (Figure 3(b)) is observed, it is likely that this OH^- is located at the interface between the dielectric and the CdS

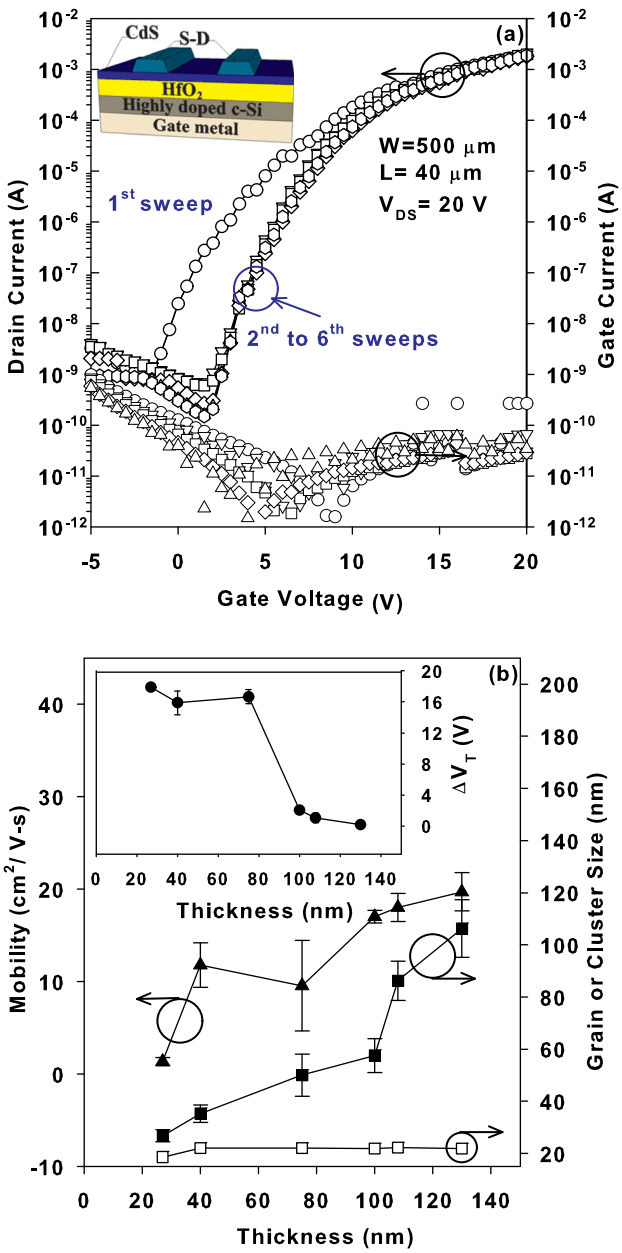

FIG. 2. (a) I_D-V_G transfer characteristics showing V_T shift between the 1st and 6th sweep for 100 nm CdS TFTs measured in the saturation regime (V_{DS} = 20 V). Inset shows a schematic cross section of the transistor used in this analysis. (b) Dependence of mobility (μ_{sat}), cluster (■), and grain size (□) with CdS film thickness. Grain size is independent of CdS film thickness, as determined by XRD. Inset shows threshold voltage (ΔV_T) shift reduction as function of CdS film thickness (nm).

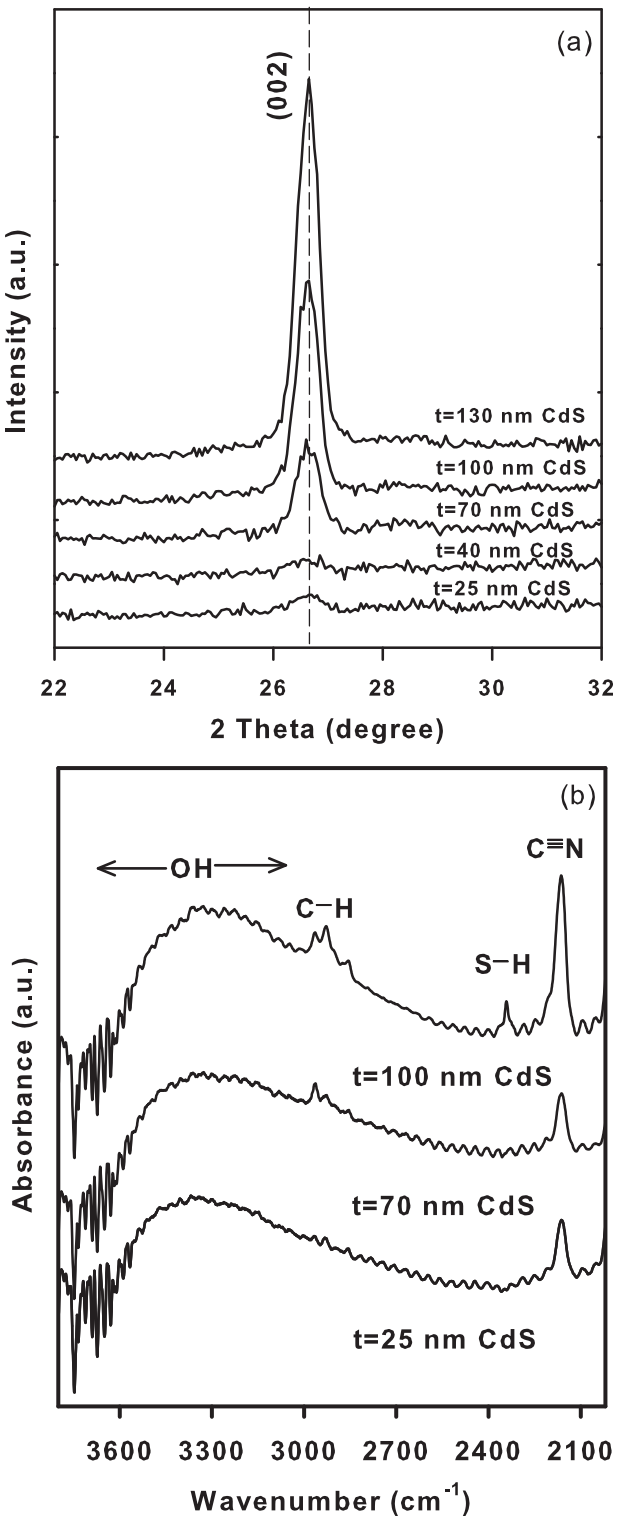

FIG. 3. (a) XRD spectra for different thickness of the CdS films show an increased intensity for thicker films. (b) FTIR absorption spectra of CdS film of different thicknesses showing three region: 3600–3000 cm^{-1} attributed to OH^- stretching at the dielectric/CdS interface, 2200 cm^{-1} attributed to the C-N stretching vibrations of cyanamide in the bulk of the CdS film, and 2400 cm^{-1} attributed to S-H in the bulk of the CdS films.

films. The presence of OH^- at the interface will generate interface traps with the associated shift in V_T.

The peak at about 2200 cm^{-1} is attributed to the carbon-nitrogen (C-N) stretching vibrations of cyanamide or thiocyanate.[21–24] Some groups have also proposed cadmium cyanamide, $CdCN_2$, as a possible impurity phase in the CBD grown CdS films,[21–24] which could be understood from the decomposition reaction of thiourea during the initial stages of the CBD as follows:

$$SC(NH_2)_2 + 2OH^- \rightarrow S^{2-} + CdCN_2 + 2H_2O, \quad (2)$$

which in the presence of excess thiourea in the latter stages of the deposition undergoes the heterogeneous reaction

$$CdCN_2 + S^{2-} \rightarrow CdS + CN_2^{2-}, \quad (3)$$

where S^{2-} is provided by the thiourea hydrolysis in the alkaline solution. This reaction has been proposed for the growth of CdS thin films by CBD.[21–24] From Figure 3(b), we can observe that there is a monotonic increase in the C-N bonding with the increase of the CdS film thickness, also suggesting its presence in the bulk of the CdS. The C-N groups are likely resulting from the excess of thiourea used in the CBD reaction reported here. Since V_T shift reduces with increasing CdS film thickness, we can conclude that the presence of the C-N bonds does not directly affect the V_T shift. However, the non-zero shift of V_T in our devices, even for thick CdS films, can be attributed to hydroxyl groups at the dielectric/CdS interface.

In summary, high mobility (~22 cm^2/V s) and low V_T (1.3 V) is achieved in TFTs fabricated using solution-based CdS films. Mobility and V_T stability are improved in thicker CdS films due to a larger cluster size. A larger V_T shift in thinner films is attributed to smaller clusters with the concomitant increase in cluster boundary density. C-N groups in the bulk of the CdS films have a reduced role in film performance and stability, whereas the residual V_T shift in thicker films (200 mV) is attributed to the presence of $Cd(OH)_2$ at the interface between the dielectric and CdS.

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