CONDITION MONITORING FOR DISCRETE PACKAGED INSULATED GATE BIPOLAR TRANSISTORS IN POWER CONVERTERS

by

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Dedicated to my wife, sister, father and late mother

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by

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Extensive utilization of insulated gate bipolar transistor (IGBTs) in the power converters has significantly increased concerns over its reliability. Failure of such critical component eventually cause unexpected shut downs and even lead to catastrophic faults resulting in huge economic loss. So, tools for incipient fault diagnosis and aging prognosis have to be utilized for reducing the risk of faults and accidents. Yet, established tools are not mature enough and there exist a major reliability gap exist in condition monitoring of IGBTs. In order to improve current prognostic and diagnostic tools, this dissertation investigates ongoing aging induced degradation and corresponding shifts in electrical parameters for IGBTs. Such useful electrical parameters are referred as aging precursors which are obtained after extensive thermal aging tests. Based on the aging test results, aging precursors are identified and an in-situ condition monitoring circuit has been proposed as well. Due to low component count, the proposed circuit is cost effective and can be easily integrated to conventional gate driver circuits. Based on the data measurements, further remaining useful lifetime estimation for IGBTs have been carried out as well. It is conceived that such tools lay foundations for smart-energy conversion systems which

are self-capable in evaluating the degradation information using aging precursors to prevent imminent failures in the system. Briefly, this dissertation discusses:

- identification and characterization of aging precursors,
- development of innovate and easy-to-integrate condition monitoring circuit
- development of remaining useful lifetime estimation tool based on the monitored data for advancing smart power conversion systems.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Today, the growing demands of energy consumption require efficient and reliable sources of energy delivery and power conversion. In this connection, most modern power electronic converters utilize efficient active and passive components, pioneering circuit design techniques and sophisticated system integration methods. Yet, with high degree of dependence on power converters for energy conversion in our daily lives, their reliability is a major concern.

Considering the example of renewable energy based power generation systems, five years of maintenance data for different installed PV systems has been presented in [1]. Based on the data, it has been highlighted that inverters are the most failing sub-system beside data acquisition systems (DASs), ac disconnects (ACDs), PV system and other components as shown in Figure 1.1. In a separate power electronics industry wide survey, it has been concluded that power switching devices are one of most frequently failing components in power converters behind capacitors as shown in Figure 1.2 (a) [2]. Understandably, as their operation could cease without the switching devices, early failure and aging discovery in switching devices is crucial for their reliable operation for incessant power delivery.

1.2 Background

Predominantly, insulated gate bipolar transistors (IGBTs) are the most widely used switching devices for low and medium power level power converters in renewable energy systems, hybrid electric vehicles and industrial motor drives etc. as shown in Figure 1.2 (b) [2]. During

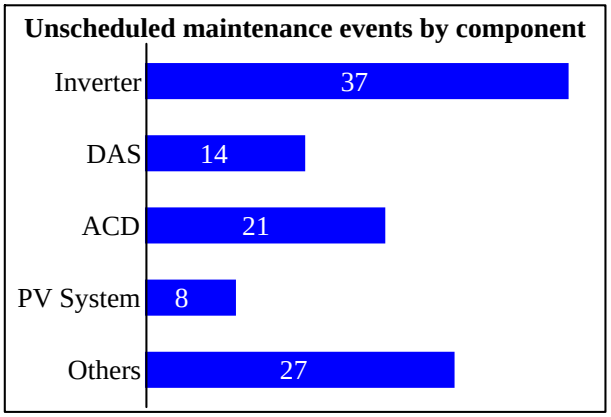


Figure 1.1. Percentage distribution of reported sub-system failure events in PV systems.

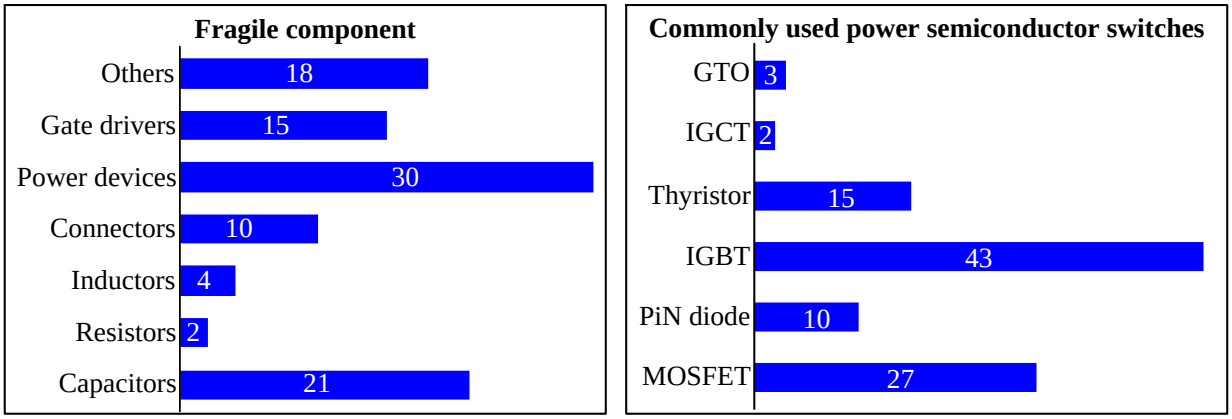


Figure 1.2. Industry wide survey regarding reliability concerns in power converters; (a) distribution of failure prone components and (b) share of different power semiconductor devices.

operational life, IGBTs may undergo severe on-field stresses triggering different aging mechanisms which can lead to catastrophic failures. Among different stress types, high cyclic temperature has been shown as the highest contributor to device aging in Figure 1.3 [3].

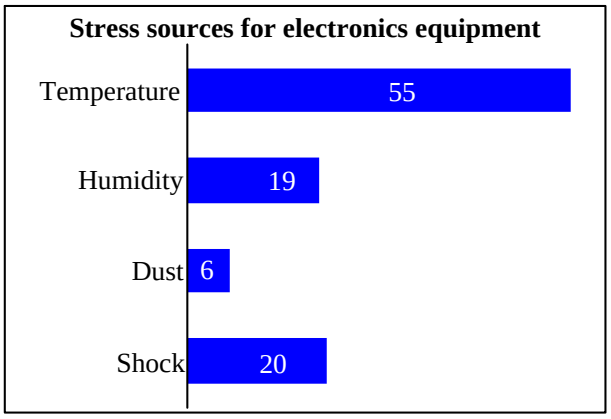


Figure 1.3. Sources of stress for power electronic systems.

Several reliability studies have been performed and different statistical models have been presented for analyzing device aging as well. Yet, operational conditions are often unpredictable and comprehensive testing for different scenarios is required to improve statistical models for estimating aging and imminent failures in devices. Furthermore, high degree of variability in device specification also exists among different batches so, lot of effort is required to test and estimate failure time for different applications.

1.3 Problem Description

Today, IGBT is considered to the industry's workhorse for switching power. At the same time, it is prone to high degree of wear and aging within the power converters as it suffers from induced thermomechanical and electrical stress during its operation. Its rapid utilization has raised significant reliability concerns due to operational uncertainties and limited on-field data. Modern advanced controllers which monitor variety of power converters' electrical signals for control purposes but these controllers significantly lack in gathering reliability information about the

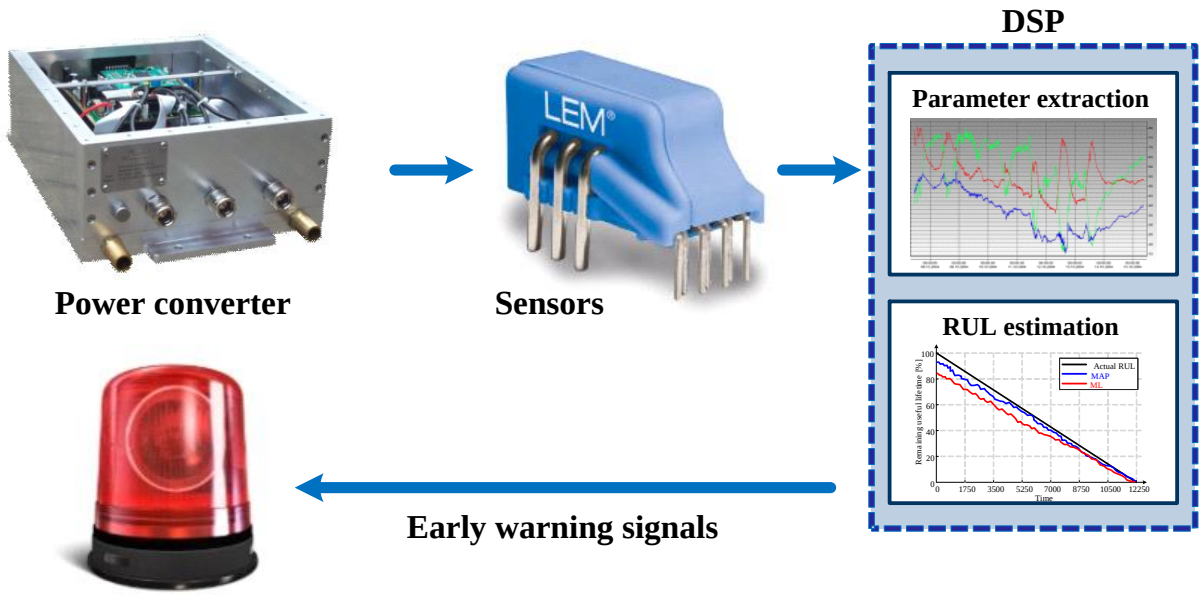


Figure 1.4. Proposed fault and aging detection system.

installed components particularly, IGBTs. The current state-of-art includes redundancy to avoid catastrophic failures and/ or protect the system after the failure. In order to move forward, a fault and aging detection system is needed which can monitor device aging, estimate its remaining useful lifetime (RUL) in the real-time based on prior aging test data for real-life operating conditions. The same has been illustrated in the Figure 1.4.

1.4 Aims and Objectives

The main objectives of this study have been summarized as following:

- To characterize electrical parameters using accelerated aging test beds at cyclic thermal stress to determine aging signatures or aging precursors.
- To develop on-line aging precursor monitoring tools for examining state-of-health of IGBTs within the power converters.

- To devise data driven approach for estimating the RUL of IGBTs based on the observed on-field aging precursors' information

1.5 Outline of the Dissertation

The chapter wise outline is given below:

- In Chapter 2, structural details for different types of discrete package IGBTs have been introduced. Also, the extrinsic, intrinsic failures and the associated aging mechanisms discussed in the literature are reviewed. Moreover, details for accelerated aging test setup are introduced and *i*-*V* characteristics results from aging test at variety of stress levels are presented. Furthermore, the underlying physical phenomena responsible for the parametric variations with respect to aging are investigated in the light of scanning acoustic microscope (SAM) analysis results.
- In Chapter 3, condition monitoring tools are introduced. A brief literature review about existing methods is presented as well. Based on the shortcomings in the existing methods, a novel circuit is presented. The proposed circuit is not only cost-effective but provides fast aging precursors monitoring in the order of microseconds and occupies small real estate on the printed circuit board (PCB). Furthermore, simulation and experimental results are presented as well to corroborate the efficacy of the proposed circuit.
- In Chapter 4, a data driven RUL estimation model based on Gaussian Process Regression (GPR) is presented. The model uses the IGBT's actual aging information instead of relying on junction temperature for RUL estimation. It takes the observed aging precursor information and estimates the RUL of aging sample device. It is shown through results

that by training the model using the aging test results from chapter 2, drastically improves the RUL estimation results compared to conventional algorithms.

- In Chapter 5, the summary of the dissertation is presented.

CHAPTER 2

IGBT DEVICE STRUCTURE AND AGING MECHANISMS

2.1 Power Semiconductor Revolution and IGBT

Since 1950, pnpn stacked layer silicon controlled rectifiers dominated the power electronics industry. Among the SCR family, Thyristor has been the most famous one. Although, Thyristor can provide both high voltage blocking (in kV) and high current conduction (in kA) capability but require additional control/ power circuit for its current commutation which restricts its widespread deployment. To some extent power bipolar junction transistor (BJT) for low voltage applications serve as good alternative but its high gate current driving requirements degrades the overall efficiency. Moreover, in order to sustain high blocking voltage (BV), BJT have been fabricated with low intrinsic gain (ratio of control input and power output).

In 1970's, the introduction of vertical power metal oxide silicon field effect transistor (MOSFET) ushered a new era in power electronics industry. Power MOSFET unlike the BJT is a majority carrier device and can switch significantly at higher speeds which have could not have been achieved using existing BJT technology. High switching speed limited only by parasitic capacitances enabled realization of various different circuit topologies. Power MOSFETs improved the system efficiencies without compromising the switching speeds only for low voltage applications. In order to sustain higher BV, thicker device need to be fabricated but at the cost of significantly higher conduction loss compare to that of BJT of the same die size. Thus, a newer type of device has been sought which can provide benefits from both devices.

In 1982, Baliga reported a new device named as insulated gate rectifier (IGR) which later became insulated gate bipolar transistor (IGBT) [4]. He combined the insulated gate FET for the input control and power BJT as a HV switch in one single device. IGBT actually filled the gap by providing much needed compromise between BJT and Power MOSFET device characteristics. An IGBT can provide high BV and conductivity modulation just like power BJT at higher power levels as well as require simpler gate drive circuits just like MOSFETs. Moreover, unlike power BJT, it can operate at higher switching frequencies as well.

Today, IGBT structural design, size and performance have improved significantly but still it resembles the same structure proposed by Baliga. Briefly, an IGBT device cell is constructed in a similar fashion as to an n-channel type double diffused vertical construction power MOSFET. The p+ collector layer replaces the n+ drain and is the major exception between the two devices. Thus, a vertical PNP bipolar junction transistor is formed whose base current is controlled by the n-channel FET. The n-channel is further controlled by providing suitable gate-emitter voltage above gate threshold voltage. An IGBT compared to the power MOSFET has

- bipolar device characteristics which means minority carriers are injected in to n-drift region to assist majority carrier transport allowing for higher current densities and require more time during transients (turn-on and turn-off times) and
- characteristic diode-voltage drop which increases logarithmically with respect to its current.

A brief comparison among power BJT, power MOSFET and IGBT is presented in Table 2.1. Further details about different IGBT structures are presented in the next section.

Table 2.1. General comparison table for few power semiconductor devices.

Characteristics	Thyristor	Power Bipolar	Power MOSFET	IGBT
Cost	Low	Low	Medium	High
Voltage rating	High above 10kV	Less than 1kV	Around 1.4kV	High above 2kV
Current rating	Around 10kA	< 500A	Around 500A	Around 1.5kA
Switching Speed	>500μs	>10μs	<10ns	<10μs
Control requirement	Complex commutation circuit	High continuous base current	Low gate current	Low gate current
Input Impedance	Low	Low	High	High
Output Impedance	Low	Low	Medium	Low

2.2 Commonly Used IGBT Device Structures

2.2.1 Punch-Through (PT) IGBT

Among the most successful device structures for IGBTs, punch-through (PT) IGBTs are the oldest surviving technologies introduced into the market. Its device manufacturing relies on depositing of a thin n+ layer (buffer layer) upon the p+ substrate. On top of n+ layer, a separate n-drift layer is grown by epitaxy process. Furthermore, similar to D-MOSFET double diffusion for p and n wells by ion implantation and/ or diffusion processes take place as well. Lastly, the emitter and gate metallization are formed.

The structure is called punch-through because the e-field can penetrate through the entire drift region and extend into the buffer layer during the forward blocking mode (absence of gate control voltage). The buffer layer captures the injected minority carriers from p+ substrate at

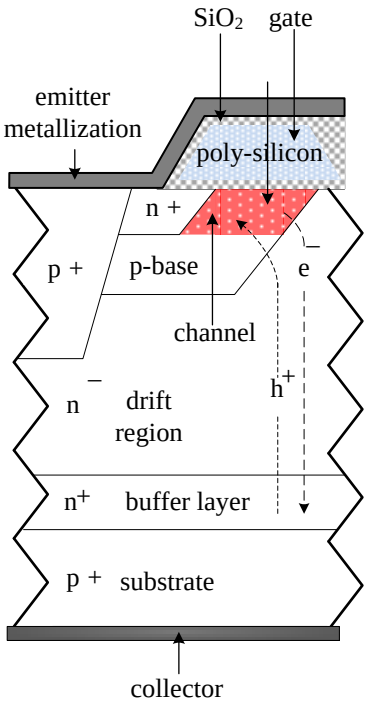


Figure 2.1. Structure for PT IGBT.

faster recombination rate than the drift layer thereby helps in reducing the switching time. Since, $V_{ce,on}$ is inversely proportional to higher recombination rate or shorter minority carrier lifetimes, the buffer layer thickness has to be adjusted accordingly. There exists another trade-off between the drift layer's thickness for sustaining higher blocking voltage and the associated conduction losses so it has to be controlled carefully during epitaxial growth.

2.2.2 Non-Punch-Through (NPT) IGBT

Non-punch-through (NPT) is another famous structure for IGBT. The main advantage with NPT is the positive temperature coefficient (tempco) of its $V_{ce,on}$ so, it can be easily paralleled for

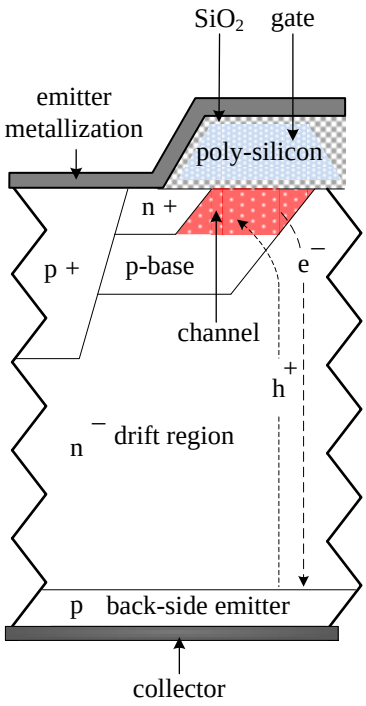


Figure 2.2. Structure for NPT IGBT.

higher current application without any complex thermal coupling mechanisms. Figure 2.3 shows the general structure of a typical NPT IGBT. Instead of p+ substrate, manufacturing of NPT IGBT starts with lightly doped n substrate which is lightly doped with acceptor (p-type) impurity to form collector. Similar to PT IGBT manufacturing, p and n wells are formed by ion implantation and/ or diffusion processes followed by gate and emitter metallization. Since thick n substrate is used to support high BV without punch through, expensive epitaxial buffer layer is not required. The absence of additional buffer layer for rapid sweeping of minority carriers thicker layer slightly degrades the turn-off characteristics and also thicker drift layer (substrate) increases the conduction losses.

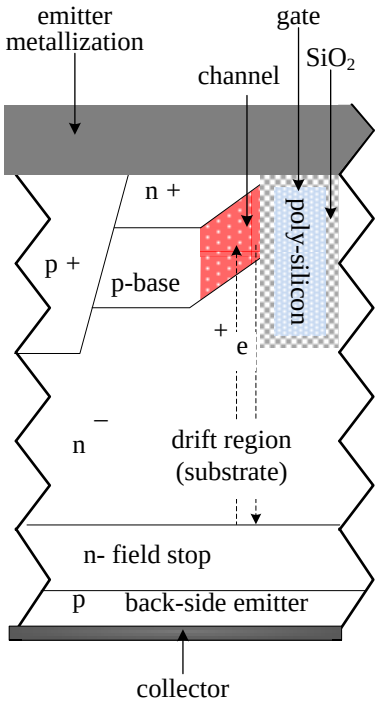


Figure 2.3. Structure for TGFS IGBT.

2.2.3 Trench Gate Field Stop (TGFS) IGBT

It is evident that PT provides lower switching and conduction losses whereas NPT has the beneficial positive tempco for easy paralleling option. So, different variants have been introduced over the time to utilize the benefits of both device structures. In this connection, trench gate field stop (TGFS) structure, is one of the most widely used device structure.

Its manufacturing is similar to NPT yet there are two major differences. The first and noticeable difference is gate structure. In the previous designs, the gate lies flat on top of the device substrate however, for TGFS, it is almost completely buried inside the deep well (or trench as the structure name suggests). The second difference is the n type field stop layer. The

Table 2.2. IGBT device technologies comparison.

Characteristics	PT	NPT	TGFS
Cost	Low	Lowest	High
Switching losses	Low	Highest (with no lifetime killing technique)	Lowest
Leakage current	High	Low	Lowest
$V_{ce,on}$	Low	High	Lowest
Tempco for $V_{ce,on}$	Negative	Positive	Positive
Chip size	Largest	Small	Smallest
Short-circuit protection	Low	High	Low

doping concentration in field stop layer is at least ten times lower to that found in the PT structure.

The main advantage of trench encapsulated gate is higher cell package ratio and removal of JFET effect by improved channel utilization and conductivity. Moreover, thinner n- substrate can sustain the high BV in the presence of field stop layer. Also, field stop layer speeds up recombination rate of the minority carriers comparable to that of PT IGBTs. Hence, the TGFS IGBTs provides the option of paralleling of multiple devices with lower on-state losses and faster turn off capability. The benefits of TGFS technology are compared with PT and NPT technologies in Table 2.2.

2.3 Physical IGBT Structure

In order to understand physical phenomena responsible for electrical parametric shift, simplified IGBT structure types and analytical expression for both $V_{ce,on}$ and V_{th} are briefly discussed. An equivalent MOSFET-BJT of IGBT is shown in Figure 2.4 (a). Similarly, a detailed gate capacitance equivalent circuit is shown in Figure 2.4 (b). It can be seen that IGBT generally

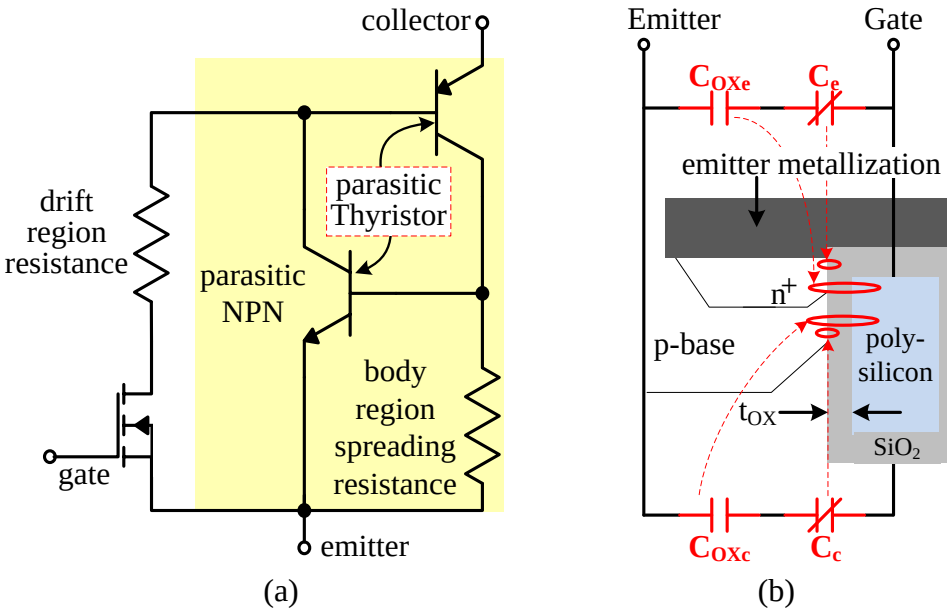


Figure 2.4. Simplified circuit model for (a) MOSFET-BJT equivalent circuit and (b) gate-oxide capacitances.

provides the benefit of both MOSFET by using low power gate control and BJT by providing same conductivity modulation at high power levels within a single die. Yet, IGBTs are also prone to latch-up due to parasitic Thyristor of the structure. In order to eliminate the parasitic Thyristor, the voltage drop across base spreading resistance has to be kept to minimum so that the parasitic NPN transistor is not turned on. Further details about PT, NPT and TGFS internal device structure are given in Fig, 3 (a) – (c).

Using the model shown in Figure 2.4 (a), $V_{ce,on}$ of an IGBT can be given as:

$$V_{ce,on} = V_{pn} + V_{NB} + V_{MOS} + V_{contact} \tag{2.1}$$

where V_{pn} is the p^+-n^- junction drop, V_{drift} or V_{NB} is the drift region (n^--layer) drop, V_{MOS} is the MOSFET region drop and $V_{contact}$ electrical contact resistance drop. Further detailed analytical analysis can be found in [5].

In order to better understand the given results and associated discussions presented later in this paper, it important to note that $V_{ce,on}$ temperature coefficient (tempco) is defined as a function of its collector current. Between different IGBT structures, the PT shows a negative tempco for much broader range of collector current compared to that of NPT and TGFS. Contrarily, NPT and TGFS display negative tempco for much smaller collector current values and are well suited for thermally-coupled parallel solution [6].

On the other hand, V_{th} of the IGBT can be defined as [5]:

$$V_{th} = V_{FB} + 2\sqrt{\phi_F^2 + 2\frac{q\epsilon_s N_A \phi_F}{C_{ox}}} \qquad (2.2)$$

where V_{FB} is the flat band voltage of Si/SiO_2 interface, Φ_F is the half contact potential, q is the charge of single electron, ε_s is the permittivity of Silicon, N_A denotes the acceptor type doping concentration of channel and C_{ox} is the gate oxide capacitance in per unit length. It is important to note that unlike other parameters in the Eq. 2.2 which remain more or less constant over IGBT lifetime, the degradation in gate oxide capacitance causes a significant impact on the V_{th}.

Gate oxide capacitance can be further divided into its constituting capacitances as well. Using the model shown in Figure 2(b), gate-emitter (C_{ge}) and gate-collector (C_{gc}) capacitances can be determined using following relationship [7]:

$$C_{ge} = \frac{C_{oxs}C_e}{C_{oxc} + C_e} + \frac{C_{oxc}C_c}{C_{oxc} + C_c} \qquad (2.3)$$

$$C_{gc} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} \qquad (2.4)$$

where C_{oxe} and C_{oxc} denote the oxide layer capacitance with n^+ and p regions respectively. Also, C_e and C_c represent the depletion layer capacitance for n^+ and p regions respectively and C_{dep} represent the depletion layer capacitance under the oxide layer where C_{ox} is the oxide capacitance per unit area. However, it is difficult to measure these capacitances directly so, manufacturers typically specify parasitic capacitances of the IGBT. The parasitic capacitances mentioned in the datasheet generally include C_{ies}, C_{oes} and C_{res} which define input, output and reverse gate capacitances, respectively. Following relationship can be used to estimate components of the total gate oxide capacitance:

$$C_{gc} = C_{res}\,; C_{ge} = C_{ies} - C_{res}\,; C_{ce} = C_{oes} - C_{res} \qquad (2.5)$$

2.4 IGBT Reliability and Aging Mechanisms

As discussed in the introduction, catastrophic failures can take place in case of IGBT failures which results in costly shutdowns of the overall system. Through continuous monitoring not only costly shutdowns can be eliminated but also system availability can be improved. Although variety of failures in IGBT can occur which are probably triggered by different aging mechanism however, the main sources of stress remain the same. In fact during on field operation IGBTs are subjected to a variety of electrical as well as mechanical stresses which impact the device age condition and lead to potential failure.

Almost, every IGBT device is manufactured such that it can last for millions of cycles before substantial devices degradation occurs under given operating conditions yet, on-field failure data suggests otherwise. So, to determine the aging mechanisms and understand fatigue

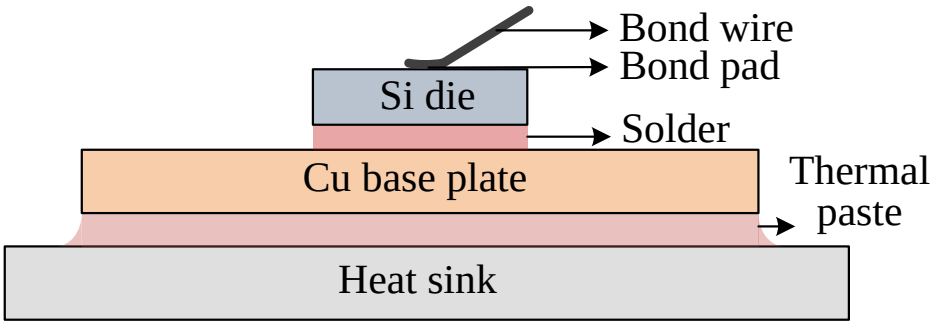


Figure 2.5. Typical discrete package structure of an IGBT.

process, accelerated aging tests are employed. Furthermore, it is evident that aging tests and corresponding reliability data are required during the designing stage to ensure the reliability of IGBT devices in the power converters [8].

Based on the literature review, failure mechanisms can be classified in to two distinct groups; intrinsic and extrinsic failures. As shown in Figure 2.5, from reliability point of view, failures within the Si die are considered intrinsic whereas and failures in the rest of the package are considered extrinsic failures. The intrinsic failures are predominantly related to electrical stresses and can be either instantaneous or time-dependent failures. Yet, both can result in to short-circuit or open-circuit of IGBTs. The most commonly reported intrinsic failure mechanism is the time dependent di-electric breakdown. On the other hand, extrinsic failures are generally related to all other failures occurring within the package. It is understandable that the package comes in direct contact to the harsh environment conditions and therefore is subjected to failures due to excessive environmental stresses and wear-out. Moreover, bond-wire issue, solder delamination, Aluminum reconstruction are the commonly reported extrinsic failures.

2.4.1 Intrinsic Failures

Gate-oxide degradation is one of the primary degradation mechanisms especially at elevated operating temperatures. Typically, gate-oxide (or Silicon Dioxide in case of IGBT) properties are altered in the presence of strong electric field. Such changes may also occur under lower electric field (applied over a longer period of time) and/or thermal degradation of gate-oxide [9]. Primarily, gate-oxide breakdown occurs due to the defects formation or traps within the oxide layer. As the traps density exceeds the percolation threshold (beyond critical limit for insulator to act like a conductor), the defects begin to accumulate and overlap one another to form a current leakage path through the previously insulating oxide layer.

Even in pristine IGBT devices thermally generated defects formation can take place. It is so because silicon dioxide like every real oxide is not a perfect insulator having some finite conductivity especially at high electric fields. Notably, these defects may be pre-existing particularly for devices manufactured using thermally grown oxide process. Nevertheless, conduction through the insulator may be detrimental as it heats the oxide more inducing further formation of traps. Once the percolation threshold is exceeded, the overlapping traps form a current leakage path and this formation is commonly referred as soft breakdown in the literature. Beyond soft breakdown, thermal runaway effect is also possible to yield more defects. This increased trap density leads to further conduction and eventual oxide meltdown [10]. Upon melting, oxygen may be released and conductive Si filaments may be formed. This catastrophic failure mode is classified as a hard breakdown [11]. Once conducting pathway is established, gate leakage current increases for both on and off states which was previously negligibly low.

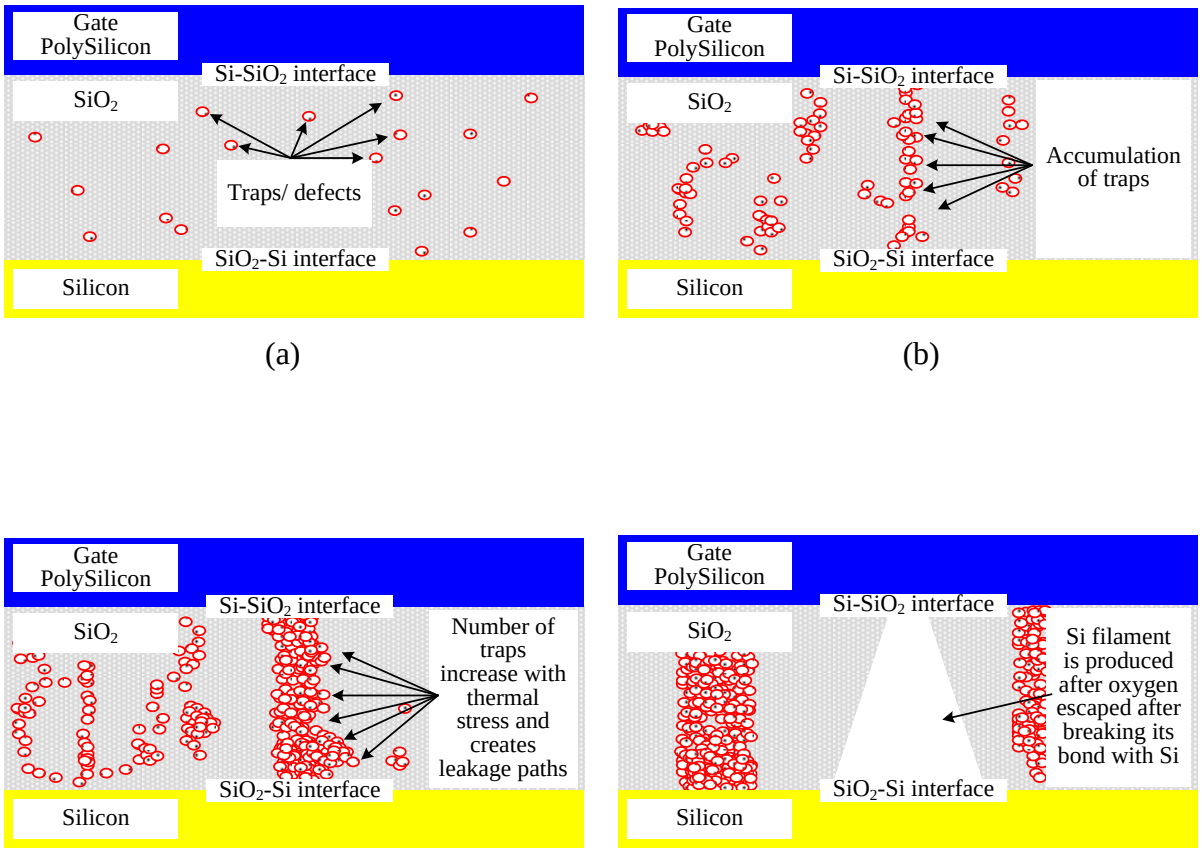


Figure 2.6. Steps of gate-oxide degradation.

Particularly in hard breakdown cases, gate current may increase by almost hundred to million times in the on and off states, respectively [12, 13]. The steps of gate oxide degradation are illustrated in Figure 2.6. More details about traps formation can be found in [14].

Hot electrons affect the gate oxide characteristics in similar fashion. Electrons (and holes) which gain sufficiently high kinetic energy under large potential difference applied across collector-emitter terminals and generate electron-hole (e^--h^+) pairs in the transistor channel due to impact ionization are termed as “hot carriers” or simply hot electrons [15, 16]. The generated

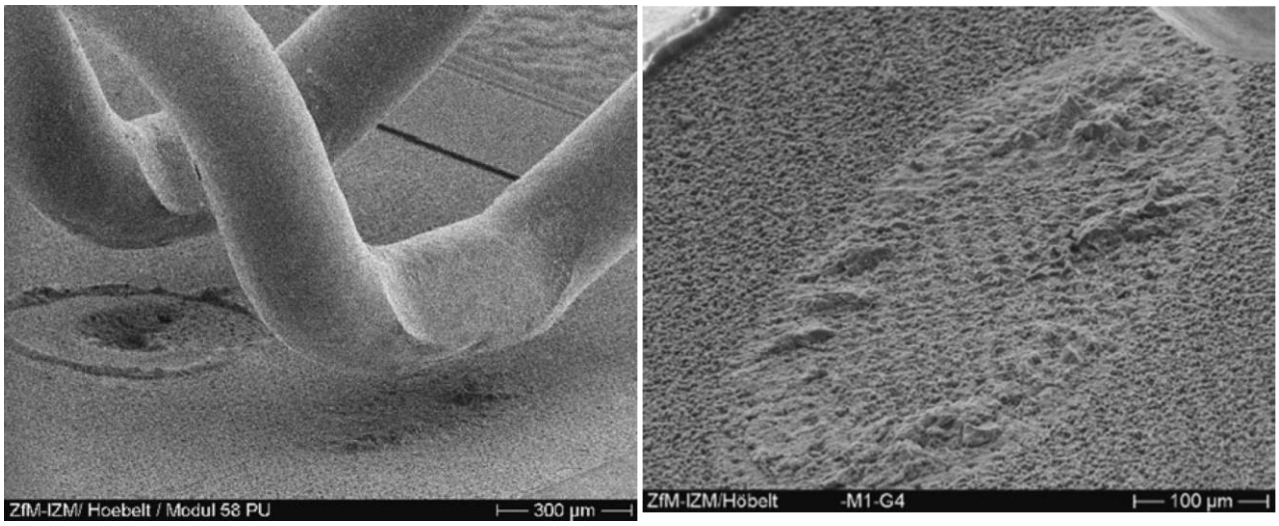
Table 2.3. Sources of stress for common package related failures.

Failure mechanism	Type of stress
Bond wire issue (lift-offs and cracks)	Maximum temperature swing, mean temperature and rising and falling slope temperature
Die attach solder joints issue (cracks and voids)	Maximum temperature swing, mean temperature, rising and falling slope temperature and humidity
Aluminum metallization reconstruction	Mean temperature and current density

e^--h^+ pair dissociates in the channel; while the hole moves to the substrate, the electron impacts the gate oxide and leads to trap formation. These charged traps can directly alter gate threshold voltage and affect the transistor operation. Moreover, hot electrons have been shown to reduce the time to gate-oxide breakdown [17].

2.4.2 Extrinsic Failures

Almost all extrinsic failure mechanisms are related to package which occur due to environmental stresses [18]. Capturing of extrinsic failures in early stages is generally easier than some of the intrinsic failures because the degradation due to underlying aging mechanisms accrue over a period of time. Mostly, temperature related stresses are held responsible for majority of package related failures. Most commonly reported extrinsic failure and corresponding aging mechanisms are briefly described in the following subsections. Table 2.3 provides the summary of the responsible electro-mechanical stresses for failure mechanisms [19].



(a) (b)

Figure 2.7. Bond wire lift-off different IGBT samples; (a) Lift-off after power cycling test and (b) magnified image of another sample showing lift-off pattern.

Bond-wire Fatigue

Bond wire lift-off is one of the most commonly reported failure mechanism especially under low temperature swing [20], [21]. Wire bond connections are most susceptible to thermomechanical stresses due to their presence in close vicinity of die and junction. During switching operation at rated current, the chip undergoes severe thermal stress due to heat generated as the result of power losses. So, the wire bonds are also exposed to almost the same temperature swing like the chip. This condition is further aggravated by the varying spatial thermal gradient within the die due to inherent uneven heating. Moreover, thermal gradients are coupled with the CTEs mismatch between the aluminum metal wire bond (~22ppm/K) and the silicon semiconductor chip (~4ppm/K).

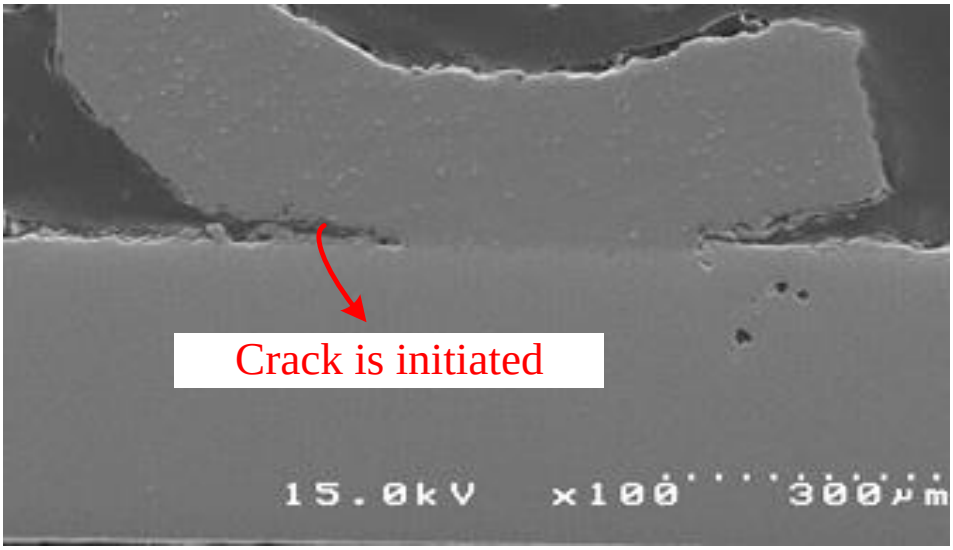


Figure 2.8. Cross-sectional image of crack initiation in the bond wire.

The wire bond failure may start from bond wire tail or heel. Cracks appear alongside the perimeter of aluminum grains. The wire-bonding process is generally produces deformation in the wire material. Particularly, small grains are formed built in the interface region (contact with the bond pad) during the following system soldering process. The grain size in the wire center is much larger than in the welded zone [22]. Typically, small sized grains exist at the periphery of the bond wire whereas larger grain sizes prevail in the center due to the process. So, the crack is initiated once the wire could not to contain local strain. Figure 2.7 shows crack in the bond wire of an aged IGBT [23]. The wire bond becomes weaker with every thermal cycle in a self-accelerating manner. As the crack reaches the center of the bonding region, the electro-mechanical contact breaks down [24]. In Figure 2.8, bond-wire lift-off has been shown for two different IGBTs.

Die-attach Solder Joint Failure

Solder joint degradation is another failure mechanisms commonly reported for IGBT devices. The primary reason for solder degradation is the mismatch between CTEs of different metals and/or alloys (Al, Cu and Si). The power loss generated in a switching cycle needs to be rapidly dissipated from the chip in to the ambience. The losses induced heat produces temperature gradients along the vertical and lateral dimensions of the package such that the product of temperature gradients and CTEs mismatch causes thermomechanical stresses across all the layers in the package creating fatigue problems. Even with closely matched CTEs, the varying temperature gradients could still cause the solder degradation. Figure 2.9 shows one example of solder issues [25].

Discrete package contains only one die and the die is directly soldered to copper back plate (base plate). Additionally, the CTEs at both the interfaces rarely match which make these interfaces more prone to fatigue [23]. Once the solder degradation starts, creepage leads to forming voids and cracks in the solder layer [26, 27]. This unevenness of the solder layer increases the thermal resistance from the die to the base plate [28, 29] as well.

It was reported that for lead-tin alloy soldered onto copper metallization, different intermetallic phases are formed near copper layer and center of the solder layer which may be rich in tin or lead [30]. Upon thermal accelerated aging test, the periodic temperature swing produces shear stress across the package. Since, copper rich intermetallic phases are more brittle, thermomechanical fatigue crack spread more in them. Particularly, these cracks progresses from the edge where the shear strain is maximum to the center which is relatively under less strain. It is so because at the corners attached materials can easily expand due to spatial temperature

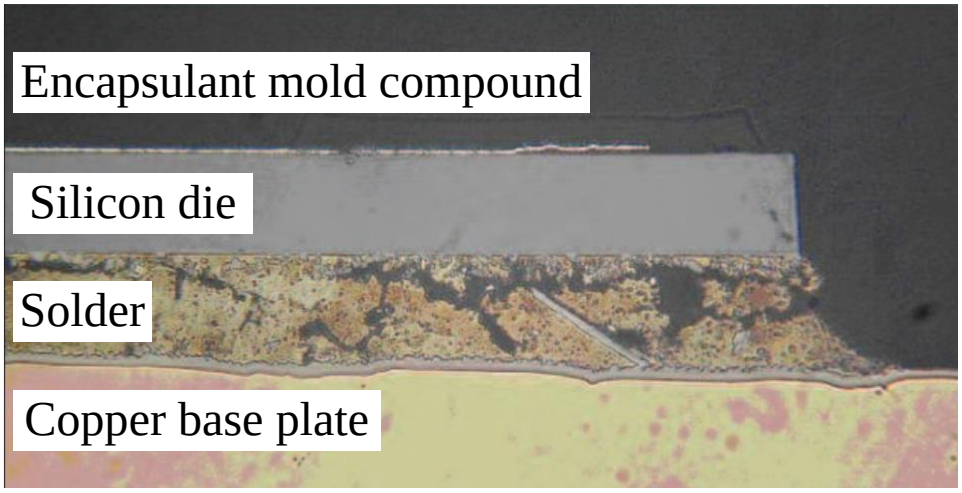
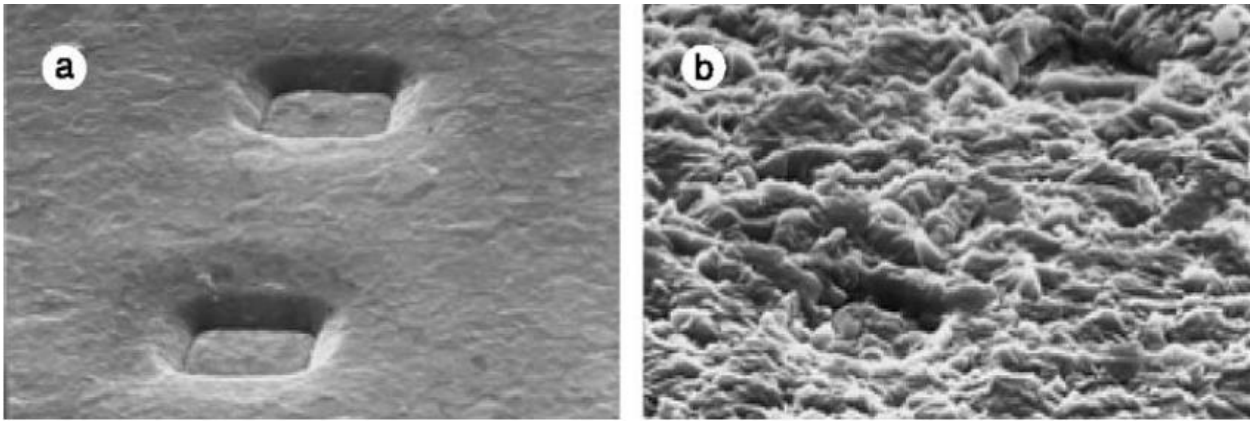


Figure 2.9. Large voids and crack in the die-attach solder layer.

gradient however, near the attachment interface the expansion is constricted leading to cracking under fatigue.

Moreover, Voids and cracks formation offer hindrance to heat flow from the chip to the ambience through the heat sink. Reduction in active surface area for heat transfer increases the thermal impedance. As more heat is accumulated within the package layers, the die temperature continue to rise which could lead to catastrophic burn-out failures and secondary breakdown. Due to lead health hazards, new lead-free solder (e.g. soft solders) have been introduced. Comparison of lifetime for lead-tin and lead free Terminal solder joint alloys was studied by Feller et al. [31]. Also, crack initiation and ensuing growth were observed for both solder types. Analysis in [32] indicates that cyclic lifetime of the die-attach bonding has a strong dependence on the variability between die bond thicknesses for tested samples.



(a) (b)

Figure 2.10. Aluminum grain boundary reconstruction (a) before power cycling and (b) after power cycling.

Aluminum Metallization Reconstruction

Periodic tensile and compressive thermomechanical forces are being exerted on the upper metallization surface under high cyclic thermal stress. There exist a significant mismatch between the top aluminum surface and the silicon semiconductor chip underneath it. Typically, for same amount of heat, aluminum metallization layer makes significant expansion (around 24 ppm/K) contrary to silicon chip which need to marginally expand (around 2-3 ppm/K) with rising temperature. As a result, the metallization layer is subjected to compressional stresses. Moreover, contact metallization layer has large grain structure. Upon experiencing such high level of thermal stresses beyond elastic limit, mechanically induced relaxation takes place which causes plastic deformation and aluminum grain boundary extrusion [30].

Ciappa [33] considers that the periodic compression stress due to rising junction temperature in excess of 110 °C causes plastic deformation of grains. Plastic deformation then leads to the extrusion of aluminum grain boundaries. As a result, the metallization surface

becomes rough and dull non-reflective surface. However, during the cooling phase (removal of thermal stress) tensile stress is generated. If the temperature makes significantly large swing, these tensile stresses may go beyond the elastic limit of aluminum and cavitation effects at the grain boundaries can occur. Nevertheless, under continued stress, such effects reduce density of contacting material thereby increasing the electrical contact resistance [34]. Also, such mechanisms can create cracks in the metallization layer surface. Figure 2.10 shows images of top aluminum surface before and after degradation [30].

CHAPTER 3

IDENTIFICATION OF SUITABLE AGING PRECURSORS[1, 2]

As discussed in previous chapter, every IGBT is manufactured for delivering maximum performance for at least few hundred million operational cycles which may correspond to 10 to 20 years of service lifetime depending on the exact operating conditions. So, to investigate the effects of thermomechanical stresses in short period of time, accelerated aging (temperature and power cycling) tests is a recognized industrial practice. Consequently, a custom aging setup has been developed for executing a variety of temperature induced aging.

In this chapter, initially, details about the accelerated aging setup for IGBTs are presented [35]. Later, variations in electrical characteristics collected by an automated state-of-art curve tracer at regular interval during aging tests for tested device samples are presented [36]. Based on the exhaustive tests results, suitable aging precursors are identified. Also, failure analysis results have been discussed in this chapter as well.

3.1 Highly Accelerated Aging Test

Through accelerated aging tests, fatigue process can be speed up [37, 38]. It has been shown that the wear-out status of the power switches can be detected through electrically measurable quantities called "aging precursors" [39]. Therefore, prior knowledge on deviation in device

[1] ©2016 IEEE. Reprinted with permission from S. H. Ali, S. Dusmez and B. Akin, "A comprehensive study on variations of discrete IGBT characteristics due to package degradation triggered by thermal stress," in Proc. of 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

[2] ©2016 IEEE. S. H. Ali, S. Dusmez and B. Akin, "Investigation of collector emitter voltage characteristics in thermally stressed discrete IGBT devices," in Proc. 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

characteristics can provide significant information for accurately predicting their failures and real-time on-board prognosis [40, 41]. A comprehensive review on current fault diagnostic and protection methods is presented in [37], [42].

In literature, reliability of IGBT modules has been studied to great extent [43-45]. In contrast to discrete package devices, an IGBT module may contain several semiconductor chips, paralleled with the help of more than one bond-wire. The findings reported in the literature are variations in collector-emitter saturation voltage [43, 44], [46], thermal impedance [47, 48], turn off time [49], input, output and reverse transfer capacitances [44], change in phase and amplitude of ringing during turn-off [50] and gate threshold voltage [12]. Nevertheless, only a few studies focused on the discrete package IGBTs [39].

During these aging tests, main focus has been devoted to capture variations in the *i-V* characteristics and parasitic elements of IGBTs. Shifts in device characteristics, such as gate threshold voltage (V_{th}), input/output/reverse capacitances (C_{ies}, C_{oes} and C_{res}), on-state collector-emitter voltage drop ($V_{ce,on}$) and breakdown voltage (BV_{ces}) for new and aged devices are investigated. Majority of these parameters require sensitive measurements, which are obtained through automated curve tracer. Due to the difficulties faced in the high-resolution measurements (μV, nA), these noise-sensitive measurements have been either omitted in previous papers or not discussed in detail.

3.1.1 Aging Test Setup Overview

To inspect the effects of electro-thermal stresses on IGBTs in a shorter amount of time, a custom designed accelerated aging test setup is developed, whose schematic details are shown in Figure 3.1. Figure 3.2 provides the snapshot of actual aging test setup including the Keysight B1506a

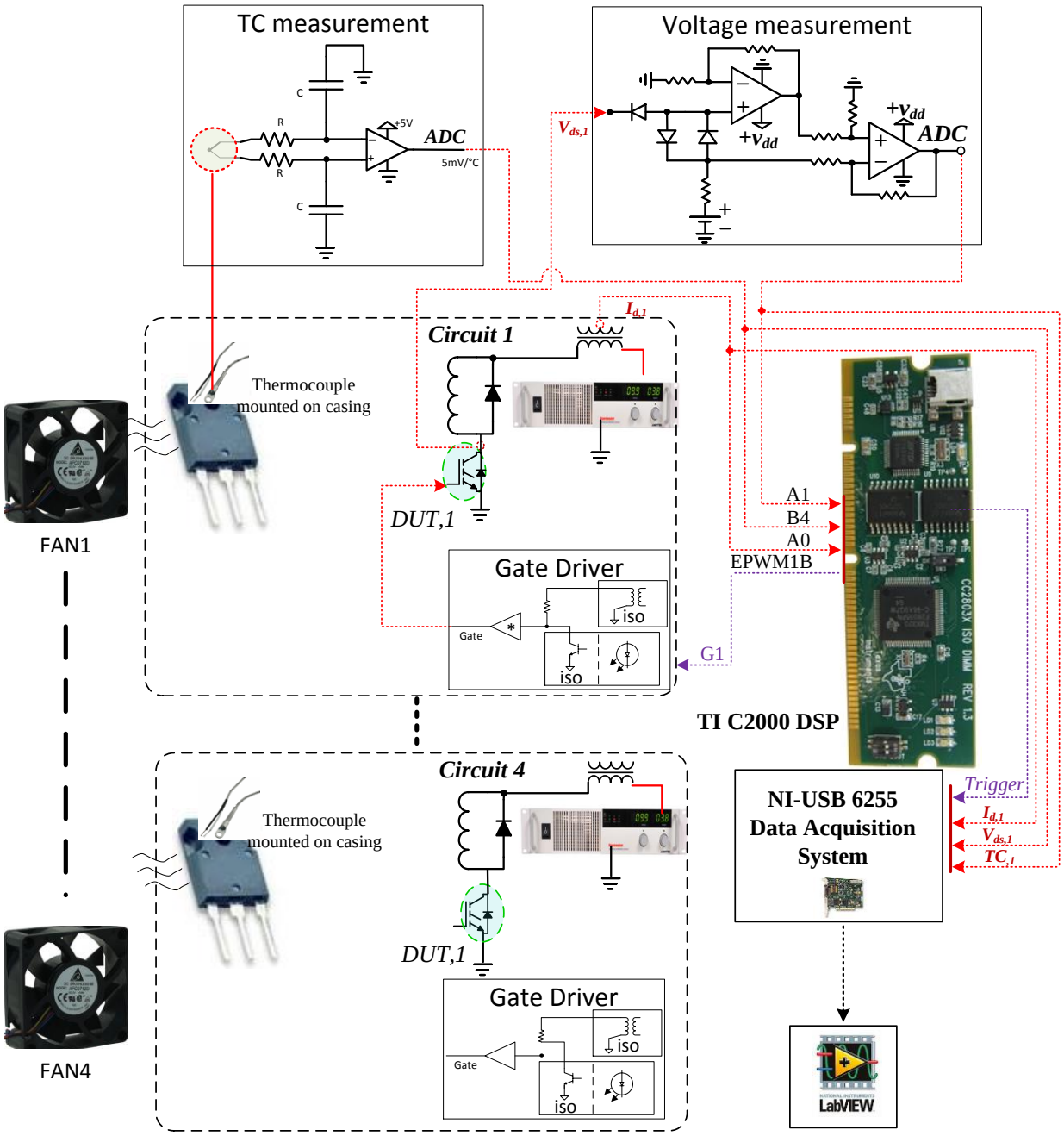


Figure 3.1. Circuit schematic for designed aging testbed for IGBTs.

Power Device Analyzer (curve tracer). The developed test-bed comprises of four independent modules. Each module is designed in a modular fashion and has its own gate driver board, power supply and signal conditioning submodules. Individual fans are also installed for cooling the devices under test (DUT). All four modules are individually controlled by TI Delfino 28335 DSP controller board. An NI 6255 data-acquisition system (DAQ) is also connected to the computer for on-line monitoring and recording of $V_{ce,on}$ voltage. Moreover, the curve tracer has been used as integral part of the setup. The curve tracer is employed at regular intervals during the aging test which takes a variety of electrical parameters measurements.

The signal conditioning sub-module measures the $V_{ce,on}$, collector current (I_{ce}), and case temperature (T_c) for temperature control purposes. $V_{ce,on}$ has to be measured by a dedicated voltage sensing circuit, whose details are discussed in [51], to protect the DAQ from high voltage when DUT is at off-state. Moreover, it allows high resolution measurement of $V_{ce,on}$ which is not possible with a voltage sensing circuit utilizing ubiquitous voltage dividing resistors. T_c is measured using K-type thermocouple attached to the bulk case of DUTs. All these signals are further sent to the DSP board for control purposes and also to the DAQ for data monitoring and recording.

Either of the continuous on/off and switching based cyclic test approaches can be implemented in the setup. DUTs are individually loaded with their own dedicated power supplies without adding any external load. Each power supply is operated as a current source to pump desired amount of current into the DUT during the heating cycle. Limiting the current manually removes the necessity for additional current control loops for each DUT in the DSP.

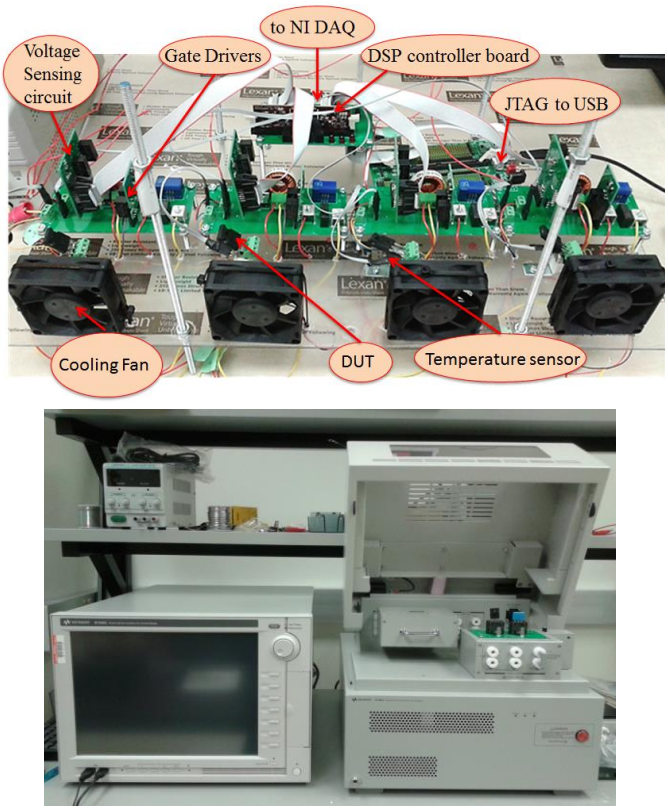


Figure 3.2. Actual photograph of designed aging testbed for IGBTs along with the curve tracer.

3.1.2 Temperature Control

A hysteresis temperature control is implemented in DSP software for each DUT. Basically, the switch is kept in on-state till the temperature reaches to defined upper limit. The DSP estimates the junction temperature of individual DUT from the conducted losses ($V_{ce,on}$ and I_{ce}), thermal impedance model (Z_{th}), and T_c measurement in order to generate corresponding gating signals for the DUTs. After the upper limit for T_j is achieved, DSP turns off the corresponding DUT. Once the DUT is turned off, the corresponding cooling fan is engaged for faster cooling. Due to heat-transfer delays from package to thermocouple, measurement differences occur. These are modeled as thermal capacitance, C_{th} in the thermal model. Comparing with measurements by

FLIR E6 IR non-contact camera, these errors are corrected in the DSP software. Nevertheless T_c measurements are not available instantly due to sluggish response of thermocouples and create some T_j estimation so, fine tuning of controller and subsequent timing for gating pulses are performed through trial and error.

3.1.3 Upper T_j Limit for Highly Accelerated Aging Test

It is well known that Silicon and other semiconductors offer intermediate conductivity (compared to typical conductors and insulators) at the room temperature. Moreover, pure (intrinsic) semiconductors contain equal distribution for electrons and holes but extrinsic semiconductors are doped with generally one dominant type-either electrons or holes to alter the electrical characteristics e.g. conductivity. For a given amount of thermal energy at a particular temperature, Si atoms contribute fairly small number of charge carriers and the overall conductivity depends on the amount of dominant charge carriers.

It is understandable that the device temperature impacts the electron-holes distribution in the power semiconductor and the devices' characteristics as well. So, the advantageous electrical characteristics of semiconductor for maintaining appropriate power control are guaranteed only within certain temperature range. As the temperature exceeds certain limit, Si atoms themselves generates comparable amount of charge carriers compared to the dominant ones [52]. So, device conductivity becomes uncontrollable and desirable power flow is compromised. Due to uncontrollable charge flow, thermal runaway is also inevitable. This thermal energy is referred as critical energy in the literature.

Typically, critical energy limit is determined by the semiconductor's bandgap energy. As a rule of thumb, 500 times the bandgap energy of Si which corresponds to ~ 300°C is considered

enough to cause thermal runaway [53]. For a device which does not experience any thermal failure, it shows typical characteristics upon cooling below 150°C (suggested by manufacturers). As explained earlier, the junction temperature and current is regulated to avoid heating the devices to the critical limits for DUTs.

3.1.4 Test Procedure for Parametric Device Characterization

Initially, a number of 1200V / 11A power rating DUTs are subjected to relatively large temperature swings to observe the aging mechanisms. Based on these tests suitable aging precursors are determined. Each device sample was individually subjected to temperature swing of 40-200°C. It is ensured that the maximum T_j is well below the corresponding temperature limit for critical energy but at the same time yields faster results. During these high temperature tests, high degrees of gate-oxide and die-attach solder degradations in the DUTs are anticipated. During this test, one thermal cycle lasts for almost three minutes (45s and 110s for heating and cooling respectively). Thus, the consequences of these two aging mechanisms were observed before there was any significant damage on the bond-wires.

The test is stopped at regular intervals and DUTs are placed in the curve tracer for measuring aged device parameters. Also, control sample is used to ensure measurement accuracy. The measurements taken using curve tracer are 1) BV_{ces}, 2) gate currents, 3) gate resistance, 4) $V_{ce,on}$, 5) V_{th}, 6) gate charge and 6) parasitic capacitances. One important point to note is that all the curve tracer measurements are taken at ambient temperature (T_{amb} = 28°C). After measurements are taken, all the DUTs are placed back into the setup for aging. This procedure is repeated for every DUT until it can no longer be turned ON or OFF by its corresponding gate driver. This is referred as “loss of gate control” in further discussion.

Table 3.1. Summary of device condition after failure for first set of devices.

Device	Number of cycles to failure (Nf)	Device description after failure
IGBT-3A	2594	Always OFF → Open Circuit (cannot turn ON by the gate driver circuit), high leakage current, small G-to-E resistance but significantly higher C-to-E resistance
IGBT-5A	2674	
IGBT-4A	2059	Always ON → Short Circuit (cannot turn OFF by the gate driver circuit), possible latch-up, high leakage current, small resistance between G-E or C-E terminals

The summary for each DUT after failure is presented in Table 3.1. In the next section, the results describing the general behavior of the tested samples are shown.

3.2 Parametric *i-V* Characterization

The *i-V* characteristics for DUTs from Table 3.1 are shown in Figures 3.3-3.7. Figure 3.3 shows the variation in BV_{ces} with aging. The compliance current for BV_{ces} measurement is 0.25mA. Almost a maximum of16V positive increase can be seen from the value before aging. This is a negligible change considering the original BV capability > 1.2kV. Moreover, this increase in BV_{ces} can be attributed to lower carrier injection rate in breakdown region at elevated temperature [23].

Similarly, variations in gate leakage current are shown in Figure 3.4. It is noticed that gate oxide degradation causes no consistent change in gate leakage currents. Similarly, consistent variation is not found for the gate resistance as is shown in Figure 3.5. Similar, to BV_{ces} measurements, the gate measurements also change significantly once the DUT reaches its end of life (EoL). Nevertheless, all of these parameters are important electrical characteristic of the

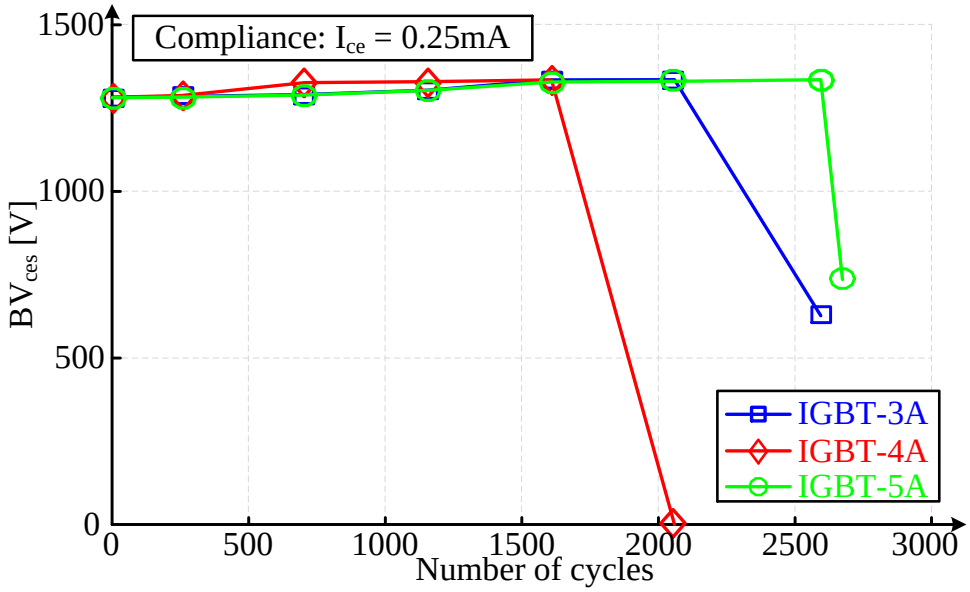


Figure 3.3. Variation in breakdown voltage with respect to aging.

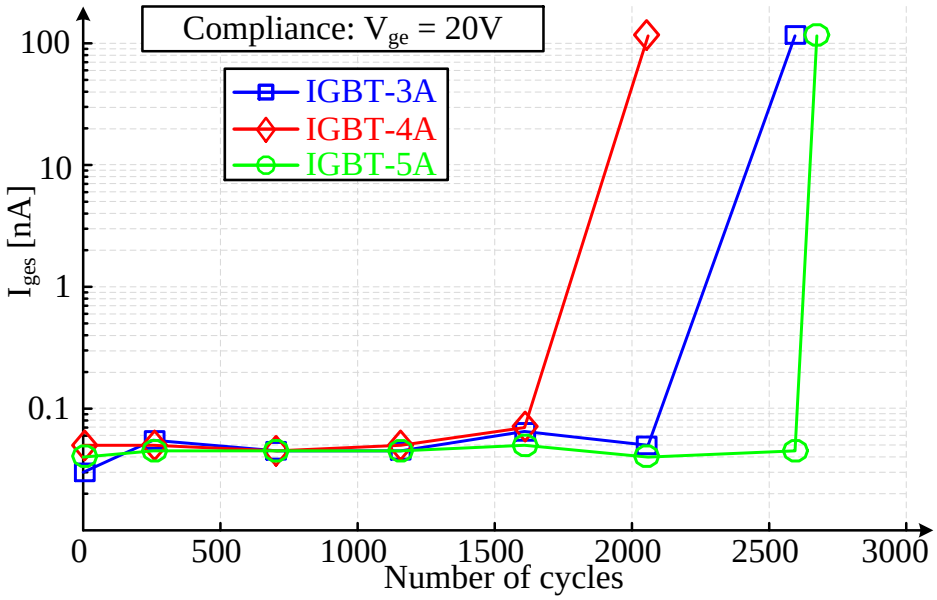


Figure 3.4. Variation in gate leakage current with respect to aging.

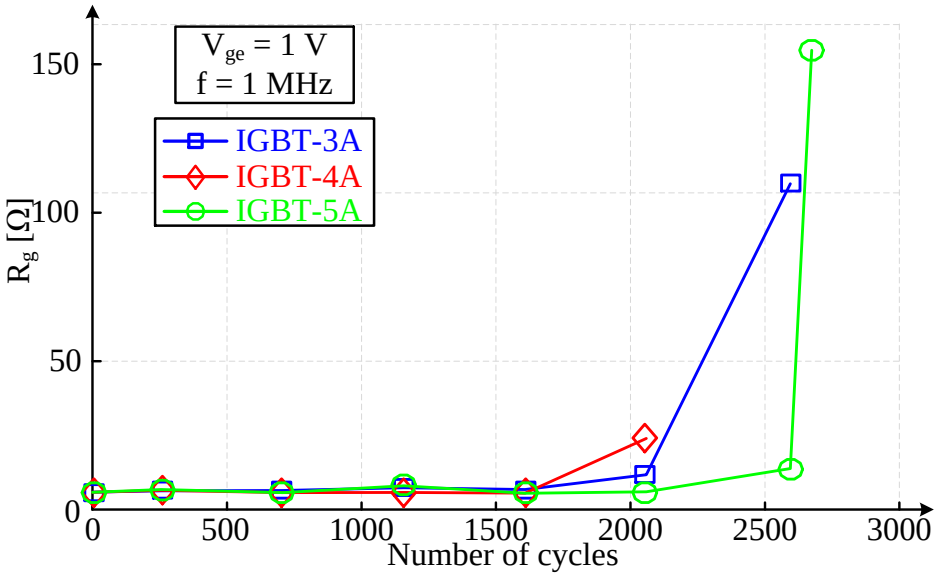


Figure 3.5. Variation in gate resistance with respect to aging.

IGBT but from selecting aging precursor point of view, the inconsistent changes are not suitable. Yet, at the same time, these measurements can be used for fault detection and other condition monitoring purposes.

Similarly, the gradual increase in on-state voltage drop of IGBT-3A sample at different current levels for multiple aging intervals have been shown in Figure 3.6. It is worthwhile to note that below I_{ce} = 5A $V_{ce,on}$ decreases with number of aging cycles and sometime before failure rises above respective values before start of aging. On the contrary, $V_{ce,on}$ for I_{ce} > 5A a continuously rising trend has been shown. The steady increase in $V_{ce,on}$ turns to sharp rise before failure suggests degradation of electrical and thermal resistances in the DUT package. The die attach solder is anticipated to be degraded which correspondingly cause $V_{ce,on}$ decrease with negative tempco below certain I_{ce}. Detailed failure analysis results are discussed later in the chapter to confirm this hypothesis.

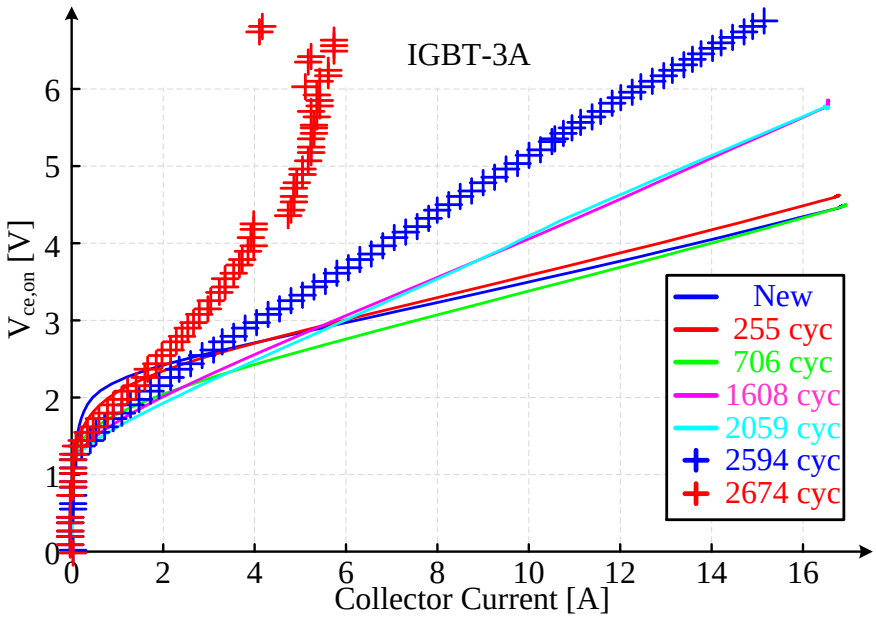


Figure 3.6. Variation in on-state collector-emitter voltage drop at different collector current with respect to aging.

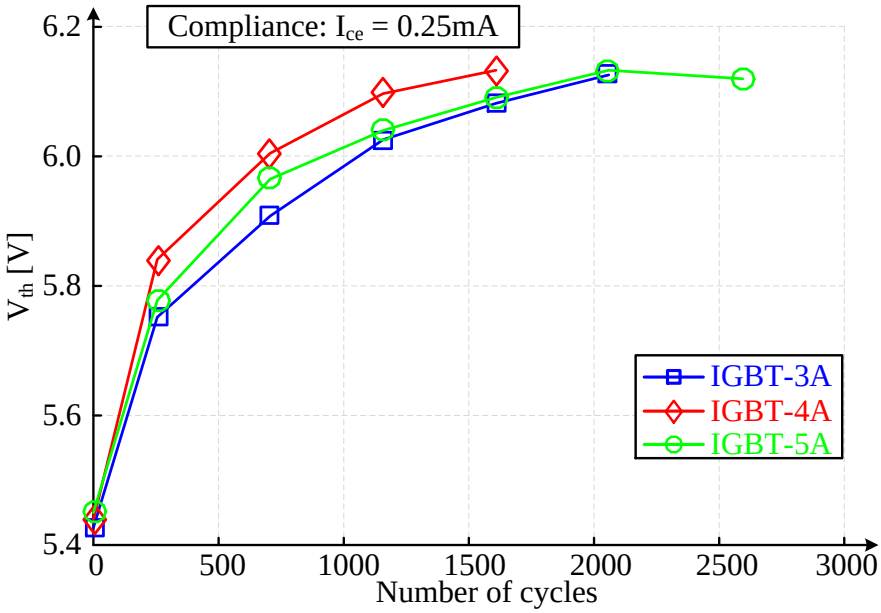


Figure 3.7. Variation in gate threshold voltage with respect to aging.

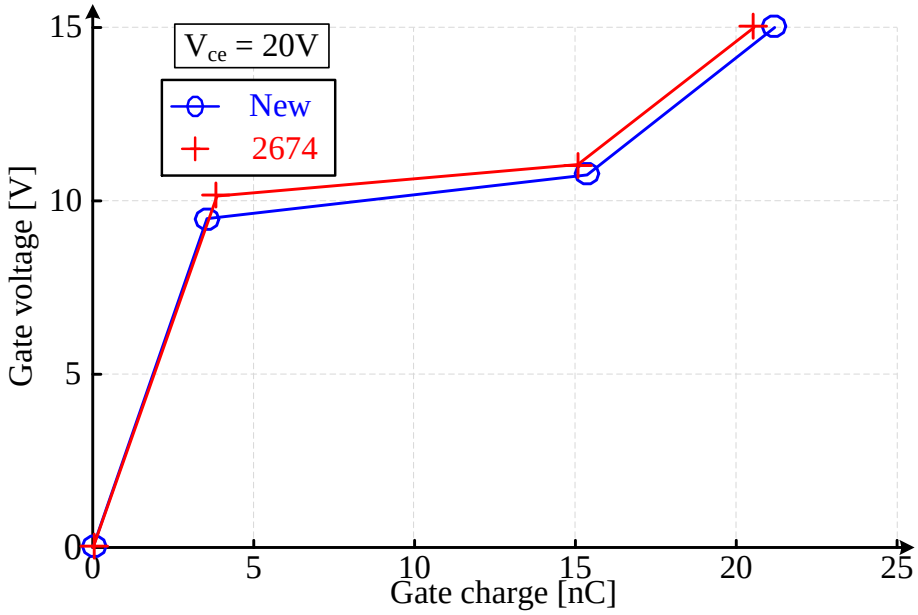


Figure 3.8. Comparison of gate charge at different gate voltages for new (before aging) and aged DUT.

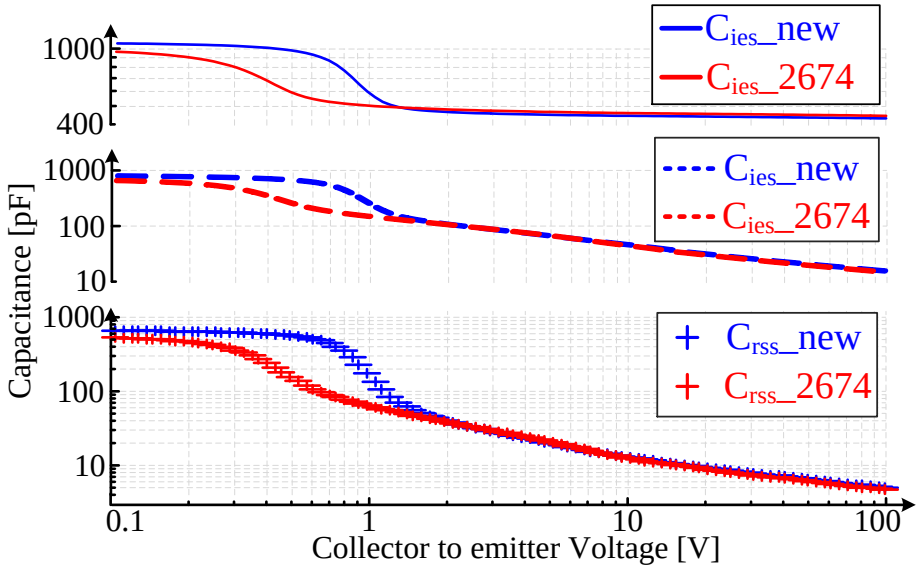


Figure 3.9. Comparison of parasitic capacitance at different collector-emitter voltages for new (before aging) and aged DUT.

Lastly, Figure 3.7 shows the variation in gate threshold voltage with respect to aging. Also, gate charge and parasitic capacitance variations are also shown in Figure 3.8 and 3.9 respectively, for better understanding and confirming of failure mechanisms. One plausible reason for the gate-oxide degradation is presence of defects and/or trapped charges in the insulator (gate-oxide) [54]. This hypothesis is strengthened by the fact that the gate charge has increased for the devices before failure. Since, the gate capacitances and gate-oxide are strongly interrelated so, it is expected that the degraded gate-oxide causes the change in gate capacitance as well. Further discussion on analytical relationship among parasitic capacitances and gate capacitance and their impact on V_{th} with aging is presented later in the chapter.

3.2.1 Failure Analysis

To shorten the device lifetime or achieving fast device failure, the *Tj* has been allowed to reach very high values which trigger multiple degradation mechanisms as discussed in the previous chapter. During the test, DUT generates heat for almost one minute and require cooling for almost two minutes. Ultimately, larger thermal swings coupled with long relaxation (cooling time) stress all the package layers. This causes more degradation in gate-oxide and die-attach solder joints than the bond-wires because of their larger lateral dimensions.

As shown in Table 3.1, DUTs lasted for less than 2500 cycles. Two failure modes are observed but generally, individual gate control for each DUT is lost before failure. Moreover, using a handheld multimeter, resistances between DUT terminals are noted as well. In order to confirm the earlier presented hypothesis, DUTs are sent to failure analysis laboratory.

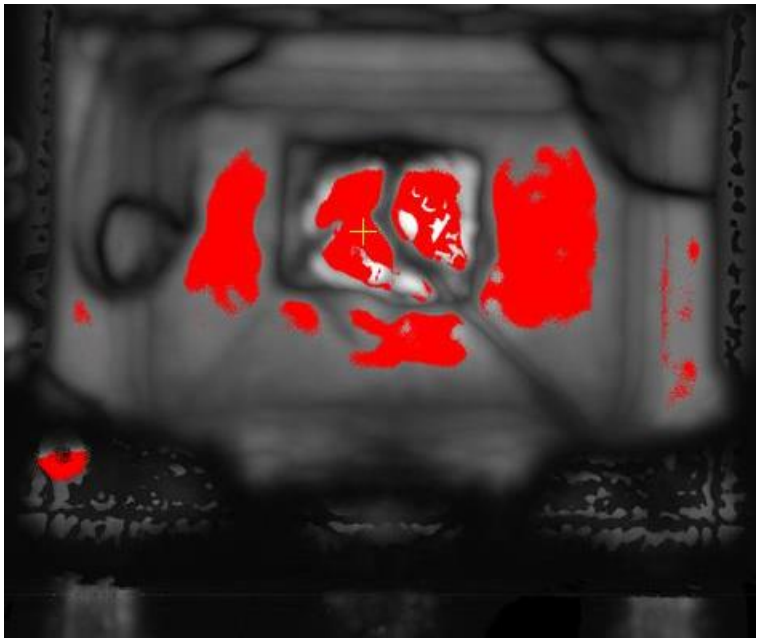


Figure 3.10. C-SAM result for failed DUT with red spots indicating large voids in the die-attach layer and no significant bond-wire issues.

The acoustic imaging analysis or C-SAM and T-SAM analyses are performed to inspect probable delamination and voids on the package layers. Both of these tests use ultrasonic transducers to transmit and receive high frequency audio signals. Since velocity of sound differs through *thin* and *thick* mediums, the analysis of time of flight/ time of arrival (ToF/ ToA) information for the received audio sample reveals possible voids in the analyzed samples. Particularly, C-SAM analyzes the ToF/ ToA for reflected audio signal time from the top surface of sample. Depending on the color scheme used in the graphical user interface (GUI) for automated C-SAM test, significant attenuation of audio signal is displayed as red spots. On the other hand, T-SAM uses two ultrasonic transducers to transmit and captures the refracted audio signals from the sample. As long as the audio signal traverses without any significant attenuation

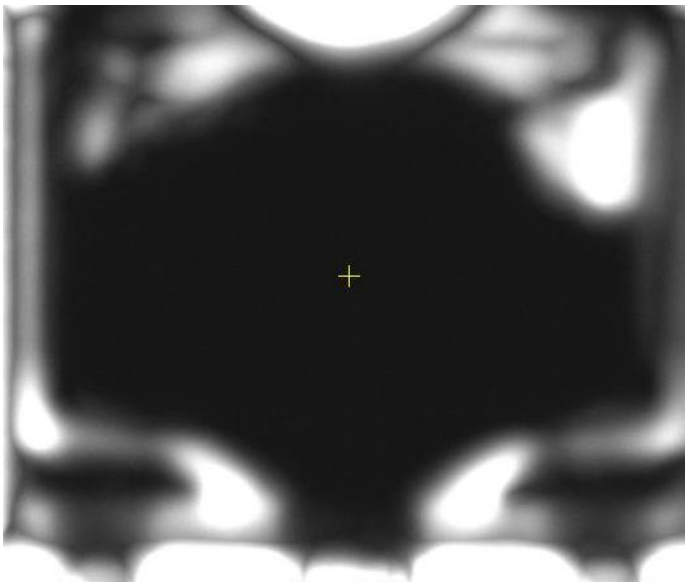


Figure 3.11. T-SAM result for failed DUT with dark spot obscuring die showing significant delamination in the package at multiple layers.

clear images appear on GUI of T-SAM test. GUI identifies those locations as dark spot(s) where the transmitted audio signal experiences attenuation due to presence of thin air or voids.

C-SAM and T-SAM results for one of the aged DUTs are shown in Figure 3.10 and 3.11. The C-SAM result indicates that there are several large voids in die-attach layer. Also, the homogenous dark spots in T-SAM images confirm delamination. Furthermore, during cross section no bond-wire issues are observed.

3.3 V_{th} and $V_{ce,on}$ Characterization at Different Thermal Stress Levels

In the previous section, both V_{th} and $V_{ce,on}$ have been observed to show reliable and consistent variations. Moreover, in order to firmly validate the utility of both as aging precursors, it is necessary more aging test at different stress levels are performed. At the same time, to emphasize

that thermal stresses resulting from all different forms of temperature variations particularly; magnitude of temperature swing, mean temperature and slope of temperature cause severe impact on the IGBTs lifetime. Also, for ac-dc rectifiers and dc-ac inverters, both the mean T_j and cyclic T_j of the IGBTs increase whereas in dc-dc converters only mean T_j for the IGBTs rise above the ambient temperature during their operation [55]. So, it is necessary to stress the devices at variety of temperature levels.

Different thermal stress scenarios applied on DUTs are grouped in to two different schemes. In the first scheme, samples have been stressed within manufacturer's specified safe operating T_j limits (SOA) or slightly above it. Although majority of the tests carried out in this scheme falls into SOA limits, just one set of DUTs have been allowed to reach $T_{j,max}$ = 180°C (above the defined SOA). In the other test scheme, the high level of stresses has been applied by maintaining the maximum T_j well above SOA limits.

Multiple IGBT technologies are tested systematically in order to verify the aging trend. All the thermal stress test schemes have been applied for different IGBT technologies. *IRG4PH20K* (punch through, PT), *IGW03N120H2* (non-punch through, NPT), *IRG8P08N120KD* (trench gate field stop, TGFS), *STGW15H120F2* (trench gate field stop, TGFS) and *HGTG5N120B* (non-punch through, NPT) have been used as DUTs in this study. These samples are referred as PT (A-series), NPT-1 (B-series), TGFS-1 (C-series), TGFS-2 and NPT-2 respectively. Since PT produces more significant parametric variations than others, the

Table 3.2. Summary of applied thermal stress testing schemes.

Test Scheme	Test number	Maximum T_c cycle range	IGBT type	Approximate maximum t_{on} / t_{off}
Scheme#1	Test # 1	(30-80°C)	PT	~ 7.5ms / 2.5ms
	Test # 2	(30-180°C)	PT	~ 45s / 105s
	Test # 3	(30-100°C)	PT	~ 15s / 35s
	Test # 4	(30-150°C)	NPT and TGFS	~ 45s / 100s
Scheme#2	Test # 5	(30-205°C)	PT	~ 50s / 130s
	Test # 6	(40-200°C)	NPT and TGFS	~ 45s / 125s

PT is tested more rigorously and subsequently studied in much detail as well. The scheme test conditions are summarized in Table 3.2. Generally, at high temperatures ranges, destructive failures have been observed whereas for lower temperature ranges, DUTs are found to be still functional without high degree of failures. Table 3.3 summarizes the general end-of-life (EoL) behavior for DUTs from schemes # 1 and 2.

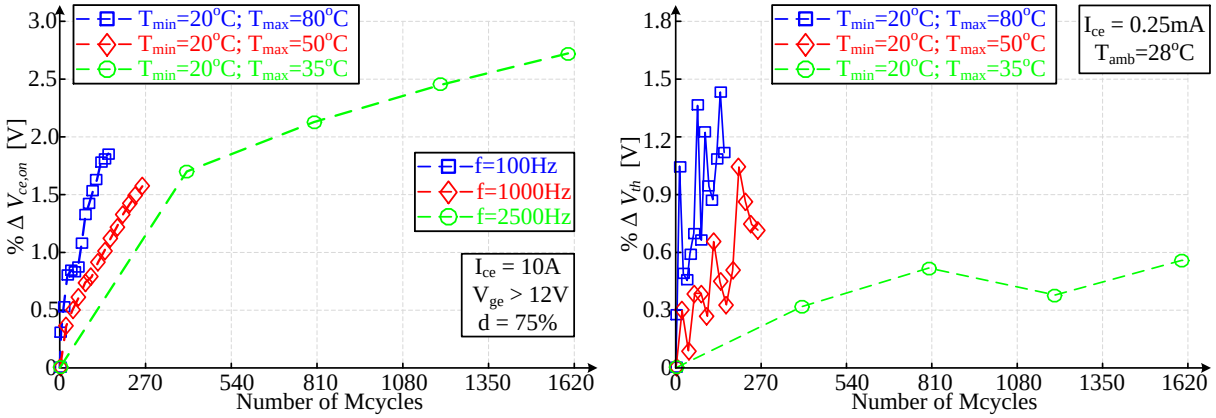
Table 3.3. General EoL behavior for DUTs classified w.r.t. to tested scheme.

Test Scheme	Maximum T_c cycle range IGBT type	Approximate maximum t_{on} / t_{off}
Scheme # 1	PT, NPT and TGFS	Always ON, very low resistance among all three terminals of the DUT's discrete package like short circuit
Scheme # 2	PT, NPT and TGFS	Always OFF or turn on with high $V_{ce,on}$ drop even at lower I_{ce}, low resistance between G-E terminal but very high resistance between C-E terminal

3.3.1 Scheme # 1

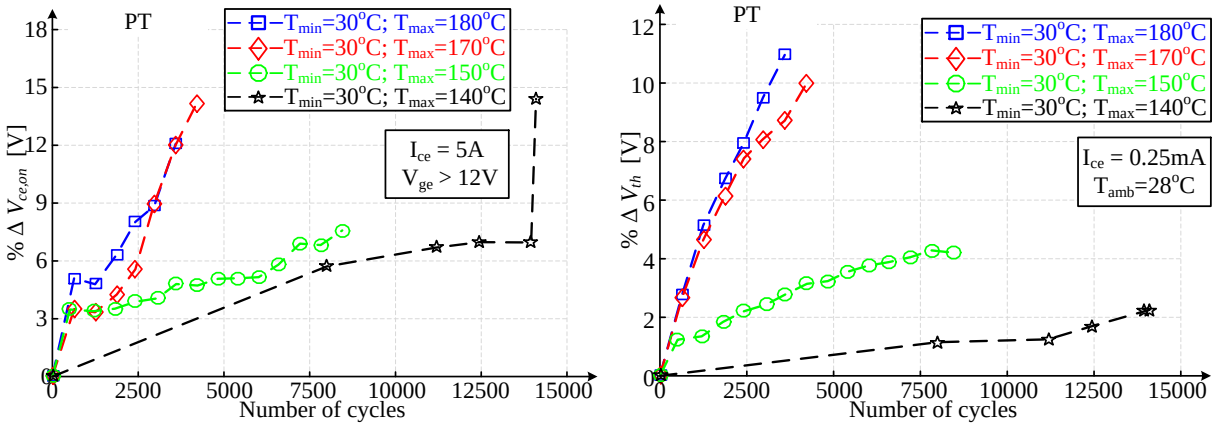
As discussed earlier, a variety of minimum and maximum T_j for the DUTs have been chosen for different tests set. Moreover, their V_{th} and $V_{ce,on}$ measurements have been recorded for analyzing their state of health and condition monitoring. So, the aging tests results for the DUTs tested under scheme # 1 are presented in Figures 3.12 – 3.15. The respective testing conditions are also mentioned in these figures as well.

As it can be seen for PT DUTs in Figure 3.12 (a) and 3.13 (a), variation in $\Delta V_{ce,on}$ profiles shows an always positive trend. Similarly, in Figure 3.14 (a), $\Delta V_{ce,on}$ profiles are shown for NPT and TGFS DUTs. Except for *NPT-2*, all DUTs have followed always positive trends in their respective $\Delta V_{ce,on}$ profiles throughout aging. Although, varying trends have been reported for $V_{ce,on}$ evolution over the device lifetime in the literature, typically, an increased electrical resistance is expected to observe with respect to aging. It is a well-studied phenomenon that contact crack formation progresses under thermomechanical stresses and leads to increased electrical contact resistance [43]. This trend is also very straightforward for condition monitoring of IGBTs by tracking $\Delta V_{ce,on}$ over aging. However, $\Delta V_{ce,on}$ profile of *NPT-2* has an unexpected



(a) (b)

Figure 3.12. Scheme # 1 aging test results for PT (maximum T_j < 80°C); (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA. Note: Mcycles = million cycles



(a) (b)

Figure 3.13. Scheme # 1 aging test results for PT (maximum T_j < 180°C); (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA.

trend and it is not possible to use it as aging precursor with same trend approach. Moreover, this profile also cannot be explained by crack formation related increased electrical resistance

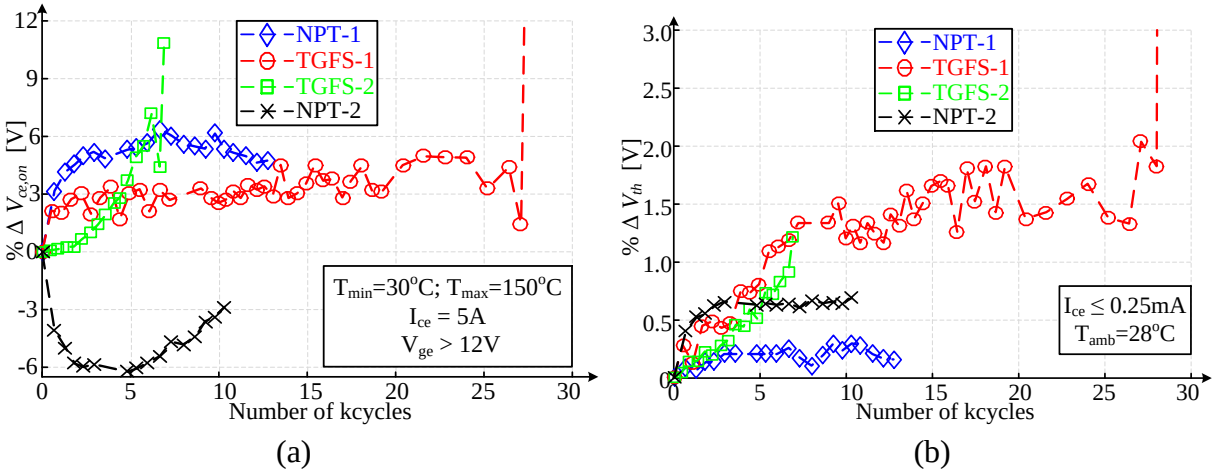


Figure 3.14. Scheme # 1 aging test results for NPT and TGFS (maximum T_j = 150°C); (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA. Note: kcycles = thousand cycles.

phenomenon. As it will be explained later in detail, different mechanisms compete here one another to determine the overall $\Delta V_{ce,on}$ trend.

On the other hand, exponentially rising ΔV_{th} profiles is seen for all DUTs under Scheme # 1 as it is shown in Figure 3.12 (b), 3.13 (b) and 3.14 (b) for PT, NPT and TGFS DUTs respectively. One major reason for shift in ΔV_{th} profiles is the degradation in gate-oxide capacitance [44]. It has been indicated in the previous section, parasitic capacitance are the constituents of the total DUTs' gate-oxide capacitances. Therefore, degradation in gate-oxide capacitance can be confirmed by investigating the shifts in parasitic capacitances for all DUTs. In this regard, parasitic capacitances for few DUTs have been presented in Figure 3.15 (a) – (c) where the shifts are speculated to be responsible for ΔV_{th} shifts. The other probable reason for potential ΔV_{th} shift can be tunneling current and charge trapping effects under high temperature environment [9]. Nevertheless, since all DUTs under Scheme # 1 shows similar exponentially rising ΔV_{th} profiles, V_{th} can be considered as a more promising parameter as a aging precursor.

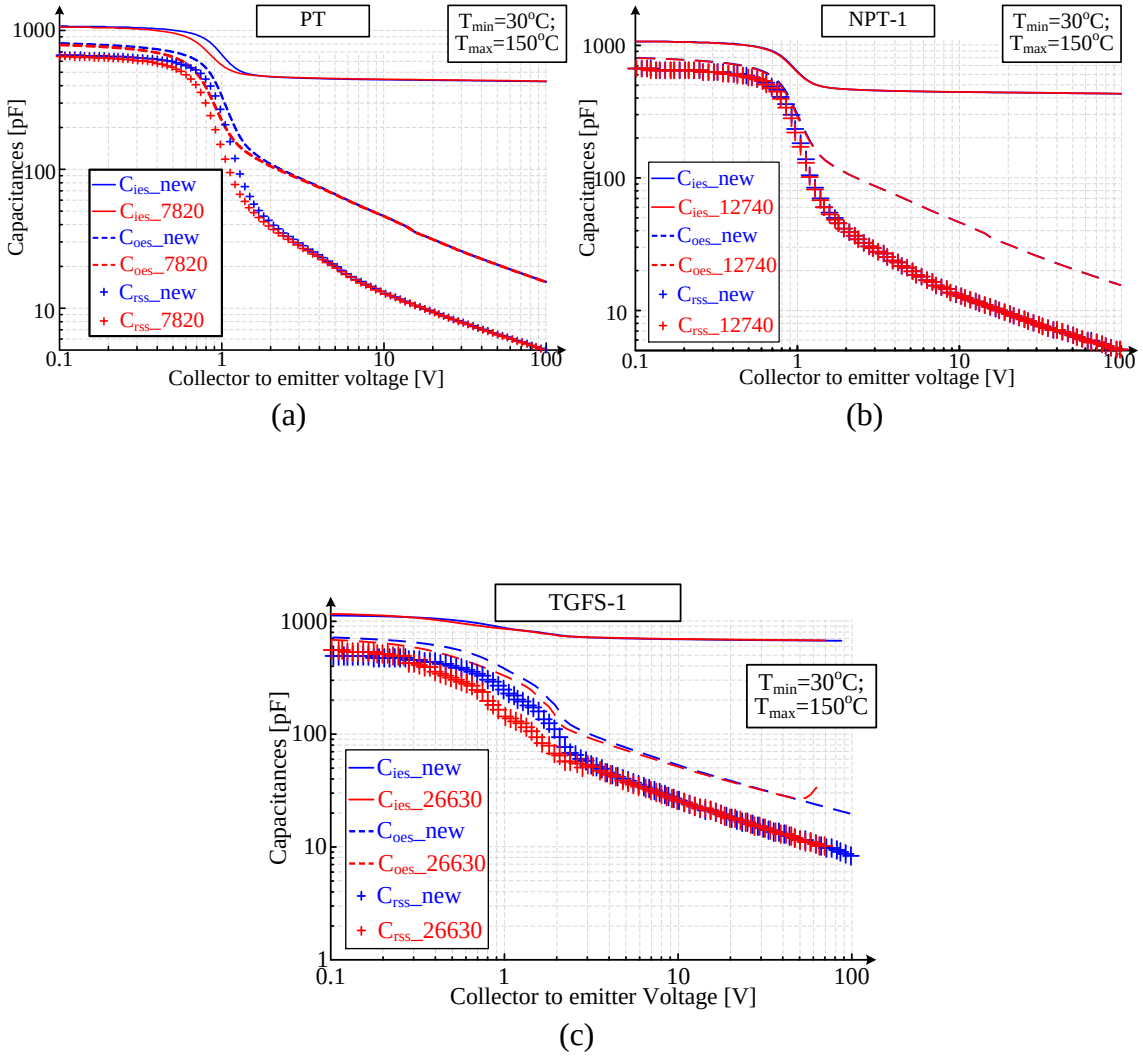
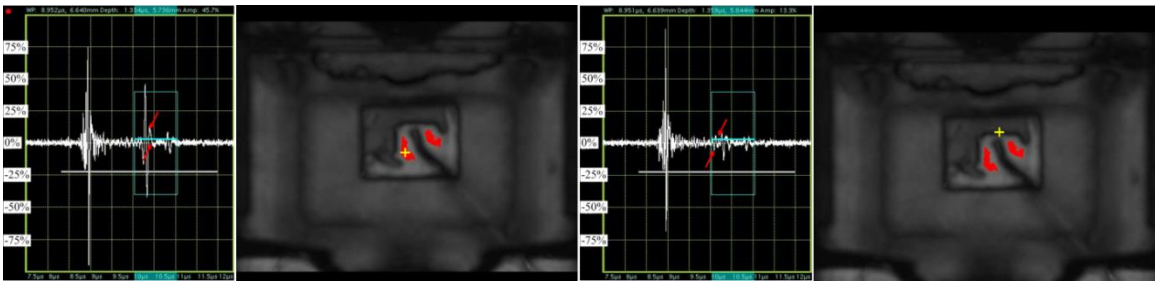


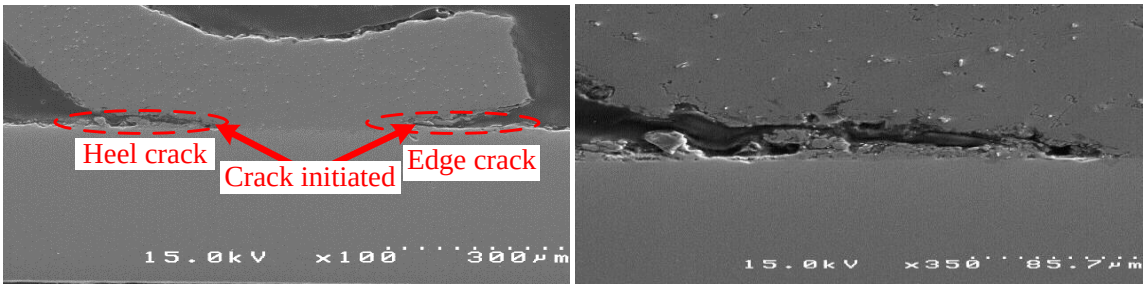
Figure 3.15. Scheme # 1 comparison of new and aged parasitic capacitances at f=1MHz for; (a) PT, (b) NPT-1 and (b) TGFS-1.

In order to have better understanding of the root cause of the aging a detailed failure analysis (FA) has been carried out. The devices first inspected with non-destructive analysis methods, using the C-Mode Scanning Acoustic Microscopy (C-SAM) in order to detect internal defects. The A-Scan waveforms are given in Figure 3.16 (a) and (c) for the yellow colored cross-

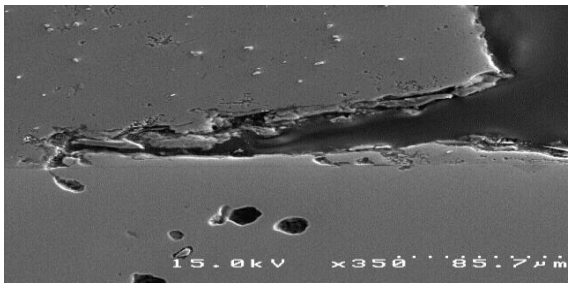


(a) (b) (c) (d)

Figure 3.16. After aging CSAM results for one PT DUT from Scheme # 1; (a) frequency response over die adjacent to bondpad, (b) its CSAM image with red spots showing delamination around bondpad, (c) frequency response over possible delamination site in mold compound and (d) its corresponding CSAM image with dark spots showing delamination at mold compound.



(a) (b)



(c)

Figure 3.17. Bond-wire to die cross-section examination snapshot; (a) complete bond pad snapshot, (b) zoomed-in at heel crack snapshot and (c) zoomed-in at bond-wire edge crack.

hair marker at the different positions on the die in Figure 3.16 (b) and (d). Furthermore, images Figure 10 (b) and (d) are captured as red spots showing delamination which provides an insight about possible issue with bond wire and mold compound (package encapsulating material). A-Scan waveforms and C-SAM images reveal the evidence of a possible area of delamination around bond wires which may also cause bond wire cracking. Furthermore, bond-wire has also been cross-sectioned to confirm potential bond wire crack propagation. Figure 3.17 (a) provides snapshot of bond wire cross-section examination. The zoomed-in Figure 3.17 (b) and (c) show the crack propagation at the bonded edges of bond-wire on top of bond pad.

3.3.2 Scheme # 2

In order to present a holistic study on thermal stress causing variations in device characteristics, DUTs are stressed beyond SOA as well. Results for few DUTs tested under test scheme # 2 are presented in Figure 3.18 and 3.19. In Figure 18 (a), the $\Delta V_{ce,on}$ profiles are shown for PT DUTs whereas $\Delta V_{ce,on}$ profiles for NPT and TGFS are shown in Figure 19 (a). All of these DUTs are tested well above their manufacturer's specified SOA limits (ΔT_{jmax} = 175°C) and the respective testing conditions are mentioned in the figures as well.

Similar aging studies in the literature have shown a continuously positive $\Delta V_{ce,on}$ trend for IGBTs throughout its lifetime. Yet, a characteristic *dip and rise* behavior has been observed for above SOA tests in this study similar to what has been reported earlier in [56]. It is hypothesized that different mechanisms are competing in determining $V_{ce,on}$ and the overall trend is defined by dominance of each mechanisms. The first mechanism is electrical resistance increase and equivalent contact resistance drop dominate the $\Delta V_{ce,on}$ profiles in the positive region. The

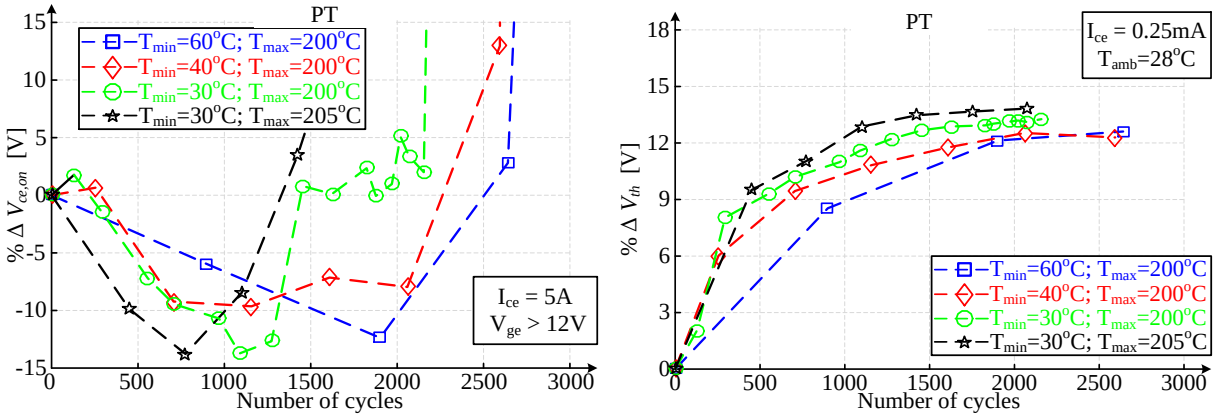


Figure 3.18. Scheme # 2 aging test results for PT; (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA.

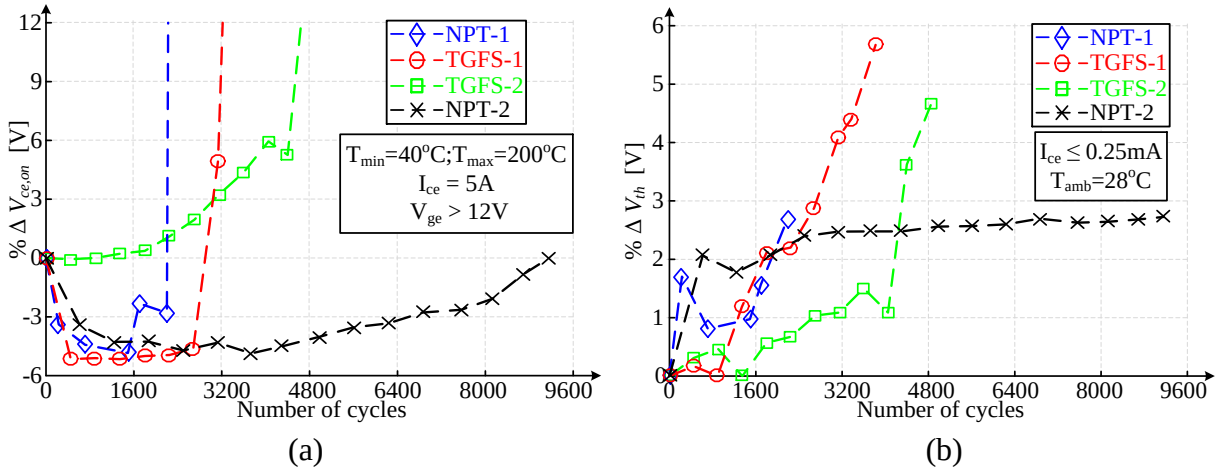


Figure 3.19. Scheme # 2 aging test results for NPT and TGFS; (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA.

second mechanism is thermal resistance increase which mainly caused by die-attach delamination for discrete IGBTs and results with higher T_j values. It is well understood that increased T_j impacts carrier concentration, gate threshold voltage and minority carrier lifetimes [53], [5]. Subsequently, $\Delta V_{ce,on}$ shifts to negative direction. Meanwhile, carrier mobility and

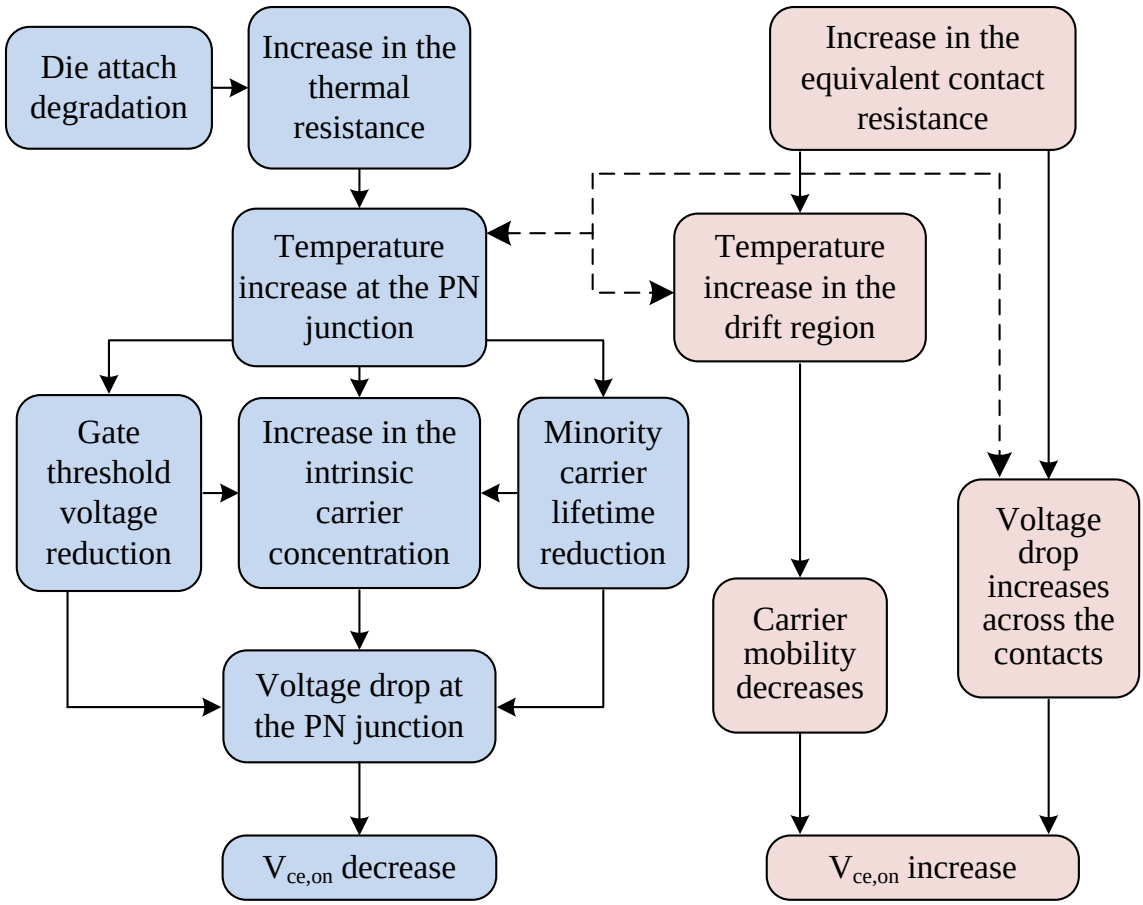


Figure 3.20. Illustration of competing mechanisms for dictating $V_{ce,on}$.

contact resistance are also impacted by the increased T_j which tend to counteract the negative change in $\Delta V_{ce,on}$ trend [19]. Thus, the net effect in $\Delta V_{ce,on}$ trend is determined by the dominant component between them [57]. This complex interaction is illustrated as flow chart in Figure 3.20.

For tests under Scheme # 1, it can be hypothesized that solder layer delamination has been minimal under reduced cyclic thermal stress. So, with minimal die-attach delamination, equivalent contact resistance drop actually dominate more and maintain the $\Delta V_{ce,on}$ profiles in the

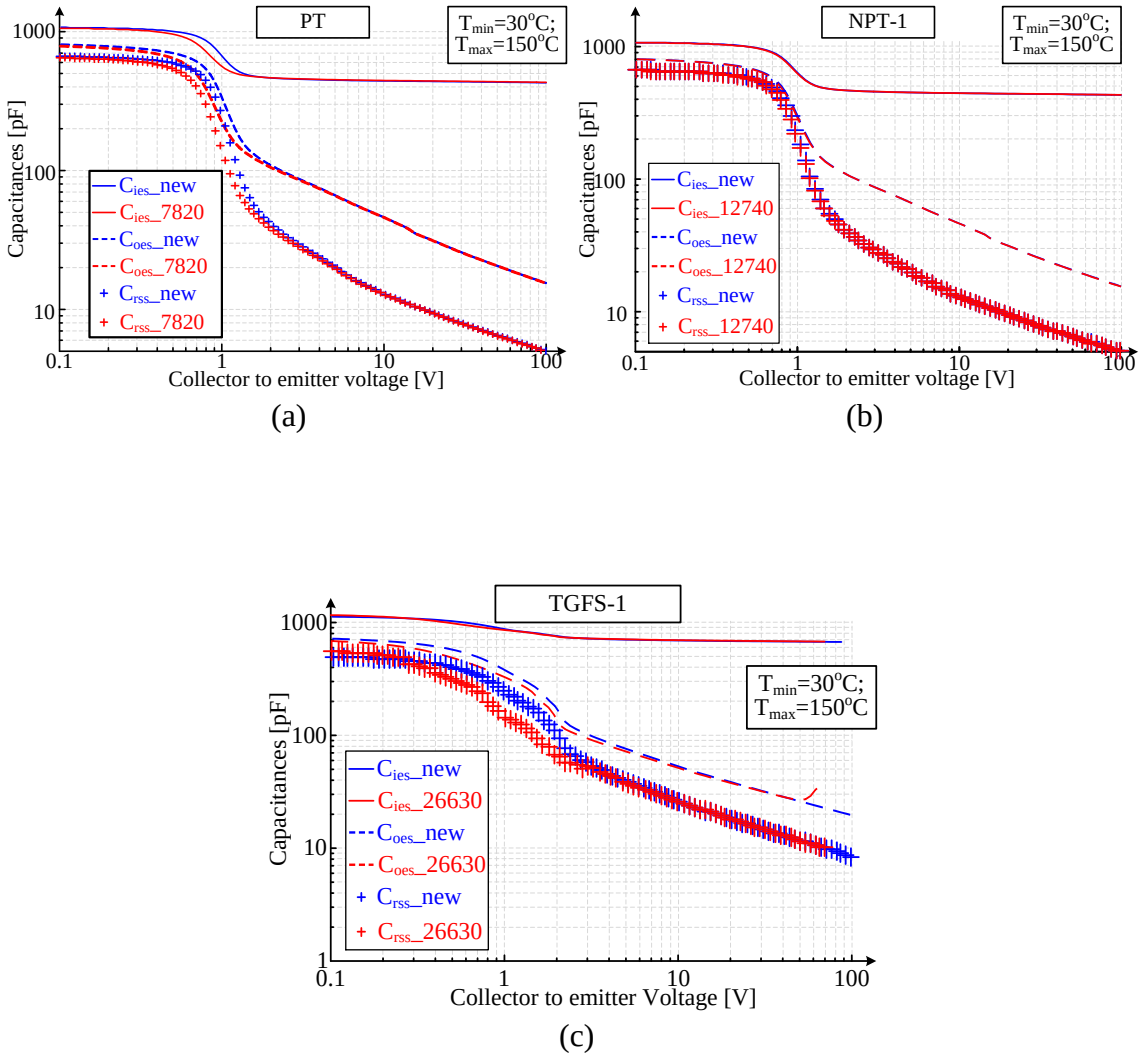


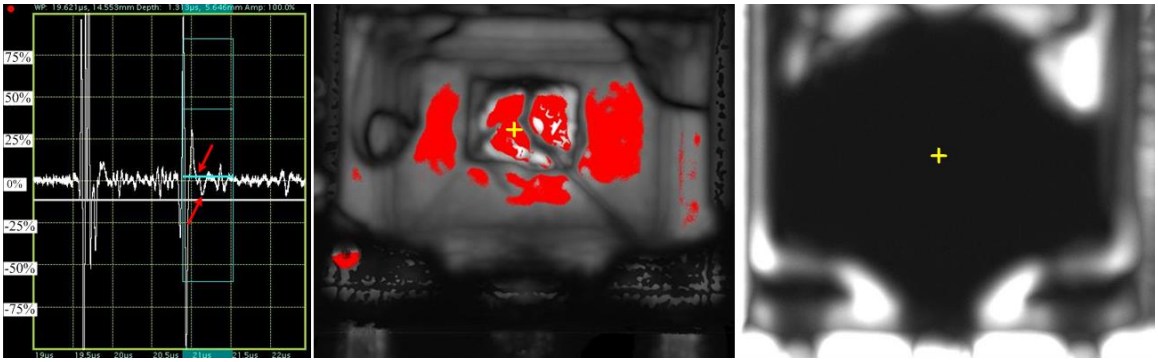
Figure 3.21. Scheme # 2 comparison of new and aged parasitic capacitances at f=1MHz for; (a) PT, (b) NPT-1 and (b) TGFS-1.

positive region. However, under Scheme # 2, higher cyclic thermal stress causes die-attach delamination, and then both the electrical and thermal resistances of the IGBT are mutually affected by the aging phenomena and also, both share a complex and weak interaction with each other as well [37]. More importantly, both resistances are responsible to altering T_j.

Another interesting observation is that the dip in $\Delta V_{ce,on}$ curves is significantly larger for PT than those for NPT or TGFS DUTs. It is speculated that for the PT DUTs, initially, negative tempco coupled with the high T_j and less contact resistance degradation shift the $\Delta V_{ce,on}$ trend to negative until it reaches the minimum value [57]. Beyond the minimum point, an increasing $\Delta V_{ce,on}$ trend is observed due to dominant effect of much degraded contact resistance. Nevertheless, for both NPT and TGFS DUTs the positive tempco somewhat compensates for the decrease in $\Delta V_{ce,on}$ due to high T_j until the minimum value is reached after which degraded contact degradation dictates the $\Delta V_{ce,on}$ trend.

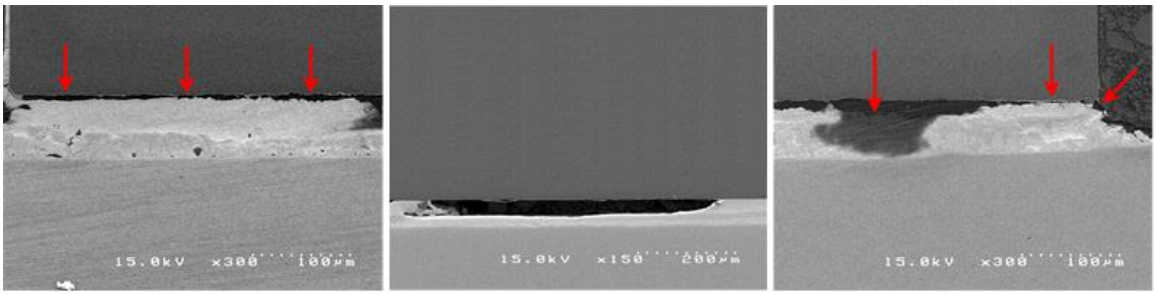
On the other hand, exponentially rising ΔV_{th} profiles can be seen in Figures 3.18 (b) and 3.19 (b) for PT, NPT and TGFS DUTs respectively. At this time it is still unclear regarding the exponential nature of ΔV_{th} variation however, as explained earlier, one major reason for shift in ΔV_{th} profiles is the degradation in gate-oxide capacitance. This hypothesis is further confirmed by comparing DUTs' parasitic capacitances for new and aged device after completing their lifetime as presented in Figure 3.21 (a) – (c). Shifts in parasitic capacitances due to aging can be seen for all three DUTs; specifically, PT DUT show drastic variation.

It is further speculated that the area underneath the emitter bond pad decreases due to aging which reduces the effective capacitance area. This area reduction results in overall less capacitance at low voltages [35]. On the other hand, at higher V_{ce}, drift region becomes more reverse-biased. This increases the overall depletion area in the region and increases C_{dep} and compensates the reduction in overall oxide capacitance [39]. Moreover, it has been shown that gate capacitances are also affected by bond-wire issues [44].



(a) (b) (c)

Figure 3.22. SAM results for one PT DUT; (a) damped acoustic frequency response for CSAM, (b) CSAM snapshot for DUT and (c) TSAM snapshot for DUT.



(a) (b) (c)

Figure 3.23. Solder die-attach layer cross-sectioning images; (a) Left edge delamination, (b) central void and (c) right edge delamination.

In order to confirm the previously speculated hypothesis, acoustic analyses are used to reveal surface voids and delamination in the package layer stack. The SAM images for one of the PT DUT are presented in Figure 3.22 (a) – (c). Surface voiding and layer delamination can be observed as red spots in CSAM and dark spots in TSAM. The given A-Scan waveform (15MHz transducer) for the yellow colored cross-hair marker at the die in CSAM result confirm die-attach delamination issues as well. Figure 3.23 provides the images of cross sectioning of solder die-

attach layer at different spots. Voids and delamination can be seen clearly in the zoomed-in images of different die sections. In contrast to SAM results for scheme # 1 which predominantly show bond wire crack issues, SAM results for high ΔT_j in scheme # 2 show die-attach delamination, bond-wire and gate-oxide degradation.

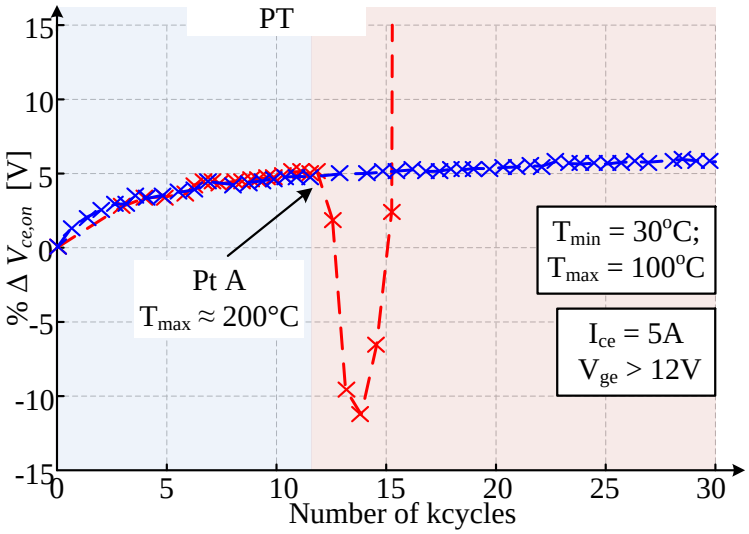
3.4 Challenges of $V_{ce,on}$ and Benefits of Using V_{th} as Failure Precursor

Although, $V_{ce,on}$ has been considered as the most useful failure precursor in the literature, $V_{ce,on}$ measurement requires re-calibration with aging and compensation for the loading effects as $V_{ce,on}$ is a function of both I_{ce} and T_j which in real-life changes according to the loading conditions of the power converters. More importantly, the trend in $\Delta V_{ce,on}$ profiles is a major concern for compensation. As discussed earlier, under solder delamination at high ΔT_j, the trend enters in to the negative region. This shift suggests reduction in absolute $V_{ce,on}$ drop and which may mislead conclusion about device health. It is shown that $\Delta V_{ce,on}$ shows an always increasing trend when T_j is kept below *SOA* limits; and it shows a characteristic *dip and rise* behavior when T_j is over *SOA* limits. However, there are still some exceptions, i.e. *NPT-2* under low thermal stress aging, which will cause extra errors in condition monitoring of IGBTs.

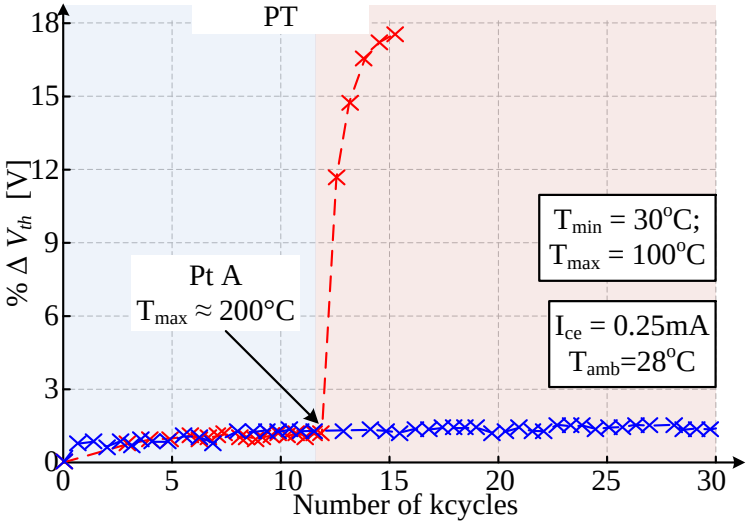
In order to further reveal the possibility of $V_{ce,on}$ misleading to a wrong conclusion about the SOH of the device, an example experiment for evaluating the robustness of precursors has been performed. In this experiment, two PT type DUTs are aged with the testing conditions similar to those from Scheme # 1 where the estimated $T_{j,max}$ has been maintained below 100°C until 12.5kcyles (Pt A). The $\Delta V_{ce,on}$ profiles for both DUTs are shown in Figure 3.24 (a). As it can be seen in Figure 3.24 (a) both DUTs follow exactly the same always increasing trend (and almost same values) for the $\Delta V_{ce,on}$ profiles for both DUTs until Pt A, as expected. Beyond Pt A,

the $T_{j,max}$ is increased to 200°C for one of the DUTs to emulate a failure in cooling system for real-life converter application. This increased stress causes the respective DUT to fail much earlier than the other DUT which in fact operates well above 30kcycles without any performance degradation or other device control issues. For this condition, although one of the switches keep the same always increasing trend, the switch with increased $T_{j,max}$ shows a significant drop after *Pt A*. This reduction is misleading as previous experimental results have shown that solder delamination can instigate reduction in $\Delta V_{ce,on}$ profiles for DUTs with high $T_{j,max}$ above their specified SOAs. Since the failure of cooling system and corresponding high value of $T_{j,max}$ stress may not be known by the condition monitoring system, this variation can be interpreted as one of the switches getting better while other keeps aging. Since the switch with higher $T_{j,max}$ stress is aging much faster compared to other switch, this misleading interpretation of SOH of IGBT from $\Delta V_{ce,on}$ trend would be critical.

On the other hand, as is shown in previous sections, ΔV_{th} profiles follow an exponential increase under all range of stress levels and have consistent variations for all tested samples from different IGBT structure types. Therefore, condition monitoring of IGBTs by utilizing ΔV_{th} profile as a failure precursor will be more straightforward and provide error free estimation of SOH of IGBTs. This conclusion can also be verified with above mentioned example experiment for verifying the robustness of the failure precursor under different range of temperature stresses. The ΔV_{th} profiles for both DUTs are shown in Figure 3.24 (b) for the example experiment. Similarly to $\Delta V_{ce,on}$ profiles, ΔV_{th} profiles of both DUTs follows exact same exponential increasing trend until Pt A. However, beyond Pt A, ΔV_{th} profile shows a sharp increase for the



(a)



(b)

Figure 3.24. Test emulating failure in cooling sub-system; (a) $V_{ce,on}$ measurements at I_{ce} = 5A and (b) V_{th} measurements at I_{ce} = 0.25mA.

DUT with high value of $T_{j,max}$ stress while it continues to increase with same slow trend for the other DUT. In fact, this trend provides correct information about SOH of the device. As it is

clearly revealed also by this experiment, ΔV_{th} profiles can provide consistent condition monitoring and using ΔV_{th} profiles information as failure precursor can timely indicate faults in sub-systems. In summary, V_{th} can provide better insight for aging and more robust imminent fault detection compared to $V_{ce,on}$.

3.5 Conclusion

Aging in switching device is imminent and needs to be evaluated using on-field monitoring of failure precursors. A comprehensive comparison of variations in different IGBT electrical parameters to improve the robustness of condition monitoring systems in energy conversion systems is presented. Particularly, $V_{ce,on}$ and V_{th} are analyzed under a variety of test conditions. The $V_{ce,on}$ and V_{th} measurement results have been captured using high precision curve tracer (Keysight B1506A). Moreover, aging mechanisms and physical phenomena responsible for variation in both $V_{ce,on}$ and V_{th} have been investigated as well. Under the given comprehensive thermal test schemes, $V_{ce,on}$ has been found to vary its trend inconsistently. On the other hand, V_{th} has maintained same trend for the variety of test. Specifically, this conclusion has been confirmed through a separate test in which sudden real-life auxiliary system failure has been emulated as high junction temperature and V_{th} unlike $V_{ce,on}$ has been observed to clearly reveal imminent device failure due to sub-system failure. Moreover, the presented compendium of $V_{ce,on}$ and V_{th} for thermal aging results will be highly useful as primary reference to further current research on device aging.

CHAPTER 4

CONDITION MONITORING CIRCUIT BASED ON IDENTIFIED AGING PRECURSORS[3]

In the previous chapters, the effects of thermal stress and aging mechanisms have been discussed. After executing a variety of thermal aging tests, V_{th} and $V_{ce,on}$ have been identified as reliable aging precursors. According to the discussed methodology in the introductory chapter, monitoring circuit for aging precursors is developed. In this regard, an in-situ V_{th} and $V_{ce,on}$ monitoring circuit has been proposed [58]. The details are discussed in this chapter.

4.1 Background

Various approaches have been presented in the literature to observe the failures and/ or detect device degradation due to aging without involving invasive device check-up. One most frequently discussed method is measuring of T_j. By using that measured T_j in the classical Coffin-Mason or other modified stress model, an IGBT's lifetime can be estimated [59]. Unfortunately, measuring T_j is not an easy task as the die is generally encapsulated in thick plastic molded packages which restrict non-invasive T_j measurements. So, different electrical parameters have been investigated for estimating T_j without modifying the die or encapsulating package [60]. Nevertheless, estimating T_j requires re-calibration and/ or complex thermal modeling to compensate for the aging effects.

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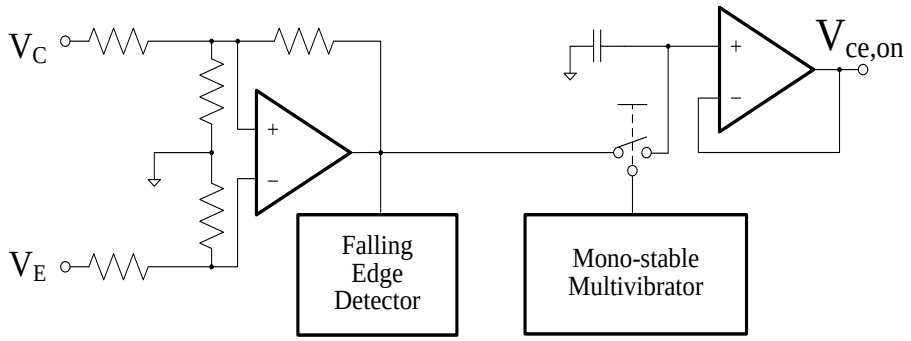
Another approach is based on directly using the device parameter information to estimate the lifetime. In [61], an easy to implement remaining useful lifetime (RUL) estimation model for power FET has been proposed based on the variations in on-state resistance ($R_{ds,on}$). This model directly utilizes $R_{ds,on}$ variation due to aging in contrast to other models which first calculate T_j based on electrical parameters [60] and then estimate switches' lifetime using stress models based on the calculated T_j [59].

Moreover, as discussed earlier, several electrical parameters have been reported in the literature as useful failure precursors for IGBTs as well [62], [43], [44], [48-50]. Among these failure precursors, $V_{ce,on}$ measurement methods have been studied extensively [51]. Besides, a comprehensive discussion is presented in [63] about non-invasive condition monitoring topologies and the corresponding issues in their implementation. Nevertheless, one of the major issues is integration of aging monitoring circuit(s) in to the existing design of converter particularly the gate driver circuit.

In [64], authors have shown utility of $V_{ce,on}$ results for degradation detection but utilized pseudo V_{th} measurement for estimating T_j. The circuit schematic is reproduced in Figure. 4.1. They have used T_j information for $V_{ce,on}$ correction however, V_{th} is affected by aging and pseudo V_{th} measurement requires *Kelvin* emitter connection which is uncommon in discrete package IGBTs. V_{ref} indicated in red color is generated based on the current associated inductive voltage drop in the *Kelvin* emitter. Similarly, in [65] and [66] circuits details have been given for capturing a variety of aging precursors including both $V_{ce,on}$ and V_{th} along with pseudo real-time capability but require too many additional components and may not fit easily in a compact gate driver.



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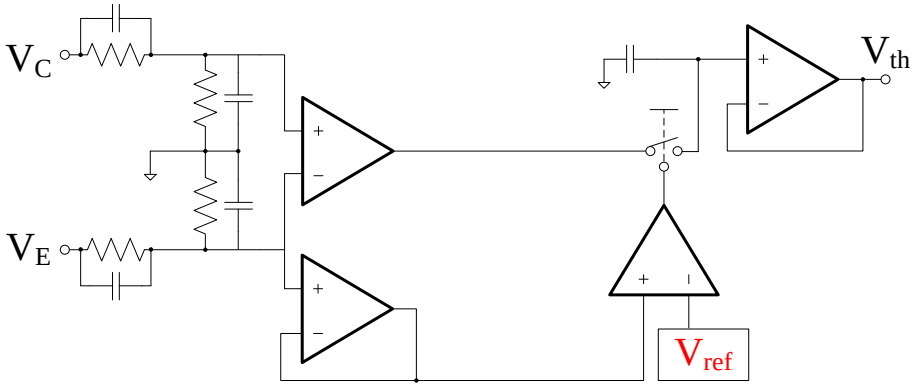


(b)

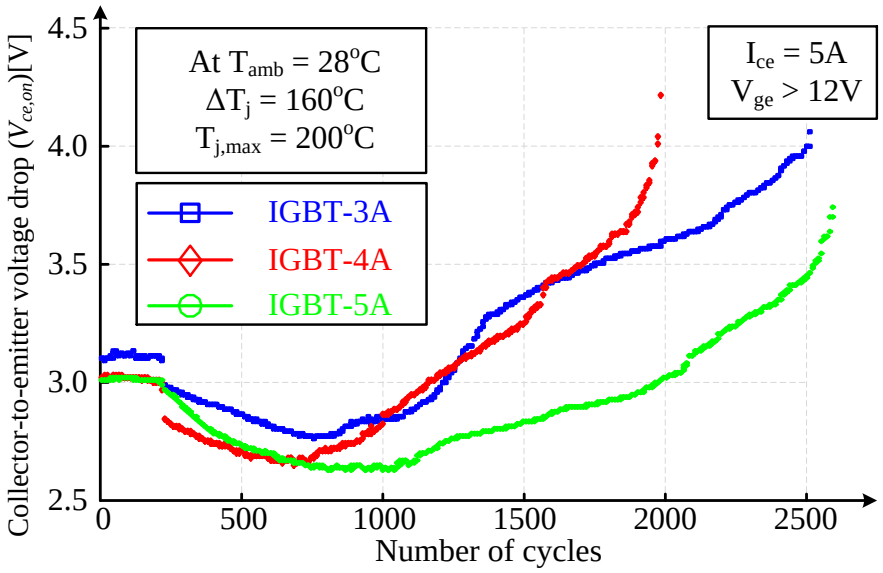
Figure 4.1. Simplified circuit schematic proposed in [66] for monitoring; (a) $V_{ce,on}$ and (b) V_{th}.

Moreover, in the literature various failure threshold limits for $V_{ce,on}$ have been discussed; such as 5% [67], [68], 15% [56] and even 20% [69]. Similarly, a failure limit of 20% change has been proposed in [70]. Based on the literature review and acquired experimental experience, the failure threshold limit is sensitive issue as it requires either replacement of the IGBT and/ or continuation of operation at degraded performance. So, both factors contribute to increasing the operational cost of power converters. It is therefore recommended to define the limits based on the specific application rather than using general limits.

4.2 Brief Discussion on Identified Failure Precursors

Using the setup described in the previous chapter, online $V_{ce,on}$ data recorded through the NI-DAQ USB 6255card has been analyzed. In Figure 4.2 (a), $V_{ce,on}$ results for few samples tested above safe-operating-area (SOA) or manufacturer specified $T_{j,max}$ limits are shown. As discussed in the previous chapter, the contact crack under thermo-mechanical stresses and fatigues leads to increased electrical contact resistance thus causing a rise in $V_{ce,on}$ curves. Yet, $V_{ce,on}$ curves at nominal collector current (I_{ce}) of 5A follow '*dip before rise'* behavior as shown in Figure 4.2 (a) for above SOA tests apparently due to die-attach solder joints degradation which impacts the thermal resistance alongside electrical resistance. Nevertheless, upon reaching the minimum value, the trend changes to positive and continues to increase until complete device failure.

$V_{ce,on}$ results for few samples tested below SOA are shown in Figure 4.3 (a). Contrarily to the previous observation, an always increasing trend in the $V_{ce,on}$ profile is observed. This shift lies in agreement with the expected outcome of aging tests at relatively low thermal swings [71]. Furthermore, this always increasing trend validates the hypothesis that the accelerated temperature cycling below the maximum temperature of 200°C restricts the solder degradation to a lower level. So, only the positive components of $V_{ce,on}$ dominates the overall $V_{ce,on}$ variations under the given conditions. These results also show good agreement with the results presented in [72] and [73] where similar trends in $V_{ce,on}$ evolution are observed.



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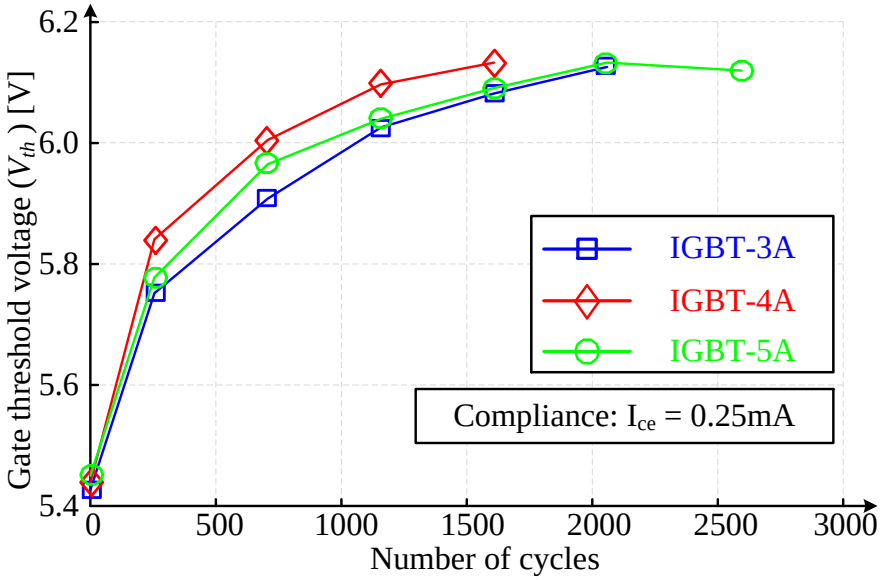
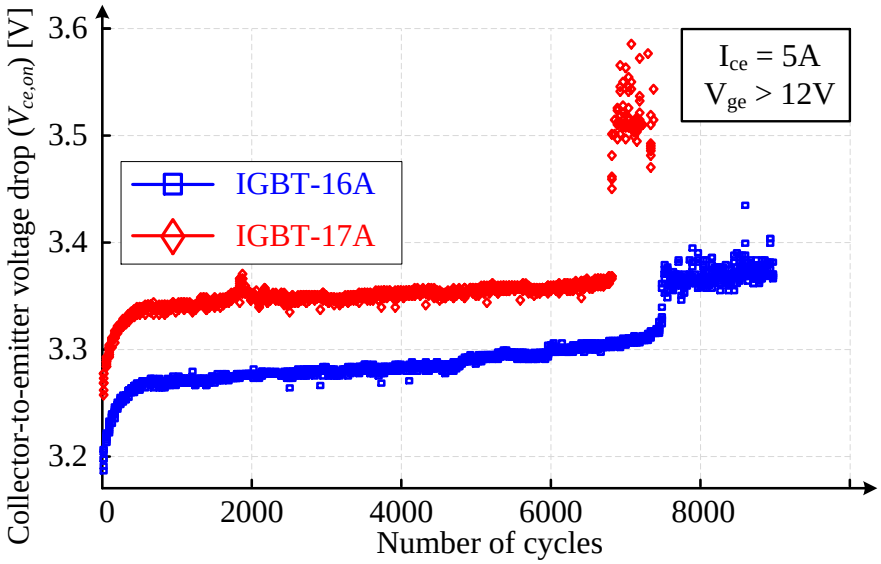
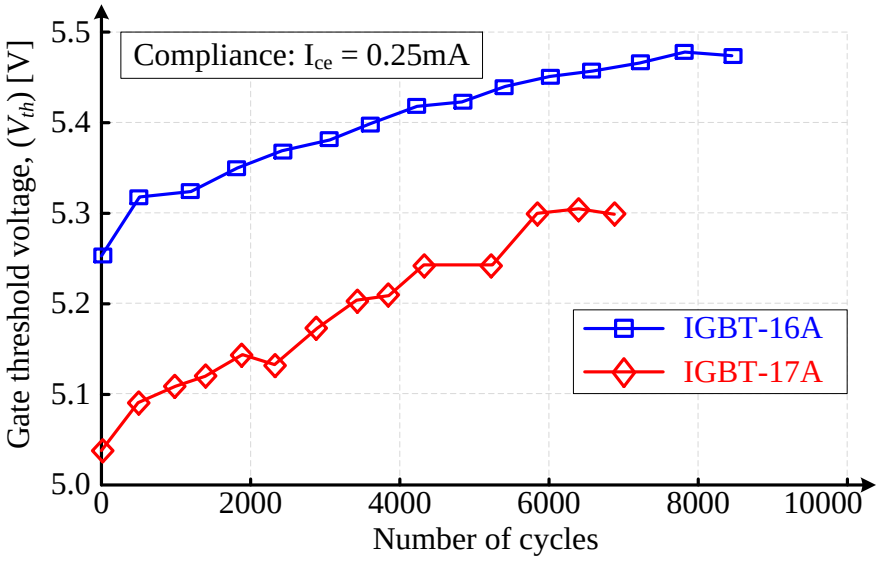


(b)

Figure 4.2. Induced thermo-electric stress aging test results for above thermal SOA limit; (a) $V_{ce,on}$ and (b) V_{th}.



(a)



(b)

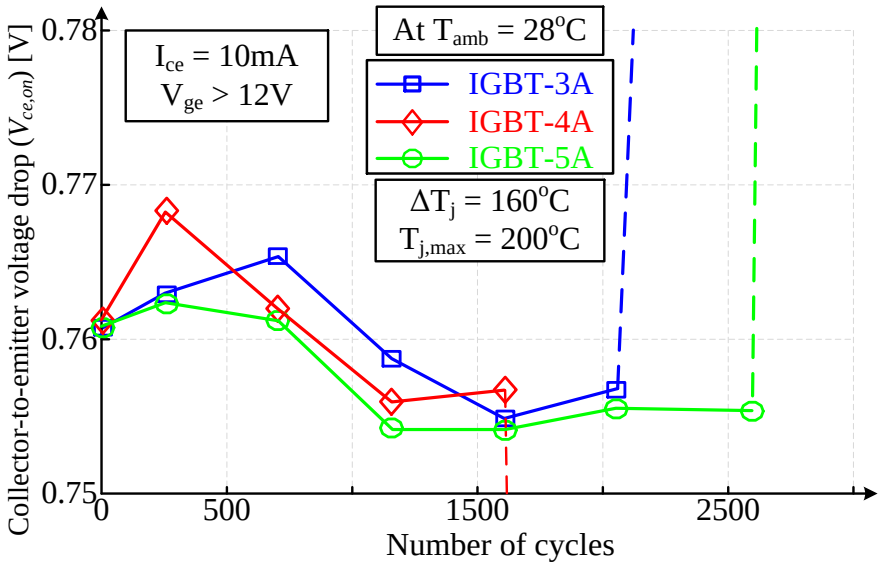
Figure 4.3. Induced thermo-electric stress aging test results for below thermal SOA limit; (a) $V_{ce,on}$ and (b) V_{th}.

Besides the package related failures, gate-oxide degradation is another important failure mechanism which has been discussed in detail in the previous chapters. Besides, as shown in Figure 4.2 (b) and Figure 4.3 (b), a consistent increasing trend in V_{th} is observed during the course of IGBT life time resulting from the decrease in parasitic capacitances [74]. Thus, variation in V_{th} during the device life time can be used to determine gate-oxide aging issues.

As a summary of the previously published results, it has been observed that V_{th} is highly useful as aging precursors when $T_{j,max}$ exceeds the SOA [74]. However, below 100°C its variation reduces drastically because the gate-oxide failure mechanisms remain relatively inactive. On the other hand, the $V_{ce,on}$ shifts highly depend on the applied thermal stress and can only provide a consistent increase for aging tests below thermal SOA [57]. Single failure precursor may give incomplete information. Therefore, to accurately detect and monitor the state of health of IGBTs, a measurement circuit for both V_{th} and $V_{ce,on}$ is proposed to determine the degradation of IGBTs in start/stop system checkups.

4.3 Issues in Measurement of V_{th} and $V_{ce,on}$ Measurements

V_{th} by definition is the gate-emitter voltage at which the channel inversion occurs and current starts to flow from collector to emitter terminals. For in-situ V_{th} measurement, a small current source is required to charge the gate-emitter capacitance until a small I_{ce} starts to flow [75]. For the V_{th} results shown in Figure 4.2 (b) and Figure 4.3 (b), the measurement has already been carried out in the order of few microseconds at the same test current (I_{ce} = 0.25mA) and correspondingly same T_j so, the measurements are considered free from the effects of variations in I_c as well as T_j.



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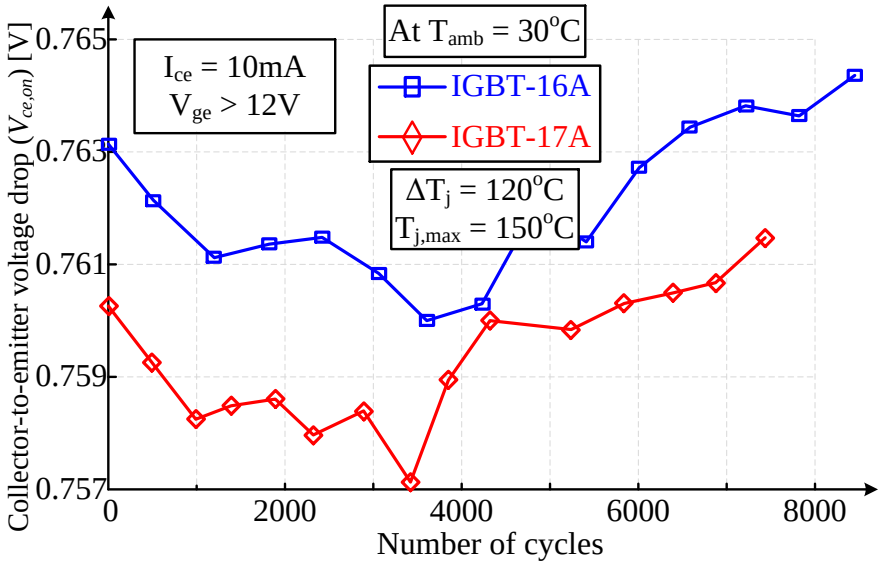


(b)

Figure 4.4. $V_{ce,on}$ measurements at I_{ce} =10mA (a) above SOA thermal limit (b) below SOA thermal limit.

On the other hand, $V_{ce,on}$ is a function of I_c as well as T_j. As discussed earlier, a complex load current compensation is required for trustworthy $V_{ce,on}$ measurement [61]. Measuring $V_{ce,on}$ at a fixed test current level can avoid this compensation problem at the cost of losing real-time measurement capability. Since, V_{th} measurement requires fixed test current through device under test (DUT) and isolation of DUT from the main currents during measurement, observing $V_{ce,on}$ at lower currents alongside V_{th} is feasible.

Before utilizing this low current $V_{ce,on}$ measurement, aging trends at lower current have to be verified. In this connection, Figure 4.4 (a) and (b) shows the $V_{ce,on}$ results at I_{ce} = 10mA for the same set of tested samples whose results at I_{ce} = 5A have been shown earlier in Figure 4.2 (a) and Figure 4.3 (a), respectively.

For the above SOA results shown in Figure 4.4 (a), significantly less voltage dips are seen as compared to the $V_{ce,on}$ measurement at high current (5A) shown in Figure 4.2 (a). The device's self-heating at I_{ce} = 5A causes increased intrinsic carrier concentration, increased carrier lifetime and decreased gate threshold voltage which results in dips in $V_{ce,on}$ curves [57]. On the other hand, the lower current measurement generates much smaller self-heating due to which tiny dips in the $V_{ce,on}$ curves are observed. For the below SOA case as summarized in Figure 4.4 (b), the $V_{ce,on}$ curves at I_{ce} = 10mA show small dips compared to the result at I_{ce} = 5A as shown in Figure 4.3 (a). In fact, $V_{ce,on}$ curves show almost a continuously increasing trend in Figure 4.3 (a). It is evident that at higher current with minimal solder degradation, the contact resistance voltage drop is the dominant component of overall $V_{ce,on}$ but the same contact voltage drop becomes negligible at low current level. Thus, for lower current with minimal solder degradation,

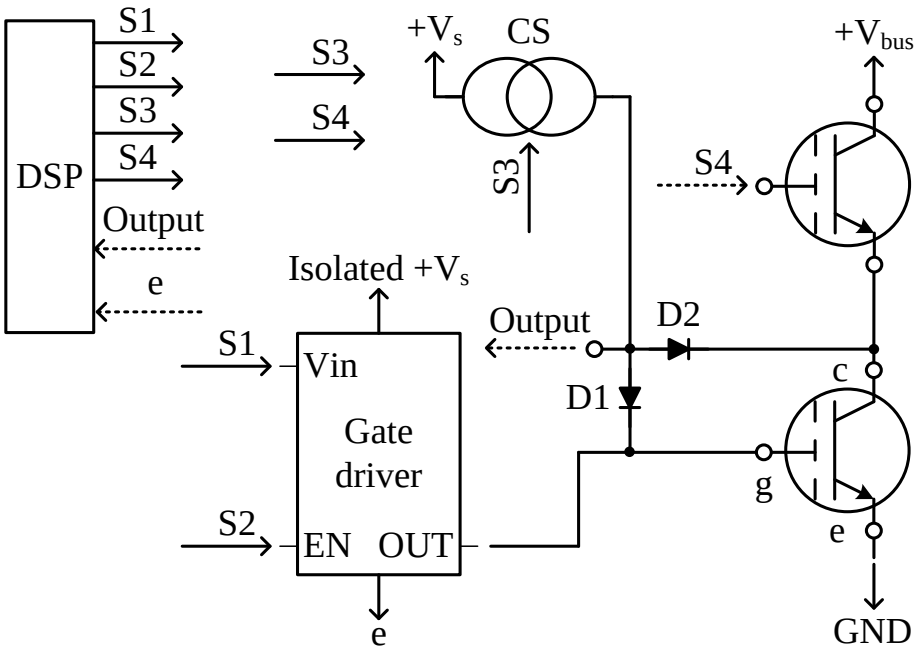
corresponding physical phenomena referred earlier become dominant which cause dips in $V_{ce,on}$ curves.

4.4 Proposed Circuit Description

Based on the aging test results, an in-situ V_{th} and $V_{ce,on}$ measurement circuit is proposed to monitor IGBT aging. The proposed circuit is intended to be used for start-up diagnostic test in power converters before the actual switching operation is activated and/or after it is halted. The schematic of the proposed circuit is shown in Figure 4.5 (a). Apart from the gate driver (GD) components, the circuit features a current source (CS) to provide a small test current; two diodes are included to protect the gate drive circuit from the applied high voltage between C-E terminals during off-state and to provide isolation between CS and GD.

The diagnostic routine involves routing of current from CS through different paths to accurately measure V_{th} and $V_{ce,on}$. In order to achieve this, a set of control signals are generated through DSP namely S1 for IGBT gate signal, S2 to enable the gate driver output, S3 to enable the weak current source and S4 to control the high-side IGBT. The required timing diagram for control signals is illustrated in Figure 4.5 (b).

Specifically, the circuit operates in three modes i.e. V_{th} measurement, $V_{ce,on}$ measurement and normal operation modes as illustrated in Figure 4.6 (a-c). In these figures, red color is used to indicate *active* and blue color for *inactive* current flow paths. During each measurement mode, output and emitter node voltages are fed back to a low-pass filter and then to the ADC pins of the DSP.



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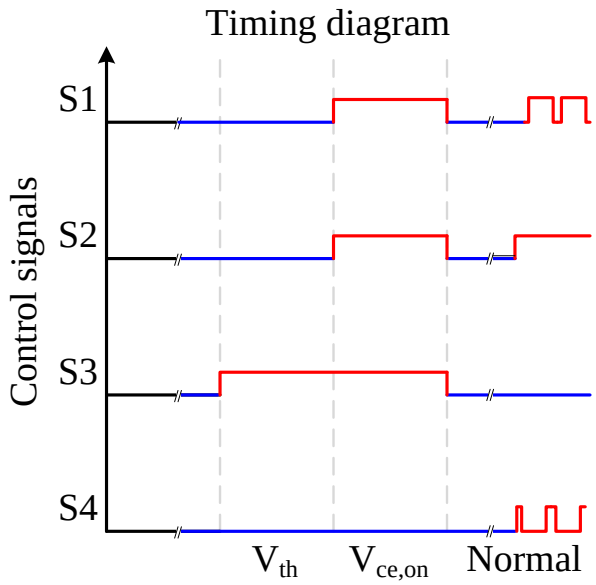

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Figure 4.5. Proposed circuit; (a) schematic, (b) timing diagram for control signals,

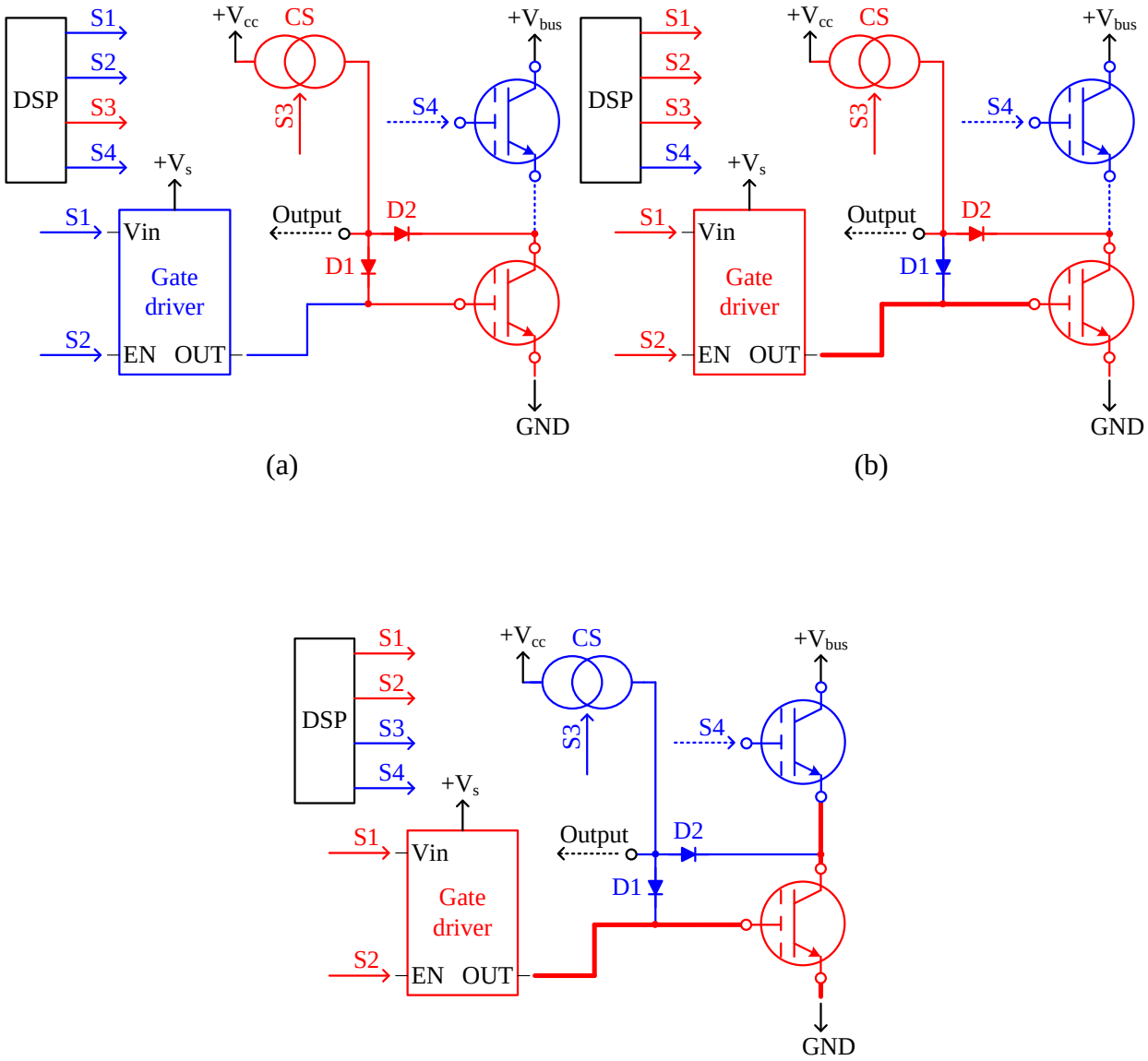


Figure 4.6. Illustration of operation for proposed circuit; (a) V_{th} measurement mode, (b) $V_{ce,on}$ measurement mode and (c) normal gate driver operation.

4.4.1 V_{th} Measurement Mode

As illustrated in the red line in Figure 4.6 (a), the CS is enabled using S3, and the current starts to charge the gate-emitter capacitance C_{ge} raising the gate-emitter voltage (V_{ge}) above the threshold

voltage V_{th}. Afterwards, channel inversion takes place which subsequently lowers the V_{ce} and the CS current is diverted through the collector terminal. At this point in time, the V_{out} reflects V_{th} of the device.

4.4.2 $V_{ce,on}$ Measurement Mode

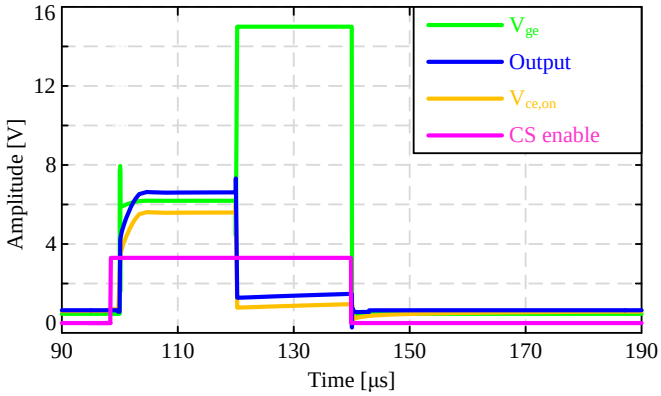
Whereas during $V_{ce,on}$ measurement mode which is also illustrated in Figure 4.6 (b), While S1 and S2 are high, the gate-emitter is charged to gate isolated supply voltage ($+V_s$) using the powerful current source within the gate driver IC. Thus, the CS current flows only through collector terminal causing voltage drop equivalent to device's $V_{ce,on}$. At this point in time, the V_{out} reflects $V_{ce,on}$ of the device.

4.4.3 Normal Operation

Moreover, one of the circuit's prominent features is that the same circuit can be used for normal switching operation without any performance degradation. For normal operation as illustrated in Figure 4.6 (c), CS is disabled by keeping S3 at low while the rest of control signals are toggled to high with exception of S1, which now provides the required PWM signal to IGBT gate.

4.5 Discussion on Results from Proposed Circuit

The PSpice simulation results for the proposed circuit are shown in Figure 4.7 (a). As shown here, V_{out} closely follows V_{ge} and V_{ce} waveforms during V_{th} and $V_{ce,on}$ measurement mode, respectively. To verify the simulated results, a prototype is built. The actual photo of the prototype is shown in Figure 4.7 (b). Figure 4.7 (c) illustrates the experiment waveforms from



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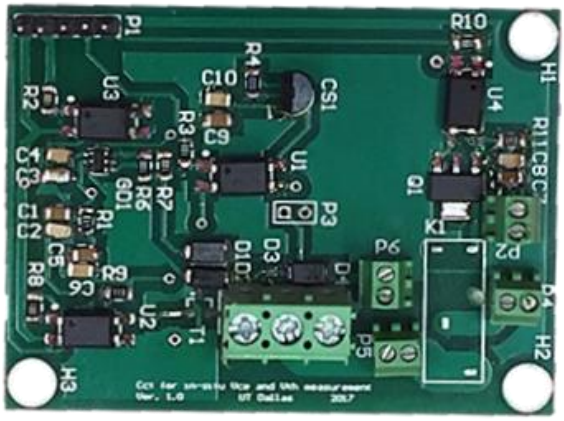

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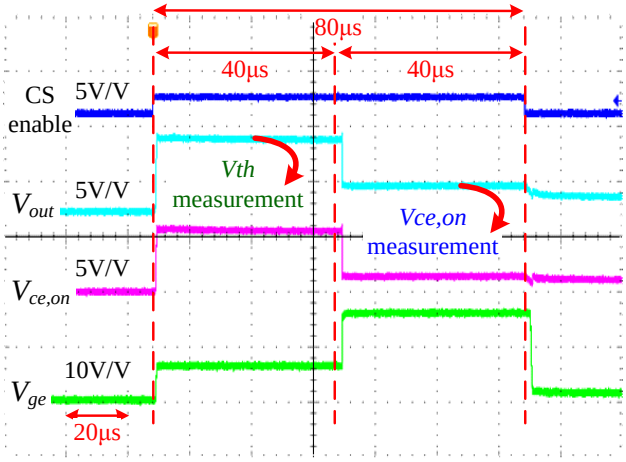
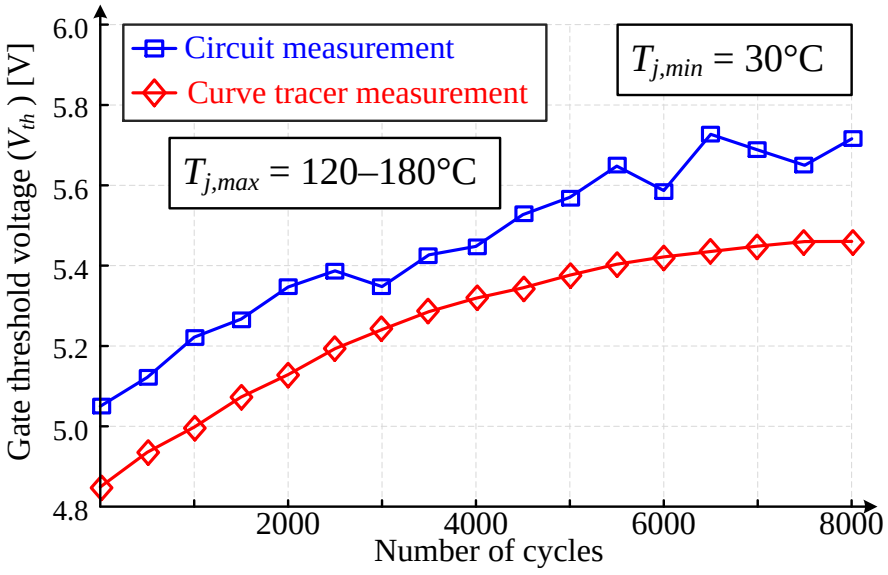


(c)

Figure 4.7. Results of prototype circuit; (a) simulation, (b) actual prototype snapshot containing both the gate driver and aging circuit, (c) oscilloscope waveforms for new IGBT sample.

oscilloscope for a new device under test (DUT). The experiment waveform confirm the simulation results and validates the feasibility of the proposed circuit.

Two aging test-one above SOA and one below SOA limit have been performed to further corroborate the simulation results. During above SOA test, T_j has been kept variable between



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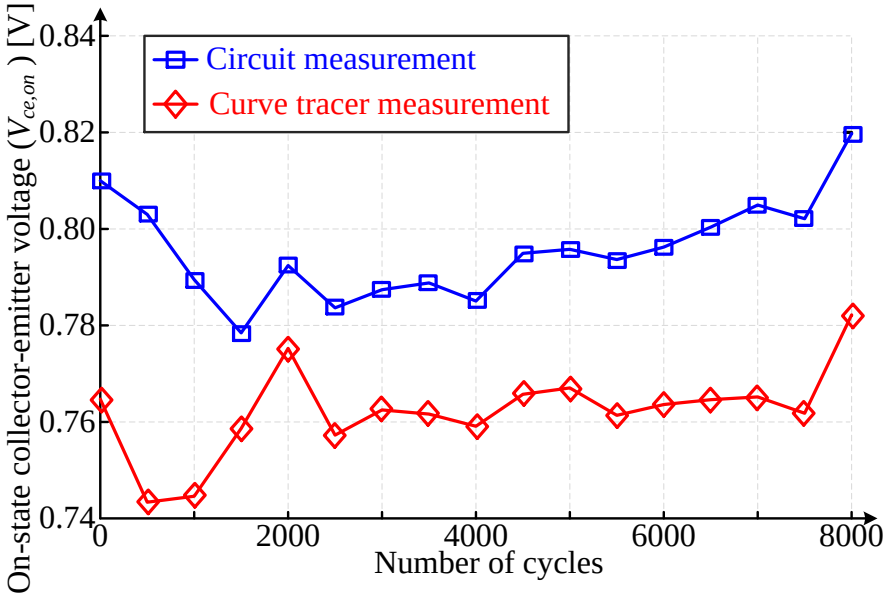


(b)

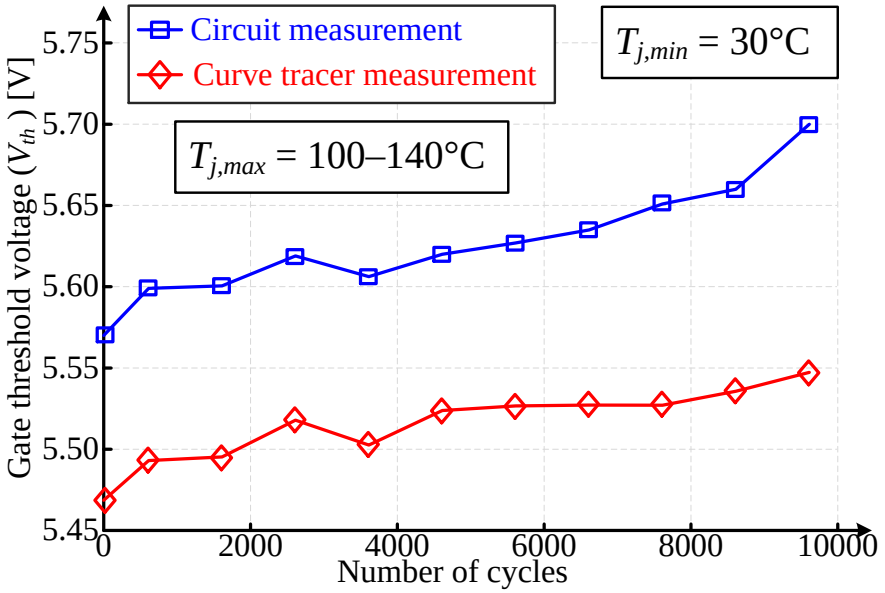
Figure 4.8. Comparative results between proposed circuit and curve tracer for above SOA case; (a) V_{th} and (b) $V_{ce,on}$.

$T_{j,max}$ = 120–180°C with $T_{j,min}$ = 30°C and T_{on} / T_{off} = (12s–45s) / (35s–105s). Similarly, for below SOA test T_j has been kept variable between $T_{j,max}$ = 100–140°C with $T_{j,min}$ = 30°C and T_{on} / T_{off} = (12s–23s) / (35s–55s).

The T_j has been varied to demonstrate monitoring circuit's efficacy under variable loading conditions. After every few hundred cycles, the aged samples are tested using both the proposed circuit and the curve tracer. The aged samples are still functional and show no sign of loss of gate control. Figure 4.8 (a) and (b) provides the V_{th} and $V_{ce,on}$ measurements comparison between proposed circuit and curve tracer for above SOA test. Similarly, Figure 4.9 (a) and (b) provides the proposed circuit and curve tracer measurements comparison for below SOA test. During all these measurement I_{ce} is maintained at approximately 1mA.

As can be seen, the proposed circuit results have offsets of few millivolts since the curve tracer and the proposed circuit use slightly different current values. Other factors like the random thermal noise by the blocking diode (D2) and trace parasitics or random variations in proposed circuit's measurement due to variable DUT placement can also lead to this offset. In this application, trend is critical for monitoring and it is similar between the proposed circuit and curve tracer measurement. Thus, the efficacy of the circuit has been validated.

With the proposed circuit, a digital signal processor (DSP) can be used to continuously monitor the values of the aging precursors. Generally, the DSP is capable to compute the relative parametric changes and the aging trends to estimate the state of health and RUL however, this RUL estimation is out of the scope of paper. . Nevertheless, the circuit measurements are to be used for RUL estimation algorithms based on V_{th} and $V_{ce,on}$ presented in [57] and [74].



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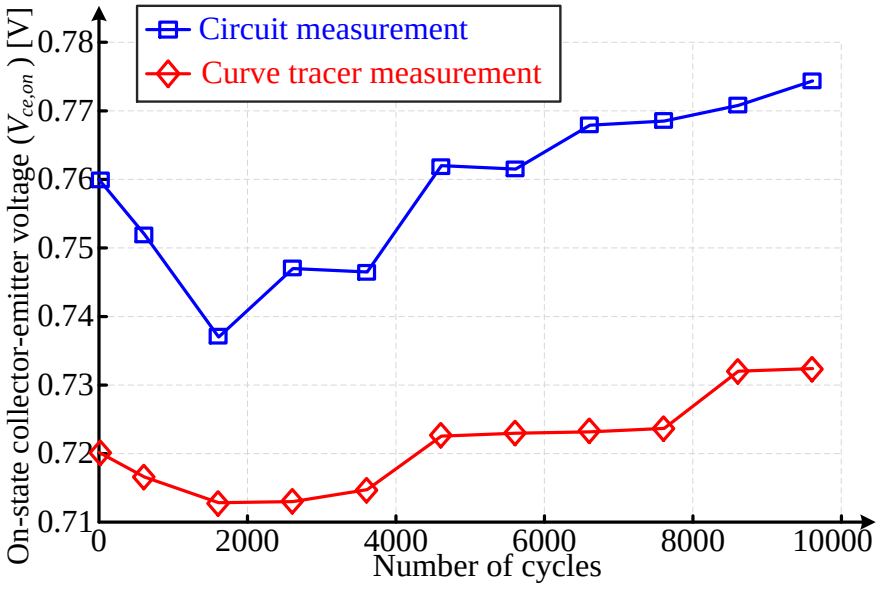

(b)

Figure 4.9. Comparative results between proposed circuit and curve tracer for below SOA case; (a) V_{th} and (b) $V_{ce,on}$.

Another important aspect of the circuit is that it needs to be used as part of start and/ or stop diagnostic test routine. Since, the device aging process spans over much longer time so the information lost during normal operation can be safely neglected. It is also important to incorporate such measurement circuit within the gate driver instead of the main circuit so as to avoid noisy measurement due to trace parasitic inductances. In fact, the proposed circuit is ideally suited for intelligent power modules (IPMs). An IPM generally houses six IGBTs and their respective gate driver next to each other in one single plastic encapsulated package [76]. So, the proposed circuit can be integrated next to respective gate driver circuits within the IPM conveniently.

4.6 Conclusion

To advance the state-of-art converters design, a cost effective in-situ V_{th} and $V_{ce,on}$ measurement circuit has been proposed which can be easily incorporated in conventional gate driver circuits. The proposed circuit can be utilized as part of a regular start and/or stop diagnostic routine in the power converter without any significant RUL estimation error as aging is a much longer process and information lost during normal operation may become trivial.

To compare with the state-of-art aging detection methods, the proposed circuit provides a simple, accurate and easy-to-implement design at the gate driver side for state of health and condition monitoring of IGBTs. With the proposed circuit, no complex compensation and/ or constant correction is required as the $V_{ce,on}$ can be directly used for estimating the RUL of the IGBT. Additionally, V_{th} information can be used to give further insight about the actual die condition and verify the previously estimated RUL using $V_{ce,on}$.

The implementation of the circuit has been validated by comparing the V_{th} and $V_{ce,on}$ measurement with the test results from the highly sensitive and accurate curve tracer. The results show good agreement between the curve tracer and proposed circuit measurements. The measurement procedure takes less than 100μs which is feasible for most real applications.

CHAPTER 5

REMAINING USEFUL LIFETIME ESTIMATION[4]

Discrete package IGBT devices are particularly a popular choice for low power converters. Although, IGBT power modules used in high power applications have been studied in the literature, there are major knowledge gaps regarding reliability and lifetime estimation of discrete devices. In the previous chapters, $V_{ce,on}$ and V_{th} variations have been characterized for discrete IGBT devices exposed to cyclic thermal stresses. Variations in $V_{ce,on}$ are carefully identified and classified depending on different aging mechanisms, stress levels and device structures. Based on the aged test data, a probabilistic framework for remaining useful lifetime (RUL) estimation based on the knowledge obtained by accelerated aging experiments for real-time RUL estimation has been proposed [57]. Specifically, the proposed model uses Gaussian Process Regression (GPR) for applying a Bayesian inference (BI) on RUL estimation of the device under test. Using BI reduces the uncertainty associated with RUL estimation and leads to more accurate results. This concept is also tested by comparing the classical maximum likelihood estimation and GPR estimation results with the ones obtained by accelerated aging tests.

5.1 Motivation

In the case of discrete package IGBT devices, the most common thermally induced failure modes include short circuit and open circuit collector-emitter faults. The root causes of these failures can be the result of package related failure mechanisms. In fact, every power device consists of

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die encapsulated in metal-plastic packaging. Further, the die and packaging itself comprise of several layers of different materials each having different coefficients of thermal expansion (CTE). In accelerated thermal cycling tests, normal and shear stresses are induced across the layers [30]. These stresses result in expansion and contraction both in the die and in the packaging parts causing deformation and degradation, which ultimately leads to failure [74].

Contrary to power modules, discrete package IGBT devices don't have an expensive die-bonded-copper (DBC) layer. As the package contains only one single die, isolation is not required. Even 'co-PAK' package which includes an anti-parallel diode along with the main transistor die does not require die-substrate isolation. Thus, the die is directly soldered onto the copper base plate. In the absence of DBC layer, the large difference in CTEs as well as longitudinal dimensions of Si-die and Cu-base plate layers make the shear stress maximum in the die attach interface. Moreover, with no DBC layer, thermal capacity and thermal time constants are also low. So at lower operating frequencies, it is expected that the die attach solder joint can degrade faster in discrete package IGBT than in a module with DBC layer.

In literature, various studies have identified aging precursors or electrically measurable quantities to determine the wear-out status of the modular IGBTs but fewer studies have inspected the parametric variations in discrete IGBTs, which are important components of low power converters. The essential aging precursor for discrete IGBTs has been identified as the variation in the $V_{ce,on}$ [39]. However, the concept of using $V_{ce,on}$ for estimating RUL has not been discussed, which is the scope of this chapter. It is shown that using the prior knowledge based on the experimental test data helps in accurate prediction of device's future health condition.

Consequently, a useful remaining life time estimation model based on Bayesian inference (BI) under the notion of Gaussian process regression using $V_{ce,on}$ has been proposed.

5.2 Accelerated Aging Test Procedure and Results for PT, NPT and TGFS

The customized accelerated thermal stress-testing system discussed in chapter 2 is used to conduct active temperature-cycling test on discrete package IGBT devices. Briefly, the system comprises of four power supplies, voltage sensing circuits, individual fans for cooling the devices, gate-drive circuits and a NI-DAQ USB 6255 connected to the computer to monitor the on-state voltage drop between collector-emitter terminals of IGBTs. In this study, active convectional cooling has been employed to accelerate cooling.

The tests have been conducted on the PT, NPT and TGFS IGBT device samples with matching power ratings, as have been discussed earlier in chapter 2. The devices under test (DUTs) were subjected to large temperature swings to cause thermally induced degradation across all the layers of the die and packaging. The temperature swing (ΔT_j) has been maintained around ΔT_j=160°C initially with maximum at $T_{j,max}$ = 200°C. Each thermal cycle consisted of active heating followed by forced convection cooling through fans. During the aging process, NI-DAQ board logs $V_{ce,on}$ across each device at the start of every 5^{th} thermal cycle.

Throughout the aging tests, devices' conditions have been verified at regular interval for possible decrease in the resistance between collector-emitter terminals (considered as loss of BV_{ces} capability) using the handheld ohmmeter. The aging process was continued until devices can no longer be controlled (turn on or off) using the gate terminal, which is referred as "loss of gate control". Table 5.1 summarizes the device terminal characteristics after the failure.

Table 5.1. DUTs condition after cycling at ΔT_j =160°C ($T_{j,max}$ = 200°C).

Name	Nf	DUTs condition at failure
IGBT-3A	2594	Always OFF → Open Circuit (cannot turn ON by the gate driver circuit), high leakage current, small G-to-E resistance but significantly higher C-to-E resistance
IGBT-5A	2674	
IGBT-1B	2250	
IGBT-1C	6071	
IGBT-4A	2059	Always OFF → Open Circuit (cannot turn ON by the gate driver circuit), high leakage current, small G-to-E resistance but significantly higher C-to-E resistance
IGBT-2B	1700	
IGBT-3B	2225	
IGBT-2C	4272	
IGBT-3C	3371	
IGBT-4C	4721	

On-line $V_{ce,on}$ measurement of few samples of PT (**A**-series) NPT (**B**-series) and TGFS (**C**-series) are shown in Figure 5.1, respectively, for complete aging period until devices fail to turn on and off. In addition, loss of BV_{ces} is also marked for each device in Figure 5.1. Even though the devices can be turned on or off beyond the end of the cycles (as given in the figure), large variations in the resistance between collector-emitter terminals have been observed compared to the original values. This is considered as loss of BV_{ces} and IGBTs are identified as "failed" when BV_{ces} drops significantly.

In Figure 5.1, after few thermal cycles, a decreasing trend in $V_{ce,on}$ value has been observed for all three series however, this trend converts to increasing trend before the complete device failure. It is also noted that the variations in $V_{ce,on}$ over the whole life time for B- and C-series device samples as shown in Figure 5.1(b) and (c), respectively are significantly lesser than that for A- series device samples as shown in Figure 5.1(a).

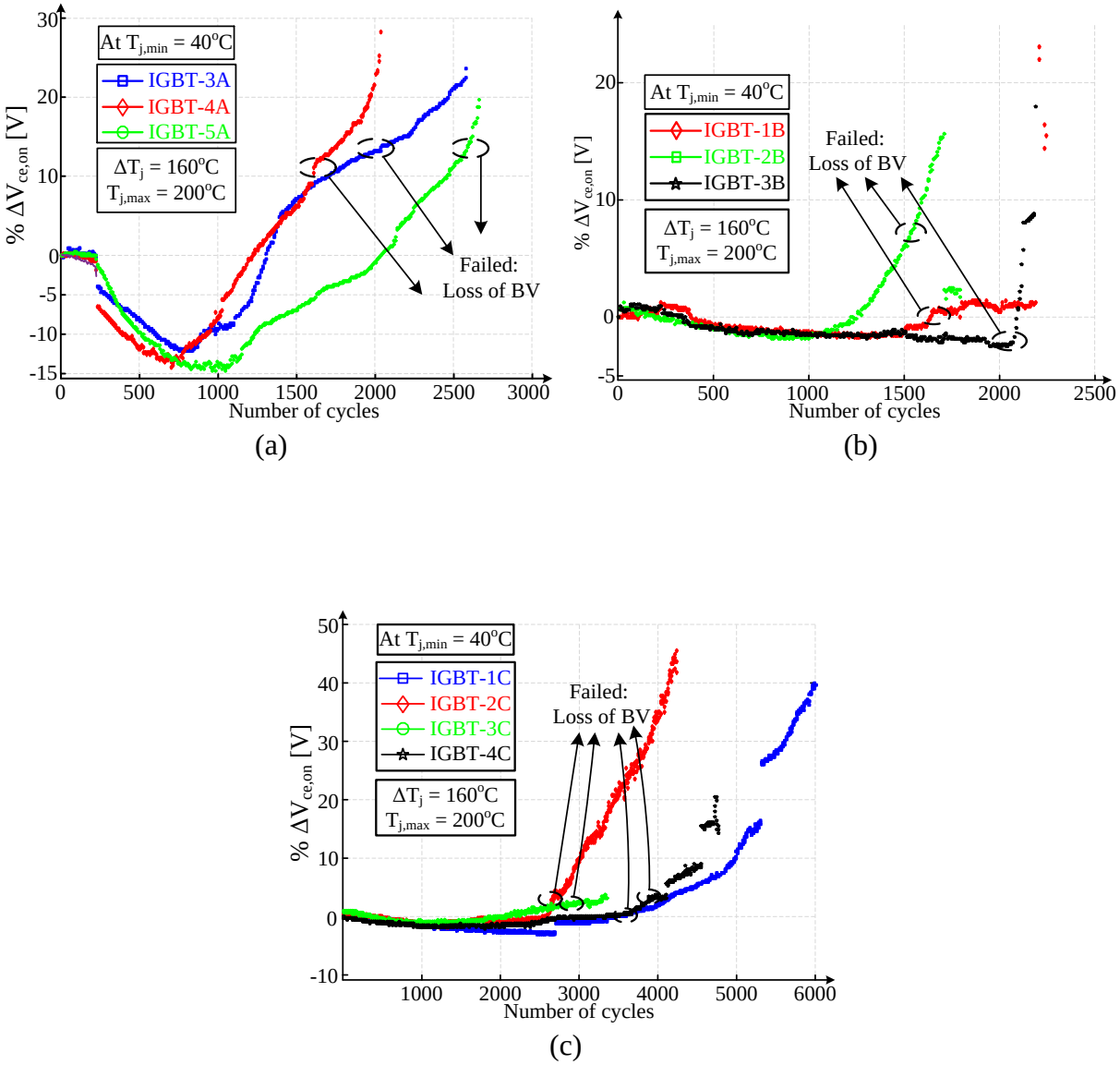


Figure 5.1. $\%\Delta V_{ce,on}$ drop measurement for; (a) A-series, (b) B-series and (c) C-series.

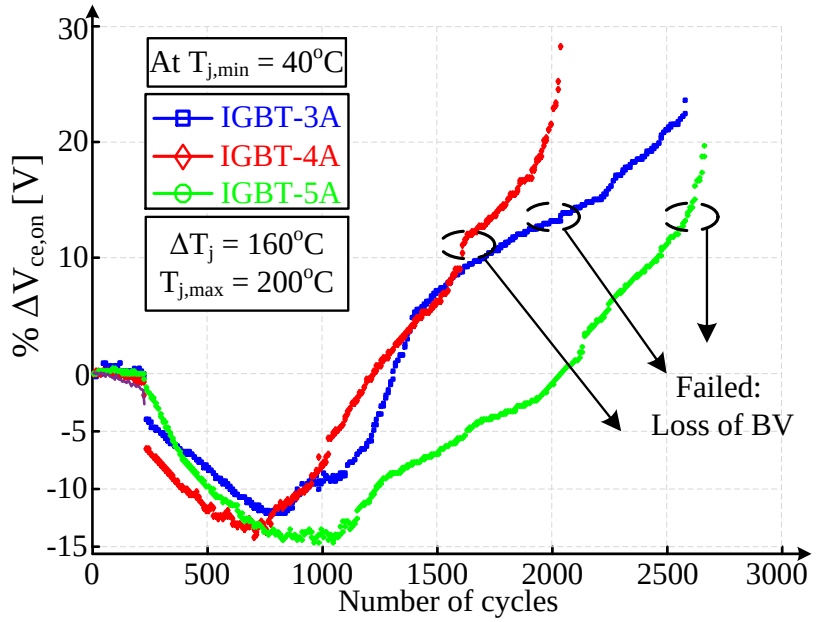
Based on the larger variations observed in A- series devices, more PT device samples were thermally cycled around the same maximum temperature to further investigate and validate the test results. Table 5.2 provides the failure analysis summary for these tested samples and Figure 5.2 shows the $V_{ce,on}$ variations of few samples from these tests.

Table 5.2. DUTs condition after cycling at at different ΔT_j.

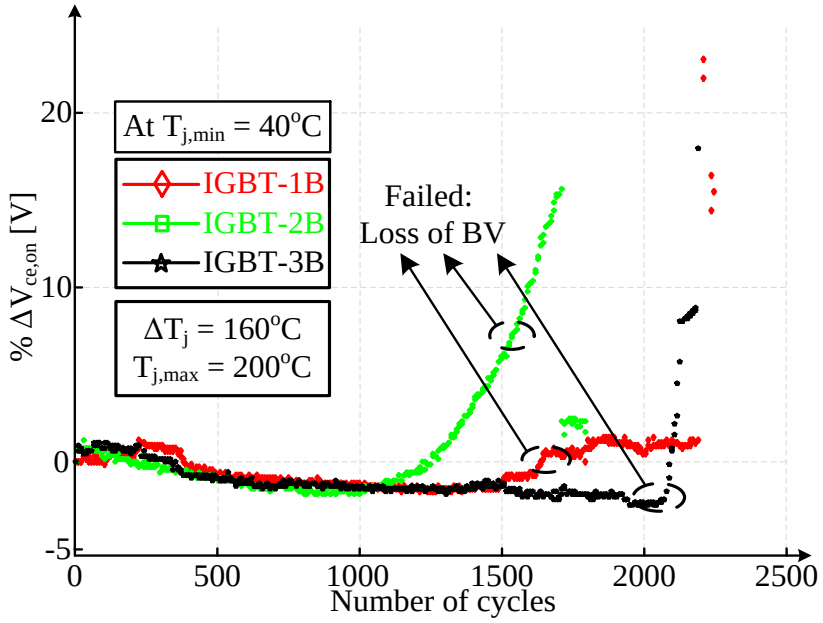
Name	ΔT cycle range	Nf	Switch condition at failure
IGBT-1A	(40-220°C)	1600	Always OFF, low resistance between G-E terminal and very high resistance between C-E terminal
IGBT-2A		1400	
IGBT-3A	(40-200°C)	2594	
IGBT-5A		2674	
IGBT-6A	(30-200°C)	2159	
IGBT-7A		2191	
IGBT-9A	(60-200°C)	3331	
IGBT-10A		3291	
IGBT-12A	(30-205°C)	2308	
IGBT-13A		2411	
IGBT-4A	(40-200°C)	2059	Loss of gate control, No G-E or C-E resistance
IGBT-8A	(30-200°C)	2440	
IGBT-11A	(30-205°C)	2250	

In literature, varying trends have been reported for $V_{ce,on}$ evolution over the device lifetime. An always increasing $V_{ce,on}$ curve is reported for different junction temperature swing in [43] but a decrease in the $V_{ce,on}$ value at the end of device life time compared to its initial value has also been reported in [39]. In [56], a precipitous 17% decrease in decreasing $V_{ce,on}$ curve has been reported too. Nevertheless, the presented results are the combination of both trends and degradation in thermal and electrical impedances are competing for dictating $V_{ce,on}$ variation as discussed in previous chapters.

The degraded thermal impedance due to die-attach degradation causes rise in junction temperature and intrinsic carrier concentration [77], which subsequently lowers overall $V_{ce,on}$ until the curve reaches its minimum value. Beyond that minimum value, the increased electrical resistance starts to dominate more and increases the overall $V_{ce,on}$. It is important to note that both



(a)



(b)

Figure 5.2. *% $\Delta V_{ce,on}$* measurement for extended A- series device samples at a) ΔT_j=140°C and (b) ΔT_j=205°C.

increased minority carrier lifetime or reduced gate threshold voltage due to rising temperature can also decrease $V_{ce,on}$. Contrarily, rising temperature can decrease the carrier mobility, thereby increasing $V_{ce,on}$. So, it is suitable to simplify Equation 2.1 into increasing and decreasing components of $V_{ce,on}$ as given below:

$$V_{ce,on} = V_{ce,on+} + V_{ce,on-} \tag{5.1}$$

These competing mechanisms are illustrated in Figure 3.20 as well.

Also, it is hypothesized that negative tempco for $V_{ce,on}$ coupled with degraded thermal impedance are responsible for significantly larger $V_{ce,on}$ dip in PT samples as shown in Figure 5.1 (a) and Figure 5.2. On the contrary, the positive tempco for $V_{ce,on}$ somewhat compensates the reduction in $V_{ce,on-}$ component which leads to an incremental decrease in $V_{ce,on}$ for NPT and TGFS samples as shown in Figure 5.1 (b) and (c), respectively.

5.3 Test Results at Reduced Temperature Levels

In the previous tests, devices have been cycled at high temperatures to trigger multiple failure mechanism in the devices. In a recent study [71], the effects of lower temperature swing as well as mean temperature on $V_{ce,on}$ have been investigated. So, to develop better understanding about $V_{ce,on}$ profile, more tests have also been performed at lower maximum junction temperature. Again, devices' conditions have been evaluated at regular interval for possible decrease in the resistance between collector-emitter terminals (considered as loss of BV_{ces} capability). The aging test is stopped once this resistance decreases from very high value to some finite value (in the order of kΩ) for the aged device. Figure 5.3 shows the $V_{ce,on}$ plot for few device samples and Table 5.3 provides the failure analysis summary for these tested samples. The thermal stress has

Table 5.3. Summary of device failures at low thermal swings.

Name	ΔT cycle range	Nf	Switch condition at failure
IGBT-14A	(30-180°C)	3592	Always OFF, low resistance between G-E terminal and very high resistance between C-E terminal
IGBT-15A	(30-170°C)	4212	
IGBT-16A	(30-150°C)	8450	
IGBT-17A		7435	
IGBT-18A	(40-140°C)	12955	
IGBT-19A		13095	
IGBT-20A	(28-100°C)	>32000	No failure observed

been lowest for sample IGBT-20A and even after 32kcycles, gradual increase in $V_{ce,on}$ but consistent with other tested samples has been observed.

Comparing Figures 5.3 and 5.1, instead of dip and rise behavior an always increasing trend has been observed in the $V_{ce,on}$ variations in Figure 5.3. This shift is in agreement with the expected outcome of such tests [71]. Furthermore, the always increasing trend validates the hypothesis that accelerated temperature cycling below maximum temperature of 200°C restricts the solder degradation to lower level. Thus, $V_{ce,on+}$ dominates the overall $V_{ce,on}$ variations under the given conditions. Besides, these results show good agreement with the recently presented results in [72] and [73] which show similar trends in $V_{ce,on}$ evolution during aging under minimal solder degradation for comparable thermal stress conditions.

5.4 Challenges in Modelling IGBT Lifetime using Estimated T_j and Proposed Approach

Previously, Palmgren-Miner method has been utilized to determine the IGBT's EoL based on Coffin-Manson Arrhenius model. This method also uses counting algorithms like rain-flow for accurate junction temperature information. Usually, junction temperature cannot be directly

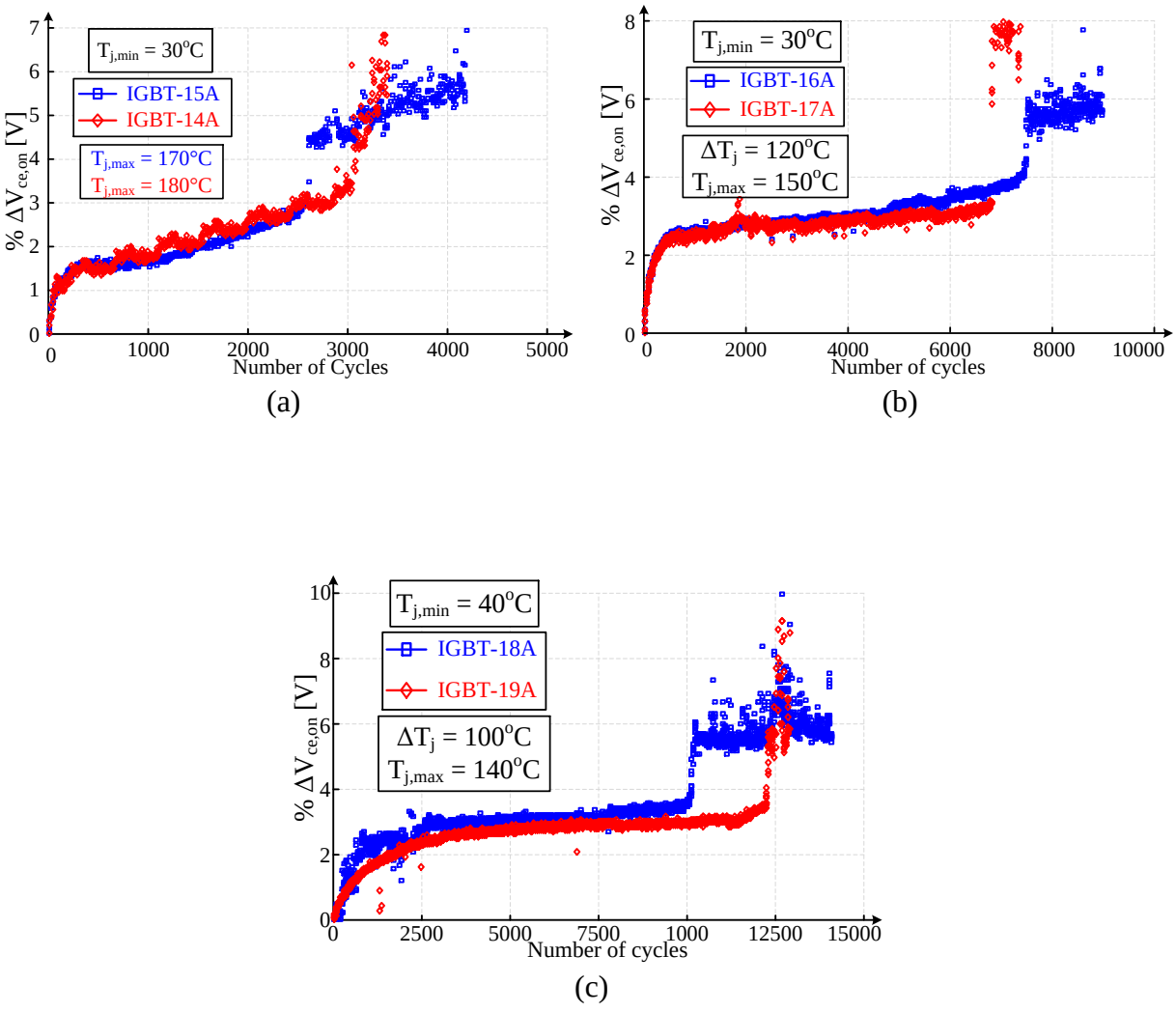


Figure 5.3. $\%\Delta V_{ce,on}$ for PT IGBT at reduced maximum temperature limits; a) $T_{j,max}$=180°C, (b) $T_{j,max}$=150°C and (c) $T_{j,max}$=140°C.

measured and therefore, estimated by using either instantaneous IGBT's power losses or monitoring thermally sensitive electrical parameters (TSEPs).

In the first approach, case temperature value is added to the device power losses to estimate the junction temperature through the thermal impedance model [78 – 80]. It is well known that the thermal impedance degrades significantly due to solder degradation as reported in

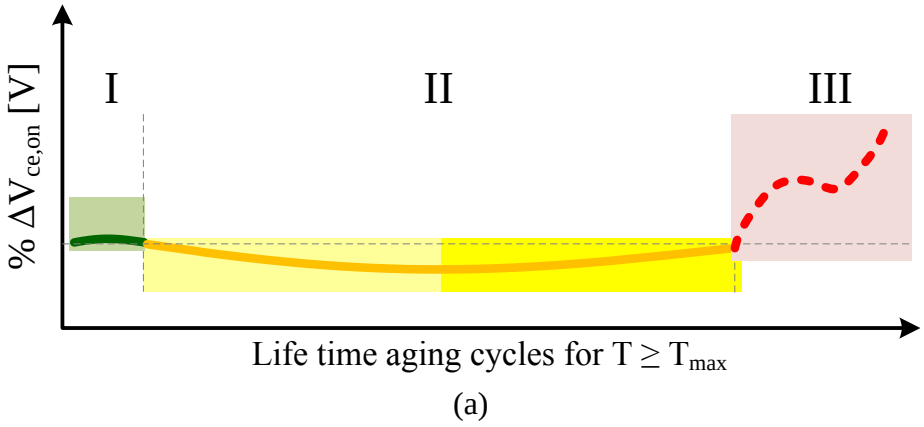
[81, 82]. So, the estimated junction temperature will be incorrect unless regular update to thermal impedance model is available.

The second method uses variations in TSEPs like $V_{ce,on}$ [83] and V_{th} [84] etc. Particularly, $V_{ce,on}$ greatly vary due to aging in solder joints, bond-wires, and metallization layers as discussed and shown in earlier sections. On the other hand, V_{th} remains unaffected by solder die-attach degradation and used to estimate the junction temperature provided there is no degradation in gate oxide layer [84]. Yet, gate oxide degradation and variation in V_{th} with respect to aging has been shown in the earlier sections as well.

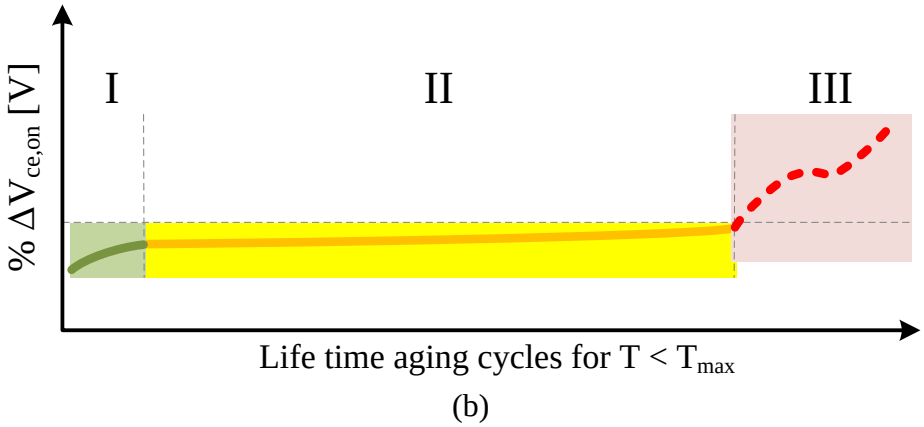
It is realized that instead of using TSEPs information to first calculate junction temperature and then estimate the lifetime, electrical parameter information can be used to directly estimate the lifetime. In [61], an easy to implement remaining useful lifetime (RUL) estimation model for power FET has been proposed based on the variations in on-state resistance ($R_{ds,on}$). This model directly utilizes $R_{ds,on}$ variation due to aging in contrast to other models which first calculate T_j based on electrical parameters [60] and then estimate switches' lifetime using stress models based on the calculated T_j [59].

5.5 Generic Behavior of IGBT under Thermal Stress and IGBT's Lifetime Estimation

The behavior of $V_{ce,on}$ can be generalized as illustrated in Figure 5.4. This generic behavior is important to analyze for generating an early warning signal to the end user before complete device failure. Figure 5.4(a) shows the generic trend for aged devices under multiple degradation mechanisms ($T \geq T_{max} = 200°C$) whereas Figure 5.4(b) depicts the common trend observed for aged devices under contact resistance degradation ($T < T_{max}=200°C$). Although it is difficult to specify the exact regional boundaries for all IGBTs yet, by comparing the results shown in



(a)



(b)

Figure 5.4. Generic variations in $\%\Delta V_{ce,on}$ during IGBT lifetime; for (a) $T \geq T_{j,max} = 200°C$ and (b) for $T < T_{j,max} = 200°C$.

Figure 5.1 and Figure 5.3 with the generic behavior of $V_{ce,on}$ illustrated in Figure 5.4 (a) and (b), it is speculated that region-I and -II constitutes almost the 80~90% of IGBT's useful life time.

In Figure 5.4 (a), Region-I defines the IGBT life duration in which $V_{ce,on+}$ drop dominates the $V_{ce,on}$ behavior. Upon entering region-II, thermal resistance degradation under solder delamination (corresponds to V_{pn} drop) dominates the $V_{ce,on}$ behavior until the global minimum point is reached for the $V_{ce,on}$ curve. However, beyond that point, the $V_{ce,on+}$ drop starts to

dominate again. In the last region, under the cumulative effect of degradation mechanisms, the increment in $V_{ce,on}$ becomes highly non-linear until failure.

In Figure 5.4 (b), again $V_{ce,on+}$ drop dominates the $V_{ce,on}$ behavior in Region-I. Contrary to Figure 5.4 (a), upon entering region-II, thermal resistance does not undergo severe degradation due to solder delamination. Correspondingly, $V_{ce,on+}$ drop increases due to electrical contact resistance degradation and continues to govern the overall $V_{ce,on}$. In the last region however, under cumulative effects of degradation mechanisms, the increment in $V_{ce,on}$ becomes highly non-linear until device failure (or loss of BV_{ces}).

For the results shown in Figure 5.1, it has been observed that the negative part of the curve constitutes the major part of useful life time for an IGBT. As first model, the negative part of the curve is modeled as the sum of two sinusoidal functions.

$$\Delta V_{ce,on} = \sum_{n=1}^{2} a_n sin(b_n x + c_n) \tag{2}$$

where a_n,b_n and c_n are the empirical coefficients which represent amplitude, frequency and phase shift for the two sine terms in the equation. By using non-linear least square, a representative curve can be fit to the data points. The fitting for devices IGBT-3A, IGBT-1B, IGBT-2C are presented in Figure 5.5. Although, different curves can be fitted with the given function however, the same model produces large variations to model below SOA test results compared to observed measurements. Moreover, with limited number of the observed samples, large estimation errors are observed.

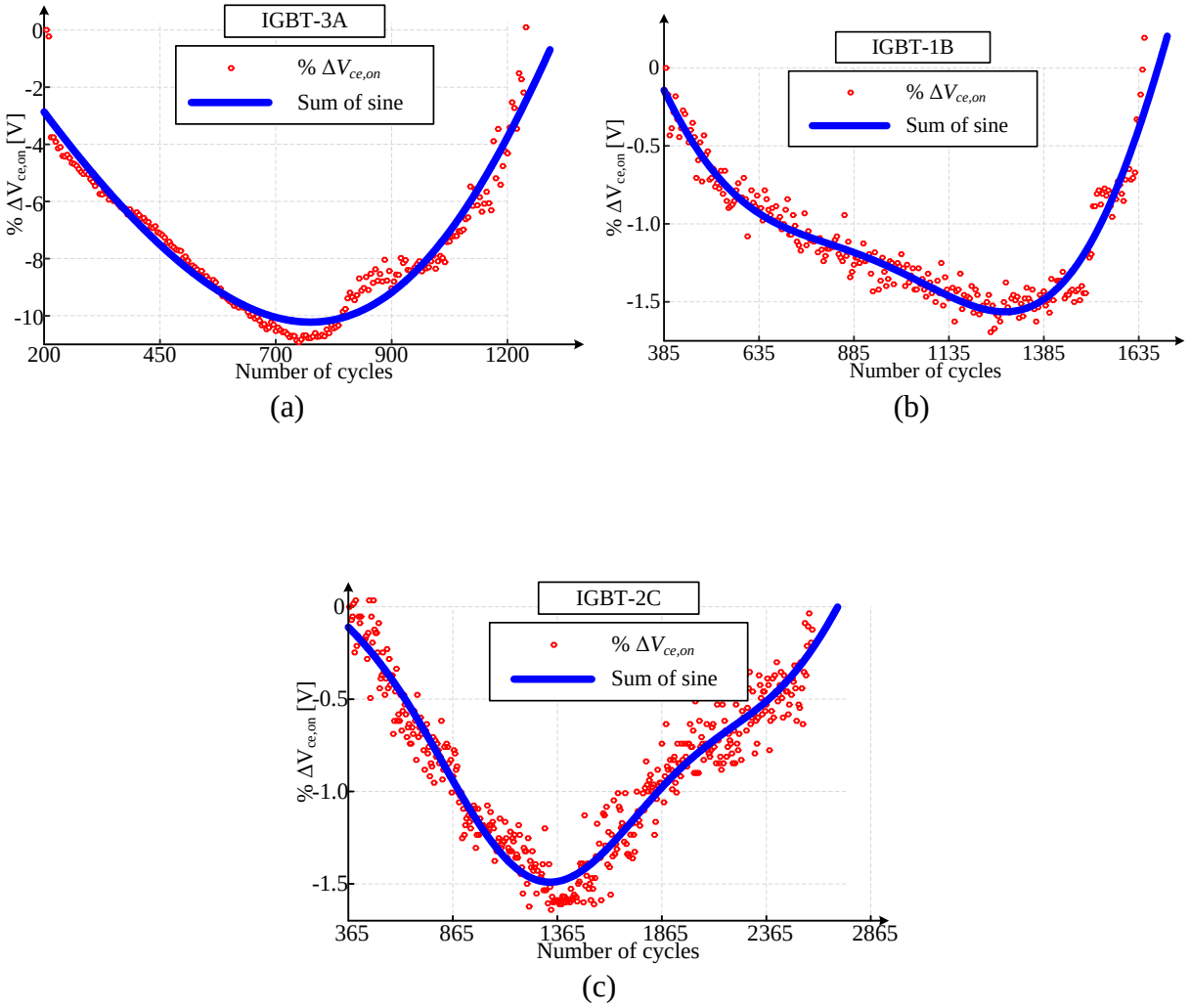


Figure 5.5. Empirical model using sinusoidal functions; a) IGBT-3A, (b) IGBT-1B and (c) IGBT-2C.

5.6 Remaining Useful Lifetime Prediction Based on $V_{ce,on}$ using Gaussian Process

Remaining useful lifetime (RUL) estimation is the process of determining the remaining time to failure of a specific device based on an aging precursor measured from the device. In simplistic terms, RUL is the data extrapolation of the system for predicting system health condition in future. Generally, extrapolation is done by fitting a model to available data points by minimizing

the interpolation error and hoping that this model is valid for future points. Thus, extrapolation is associated with an inherent error.

To overcome this difficulty, another information source needs to be included. The later information can be obtained by doing experiments on the devices with the same type. Devices from the same type are expected to fail for the same reasons and having similar aging precursors. This similarity is another source of information beyond the samples from a device under test. The question is how to merge this source of information with samples from the test device to estimate its RUL. This issue can be seen as a probabilistic problem and accordingly, an RUL estimator can be developed. Moreover, this estimator can also be biased with the knowledge obtained from prior experiments. With Bayesian inference, the estimator can be biased systematically.

In this connection, RUL model based on Bayesian Inference under notation of Gaussian process regression (GPR) has been proposed in this section. Although, GPR is a concept from modern probabilistic theory and has been applied recently for RUL estimation [85] [86] however, the proposed model uses GPR modeling based for applying our prior knowledge, which differs from prior works.

Suppose $f(t)$ is a function of time which represents the $V_{ce,on}$ and accordingly, its failure threshold value V_F can be defined. So, the failure time (t_F) will be time corresponding to $f(t_F) = V_F$. Also, RUL can be estimated by subtracting the current time from failure time. The challenge is that the function $f(t)$ is not known.

Different IGBTs are aged under the same failure mechanisms but they fail with different aging profile. So, there is not a unique curve for the $V_{ce,on}$ rather a group of possible curve. In

traditional RUL estimation this issue is addressed by parameterizing $f(t)$ [87], [88]. Suppose, $f(t, \boldsymbol{\theta})$ is a parameterized version which can capture all possible curves where $\boldsymbol{\theta}$ is the vector of parameters. This means each device's aging profile corresponds to a specific value of $\boldsymbol{\theta}$. For each device, $\boldsymbol{\theta}$ can be estimated using observed values of $V_{ce,on}$ from past to the current time.

In the proposed model, RUL estimation benefits from modeling prior knowledge using a statistical inference. In order to understand the concept of prior knowledge and Bayesian inference, consider a linear model for the $V_{ce,on}$ as a function of time and vector of parameters (i.e. $f(t, \boldsymbol{\theta})$). Suppose $\boldsymbol{x}$ is a time dependent input vector to the regression problem and y is the $V_{ce,on}$. This linear regression model can be defined as:

$$y = f(x) + \epsilon \tag{5.2}$$

$$f(x) = \boldsymbol{x}^t \boldsymbol{w} \tag{5.3}$$

where, $\boldsymbol{w}$ is a weight vector which corresponds to models parameters, and $\epsilon \sim N(0, \sigma_n^2)$ is the measurement noise. For $\boldsymbol{X} = [\boldsymbol{x}_1, \boldsymbol{x}_2, \cdots, \boldsymbol{x}_n]^t$ and $\boldsymbol{y} = [y_1, y_2, \cdots, y_n]^t$ are matrix representation of this training set, the likelihood of these observations is the probability distribution function (pdf) of observing $\boldsymbol{y}$ given $\boldsymbol{X}$.

In the maximum likelihood (ML) philosophy of estimation, $\boldsymbol{w}$ is chosen based on only available data as:

$$\boldsymbol{w}_{ML} = argmax_w p(\boldsymbol{y}|\boldsymbol{X}, \boldsymbol{w}) \tag{5.4}$$

Similarly, this estimator under the assumption of Gaussian likelihood leads to the well-known least-square method [89]. It is important to note that ML estimator is an efficient estimator for interpolation tasks but RUL estimation is an extrapolation task so, ML estimator is prone to large

estimation errors. Usually, extrapolation is associated with a high error since the training data does not have any information about the behavior of $V_{ce,on}$ curve in the future times. So, ML is prone to make erroneous estimation.

In order to improve the estimation, another source of information beyond the training set needs to be added. This information can be obtained using knowledge about the failure cursor behavior during past aging experiments on devices with the same type. It is assumed that the devices tend to fail with a similar trend with acceptable variability among them. This similarity can be used as an extra source of information to increase the estimation accuracy.

Institutively, in the above discussed linear regression problem, ML chooses a $\boldsymbol{w}$ from weight space without any bias but possible $\boldsymbol{w}$ values for a device can be determined using past experiments. So, the estimator can be biased in such a way that it chooses a value for $\boldsymbol{w}$ from a specific region in weight space.

BI is an effective way of applying this prior knowledge. While ML infers a specific value for an unknown parameter, BI extracts a pdf for the unknown parameter using the Bayes rules given as:

$$p(\boldsymbol{w}|\boldsymbol{y},\boldsymbol{X}) = \frac{p(\boldsymbol{y}|\boldsymbol{X},\boldsymbol{w})p(\boldsymbol{w})}{p(\boldsymbol{y}|\boldsymbol{X})} \tag{5.5}$$

where $p(\boldsymbol{w})$ is called prior pdf and models prior knowledge about the possible values of $\boldsymbol{w}$ without having any sample while $p(\boldsymbol{w}|\boldsymbol{y},\boldsymbol{X})$ is called the posterior pdf which models uncertainty about the value $\boldsymbol{w}$ after having an observation set. Having the posterior pdf, one way of choosing a specific value for weights is the maximum posteriori probability (MAP) estimation.

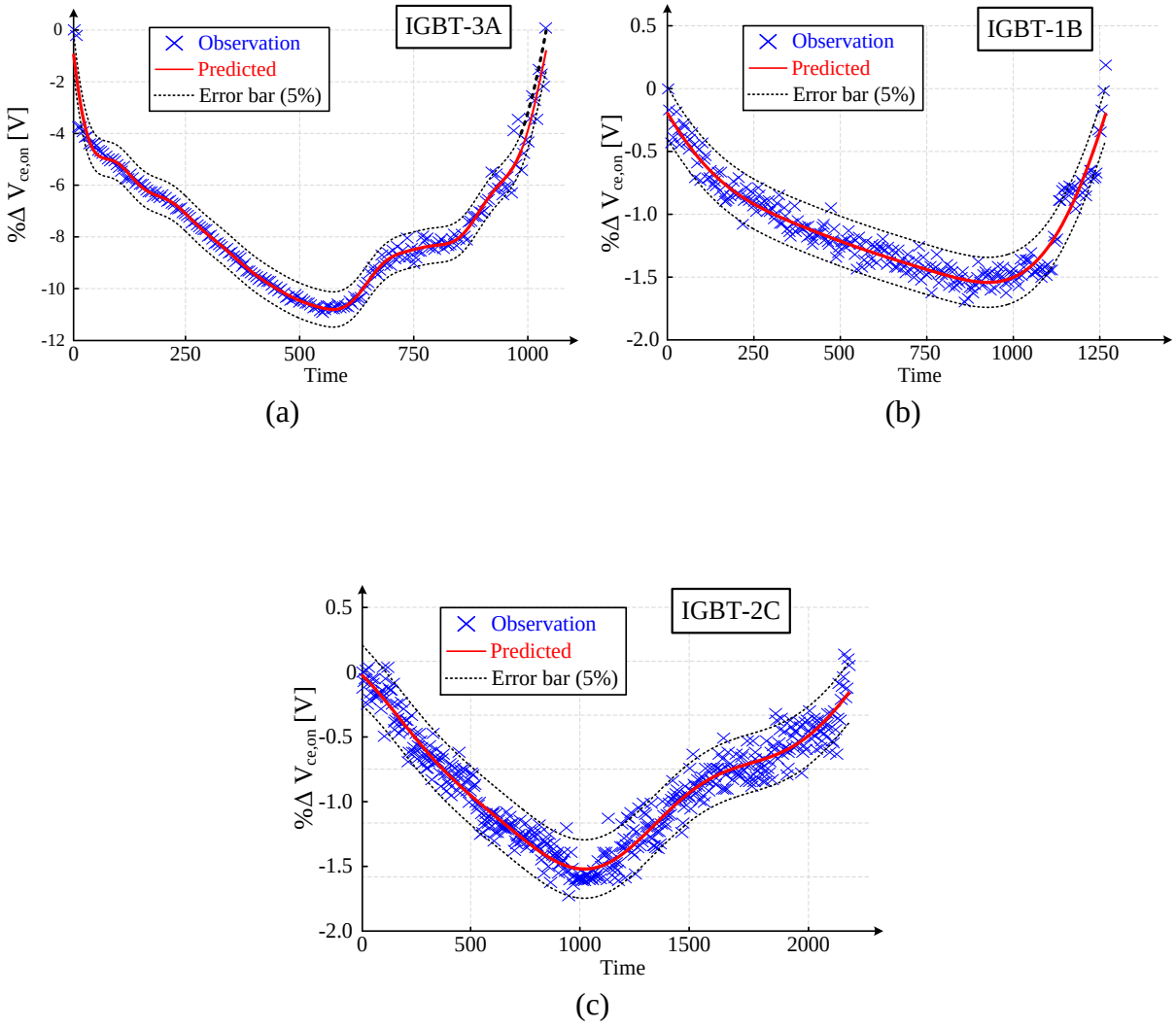


Figure 5.6. GPR based curve fitting with square exponential covariance kernel using all training data samples and no prior knowledge for: (a) IGBT-3A, (b) IGBT-1B and (c) IGBT-2C.

Furthermore, MAP can choose $\boldsymbol{w}_{MAP} = argmax_w p(\boldsymbol{w}|\boldsymbol{y}, \boldsymbol{X})$. Yet, the denominator of posterior is not a function of $\boldsymbol{w}$. So, now $\boldsymbol{w}$ can be obtained as:

$$\boldsymbol{w}_{MAP} = argmax_w \, p(\boldsymbol{y}|\boldsymbol{X}, \boldsymbol{w}) p(\boldsymbol{w}) \tag{5.6}$$

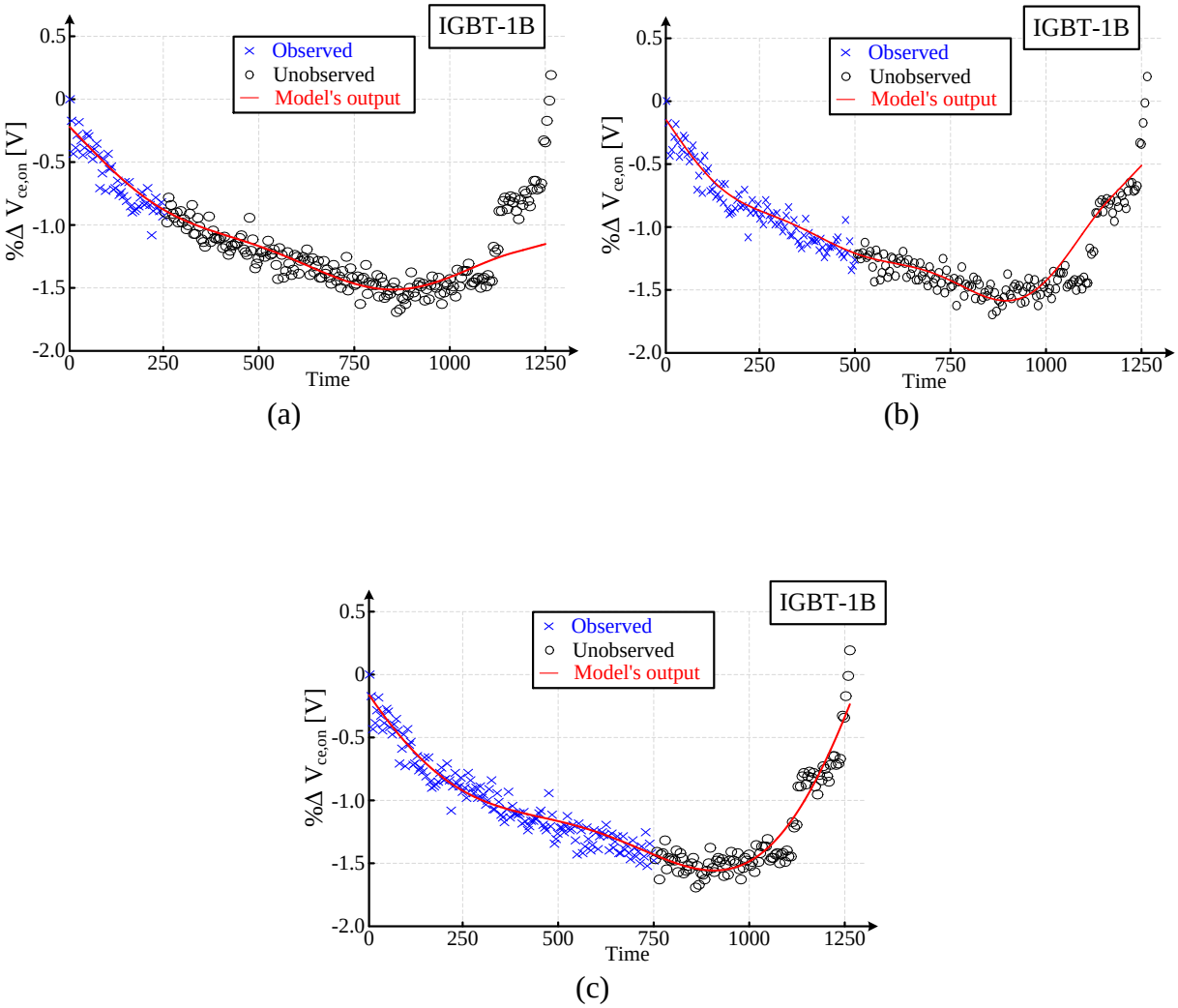


Figure 5.7. GPR based curve fitting with square exponential covariance kernel using all training data samples and no prior knowledge for: (a) IGBT-3A, (b) IGBT-1B and (c) IGBT-2C.

The difference of ML and MAP is the prior pdf i.e. compare Equation 5.4 and Equation 5.6 which can be obtained from training data of the past experiments. Finally, the square exponential covariance kernel has been used to develop the model [90], [91].

Figure 5.6 shows the fitted curve with this model (V_F = 0) for few tested samples. It can be seen clearly that GPR can fit the $V_{ce,on}$ with different shapes very well. For applying the prior knowledge prior pdf has to be specified however, as per the assumption this pdf is Gaussian so

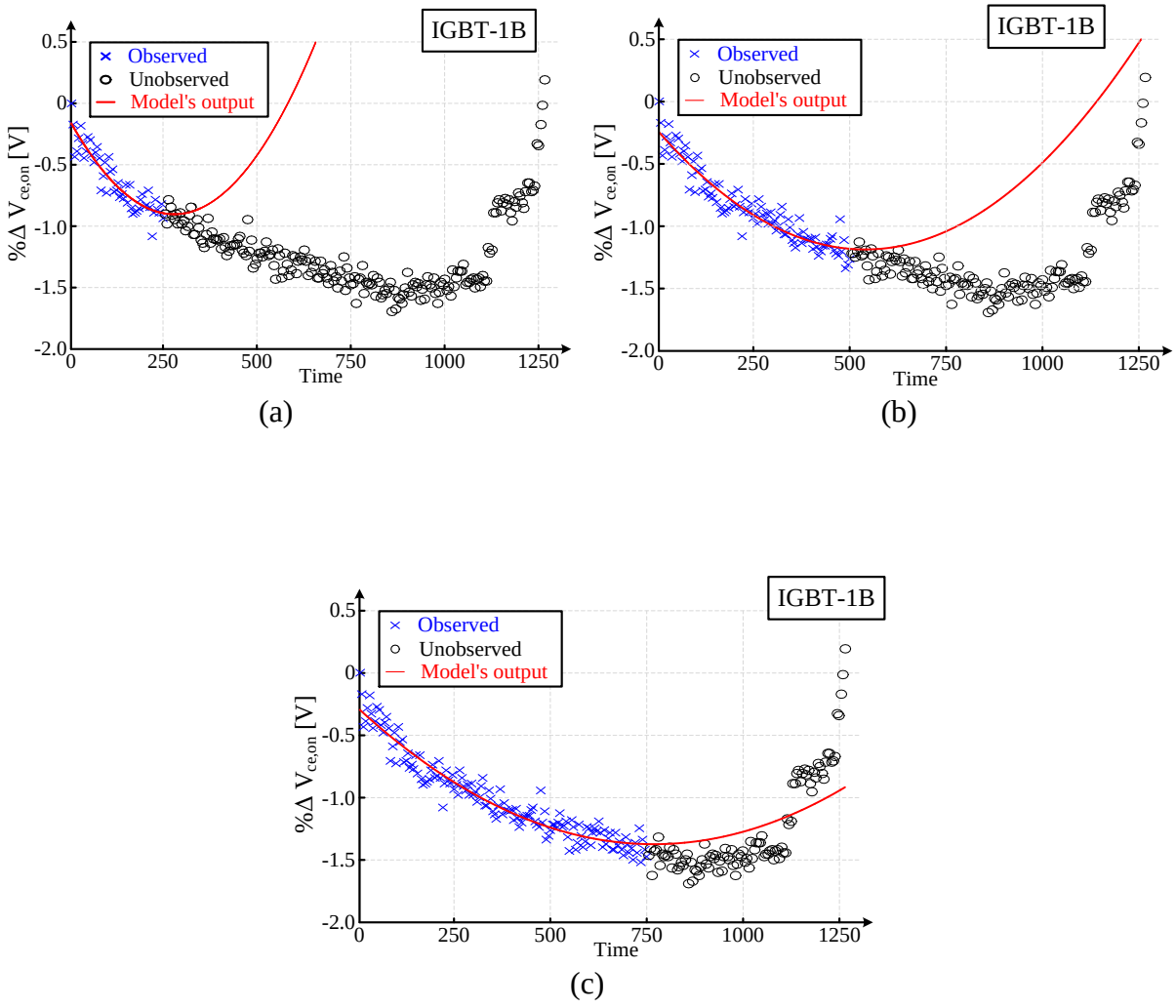


Figure 5.8. A polynomial model has been used to fil $\%\Delta V_{ce,on}$ using the ML estimator after observing: (a) 50 points, (b) 100 points and (c) 150 points.

only its mean and covariance matrix has to be characterized. Using GPR for all the experiments, these quantities are estimated based on the $V_{ce,on}$ data. Then, the vector $\boldsymbol{w}$ takes different values for each device which is used to estimate mean and covariance of prior pdf. Figure 5.7 shows the effect of applying the prior knowledge in fitting a curve to $V_{ce,on}$ using MAP with different number of observed points. The efficacy of GPR under the notion of BI using prior knowledge

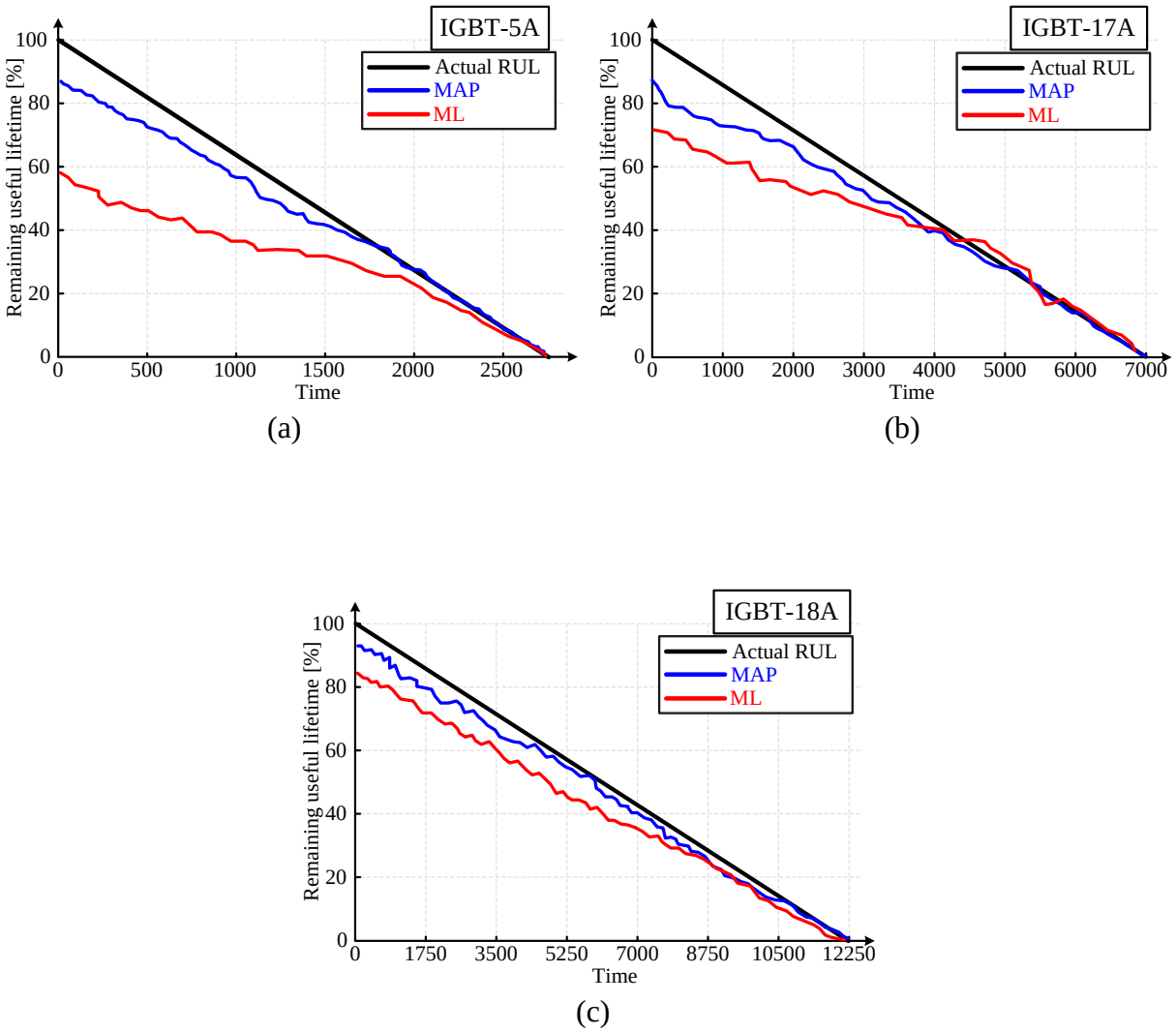


Figure 5.9. Absolute % error in RUL estimation stated for three different devices using GPR with prior knowledge (MAP estimator) and without prior knowledge (ML) for (a) IGBT-5A (b) IGBT-17A and (c) IGBT-18A.

can be seen by comparing Figure 5.7 with Figure 5.8. As clearly seen, the extrapolation error in MAP is much less than that in ML method.

In the last step, accurate RUL estimation can be made by evaluating the intersection of fitted GPR and V_F which needs a numerical solution. Since, the sampling rate for $V_{ce,on}$ measurement is very low during the aging test (almost 1 measurement / thermal cycle = 1Hz), an

embedded processor can estimate the intersection point by a binary search algorithm at minimal computational cost. This makes the real time implementation of the RUL estimation algorithm possible on an inexpensive embedded processor. Figure 5.9 shows the results of RUL estimation for three devices and it can be seen clearly that the MAP produces accurate estimation results compared to that of ML.

5.7 Conclusion

In this chapter, the effect of underlying physical phenomena on evolution of $V_{ce,on}$ under temperature-cycling test for samples of different discrete package IGBT technologies has been investigated. The trends in $V_{ce,on}$ curves has been observed to change with the applied level of thermal stress. At higher temperature, '*dip before rise*' curves have been obtained for all the tested samples suggesting interaction of multiple failure mechanisms. Conversely, at lower temperature, an always increasing trend has been observed in $V_{ce,on}$ curves. Based on the findings, $V_{ce,on}$ has been categorized as a function of maximum junction temperature as well as useful aging precursor. Utilizing this important characteristic, an RUL estimation model using GPR biased with BI has been proposed. It has also been shown that using BI can increase the accuracy of RUL estimation by estimator biasing to utilize the knowledge obtained through prior experiments.

CHAPTER 6

SUMMARY

Since 1980s, IGBTs have been improved in terms of both performance and package density to reshape power electronics industry and associated fields. Contrary to the previous design practices, modern power converters are designed based on the goal of providing continuous performance till the end of life of their main switching devices like IGBTs. Particularly, such designs are highly desirable for safety critical systems. Still, there are few key challenges in fully incorporating innovative prognostic designs and self-diagnostic schemes. Particularly, unavailability of on-field device failure data, suitable monitoring circuits and corresponding lifetime estimation tool are few areas which have to be worked on. Accordingly, this dissertation addressed the health monitoring of discrete IGBTs based power converters by first identifying the aging and failure mechanisms and aging precursors, developing in-situ aging precursors monitoring circuit and lastly, proposing remaining useful lifetime estimation tool.

A major challenge is the unavailability of on-field data for which a comprehensive device characterization is required to determine suitable aging precursors for online state of health monitoring. This information is critical for developing early warning system and subsequently, lifetime extension algorithms. Moreover, discrete power semiconductor have not been thoroughly studied and analyzed by the previous researchers in their publications as well.

Device characterization for identifying potential aging mechanisms and aging precursors requires on-field failure data collection. Since, the devices are manufactured to be operational for few several years therefore, accelerated aging test are employed to fasten the process.

Different types of discrete package IGBTs namely, punch through (PT), non-punch through (NPT), and trench gate field stop (TGFS), are tested. The device samples are aged in custom built aging setup by applying a variety of cyclic thermal stress levels. A state-of-art curve tracer is also used to characterize these devices at regular intervals as well before failures. Some of the important *i-V* characteristics like breakdown voltage, gate leakage current, gate resistance, gate charge, parasitic capacitances and gate threshold voltage have been discussed in detail. Furthermore, to confirm the hypothesis about probable aging mechanisms, failure analyses tools such as acoustic analyses, cross-sectioning and de-capsulation are used.

Overall, a consistent and predictable variation with respect to applied stress has been observed in on-state collector-emitter drop indicating die attach degradation and bond-wire issues. Yet because of non-monotonic variations and negative sags due to negative temperature dependence for PT devices, another aging precursor has to be sought. Alongside, gate threshold voltage has been investigated in much detail. This parameter is suitable to detect gate-oxide aging as well as complement on-state drop as well.

As a second step in advancing current device health monitoring system, a cost effective in-situ monitoring circuit has been developed. The monitoring circuit which measures both aging precursors can be easily incorporated in conventional gate driver circuits. As one of the key advantages, $V_{ce,on}$ monitoring circuit does not require complex compensation and re-calibration like some of the earlier methods. The proposed circuit can measure $V_{ce,on}$ and V_{th} in the order of micro-seconds during system start/ stop diagnostic test routine . The measurement results of the proposed circuit are also compared with those from curve tracer (Keysight B1506A) to validate its utility as well.

Based on the knowledge about IGBT aging mechanisms and associated characteristics, estimation of remaining useful time is possible. Generally, several variants of Palmgren-Miner rule with Coffin-Manson models based on the estimated junction temperature information have been proposed in the literature. However, these models provide only rough estimate for the end of life by counting the junction temperature cycles. Major reasons for estimation errors are the lack of physical device structure information in the model and estimation errors during junction temperature information acquisition. Nevertheless, the first two chapters of this dissertation present the summary of aging mechanisms and also, discuss certain electrical parameters which vary consistently with thermal stress induced aging. Therefore, such parameters or aging precursors can be used for lifetime estimation. Lastly, utilizing this knowledge, a remaining useful lifetime estimation model using Gaussian process regression biased with Bayesian inference has been presented. The results from the model are compared with typical maximum likelihood model as well. It has also been shown that using Bayesian inference or the prior experimental knowledge increase the lifetime estimation accuracy.

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BIOGRAPHICAL SKETCH

Syed Huzaif Ali received his BE degree in electronics engineering from NED University, Karachi, Pakistan, in 2010. He is pursuing his PhD at The University of Texas at Dallas, Richardson, TX, USA. He has been working under the supervision of Dr. Bilal Akin. Since, Jan 2015 he has been associated with Power Electronics and Drives Laboratory in the Engineering and Computer Science Department at The University of Texas at Dallas. His research interests include real-time fault diagnosis of power converters and remaining useful lifetime estimation of power devices. He is also a *Student Member* of IEEE since 2016.

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Education

Ph.D., Electrical Engineering (expected graduation in Summer 2018) — GPA 3.867
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M.S., Electrical Engineering, — GPA 3.867
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Projects

- Aging detection and monitoring in variable speed motor drives using IGBT inflection point monitoring.
- Implemented Start-stop diagnostic circuit for aging detection in motor drives for EV vehicles.
- Designed 1.8V/ 150mA Low Dropout Regulators for Portable Applications with fast transient response.
- Designed 1.8V 150MHz high CMRR Fully Differential Amplifier.

Experience

Research Assistant at **The University of Texas at Dallas**, Richardson, TX
sponsored by **Texas Instruments Inc.**, Dallas, TX — [2015 – 2018]

- Developed online inflection point detection algorithm for variable speed motor drives.

- Designed 2-level 1kW dc/ac inverter with in-situ monitoring of on-state collector-emitter voltage drop and gate threshold voltage for IGBTs.
- Developed remaining useful lifetime algorithm for IGBTs based on their on-state collector-emitter voltage drop.
- Failure precursor identification for IGBT under thermal and electrical stress.
- Used C-SAM, T-SAM, de-capsulation and cross-section failure analysis tools to study failure modes of thermally stressed failed IGBTs.
- Designed comprehensive aging setup (HALT) for IGBTs under thermal stress with on-state collector-emitter, collector current and case temperature monitoring.
- Carried out extensive literature review for developing knowledge about current state-of-art for monitoring imminent fault detection and aging prognosis.

Lecturer at **Nazeer Hussain University**, Karachi, Pakistan [2013 – 2014]

- Designed 200W solar battery charger for solar hybrid vehicle.
- Developed Bio-gas pilot plant for faculty of Renewable Energy to provide methane gas for on-campus utilization.
- Setting up Lab for Basic Electronics and Power Electronics.

Assistant Manager at **Space & Upper Atmosphere Research Commission**, Karachi, Pakistan [2011 – 2013]

- Designed closed loop control for satellite ground station antenna by on-off control AC-Motor drives.
- Drafted solutions/ proposals based on exhaustive link budgeting for mutual interference analysis between satellites of Pakistan and satellites of International Administration.
- Demonstrated strong leadership skills by managing a team of four technical staff members and trained them on sat-link budget analysis.

Intern at **Pak Arab Oil Refinery Company**, Karachi, Pakistan [May – Jul 2009]

- Calibrated temperature, pressure and flow sensors installed with the Karachi to Mehmood Kot pipeline, pumps and other equipment.
- Improved Process & Instrumentation Diagrams for transforming into PLC Ladder Diagrams.

Publications

- S. H. Ali, E. Ugur and B. Akin, "Analysis of Vth Variations in IGBTs Under Thermal Stress for Improved Condition Monitoring in Automotive Power Conversion Systems," in *IEEE Transactions on Vehicular Technology* [in *Review*].
- S. H. Ali, X. Li, A. S. Kamath and B. Akin, "A Simple Plug-in Circuit for IGBT Gate Drivers to Monitor Device Aging," in *IEEE Power Electronics Magazine* [in *Press*].
- S. H. Ali, M. Heydarzadeh, S. Dusmez and B. Akin, "Lifetime Estimation of Discrete IGBT Devices Based on Gaussian Process," in *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 395-403, Jan.-Feb. 2018.
- S. Dusmez, S. H. Ali, M. Heydarzadeh, A. S. Kamath, H. Duran and B. Akin, "Aging Precursor Identification and Lifetime Estimation for Thermally Aged Discrete Package Silicon Power Switches," in *IEEE Transactions on Industry Applications*, vol. 53, no. 1, pp. 251-260, Jan.-Feb. 2017.
- S. H. Ali, S. Dusmez and B. Akin, "A comprehensive study on variations of discrete IGBT characteristics due to package degradation triggered by thermal stress," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-6.
- S. H. Ali, S. Dusmez and B. Akin, "Investigation of collector emitter voltage characteristics in thermally stressed discrete IGBT devices," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-6.
- S. Dusmez, S. H. Ali and B. Akin, "An active life extension strategy for power switches in interleaved converters," in *2015 IEEE Industry Applications Society Annual Meeting*, Addison, TX, 2015, pp. 1-8.

Courses

- Power Electronics
- Control, Modeling and Simulation in Power Electronics
- Analog Integrated Circuit Design
- Active Semiconductor Devices
- Adjustable Speed Motor Drives
- Power electronics and drives related topics
- Renewable Energy and Distributed Power Generation Systems
- Power Management Circuits

Skills

- Skillful in MATLAB, C, Code Composer, PSIM, LabVIEW, Altium PCB and PSPICE.
- Familiar with PIC microcontroller series and TI Delfino TMS28335 floating point controller.
- Experienced in using HV power supplies, function generators, fast acquisition oscilloscopes, Keysight B1506a Curve tracer and NI DAQ 6255.
- Documentation: Microsoft office tools (PowerPoint, Word, Excel, Outlook) and Microsoft Visio.

Achievements

- Received **Mary and Richard Templeton** Graduate Fellowship 2017-2018.
- Received 1st prize conference paper award at **IEEE IAS IACC**.
- Received **Mary and Richard Templeton** Graduate Fellowship 2016-2017.
- Winner at national entrepreneurship competition **INVENT-2010**, Karachi, Pakistan.