NOVEL BIDIRECTIONAL SINGLE-PHASE SINGLE-STAGE ISOLATED AC-DC CONVERTER WITH PFC FOR CHARGING OF ELECTRIC VEHICLES

by

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Dedicated to my beloved family and teachers

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by

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This thesis proposes a novel bidirectional single-phase single-stage AC-DC converter for Electric Vehicle (EV) charging application. AC side of the proposed converter consists of a current-fed half bridge converter. This is connected to the full-bridge converter on secondary side of a high-frequency (HF) transformer. Power Factor Correction (PFC) can be attained by regulating the current at the input of the ac side. In addition to that, the proposed converter achieves Zero Current Switching (ZCS) of primary side switches and zero current turn-on for secondary side devices throughout the operation without any additional components. Furthermore, a novel modulation technique and control algorithm is implemented. This ensures soft-switching throughout the operation range of the converter during bidirectional power flow. Design equations are derived to help suitable selection of components for a given specification. The proposed converter is designed for 1.5KW capacity for EV charging application. The simulation and experimental results are presented.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

There is an increasing interest in deployment of electric vehicles (EVs) to reduce greenhouse emissions and fuel usage. The growing environmental awareness, innovation, and the government support are together paving the way for EVs. However, the wide adoption of these vehicles is limited. One of the reasons for this is the limited availability of electric vehicle battery chargers. Moreover, EV charging technologies that are fast, efficient, and low cost with a small form factor are needed. In addition to that, these technologies should have features to minimize harmonics and operate at high power factor. Their impact on the grid should be minimal as they would contribute to a significant share of the grid load in future. Another desirable feature is the ability to provide ancillary services to support smart grids [1]. A graph showing the grid load characteristics with different operational modes of EV charger is shown in Figure 1-1. The focus of this thesis is to analyze the present EV charger technologies and introduce a topology that has the potential to bridge the gap between the infrastructure and the demand for EVs.

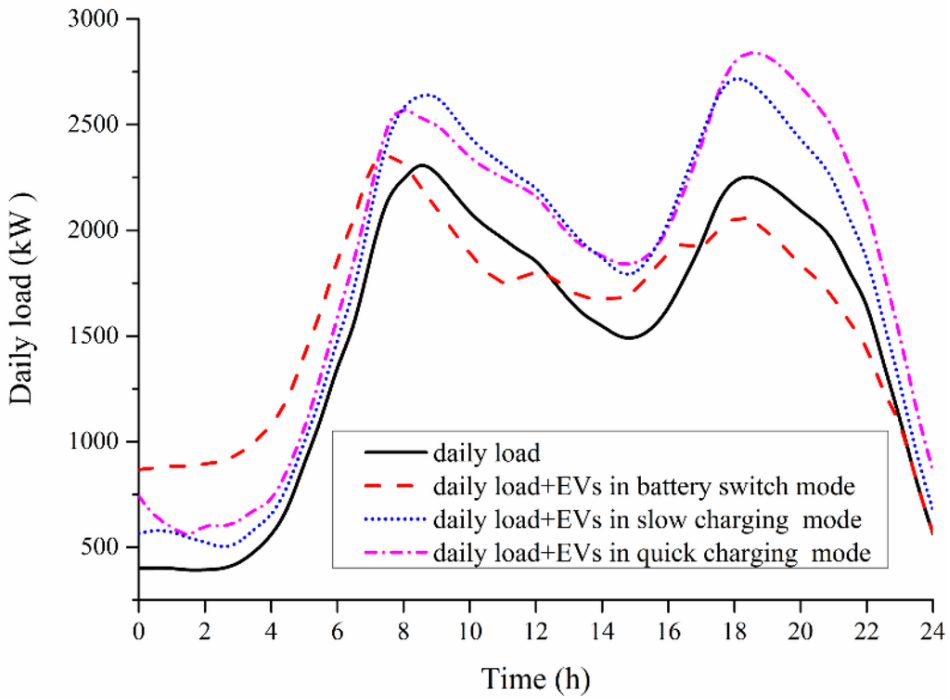


Figure 1.1 Load impact of EV charger operation on grid [2].

The following section discusses the different types of EV charger.

Types of EV Chargers

EV chargers are classified into two types based on their energy transfer methods. Both the methods have different power electronics interfaces and their own advantages and limitations related to efficiency, usage, and the infrastructure.

Conductive Chargers: These chargers have a hard-wired connection between the power source and the power converter that is used for charging the EV's. They usually consist of two stages, an active rectifier for power factor correction and a boost converter [3][4].

Inductive Chargers: These chargers do not need a physical hard-wired connection with the power source to transfer the energy to the EV's battery system. They utilize primary (transmitter) and secondary (receiver) coils for power transfer using the magnetic induction principle.

Generally, a resonant converter transfers the power through the large air gap which is then rectified to charge the battery [3][4].

Conductive chargers are more efficient compared to inductive chargers. However, the scope of applications is limited for conductive chargers. They only support “stationary charging”, which requires the vehicle to be at a standstill condition for charging. On the other hand, inductive charger may support “en-route” charging in addition to stationary charging, which allows the vehicle to charge while it is in motion [5]. The scope of this thesis covers only conductive chargers.

Conductive Charger Types

The conductive chargers are classified as “on-board” or “off -board” based on their location. The on-board chargers are mounted on the vehicle whereas the off-board chargers are mounted off the vehicle. The on-board chargers are constrained by the physical limits of weight and space. These constraints limit the power level for which they can be used. In contrast, off-board chargers have no physical constraints. They can be used for higher power levels. They also allow sharing the charging infrastructure, as shown in Figure 1.3, unlike on-board chargers which require every vehicle to have its own on-board equipment . This can reduce a considerable cost involved with EVs.

The chargers are further classified as “unidirectional” or “bidirectional”, based on their power flow characteristics. The unidirectional chargers support only single direction of power flow, from grid to the battery. On the other hand, bidirectional power chargers support the power transfer in either direction, from grid to the battery and from battery to the grid. The unidirectional chargers have a simple structure with less hardware components, fewer

interconnection issues, and low impact on the life of the battery. The bidirectional chargers may comparatively have a complex structure, but they support features for power stabilization with adequate power conversion. They can be utilized for microgrids and also for reducing the peak demands on the grid, which makes their application scope much larger than just charging the vehicle. Table-1 shows a comparison of different technological and economical aspects of these two types.

Table 1.1 EV Charger Classification [4].

	Power Flow and Switches	**Power Level**	**Control**	**Battery Effect**	**Benefits**
Unidirectional Chargers and Infrastructure	One way electrical energy flow, basic battery charge(G2V) Diode Bridge + Unidirectional converter	Levels 1,2 or 3	Simple, Active Control of Charging current. Basic control can be managed with time sensitive energy pricing	No Discharging Degradation	• Provides services based on reactive power and dynamic adjustment of charge rates, even without reversal • Supplies or absorbs reactive power, without having to discharge a battery, by means of current phase angle control
Bidirectional Chargers and Infrastructure	Two-way electrical energy flow and communication, charge/discharge (V2G) MOSFET (low power) GTO (High power level)	Expected only for Level 2	Complex Extra Drive control circuits	Degradation due to frequent cycling	• Ancillary services (Voltage Regulation, Frequency Regulation) • Spinning Reserves • Reactive Power Support • Peak Shaving • Valley Filling • Load Following • Energy balance

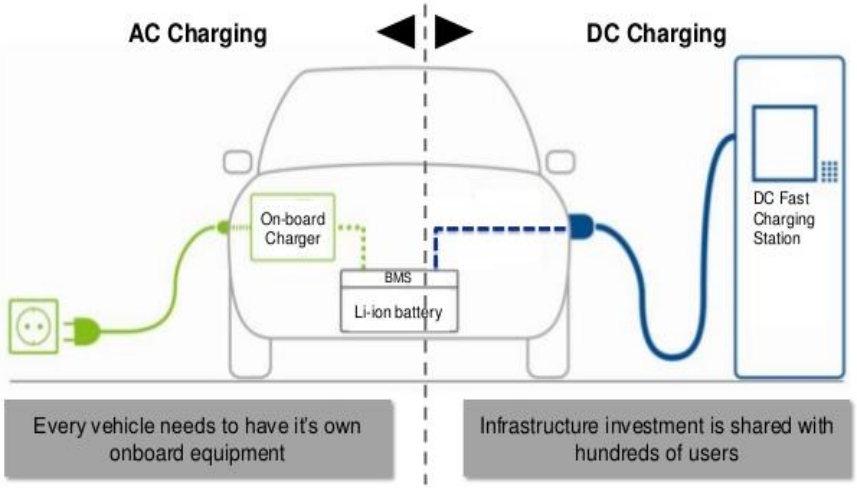


Figure 1.2 On-board vs Off-Board EV charger [6].

1.2 Standards of EV charger

This section deals with the Charge Method Electrical Ratings according to SAE EV Charging Power Levels. The chargers are classified by power they can provide to the battery pack. The classification is separately shown for AC and DC Charging systems [7][8].

1.2.1 AC Charging System

These type of charging systems mostly utilize on-board AC-DC charger for EV batteries. They are classified as level 1, level 2, and level 3.

(a) Level 1

The level 1 charger provides charging with a standard 120V (16A max) alternating current (AC) plug using a dedicated circuit. These chargers are mostly standard on vehicles and do not require a separate system to be installed for usage. The typical time these chargers take to charge a fully depleted battery ranges from 8- 12 hours. They support power levels of up to 2KW.

(b) Level 2

These chargers provide charging through a 240V power outlet and require a special installation with a dedicated 40 Amp circuit. They are compatible with most of the electric or plug-in hybrid vehicles. The power level for these chargers may range from 4-20 KW. It can take 4-6 hours to charge a fully depleted battery.

(c) Level 3

These chargers are used for power ratings greater than 14.4KW. They are commonly known as fast chargers . But not all Level 3 chargers can be classified as fast chargers, as this classification is based on the size of the battery pack and the time required to charge that battery pack [8]. One may consider a charger as a fast charger if it can charge a EV battery pack in a duration of 30 minutes or less.

The AC charging system power levels are summarized in Table 1-2.

Table 1.2 AC Charging System Power Levels [4].

Charge Method	Nominal Supply Voltage(V)	Maximum Current (A)	Power Level (KW)
AC Level 1	120 V AC, 1-phase	12	1.08
	120 V AC, 1-phase	16	1.44
AC Level 2	208 to 240 V AC, 1-phase	16	3.3
	208 to 240 V AC, 1-phase	32	6.6
	208 to 240 V AC, 1-phase	<=80	<=14.4

1.2.2 DC Charging System

Analogous to the AC charging systems, these systems are mounted at fixed locations. Compared to AC charging systems, these chargers can handle much higher power and quickly charge the battery. The requirement of DC voltages may vary with the model of the car, hence these chargers first identify the voltage required for a particular vehicle before starting to charge the battery.

(a) Level 1

These chargers are rated for power levels up to 36KW, with a dc voltage varying from 200-450V and current range up to 80A.

(b) Level 2

These chargers are rated for power levels up to 90KW, with a dc voltage varying from 200-450V and current range up to 200A.

(c) Level 3

These chargers are rated for power levels up to 240KW, with a dc voltage varying from 200-600V and current range up to 400A.

The DC charging system power levels are summarized in Table 1-3.

Table 1.3 SAE EV DC Charging Power Levels [8].

Charge Method	Supplied DC Voltage Range (V)	Maximum Current (A)	Power Level (KW)
DC Level 1	200-450V	≤ 80A	≤ 36 KW
DC Level 2	200-450V	≤ 200A	≤ 90 KW
DC Level 3	200-600V	≤ 400A	≤ 240 KW

1.3 Research Goal

The objective of this thesis is to develop a charger that is compact, efficient, and light weight. The problems with EV chargers are generally associated with multiple stages of power conversion; circulating currents in topologies with high-frequency transformers; losses in the switches; reverse recovery losses in the diodes; or the losses in the snubber circuits associated with the topologies. The reduction in the conduction losses is limited by the availability of the devices with low on-state voltage drop (or low RDS_{ON} in MOSFETS). To reduce other losses, one of the methods could be lowering the circulating currents or minimizing the duration where the current flows in a direction opposite to the required power flow. This can be achieved by employing techniques utilizing zero voltage switching (ZVS) and/or zero current switching (ZCS). The topologies using these techniques are commonly known as "soft-switching topologies". Another method to reduce the losses involves using fewer power conversion stages. In the literature reviews, it has been found that topologies using fewer stages tend to be more efficient and light weight. However, they may have lower power factor compared to topologies with multiple power conversion stages. These methods are reviewed and a new topology is introduced that achieves the bidirectional power flow characteristics with a single isolated soft switching stage.

1.4 Thesis Organization

Chapter 1 is an introduction to EV chargers focusing on different types and power levels. The research motivation and the thesis outline is also presented in this chapter. A detailed review of some of the soft switching topologies with their advantages and limitations is provided in

Chapter 2. Chapter 3 discusses the proposed bidirectional single-stage single-phase isolated AC-DC converter topology with PFC for EV charging. In Chapter 4, the control for the proposed topology is designed utilizing the derived small signal model and the frequency response methods. The hardware design procedure for the proposed converter is described in Chapter-5, with detailed descriptions for selecting hardware components; designing control board sensor circuits; and PCB design considerations. The simulation and the experimental results are discussed in Chapter 6. Finally, Chapter 7 provides a summary of the thesis; and the future work that can be done to optimize the performance of the proposed converter.

CHAPTER 2

REVIEW OF SOFT SWITCHING EV CHARGER TOPOLOGIES

2.1 Introduction

The performance and the size of converter primarily depend on the switching methodology adopted. Further, the performance can be evaluated in terms of its efficiency, total harmonic distortion and the ability to operate at the desired power factor. It also determines the converter compliance with different electrical codes and standards. Generally, the regulations are met by adopting complex control strategies and additional hardware circuits. Most of these strategies are not suitable solutions for the recent and developing power electronics applications. The operational switching state of the semiconductor devices is responsible for many of the regulation issues. The life of the converter is also dependent on the switching state. Most of the existing EV charger topologies adopt hard switching. Here, the voltage or current across the switch is non-zero when its switching state is changed. This causes switching losses and also limits the converter operational frequency. Hard switching with high frequency may lead to electromagnetic interference (EMI) and electromagnetic compatibility (EMC) issues. However, soft switching techniques may reduce most of the problems associated with hard switching converters. Soft switching refers to methods that shape the rising and falling edges of the switch current and voltage waveforms of conventional PWM waveforms, in a way that the switches and diodes can be turned off or turned on under zero voltage or zero current condition [9],[10]. It

reduces the switching losses and the associated harmonics. In addition, the EMI/EMC issues are decreased due to its low $\frac{dV}{dt}$ and/or $\frac{dI}{dt}$. It is also suitable for high frequency operation which results in the size and weight reduction of the converter while increasing its efficiency [11], [12].

2.2 Classification of EV charger topologies and their associated problems

The EV charger topologies can be classified into two types a) Isolated b) Non – Isolated as shown in Figure 2.1. In isolated topologies a galvanic isolation is provided with a high-frequency transformer between the source and the load. In non-isolated topologies there is no physical isolation between the source and the load. The isolated topologies are more prominent because of their compliance with various safety and EMI/EMC regulations. The isolated topologies offer a wide output voltage range while non-isolated topologies offer only a small range or a single value of output voltage. However, the usage of high-frequency transformers for isolation causes problem of circulating currents and hard switching in converters. In addition, various losses and high stress on the silicon devices are incurred. Hence, the converter may have low efficiency and longevity.

Auxiliary circuits are employed to overcome the limitations of the high frequency transformer. These auxiliary circuits increase the control complexity and losses. The other methods may utilize complex computational models which are difficult to implement in real hardware designs. These limitations can be met by adopting soft switching techniques.

Most of the soft switching topologies use interleaved PFC boost converters [13],[14]. However, the leakage inductance of the transformer used in these converters causes high oscillation in the circuit [12]. These oscillations can be reduced by using separate snubber circuits. In [15], an

active clamped capacitor is used to reduce the primary current of the high-frequency transformer before changing the state of the switching devices. In topologies similar to [15], the range for achieving ZVS is limited especially on the lagging side.

Section 2.3 discusses different soft switching EV charger topologies. The background on these topologies would help us understand the benefits achieved in the proposed soft switching converter.

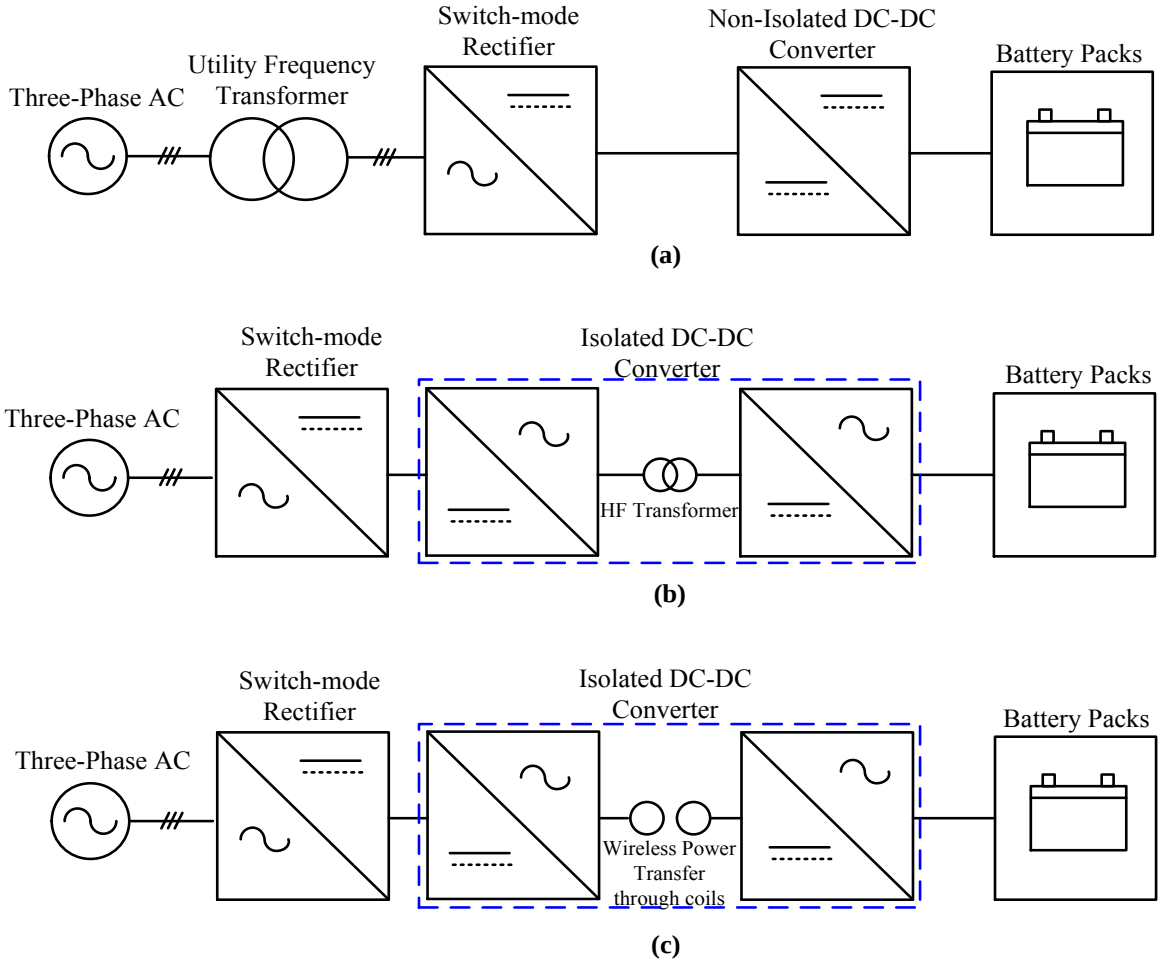


Figure 2.1 Power conversion flow diagram for: (a) non- isolated dc-dc converter, (b) conductive HF ac-link dc-dc converter, and (c) contact-less HF ac-link [16].

2.3 Soft Switching EV charger Topologies

This section describes the operation of few of the soft switching topologies used for EV charger.

2.3.1 Soft Switching Topology with active clamped capacitor [15]

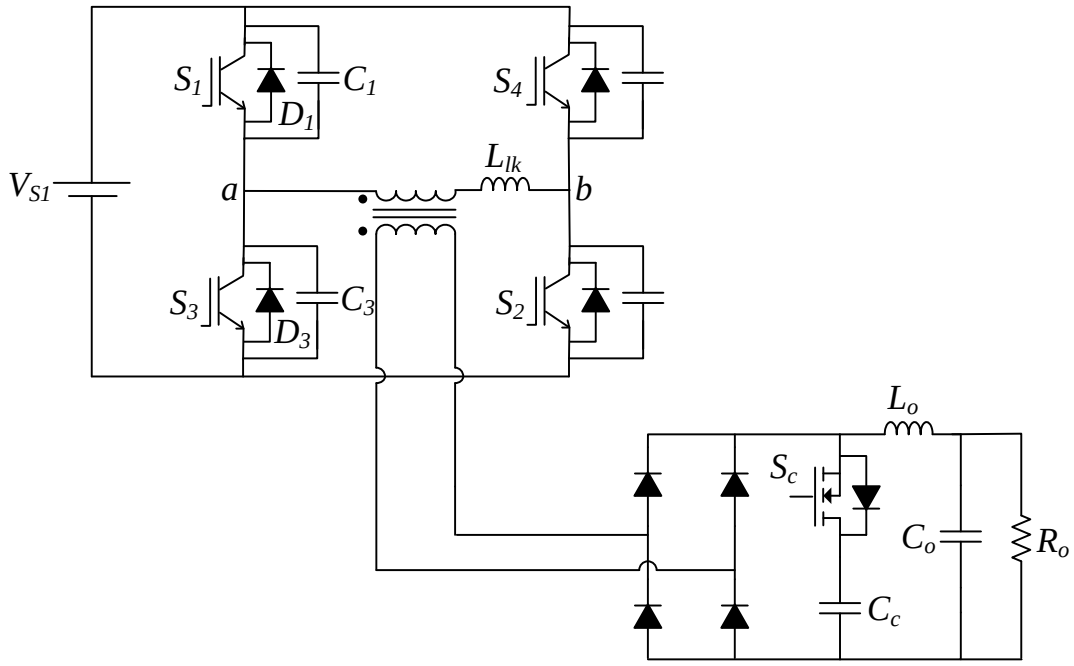


Figure 2.2 Zero Voltage Zero Current Switching Full-Bridge PWM Converter.

A soft-switching topology utilizing an active clamped capacitor is shown in Figure 2.2. The primary side of this topology consists of full H-bridge. The secondary side consists of a diode bridge rectifier, followed by a stage consisting of a series connection of a clamping capacitor and a switch (S_c); inductor (L_o) and; a output capacitor (C_o). A high frequency transformer is used to couple the primary and the secondary side. L_{lk} is the leakage inductance of the high frequency transformer. Two additional capacitors C_1 and C_3 are used across the primary diodes of switches S1 and S3 for clamping the input dc voltage during a particular operational state of the converter.

Initially, the switches S_1 and S_2 are turned ON, the clamping capacitor switch is ON at this instant. The primary current I_p starts flowing through the transformer. The clamping capacitor starts getting charged by the current represented by (2.1):

$$I_C = \frac{I_p}{n} - I_o \tag{2.1}$$

The current I_o is flowing across the load. The increasing voltage on the rectifier side is limited by the clamping capacitor. Hence, the primary current starts decreasing according to (2.2):

$$I_p(t) = \frac{1}{L_{lk}}\left(V_s - \frac{V_c}{n}\right).t \tag{2.2}$$

After the capacitor is fully charged, the current I_c becomes zero. The switch S_c is then turned off. The body diode of the switch S_c is blocking the current flow and the rectifier voltage at this instant is (2.3)

$$V_{rec} = nV_s \tag{2.3}$$

Switch S_1 is then turned off. The reflected load current then starts charging capacitor C_1 and discharging capacitor C_3. If capacitor C_1 is large enough to hold the voltage near zero, during the switching of S_1, the losses are very less. After a certain interval, D_3 starts conducting and the primary current starts freewheeling between diode D_3 and switch S_2. Since diode D_3 is conducting, switch S_3 is turned on with ZVS. Following this, switch S_c is turned on. The voltage V_c is reflected on the primary, which reduces the primary current by the slope $\frac{V_c}{nL_{lk}}$. Since (2.1) is still valid, the capacitor current starts to increase with decreasing I_p. After the primary current is reduced to zero, switch S_2 is turned off with zero current switching. The current through the rectifier diodes also reduces to zero and the complete load current is supplied by C_c. The switch

S_c is then turned off and the load current starts free wheeling through the recifier diodes. The primary current is zero. The switch S_4 is turned on and the same process is repeated. Hence, ZCS for leading leg switches and ZVS for lagging leg switches is achieved. The operation waveform for this converter is shown in Figure 2.3.

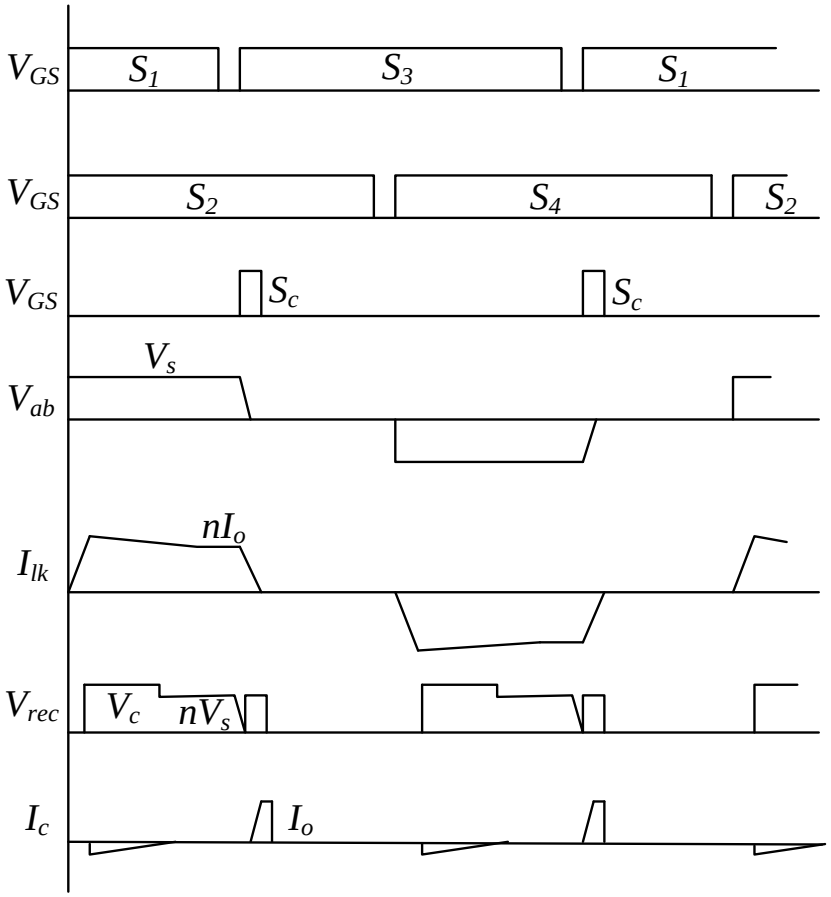


Figure 2.3 ZVZCS FB PWM Converter Output Waveform.

2.3.2 Naturally clamped zero-current commutated soft-switching current fed push-pull dc/dc converter [17]

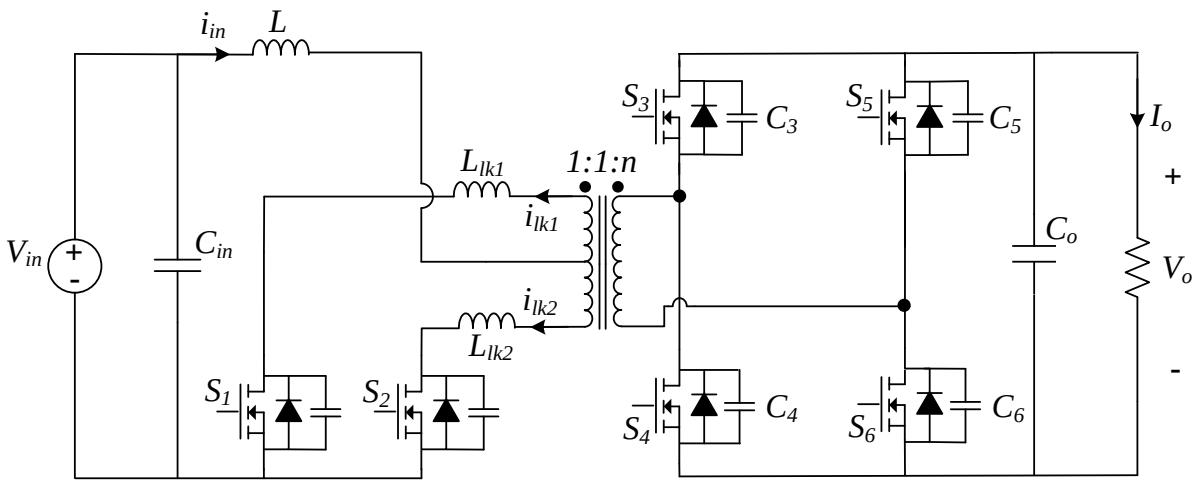


Figure 2.4 Zero current switching push-pull dc-dc converter.

A naturally clamped zero-current commutated soft-switching current fed push-pull dc/dc converter for EV charger is shown in Figure 2.4. This topology uses two switches which are connected to each end of the primary winding. This is coupled to a secondary winding feeding the full H-bridge connected to the load. The positive end of the dc source on the primary side is connected to the center tap of the high-frequency transformer.

The advantage of this topology is its snubberless design. The snubbers are used in the circuit for protection against the high voltage spikes that may occur during switching. Since this topology has ZCS of its primary devices and ZVS of secondary devices, the need of it is eliminated. To achieve ZCS, current is transferred from one primary switch to another, before turning it on or off. This is done by utilizing high-frequency modulation of the secondary switches. For ZCS, the

gating signals of the primary switches should be identical and have a phase shift of 180 degrees with overlap. This overlap requires the duty cycle to be greater than 50 %. The modulation of the secondary switches introduces a voltage of $\frac{V_o}{n}$ across the primary side. This voltage reduces the current from the turning off primary switch and transfers it to the other switch which is just turned on. The turning on and turning off the switch takes place at zero current condition, achieving ZCS. On the secondary side, the diodes across the switches are conducting before the switches are turned on. This is due to the natural flow of current because of the voltage on the secondary winding. Hence, zero voltage switching is achieved on the secondary side.

The proper functioning of this topology is critical to the design of its components, especially the leakage inductance. It is the energy transferring element of the circuit which directly impacts the efficiency and performance of the converter. The leakage inductance is calculated using the relation represented by (2.4):

$$L_{lkT} = L_{lk1} + L_{lk2} = \frac{2V_o(d - 0.5)}{nI_{in}f_s} \tag{2.4}$$

And the input and output voltage can be related using (2.5):

$$V_o = \frac{nV_{in}}{2(1 - d - d')} \tag{2.5}$$

Where

$$d' = d - 0.5 - \frac{nI_{in}L_{lkT}f_s}{2Vo}$$

The operation waveform for this converter is shown in Figure 2.5.

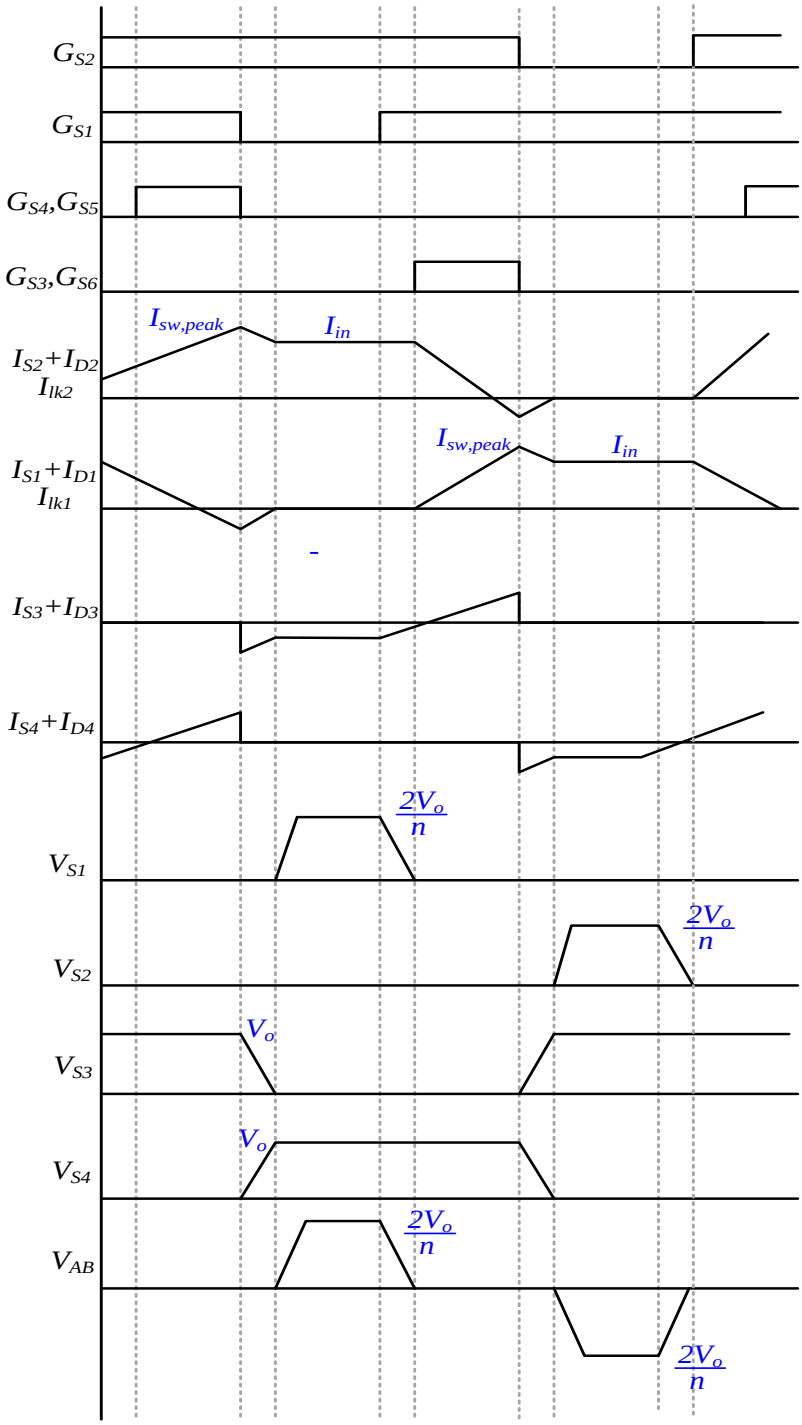


Figure 2.5 Zero current switching current fed push pull converter operation waveforms in the boost mode.

2.3.3 Snubberless bidirectional naturally clamped ZCS/ZVS Current fed half bridge dc-dc converter for fuel cell vehicles [18]

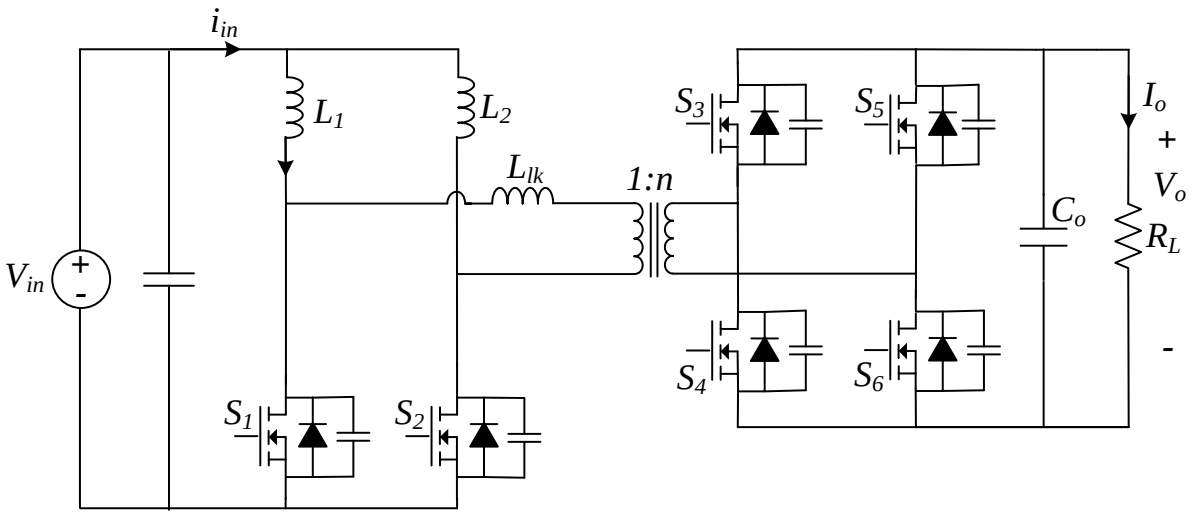


Figure 2.6 Current fed half-bridge dc-dc converter.

A snubberless bidirectional naturally clamped ZCS/ZVS current fed half-bridge dc-dc converter for fuel cell vehicles is shown in Figure 2.6, which is similar to Section 2.3.2. The distributed primary winding in Section 2.3.2 topology, is replaced by single primary winding of high frequency transformer. The secondary side utilizes full H-bridge for achieving bidirectional characteristics. The two large inductors connected on the primary side provide the boost function. L_{lk} is the leakage inductance of the high-frequency transformer.

During the power transfer from input to the battery, it acts as a isolated dual-phase boost converter. For the power transfer from the battery to the input, it acts as a voltage fed dc-dc converter. ZCS is achieved on primary side and ZVS is achieved on the secondary side. Before either of the primary switch S_1 or S_2 is turned off/turned on, the current through it is made zero. This is done by modulating the switches on the secondary side. When either pair S_3, S_6 or S_4, S_5

is turned on, a voltage of $\frac{V_o}{n}$ is reflected on the primary windings of the high-frequency transformer . The direction of this reflected voltage is dependent on the switch pair that is turned on. This voltage reduces the current flowing through one of the primary switches to zero, transferring the entire current to the other switch. On the secondary side, since the diodes are conducting for the switch pair that is turned on, ZVS is attained. The current flow on the secondary side is due to the voltage appearing on the secondary winding. This voltage is caused by the current flowing on the primary side. The primary switches are therefore required to have 180 degree phase shift and an overlap period. This requires duty cycle to be greater than 50%. The operation waveform for this converter is shown in Figure 2.7.

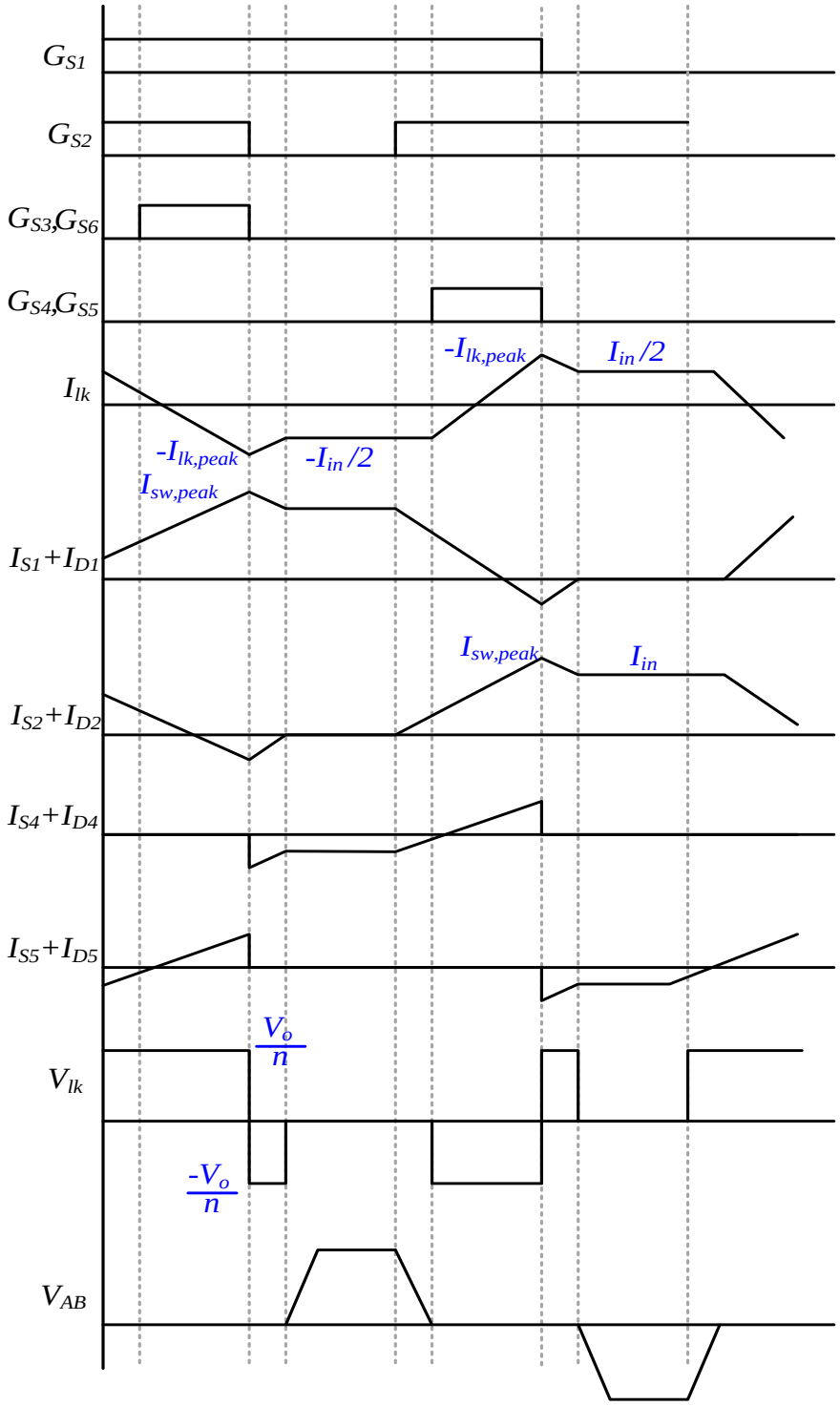


Figure 2.7 ZCS two-inductor current-fed half bridge isolated dc/dc converter.

2.3.4 Commercial Brusa EV charger [19]

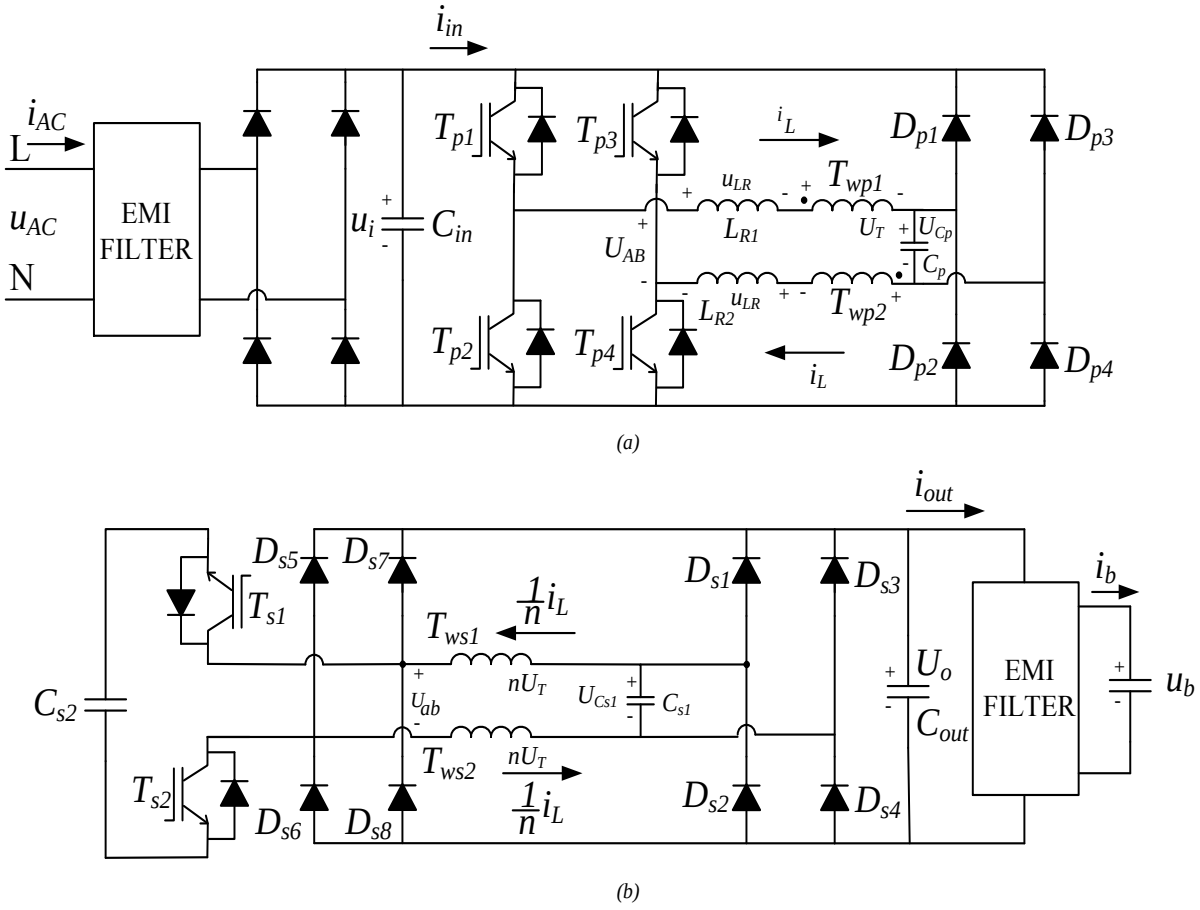


Figure 2.8 Brusa EV Battery Charger (a) Primary and (b) Secondary side structures.

An EV charger topology employed commercially by BRUSA is shown in Figure 2.8. The uniqueness of this topology is the simplicity of its control. The topology uses sinusoidal like dc current to charge the battery. It uses six switching devices, four of which are used on the primary side and two other are used on the secondary side. The primary four switches are denoted as T_{p1}, T_{p2}, T_{p3} & T_{p4} and the secondary switch are denoted as T_{s1} and T_{s2}. L_{r1} and L_{r2} represent the leakage inductance of the primary windings. The primary windings are denoted as T_{wp1} and

T_{wp2}. The secondary windings are represented as T_{ws1} and T_{ws2}. C_p and C_s are the voltage clamping capacitors on the primary and the secondary side.

The rectified and the battery voltage are compared to decide the operational state of the converter. If u_i is the rectified voltage of the input u_{AC}, and n is the turns ratio of the transformer. For duration, when $u_i > u_b$, battery is charged by the resonant circuit formed by the isolation transformer leakage inductance and the voltage clamped capacitors. When $nu_i < u_b$, then an additional capacitor C_{S2} is added to the secondary resonant circuit. This added capacitance increases the amplitude of voltage oscillation on the secondary side, which is used to charge the battery. The charging current can be controlled by regulating the input current which is represented as (2.6):

$$i_{AC} = 4fC_p u_{AC} \tag{2.6}$$

The input current is causing a voltage change of $2u_i$ across the capacitor C_p, during each turn-on period of the primary switches. From (2.6), the charging current can be controlled by adjusting the switching frequency. In addition, the input current is proportional to the input voltage for a fixed switching frequency. This maintains unity power factor throughout the operation. The switching waveforms during operation are shown in Figure 2.9.

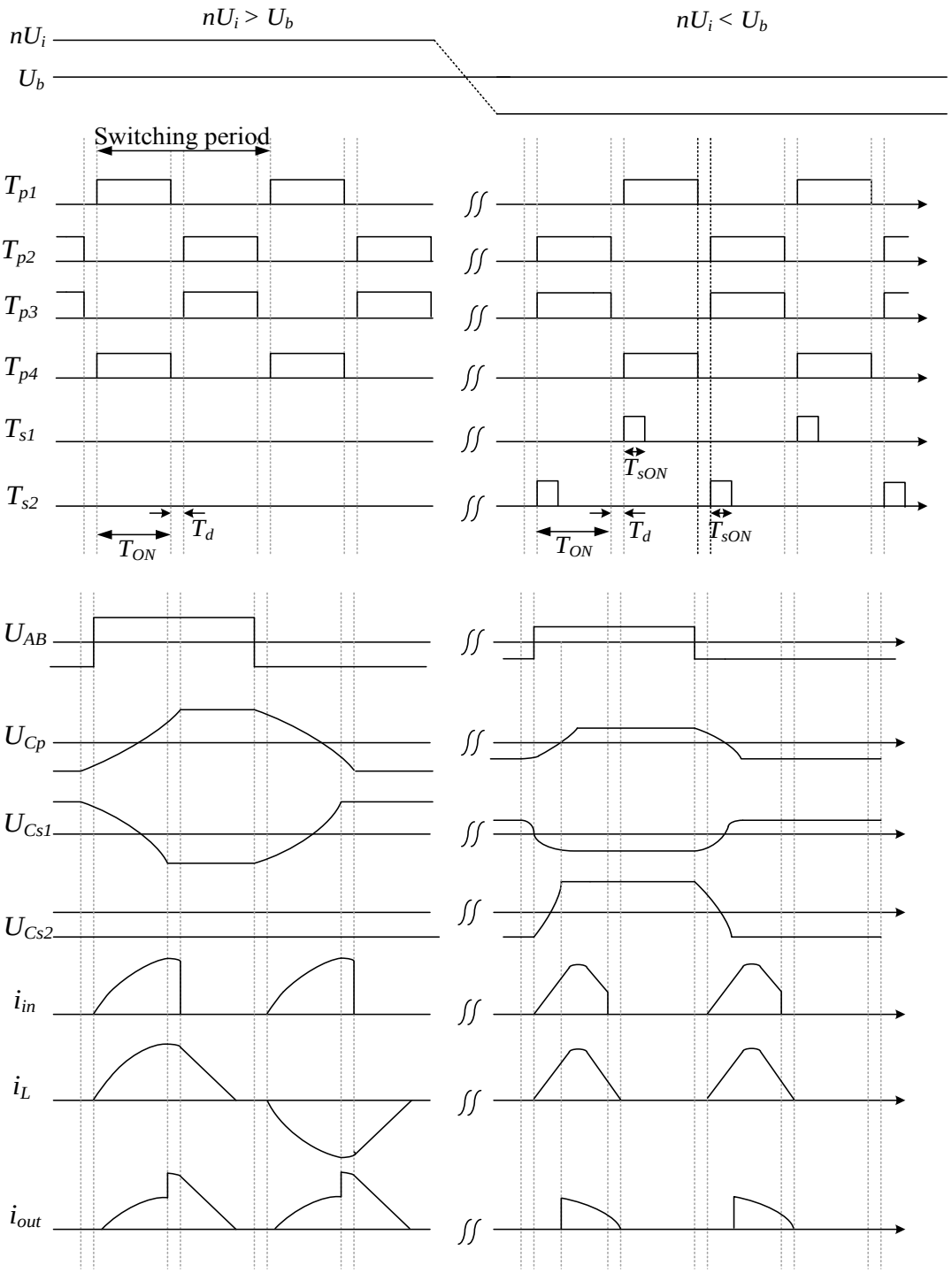


Figure 2.9 Switching waveform for Brusa EV charger.

The issues related to soft switching EV charger topologies can be summarized into following points:

- In most topologies, there is a need of additional ac-dc rectifier stage to support operation with AC inputs. Using multiple stages of power conversion reduces the efficiency in addition to, increasing the size of the system.
- An additional filter stage is needed to reduce Total Harmonic Distortion.
- Some of the topologies utilize more number of components/additional circuits to achieve soft switching characteristics, which directly affect the overall volume and cost of the converter.
- Only few of these topologies have bidirectional characteristics.

To deal with these issues a novel EV charger topology is proposed in the Chapter 3.

CHAPTER 3

BIRECTIONAL SINGLE-PHASE SINGLE-STAGE ISOLATED AC-DC CONVERTER WITH PFC FOR CHARGING OF ELECTRIC VEHICLES

This chapter introduces the bidirectional single-phase single-stage isolated ac-dc converter with PFC for charging of electric vehicles. This topology targets the key issues associated with other soft switching EV charger topologies discussed in Chapter-2. The control for the topology is described in the following chapter.

3.1 Introduction

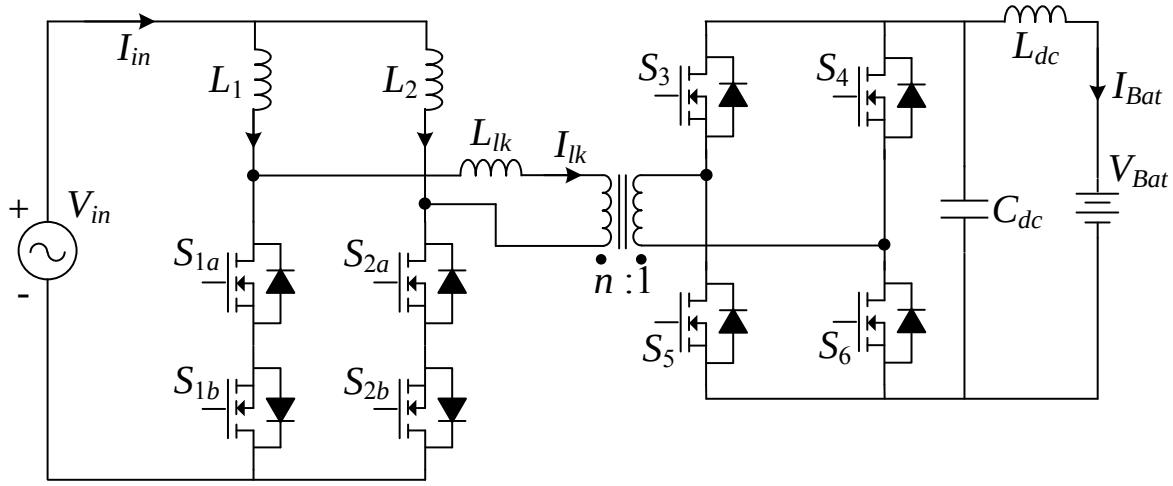


Figure 3.1 Soft switching single stage EV charger with PFC.

A soft switching single stage current EV charger with power factor correction is shown in Figure 3.1. It can operate in all four quadrants of voltage and current. It has current-fed bidirectional

half-bridge converter on primary side. Secondary side has full-bridge topology interfacing with the battery through a filter inductor L_{dc}. Power is exchanged between primary and secondary through a HF transformer. L_{lk} is the equivalent series inductance which represents leakage inductance of the transformer. If the leakage inductance is smaller than the requirement, then an external series inductance is connected. While charging the battery, the converter operates as a two-phase boost converter and during reverse power flow, the converter acts as a full-bridge converter with current doubler.

3.2 Operation of the EV charger

The operation of the converter can be divided into four modes depending on the polarity of input voltage and the direction of input current as shown in Figure 3.2(a). In mode-1 and mode-2, power is being transferred from grid to the battery. Mode-3 and mode-4 are used to function as V2G where power from the EV battery is being transferred to the grid. Since it is possible to regulate both active and reactive power in either direction, it can operate in all the 4-quadrants of P-Q plot as shown in Figure 3.2(b). Power factor of the input current can be controlled to regulate both active and reactive power flow.

Figure 3.3 shows variation in input voltage and input current in time-domain for a typical operation where power factor angle is controlled to be at α. Converter will be operating in all the four modes of operation depending on the polarity of the input voltage and current.

Operation and analysis of the converter in all the four modes is explained in the following sections.

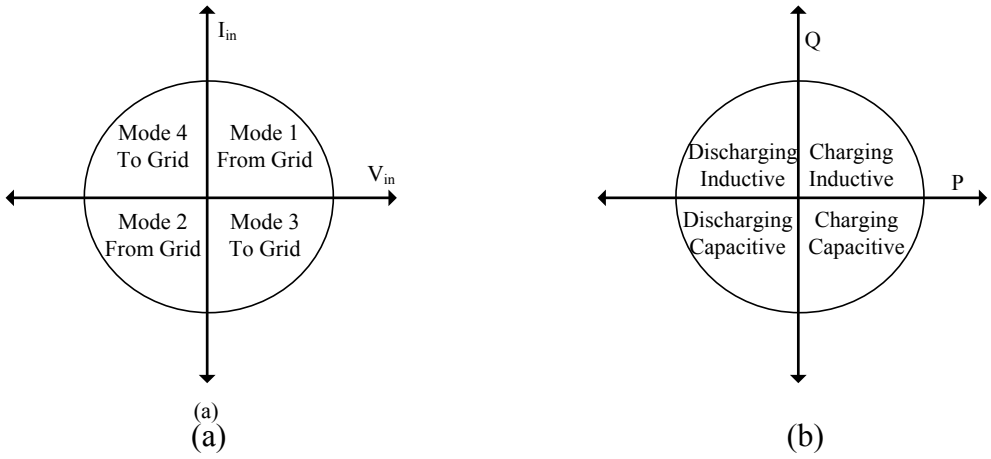


Figure 3.2 Different modes of operation.

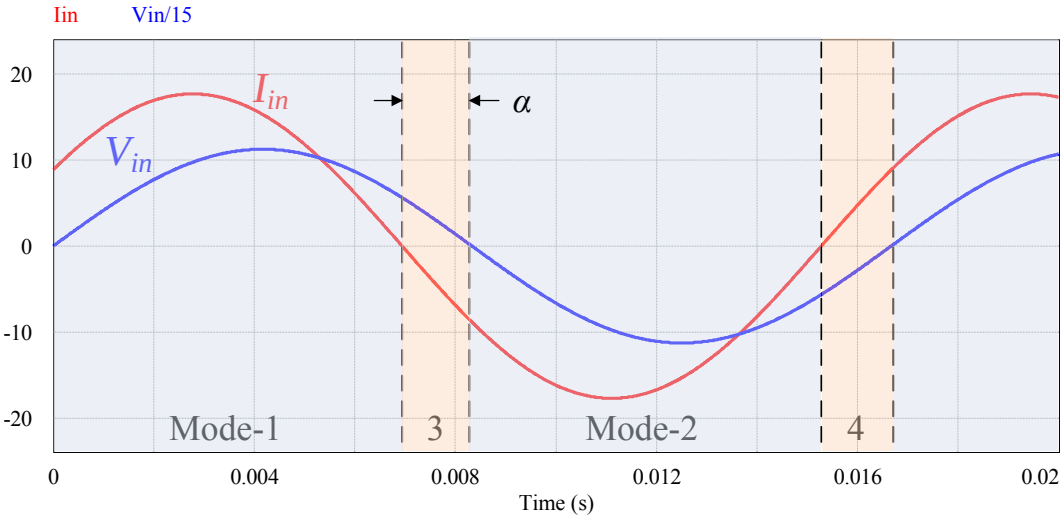


Figure 3.3 Modes of operation in a typical line frequency cycle.

3.3 Mode-1 Operation

Converter operates in this mode when the input voltage is in positive half cycle and power is flowing from the grid to the battery. In this mode, primary switches, S_{1a} and S_{2a} are operated at HF with duty ratio modulation and gate pulses of two phases are phase shifted by 180° as shown in Figure 3.4. In order to ensure overlap between conduction of S_{1a} and S_{2a}, duty ratio, d_1 is always maintained between 0.5 and 1. Since the input voltage is positive in this mode, other two

primary switches, S_{1b} and S_{2b} are kept on throughout. Devices on secondary side are switched at a fixed duty ratio, d_2 and their turn-off is synchronized with turn-off of the primary switches as illustrated.

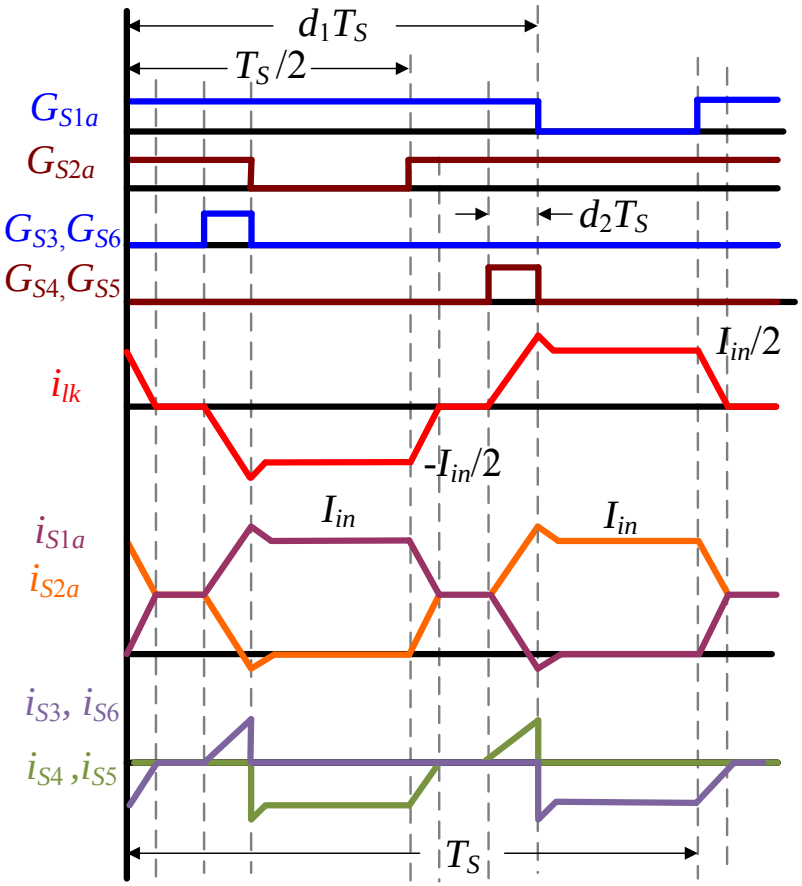


Figure 3.4 Operating waveforms of the proposed converter in mode-1.

As the switching frequency is much higher than the ac line frequency, input inductor current can be considered constant over a HF cycle. Input boost inductors are high enough to maintain equal current sharing between them.

When S_{1a} is on and S_{2a} is off, entire input current flows through S_{1a}. Inductor current, i_{L2} flows through the transformer transferring power to the secondary. When switch S_{2a} is gated on, the current is being transferred from the transformer to the switch linearly. Similarly, current through switch S_{1a} decreases and reaches $I_{in}/2$. On the secondary side of the transformer, current flowing through diodes of switches S_4 and S_5 becomes zero. In this modulation technique, secondary switches are used to reduce the current in primary switches to zero naturally to achieve ZCS. By gating switches S_4 and S_5 just before turning off of the primary switches results in voltage $-V_o/n$ across the primary of the transformer. This brings the current through the primary switch to zero naturally and it is independent of the load conditions. Duty ratio of the secondary switch, d_2 is calculated to make sure the current in the primary switch reaches zero before it is being turned off. This also limits the peak current flowing through the switch in other leg. Fixing duty ratio of secondary switch to a specific value prevents peak current through the primary switches to a value just above the input peak current under all operating conditions of input voltage and current.

Relation between input and output voltage is given by the relation (3.1),

$$V_o = \frac{nV_{in}}{1 - d_1} \tag{3.1}$$

Current through the transformer and switches are also shown during mode-1 illustrating ZCS of primary switches. Power transfer is limited by the product of series inductance and the switching frequency. In order to track the input current to the reference value, controller is designed to modulate the duty ratio of the primary switches between 0.5 and 1.

Table 3.1 Operation conditions for different modes.

	Mode-1	**Mode-2**	**Mode-3**	**Mode-4**
V_{in}	Positive	Negative	Positive	Negative
I_{in}	Positive	Negative	Negative	Positive
P_{in}	Grid to battery	Grid to battery	Battery to grid	Battery to grid
S_{1a}, S_{2a}	HF duty ratio modulation (ZCS)	ON	OFF (ZCS)	ON
S_{1b}, S_{2b}	ON	HF duty ratio modulation (ZCS)	ON	OFF (ZCS)
S_3-S_6	Fixed duty ratio, d_2 and synchronized with S_1-S_2 S_3, S_6 same S_4, S_5 same		50% duty ratio and phase shift modulation S_3, S_5 complementary (ZVS) S_4, S_6 complementary (ZVS)	

3.4 Mode-2 Operation

In this mode of operation, power is being drawn from the grid when voltage is in negative cycle. Since the input current is in opposite direction, S_{1a} and S_{2a} are kept at on state and S_{1b} and S_{2b} are operated at HF with duty ratio modulation. Similar to mode-1, duty ratio of primary switches is maintained above 0.5 and phase shifted by 180°. Secondary switches are gated with a fixed duty ratio of d_2 synchronizing turn off with the primary switch. In order to get voltage of opposite polarity across the primary of the transformer, gate signals of the secondary are interchanged as compared with the mode-1. Turn-off of switch S_{1b} is synchronized with turn-off of S_3 and S_6.

Turn-off of S_4 and S_5 is synchronized with that of switch S_{2b}. Gate signals and current waveforms in this mode are demonstrated in Figure 3.5. Currents in switches S_{1b} and S_{2b} decrease to zero before turning off resulting in ZCS. During turn-on, current rises linearly from zero reducing turn-on losses. Output voltage is derived as,

$$V_o = \frac{nV_{in}}{1 - d_1}$$

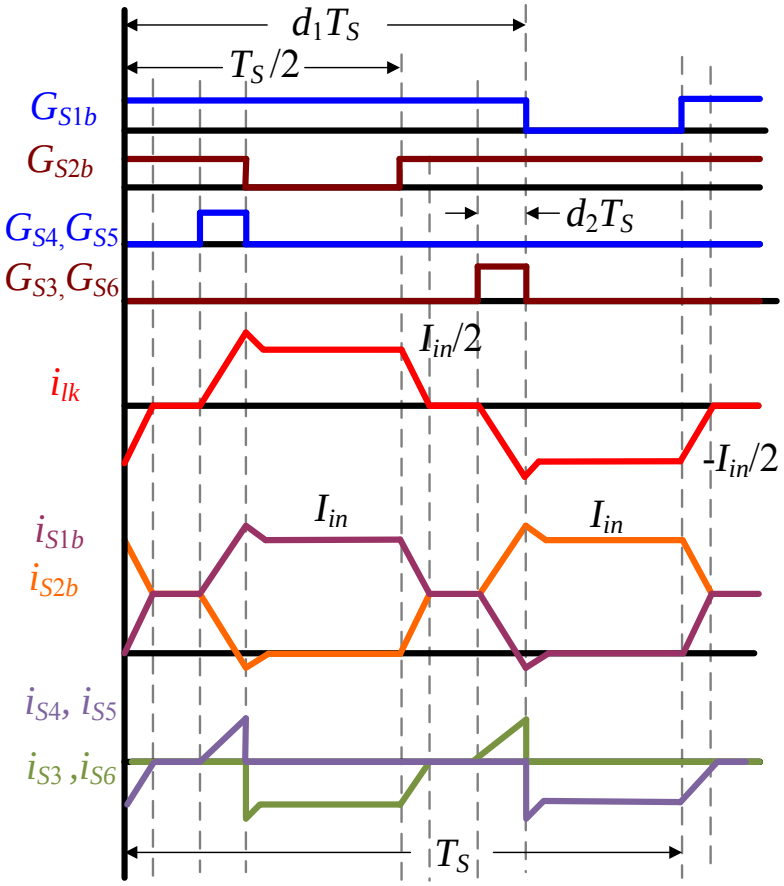


Figure 3.5 Operating waveforms of the proposed converter in mode-2.

3.5 Mode-3 Operation

In mode 3, power is being transferred to the grid from the battery storage. Primary switches, S_{1b} and S_{2b} are kept on and S_{1a} and S_{2a} are maintained in off state to maintain current in negative direction. During this mode of operation, gate signals of top and bottom switches on secondary sides are complementary to each other. Gate signal between two legs are phase shifted by φT_S as shown in Figure 3.6 changing the effective voltage across the transformer. The converter acts like voltage-fed full-bridge converter with current doubler on the output side. Phase angle φ can be varied between 0 and 0.5 to vary the effective output voltage which is represented as (3.2),

$$V_{in} = \frac{(\emptyset - \emptyset')V_o}{n} \tag{3.2}$$

Where, $\varphi' T_S$ represents the time taken for the current in L_{lk} to transit from positive to negative and vice versa, as shown in Figure 3.6. Dead time between top and bottom switches on the secondary side are chosen to make sure anti parallel diodes are conducting before turning on to ensure ZVS. In primary, current flows through S_{1b} and S_{2b} and through diodes of switches S_{1a} and S_{2a}. Since these currents are continuous, ZCS is achieved improving the converter efficiency.

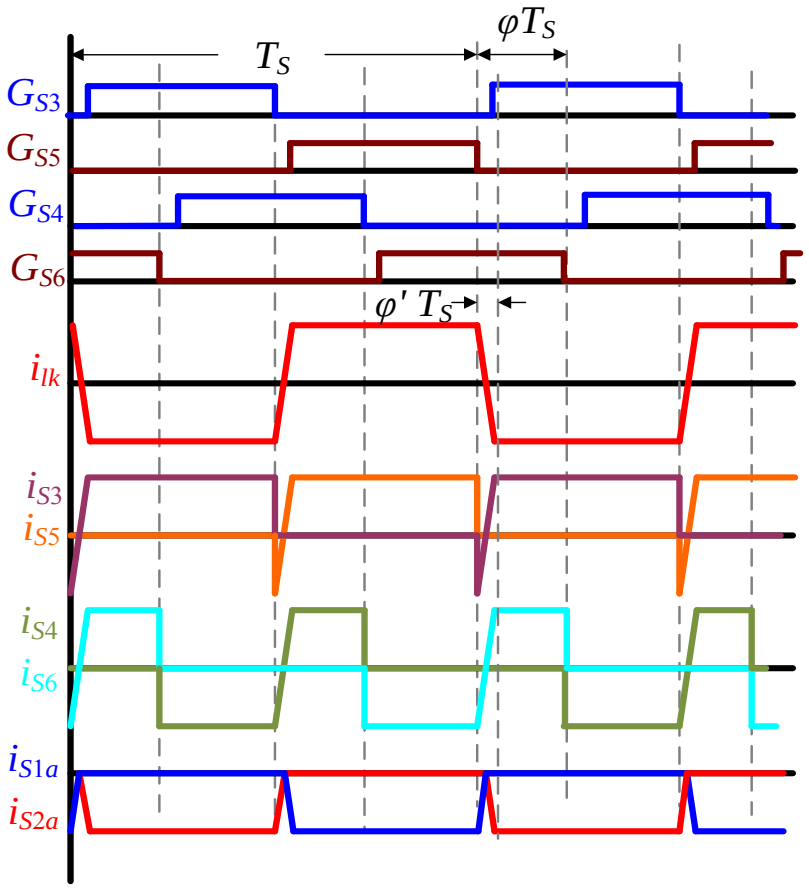


Figure 3.6 Operating waveforms of the proposed converter in mode-3.

3.6 Mode-4 Operation

Primary devices are being kept in a specific switching state based on the direction of input current. For positive direction of the input current in this mode, switches S_{1b}, S_{2b} are retained in on-state and currents flow through diodes of S_{1a}, and S_{2a}. On the secondary side, switches are operated similar to mode-3 by controlling the phase shift modulation.

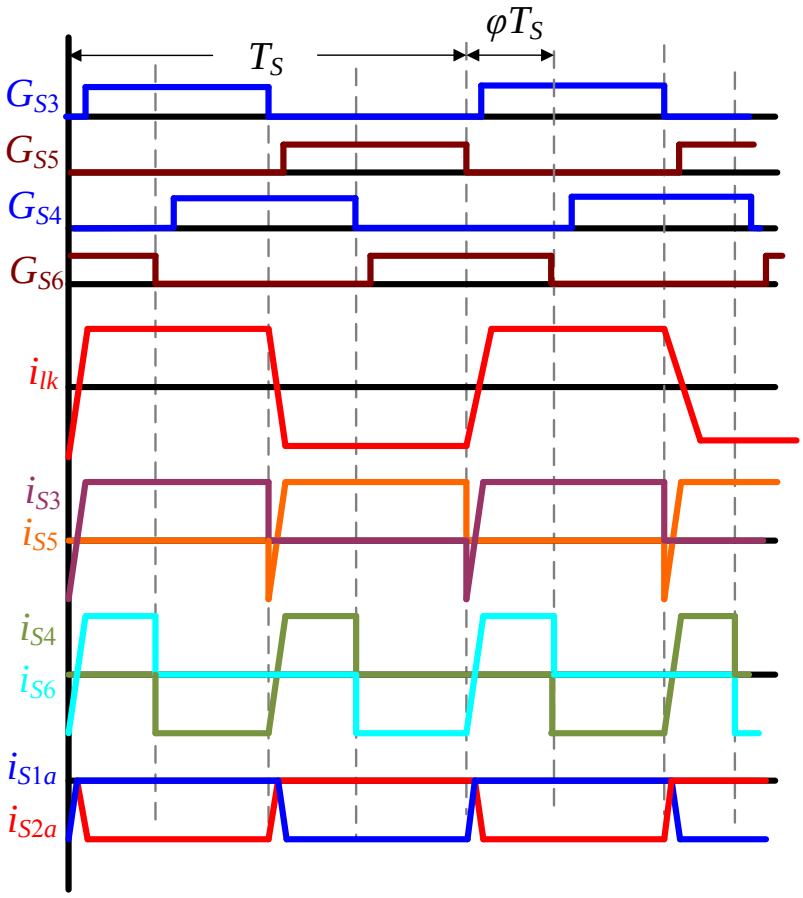


Figure 3.7 Operating waveforms of the proposed converter in mode-4.

The Table 3.2 shows a comparison of different EV charger topologies with the proposed converter. It highlights the advantages achieved with the proposed soft switching converter in terms of components count, control complexity and harmonic suppression.

Table 3.2 Comparison of different EV charger topologies.

	No. of Inductors	No. of Switches	No. of Diodes	Exis. Of Diode Bridge	Bidirectional Operation	Control Complexity	THD Suppression	Soft Switching
Positive Buck/Boost Rectifier [26]	1	6	9	Yes	No	Moderate	Low	No
Buck/Boost Diode Rectifier [29]	1	4	7	Yes	No	Low	Moderate	No
Three-Level AC/DC [27]	2	11	14	No	Yes	High	High	No
Bridgeless Direct AC/DC [28]	1	9	3	No	Yes	Moderate	Moderate	No
Proposed Converter	2	8	0	No	Yes	Low	High	Yes

This section introduced the bidirectional single-phase single-stage isolated ac-dc converter with PFC, along with the detailed discussion of its different operational modes. In Chapter 4, the control of this converter is designed utilizing its mathematical model. In later chapters, this control model is utilized to develop the hardware for the converter.

CHAPTER 4

CONTROL DESIGN FOR THE PROPOSED BIDIRECTIONAL SINGLE-PHASE SINGLE-STAGE AC-DC CONVERTER FOR EV CHARGING

In this chapter, the control for the proposed EV charger topology is designed. The first section shows the overall block diagram of the control, followed by the section describing the detailed mathematical model of the EV charger. It is later followed by separate sections, which discuss other control blocks in detail.

In forthcoming sections following notations are used:

V_{in} is the input voltage

I_{in} is the input current

L_1, L_2 are the input inductors

I_{L1}, I_{L2} are the currents in inductors L_1 and L_2 respectively

L_{lk} is the leakage inductance of the high frequency transformer

C_{dc} is the output capacitor

V_{batt} is the battery voltage connected at the output

I_{lk} is the current through the leakage inductance

I_{batt} is the current charging the battery

n is the transformer's turn ratio

V_c is the voltage across the output capacitor

D is the duty ratio of the primary switch

4.1 Complete Control Block Diagram for the proposed EV Charger Topology

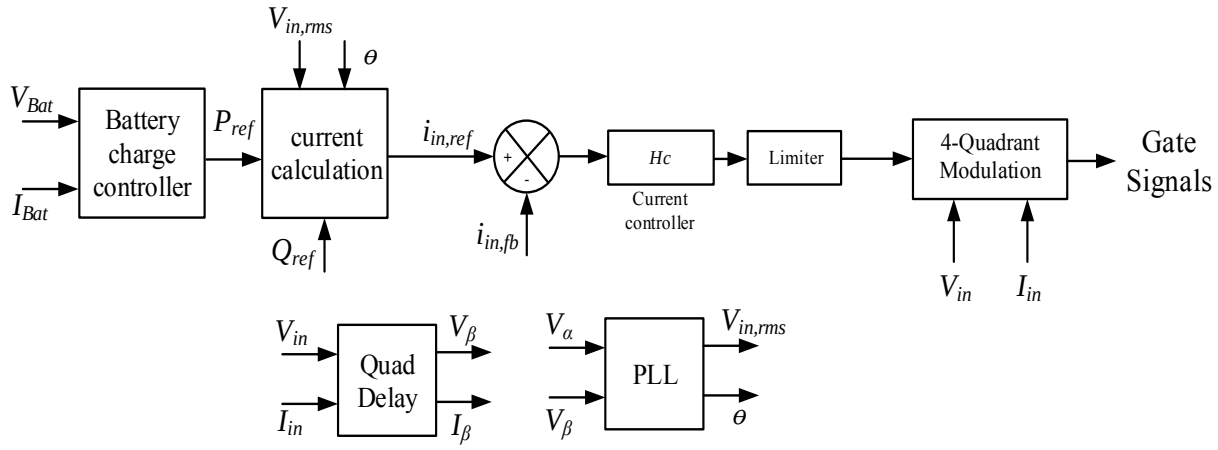


Figure 4.1 Complete control loop of the proposed converter.

The complete model of the proposed EV charger topology is shown in Figure 4.1. The reference values for active and reactive power are decided by the input received from the battery charge controller. A input current reference is derived from these values and compared with the actual input current. The difference between the actual and the reference value is fed to the hysteresis current control block. This block generates the output gate signals. The current is maintained in phase with the voltage using Phase Locked Loop (PLL). In addition, PLL can be used to operate the converter at desired power factor.

4.2 Mathematical modelling of the converter

The mathematical model of the converter is necessary to understand its dynamics and steady state response. A small signal model of the converter is derived using the state space averaging method. The mode-1 operational states shown in Figure 4.2, are utilized to arrive at the model.

The different operational states are divided into intervals represented by $d_1, d_2, d_3, d_4, d_5, d_6, d_7, d_8, d_9$ and d_{10}. The associated voltage and current equations are written for these intervals. The derived state space model is used to design the current control loop. The input and output voltage relation is also derived.

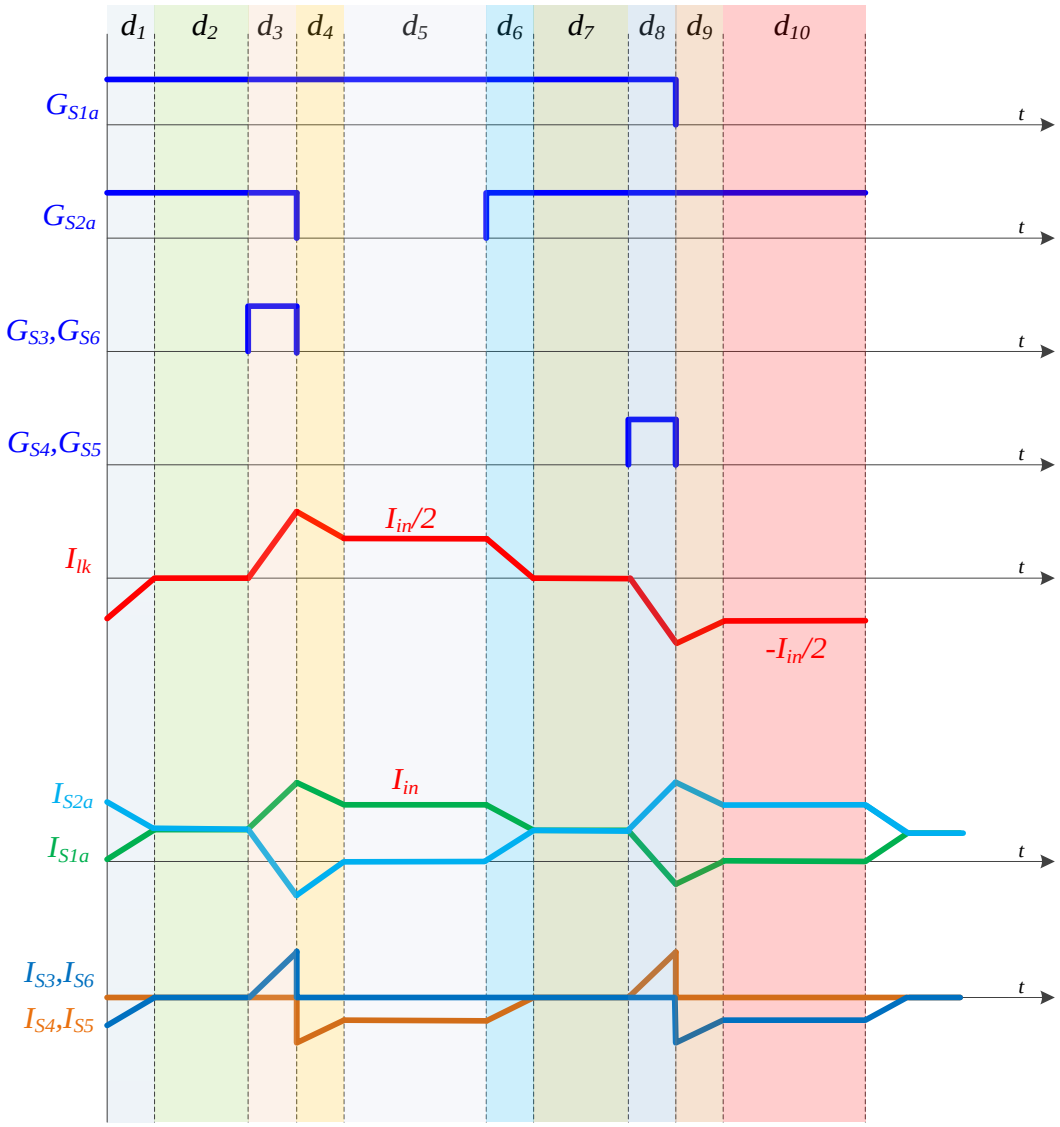
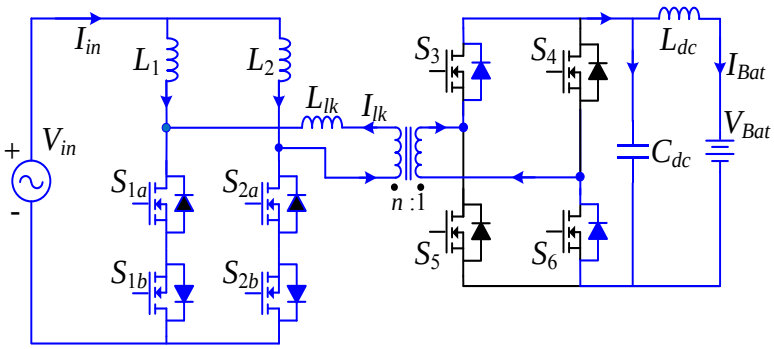


Figure 4.2 Graph for the operation of the converter in Mode-1.

Following assumptions are made:

$L_1 = L_2 = L, C_{dc} = C, V_{batt} = V_o, V_c = V_o$

The voltage and current relation during different intervals are represented as:



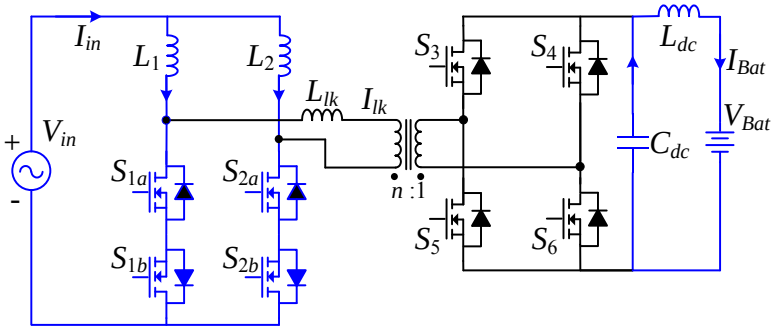
$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.1)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.2)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} - \frac{L_{lk} dI_{lk}}{dt} + nV_o = 0 (4.3)$$

$$nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.4)$$

Figure 4.3 Current Flow during interval d_1.



$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.5)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.6)$$

$$\frac{CdV_c}{dt} + I_{batt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.7)$$

Figure 4.4 Current Flow during interval d_2.

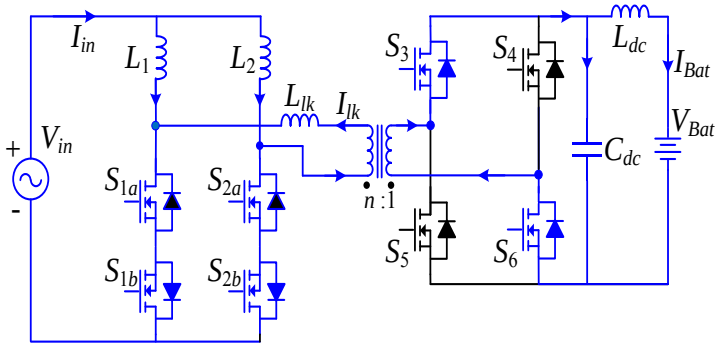


Figure 4.5 Current Flow during interval d_3.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.8)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.9)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} - \frac{L_{lk} dI_{lk}}{dt} + nV_o = 0 (4.10)$$

$$nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.11)$$

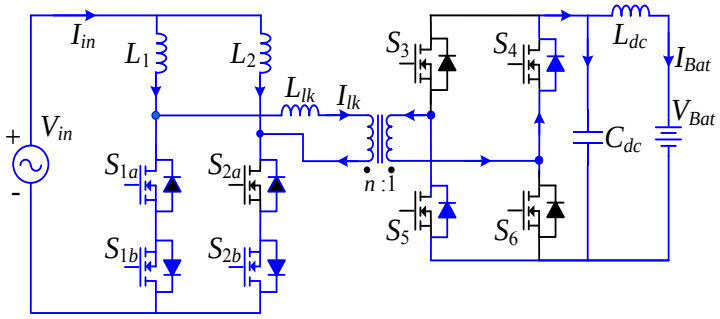


Figure 4.6 Current Flow during interval d_4.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.12)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.13)$$

$$-nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.14)$$

$$V_{in} - \frac{L_1 dI_{L1}}{dt} + nV_o + \frac{L_{lk} dI_{lk}}{dt} = 0 (4.15)$$

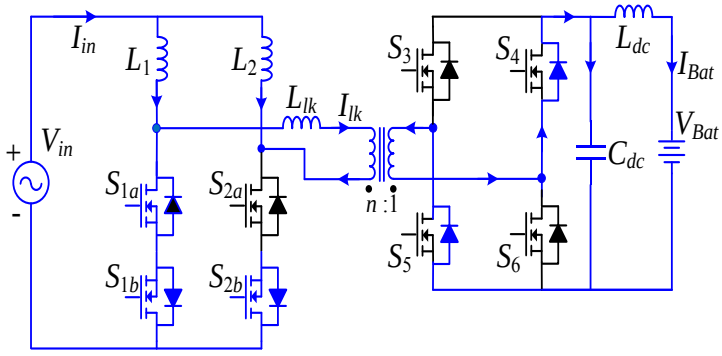


Figure 4.7 Current Flow during interval d_5.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.16)$$

$$-nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.17)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} - nV_o - \frac{L_{lk} dI_{lk}}{dt} = 0 (4.18)$$

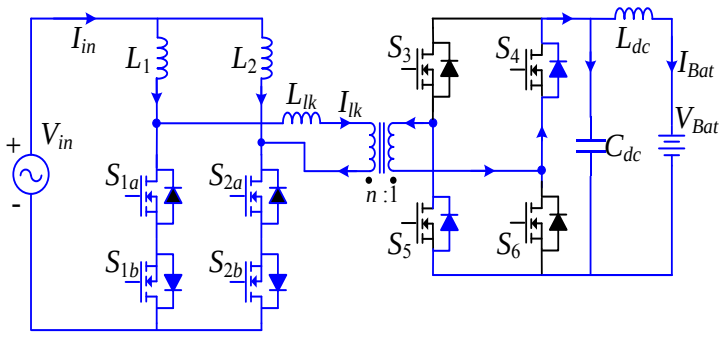


Figure 4.8 Current Flow during interval d_6.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.19)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.20)$$

$$V_{in} - \frac{L_2 dI_{L1}}{dt} + \frac{L_{lk} dI_{lk}}{dt} - nV_o = 0 (4.21)$$

$$-nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.22)$$

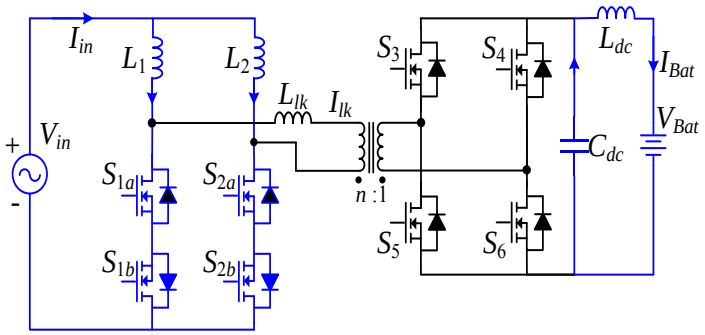


Figure 4.9 Current Flow during interval d_7.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.23)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.24)$$

$$\frac{CdV_c}{dt} + I_{batt} = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.25)$$

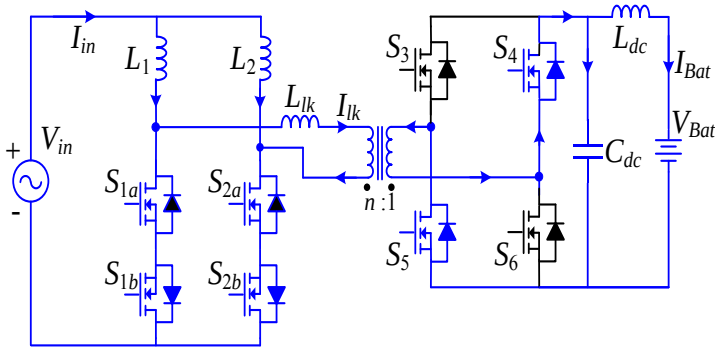


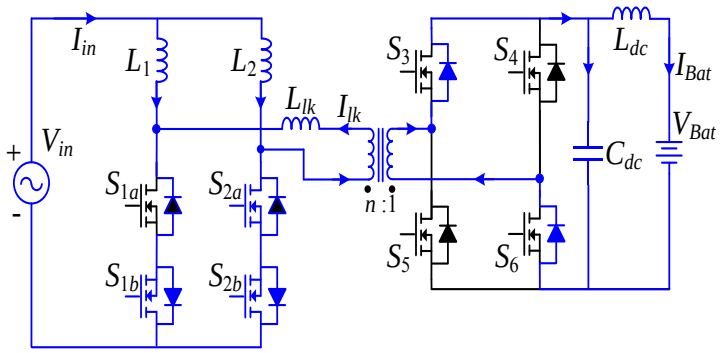
Figure 4.10 Current Flow during interval d_8.

$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.27)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.28)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} + \frac{L_{lk} dI_{lk}}{dt} - nV_o = 0 (4.29)$$

$$-nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.30)$$



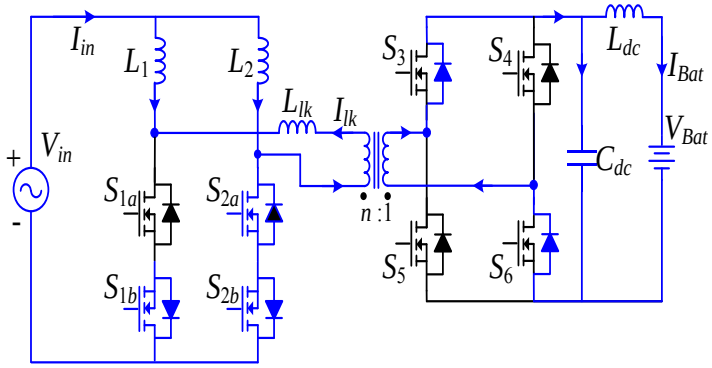
$$V_{in} - \frac{L_1 dI_{L1}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.31)$$

$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4.32)$$

$$V_{in} - \frac{L_1 dI_{L1}}{dt} - nV_o + \frac{L_{lk} dI_{lk}}{dt} = 0 \quad (4.33)$$

$$nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.34)$$

Figure 4.11 Current Flow during interval d_9.



$$V_{in} - \frac{L_2 dI_{L2}}{dt} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots (4.35)$$

$$V_{in} - \frac{L_1 dI_{L1}}{dt} - nV_o + \frac{L_{lk} dI_{lk}}{dt} = 0 \quad (4.36)$$

$$nI_{lk} = \frac{CdV_c}{dt} + I_{batt} \quad \ldots\ldots\ldots\ldots\ldots (4.37)$$

Figure 4.12 Current Flow during interval d_{10}.

From graph, we have

$$d_1 + d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10} = 1 \quad (4.38)$$

$$Let\ d_4 = d_9 = D'$$

$$d_4 + d_5 = d_9 + d_{10} = (1 - D) \quad (4.39)$$

Combining the equations from different states and averaging gives (4.42), (4.43) and (4.47):

$$\frac{dI_{L1}}{dt} = \frac{d_1 V_{in}}{L_1} + \frac{d_2 V_{in}}{L_1} + \frac{d_3 V_{in}}{L_1} + \frac{d_4 V_{in}}{L_1} + \frac{d_5 V_{in}}{L_1} + \frac{d_6 V_{in}}{L_1} + \frac{d_7 V_{in}}{L_1} + \frac{d_8 V_{in}}{L_1} + \frac{d_9 V_{in}}{L_1} + d_{10}\left(\frac{V_{in} - nV_o}{L_1}\right) \tag{4.40}$$

$$\frac{dI_{L1}}{dt} = \frac{V_{in}}{L_1} - \frac{d_{10} n V_o}{L_1} \tag{4.41}$$

$$\boldsymbol{\frac{dI_{L1}}{dt} = \frac{V_{in} - \left(1 - (D + D')\right) n V_0}{L_1}} \tag{4.42}$$

Similarly,

$$\boldsymbol{\frac{dI_{L2}}{dt} = \frac{V_{in} - \left(1 - (D + D')\right) n V_0}{L_2}} \tag{4.43}$$

$$\begin{aligned}\frac{dV_c}{dt} = \frac{1}{C}[&d_1(nI_{lk} - I_{batt}) + d_2(-I_{batt}) + d_3(nI_{lk} - I_{batt}) - d_4(nI_{lk} + I_{batt}) \\ &- d_5(nI_{lk} + I_{batt}) - d_6(nI_{lk} + I_{batt}) + d_7(-I_{batt}) - d_8(nI_{lk} + I_{batt}) \\ &+ d_9(nI_{lk} - I_{batt}) + d_{10}(nI_{lk} - I_{batt})]\end{aligned} \tag{4.44}$$

$$\begin{aligned}\frac{dV_c}{dt} = \frac{1}{C}[&nI_{lk}(d_1 + d_3 - d_4 - d_5 - d_6 - d_8 + d_9 + d_{10}) \\ &- I_{batt}(d_1 + d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 + d_{10})]\end{aligned} \tag{4.45}$$

From graph the average of I_{lk} can be represented as (4.46):

$$I_{lk} = 2 * \frac{I_{in}}{2} * n(1 - (D + D') = nI_{in}(1 - D) \tag{4.46}$$

$$\boldsymbol{\frac{dV_c}{dt} = \frac{1}{C}\left[n I_{in}(1 - D) - \frac{V_o}{R}\right]} \tag{4.47}$$

Perturbing (4.42), (4.43) and (4.47) with small signal gives (4.48), (4.49) and (4.50):

$$\frac{d(I_{L1}+\widehat{\imath_{l1}})}{dt}=\frac{(V_{in}+\widehat{v_{in}})}{L_1}-\frac{n(D+\hat{d})(V_o+\widehat{v_o})}{L_1} \tag{4.48}$$

$$\frac{d(I_{L2}+\widehat{\imath_{L2}})}{dt}=\frac{(V_{in}+\widehat{v_{in}})}{L_2}-\frac{n(D+\hat{d})(V_o+\widehat{v_o})}{L_2} \tag{4.49}$$

$$\frac{d(V_c+\widehat{v_c})}{dt}=\frac{n}{C}(I_{L1}+\widehat{\imath_{L1}}+I_{L2}+\widehat{\imath_{L2}})(1-(D+\hat{d})-\frac{(V_c+\widehat{v_c})}{RC} \tag{4.50}$$

Equating all the ac quantities gives (4.51), (4.52):

$$\frac{d\widehat{\imath_{L1}}}{dt}=\frac{\widehat{V_{in}}}{L_1}-\frac{n(D\widehat{V_o}+\hat{d}V_o)}{L_1} \tag{4.51}$$

$$\frac{d\widehat{\imath_{L2}}}{dt}=\frac{\widehat{V_{in}}}{L_2}-\frac{n(D\widehat{V_o}+\hat{d}V_o)}{L_2} \tag{4.52}$$

The state space model is represented as (4.53):

$$\begin{bmatrix}\dot{\widehat{\imath_{L1}}}\\ \dot{\widehat{\imath_{L2}}}\\ \dot{\widehat{v_c}}\end{bmatrix}=\begin{bmatrix}0 & 0 & -\frac{n(1-D)}{L_1}\\ 0 & 0 & -\frac{n(1-D)}{L_2}\\ \frac{n(1-D)}{C} & \frac{n(1-D)}{C} & -\frac{1}{RC}\end{bmatrix}\begin{bmatrix}\widehat{\imath_{L1}}\\ \widehat{\imath_{L2}}\\ \widehat{v_c}\end{bmatrix}+\begin{bmatrix}\frac{nV_c}{L_1}\\ \frac{nV_c}{L_1}\\ -\frac{n(I_{L1}+I_{L2})}{C}\end{bmatrix}\hat{d}+\begin{bmatrix}\frac{1}{L_1}\\ \frac{1}{L_2}\\ 0\end{bmatrix}\widehat{V_{in}} \tag{4.53}$$

From design $L_1 = L_2 = L$. Hence, the state space model can also be represented as (4.54), (4.55):

$$\begin{bmatrix}\dot{\widehat{\imath_{L1}}}\\ \dot{\widehat{\imath_{L2}}}\\ \dot{\widehat{v_c}}\end{bmatrix}=\begin{bmatrix}0 & 0 & -\frac{n(1-D)}{L}\\ 0 & 0 & -\frac{n(1-D)}{L}\\ \frac{n(1-D)}{C} & \frac{n(1-D)}{C} & -\frac{1}{RC}\end{bmatrix}\begin{bmatrix}\widehat{\imath_{L1}}\\ \widehat{\imath_{L2}}\\ \widehat{v_c}\end{bmatrix}+\begin{bmatrix}\frac{nV_c}{L}\\ \frac{nV_c}{L}\\ -\frac{nI_{in}}{C}\end{bmatrix}\hat{d}+\begin{bmatrix}\frac{1}{L}\\ \frac{1}{L}\\ 0\end{bmatrix}\widehat{V_{in}} \tag{4.54}$$

$$V_o=[0\ 0\ 1]\begin{bmatrix}\widehat{\imath_{L1}}\\ \widehat{\imath_{L2}}\\ \widehat{v_c}\end{bmatrix} \tag{4.55}$$

4.3 Current reference calculation from active and reactive power

The active and reactive power commands determine the current reference for the controller. The current waveform shifts according to the set value of active and reactive power. This shift is represented by (4.56):

$$Shift = atan2\left(-\frac{Q}{P}\right) \tag{4.56}$$

To operate at unity power factor, the reactive power is set to zero. According to (4.56), the shift for unity power factor would be zero. The generalised equation for the current reference using shift can be written as (4.57):

$$I_{ref} = \frac{\sqrt{2}\sqrt{P^2 + Q^2}\sin\left(\theta + atan2\left(-\frac{Q}{P}\right)\right)}{V_{mag}} \tag{4.57}$$

Where,

P is the active power

Q is the reactive power

θ is the phase angle of the input voltage

$atan2\left(-\frac{Q}{P}\right)$ is the shift or the phase angle introduced by the active and reactive power

V_{mag} is the magnitude of input voltage

4.4 Current control loop of the converter

The plant transfer function for the proposed converter is represented by the ratio of the inductor current and the duty ratio. The transfer function is determined using the state space model derived in (4.54), which is given as:

$$\begin{bmatrix} \dot{\widehat{i_{l1}}} \\ \dot{\widehat{i_{l2}}} \\ \dot{\widehat{v_c}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{n(1-D)}{L} \\ 0 & 0 & -\frac{n(1-D)}{L} \\ \frac{n(1-D)}{C} & \frac{n(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \widehat{i_{l1}} \\ \widehat{i_{l2}} \\ \widehat{v_c} \end{bmatrix} + \begin{bmatrix} \frac{nV_c}{L} \\ \frac{nV_c}{L} \\ -\frac{nI_{in}}{C} \end{bmatrix} \hat{d} + \begin{bmatrix} \frac{1}{L} \\ \frac{1}{L} \\ 0 \end{bmatrix} \widehat{V_{in}}$$

A new state variable is defined as $\widehat{i_{l1}} + \widehat{i_{l2}} = \widehat{i_l}$. This variable represents the input current which is the sum of the inductor currents i_{L1} and i_{L2}. Using this variable, the model in (4.54) reduces to (4.58):

$$\begin{bmatrix} \dot{\widehat{\boldsymbol{i_l}}} \\ \dot{\widehat{\boldsymbol{v_c}}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{0} & -\frac{\boldsymbol{2n(1-D)}}{\boldsymbol{L}} \\ \frac{\boldsymbol{n(1-D)}}{\boldsymbol{C}} & -\frac{\boldsymbol{1}}{\boldsymbol{RC}} \end{bmatrix} \begin{bmatrix} \widehat{\boldsymbol{i_l}} \\ \widehat{\boldsymbol{v_c}} \end{bmatrix} + \begin{bmatrix} \frac{\boldsymbol{2nV_c}}{\boldsymbol{L}} \\ -\frac{\boldsymbol{nI_{in}}}{\boldsymbol{C}} \end{bmatrix} \hat{\boldsymbol{d}} + \begin{bmatrix} \frac{\boldsymbol{2}}{\boldsymbol{L}} \\ \boldsymbol{0} \end{bmatrix} \widehat{\boldsymbol{V_{in}}} \tag{4.58}$$

Using (4.58), the transfer function is derived as (4.59):

$$\frac{\widehat{i_l}(s)}{\hat{d}(s)} = \frac{2n^2(1-D)V_c - nLI_{in}s}{LC\left(s^2 + \frac{s}{RC} + \frac{2n^2(1-D)^2}{LC}\right)} = T_p(s) \tag{4.59}$$

The frequency response analysis method is used to design the control loop for the proposed converter model. The nyquist plots are generated using MATLAB.

Figure 4.13 shows the nyquist plot for open loop plant transfer function derived in (4.59). It can be observed that the open loop transfer function is unstable since it crosses (-1,0) point. Also, the system has a negative gain margin. For stability, the plot should not cross (-1,0) point.

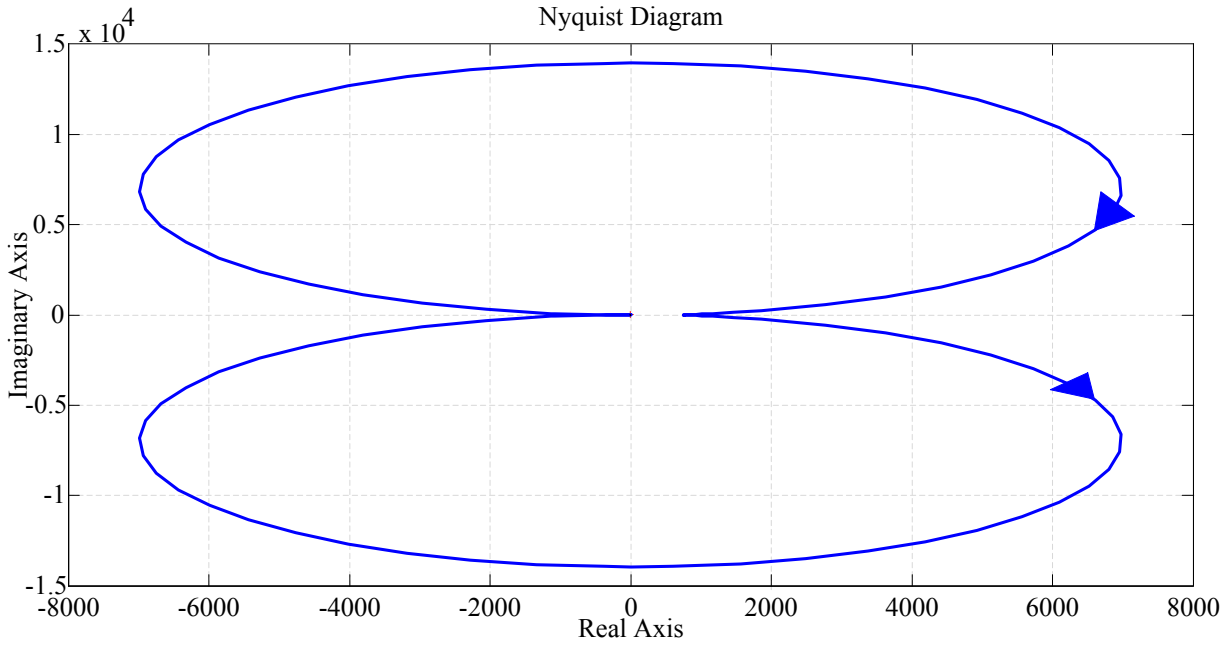


Figure 4.13 Nyquist plot of the open loop gain transfer function without the PI controller.

In order to achieve stability and desired operational characteristics, a control loop utilizing a PI controller and a unity feedback is designed. The current control loop is shown in Figure 4.14.

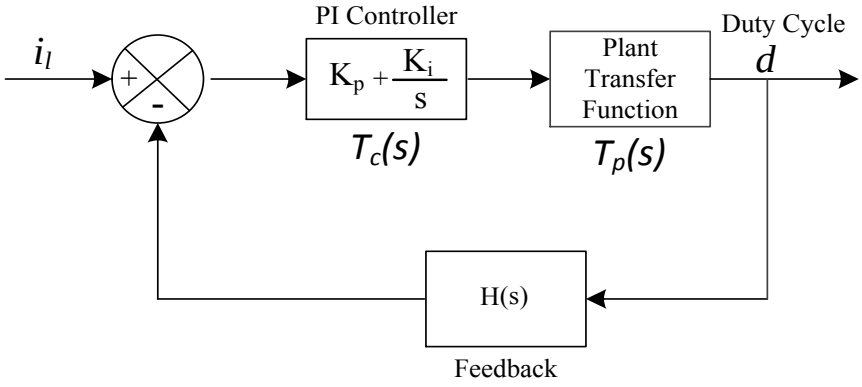


Figure 4.14 Current control loop for the proposed converter.

The nyquist plot with the PI controller and feedback is shown in Figure 4.15. The overall gain transfer function is given as (4.60):

$$\text{Gain Transfer function } = T_c(s) * T_p(s) * H(s) \tag{4.60}$$

It can be observed from Figure 4.15 that the plot is well within (-1,0) point, showing that the system is stable. The phase margin in this case is 90 degrees. Hence, the control design achieves the desired characteristics for the converter.

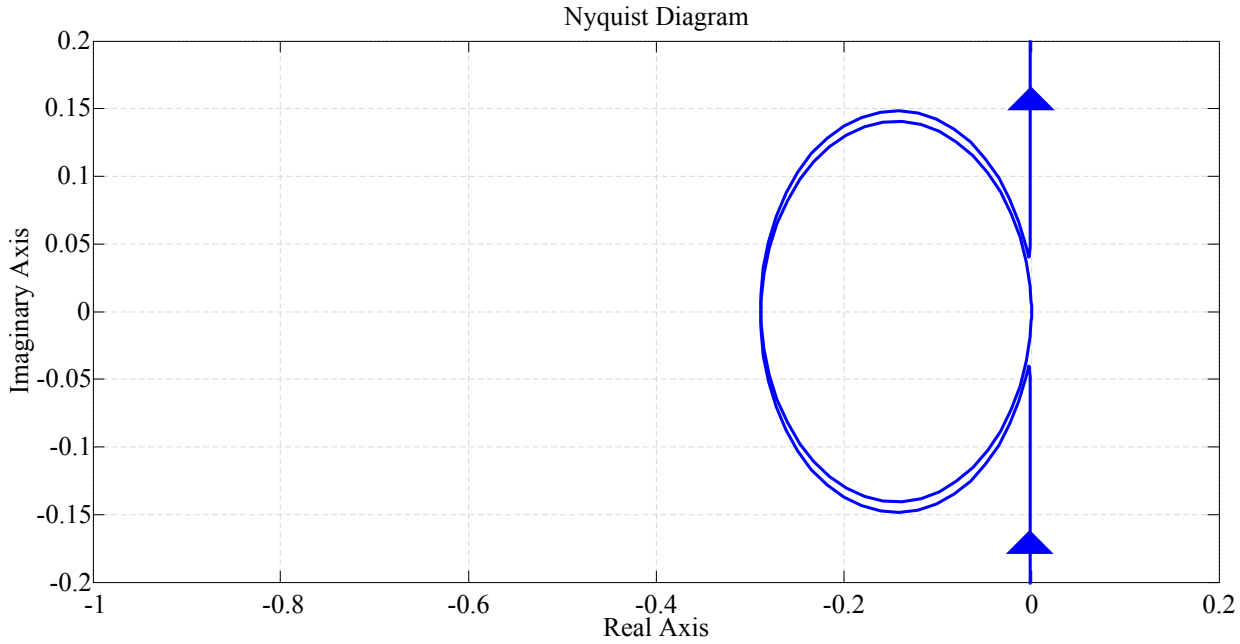


Figure 4.15 Nyquist plot of the open loop gain transfer function with the PI controller.

However, it should be noted that the PI values are derived for the operation at full power rating of the converter. When operating at different voltage or current, these values might need to be adjusted. Although, these PI values give us a good start point for the controller to be used for the hardware.

4.5 Phase locked loop for the converter

Phase Locked Loop (PLL) is used to operate the converter at desired power factor. The most common problem associated with conventional PLL as shown in Figure 4.16, is the noise

injected due to the second harmonic term [20]. In addition, for single phase systems the estimation of angle is difficult due to availability of single input. Further, the method of zero crossing detection in single phase system suffers from slow transient dynamics, since it will be updated only twice per cycle. Moreover, it is sensitive to noise near zero crossing.

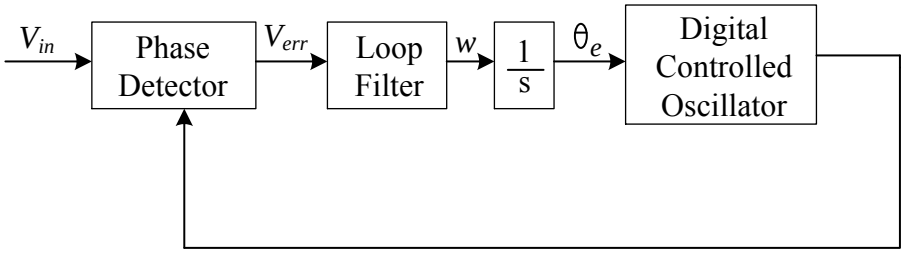


Figure 4.16 Basic Phase Locked Loop [20].

The PLL loop used for the control of the proposed converter uses a modified mixer phase detector, proposed in [20]. It utilizes additional feedback terms to reduce the second harmonic and higher order ripples. A mixer phase detector uses the product of two signals which are of sinusoidal nature to produce trignometric relationships between the summation and difference of the input and estimated frequencies in the resulting signal [20]. A clear illustration is shown in Figure 4.17.

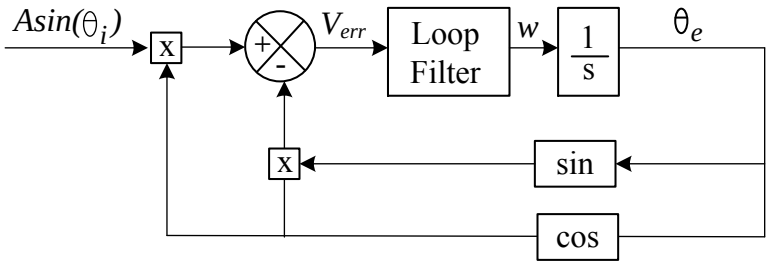


Figure 4.17 Modified Phase Locked Loop [20].

For the mathematical analysis of the modified PLL, following notations are used:

θ_i is the input angle

θ_e is the estimated angle

A is the per unit gain representing any amplitude mismatch in grid voltage magnitude from the nominal value

ω_i is the input signal frequency

ω_e is the estimated frequency

V_{err} is the error signal

From the Figure 4.17

$$\varphi = \theta_i - \theta_e \tag{4.61}$$

$$V_{err} = A sin\theta_i cos\theta_e - sin\theta_e cos\theta_e \tag{4.62}$$

Using (4.61) and (4.62), we get:

$$V_{err} = A sin(\theta_e + \varphi) cos\theta_e - sin\theta_e cos\theta_e \tag{4.63}$$

$$V_{err} = A[sin\theta_e cos\varphi + cos\theta_e sin\varphi] cos\theta_e - sin\theta_e cos\theta_e$$

$$V_{err} = (Acos\varphi - 1) sin\theta_e cos\theta_e + Acos^2\theta_e sin\varphi$$

$$V_{err} = \frac{(Acos\varphi - 1)}{2} \sin(2\theta_e) + \frac{Asin\varphi}{2} \cos(2\theta_e) + \frac{Asin\varphi}{2} \tag{4.64}$$

Using the trignometric relation (4.65) in (4.64), (4.66) is derived:

$$asin\alpha + bsin\alpha = \sqrt{a^2 + b^2} \sin(\alpha + K) \tag{4.65}$$

Where K=$\tan^{-1}\left(\frac{b}{a}\right)$

$$V_{err} = \left[\frac{A sin\varphi}{2} + \sin(2\theta_e + \delta)\right] * \sqrt{\left(\frac{A^2+1}{4} - \frac{A}{2}cos\varphi\right)} \tag{4.66}$$

Where,

$$\delta = \tan^{-1}\frac{A sin\varphi}{(A cos\varphi - 1)}$$

From the error signal, it is clear that the feedback is introducing a sine trigonometric term which can be used to reduce the second harmonic and the higher order ripples as expected. This design is therefore more rugged then the conventional PLL.

In this section, different blocks required for the control of the converter were derived and studied in detail. The information on these blocks becomes very relevant when debugging problems at the hardware level. In real hardware systems, the control systems work on the sampled values of the actual signals. It is very important to design the hardware that limits these values within the operational constraints of the control system. In Chapter 5, the hardware for the proposed converter is designed.

CHAPTER 5

HARDWARE DESIGN FOR THE PROPOSED BIDIRECTIONAL SINGLE-PHASE SINGLE-STAGE ISOLATED AC-DC CONVERTER FOR EV CHARGING

The hardware for the proposed EV charger topology is implemented. In this chapter, a detailed discussion for the choice of electrical components, filter designs, including the PCB layout is provided. The parts are designed keeping into consideration the control constraints discussed in Chapter 3.

The EV charger is designed to serve the specific requirements of project funded by Qatar National Research Fund. The complete specification list is shown Table 5-1:

Table 5.1 Specifications used for the EV charger.

Input Voltage (V_{in})	120V rms/60 Hz
Battery Voltage (V_{bat})	220V – 336V using 80 lithium ion batteries
Power	1.5KVA
Switching Frequency (f_s)	100kHz
Input Current peak value $(I_{in,max})$	17.7A

In this chapter, following notations are used:

n is the turns ratio

$V_{o,min}$ is the minimum value of the output voltage

$d_{1,min}$ is the minimum duty cycle of the primary side

$V_{in,max}$ is the peak value of the input voltage

N_1 is the number of turns on the primary side

N_2 is the number of turns on the secondary side

A_c is the cross sectional core area of the magnetic core

B_m is the saturation flux density of the magnetic core

A_w is the winding cross sectional area

f_s is the switching frequency

D_{min} is the minimum duty cycle

K_w is the window utilization factor (0.4)

J is the maximum allowed current density in the winding

$I_{1,rms}, I_{2,rms}$ is the rms currents on the primary and secondary side for the high frequency cycle

$I_{1,peak}, I_{2,peak}$ is the peak currents through the primary and secondary of the transformer

ΔI_L is the peak to peak ripple in the boost inductor current

$V_{in,max}$ is the peak value of the input voltage

d is the primary side duty cycle

d_2 is the secondary side duty cycle

P_o is the output power

ω is the line frequency in rad/s given by $2\pi * 60$

ΔV_o is the output ripple voltage

5.1 High Frequency Transformer Design

The turns ratio for the high frequency transformer is determined by the input and output specifications. Other limits are set by the operational characteristics of the converter. The transformers turns ratio, n is calculated as (5.1):

$$n = \frac{V_{o,min}\left(1 - d_{1,min}\right)}{V_{in,max}} \tag{5.1}$$

Using the values from Table 5-1 in (5.1), n is obtained as:

$$n = \frac{220 * (1 - 0.6)}{\sqrt{2} * 120} = 0.518 \approx 0.5$$

The core is selected after deciding the turn's ratio. The selection of the core and its area is dependent on the core saturation flux density and the switching frequency of the converter. In order to proceed, it is necessary to know the rms value of the currents flowing in the transformer windings. It is calculated by accumulating the rms values of the high frequency cycle over a line frequency by varying corresponding I_{in} and d.

$$I_{1,peak} = \frac{V_{o,max} d_2}{n L_{lk} f_s} \tag{5.2}$$

$$I_{2,peak} = \frac{V_{o,max} d_2}{n^2 L_{lk} f_s} \tag{5.3}$$

$$I_{1,rms} = I_{in} \sqrt{\left(\frac{1 - d}{2}\right) + \frac{d_2}{3}} \tag{5.4}$$

$$I_{2,rms} = \frac{I_{in}}{n} \sqrt{\left(\frac{1 - d}{2}\right) + \frac{d_2}{3}} \tag{5.5}$$

$I_{1,rms}\ and\ I_{2,rms}$ are the currents flowing through the primary and the secondary windings of the transformer. Following the winding currents calculation, the turns on the individual windings are determined. It is used to calculate the A_cA_w product of the transformer. The turns on the primary winding (N_1) and the secondary winding (N_2) are given by the relation (5.6) and (5.7):

$$N_1 = \frac{V_{o,max}(1 - d_{min})}{nA_cB_mf_s} \tag{5.6}$$

$$N_2 = \frac{V_{o,max}(1 - d_{min})}{A_cB_mf_s} \tag{5.7}$$

For the transformer, it is known that

$$K_wA_wJ = N_1I_{1,rms} + N_2I_{2,rms} \tag{5.8}$$

Using (5.6) and (5.7) in (5.8) gives:

$$K_wA_cA_wJB_mf_s = V_{o,max}\left[\frac{I_{1,rms}}{n} + I_{2,rms}\right](1 - d_{min}) \tag{5.9}$$

$$A_cA_w = \frac{2V_{o,max}(1 - d_{min})I_{1,rms}}{nK_wJB_mf_s} \tag{5.10}$$

$$A_cA_w = \frac{2 * 336 * (1 - 0.6) * 19.5}{0.5 * 0.4 * 7.5 * 10^6 * 0.1 * 100k}$$

$$A_cA_w = 3.5 * 10^{-7}m^4 = 349440\ mm^4$$

For the results obtained, **EE65/32/27 core** is chosen, where

$$A_cA_w = 2 * 535 * 10^{-6}$$

$$N_1 = 26\ and\ N_2 = 13$$

Primary side rms current = 19.5A (2 strands of AWG-16): J = 7.44

Secondary side rms current = 39A (4 strands of AWG-16): J = 7.44

5.2 Boost Inductor Design

The boost inductor design is dependent on the current ripple requirement. The current ripple percentage requirement was set as 1%. The inductor value for obtaining the given ripple requirement is calculated as (5.11):

$$L_1 = L_2 = \frac{V_{in,max}\, d_{1,min}}{\Delta I_L f_s} \tag{5.11}$$

$$L_1 = L_2 = \frac{169 * 0.6}{1 * 100k} = 1mH$$

Hence, the value of 1mH is used for the boost inductors on the primary side.

5.3 Leakage Inductance Design

The leakage inductance design is critical in order to have ZCS throughout the operation of converter. In order to ensure zero current crossing under all operating conditions, the used leakage inductance value is slightly higher than the calculated value. However, the difference should not be higher as it directly affects the overall efficiency of the converter.

The expression for determining the leakage inductance is obtained from the graph shown in Figure 5.1. It can be observed that when the current in the leakage inductor changes from 0 to I_{in}, the voltage across it is $\frac{V_o}{n}$. This happens during the on-time of the secondary switches. Hence the leakage inductance is calculated as (5.14):

$$L_{lk} = \frac{V_{o,min}\left(d_{1,min} - 0.5\right)}{nI_{in,max}f_s} \tag{5.14}$$

$$L_{lk} = \frac{220 * 0.1}{0.5 * 17.7 * 100k} = 25\mu H$$

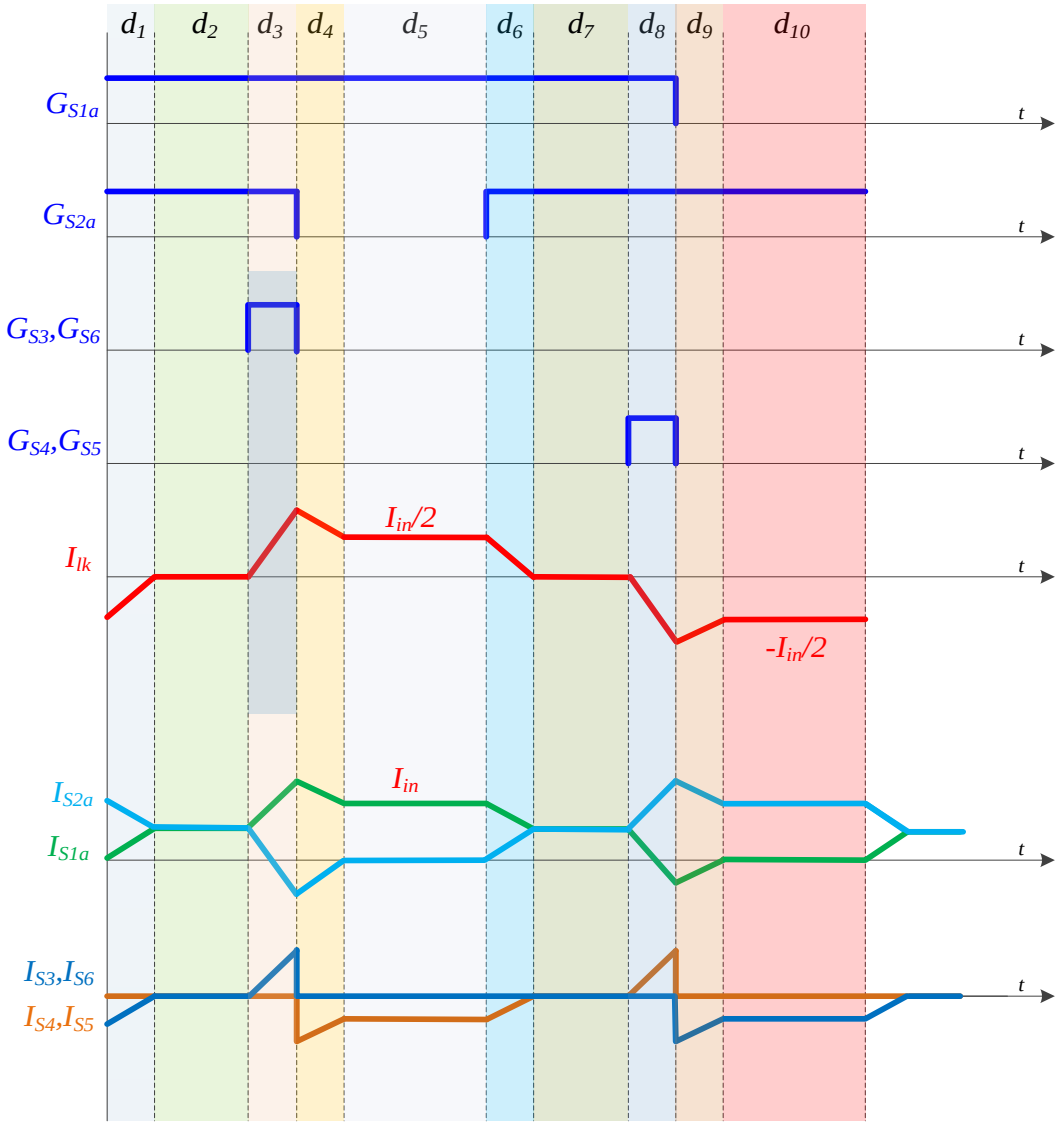


Figure 5.1 L_{lk} equation derivation.

The ZCS is also dependent on the duty cycle of the secondary switches, which is given by (5.15):

$$d_2 \geq \frac{I_{in,max} n I_{lk} f_s}{2V_{o,min}} \approx 0.05 \tag{5.15}$$

Where d_2 is the minimum limit on the duty cycle of the secondary switches.

The leakage inductance of the high frequency transformer is calculated. If the value obtained is less than the calculated value, then an additional inductance is added across the primary of the transformer to achieve the target value.

5.4 Output Capacitor Design

The output capacitor is needed to absorb the variation in power corresponding to twice the line frequency, as shown in Figure 5.2. Depending on the output voltage ripple requirements, the capacitance value is calculated.

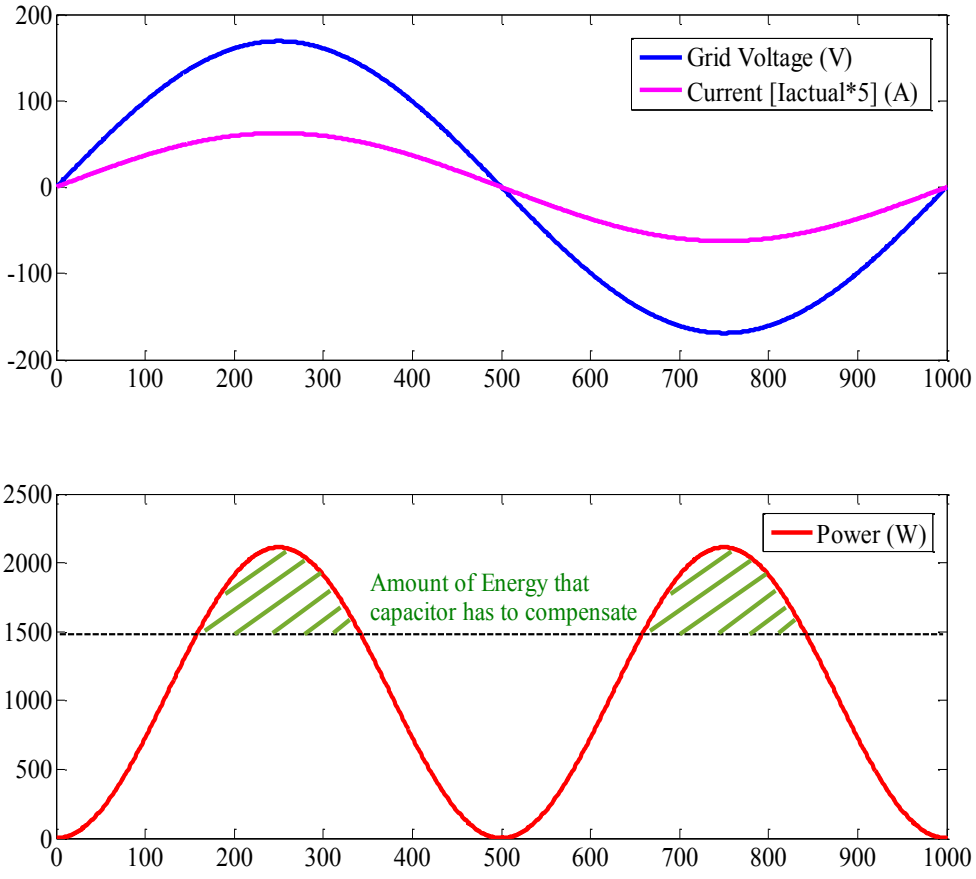


Figure 5.2 C_{dc} capacitor equation derivation.

The expression for capacitance is derived from the graph, which is given as:

$$C_{dc} = \frac{2P_o}{\Delta V_o \omega V_{o,min}} \tag{5.16}$$

In the present setup, (2x1200μF), 450V electrolytic capacitors are used.

5.5 Selection of Switching Devices

The selection for the switching devices is based on the continuous current and voltage rating, the peak values of voltage, current and power that the devices can handle. In order to minimize the conduction losses associated with the devices switches with low $R_{ds,on}$ are selected.

The peak current through the primary devices is given by (5.17):

$$I_{S(primary),peak} = \frac{I_{in,max}}{2} + \frac{V_{o,max} d_2}{n L_{lk} f_s} = 25A \tag{5.17}$$

The maximum voltage across the primary switches is given by (5.18):

$$\frac{V_{o,max}}{n} = 672V \tag{5.18}$$

Selected Primary Switch: C2M0040120D, SiC MOSFET from CREE, 1200V, 60A, 40mΩ

The peak current through the secondary switches is given by (5.19):

$$I_{S(secondary),peak} = \frac{1}{n} * \frac{V_{o,max} d_2}{n L_{lk} f_s} = 32.25A \tag{5.19}$$

The voltage rating should be higher than the output voltage given in the specification, 336V

Selected Secondary Switch: C2M0025120D, SiC MOSFET from CREE, 1200V, 90A, 25mΩ

5.6 Control Board Design

This section describes in detail about the different components and circuits used for the control board design. The design of the filter, offset and gain circuits is dependent on the quality and output type of different sensors. A flow diagram showing different stages for signal manipulation is presented in Figure 5.3. The signal conditioning stage shown in the flow diagram is Sallen Key filter circuit.

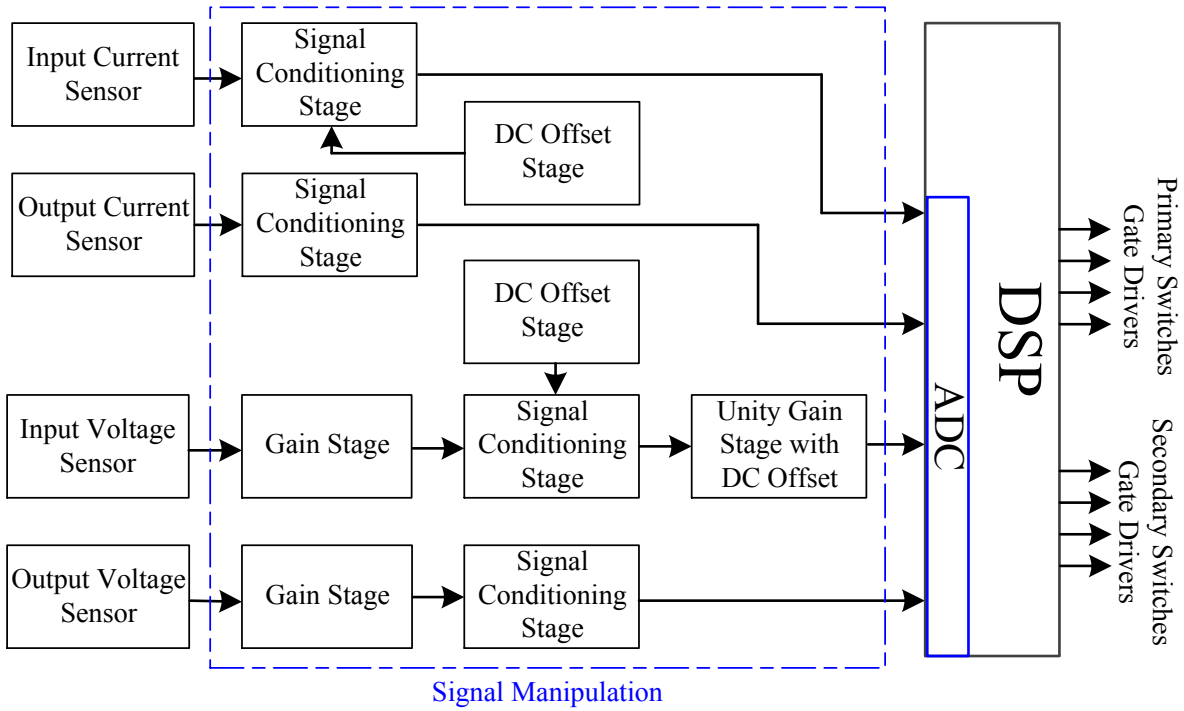


Figure 5.3 Different Stages in Control Board.

5.6.1 Current and Voltage Sensors

Current Sensor (Allegro ACS714)

Allegro ACS714 is chosen because of its small footprint, high voltage isolation, high precision and single supply operation. It has a large bandwidth of 80 kHz which can be altered via the

filter pin. The output voltage of this sensor is directly proportional to the AC or DC currents measured.

Voltage Sensor (ACPL-C79)

ACPL-C79 voltage sensor is used because of its linearity and dynamic performance. It's a fully differential operational amplifier that uses a single 5V supply and has a large bandwidth of 200 kHz with a fast response time of $1.6\mu s$. In addition, it has the capability to capture the transients in short circuit and overload conditions. This helps for debugging fault conditions of the converter.

Voltage Sensor (Input and Output) Gain stage

In order to bring the voltage output from the sensor to a specific range, a gain stage is used. This specific range is dependent on the sensor output and the choice of DC offset voltage. An opamp based differential amplifier circuit, with an appropriate gain and cut off frequency is used as shown in Figure 5.4.

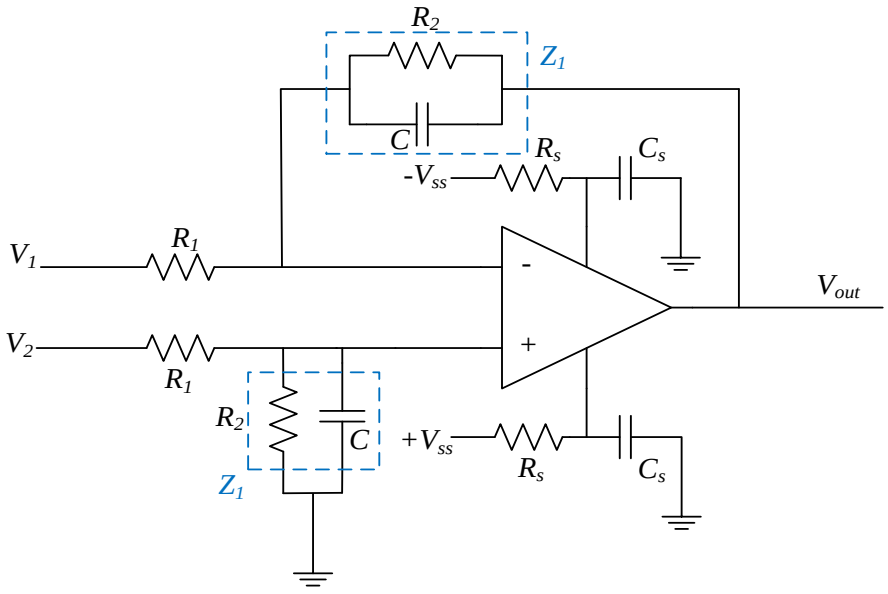


Figure 5.4 Differential op-amp circuit for voltage sensor gain stage.

The relation between the output and the differential input is given as (5.20):

$$\boldsymbol{V_{out} = \frac{R_2}{R_1}(V_1 - V_2)} \tag{5.20}$$

The frequency response of this opamp circuit is shown in Figure 5.5.

$$\textbf{Cut-off Frequency} = \frac{1}{CR_1} \tag{5.21}$$

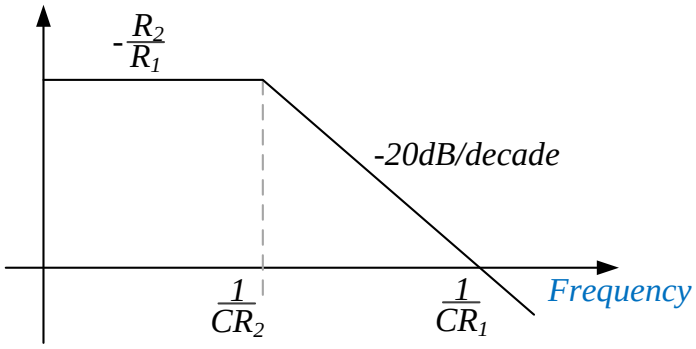


Figure 5.5 Cut-off frequency for the differential op-amp configuration.

The chosen values for different components are:

$$R_1 = 2k, R_2 = 10k, C = 47pF$$

$$V_{out} = \frac{10k}{2k} * (V_1 - V_2)$$

Using (5.20), we get

$$V_{out} = 5(V_1 - V_2)$$

For the input and output voltage sensor, the circuit and the gain values used are same.

5.6.2 Current and Voltage Sensor Signal Conditioning

A robust filter design is needed to protect the converter from high frequency noise and/or unwanted signals. These undesirable signals may affect the normal functioning of the converter. For the control board design, Sallen Key topology is used to design second order filters. A second order filter circuit reduces unnecessary frequency components twice as fast compared to

the normal first order filter circuit. This filter circuit is used after the voltage gain stage or after the current sensor as shown in Figure 5.3.

The general topology for Sallen Key Low Pass Filter is shown in Figure 5.6. The transfer function H(s), cut-off frequency (f_c) and the quality factor (Q) for the filter are given as (5.21), (5.22) and (5.23) [21]:

$$H(s) = \frac{1}{C_1 C_2 R_1 R_2 s^2 + C_2(R_1 + R_2)s + 1} \tag{5.21}$$

$$w_c = 2\pi f_c = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \tag{5.22}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2(R_1 + R_2)} \tag{5.23}$$

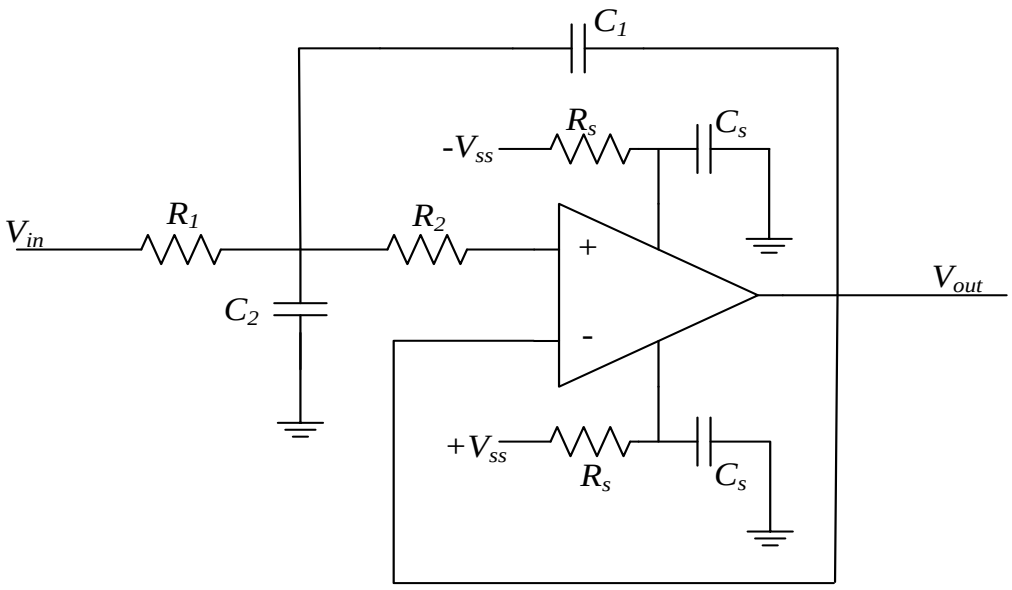


Figure 5.6 Sallen key topology for signal conditioning.

Using (5.21), (5.22), (5.33) and the operational requirements, the R and C values for the circuits are chosen as shown in Table 5-2:

Table 5.2 R, C and f_c values for different signal manipulation stages

Circuits	R_1 (in kΩ)	R_2 (in kΩ)	C_1 (in µF)	C_2 (in µF)	f_c (in kHz)
Input Current Sensor	10	10	0.01	0.02	1.125
Output Current Sensor	10	10	1e-3	1e-3	15.92
Input Voltage Sensor	10	10	1e-3	1e-3	15.92
Output Voltage Sensor	10	10	1e-3	1e-3	15.92

DC Level Shift Circuit:

The DC level shift circuit is required to bring the measured value within the range of 0-3.3V. This is required to utilize the ADC of DSP. For the AC signals, the sensors used would provide both positive and negative values. Adding a DC shift of 1.65V, brings the sensor value between 0-3.3V range. The circuit used for the design is shown in Figure 5.7.

Choosing $R_1 = 150k$ and $R_2 = 90.9k$

$$V_{ref} = 2.5V$$

$$DC\ Shift = \frac{90.9k}{150k} * 2.5V = 1.65V \tag{5.24}$$

This dc shift circuit is used with input voltage sensor and input current which senses grid voltage and current (ac signal). The input voltage sensor circuit with dc offset is shown in Figure 5.8.

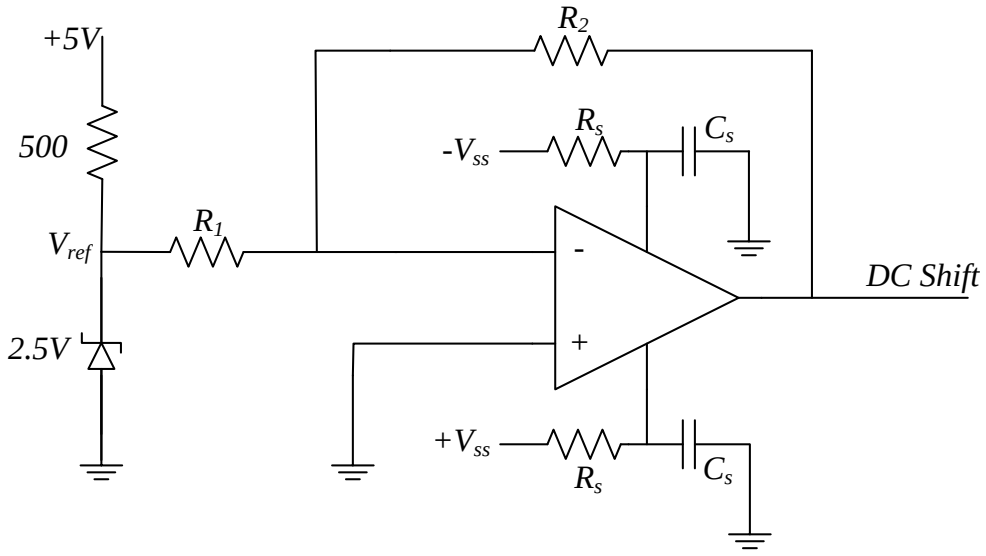


Figure 5.7 DC Level Shift circuit.

Voltage Sensor Circuit utilizing DC offset:

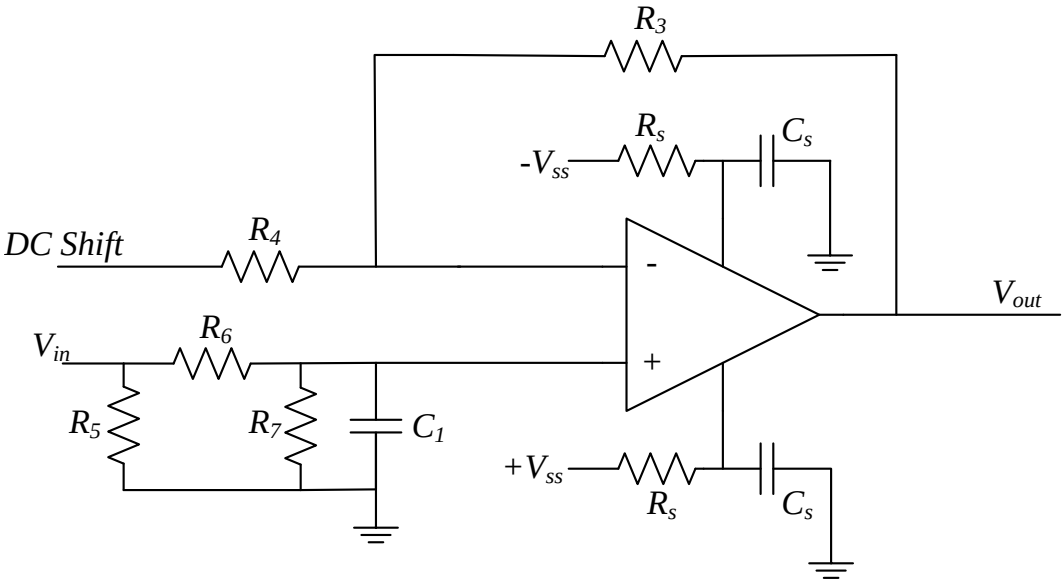


Figure 5.8 Voltage Sensor Circuit utilizing DC offset.

The voltage V_{out} for the op-amp circuit in Figure 5.8 is given as (5.25):

$$V_{out} = DC\ Shift + \frac{R_7}{R_6 + R_7} V_{in} \tag{5.25}$$

Using (5.25) and DC shift of 1.65V, we get

$$V_{out} = 1.65 + \frac{R_7}{R_6 + R_7} V_{in}$$

5.6.3 Snubber Circuit Design

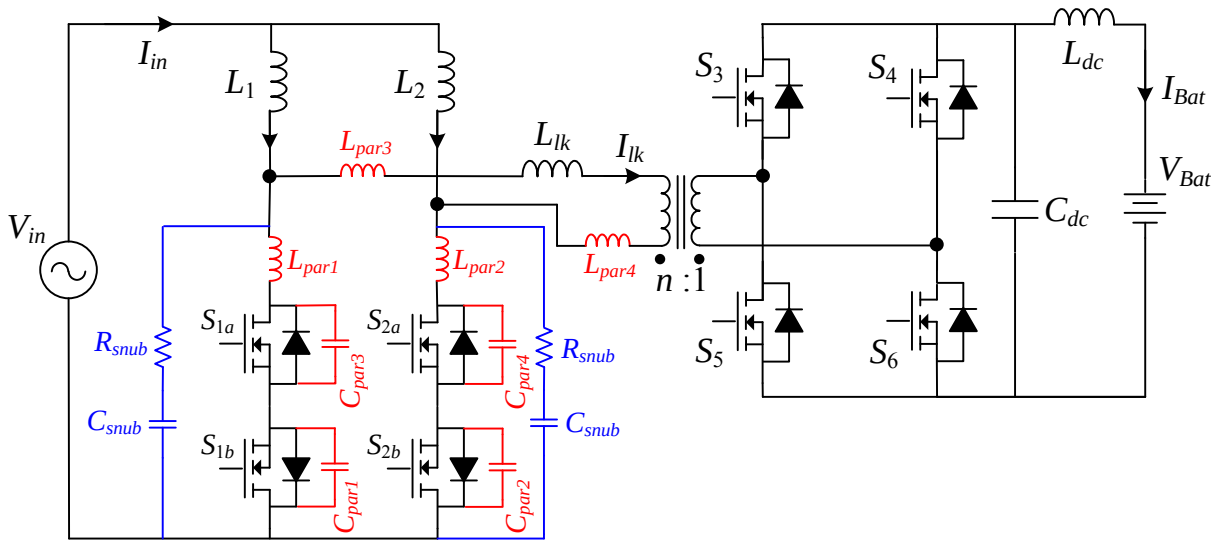


Figure 5.9 Snubber circuit design to reduce the parasitic effect.

The parasitic inductances and capacitance for the primary side of the proposed converter are shown in Figure 5.9. These parasitic components may cause oscillations in the circuit. These oscillations may damage the devices if they exceed their absolute maximum rating. These oscillations are also termed as “ringing”. To reduce the ringing effect, snubber circuits are used. These circuits provide an alternate path to ground, for the currents from parasitic inductances. This reduces the voltage transients and the ringing with the parasitic capacitance.

Since the parasitic inductance shown in Figure 5.9 is much lower than the leakage inductance of the transformer, the oscillation causing inductor value is 25μH. In order to dampen this oscillation, a snubber circuit with a damping ratio (ξ) of 2 utilizing a capacitor of value 150pF is used. The required snubber resistance is calculated as (5.26):

$$R_{snub} = 2\xi\sqrt{\frac{L}{C_{snub}}} \tag{5.26}$$

$$R_{snub} = 1.632K\Omega$$

Hence, the snubber circuits parameters are $R_{snub} = 2k\Omega$ and $C_{snub} = 150pF$.

The maximum voltage across the switch is 600V, when the output dc voltage is 300V (high frequency transformer turns ratio is 2). For a switching frequency of 100kHz, the power loss in the snubber circuit is given as (5.27):

$$P_{loss} = \frac{1}{2}CV^2 f_s \tag{5.27}$$

$$P_{loss} = \frac{1}{2} * 150 * 10^{-12} * 600^2 * 100 * 10^3$$

$$P_{loss} = 2.7W$$

Hence, the power rating for the snubber resistance used is 5W.

5.7 Gate Driver Design

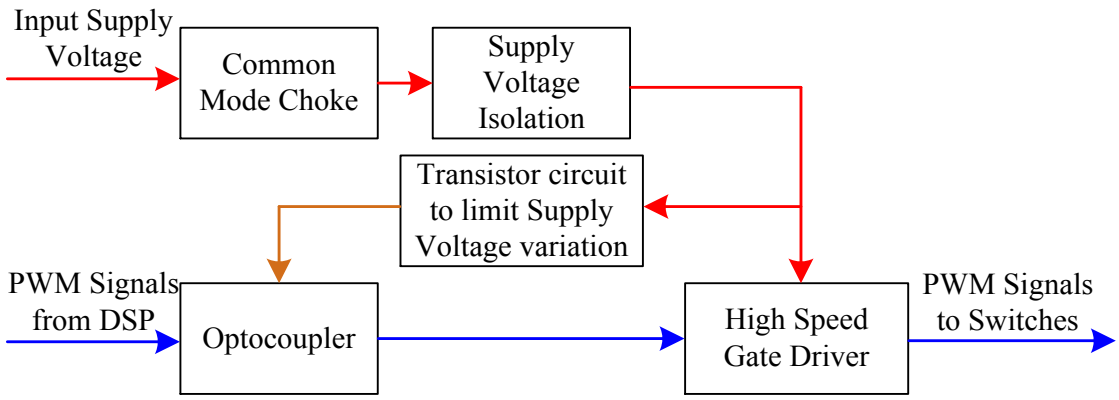


Figure 5.10 Different blocks of the gate driver.

Gate driver circuits should be able to provide the required switching current and voltage within suitable intervals to the semiconductor devices. The switches used for the present converter design are SiC MOSFETs. These devices require a larger voltage swing and higher peak current, compared to other Si devices. For the gate voltage design, the specifications chosen were +15V and -5V with a peak current of 9A. In order to protect these drivers from supply voltage noise, common mode choke and isolated voltage supplies are used. Figure 5.10 shows different blocks of the gate driver circuit.

5.8 Circuit Board Design

The designing process of the board design was similar to any other conventional PCB but the following key points were taken into consideration while doing the layout for the proposed converter PCB [22]:

1. In power routing, the inductance causes voltage drops that radiate and propagate. It increases with the increasing length, and decreases with the width of the conductor. Hence, the tracks for the power supply were kept as short and as wide as possible and they were run directly over each other to reduce impedance and the loop area. Since it would be difficult to route the ground plane every time beneath the power line, a complete layer was made as ground.

2. In order to prevent the cross talk (Cross talk occurs when the signal "bleeds" onto the nearby traces through the parasitic low-impedance path), the distance between the traces is maintained around 2-3 times of the trace width.

3. To avoid the vias for the high speed signals, the top layer is used for all the small signal traces. The use of vias is mainly done for power signals. Signal reflection may occur with through-hole vias, which create multilayer stubs.

4. Power Supply bypassing was done to decouple the unwanted noise from the local integrated circuits (IC). In order to achieve so capacitors with low ESR were placed close to the power supply pins of the given IC. This guarantees a low impedance bypass to ground for efficient decoupling of high frequency power-supply noise.

5. In order to lower ESR and ESL, ceramic capacitors and resistors of 0603 package were used.

6. All the power supplies of the control board, the gate driver board and the power board are isolated from each other in order to avoid any noise interference because of common ground.

7. While laying down the isolated power supplies tracks proper care was taken not to run any traces through the package footprint as it might void the isolation characteristics of that particular IC or component.

5.9 Final Developed Hardware Circuit

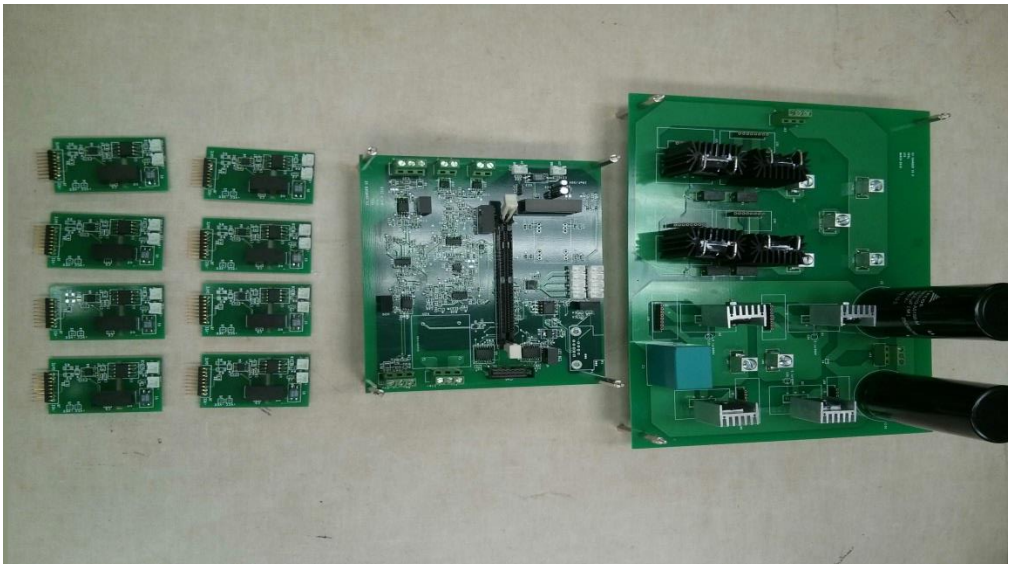


Figure 5.11 Gate Driver Boards, Control Board and the Power Board of the EV Charger.

Figure 5.11 shows the different boards for the complete EV charger. Better isolation is achieved by having separate boards. The control board and the gate driver boards, in this case, are protected better from noise that may occur due to switching or other parasitic associated with the circuit.

The control board is a four layer PCB, gate driver board and the power board are both double layer PCB's.

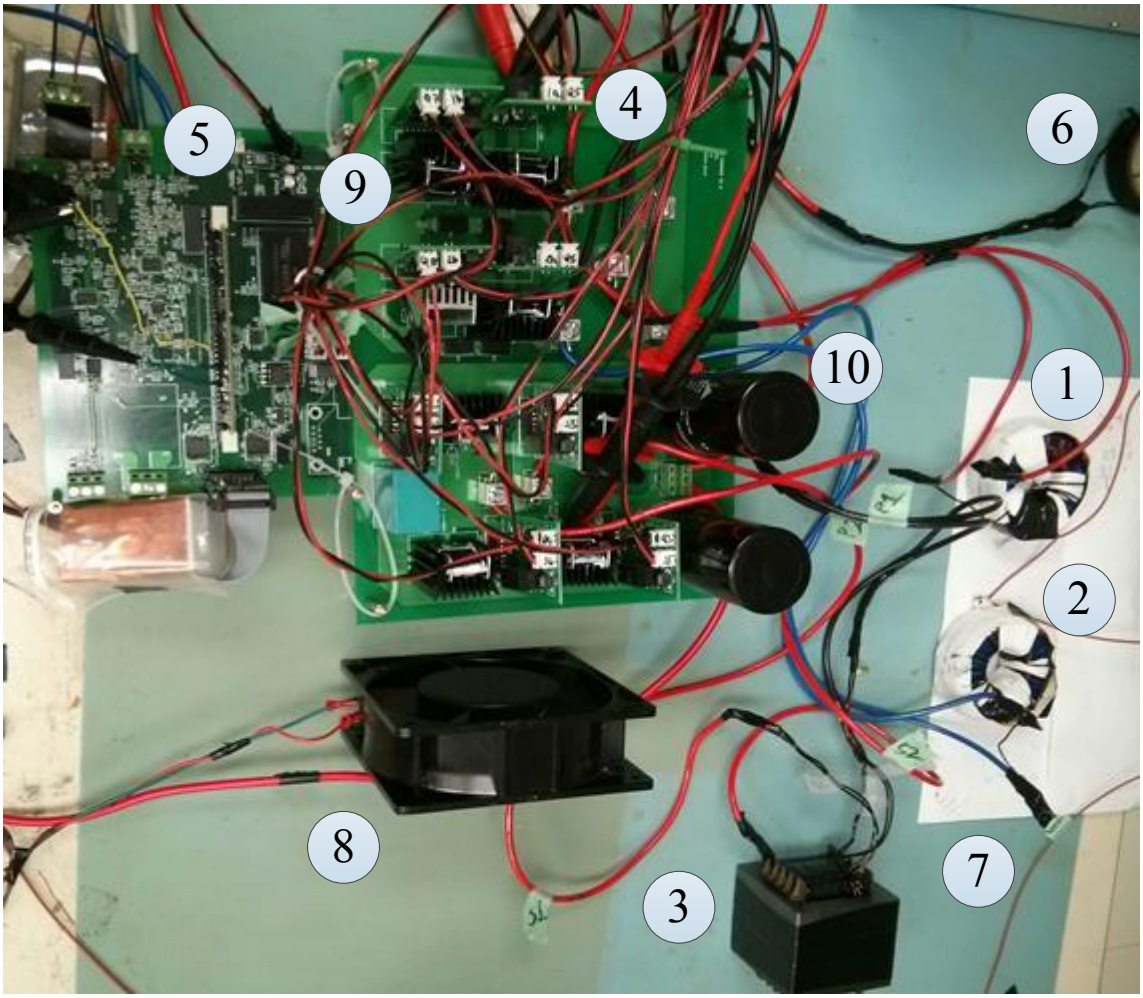


Figure 5.12 EV Charger Board with all the connections and components.

The notations for the numbers used in the Figure 5.12, are shown in Table 5-3.

Table 5.3 Description of the numbers in Figure 5.12.

1. Filter Inductor	6. Additional Leakage Inductance
2. Filter Inductor	7. Ground Wire for Shields
3. Transformer	8. Cooling Fan
4. Gate Driver Board	9. MOSFETs
5. Controller Board	10. Capacitor

CHAPTER 6

SIMULATION AND EXPERIMENTAL RESULTS FOR THE PROPOSED SOFT SWITCHING EV CHARGER TOPOLOGY

This chapter discusses the various results obtained from simulation which are validated by the experimental setup of the proposed EV charger. Section 6.1 discusses the simulation results which verify the mathematical model derived in Chapter 4. In section 6.2, experimental results are presented, which validate the design and the control strategy of the proposed converter.

6.1 Simulation Results

The proposed converter was simulated using the PSIM platform. It was tested for different modes of power flow discussed in Chapter 3. The values of the passive components and switches are chosen according to the design equations derived in Chapter 5.

Figure 6.1 shows the simulation waveform for the grid integration and transient response. The input voltage from grid, V_{in}, current drawn by the source, I_{in} and current flowing through the input inductor, I_{L1} are shown during power flow in both directions. V_{in} of 120 V_{rms} and V_{Bat} of 300V are considered. Initially, the power reference P_{ref} is set to zero. At t = 0.075s, P_{ref} of 1.5kW is commanded to the controller changing the input current to 17.7A peak. Both input voltage and current are in phase operating in unity power factor. At t = 0.1s, P_{ref} is changed to (-

1.5kW). Input current goes 180° phase shifted with respect to the grid voltage instantly demonstrating the dynamic performance of the controller.

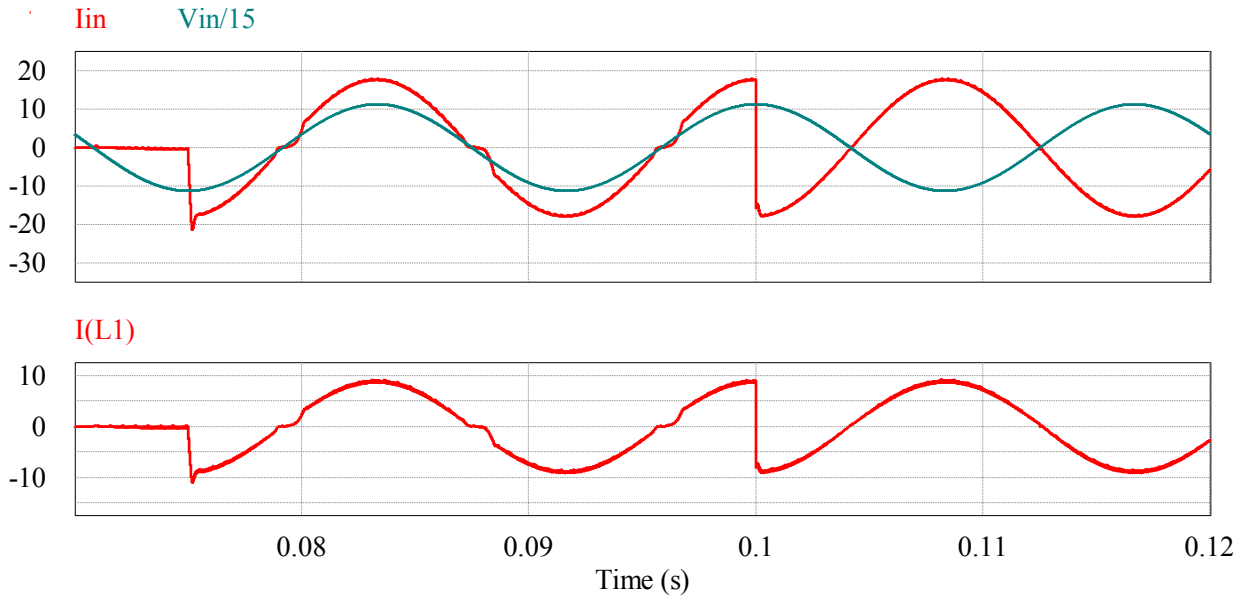


Figure 6.1 Simulation waveform for grid integration and transient response.

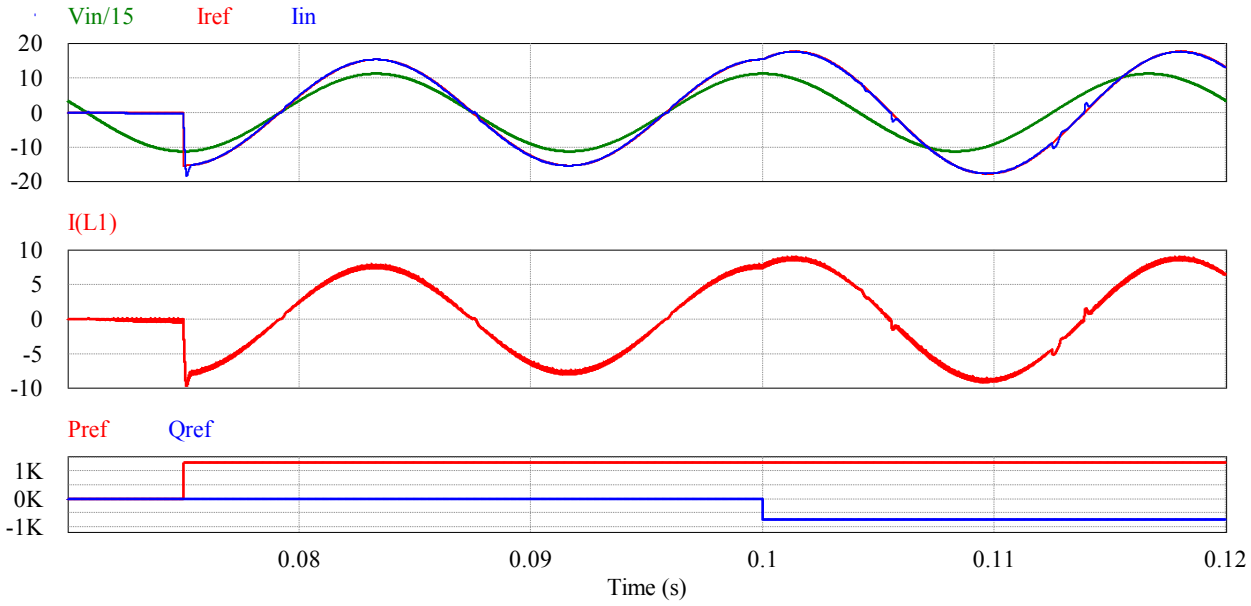


Figure 6.2 Simulation results showing reactive power transfer.

Figure 6.2 shows the simulation results for the reactive power transfer capability of the converter. In this figure, P_{ref} is set to 1.3kW at t = 0.075s keeping the reference for reactive power, Q_{ref} to 0kVAr. At t = 0.1s, Q_{ref} of -0.7kVAr is being commanded with the converter functioning at 1.47kVA of power.

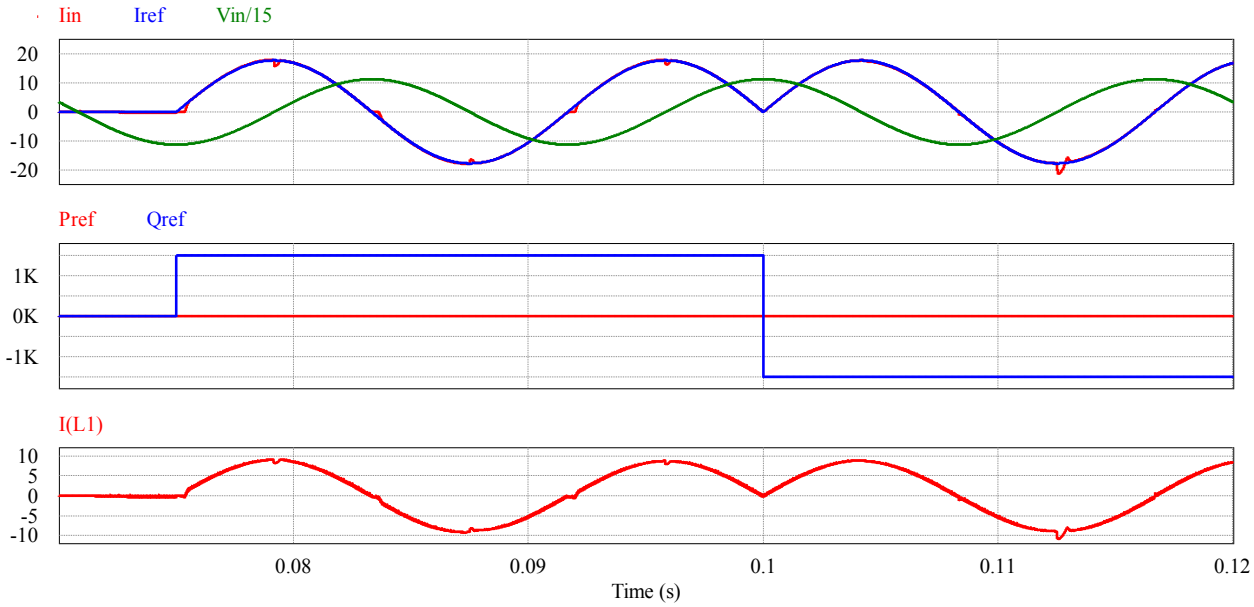


Figure 6.3 Simulation results showing the reactive power compensation.

Figure 6.3 simulation results show the reactive power compensation capability of the converter. It is possible to utilize the converter for reactive power compensation during the idle condition transferring only reactive power without charging/discharging the battery. Figure 6.2 and Figure 6.3 also demonstrate the ability of the converter to operate in all the four quadrants providing flexibility to control both active and reactive power flow in both the directions.

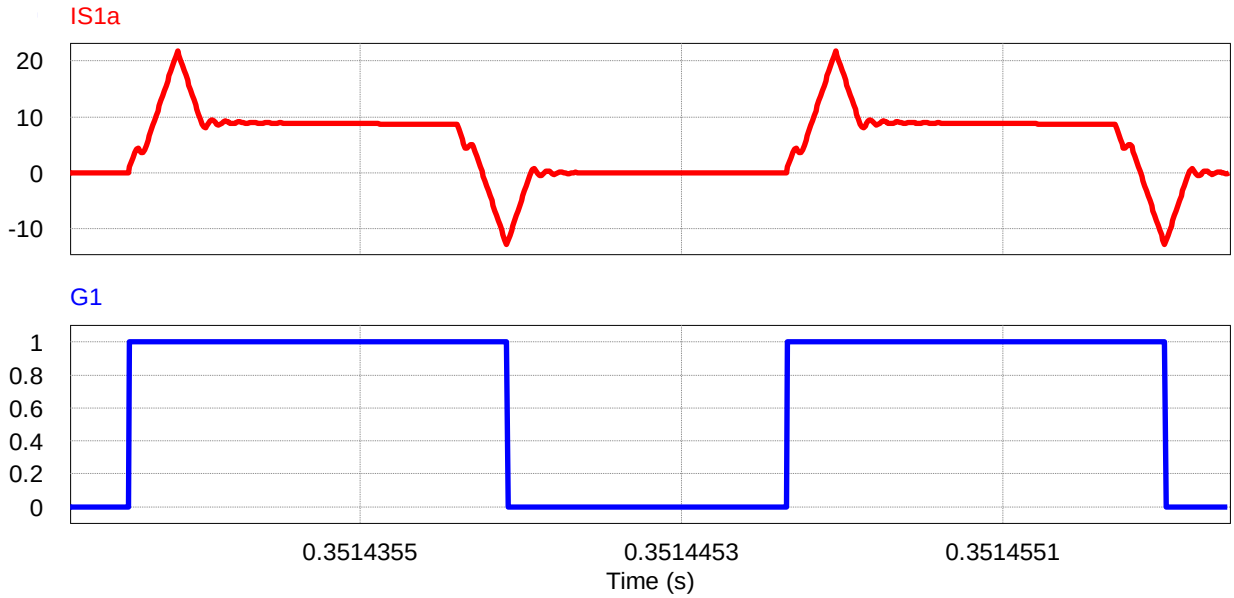


Figure 6.4 Simulation waveforms showing ZCS of primary switch.

Figure 6.4 demonstrates the ZCS of the primary switch of the converter. The current through the switch S1a and the associated gate signal with the switch during the operation in mode-1 or mode-2 is shown. The current in the switch naturally reaches zero without any additional circuit before removing the gate signal achieving ZCS. This is maintained for all the conditions of the voltage and load range. The equations for which are described in the design section of the Chapter 5.

Figure 6.5 shows the simulation waveforms demonstrating the zero current turn on of secondary switch. The current through one of the secondary devices along with its associated gate signal is shown during operation in mode-1 or mode-2, when power is flowing from the grid to the battery. When the gate signal is turned-on, the current starts from zero with positive slope to achieve zero current turn-on of the devices on secondary.

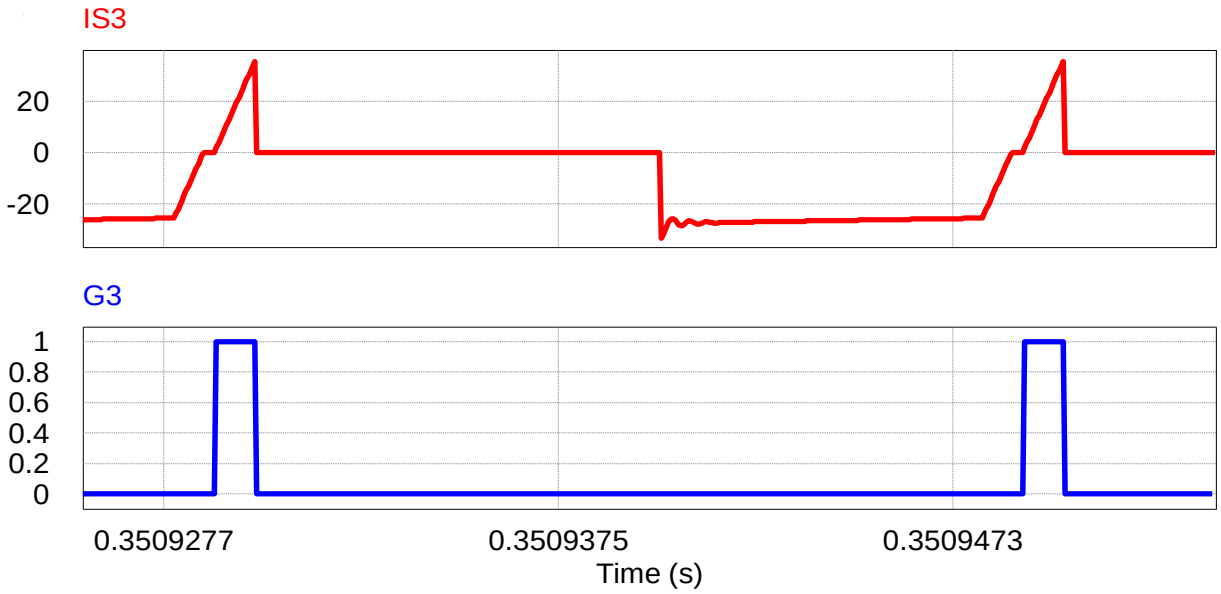
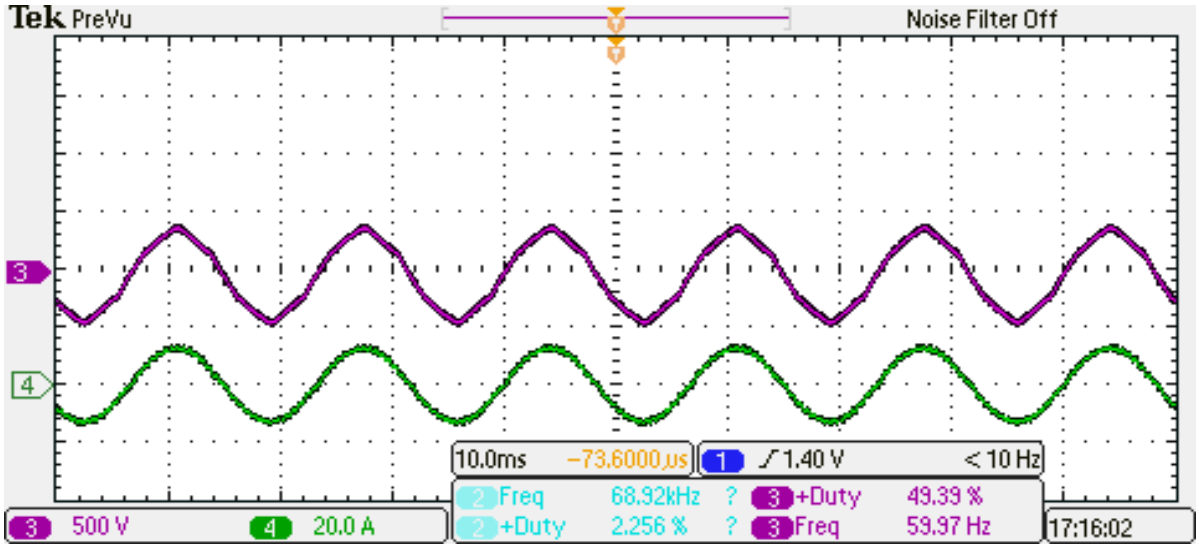


Figure 6.5 Simulation waveforms showing zero current turn on of secondary switch.

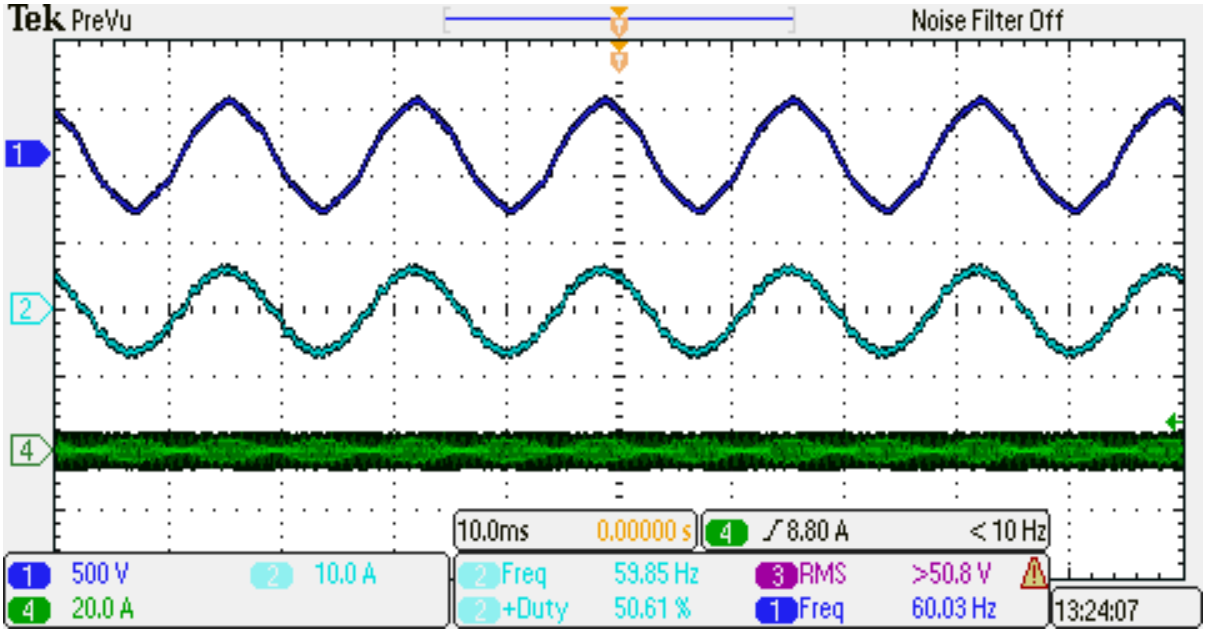
6.2 Experimental Results

This section discusses the experimental results. The results are shown separately for grid to vehicle and vehicle to grid power transfer.

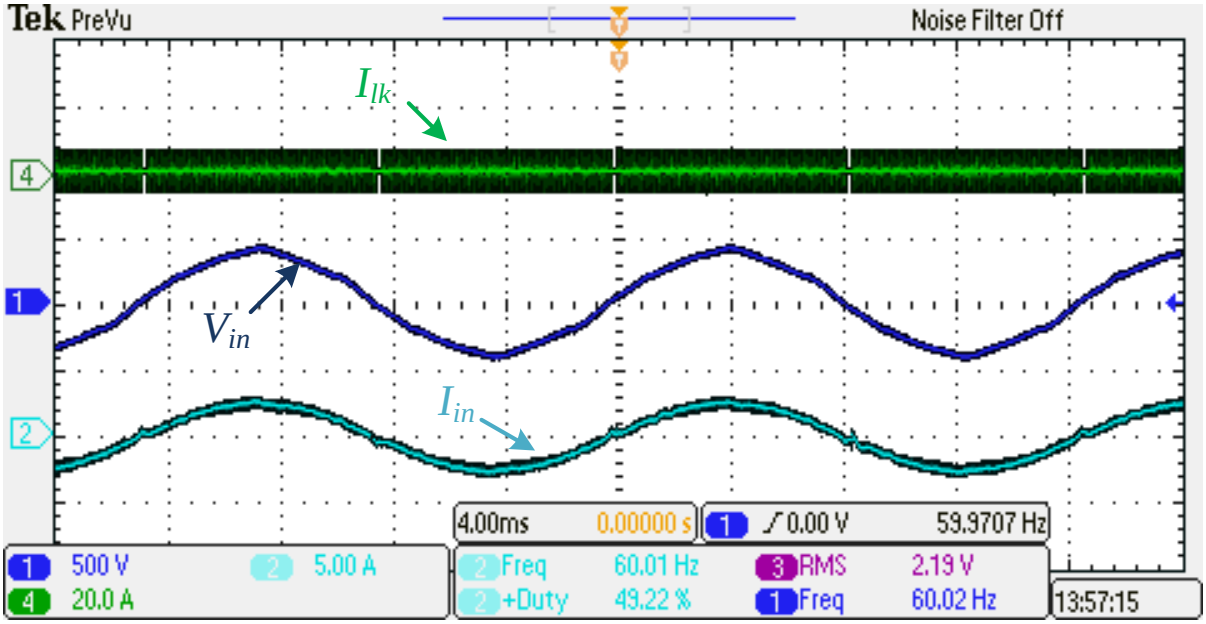
For the experimental setup, tests are performed for different power and voltage levels. Experimental results for G2V mode are shown in Figure 6.6 where power from ac grid is converted to dc. The waveforms of the grid voltage and the current drawn from the ac source show the unity power factor operation of the converter at different power levels. Input current is regulated to be in-phase with the voltage while also maintaining THD to be less than 5%. The experimental waveforms are coinciding and similar to the waveforms shown in Figure 6.1. The accuracy of the mathematical analysis and design of the converter described in Chapter 4 and Chapter 5 is verified by these waveforms.


Tek PreVu
Noise Filter Off
3
4
10.0ms
−73.6000 µs
1 ⁄ 1.40 V
< 10 Hz
2 Freq 68.92kHz ? 3 +Duty 49.39 %
2 +Duty 2.256 % ? 3 Freq 59.97 Hz
3 500 V
4 20.0 A
17:16:02

(a)

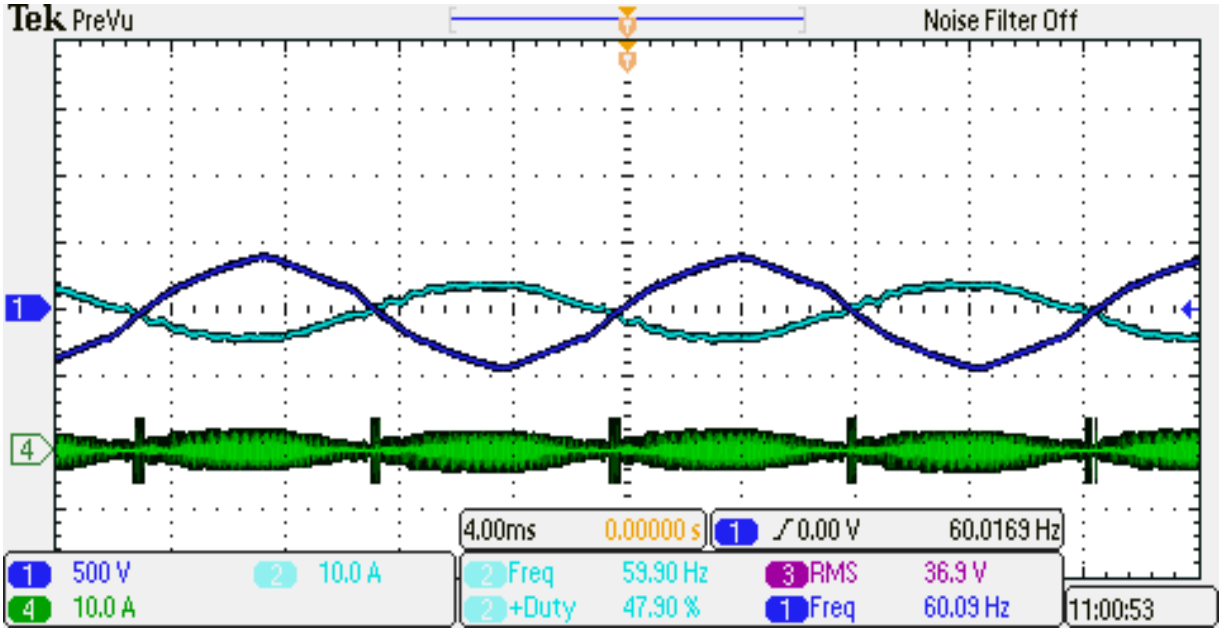

Tek PreVu
Noise Filter Off
1
2
4
10.0ms
0.00000 s
4 ⁄ 8.80 A
< 10 Hz
1 500 V
2 10.0 A
4 20.0 A
2 Freq 59.85 Hz
3 RMS >50.8 V
2 +Duty 50.61 %
1 Freq 60.03 Hz
13:24:07

(b)

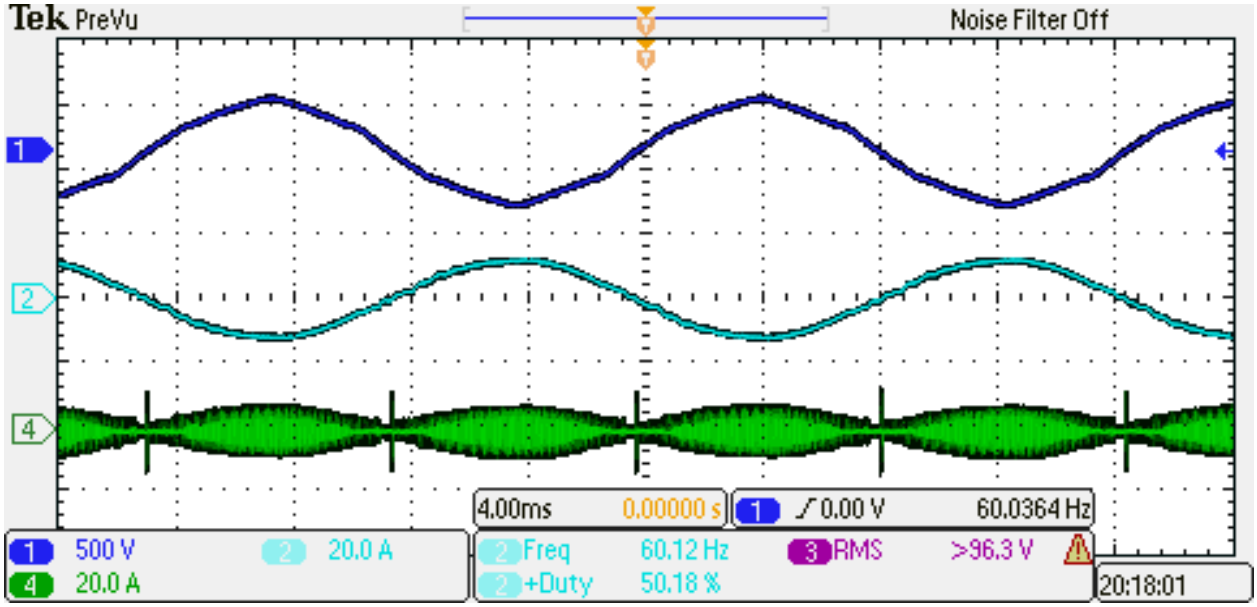


(c)

Figure 6.6 Experimental results for conversion from AC-DC (G2V mode). (a), (b), (c).



(a)



(b)

Figure 6.7 Experimental results for conversion from DC-AC (V2G mode). (a), (b).

The peak value of the leakage inductor current shown in the Figure 6.6(b) and Figure 6.6(c) is within the calculated limits without any spikes. The current naturally reduces to zero and the negative current shows the conduction of the antiparallel diode across the switch, causing ZCS turn-off. Soft-switching is maintained well throughout the cycle and also at lower power levels.

Experimental results for V2G mode are shown in Figure 6.7. The voltage and current waveforms are as per the predicted simulation waveform shown in Figure 6.3. It also demonstrates the ability of the power factor to compensate for specific reactive power demands.

The experimental results confirm the four quadrant operation capability if the converter along with ZCS and zero current turn on secondary switches. The ringing free current and the voltage waveforms reduce the electromagnetic interference in the circuit.

The rms value of the currents change proportionate to the output of the converter. Hence the losses under light load conditions are not affected in the semiconductor devices and the transformer. But in conventional active-clamped converters, the duty cycle of the auxiliary switches is comparable to the duty cycle of the main switches. The auxiliary devices have higher conduction losses at light load as they have high ON-sate resistance due to their low current rating.

CHAPTER 7

CONCLUSION AND FUTURE WORK

This thesis investigates the problems associated with the current EV charger technologies. A novel bidirectional single-phase single-stage isolated AC-DC converter with PFC for EV charging is proposed and experimental unit is demonstrated. The conclusions and recommendations for future work are presented in this chapter.

7.1 Summary

- Different types and standard of EV charger are discussed. The requirements for the EV charger to efficiently work with the grid are described.
- A review of different soft switching EV charger topologies is presented highlighting the limitations of existing hard switched and soft switched converter based EV chargers.
- A novel bidirectional single-phase single-stage isolated AC-DC converter with PFC for EV charging is proposed. The design is compact and light weight, making it suitable to be used for wide variety of EV charger applications, especially for on board charging purpose. It has current-fed half-bridge converter on primary with ZCS and full-bridge converter on secondary with zero current turn-on. Two interleaved phases at the grid side reduces the input current ripple and moves the harmonics to twice the switching frequency reducing the size of input filter. Soft-switching is achieved throughout the operation range without any additional active/passive circuit reducing the heat sink

requirement. Converter can be operated in all four quadrants with regulation of active and reactive power flow in both the directions. HF transformer provides galvanic isolation and flexibility in the design for a wide range of grid and battery voltages.

- The control for the proposed converter is designed using the frequency response analysis method. The mathematical model to be used for the design is derived using the different operational states of the converter. The different modules required for the operation are described. The hardware design along with the component selection has been discussed. The sensor and the signal conditioning op-amp circuits to be used for the control board are developed. Few considerations for laying out the PCB have also been highlighted.
- The simulation results are shown for the operation of the converter. The developed hardware operation and performance is validated with the simulation results.

7.2 Future Work

The computational speed of the DSP was not sufficient to run the entire code within the 100 kHz switching interval. The code used for the charger realization consisted of two different interrupt subroutines, the computation subroutine was run at 50 kHz and the switching subroutine was run at 100 kHz. The controller could be improved using a faster DSP

The power board may be redesigned to have a closer arrangement of the components to minimize the parasitic effects. The snubber circuit can also be made into a separate circuit to minimize its distance with the switches.

These suggestions may optimize the performance of the converter with a possible increase in the overall efficiency.

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VITA

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