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Accumulation Capacitance Frequency Dispersion of III-V Metal-Insulator-Semiconductor Devices due to Disorder Induced Gap States

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The origin of the anomalous frequency dispersion in accumulation capacitance of metal-insulator-semiconductor devices on InGaAs and InP substrates is investigated using modeling, electrical characterization, and chemical characterization. A comparison of the border trap model and the disorder induced gap state model for frequency dispersion is performed. The fitting of both models to experimental data indicate that the defects responsible for the measured dispersion are within approximately 0.8 nm of the surface of the crystalline semiconductor. The correlation between the spectroscopically detected bonding states at the dielectric/III-V interface, the interfacial defect density determined using capacitance-voltage, and modeled capacitance-voltage response strongly suggests that these defects are associated with the disruption of the III-V atomic bonding and not border traps associated with bonding defects within the high-k dielectric. © *2014 AIP Publishing LLC*.
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I. INTRODUCTION

Frequency dispersion in accumulation is a commonly observed feature in the experimental capacitance-voltage (C-V) characteristics of III-V metal-insulator-semiconductor (MIS) devices. This dispersion has been reported on a wide variety of III-V substrates such as GaAs,[1–5] $In_{0.53}Ga_{0.47}As$,[6–16] InP,[17,18] and GaSb.[19] Particularly on $In_{0.53}Ga_{0.47}As$ substrates, dispersion has been reported for a variety of dielectrics including Al_2O_3,[6,7,15,16,20] HfO_2,[12] ZrO_2,[10] LaAlO,[8] HfAlO,[13] MgO,[14] Si_3N_4,[11] and ErO_x.[9]

For silicon-based MIS devices, dispersion of the capacitance in accumulation due to defects is not typically observed. Even for a reasonably high interface defect density ($\sim 10^{12}/cm^2eV^{-1}$), the measured frequency response is typically small and present only in the depletion region of the capacitance-voltage characteristic (interface state "hump"). For silicon, the primary defects associated with frequency dispersion in depletion are the well-known P_b centers; unsatisfied dangling bonds of the (substrate) crystalline silicon atoms at the immediate interface with the dielectric.[21] This is the case for silicon oxide dielectrics as well as the vast majority of metal oxides where a very thin silicon dioxide interlayer is typically present.[22] This capacitance dispersion behavior for silicon is modeled using the conventional approach developed by Nicollian and Brews which accounts for the inelastic capture and emission of free carriers at the surface of the crystalline silicon, but does not typically require transport of these carriers into the interfacial region or insulator.[23] The lack of accumulation dispersion for silicon MIS devices is attributed to the low defect density and high band offsets with the insulator.

There have been numerous publications on modeling of the capacitance accumulation dispersion for III-V MIS devices.[1,2,4–7,15,16,24–26] All of these models require transport of carriers from the crystalline semiconductor into either a disordered and defective interfacial region or into defects within the bulk of the dielectric itself. All of these models begin with the results of Heiman and Warfield[27] whereby the impedance associated with a trap a distance, x, away from the outermost layer of the undisrupted crystalline semiconductor can be calculated by assuming that it has a trapping time constant given by

$$\tau = \tau_0 e^{2\kappa x}, \tag{1}$$

where

$$\tau_0 = \frac{1}{\sigma v_t n} \quad \text{and} \quad \kappa = \sqrt{\frac{2m^*_{ox}\Delta E_c}{\hbar^2}}, \tag{2) and (3}$$

where τ_0 is the trap time constant at the interface, κ is the attenuation coefficient of the decaying electron wave function, σ is the electron capture cross section, v_t is the thermal velocity of the electrons, n is the surface electron density, m^*_{ox} is the effective mass of the electron in the oxide, ΔE_c is the conduction band offset between the oxide and the semiconductor, and $\hbar$ is the reduced Planck constant. The distance into the disordered interfacial layer or insulator that is probed at a given frequency is calculated as

$$x_{tun} = \frac{1}{2\kappa}\ln\left(\frac{1}{\omega\tau_0}\right), \tag{4}$$

where $\omega = 2\pi f$ and f is the measurement frequency (Hz).

Starting with the Heiman and Warfield formulation for effective trapping time constant, Hasegawa and Sawada developed the Disorder Induced Gap State (DIGS) model which assumed that the trap capacitance is parallel with the semiconductor capacitance (C_{semi}) and in series with the oxide capacitance ($C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, where ε_{ox} and t_{ox} are the dielectric constant and thickness of the insulator, respectively) as shown in Fig. 1(a).[1,5,24,25] The model also assumed an exponentially decreasing trap distribution away from the semiconductor-insulator interface

$$N_{DIGS} = N_{t0}e^{-\alpha x}, \tag{5}$$

where N_{t_0} is the trap density at the interface of the semiconductor and the dielectric and α is a decay constant. Using detailed electrical and physical characterization of thick dielectrics available at that time, they concluded that the majority of defects resulting in capacitance dispersion were associated with a near-interfacial disordered region caused by dielectric deposition and resulting in DIGS. With these assumptions, the trap capacitance can then be written as

$$C_{DIGS} = \frac{q^2 N_{t0}}{2\kappa}(\omega\tau_0)^{\frac{\alpha}{2\kappa}} \int_0^{\frac{1}{\omega\tau_0}} (z)^{\frac{\alpha}{2\kappa}} \tan^{-1}(z^{-1})dz. \tag{6}$$

The total capacitance (C_{total}) is then

$$C_{total} = ((C_{semi} + C_{DIGS})^{-1} + C_{ox}^{-1})^{-1}. \tag{7}$$

We previously studied III-V devices with thin atomic-layer-deposited (ALD) dielectrics and confirmed that: (1) the Nicollian and Brews model for interface states cannot explain the dispersion behavior for these interfaces and (2) that the salient features of the dispersion are consistent with the Hasegawa and Sawada model if the spatial distribution of defects is approximately uniform into the dielectric (small α).[5]

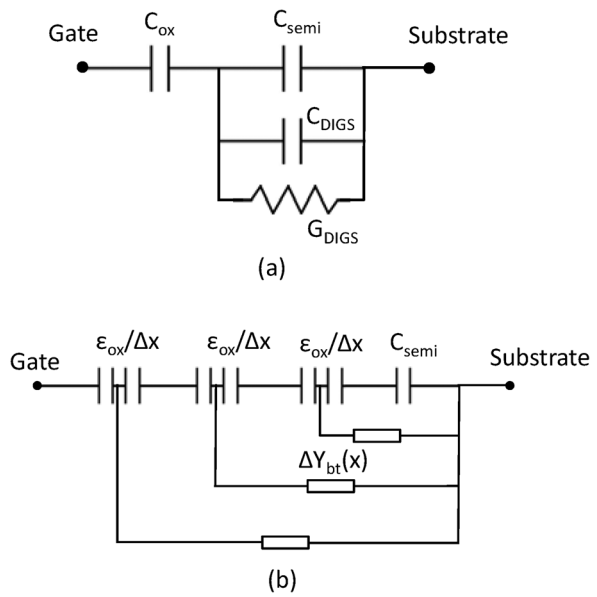

FIG. 1. Equivalent circuits for the (a) Disorder Induced Gap State model, and the (b) Border Trap model.

More recently, Taur and co-workers developed another model which also begins with the results of Heiman and Warfield.[6,7,15,16] This distributed border trap (BT) model calculates the incremental trap impedance as

$$\Delta Y_{bt}(x) = \frac{q^2 N_{bt}(x)\ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}}\Delta x, \tag{8}$$

where q is the electron charge, $N_{bt}(x)$ is the density of the border traps, and Δx is the incremental depth at a position x into the insulator. The total impedance of the MIS device is then calculated numerically and C_{total} is extracted from the total impedance. There are several important differences between this BT model by Taur *et al.* and the DIGS model of Hasegawa and Sawada: (1) the BT model requires numerical simulation but permits an arbitrary distribution of defects as a function of distance into the dielectric (however, Taur *et al.* also finds that a uniform spatial distribution of defects best fits experimental data), (2) the defect capacitance is piece-wise parallel with the incremental dielectric capacitance as shown in Fig. 1(b), and (3) the authors explicitly state that defects responsible for the dispersion are contained within the dielectric itself ("trap states inside the gate insulator, called bulk-oxide traps or border traps").[16] This definition of border traps is consistent with the original definition provided for the Si/SiO_2 interface in which border traps were due to defects primarily associated with the bonding and structure of the *bulk* of SiO_2 (E' centers), but close to the crystalline Si semiconductor so as to enable efficient tunneling.[28]

In the following, we explore the similarities and differences of the BT and DIGS models by varying key model parameters and by fitting experimental data. The conclusions that can be drawn based on the fits of these models to experimental data are then described. The results of detailed physical characterization as well as results from the literature are then used to determine the physical nature of the defects responsible for the observed frequency dispersion in capacitance-voltage behavior. We note here that our primary focus for this paper is the defects responsible for frequency dispersion in accumulation. The defects responsible for dispersion in depletion are not considered.

II. COMPARISON OF THE BT AND DIGS MODELS

Before fitting the two models to experimental data, the impact of key parameters on the modeled capacitance versus frequency behavior will first be explored. In the following, a uniform trap distribution is assumed for both models ($\alpha = 0$) with trap density, N_t. Figures 2(a) and 2(b) show the modeled total capacitance as a function of frequency for the DIGS and BT models, respectively. The modeled data labeled as reference uses the following parameters ($\tau_0 = 8\,\mu s$, $\kappa = 6 \times 10^7\,cm^{-1}$, $N_t = 3.5 \times 10^{20}\,cm^{-3}eV^{-1}$, $C_{semi} = 2.5\,\mu F/cm^2$, $t_{ox} = 12\,nm$, $\varepsilon_{ox} = 20\varepsilon_0$). Each of these parameters is then individually varied while keeping the remaining parameters the same.

At high frequencies above the inverse of the trap time constant, the defect capacitance becomes very small so that

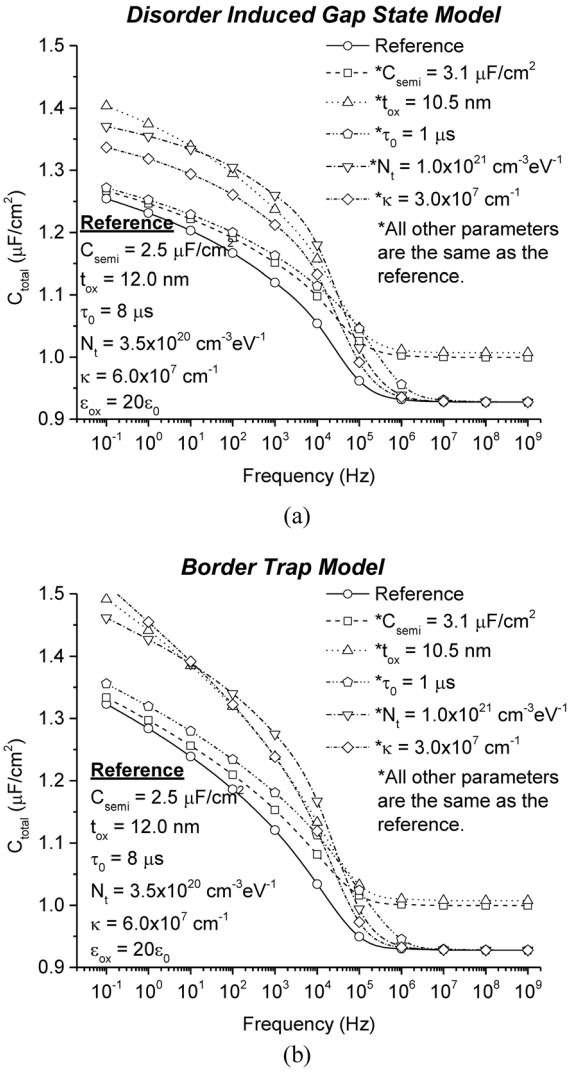

FIG. 2. Capacitance-frequency characteristics generated using the (a) Disorder Induced Gap State model, and the (b) Border Trap Model.

both models have a minimum capacitance (C_{min}) equal to the series combination of C_{semi} and C_{ox}

$$C_{\min} = \frac{C_{ox}C_{semi}}{C_{ox} + C_{semi}}. \quad (9)$$

For the reference models, $C_{min} = 0.94\ \mu F/cm^2$. For both models, C_{semi} is observed to change the minimum capacitance but does not dramatically alter the maximum capacitance at low frequencies. The t_{ox}, on the other hand, is observed to modify both the minimum capacitance and the maximum capacitance at low frequencies.

One of the key differences between the models is that the maximum capacitance at very low frequencies for the DIGS model is C_{ox}. In the BT model, the oxide thickness is divided into n subsections of thickness $\Delta x = t_{ox}/n$. The trap capacitance arising from the tunneling of the electron into the border traps at the position x is in parallel with $\varepsilon_{ox}/\Delta x$. Because of this equivalent circuit, the distributed BT model predicts that the measured C_{total} at low frequency (below frequencies typically probed by experiment) should be significantly higher than C_{ox}.[6] However, we are not aware of experimental evidence for $C_{total} > C_{ox}$ for III-V MIS capacitors.

Because of the differences in the equivalent circuit assumed, the BT model shows more linearity in C_{total} versus f at low frequency as compared to the DIGS model. For both models, τ_0 is observed to change the frequency at which C_{total} reaches C_{min} but does not strongly change the shape of the curve at low frequencies. For frequencies at which $\omega\tau_0 >\sim 1$, the defect capacitance becomes small and the total capacitance is dominated by C_{ox} and C_{semi}. It is also observed that none of the other parameters strongly modify the frequency at which this occurs. N_t is observed to change the magnitude of C_{total} at low frequencies but does not strongly modify the shape of the curve. κ is observed to also modify the magnitude of C_{total} at low frequencies and modifies the shape of the C_{total} versus f.

Overall, these results suggest that experimental C_{total} versus f curves can likely be fit using a variety of non-unique solutions. Therefore, fitting of data using these models should be accompanied by a description of the assumptions used to determine the best fit and conclusions drawn from these models must consider these assumptions.

III. FITTING OF EXPERIMENTAL DATA USING THE BT AND DIGS MODELS

Metal-oxide-semiconductor capacitors were fabricated on n-type $In_{0.53}Ga_{0.47}As$ and n-type InP substrates with ALD HfO_2 and Al_2O_3 dielectrics. Details of the InP MOS capacitor fabrication process are described elsewhere.[17,18] $In_{0.53}Ga_{0.47}As$ MIS capacitors were fabricated with the same process flow. Figures 3 and 4 show the experimental C-V results for $In_{0.53}Ga_{0.47}As$ and InP MIS capacitors, respectively, with Al_2O_3 and HfO_2 gate dielectrics. $In_{0.53}Ga_{0.47}As$ substrate devices demonstrate qualitatively similar response to the InP substrate MIS capacitors,[12,13] i.e., frequency dispersion in the accumulation region which is indicative of a large density of traps somewhere in the gate stack. For the accumulation dispersion, we rule out parasitic responses such as series resistance which would manifest itself in an ω^{-2} dependence and is not observed in the experimental data.[29,30] The leakage current for these devices is also low, further precluding the impact of series resistance on the experimental results. Low temperature measurements were also taken on these MIS devices to verify that these devices exhibit true accumulation. Measurements at 77 K (not shown) show almost no dispersion indicating that the devices reach true accumulation.

To ensure that our results are consistent with previous work by others, Fig. 5 shows C_{total} in accumulation as a function of measurement frequency for our experimental results as well as similar results from the literature.[15,31–34] The change in total accumulation capacitance from the lowest to highest measurement frequency for our results is largely consistent with those of the literature. We note that while the substrates and dielectrics used for our comparisons are the same, many of the experimental conditions (e.g., oxide thickness, pre-treatments, annealing conditions) are different. For example, Chobpattana *et al.*[33] showed that the

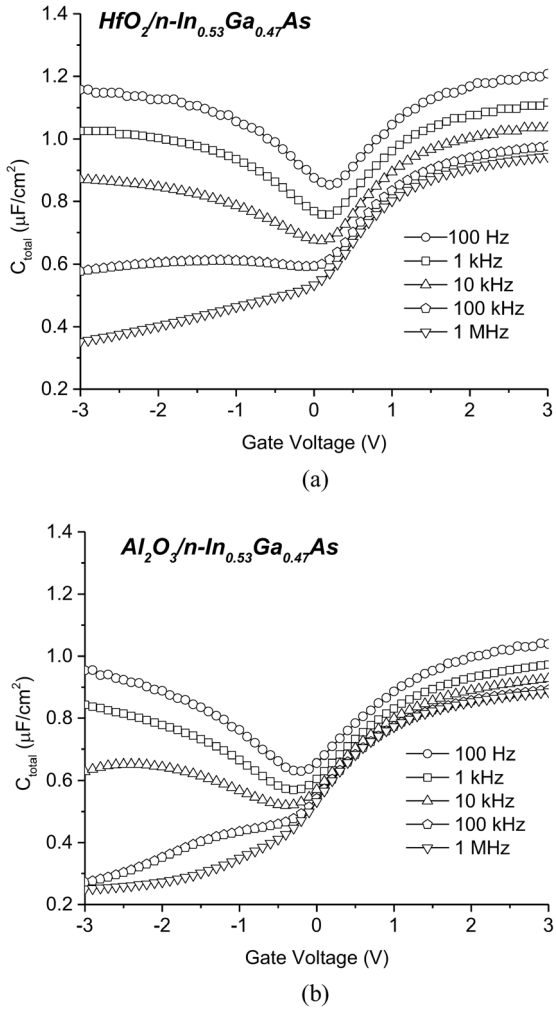

FIG. 3. Experimental capacitance-voltage characteristics as a function of frequency for (a) HfO_2 and (b) Al_2O_3 on n-type $In_{0.53}Ga_{0.47}As$.

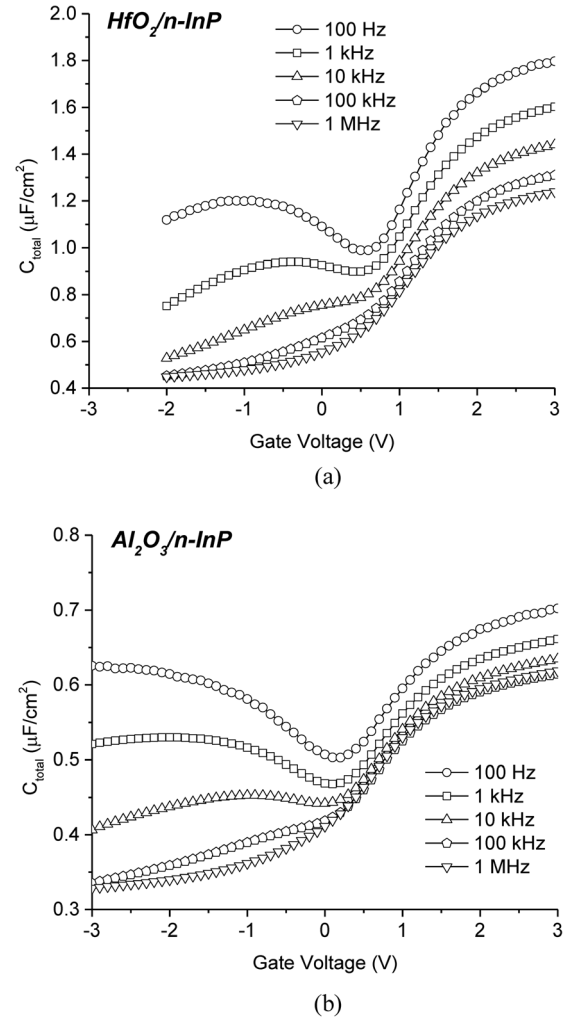

FIG. 4. Experimental capacitance-voltage characteristics as a function of frequency for (a) HfO_2 and (b) Al_2O_3 on n-type InP. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **102**(13), 132903 (2013). Copyright 2013 AIP Publishing LLC. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **99**(17), 172901 (2011). Copyright 2011 AIP Publishing LLC.

dispersion in depletion for $HfO_2/In_{0.47}Ga_{0.53}$ can be improved using a nitrogen plasma pre-treatment of the substrate. However, the dispersion in accumulation is largely unchanged with this treatment. This is likely due to differences in the atomic scale structure of defects responsible for dispersion in depletion compared to those in accumulation.[35] Therefore, this comparison indicates that our data for accumulation dispersion is consistent with the state-of-the-art.

Figure 6 shows our fits of both the DIGS and BT model to the experimental C_{total} at gate voltage of 2.5 V as a function of measurement frequency. The exact same parameters (shown in Table I) were used to fit both the DIGS and BT model to a given set of experimental data for each device. To obtain the fits, the following assumptions were used: The oxide thickness was obtained by assuming 0.8 nm to 0.85 nm per ALD cycle which is expected, and previously measured, for our ALD process. The dielectric constant of HfO_2 is assumed to be $\varepsilon_{ox} = 20\varepsilon_0$ and that of Al_2O_3 is assumed to be $\varepsilon_{ox} = 7\varepsilon_0$. Given the C_{ox} for each device, C_{semi} is determined by fitting the magnitude of C_{min} at high frequencies. The extracted values of C_{semi} (2.5 μF/cm^2 to 3.0 μF/cm^2) are consistent with values found using simulation of ideal capacitance-voltage behavior. N_t and κ were chosen to best fit the magnitude and shape of C_{total} at lower frequencies. N_t

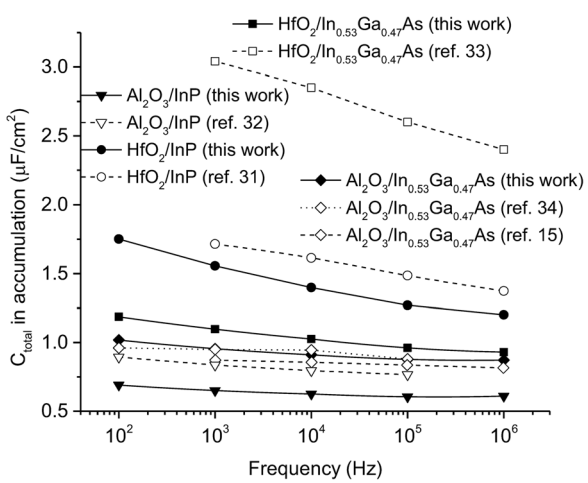

FIG. 5. Experimental capacitance versus frequency data for $HfO_2/In_{0.53}Ga_{0.47}As$, $Al_2O_3/In_{0.53}Ga_{0.47}As$, HfO_2/InP, and Al_2O_3/InP comparing this work to state-of-the-art results in the literature.[15,31–34]

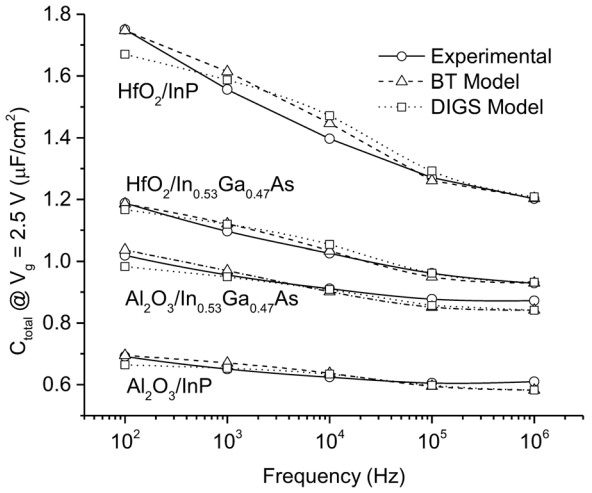

FIG. 6. Fit of the Border Trap and Disorder Induced Gap State model to experimental capacitance versus frequency data for $HfO_2/In_{0.53}Ga_{0.47}As$, $Al_2O_3/In_{0.53}Ga_{0.47}As$, HfO_2/InP, and Al_2O_3/InP. The parameters used to fit the data and other extracted parameters are shown in Table I.

was found to range from 1×10^{20} $cm^{-3}eV^{-1}$ to 8×10^{20} $cm^{-3}eV^{-1}$ which is consistent with previous experimental reports for similarly processed devices.[1,6,10,12,15–18,36] κ was found to be approximately $5 \times 10^7\,cm^{-1}$ which, using Eq. (3), is consistent with a conduction band offset of ~2.5 eV and effective mass of $\sim 0.4\,m_e$ (m_e is the free electron mass). This value of κ is consistent with previous work.[5–7,15,16] All of these devices are observed to exhibit flattening of the C_{total} versus f curve for frequencies between 100 kHz to 1 MHz. As noted in Sec. II, this behavior can only be fit by choosing τ_0 such that $\omega\tau_0 \rightarrow \sim 1$ in this frequency range. The τ_0 values used to fit the experimental data ranged from 5 μs to 8 μs. The values of τ_0 and κ found through the fitting imply a tunneling distance at 100 Hz calculated using Eq. (4) of 0.4 nm to 0.8 nm, consistent with typical bonding distances of a disrupted interface and strongly suggesting that these defects are from the disruption of the III-V bonding and not related to bonds within the bulk high-k dielectric.

Given the importance of τ_0 in determining the tunneling distance, additional discussion is warranted. The τ_0 calculated using Eq. (2) for $In_{0.53}Ga_{0.47}As$ in accumulation and assuming a capture cross-section, σ, of $10^{-16}\,cm^2$ is approximately 10^{-11} s. To obtain τ_0 in the range of 1 μs to 10 μs requires a very small capture cross-section ($\sim 10^{-20}\,cm^2$). However, τ_0 measured near the conduction band edge using the frequency associated with the peak in measured interface state conductance has been independently shown to be within the range of 1 μs to 10 μs, consistent with the modeling results.[7,36] Furthermore, several researchers have reported very small electron capture cross-sections for energies in the valence or conduction band of Si,[37] GaAs,[38,39] and GaP (Ref. 38) using deep level transient spectroscopy (DLTS). The capture cross-section was shown to decrease exponentially towards the conduction band edge (E_c)[37,38]

$$\sigma(E_t) = \sigma_0 \exp(E_c - E_t), \tag{10}$$

where E_t is the trap energy level and σ_0 is a constant inherent to the trap level. Capture cross-sections for electrons deep inside the conduction band predicted by Eq. (10) are very small and consistent with our results. Since several independent measures of τ_0 and σ are consistent with the results of the fitting of the C_{total} versus f behavior, we believe that τ_0 in the range of 1 μs to 10 μs is correct for the $In_{0.53}Ga_{0.47}As$ and InP MIS devices.

While better fits could be obtained by slightly adjusting parameters for each model individually, the fact that both models can reasonably fit the experimental data using the same parameters shows that similar conclusions can be drawn using either model. However, in order to make the modeling tractable, both of these models involve numerous approximations. In both models, a constant trap density and a constant capture cross-section inherent to the trap level as a function of position into the defective interfacial region or insulator is assumed. The variation of bonding detected from the crystalline semiconductor into the bulk of the oxide suggests that this is likely not the case (see below). The trap density and capture cross-section could be changed as a function of position to better fit the data. Neither model accounts for variation of the surface potential across the surface of the semiconductor due to the spatial distribution of charged states in the insulator. It is well known that this surface potential variation causes a distribution of effective trap time constants across the surface of the semiconductor which, when integrated, can linearize the defect capacitance response as a function of frequency.[5,23] This would especially be true for the case of insulators on III-V substrates which typically exhibit a large charged defect density. Finally, both of these models assume elastic tunneling of the free carriers to the defects in the defective interfacial region or insulator. Especially given the large defect densities present, this transport process may not be valid and could affect the details of the modeled behavior.

Given the approximations in both of these models and given the fact that the detailed C_{total} versus f behavior can be fit with a variety of non-unique solutions, it is expedient to draw only general conclusions from such fits. Therefore, we conclude that frequency dispersion for $In_{0.53}Ga_{0.47}As$ and InP MIS devices is caused by a large defect density within

TABLE I. Parameters used to fit the experimental data and other extracted parameters obtained using both the BT model and DIGS model. For a given set of experimental data, the same parameters were used by both models to fit the experimental data.

Parameter	HfO_2/InGaAs	Al_2O_3/InGaAs	HfO_2/InP	Al_2O_3/InP
t_{ox} (nm)	12.0	4.8	8.0	8.5
N_t ($cm^{-2}eV^{-1}$)	3.5×10^{20}	1.3×10^{20}	3.0×10^{20}	7.0×10^{20}
$\varepsilon_{ox}/\varepsilon_0$	20	7	20	7
κ (cm^{-1})	6.0×10^7	4.0×10^7	4.0×10^7	5.0×10^7
τ_0 (μs)	8.0	8.0	5.0	8.0
C_{semi} ($\mu F/cm^2$)	2.60	2.40	2.60	3.20
C_{ox} ($\mu F/cm^2$)	1.48	1.35	2.21	0.74
C_{min} ($\mu F/cm^2$)	0.94	0.87	1.20	0.60
x_{tun} at 100 Hz (nm)	0.44	0.66	0.72	0.54

~0.8 nm (at 100 Hz) of the crystalline substrate. The remainder of the paper will focus on determining whether these defects are due primarily to states associated with the bulk of the dielectric (BTs associated with the bonding and structure of the Al_2O_3 or HfO_2) or due to DIGS caused by the dielectric deposition and associated oxidation of the semiconductor (InP or $In_{0.53}Ga_{0.47}As$). This difference is technologically important because it determines whether one should primarily focus on reducing defects within the dielectric by engineering the dielectric itself or by controlling oxidation-induced disruption of the crystalline semiconductor arising from dielectric deposition.

IV. EXPERIMENTAL EVIDENCE FOR DIGS

While obtaining unique parameters by fitting of the details of the shape and magnitude of the C_{total} versus f behavior is difficult due to the number of parameters which can be used, it is possible to obtain a relative measure of the total interfacial defect density (D_{it} ($cm^{-2}eV^{-1}$)) as a function of energy in the band gap from the high-low frequency method, the details of which are presented elsewhere.[17,18,40] In summary, low temperature (77 K) C-V curves at high frequency (1 MHz) are used to obtain a response that is relatively free from defects and associated dispersion. Room temperature C-V at low measurement frequency (e.g., 100 Hz) is used to obtain a response which contains all defects within the interfacial region associated with the long time constant at this low frequency (e.g., $(2\pi \times 100)^{-1}$ s). To use this technique across the entire bandgap requires that no inversion response is present in the experimental C-V curves. However, inversion charge does not affect the extracted D_{it} measured in accumulation which is the main focus of this study.

Using this methodology, the D_{it} was calculated for the four different samples as shown in Fig. 7. It is observed that Al_2O_3 on $In_{0.53}Ga_{0.47}As$ has a lower D_{it} as compared to HfO_2 on $In_{0.53}Ga_{0.47}As$, as previously reported by others in the literature.[41] Conversely, the D_{it} for Al_2O_3 on InP is higher than HfO_2 on InP. For this work, the surface treatment, annealing conditions and deposition temperatures are consistent, independent of the dielectric/substrate used. This helps to ensure that the quality of the bulk of the dielectric is similar independent of the substrate. Fig. 5 showed that the level of accumulation dispersion for our work on a given dielectric/substrate is consistent with that of the literature even though processing conditions for the work in the literature may be different. This indicates that the trends we observe are consistent with the literature. We are unaware of evidence that the bonding in the bulk of the Al_2O_3 or HfO_2, well away from the crystalline semiconductor, is different when deposited on InP as compared to $In_{0.53}Ga_{0.47}As$, particularly under atomic layer deposition conditions. Therefore, these results suggest that defects associated only with the dielectrics themselves, as assumed in the BT model, are not responsible for the anomalous frequency dispersion observed in the experimental C-V data.

Physical characterization of the interface by XPS provides further, complementary information about the chemical origin of the defects which can lead to the trap response observed in the C-V data. Figures 8(a) and 8(b) shows the Ga 2*p* core level spectra for HfO_2 and Al_2O_3 on n-$In_{0.53}Ga_{0.47}As$ substrates. All peaks were fit using a Shirley background and a Voigt lineshape for the individual peaks, with independent control over the width of the Gaussian and Lorentzian components of the Voigt lineshape. These XPS spectra show detection of Ga_2O and Ga_2O_3 states with binding energy separations of 0.55 eV and 1.2 eV from the bulk peak associated with Ga bonding in InGaAs.[2] XPS spectra indicate that ALD of HfO_2 on $In_{0.53}Ga_{0.47}As$ substrates results in more oxidation of the substrate as compared to that from ALD of Al_2O_3. Of particular note are the concentrations of Ga_2O_3-like bonding[2,4] and the resulting As-As bonding at the interface which correlate with degraded device performance[42] and are predicted by first principles calculations to produce defect levels in the band gap.[35,43–48] It has been shown that deposition of an amorphous-Si interlayer

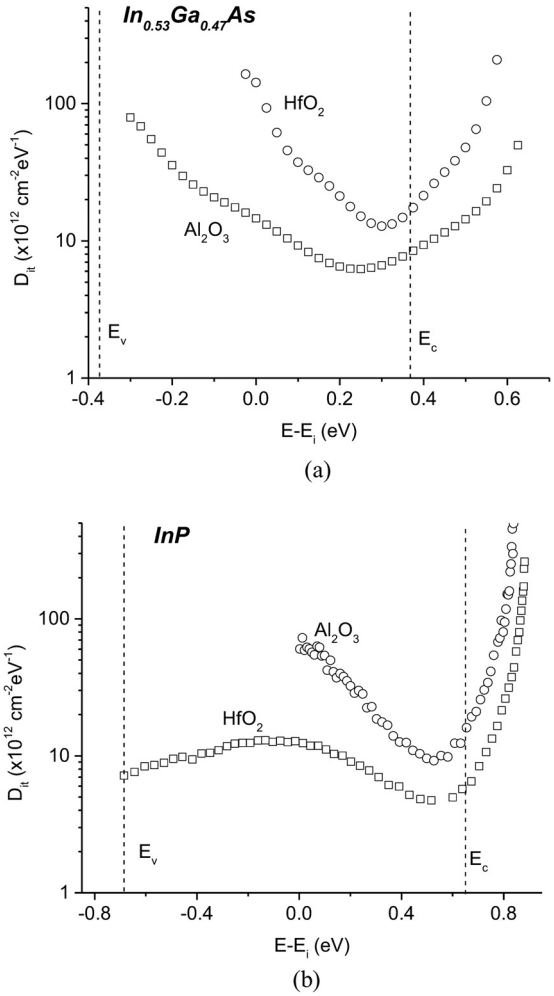

FIG. 7. Extracted D_{it} for $In_{0.53}Ga_{0.47}As$ and InP devices using the high-low frequency method.[17,18] Al_2O_3 on $In_{0.53}Ga_{0.47}As$ has lower D_{it} compared to HfO_2 on $In_{0.53}Ga_{0.47}As$. However, the D_{it} for Al_2O_3 on InP is higher than that of HfO_2 on InP. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **102**(13), 132903 (2013). Copyright 2013 AIP Publishing LLC. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **99**(17), 172901 (2011). Copyright 2011 AIP Publishing LLC.

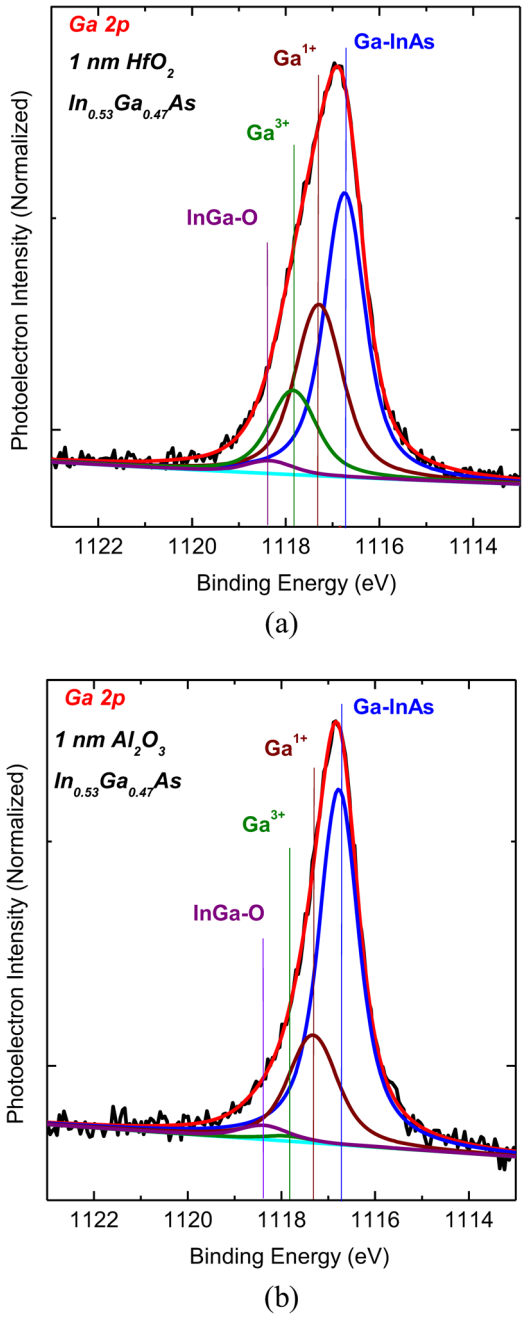

FIG. 8. XPS data of the Ga 2*p* core level for (a) HfO_2 and (b) Al_2O_3 on $In_{0.53}Ga_{0.47}As$. The 3+ oxidation state of Ga is indicative of high defect density. ALD of HfO_2 on $In_{0.53}Ga_{0.47}As$ substrates results in higher oxidation of the substrate.

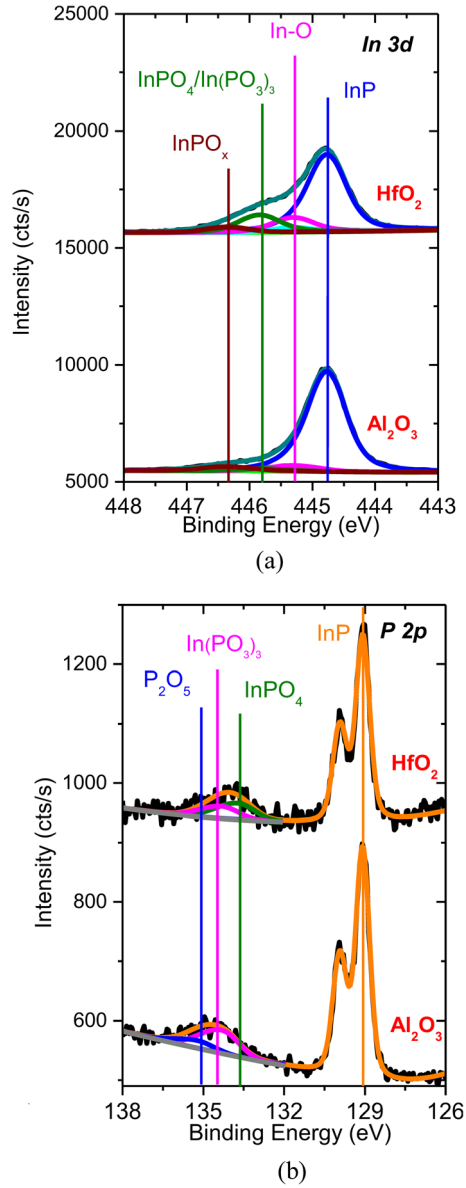

FIG. 9. XPS of the (a) In 3*d* and (b) P 2*p* core level spectra Al_2O_3/n-InP and HfO_2/n-InP interface showing an increase in native oxides with annealing.[17,18] Binding energies of the In-P oxides at Al_2O_3/InP suggests that these are more phosphorus rich when compared to In-P oxides at HfO_2/InP interface. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **102**(13), 132903 (2013). Copyright 2013 AIP Publishing LLC. Reprinted with permission from R. V. Galatage, H. Dong, D. M. Zhernokletov, B. Brennan, C. L. Hinkle, R. M. Wallace, and E. M. Vogel, Appl. Phys. Lett. **99**(17), 172901 (2011). Copyright 2011 AIP Publishing LLC.

results in the reduction of the Ga_2O_3 oxide states and devices with this a-Si interlayer does not result in frequency dispersion of accumulation capacitance.[2,42] One could argue that reduction of the frequency dispersion is due to moving of defective high-k oxide away from the substrate. However, previous work has shown that removal of the frequency dispersion is not possible by simply depositing the a-Si interlayer but control over the oxidation of the substrate is also necessary.[4] Figure 9 shows the In 3*d* and P 2*p* core level spectra of InP following the ALD deposition of Al_2O_3 and HfO_2. ALD of Al_2O_3 results in the formation of the more phosphorous rich native oxides than ALD HfO_2. Increased D_{it} levels in the case of Al_2O_3 have previously been correlated with increased levels of these phosphorus rich native oxides.[18]

These experimental findings as well as our previous studies[2–4,17,18,34,35,42,44–46,49–53] strongly suggest that the bonds associated with disorder-induced oxidation of the III-V substrate are primarily responsible for the defects (DIGS) causing the measured capacitance frequency dispersion in accumulation. There have also been experimental studies by others suggesting the presence of a thin disordered region near the crystalline semiconductor. Minimization of air exposure and associated oxidation of the substrate has been

observed to improve accumulation dispersion.[34] Internal photoemission of Al_2O_3 and HfO_2 on $In_{0.53}Ga_{0.47}As$ has shown two thresholds (barrier heights) at the interface: one associated with a lower bandgap oxide interlayer, and one associated with the bulk of the oxide.[54] ESR measurements have shown evidence of paramagnetic defect sites associated with oxidation of the interface where the authors conclude that oxidation of the III-V substrate must be avoided to reduce interfacial defects.[55] EELS measurements of Al_2O_3 on GaAs consistently shows the presence of an interfacial layer containing Ga, As, O, and Al.[56] Finally, theoretical studies show that oxygen atoms can attack the back-bonds of GaAs resulting in generated interfacial defects.[35,42–48,57–60]

V. CONCLUSIONS

In conclusion, while there are differences in the details of the fits of the BT and DIGS models to experimental capacitance frequency dispersion of HfO_2 and Al_2O_3 on InP and $In_{0.53}Ga_{0.47}As$ substrates, both models lead to the same general conclusion: frequency dispersion is caused by a large defect density within ~0.8 nm (at 100 Hz) from the crystalline semiconductor surface. The high-low frequency method suggests that the conduction band D_{it} for HfO_2 is higher than Al_2O_3 for $In_{0.53}Ga_{0.47}As$ substrates but is lower for InP. III-V chemical states measured using XPS (e.g., Ga_2O_3 and P-rich native oxides) correlates well to this trend in D_{it}. These observations, our modeling of the C-V behavior, as well as additional complementary experimental and theoretical evidence in the literature supports the conclusion that the observed experimental capacitance frequency dispersion in accumulation is due primarily to disorder induced gap states and not border traps located within the bulk of the dielectric.

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