DESIGN TECHNIQUES FOR VOLUME-EFFICIENT SOFT-SWITCHED POWER CONVERTERS WITH ENHANCED POWER EFFICIENCY AND RELIABILITY

by

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Dedicated to my family

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Zero voltage switching technique has been popular in high voltage DC-DC converter design to increase the switching frequency while maintaining high power efficiency and thus reducing the volume of passive components. Recently, enhancement-mode GaN FETs attracts more and more attention in high voltage converters for better figure of merits in $R_{DSON}$ and $Q_G$ compared with the traditional MOSFETs. Although GaN FETs have been used in soft-switched DC-DC converters to further improve the power efficiency and power density, GaN FETs can cause more power loss in the third quadrant conduction than traditional MOSFETs if the dead time is not precisely controlled. In addition, fast transition of GaN FETs requires the high-voltage level shifter handle much faster dv/dt without creating logic errors. This dissertation develops a novel GaN driver with adaptive dead time control scheme, based on an innovative methodology of slope-sensing ZVS detection to minimize the third quadrant conduction time of GaN FETs. Also, a differential-mode noise blanking scheme is proposed to increase the dv/dt noise immunity of the high voltage level shifter. The proposed GaN driver can help to reduce power loss by 1.6W

and achieve 90.2% power efficiency at 150V input and 2MHz frequency, or 88.6% power efficiency at 400V input and 1MHz frequency.

Traditional non-isolated ZVS converters utilize an auxiliary branch to assist soft-switching operation of the active FET. In multiphase topologies or non-inverting buck-boost topology, each active power FET requires an auxiliary branch such that the total number and volume of auxiliary components make the traditional ZVS scheme infeasible. This dissertation proposes a new passive-saving technique to share one auxiliary branch between two active FETs such that the total number and volume of auxiliary components can be reduced by 50%. It is worth to notice that the proposed passive-saving technique can be applied to both ZVS and ZVT topologies.

Traditional ZVT converters adopted fixed on-time of the auxiliary switch for simplicity. Since the auxiliary current ripple cannot scale with the load current, power efficiency at light load condition is quite limited. This dissertation proposes a monolithic control loop to regulate the auxiliary current ripple according to load current. Compared with the traditional ZVT converters, the proposed converter with auxiliary current control scheme can improve light load efficiency by 14.5% without folding back switching frequency.

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# CHAPTER 1

# INTRODUCTION

## 1.1 Introduction of DC-DC Converters

DC-DC converters are widely used where a regulated DC voltage is created from an unregulated DC voltage for different applications. Generally, there are three main topologies of DC-DC converters, namely linear regulators, switched-capacitor DC-DC converters, and inductor-based switched-mode DC-DC converters.

A linear regulator, which is also known as a low-dropout regulator (LDO), is the one with the simplest structure as shown in Figure 1.1. It consists of an error amplifier $A_1$, a voltage reference, a power FET $M_P$, an output capacitor $C_O$, and a loading resistor $R_L$. Resistors $R_{FT}$ and $R_{FB}$ feed the scaled-down output voltage $V_{OUT}$ to the non-inverting input of $A_1$. With negative feedback in the LDO, $V_{OUT}$ is regulated as

$$V_{OUT} = (1 + \frac{R_{FT}}{R_{FB}}) \times V_{REF} \tag{1.1}$$

Neglecting the quiescent current in the error amplifier and the feedback resistors, the power efficiency of the LDO is given as

$$\eta_{LDO} = \frac{V_{OUT} I_L}{V_{IN} I_{IN}} \approx \frac{V_{OUT}}{V_{IN}} \tag{1.2}$$

It should be noted that the output voltage can only be smaller than the input voltage and its efficiency highly depends on the output-to-input ratio. When the difference between $V_{OUT}$ and $V_{IN}$ increases, the power efficiency drops.

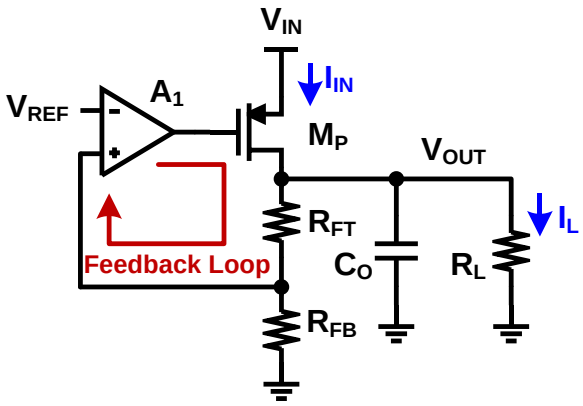



Figure 1.1. Schematic of a low-dropout regulator.

A switched-capacitor converter uses capacitors to store and transfer energy to achieve a desired $V_{OUT}$ which can be higher or lower than $V_{IN}$. Figure 1.2 shows an example of 3-to-1 switched capacitor converter in ladder topology. A switched-capacitor converter is often the best choice for applications requiring some combination of low power, simplicity and low cost. The power efficiency of a switched-capacitor converter is typically higher than a linear regulator but lower than an inductor-based switched-mode converter. Note that if different conversion ratios between $V_{OUT}$ and $V_{IN}$ are desired, different arrangements of power FETs and capacitors are needed, thereby resulting in the discontinuous voltage conversion. Since the switched-capacitor converter does not have a close-loop regulation by its nature, the output regulation is very poor for this type of converters. Therefore, if an accurate regulation and continuous conversion ratio are desired, an LDO is commonly used as a downstream regulator for switched-capacitor converters.

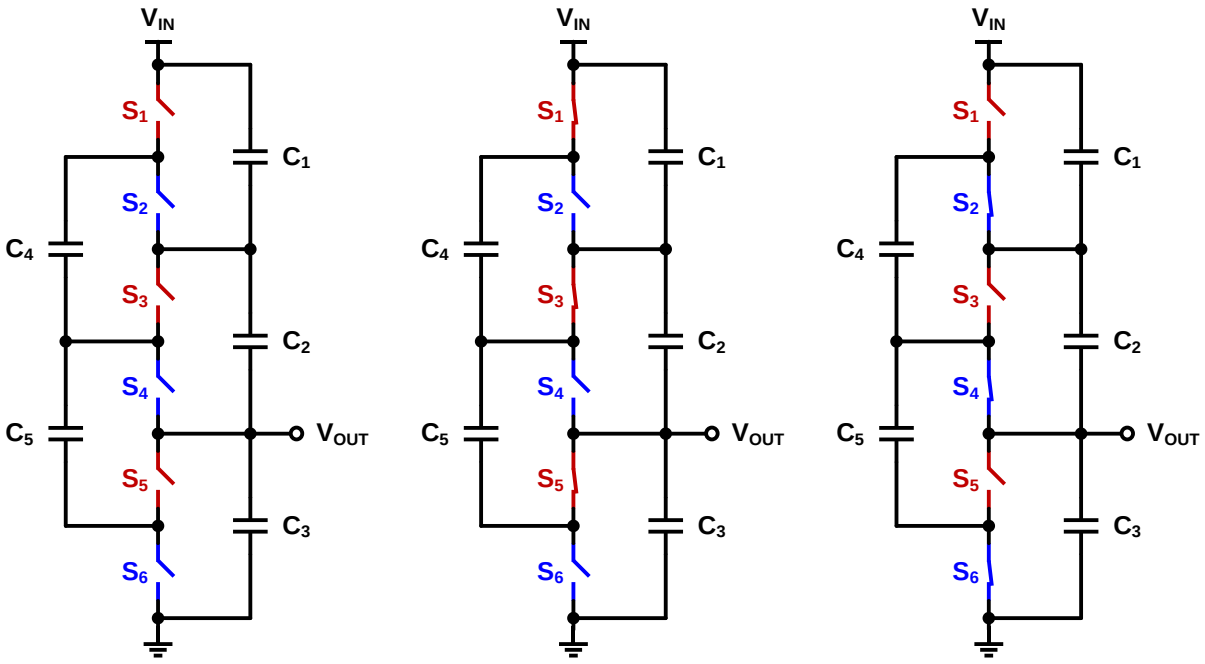



Figure 1.2. (a) A switched capacitor converter in 3-to-1 ladder topology, including networks in (b) phase 1 and (c) phase 2.

Inductor-based switched-mode DC-DC converters have found wide applications due to the continuous conversion ratio and high power efficiency. Both inductor and capacitor are used as energy storage and transfer elements in the converter. Since energy transfer between an ideal inductor and an ideal capacitor is a lossless process, the theoretical power efficiency of switched-mode DC-DC converters can reach 100%. Figure 1.3 shows the schematic of a buck converter, which is a typical example of the inductor-based switched-mode DC-DC converters. $V_{OUT}$ is given as

$$V_{OUT} = D \times V_{IN} \tag{1.3}$$

where D represents the duty cycle of high-side switch $M_H$ and the value is between 0 and 1. Based on equation (1.3), $V_{OUT}$ can be designed to any value by changing D continuously. Due to the advantages of high efficiency, high power density and continuous output-to-input conversion ratio, the switched-mode converter has gain more and more popularity compared with the other two counterparts. Therefore, all the research work presented in this dissertation is based on switched-mode DC-DC converters.

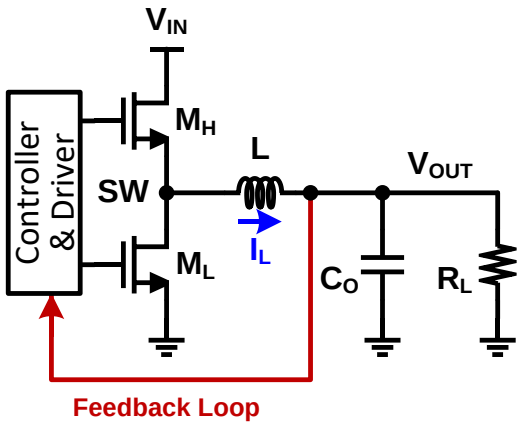



Figure 1.3. Schematic of a buck converter.

## 1.2 Overview of Soft Switched DC-DC Power Converters

Increasing the switching frequency of DC-DC converters is demanded by industry in order to reduce the system cost, weight and volume, as the required values and thus the sizes of passive components in power converters running at higher frequencies can be smaller. For automotive applications, power converters would typically need to support an input voltage up to 40 – 100 V and deliver an output power of 100s of Watts; whereas industrial and telecom systems may experience fluctuations of the input voltage from 150 V to 400 V [1].The switching power loss, which occurs at the switching node of the converter, dominates the total converter power loss

and significantly degrades the power efficiency of these high-voltage converters if they operate in hard-switching mode with a high switching frequency. Therefore, state-of-the-art hard-switching synchronous and asynchronous high-voltage converters operate at switching frequencies of 100 – 300 kHz [2] – [4] in order to limit the converter switching power loss. For low cost and small converter size, it is thus important to develop an effective technique to enable high-voltage power converters to obtain high power efficiency at high switching frequencies by reducing the switching power loss.

To minimize the converter switching loss, quasi-resonant based soft switching was first reported to use auxiliary LC resonant elements to shape the switching device's voltage waveform in order to establish zero-voltage switching (ZVS) of all power devices [5], [6]. However, as shown in Figure 1.3, this technique increases the voltage stress of the power diode D and the current stress on power switch $M_H$. When power devices with a higher voltage rating are used to handle the increased voltage stress during this quasi-resonant operation, larger parasitic capacitance limits the switching frequency and higher on-resistance increases the conduction power loss of the converter. The quasi-square-wave (QSW) scheme was proposed to discharge the voltage across the power devices during the dead time without increasing the voltage stress [7], [8]. However, as shown in Figure 1.4, since the peak current of the auxiliary inductor needs to be larger than the average inductor current to establish the ZVS condition, large current ripple of the auxiliary inductor is resulted in high load-current conditions. The core loss of the auxiliary inductor would thus be increased significantly to degrade the converter power efficiency in high switching-frequency and load-current conditions. In order to reduce the power loss caused by the current ripple in QSW-ZVS converters, the zero-voltage-transition (ZVT) technique has been

reported to control the transient current for ensuring ZVS occurs only in the vicinity of transition intervals by an auxiliary power switch [9], [10]. Since the auxiliary inductor current is in discontinuous conduction mode and its RMS value is much smaller than the traditional ZVS converters, the associated conduction loss in the auxiliary branch is much reduced in ZVT converters. Schematic and waveforms of a conventional ZVT buck converter is shown in Figure 1.6.

For the isolated DC-DC converters, since the primary-side current $I_{LR}$ is alternating by nature ZVS of all FETs can be achieved on the primary side [11] as shown in Figure 1.7. This dissertation presents new system and circuit design for non-isolated QSW ZVS converters, ZVT converters and isolated QSW ZVS converters.

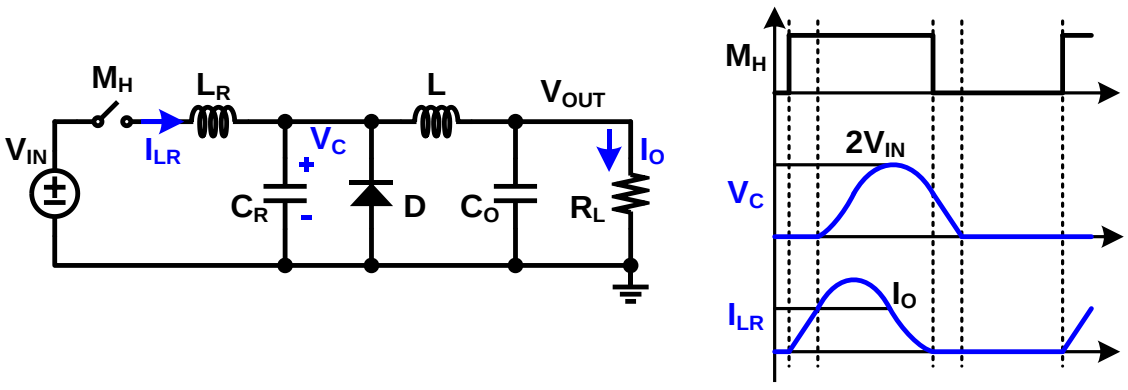



Figure 1.4. Schematic and waveforms of a conventional quasi-resonant buck converter.

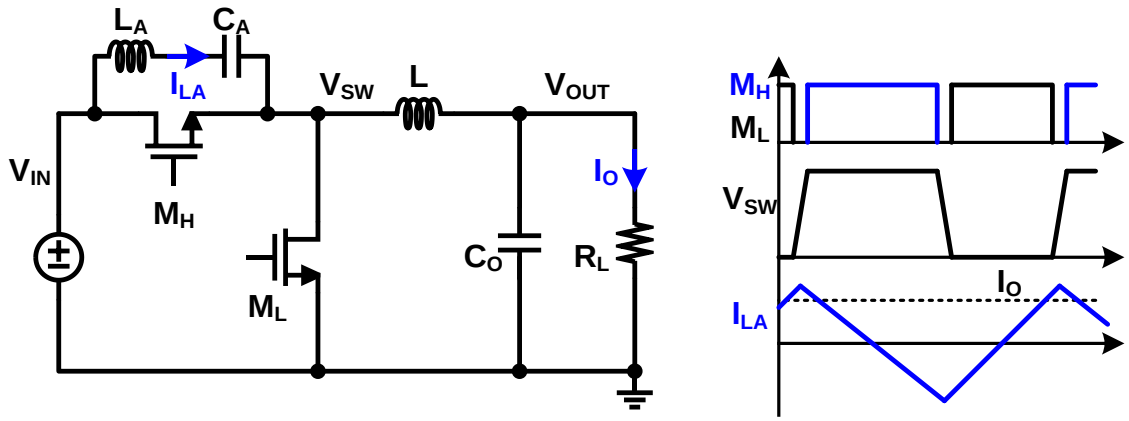



Figure 1.5. Schematic and waveforms of a conventional quasi-square-wave buck converter.

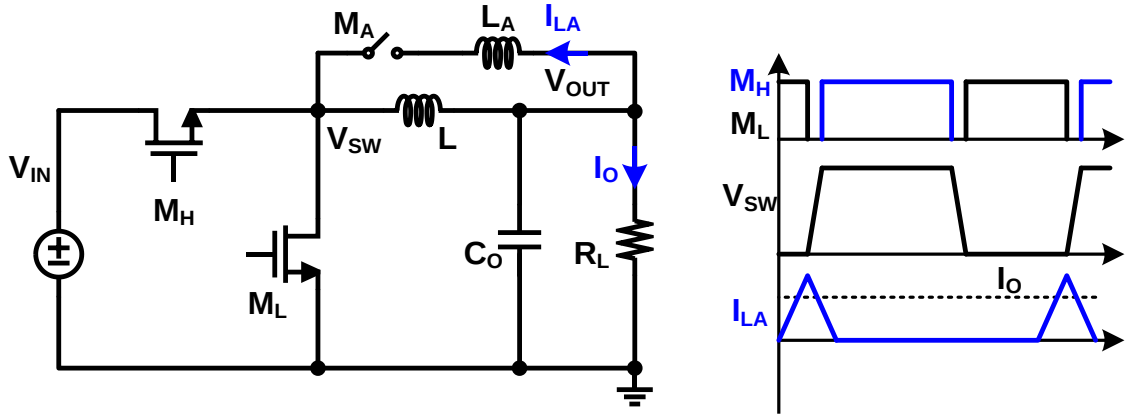



Figure 1.6. Schematic and waveforms of a conventional zero-voltage-switched buck converter.

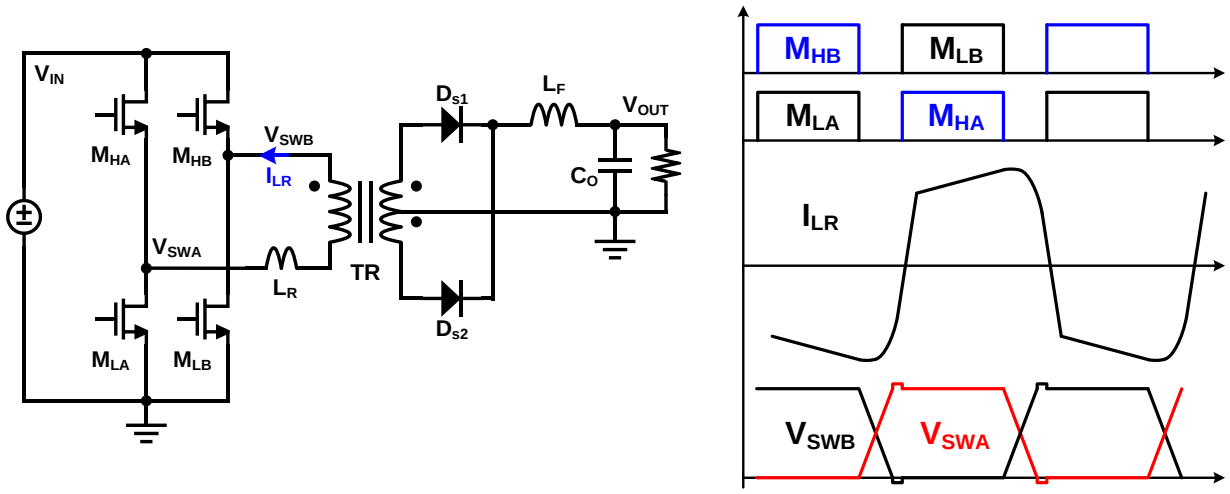



Figure 1.7. Schematic and waveforms of an isolated full-bridge ZVS converter.

## 1.3 Overview of Gallium Nitride FETs

With increasing popularity among power electronics engineers, enhancement-mode gallium nitride (GaN) transistors behave very similarly to Silicon power MOSFETs. A positive bias on the gate relative to the source causes a field effect which attracts electrons that complete a bidirectional channel between the drain and the source. Since the electrons are pooled, as opposed to being loosely trapped in a lattice, the resistance of this channel is quite low. When the bias is removed from the gate, the electrons under it are dispersed into the GaN, recreating the depletion region and giving it the capability to block voltage [12].

However, there are important differences, in addition to the obvious semiconductor material and process differences. First, GaN's top-tier specification of on-resistance $R_{DS(ON)}$ is very low, thus reducing a major source of static losses and inefficiency when in the on state. Also, the structure of the GaN FET results in a device with very low input capacitance, which enables faster on/off switching. A detailed FoM ($Q_G$ vs $R_{DS}$) comparison between GaN FETs and

traditional Si MOSFET provided by EPC [13] is shown in Figure 1.8. With the improved FoM, a GaN device can switch hundreds of volts in nanoseconds, supporting the design of power supplies that can switch large currents at rates of several megahertz. This improvement potentially means higher efficiency and allows use of smaller magnetics and passive components [14].

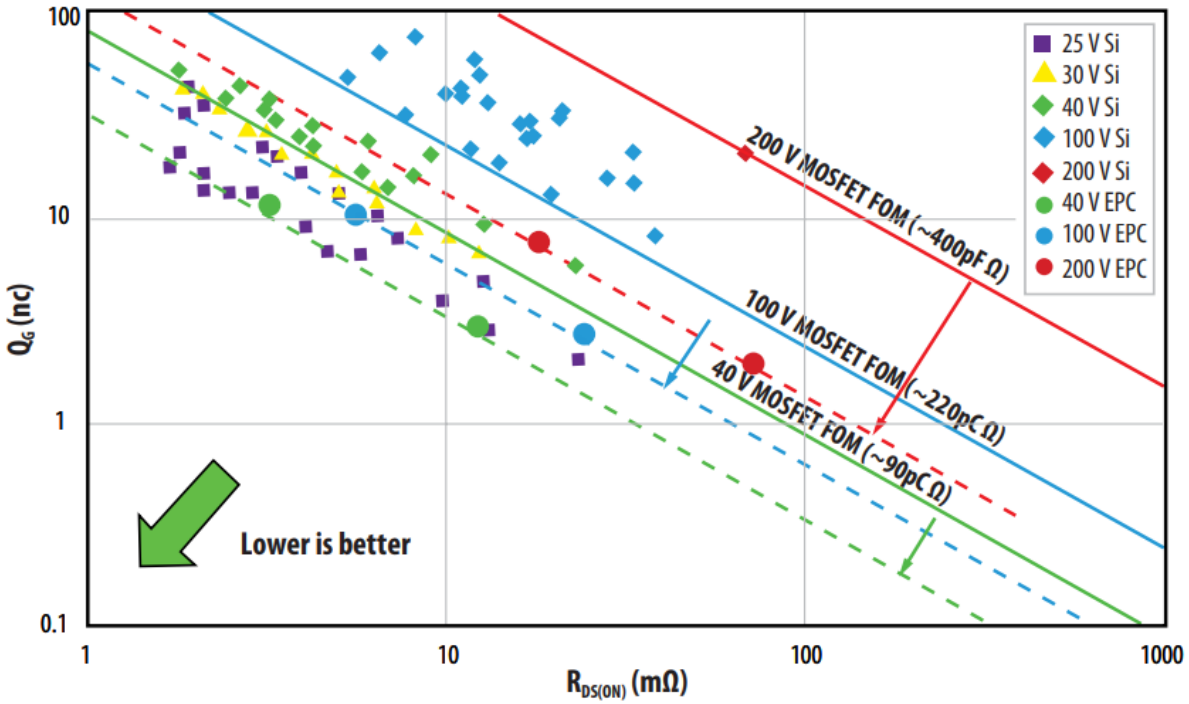



Figure 1.8. FoM comparison between GaN FETs and Si MOSFETs provided by EPC.

## 1.4 Research Motivation

Although QSW-ZVS technique and ZVT technique has been around in the power electronics society for decades, most of the research progress is mainly focused on the power stage development in the printed circuit board (PCB) level. Very limited research effort has been made on monolithic design (i.e. driver and controller improvement) dedicated to the soft-switched

converters. In addition, the unique property of GaN FETs place special requirements on the driver especially for soft switch operations. The motivation of this dissertation is to develop the monolithic circuit design for control and driver of soft-switched converters with both GaN FETs and traditional MOSFETs, as well as novel optimization in the power stage architecture.

# CHAPTER 2

# BACKGROUND REVIEW

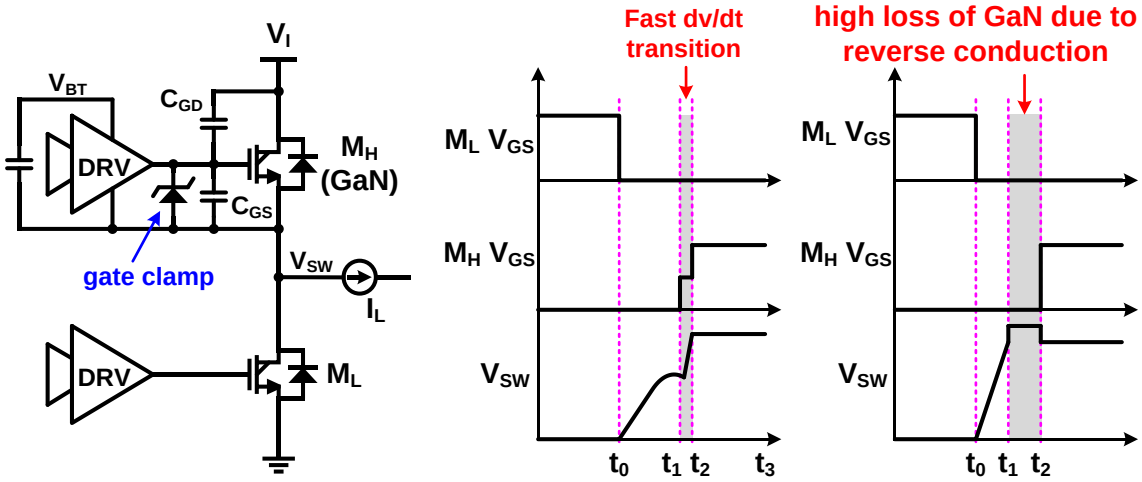
## 2.1 Design Challenge for GaN Drivers in ZVS Operation

GaN FETs have some unique characteristics that require special caution in the driver design. First of all, since GaN FETs has much smaller input capacitance ($C_{GS}$) and miller capacitance ($C_{GD}$) compared with MOSFETs with similar voltage and current ratings, the switch node (SW) of a GaN converter experiences much faster dv/dt transition than the switch node of a MOSFET converter does. The fast transition could cause logic failure in the level shifter as shown in the next section. Although ZVS operation helps to slow down the SW transition by nature, a soft-switched converter still has to operate in hard switching condition or at least partial ZVS condition during startup and line/load transitions [15] as shown in Figure 2.1. Therefore, the GaN driver for soft-switched converter still has to be able to handle fast dv/dt transition.

Secondly, the GaN FET does not have so called "body diode" as of the MOSFET due to the difference in material and structure. However, the GaN FET can still conduct current from source to drain with gate voltage equal to its source voltage (reverse conduction) because of the minority channel formed at the drain [16, 17]. Since this reverse conduction behavior is very similar to the body diode conduction of the MOSFET, a diode symbol is illustrated between source and drain terminals in the GaN FET symbol in Figure 2.1 for simplicity. Typically, the source to drain voltage of the GaN FET is 2 – 3 V in order to turn on the reverse conduction channel, and this voltage drop increases with the increased reverse current. Therefore, if there is excessive dead time after ZVS is finished as shown in Figure 2.1 (c), the reverse conduction loss of the GaN FET is at least 3x larger than the body diode conduction loss of the MOSFET, which

requires accurate and adaptive dead time control to realize high efficiency ZVS operation with GaN FETs [15, 18].

Finally, Table 2.1 compares the threshold voltage ($V_{TH}$) and absolute maximum rating of gate-source voltage ($V_{GS}$) between multiple GaN FETs (i.e. EPC2007C [19] and GS61004B [20]) and a typical MOSFET (NTMFS6H858NL [21]) with similar voltage and current ratings. Although GaN FETs have similar $V_{TH}$ as the MOSFET, the absolute $V_{GS}$ rating of GaN FETs is smaller than that of the MOSFET which can cause GaN FETs not in safe operating area (SOA). For example, $V_{TH}$ of EPC2007C is around 0.8 – 2.5V, so that at least 3.5 – 4.5V of $V_{GS}$ is needed to fully turn on this GaN FET. With the maximum $V_{GS}$ being 6V, there is only around 1.5V margin for $V_{GS}$ ringing. A Zener diode can be used to clamp the gate voltage within safe region with extra transition delay [22, 23] as shown in Figure 2.1 (a). On the other hand, GS61004B has wider range of $V_{GS}$ transient rating, and thus does not require the gate clamping diode.




(a) (b) (c)

Figure 2.1. (a) Schematic showing design challenges of GaN drivers; (b) waveform of partial ZVS operation and (c) waveform of full ZVS operation.

Table 2.1. Comparison of threshold voltage ($V_{TH}$) and gate-source voltage ($V_{GS}$) between GaN FETs and MOSFETs

| | GaN FETs | | MOSFETs |
|---|---|---|---|
| | EPC2007C [19] | GS61004B [20] | NTMFS6H858NL [21] |
| $V_{TH}$ | 0.8V – 2.5V | 1.1V – 2.6V | 1.2 – 2.0V |
| Max $V_{GS}$ | -4V – 6V | -10V – 7V | ±20V |
| Max $V_{GS}$ transient | -4V – 6V | -20V – 10V | N.A. |

## 2.2 Design Challenge for HV Level Shifting Circuits

Figure 2.2 demonstrates the failure root cause of the traditional HV level shifter during very fast transitions of $V_{SW}$ and $V_{BT}$ [18, 24, 25]. As mentioned in the section 2.1, a fast transition of $V_{BT}$ is still a valid concern for soft-switched converters in case full ZVS operation is not achieved (i.e. partial ZVS or hard switching operations during line/load transients and startup). The capacitors highlighted in red in Figure 2.2 are the parasitic capacitor of HV transistors $M_{N1}$ and $M_{N2}$. During fast transition, the displacement current caused by the parasitic capacitors can pull both outputs of HV level shifter (i.e. $V_1$ and $V_2$) to logic low. Due to the mismatch between $M_{N1}$ and $M_{N2}$ and the mismatch between $M_{P1}$ and $M_{P2}$, the negative magnitude of $V_1$ can be larger (or smaller) than that of $V_2$, and the falling (and rising) edge of $V_1$ can also be sooner (or later) than that of $V_2$, resulting in uncertain output of SR latch ($V_O$) and unexpected turn-on or turn-off of $M_H$ eventually. As a result, a more robust HV level shifter is needed to handle very fast transition reliably. [24] proposed to insert a damping resistor at $V_1$ and $V_2$ to slow down the dv/dt at these two nodes to improve noise immunity; [25] proposed to apply a dynamic current

source between $V_{BT}$ and $V_1$ ($V_2$) to prevent both $V_1$ and $V_2$ pulled low during dv/dt transition. Both methods are proved effective in improving noise immunity, but also increase the propagation delay of the HV level shifter and hence increase the mismatch of propagation delay between high side and low side.

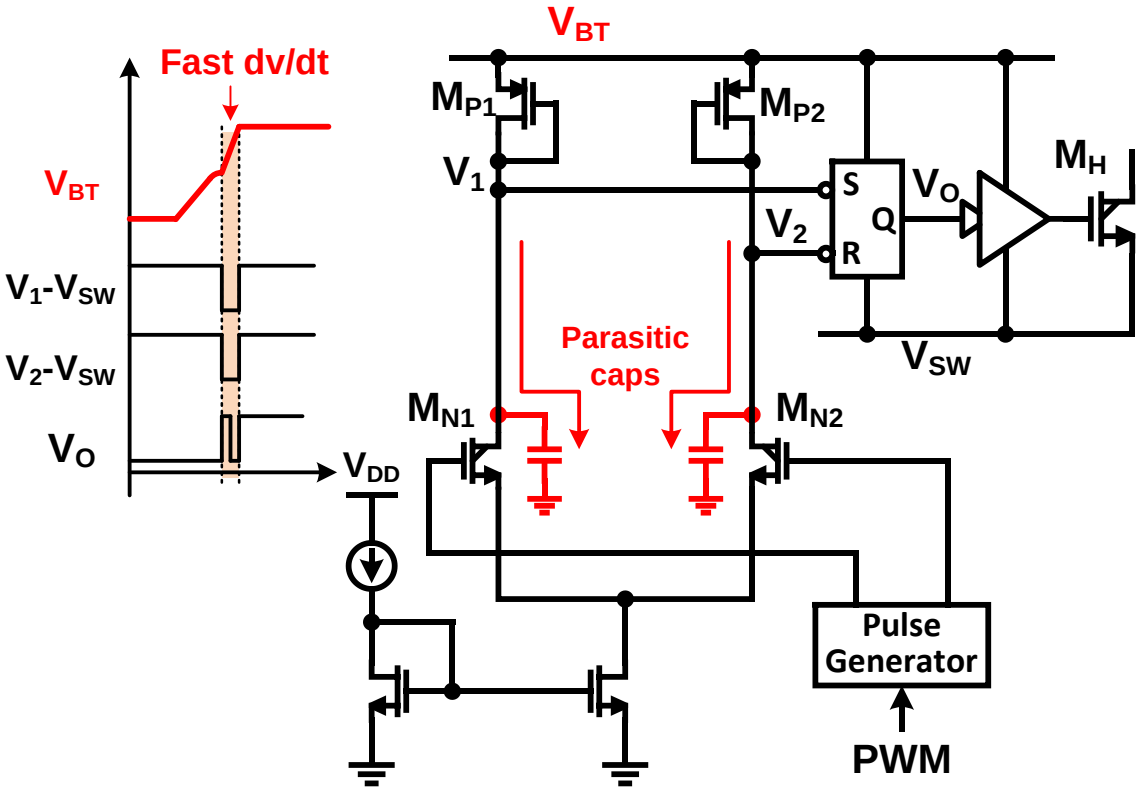



Figure 2.2. Design challenge of the HV level shifter during fast transition.

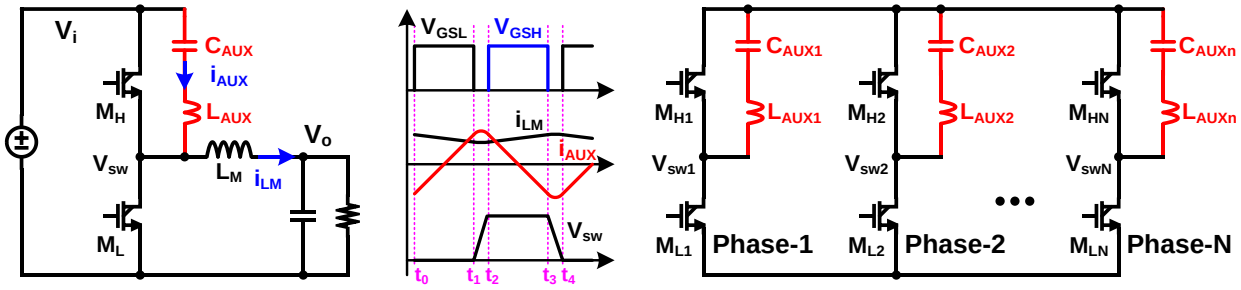
## 2.3 Design Consideration of Auxiliary Components in Soft-Switched Converters

Figures 2.3 (a) and (b) shows the schematic and waveforms of a traditional QSW-ZVS buck converter [7]. The auxiliary branch is connected between $V_i$ and $V_{SW}$ to create an alternating current $i_{AUX}$ assisting ZVS operation of $M_H$. During the on time of $M_L$ ($t_0 - t_1$), $i_{AUX}$ is charged towards its positive peak which is higher than the main inductor current $i_{LM}$, and then after $M_L$ is

turned off at $t_1$, the difference between $i_{AUX}$ and $i_{LM}$ charges $V_{SW}$ all the way to $V_i$ such that $M_H$ can be turned on under ZVS condition. After $M_H$ is turned off at $t_3$, both $i_{LM}$ and $i_{AUX}$ discharge $V_{SW}$ towards 0 such that $M_L$ can be turned on under ZVS condition. It is worth to note that without the auxiliary branch, synchronizing switch $M_L$ can still operate under ZVS condition due to $i_{LM}$; However, ZVS operation of the active switch $M_H$ requires assistance from the auxiliary branch.

In the multiphase (N-phase) topology as shown in Figure 2.3 (c), each active switch in each phase requires one branch of the auxiliary circuitry, and therefore a total number of N branches are required which not only increases the board volume and cost, but also introduces additional conduction loss in the auxiliary components [26, 27]. It would be beneficial if the auxiliary circuitry can be somehow shared between multiple phases such that ZVS operation of each power FET can be achieved with less number of auxiliary components and less penalty in board volume, cost and conduction loss [28].

Similar demand for auxiliary circuitry sharing also exists in non-inverting buck boost converters [29, 30] as shown in Figure 2.4. $M_1$ and $M_2$ are active switches of which ZVS operation requires assistance from the auxiliary branch. It would potentially reduce the power loss and component counts if one auxiliary branch could achieve ZVS for both active switches [31]. It is also worth to note that such demand for auxiliary circuitry sharing exists universally in every type of soft-switched converters (including ZVT topologies) with multiphase or multi-switch-node, instead of only in QSW-ZVS topologies as shown in Figures 2.3 and 2.4.




(a) (b) (c)

Figure 2.3. (a) schematic of QSW-ZVS buck converter; (b) waveforms of QSW-ZVS buck converter; (c) N-phase QSW-ZVS topology.

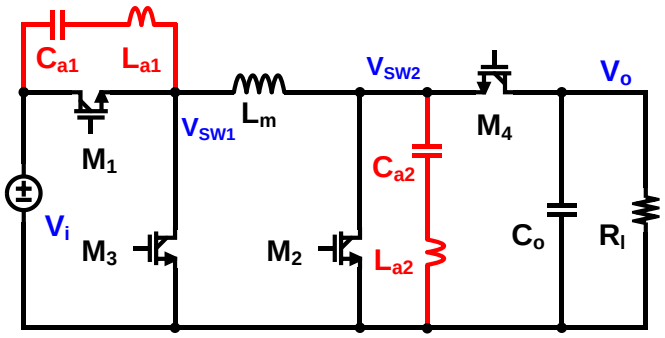
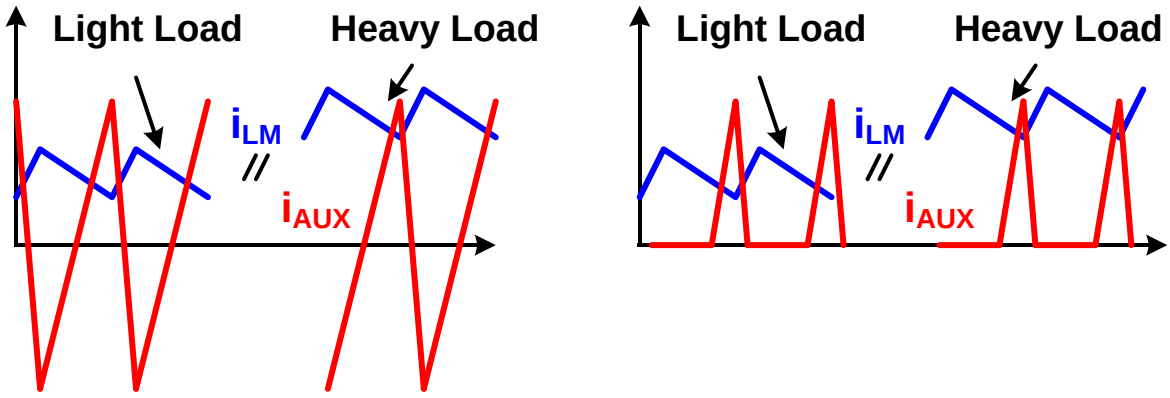



Figure 2.4. Schematic of QSW-ZVS non-inverting buck boost converter.

## 2.4 Design Challenge for Light-Load Efficiency in Soft-Switched Converters

The auxiliary branch of the soft-switched converter is such designed that soft switching is ensured under the worst case (i.e. heavy load condition) of steady state operation. For QSW-ZVS technique, the auxiliary inductor current ripple ($i_{AUX}$) needs to be larger than the maximum value of main inductor current ($i_{LM}$) as shown in Figure 2.5 (a). Since the current ripple is merely dependent on the value of $L_{AUX}$, $V_i$ and $V_o$ and none of these parameters changes with load condition, $i_{AUX}$ ripple cannot decrease in light load condition. Therefore the power efficiency of QSW-ZVS converter is only optimized for the heavy load condition, but not for the light load condition [28, 30, 32].

Figure 2.6 demonstrates one of ZVT topologies for a buck converter and its inductor currents under heavy load and light load conditions are shown in Figure 2.5 (b). Since the auxiliary inductor operates in DCM, the conduction loss of the auxiliary branch is much smaller in the ZVT converter than that in the ZVS converter with the same load current. However, the on-time of the auxiliary switch $M_a$ is either fixed or manually controlled in all the existing ZVT converters in order for simple control on the board [33 – 36]. In fixed on-time control, the on-time is determined by the worst case of all combinations of the input voltage, output current and switching frequency. Since the auxiliary current ripple and the associated conduction loss do not scale with the load current, the power efficiency at the light load condition can be very poor. While manual control of the auxiliary switch can achieve better efficiency in the open-loop prototype for power stage demonstration, it is not practical in closed-loop converters with wide range of input voltage and output current. Therefore, an auxiliary control loop to dynamically adjust the on-time of the auxiliary switch based on the load current is highly desired [37].




(a) (b)

Figure 2.5. (a) Inductor waveforms of QSW-ZVS converters; (b) Inductor waveforms of ZVT converters.

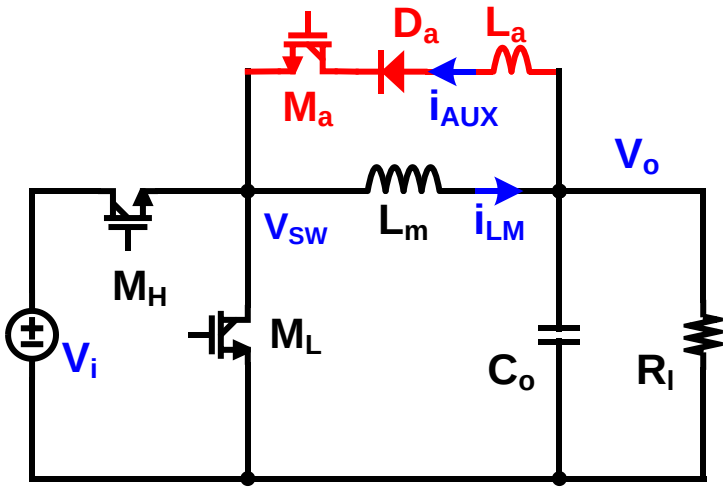



Figure 2.6. Schematic of ZVT buck converter.

## 2.5 Contributions of This Research and Dissertation Organization

As discussed in the previous chapters, soft-switched converters are widely used in high-voltage and high-frequency applications. Enhancement-mode GaN FETs have gained more and more popularity and can contribute their merits of low $R_{DS,ON}$ and small parasitic capacitance in the soft-switched converters. However, the electrical characteristics of GaNs are different from that of traditional MOSFETs, which requires new functions in the driver design. Also, the existing non-isolated soft-switching topologies require one dedicated auxiliary branch for each active power FET, and therefore the number and volume of auxiliary components are prohibitively large in multi-phase converters and non-inverting buck-boost converters. Finally, the traditional ZVS and ZVT converters can only optimize the power efficiency at heavy load but have light load efficiency adversely affected due to the additional conduction loss in the auxiliary branch.

To solve the above issues, this dissertation proposes new circuit design techniques to adaptively control the dead time to minimize the reverse conduction loss of GaN FETs in any soft-switched converters and enhance the dv/dt noise immunity in high-voltage level shifter. In addition, in the system design level, the dissertation proposes new topologies to minimize the number and volume of auxiliary components in the soft-switched multi-phase converters and non-inverting buck-boost converters, as well as adaptive auxiliary current control scheme for ZVT converters to realize optimized power efficiency from heavy load down to light load conditions.

This dissertation is organized as follows. Soft-switched DC-DC converters and enhancement-mode GaN FETs are generally introduced in Chapter 1. Chapter 2 reviews the circuit design challenges of GaN drivers for soft-switched converters, the system design challenges for soft-switched multi-phase converters and non-inverting buck-boost converters, and the design challenge to optimize the power efficiency of ZVT converters in a wide range of load conditions. Chapter 3 proposes a GaN-based isolated bus converter and demonstrates the design and experiment results of the proposed GaN driver with slope-sensing ZVS detection, adaptive dead time control and noise immunity enhanced level shifter. Chapter 4 proposes the sharing scheme of the auxiliary branch for multi-phase and non-inverting buck-boost converters, as well as the adaptive auxiliary current control scheme for ZVT converters with improved light load efficiency. Finally, the future work that can be extended from this dissertation is provided in Chapter 5.

# CHAPTER 3

# DESIGN OF HIGH-VOLTAGE HIGH-FREQUENCY GAN-BASED ISOLATED DC-DC BUS CONVERTER WITH MONOLITHIC GATE DRIVER AND SLOPE-SENSING ZVS DETECTION [1]

## 3.1 Overview

The growing development of power supplies in industrial and telecom systems demands for DC-DC converters to be increasingly power efficient, compact and reliable. As these power supplies could experience fluctuations of the input voltage from 150 V to 400 V [1], isolated DC-DC converters should properly support a wide range of the high input voltage to ensure the reliability of the power system. For lowering the system cost and the converter volume, these converters need to operate in the high frequency of the MHz range in order to reduce the required values and volumes of the passive components. It is crucial to turn on the power FETs on the primary side under ZVS condition with such high input voltage and high switching frequency [38, 39]. In addition, enhance mode GaN FETs become more and more popular in high voltage applications with their superior $R_{DSON}$ to the traditional MOSFET counterparts.

To address the issues associated with driving GaN FETs in ZVS operation and level-shifting signals reliably to high voltage domain as discussed in Chapter 2, this chapter describes an isolated full-bridge phase-shifted DC-DC converter with eGaN power FETs to support a wide input voltage range from 150 V to 400 V and deliver a maximum output power of 250 W [15, 18]. A synchronous gate driver with a fully-integrated slope-sensing ZVS detector (SS-ZVSD) is developed to enable full- and partial-ZVS operations. Adaptive dead-time with near-constant

[1] © 2018 IEEE. Adapted, with permission, from L. Cong, H. Lee, A 1-2MHz 150- -400V GaN-based isolated DC-DC bus converter with monolithic slope-sensing ZVS detection, IEEE Journal of Solid-State Circuits, 10/2018.

ZVS turn-on delay of 13 ns is achieved to allow the converter operation in the MHz range and minimize various power losses under different input voltages and load currents. A new level shifter with a differential-mode noise blanking scheme is also proposed in the gate driver to enhance the converter reliability in high input voltages. This chapter details the design considerations, operation principle and circuit implementations of the isolated full-bridge converter, the SS-ZVSD and the new high-voltage level shifter. This chapter is organized as follows. Section 3.2 presents system architecture, design considerations, and full- and partial-ZVS operations of the isolated GaN-based full-bridge converter. The circuit implementation details of the proposed gate driver including the monolithic SS-ZVSD and the reliable HV level shifter are discussed in Section 3.3. Finally, the experimental results and conclusions are given in Sections 3.4 and 3.5, respectively.

## 3.2 Isolated QSW-ZVS DC-DC Bus Converter

Figure 3.1 shows the system architecture of the proposed high-voltage isolated ZVS bus converter. In the power stage, four 650-V eGaN FETs form a full-bridge topology on the primary side of the transformer. Two diodes $D_1$, $D_2$, a filtering inductor $L_F$ and an output capacitor $C_O$ form a rectifier topology on the secondary side. The planar transformer TR is used for the voltage scaling and electrical isolation between primary and secondary sides. In addition, the leakage inductance $L_R$ of TR is used to resonate with the output capacitance $C_{OSS}$ of each power FET for realizing ZVS operation during switching.

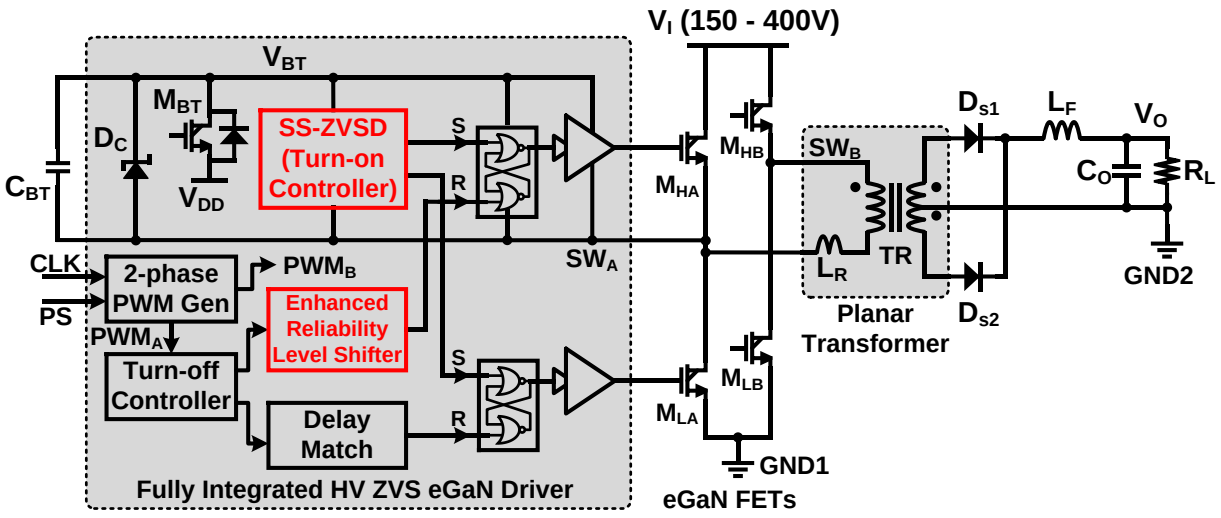



Figure 3.1. Schematic of the proposed isolated full-bridge bus converter with a monolithic ZVS driver.

### 3.2.1 Full-ZVS Operation Principles of the Proposed Full-Bridge Converter

Figure 3.2(a) shows the key waveforms of the proposed full-bridge converter during the full-ZVS operation. The leakage inductance of the transformer is used to resonate with $C_{OSS}$ of the power FETs during the dead time such that the positive leakage inductance current $I_{LR}$ realizes ZVS of $M_{LA}$ and $M_{HB}$, while the negative $I_{LR}$ enables ZVS of $M_{HA}$ and $M_{LB}$. Since the ripple of $I_{LR}$ is proportional to the load current $I_O$, the $I_{LR}$ ripple is large enough to fully discharge $C_{OSS}$ and achieve the full-ZVS operation for power FETs in the medium- and heavy-load condition. Although increasing the leakage inductance can enlarge the load current range for the full-ZVS operation due to the increase in energy of the resonant tank on the primary side, it would decrease the effective duty ratio $D_{eff}$ of $V_C$ on the secondary side in Figure 3.2 (a). As the average value of $V_C$ is the output voltage, the upper bound of the leakage inductance is limited by the converter output voltage. In this design, the leakage inductance is selected as 15 μH. For

the full-ZVS operation, there are ten time subintervals in a switching period and their operation states shown in Figure 3.3 are described below.

*Subinterval 1 [$t_0 - t_1$]*: $M_{HB}$ and $M_{LA}$ are in the on-state, while $M_{HA}$ and $M_{LB}$ are off. $V_{SWA}$ and $V_{SWB}$ are pulled to 0 and $V_I$, respectively. Current $I_{LR}$ is decreasing towards its negative valley value as shown in Figure 3.2 (a). On the secondary side, $D_{S2}$ is on to deliver the filtering inductor current $I_{LF}$.

*Subinterval 2 [$t_1 - t_2$]*: $M_{HB}$ and $M_{LA}$ are turned off at $t_1$, and the negative $I_{LR}$ charges node $SW_A$ towards $V_I$ and discharges $SW_B$ towards 0. By $t_2$, $V_{SWA}$ is still lower than half of $V_I$ and $V_{SWB}$ is still higher than half of $V_I$. Diode $D_{S2}$ is on to deliver the filtering inductor current $I_{LF}$.

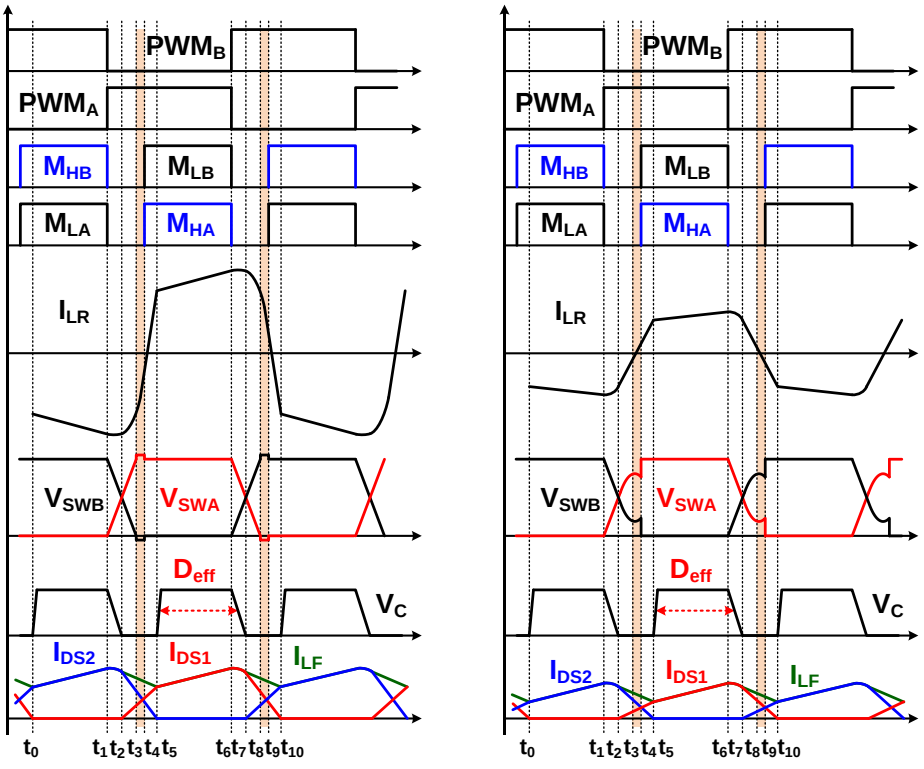



Figure 3.2. Key waveforms of (a) full-ZVS and (b) partial-ZVS operation of the proposed full-bridge converter.

*Subinterval 3 [$t_2 - t_3$]*: Negative $I_{LR}$ continues to charge $SW_A$ and discharge $SW_B$ such that $V_{SWA}$ reaches $V_I$ and $V_{SWB}$ reaches 0 at $t_3$. ZVS condition is ready for $M_{HA}$ and $M_{LB}$ at the end of this subinterval.

*Subinterval 4 [$t_3 - t_4$]*: This subinterval represents the delay from ZVS being achieved to the moment $M_{HA}$ and $M_{LB}$ being fully turned on. This ZVS turn-on delay is mainly due to the speed of the ZVS detector. Since $M_{HA}$ and $M_{LB}$ would be reversely conducting with considerable power loss, this subinterval is minimized by the proposed driver with the SS-ZVSD for the dead time control.

*Subinterval 5 [$t_4 - t_5$]*: $M_{HA}$ and $M_{LB}$ are turned on with zero drain-to-source voltage at $t_4$ and then current $I_{LR}$ is changed to the positive direction. Both $D_{S1}$ and $D_{S2}$ are conducting $I_{LF}$ on the secondary side.

*Subinterval 6 [$t_5 - t_6$]*: At $t_5$, $I_{LR}$ reaches the reflected value of $I_{LF}$ and then $D_{S2}$ turns off with only $D_{S1}$ conducting $I_{LF}$ on the secondary side. $I_{LR}$ continues to increase towards its positive peak as shown in Figure 3.2 (a).

*Subinterval 7 [$t_6 - t_7$]*: At $t_6$, $M_{HA}$ and $M_{LB}$ are turned off and positive $I_{LR}$ discharges $SW_A$ towards 0 and charges $SW_B$ towards $V_I$. By $t_7$, $V_{SWB}$ is still lower than half of $V_I$ and $V_{SWA}$ is still higher than half of $V_I$. $D_{S1}$ is on to deliver the filtering inductor current $I_{LF}$.

*Subinterval 8 [$t_7 - t_8$]*: Positive $I_{LR}$ continues to discharge $SW_A$ and charge $SW_B$ such that $V_{SWA}$ reaches 0 and $V_{SWB}$ reaches $V_I$ at $t_8$. ZVS condition of $M_{HB}$ and $M_{LA}$ is established at the end of this subinterval.

*Subinterval 9 [$t_8$ – $t_9$]*: This subinterval represents another ZVS turn-on delay similar to subinterval 4. It starts from ZVS being achieved to the moment $M_{HB}$ and $M_{LA}$ being fully turned on.

*Subinterval 10 [$t_9$ – $t_{10}$]*: $M_{HB}$ and $M_{LA}$ are turned on with zero drain-to-source voltage and then $I_{LR}$ is changed to the negative direction. Both $D_{S1}$ and $D_{S2}$ are conducting $I_{LF}$ on the secondary side. Time instant $t_{10}$ is the end of this switching period and the operation sequence will repeat from subinterval 1 thereafter.

### 3.2.2 Partial-ZVS Operation Principles of the Proposed Full-Bridge Converter

When the load current becomes low, energy stored in the resonant tank decreases. When there is not sufficient energy to completely discharge $C_{OSS}$ during the dead-time, partial-ZVS of power FETs occurs. For the partial-ZVS operation, the key waveforms are shown in Figure 3.2 (b). There are also ten subintervals in a switching period, most of which are the same or very similar to those of full-ZVS operation and are not repeated here. As shown in Figure 3.4, subintervals 4 and 9 of the partial-ZVS operation are different from those of the full-ZVS operation and are described as below.

*Partial-ZVS Subinterval 4 [$t_3$ – $t_4$]*: This subinterval represents the delay from soft switching being completed to the instant that $M_{HA}$ and $M_{LB}$ being fully turned on. Since $I_{LR}$ increases to 0 and changes its direction at $t_3$ in Figure 3.2 (b), $V_{SWA}$ starts to drop after reaching its peak value and $V_{SWB}$ starts to rise after reaching its valley value, resulting in residual switching loss when $M_{HA}$ and $M_{LB}$ are turned on at $t_4$. In order to minimize this residual switching loss, the proposed

SS-ZVSD identifies the peak and valley voltages of the switch nodes and minimizes the duration of this subinterval.

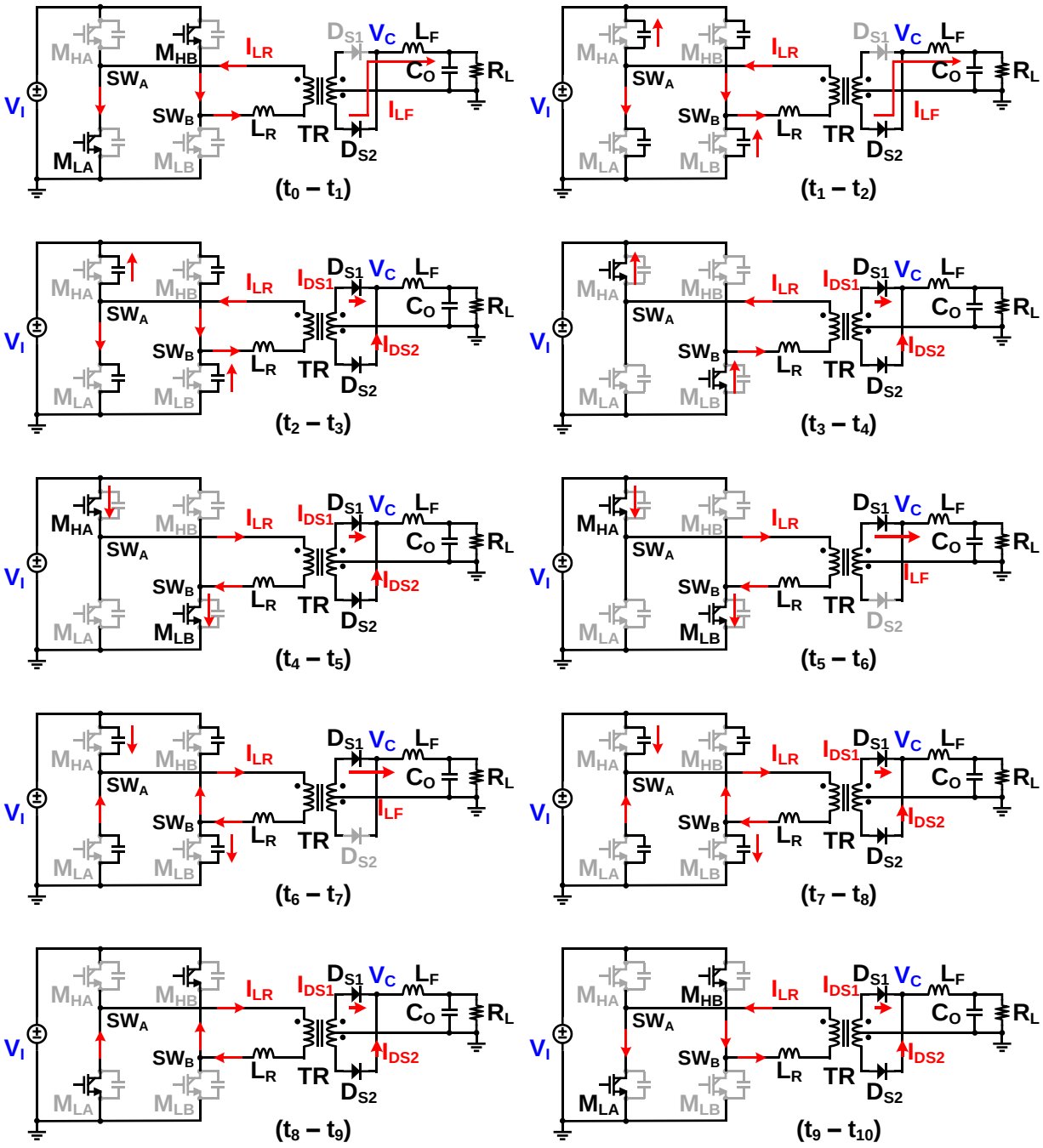



Figure 3.3. Converter states in different time subintervals of a period for full-ZVS operation.

*Partial-ZVS Subinterval 9 [$t_8$ – $t_9$]*: This subinterval represents another ZVS turn-on delay similar to the partial-ZVS subinterval 4. The proposed driver also minimizes this subinterval for improving the converter power efficiency.

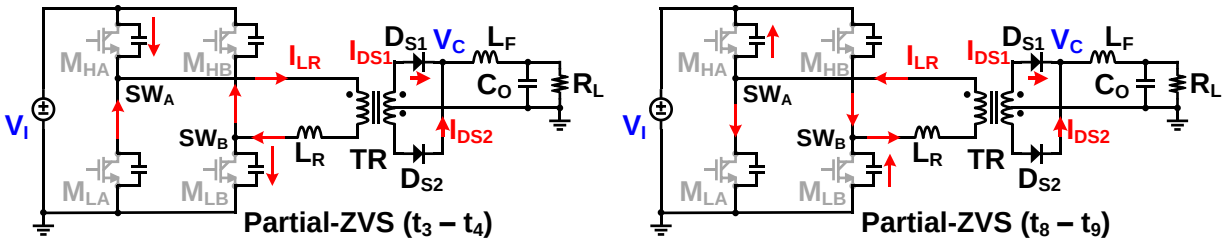



Figure 3.4. Partial-ZVS operation states that are different from those in the full-ZVS operation.

### 3.3 Proposed On-chip Gate Driver with Adaptive Dead Time Control

A fully-integrated high-voltage ZVS driver is developed to drive four eGaN power FETs in two phases. A two-phase PWM signal (i.e. $PWM_A$ and $PWM_B$) is generated from the input CLK with default phase shift equal to 180°, and $PWM_A$ and $PWM_B$ have the same duty ratio of 0.5. In order to continuously adjust the conversion ratio between input voltage $V_I$ and output voltage $V_O$, the phase shift between $PWM_A$ and $PWM_B$ can be changed via input PS. For each phase, the turn-off of both high- and low-side power FETs is controlled by the respective PWM signal, while the turn-on of both FETs is automatically controlled by the proposed slope-sensing ZVS detector (SS-ZVSD) such that both power FETs are turned on with minimized switching loss due to appropriate dead-time. For supporting the partial-ZVS operation of the converter, a new HV level shifter is developed. The new level shifter can avoid internal logic error under very fast slew rate of the switch node, thereby improving the converter reliability.

### 3.3.1 Slope-Sensing ZVS Detector and Near-Optimum Dead Time Control Scheme

To minimize the reverse conduction loss during the dead time in the full-ZVS operation and the residual switching loss in the partial-ZVS operation, the slope-sensing ZVS detector is developed to realize near-optimum dead-time control with minimized ZVS turn-on delay for both operations in high frequency. The common scenario of full- and partial-ZVS operations is that the slope of switch node voltage $V_{SW}$ equals 0 when $V_{SW}$ reaches its peak value. Therefore, instead of using state-of-the-art voltage-sensing based ZVSDs [40 – 42] that monitor the absolute voltage at SW but fail to generate dead-time when $V_{SW}$ never reaches $V_I$ in the partial-ZVS operation, the proposed SS-ZVSD senses the slope of $V_{SW}$ and automatically provides dead-time when zero slope is detected in both full- and partial-ZVS operations. As shown in Figure 3.5, the proposed SS-ZVSD for a half-bridge topology consists of a $V_{SW}$ slope sensor, a high-side turn-on controller and a low-side turn-on controller. The $V_{SW}$ slope sensor uses the parasitic cap ($C_P \approx$ 0.2 pF) of an always-off HV transistor $M_D$ to convert the slope of $V_{SWA}$ to a current pulse $I_{SEN}$ and mirrors the current pulse into the high- and low-side turn-on controllers as $I_{SENH}$ and $I_{SENL}$, respectively. Note that the HV transistor $M_D$ is a typical low-side device with its gate and source terminals connected to low voltage and only drain terminal exposed to high voltage, and is thus commonly available in commercial HV CMOS processes. In the high-side (or low-side) turn-on controller, $I_{SENH}$ (or $I_{SENL}$) is compared with a dynamic current reference $I_{REFH}$ (or $I_{REFL}$) to determine when the slope of $V_{SWA}$ turns to 0. The key timing waveforms of the proposed SS-ZVSD for full- and partial-ZVS operations are shown in Figure 3.6.

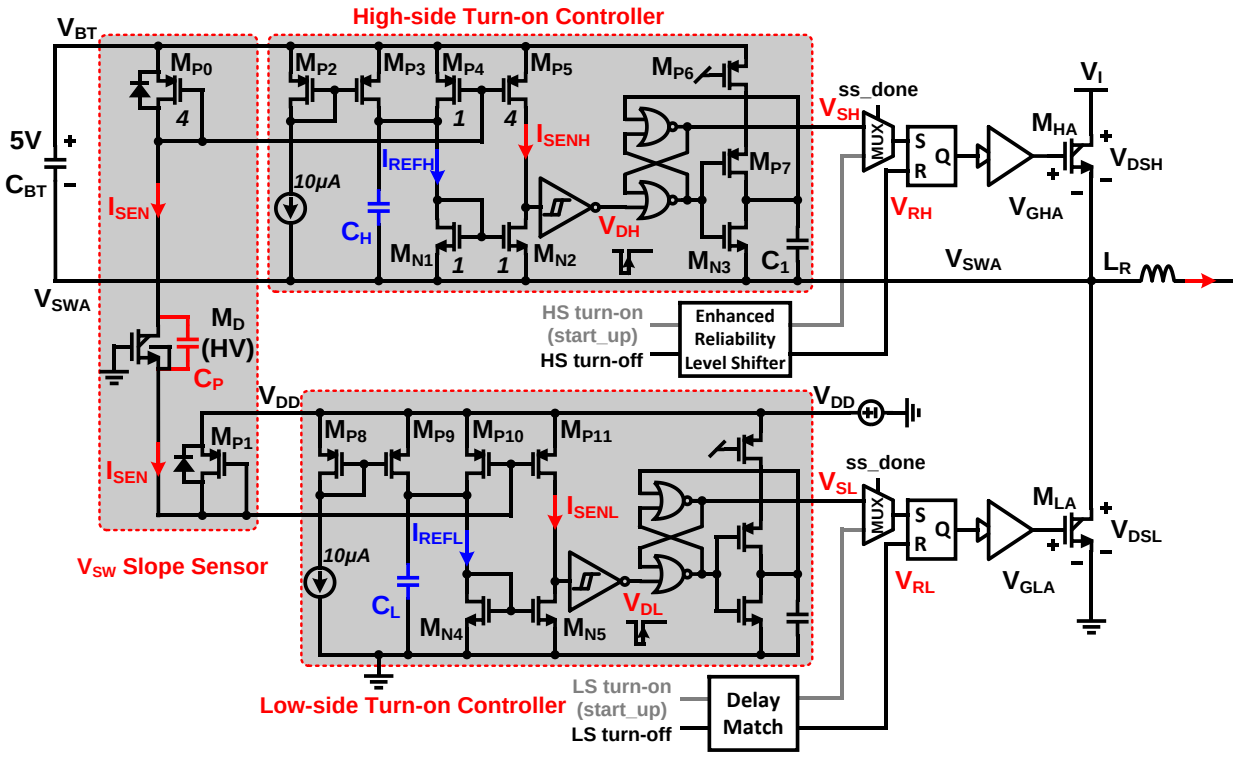



Figure 3.5. Schematic of the proposed SS-ZVSD.

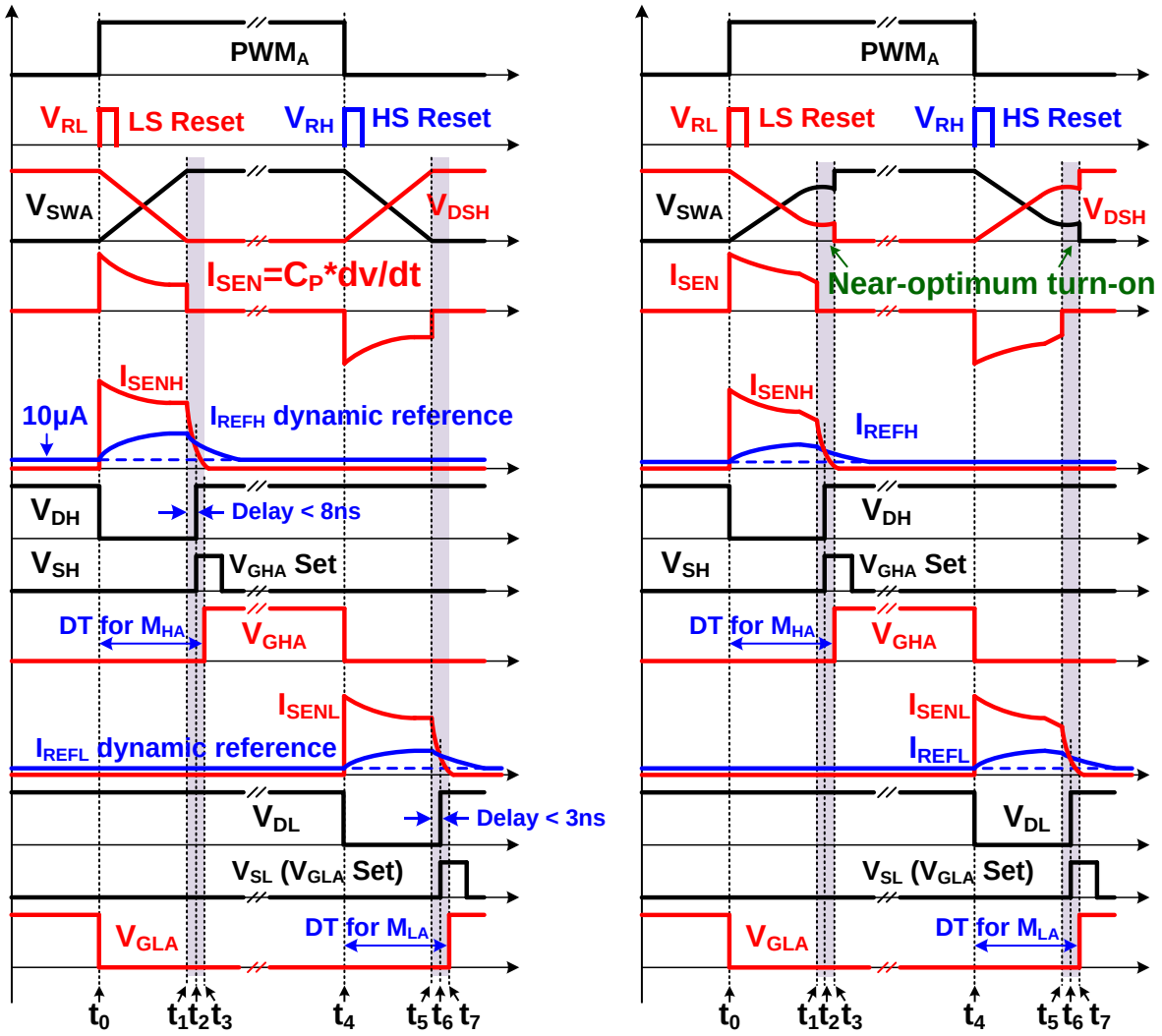



Figure 3.6. Timing waveforms of the SS-ZVSD during (a) full-ZVS and (b) partial-ZVS operations.

Without loss of generality, the operation of turning on high-side power FET $M_{HA}$ is described as follows. After the low-side $M_{LA}$ is turned off, the transient current of $L_R$ flows into the node $SW_A$ such that both voltages $V_{SWA}$ and $V_{BT}$ increase towards $V_I$, and thus $C_P$ generates a positive current pulse $I_{SEN}$ that is given as

$$I_{SEN} = C_P \frac{dV_{SWA}}{dt} \tag{3.1}$$

With the designed aspect ratios, during $t_0$ to $t_1$, the current in $M_{P5}$ ($I_{SENH}$) tends to be larger than the current in $M_{N2}$, resetting the output of the comparator $V_{DH}$. At $t_1$, after $V_{SWA}$ reaches $V_I$ for the full-ZVS operation in Figure 3.6 (a) or reaches its peak value for the partial-ZVS operation in Figure 3.6 (b), $V_{SWA}$ slope turns flat and thus $I_{SEN}$ drops to 0. $I_{SENH}$ decays to 0 with finite time constant due to parasitics at the gate and drain terminals of $M_{P5}$. Since $I_{REFH}$ has been dynamically biased to around a quarter of $I_{SEN}$ before $t_1$ and $I_{REFH}$ decays much slower than $I_{SENH}$ with $C_H$ designed larger than $M_{P5}$ parasitic capacitance, $I_{SENH}$ drops lower than $I_{REFH}$ at $t_2$, which sets the Schmitt trigger output $V_{DH}$ and initiates one shot of $V_{SH}$ to set $V_{GHA}$ and turn on $M_{HA}$ at $t_3$. The low-side turn-on controller has the same operation principle as the high-side counterpart and the operations for turning on power FET $M_{LA}$ in both full- and partial-ZVS cases are illustrated from $t_4$ to $t_7$ in Figure 3.6 (a) and (b), respectively.

As shown in Figure 3.6, the total ZVS turn-on delay consists of the detection delay $t_{dect\_delay}$ ($t_1 - t_2$ for high-side power FET $M_{HA}$ or $t_5 - t_6$ for low-side power FET $M_{LA}$) and the delays of the logic (MUX and SR latch) and digital buffer ($t_2 - t_3$ for $M_{HA}$ or $t_6 - t_7$ for $M_{LA}$). Since the buffer delay $t_{buf\_delay}$ is much longer than the logic delay, the ZVS turn-on delay $t_{total\_delay}$ can be given as

$$t_{total\_delay} = t_{detect\_delay} + t_{buf\_delay} \tag{3.2}$$

where the buffer delay $t_{buf\_delay}$ is about 3 – 4 ns. The value of $t_{dect\_delay}$ is typically < 8 ns for high side and 3 ns for low side in this design. Therefore, $t_{total\_delay}$ is around 12 ns and 6 ns for turning on $M_{HA}$ and $M_{LA}$, respectively. With the constant supply ($V_{BT} - V_{SWA}$) (or $V_{DD}$) for the high-side

(or low-side) turn-on controller, logic circuit and buffer, the value of $t_{total\_delay}$ can maintain constant even when the converter input $V_I$ or the load $I_O$ (thus $I_{LR}$) changes. Moreover, since the proposed SS-ZVSD performs high-side and low-side ZVS detections in their respective common-mode voltage domain, no level shift is needed for turning on the power FETs. By removing the delay of the level shifting in $t_{total\_delay}$, the proposed SS-ZVSD provides adaptive dead time with short turn-on delay for both full- and partial-ZVS operations under different input voltages and load currents.

Since the magnitude of $I_{SEN}$ is proportional to the slope of $V_{SWA}$ and the zero slope detection is performed by comparing $I_{SENH}$ ($I_{SENL}$) with the reference $I_{REFH}$ ($I_{REFL}$), the slowest slope that is detectable is determined by the current level of the reference $I_{REFH}$ ($I_{REFL}$). To achieve a wide detection range of $V_{SWA}$ slope, $I_{REFH}$ ($I_{REFL}$) is dynamically biased by a quarter of $I_{SENH}$ ($I_{SENL}$) in this design in addition to the static bias current of 10 μA for boosting the value of $I_{REFH}$ ($I_{REFL}$). With a larger $I_{REFH}$ ($I_{REFL}$), $I_{SENH}$ ($I_{SENL}$) is still larger than $I_{REFH}$ ($I_{REFL}$) at $t_1$ ($t_5$), but quickly falls smaller than $I_{REFH}$ ($I_{REFL}$) after $t_1$ ($t_5$) to trigger $V_{DH}$ ($V_{DL}$), thereby reducing $t_{dect\_delay}$. It should be noted that the 10-μA current source is used to only hold $V_{DH}$ ($V_{DL}$) logic after detection is finished and the variation to this static current does not affect the detection range. Two SS-ZVSDs dissipate a total 200-μW (that is only 0.0002% of the minimum converter output power of 96 W) in the full-bridge converter. Moreover, since the dynamically-biased reference $I_{REFH}$ ($I_{REFL}$) depends on the magnitude of $I_{SENH}$ ($I_{SENL}$) itself, the reference helps reduce the sensitivity of the slope change requirement. The correct ZVS detection is ensured for the slope changing from the initial value of at least 0.5 V/ns to 0 based on corner simulations in the design phase. This 0.5-V/ns slope requirement practically covers the entire slope range of the HV bus

converter in both full- and partial-ZVS operations. Moreover, hysteresis used in the Schmitt trigger and the NOR-based RS latch following $V_{DH}$ ($V_{DL}$) in the turn-on controller avoid sending repetitive turn-on commands if voltage ringing is present at $SW_A$ to maintain system reliability.

### 3.3.2 HV Level Shifter with Differential-Mode Noise Blanking Scheme

With the turn-on command generated locally from the SS-ZVSD, the level shifter is another key block in the proposed gate driver to upshift the turn-off command from the low-side PWM signal to the high-voltage domain, as shown in Figure 3.5. The level shifter is also used to upshift the turn-on command with fixed dead time during the startup process (ss_done = 0) when soft-switching is not yet available. The major design challenge of the level shifter in high input voltages is its reliability in partial-ZVS and hard-switching operations, in which positive dv/dt at the switch node voltage can be as large as tens of V/ns. Figure 3.7 shows the schematic of the traditional level shifter design and its operation waveforms during the turn-on of high-side power FET $M_H$. During positive slewing of voltages $V_{SW}$ and $V_{BT}$, the large parasitic capacitance at drain terminals of HV transistors $M_{N1}$ and $M_{N2}$ slows down the increase in $V_1$ and $V_2$ and simultaneously pulls down ($V_1 - V_{SW}$) and ($V_2 - V_{SW}$). With both inputs of the SR latch being logic 1, $V_O$ can present false logic to cause unexpected turn-on / -off of power FET $M_H$. In addition, both LV devices $M_{P1}$ and $M_{P2}$ may experience their drain-to-source voltage ($V_{BT} - V_1$ or $V_{BT} - V_2$) higher than the allowable voltage rating due to slow increase in $V_1$ and $V_2$ caused by large parasitic capacitance.

Previously, a pair of dynamic current sources (one connected from node $V_{BT}$ to $V_1$ and the other from $V_{BT}$ to $V_2$) were reported to provide additional transient current to increase the

positive slew rate of $V_1$ and $V_2$ [25]. However, large-size transistors in the dynamic current sources are needed to provide sufficient transient current to handle high dv/dt of the switch node voltage, and the parasitic capacitance of the large-size transistors would slow down the transition of the level shifter.

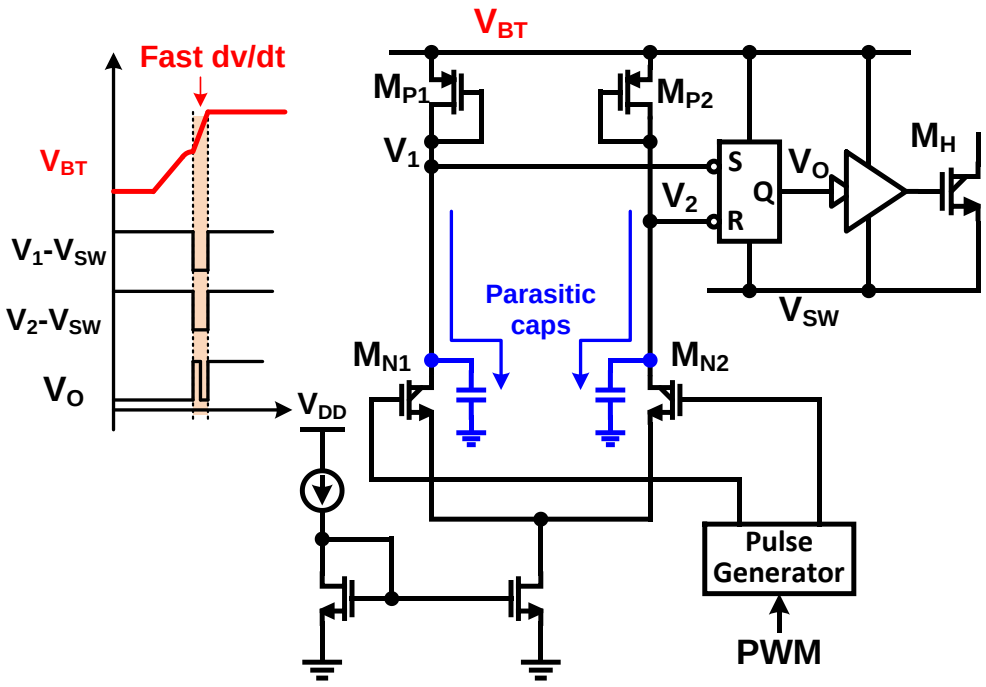



Figure 3.7. Structure and waveforms of a traditional HV level shifter.

To enhance the reliability under fast slew rate of the switch node voltage without compromising the speed of the level shifting, a new HV level shifter as shown in Figure 3.8 is proposed via body diode clamping and differential-mode noise blanking (DMNB). Body diodes of two small-size always-off LV nMOS (one connected between node $V_{H1}$ and $V_{SWA}$ and the other located between $V_{H2}$ and $V_{SWA}$ in Figure 3.8) ensures drain-to-source voltage of four isolated LV transistors located between node $V_{BT}$ and $V_{H1}$ / $V_{H2}$ within their maximum voltage

rating, while having insignificant impact on the speed of the level shifting due to small parasitic capacitance from both small-size clamping transistors.

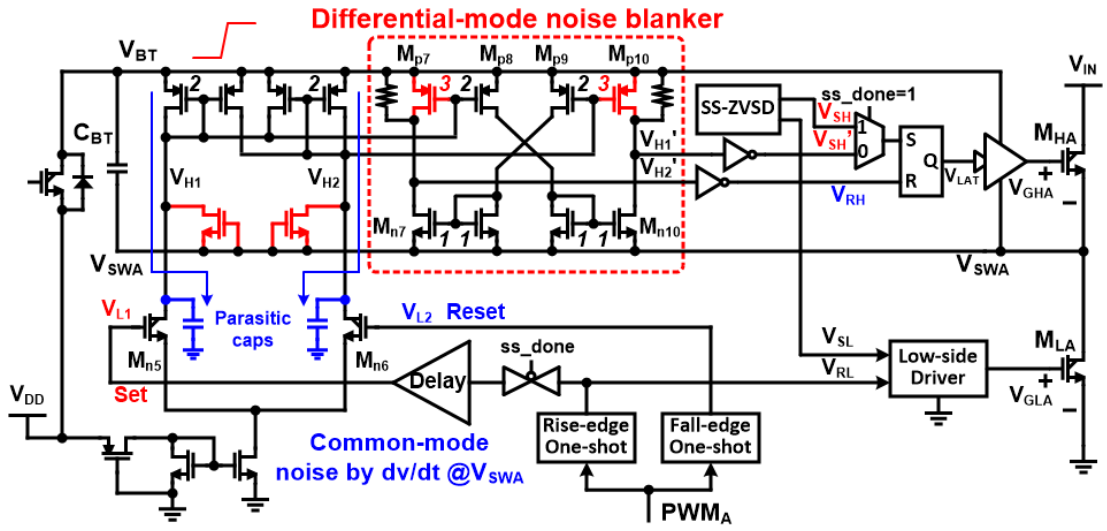



Figure 3.8. Structure of the proposed HV level shifter with the differential-mode noise blanking circuit for enhanced reliability.

The DMNB circuit is developed to block the common-mode voltage of $V_{H1}$ and $V_{H2}$ from affecting the logic output of the SR latch, and its key waveforms for different operation states are depicted in Figure 3.9 (a) – (c). In the partial-ZVS operation as shown in Figure 3.9 (a), when the SS-ZVSD detects $V_{SWA}$ slope = 0 and turns on power FET $M_{HA}$ at $t_1$, $V_{SWA}$ is pulled up to the input $V_I$ with a fast slew rate, and both ($V_{H1}$ – $V_{SWA}$) and ($V_{H2}$ – $V_{SWA}$) are pulled low by parasitic capacitors. Both $M_{P7}$ – $M_{P10}$ and $M_{N7}$ – $M_{N10}$ in the DMNB circuit are turned on. With the designed aspect ratios of $M_{P7}$ and $M_{N7}$, the drain voltage of $M_{P7}$ and $M_{N7}$ becomes logic 1 such that $V_{RH}$ can be held at logic 0 (inactive state for SR latch). With $V_{SH}$ being set at logic 1 by the SS-ZVSD, on-state of power FET $M_{HA}$ can be maintained during fast transition of $V_{SWA}$ ($t_1$ – $t_2$).

In the full-ZVS operation as shown in Figure 3.9 (b), dv/dt slope of $V_{SWA}$ is slow enough not to pull low ($V_{H1} - V_{SWA}$) and ($V_{H2} - V_{SWA}$) such that both ($V_{RH} - V_{SWA}$) and ($V_{SH} - V_{SWA}$) are logic 0 and power FET $M_{HA}$ is maintained off reliably during the positive slewing of $V_{SWA}$. Only after $V_{SWA}$ reaches $V_I$, $V_{SH}$ is set by the SS-ZVSD to turn on $M_{HA}$ under the ZVS condition. In the hard-switching operation of startup as shown in Figure 3.9 (c), both turn-on and –off of power FET $M_{HA}$ are controlled by low-side signal $V_{L1}$ and $V_{L2}$, respectively, at the inputs of the level shifter with signal ss_done = 0. After $M_{HA}$ is turned on at $t_1$, both ($V_{H1} - V_{SWA}$) and ($V_{H2} - V_{SWA}$) are pulled down due to fast slew rate of $V_{SWA}$. With $M_{P7}$ (or $M_{P10}$) providing a higher current than $M_{N7}$ (or $M_{N10}$), both outputs $V_{RH}$ and $V_{SH}$' of the DMNB circuit can be held at logic 0 (inactive state of SR latch) such that SR latch maintains its state and $M_{HA}$ stays in on-state reliably.

It should be noted that since the proposed level shifter and its DMNB circuit only has power consumption during the short pulses of $V_{L1}$ and $V_{L2}$ and during the transition of $V_{SWA}$, the average power consumption of the DMNB circuit is as low as 120 μW and the total average power dissipation of the proposed HV level shifter is 1.6 mW with 400-V input and 2-MHz switching frequency. With the push-pull structure in the DMNB circuit to reduce delay, the total propagation delay of the proposed HV level shifter is less than 15 ns for 150 – 400-V input.

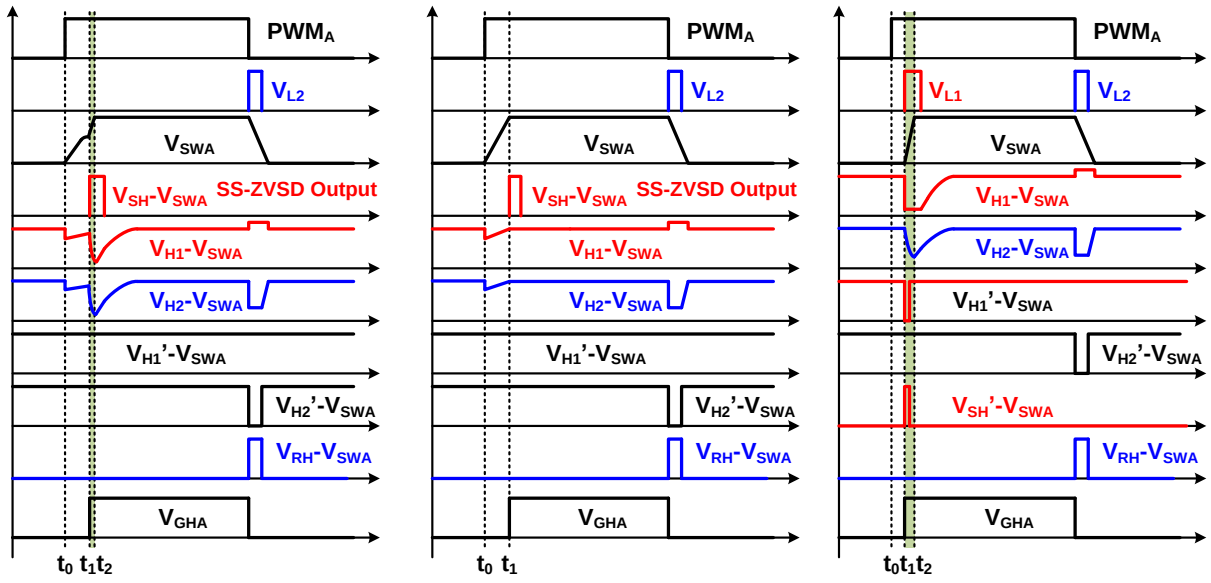



Figure 3.9. Operation waveforms of the proposed HV level shifter under (a) partial-ZVS, (b) full-ZVS, and (c) start-up conditions.

## 3.4 Measurement Results and Discussions

To verify the performances of the isolated phase-shifted full-bridge converter, the proposed full-bridge ZVS driver for four eGaN power FETs was implemented in a chip fabricated in a 1.45-µm 700-V BCD process [15, 18]. Figure 3.10 shows the micrograph of the ZVS gate driver and the total chip area is around 9 $mm^2$ excluding the testing circuit. In the experimental setup, the proposed driver IC adopts a commercial chip package and connects with power FETs on the printed circuit board. With $V_I$ from 150 V to 400 V, the proposed ZVS converter (Figure 3.1) delivers a nominal 48-V $V_O$ with the load current $I_O$ up to 5 A. Four 650-V e-mode GaN FETs (GS66502B) [43] from GaN Systems Inc. with their maximum tolerance of gate-to-source voltage being ±10V are employed as power switches on the primary side. Both the transformer and the filtering inductor on the secondary side are custom designed with planar magnetics. The

transformer is designed to provide the magnetizing inductance of 500 µH and the leakage inductance of 15 µH with 6-cm$^2$ footprint. The filtering inductor is designed to be 4 µH with 1.8-cm$^2$ footprint. 200V-5A diodes (S5DS) are utilized as rectifiers on the secondary side.

Figures 3.11 (a) – (d) show the ZVS turn-on delays $t_{total\_delay}$ for both high- and low-side power FETs in the full-ZVS operation for $V_I$ of 200 V and 400 V, respectively. The high-side ZVS turn-on delay, measured from the moment $V_{SWA}$ rising to $V_I$ (i.e. $V_{DSHA} = 0$) to the moment high-side FET is fully turned on, is around 12 ns – 13 ns in Figures 3.11 (a) and (c). The low-side ZVS turn-on delay, measured from the moment $V_{SWA}$ falling to 0 (i.e. $V_{DSLA} = 0$) to the moment low-side FET is fully turned on, is around 6 ns in Figures. 3.11 (b) and (d). With fast ZVS turn-on delays in full-ZVS operation, the reverse conduction time and the corresponding conduction loss of eGaN FETs can be minimized.

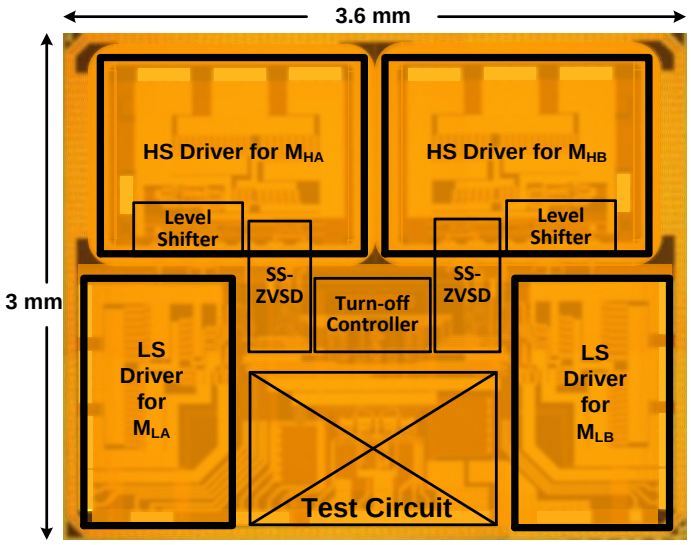



Figure 3.10. Micrograph of the proposed ZVS gate driver for the full-bridge converter using eGaN power FETs.

Figures 3.12 (a) and (b) show the measured waveforms of the switch-node voltage $V_{SWA}$ and high-side gate-drive voltage $V_{GHA}$ under the partial-ZVS condition with $V_I$ of 150 V and the load currents of 2.5 A and 2.1 A, respectively. The ZVS turn-on delay, measured from the moment $V_{SWA}$ reaching its peak to the moment high-side power FET is fully turned on, is around 12 – 13 ns in both cases, consistent to the measured ZVS turn-on delay of the high-side power FET in the full-ZVS operation. Thanks to the fast detection of the partial-ZVS operation, high-side power FET is able to fully turn on before switch-node voltage starts to drop and therefore the residual switching loss can be minimized. In addition, Figure 3.12 (b) shows that the proposed level shifter can withstand dv/dt transition of 45 V/ns in the partial-ZVS operations. It should be noted that the difference between the input voltage $V_I$ and the resonant peak of $V_{SWA}$ would cause transient overshoot at the gate voltage of low-side e-mode GaN FET $M_{LA}$ via its gate-to-drain capacitance $C_{gd}$ during the hard-switching duration (after $V_{SWA}$ reaches its resonant peak). In the design phase, this difference is set to be 50 V or less under different conditions. For the e-mode GaN FET GS66502B, the gate-to-drain capacitance $C_{gd}$ of 0.5 pF is much smaller than the gate-to-source capacitance of 50 pF. According to [44], the worst-case gate voltage overshoot of $M_{LA}$ is about 0.5 V even with infinite slew rate of $V_{SWA}$ and the maximum 50-V difference between $V_I$ and the resonant peak. Since the worst-case gate voltage overshoot of 0.5 V is always smaller than the device threshold voltage of 1.6 V, $M_{LA}$ is ensured to be off and no shoot-through current would exist.

Figure 3.13 (a) demonstrates that the dead time achieved by the proposed SS-ZVSD follows the same trend of the ideal dead time needed for switch-node voltage rising from 0 to $V_I$ at $V_I$ = 250 V for the load current range from 2 A to 5 A. The difference between the two curves

indicates the ZVS turn-on delay, which is very consistent with only 1-ns variation across the entire load range. Figure 3.13 (b) also compares the achieved dead time and the ideal dead time across a wide range of the input voltage from 150 V to 400 V, proving that the achieved ZVS turn-on delay is constant with respect to the input-voltage variation.

Figures 3.14 (a) and (b) validate the proper operation of the full-bridge converter with the proposed ZVS driver and dead-time control scheme by showing the steady-state waveforms with 300-V input and 1-MHz switching frequency and with 150-V input and 2-MHz switching frequency, respectively.

In Figures 3.15 (a) and (b), the power efficiency of the full-bridge bus converter is compared between using the proposed gate driver and using the traditional gate driver with 100-ns ZVS turn-on delay [45]. In the operation with 400-V input and 1-MHz switching frequency, the proposed driver helps the converter achieve 88.6% peak power efficiency at 3.3-A load current and reduce 1-W power loss at the full load of 5 A. In the operation with 150-V input and 2-MHz switching frequency, the proposed driver helps the converter achieve 90.2% peak power efficiency at 4-A load and reduce 1.6-W power loss at the full load condition.

Table 3.1 provides the performance comparisons of the proposed driver and the bus converter with those of other state-of-the-art designs having similar wide input voltage ranges. With the proposed SS-ZVSD for adaptive dead-time control in both full- and partial-ZVS operations, this driver reduces the ZVS turn-on delay from the traditional 100 ns to 13 ns and enables the usage of eGaN FETs up to 2-MHz ZVS operation with minimized reverse conduction loss and residual switching loss. With the merits of eGaN FETs and fast ZVS detection, the proposed converter

achieves comparable power efficiency with 14 times higher switching frequency and is capable of delivering higher maximum output power as compared to the prior art.

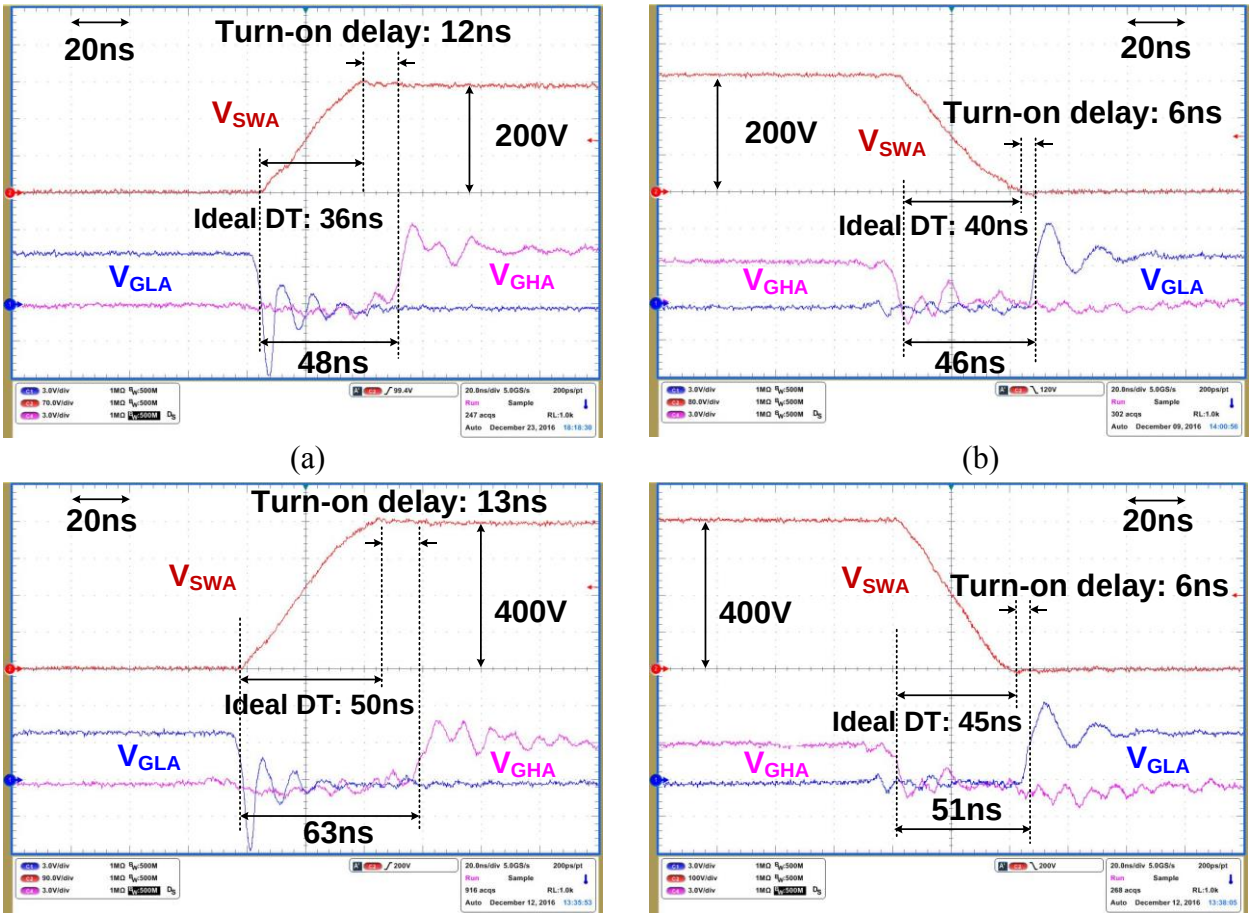
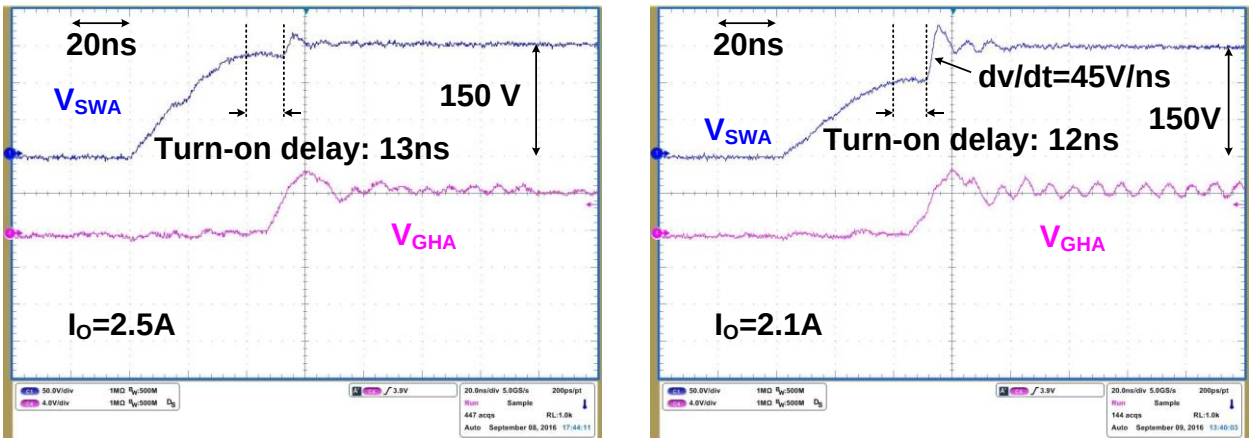
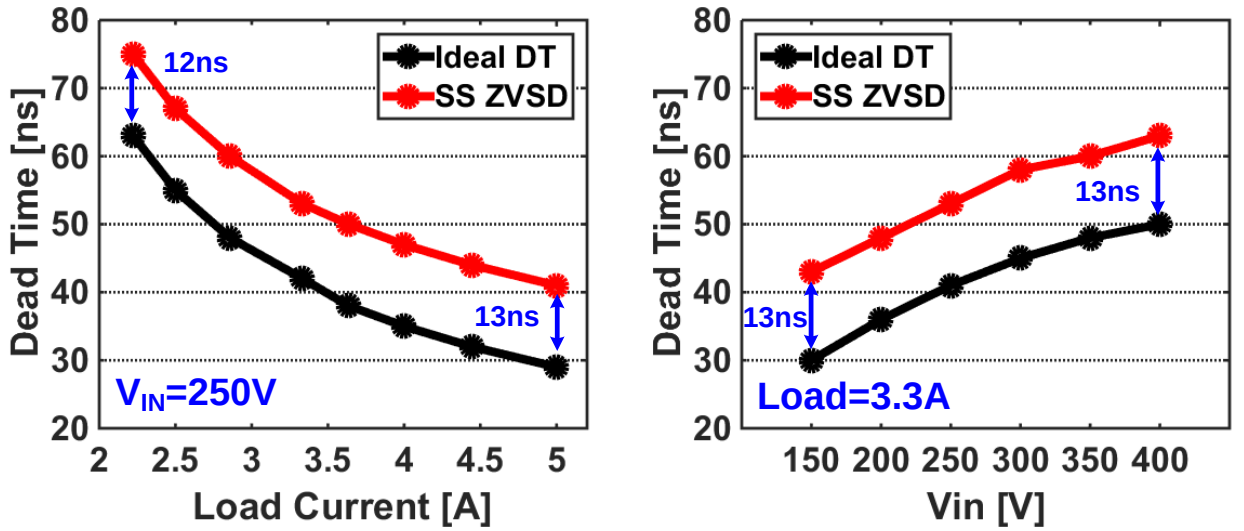



Figure 3.11. Measured $t_{total\_delay}$ in full-ZVS operation for (a) high-side and (b) low-side power FETs at $V_I$ = 200 V, $I_O$ = 4 A, and (c) high-side and (d) low-side power FETs at $V_I$ = 400 V, $I_O$ = 4 A.



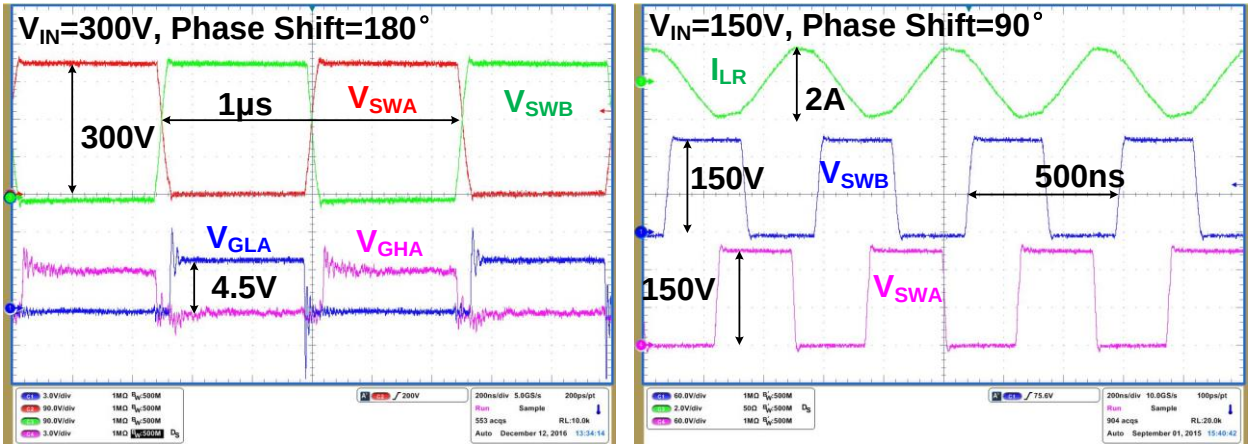

(a) (b)

Figure 3.12. Measured $t_{total\_delay}$ in partial-ZVS operation for (a) $I_O$ = 2.5 A and (b) $I_O$ = 2.1 A.



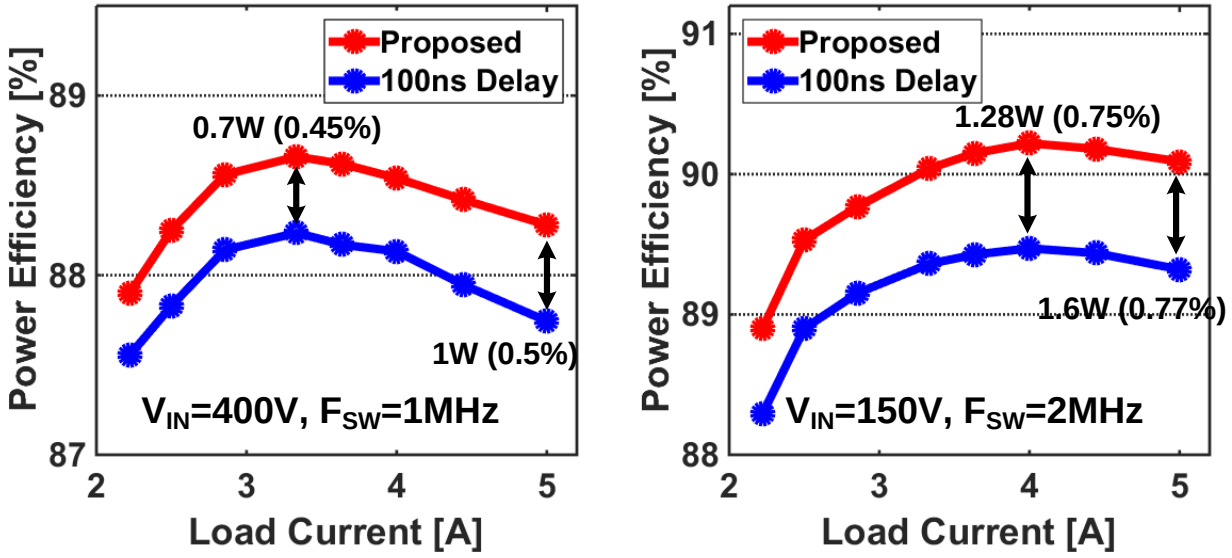

(a) (b)

Figure 3.13. Measured dead-time under different (a) load-current and (b) input-voltage conditions.




(a) (b)

Figure 3.14. Measured converter steady-state waveforms at (a) $V_I$ = 300 V, $I_O$ = 5 A, phase shift = 180° and (b) $V_I$ = 150 V, $I_O$ = 5 A, phase shift = 90°.




(a) (b)

Figure 3.15. Measured power efficiency under (a) $V_I$ = 400 V and $F_{SW}$ = 1 MHz and (b) $V_I$ =150 V and $F_{SW}$ = 2 MHz.

Table 3.1. Performance comparisons of state-of-the-art isolated ZVS converters

| | VICOR V300C48C150BL [1] | MPS HFC0100 [45] | **This work** |
|---|---|---|---|
| $V_I$ [V] | 180 – 375 DC | 85 – 265 AC | **150 – 400 DC** |
| $V_O$ [V] | 48 | 24 | **48** |
| Max $P_{OUT}$ [W] | 150 | 120 | **250** |
| $F_{SW}$ [kHz] | Not reported | 140 | **Up to 2000** |
| Power switch | MOSFET | MOSFET | **650V GaN** |
| Switching method | ZVS | ZVS | **ZVS** |
| Gate driving Method | Isolated gate driver w/ transformer | Integrated driver for low-side FET | **Integrated synchronous driver for high- and low-side FETs** |
| ZVS detection and adaptive dead time control | Not available | Auxiliary winding based valley detection | **Integrated $V_{SW}$ slew rate detection** |
| ZVS turn-on delay [ns] | Not available | 100 | **13** |
| Peak power efficiency | 88.2% | 90.5% (220VAC, 1.5A) | **90.2% (150V, 2MHz, 4A) 88.6% (400V, 1MHz, 3.3A)** |

## 3.5 Conclusions

A 1 – 2-MHz 150 – 400-V isolated full-bridge phase-shifted DC-DC bus converter with near-optimum adaptive dead-time control has been introduced, discussed and validated in this chapter. With the proposed monolithic SS-ZVSD, the gate driver is able to support both full- and partial-ZVS operations with 13-ns (6-ns) delay for high-side (low-side) eGaN FETs and adaptively adjust the dead time to minimize the converter switching power loss and the reverse conduction loss of eGaN FETs at the same time. The differential-mode noise blanking scheme is also developed in the level shifter to blank common-mode noise and only pass differential pulses from low-side to high-side domain, thereby improving dv/dt immunity to 45 V/ns at switching nodes. Proper operation and performance of the proposed ZVS driver has been validated with the full-bridge converter in experiments. Compared to state-of-the-art counterparts, the proposed driver enables application of eGaN FETs in MHz ZVS operation and helps achieve comparable power efficiency with 14 times higher switching frequency in the converter.

# CHAPTER 4

# MULTIPHASE ZVS CONVERTERS WITH AUXILIARY COMPONENTS REDUCTION [1]

## 4.1 Overview

In addition to the isolated high-voltage converters, non-isolated converters tend to handle higher and higher input/output voltage. Nowadays, it is not uncommon for a non-isolated converter to operate under 80-100V [46]. In this situation, zero-voltage switching technique is important to reduce the switching loss and maintain high efficiency with high frequency operation. However, for any non-isolated power converter topology, the efficiency benefit of zero-voltage switching technique comes with the penalty of increased cost and board volume due to its required auxiliary components. Typically, in a non-isolated power converter (i.e. buck, boost, inverting buck-boost and etc.), there is only one active FET associated to only one switch node which needs ZVS assistance from one branch of the auxiliary circuitry [7, 32]. However, in multi-phase buck converters, there are multiple active FETs, and each of them needs ZVS assistance. In [26, 27], one dedicated branch of auxiliary circuitry is deployed to assist ZVS operation of each phase in the multiphase converter. Such deployment increases not only the cost and volume of the auxiliary components, but also the power loss associated with the auxiliary branches, which eventually limits the application of ZVS technique in complex non-isolated topologies. To solve this issue, in Section 4.2, a novel two-phase QSW-ZVS technique is proposed and generalized in multi-phase converters to reduce the cost and volume of the auxiliary components while maintain similar power efficiency.

[1] Adapted from: L. Cong and H. Lee, High-voltage high-frequency non-isolated DC-DC converters with passive-saving two-phase QSW-ZVS technique, Analog Integrated Circuits and Signal Processing, published 2016, Springer.

## 4.2 High-Voltage High-Frequency Non-isolated Multi-Phase DC-DC Converters with Two-Phase QSW-ZVS Technique

### 4.2.1 Proposed Two-Phase QSW-ZVS Cell

The traditional two-phase QSW-ZVS converter is shown as in Figure 4.1. For evaluating power losses, three assumptions are used to simplify the calculation as follows: (1) $I_{LMA} = I_{LMB} = 0.5*I_{LOAD}$, where $I_{LMA}$ and $I_{LMB}$ are main inductor currents; (2) The peak current in the auxiliary branches is just enough for assisting ZVS operation, that is, $I_{AP} = 0.5*I_{LOAD}$; and (3) all power FETs have the same on-resistance $R_{on}$ that is independent of their drain currents $I_{D,MLA}$, $I_{D,MHA}$, $I_{D,MLB}$, $I_{D,MHB}$. Hence, based on Figure 4.1(b) and [47, 48], conduction losses of power FETs and auxiliary inductors ($P_{C2,FETs}$ and $P_{C2,Ind}$), and the core loss of the auxiliary inductors ($P_{Core2}$) in the traditional two-phase ZVS cell at the duty ratio of 0.5 are given as

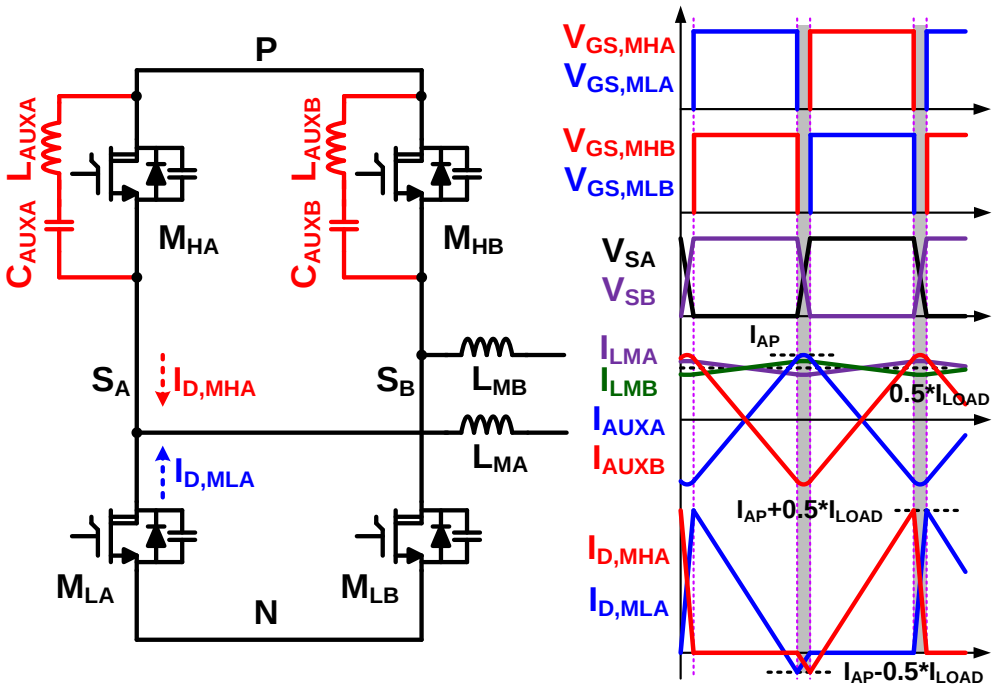
$$P_{C2,FETs} \approx \frac{2}{T_S}\left[\int_0^{0.5T_S} I_{D,MHA}^2 R_{on} dt + \int_{0.5T_s}^{T_s} I_{D,MLA}^2 R_{on} dt\right] = \frac{2}{3} I_{LOAD}^2 R_{on} \tag{4-1}$$

$$P_{C2,Ind} \approx \frac{2}{T_S}\int_0^{T_S} I_{AUXA}^2 R_{wind} dt = \frac{1}{6} I_{LOAD}^2 R_{wind} \tag{4-2}$$

$$P_{Core2} \approx 2k_1 F_{SW}^x (0.5 I_{LOAD})^y \quad . \tag{4-3}$$

However, this traditional two-phase topology requires a dedicated ZVS branch for each phase and thus needs 2 auxiliary inductors and 2 auxiliary capacitors totally. To reduce the required number of passive components and further decrease the core and conduction losses of the auxiliary inductors, a new ZVS cell is developed for the two-phase topology and its structure is shown in Figure 4.2 (a). In contrast to the traditional two-phase structure, the proposed passive-saving two-phase ZVS (PS-TPZVS) cell only requires one auxiliary branch ($L_{AUX}$ and $C_{AUX}$)

connecting between two switching nodes $S_A$ and $S_B$. The auxiliary branch injects transient currents into nodes $S_A$ and $S_B$ during their respective dead times to enable ZVS of all power FETs.




(a) (b)

Figure 4.1. (a) structure and (b) timing diagram of a traditional two-phase ZVS cell.

To understand the function of the transient current in the PS-TPZVS cell, a buck converter is adopted here for explanation as shown in Figure 4.2 (a). Figures 4.2 (b), (c) and (d) show the key waveforms of a PS-TPZVS buck converter with the duty ratio ($D$) of 0.5, $< 0.5$ and $\geq 0.5$, respectively. The two phases of the power stage are controlled by two PWM signals from the controller with the same duty ratio but 180° out of phase. A pair of non-overlapping gate drive signals (i.e. $V_{GS,MH*}$ and $V_{GS,ML*}$) is then generated from each PWM signal for the high-side and low-side power FETs in each phase. With the two switching-node voltages ($V_{SA}$ and $V_{SB}$) 180°

out of phase, current in the auxiliary branch is alternating between its positive and negative peak values. During switching transitions, the positive (negative) peak of auxiliary current $I_{AUX}$ would be used to charge the parasitic capacitance at node $S_A$ ($S_B$) to establish ZVS for $M_{HA}$ ($M_{HB}$). On the other hand, the summation of the main inductor current $I_{LMA}$ ($I_{LMB}$) and $I_{AUX}$ would discharge voltage $V_{SA}$ ($V_{SB}$) to enable ZVS of the low-side power FET $M_{LA}$ ($M_{LB}$) during the dead-time. Without loss of generality, similar ZVS operation could also be achieved in boost and buck-boost converter topologies with the use of the PS-TPZVS cell.

According to Figure 4.2 (b) for D=0.5 case, the conduction losses of power FETs and the auxiliary inductor ($P_{C2PS,FETs}$ and $P_{C2PS,Ind}$) and the core loss of the auxiliary inductor ($P_{Core2PS}$) are calculated with the same assumptions for obtaining (4-1) – (4-3) and given as

$$P_{C2PS,FETs} \approx \frac{2}{T_S}[\int_0^{0.5T_S} I_{D,MHA}^2 R_{on} dt + \int_{0.5T_s}^{T_s} I_{D,MLA}^2 R_{on} dt] = \frac{2}{3} I_{LOAD}^2 R_{on} \quad (4\text{-}4)$$

$$P_{C2PS,Ind} \approx \frac{1}{T_S}\int_0^{T_S} I_{AUXA}^2 R_{wind} dt = \frac{1}{12} I_{LOAD}^2 R_{wind} \quad (4\text{-}5)$$

$$P_{Core2PS} \approx k_1 F_{SW}^x (0.5 I_{LOAD})^y \quad . \quad (4\text{-}6)$$

Comparing (4-4) – (4-6) with (4-1) – (4-3), both core loss and conduction loss of the auxiliary inductor in the proposed PS-TPZVS cell are lower than those of the traditional two-phase ZVS topology by 50%, while the conduction loss of the power FETs in both topologies are the same. Hence, the power efficiency of the proposed PS-TPZVS topology can be higher than that of the traditional two-phase counterpart.

It should also be noted that the proposed PS-TPZVS cell can be extended into a *2N*-phase converter with *N* identical two-phase cells connected in parallel as shown in Figure 4.2 (e) such

that only *N* auxiliary branches are required. Both the required numbers of auxiliary branches and passive components are thus reduced by 50% compared to the generic multi-phase counterparts.

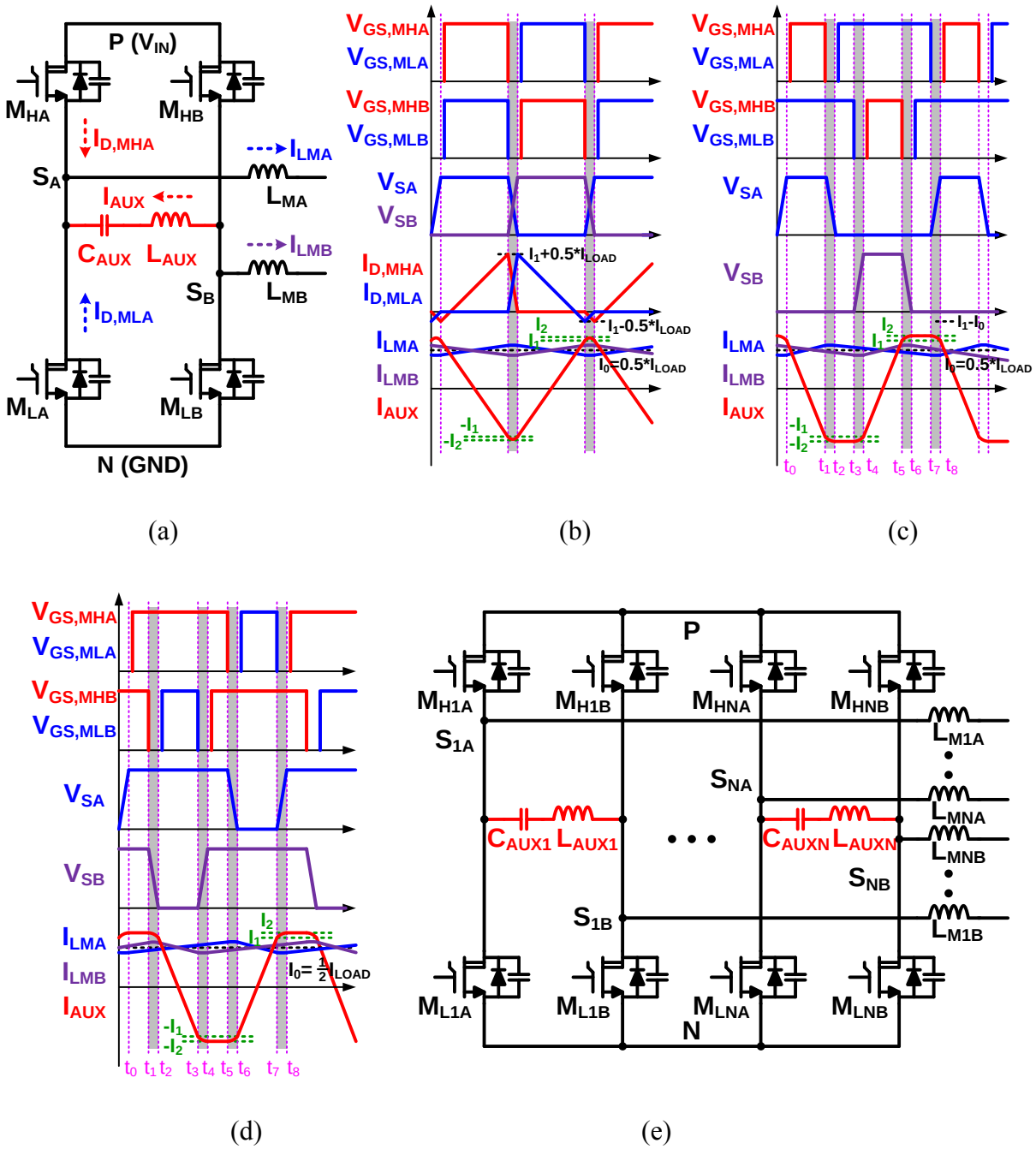



Figure 4.2. (a) Proposed PS-TPZVS cell; timing diagram of the PS-TPZVS cell under (b) D = 0.5, (c) D < 0.5 and (d) D > 0.5; and I 2N-phase PS-TPZVS cell.

### 4.2.2 Operation Principles

To analyze the ZVS operation of the proposed PS-TPZVS buck converter in detail, an equivalent circuit with two sub-converters A and B shown in Figure 4.3 is used. There exist two dynamic circuit operation sequences shown in Figures 4.3 and 4.4 corresponding to the timing diagrams of Figure 4.2 (e) (for $D < 0.5$) and Figure 4.3 (d) (for $D \geqslant 0.5$), respectively. Three assumptions are made to simplify the circuit analysis.

(1) All circuit components are ideal; i.e. the on-resistance of power FETs ($M_{HA}$, $M_{LA}$, $M_{HB}$, $M_{LB}$), parasitic resistance of inductors ($L_{MA}$, $L_{MB}$, $L_{AUX}$), the ESR of capacitors ($C_O$, $C_{AUX}$) are neglected.

(2) Output capacitor $C_O$ and auxiliary capacitor $C_{AUX}$ are sufficiently large, so the voltages across them are considered to be constant.

(3) Parameters of sub-converter A perfectly match with those of sub-converter B.

The proposed PS-TPZVS buck converter operates in continuous conduction mode for both small inductor current ripple and low core loss considerations under high load-current condition. There are 8 sub-intervals in a switching period for both $D < 0.5$ and $D \geqslant 0.5$ and their operations are described below.

**1. For the case of D < 0.5**

*Subinterval 1 (Figure 4.3 (a)) [$t_0 - t_1$]*: At $t_0$, $M_{HA}$ is turned on while $M_{LB}$ remains in the on state. So, $V_{SA}$ equals $V_{IN}$, and $V_{SB}$ is about 0. The input voltage $V_{IN}$ is applied across $L_{AUX}$ and the current $I_{AUX}$ is linearly decreased from a predefined level $I_1$ to $-I_1$ at the end of $t_1$ shown in Figure 4.2 (c), where positive $I_{AUX}$ is defined as the current flowing from node $S_B$ to node $S_A$. Current $I_{AUX}$ would be used to establish ZVS for $M_{HB}$ in subinterval 4 and for $M_{HA}$ in subinterval

8. Note that the value of $I_1$ is designed to be larger than the average main inductor current $I_0$ via selecting a proper value for $L_{AUX}$.

*Subinterval 2 (Figure 4.3 (b)) [$t_1 - t_2$]*: power FET $M_{HA}$ is turned off at $t_1$, while both auxiliary current $I_{AUX}$ and main inductor current $I_{LMA}$ flow out of the node $S_A$. The current sum $I_{SA}$ (= $I_{AUX}$ + $I_{LMA}$) discharges the parasitic capacitance at node $S_A$ until voltage $V_{SA}$ falls to zero at $t_2$. Values of $V_{SA}$ and $I_{AUX}$ are given as

$$V_{SA}(t) = V_{IN}\cos\omega_0(t-t_1) - (I_0 + I_1)Z_0\sin\omega_0(t-t_1) \tag{4-7}$$

$$I_{AUX}(t) = -(I_0 + I_1)\cos\omega_0(t-t_1) - \frac{V_{IN}}{Z_0}\sin\omega_0(t-t_1) + I_0 \tag{4-8}$$

where $C_S$ is the equivalent capacitance at either switching node ($S_A$ or $S_B$), $\omega_0 = 1/\sqrt{L_{AUX}C_S}$, and $Z_0 = \sqrt{\frac{L_{AUX}}{C_S}}$. At $t_2$, $I_{AUX}$ resonates to its negative peak value ($-I_2$) and, solving (4-7) and (4-8), $I_2$ is given as

$$I_2 = \sqrt{(I_0 + I_1)^2 + (\frac{V_{IN}}{Z_0})^2} - I_0 \tag{4-9}$$

*Subinterval 3 (Figure 4.3 (c)) [$t_2 - t_3$]*: The gate-to-source voltage of $M_{LA}$ starts to increase after $t_2$ and turns on $M_{LA}$ under the ZVS condition. The auxiliary inductor freewheels as both $M_{LA}$ and $M_{LB}$ are on, and nodes $S_A$ and $S_B$ are connected to ground potential. The auxiliary current $I_{AUX}$ keeps at its negative peak value in this interval as shown in Figure 4.3 (c).

*Subinterval 4 (Figure 4.3 (d)) [$t_3 - t_4$]*: $M_{LB}$ is turned off at $t_3$ while $I_{AUX}$ flows into node $S_B$ and $I_{LMB}$ flows out of $S_B$. The current difference $I_{SB}$ (= $I_{AUX}$ – $I_{LMB}$) charges the parasitic capacitance at node $S_B$ until $V_{SB}$ rises to $V_{IN}$ at $t_4$. During this interval, both $V_{SB}$ and $I_{AUX}$ are given as

$$V_{SB}(t) = (I_2 - I_0) Z_0 \sin \omega_0 (t - t_3) \tag{4-10}$$

$$I_{AUX}(t) = -(I_2 - I_0) \cos \omega_0 (t - t_3) - I_0 \tag{4-11}$$

*Subinterval 5 (Figure 4.3 (e)) [$t_4$ – $t_5$]*: The gate-to-source voltage $V_{GS,MHB}$ of $M_{HB}$ starts to increase and turns on $M_{HB}$ after $t_4$ to establish ZVS for $M_{HB}$. When $M_{LA}$ and $M_{HB}$ are both on, $S_A$ and $S_B$ are connected to ground and $V_{IN}$, respectively, so $I_{AUX}$ increases linearly from $-I_1$ to $I_1$, as shown in Figure 4.2 (e).

*Subinterval 6 (Figure 4.3 (f)) [$t_5$ – $t_6$]*: $M_{HB}$ is turned off at $t_5$ while both $I_{AUX}$ and $I_{LMB}$ flow out of node $S_B$. The current sum $I_{SB}$ discharges the parasitic capacitance at node $S_B$ until $V_{SB}$ falls to zero and $I_{AUX}$ resonates to its positive peak value $I_2$ at $t_6$. During this interval, both $V_{SB}$ and $I_{AUX}$ are given as

$$V_{SB}(t) = V_{IN} \cos \omega_0 (t - t_5) - (I_0 + I_1) Z_0 \sin \omega_0 (t - t_5) \tag{4-12}$$

$$I_{AUX}(t) = (I_0 + I_1) \cos \omega_0 (t - t_5) + \frac{V_{IN}}{Z} \sin \omega_0 (t - t_5) - I_0 \tag{4-13}$$

*Subinterval 7 (Figure 4.3 (g)) [$t_6$ – $t_7$]*: The gate-to-source voltage $V_{GS,MLB}$ is controlled to increase and turn on $M_{LB}$ under ZVS condition after $t_6$.The auxiliary inductor freewheels as both $M_{LA}$ and $M_{LB}$ are on and both nodes $S_A$ and $S_B$ are connected to ground potential. The value of $I_{AUX}$ keeps at its positive peak $I_2$ in this interval as shown in Figure 4.2 (e).

*Subinterval 8 (Figure 4.3 (h)) [$t_7$ – $t_8$]*: $M_{LB}$ is turned off at $t_7$, while $I_{AUX}$ flows into $S_A$ and $I_{LMA}$ flows out of $S_A$. The current difference $I_{SA}$ (= $I_{AUX}$ – $I_{LMA}$) charges the parasitic capacitance at node $S_A$ until $V_{SA}$ rises to $V_{IN}$ at $t_8$. Both $V_{SA}$ and $I_{AUX}$ are given as

$$V_{SA}(t) = (I_2 - I_0) Z_0 \sin \omega_0 (t - t_7) \tag{4-14}$$

$$I_{AUX}(t) = (I_2 - I_0) \cos \omega_0 (t - t_7) + I_0 \tag{4-15}$$

After $t_8$, the gate-to-source voltage $V_{GS,MHA}$ shown in Figure 4.2 (e) will then be controlled to increase and turn on $M_{HA}$ under the ZVS condition, and the operation sequence will repeat again from subinterval 1 to subinterval 8 in the next switching period.

Note that proper ZVS operation of power FETs in the proposed PS-TPZVS cell does not require accurate dead-time matching of power FETs in two branches. Without loss of generality, the ZVS operation of $M_{HB}$ is taken as an example for illustration. After $M_{LB}$ is turned off at $t_3$, the switching node voltage $V_{SB}$ rises in a sinusoidal form according to (4-10). When $V_{SB}$ reaches $V_{IN}$, $V_{SB}$ gets clamped by the body diode of $M_{HB}$ at $t_4$. The body diode keeps the drain-to-source voltage of $M_{HB}$ at around zero, and $M_{HB}$ can be turned on under the ZVS condition even if the dead-time is extended for a few ns after $t_4$ due to, for example, turn-on delay of the gate driver. ZVS turn-on of other power FETs is similar as that of $M_{HB}$ and mismatch in dead-time of two branches would not affect the operation of the proposed PS-TPZVS cell.

Moreover, mismatch in dead-time resulting from rise/fall time of switching-node voltages or gate-drive signals will not affect the proper operation as well because each dead-time slot establishes ZVS of one power FET only as shown in Figure 4.2 (e). Four power FETs in the proposed PS-TPZVS cell achieve ZVS in different dead-time slots in one switching period of $I_{AUX}$.

**2. For the case of $D \geqslant 0.5$**

Figure 4.2 (d) shows the timing diagram of the PS-TPZVS buck converter when $D \geqslant 0.5$. Comparing Figure 4.2 (d) with Figure 4.2 (c), the operation of the converter for $D \geqslant 0.5$ is similar to the case of $D < 0.5$ and ZVS for power FETs will also occur at times $t_2$, $t_4$, $t_6$, and $t_8$. In contrast to the case of $D < 0.5$, the auxiliary inductor freewheeling occurs in time intervals [$t_0$ –

$t_1$] and [$t_4 - t_5$] for D > 0.5 as shown in Figure 4.4. For D = 0.5, the time interval for the auxiliary inductor freewheeling is decreased to 0 and a triangular waveform for $I_{AUX}$ is obtained. As shown in Figure 4.2 (d), ZVS operation for all the power FETs is also ensured by the proposed PS-TPZVS cell for D $\geqslant$ 0.5 cases.

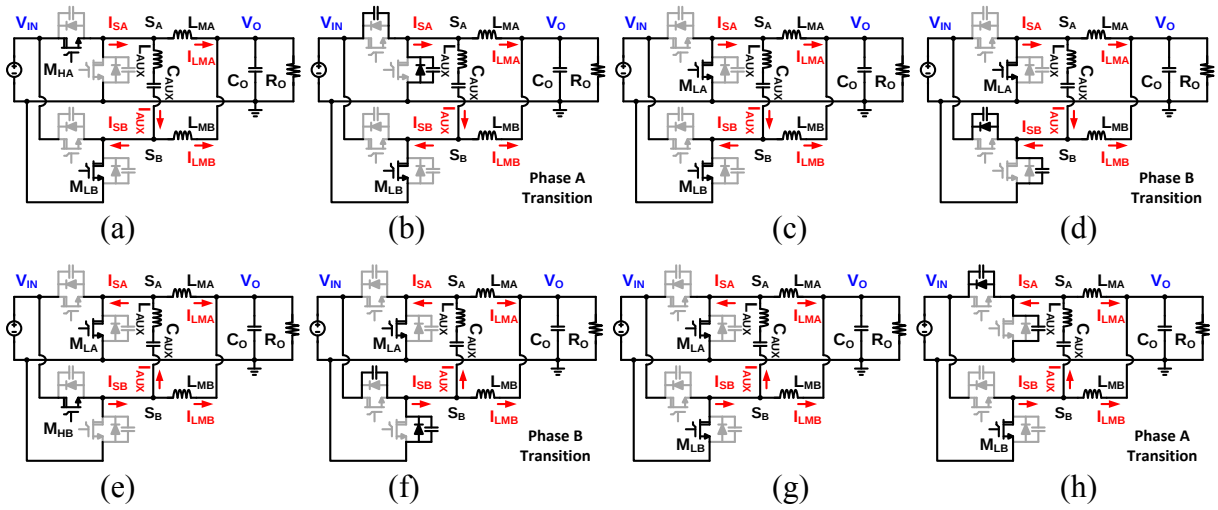



Figure 4.3. Equivalent circuit of the PS-TPZVS buck converter and its operation for D < 0.5 during intervals (a) [$t_0$-$t_1$], (b) [$t_1$-$t_2$], (c) [$t_2$-$t_3$], (d) [$t_3$-$t_4$], (e) [$t_4$-$t_5$], (f) [$t_5$-$t_6$], (g) [$t_6$-$t_7$], and (h) [$t_7$-$t_8$].

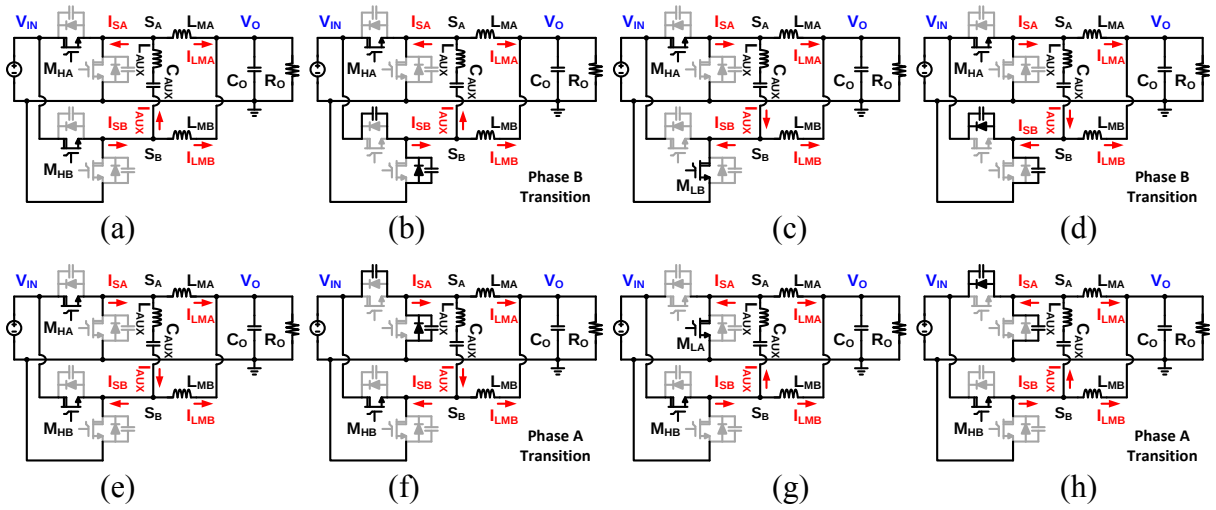



Figure 4.4. Equivalent circuit of the PS-TPZVS buck converter and its operation for D $\geq$ 0.5 during intervals (a) [$t_0$-$t_1$], (b) [$t_1$-$t_2$], (c) [$t_2$-$t_3$], (d) [$t_3$-$t_4$], (e) [$t_4$-$t_5$], (f) [$t_5$-$t_6$], (g) [$t_6$-$t_7$], and (h) [$t_7$-$t_8$].

### 4.2.3 Performance Verifications and Discussions

A two-phase buck converter prototype [28, 49] as shown in Figure 4.5 is built to verify the proposed PS-TPZVS cell with an on-chip PWM controller based on a Type-III compensator [50] and a synchronous gate driver. Both the controller and the on-chip gate driver are realized in a 0.35-μm HV CMOS technology. The two-phase synchronous buck converter can be configured to an output voltage from 24 V to 48 V with the input voltage varying between 72 V and 100 V at a 4-MHz switching frequency. To demonstrate the performance of the proposed PS-TPZVS technique, both 150-V enhancement-mode GaN (eGaN) (EPC2018 [51]) and 150-V MOSFET (FDMS86255 [52]) are used in the converter prototype. The value of $L_{AUX}$ is chosen to be 1.2 μH in the designed converter such that the amplitude of the auxiliary current is 2.1 A and is larger than the average inductor current of 1.5 A for establishing full ZVS for all power switches under different conditions. Table 4.1 provides the performance comparisons between the proposed PS-TPZVS buck converter prototype and the traditional two-phase ZVS counterpart. By saving one auxiliary inductor and one auxiliary capacitor, the volumes of the auxiliary passives and the total passives in the proposed PS-TPZVS converter are reduced by 2 times and 1.4 times, respectively, as compared to the traditional two-phase counterpart by. In addition, the proposed PS-TPZVS converter provides higher peak power efficiencies than the traditional counterpart with both eGaN FETs and power MOSFETs.

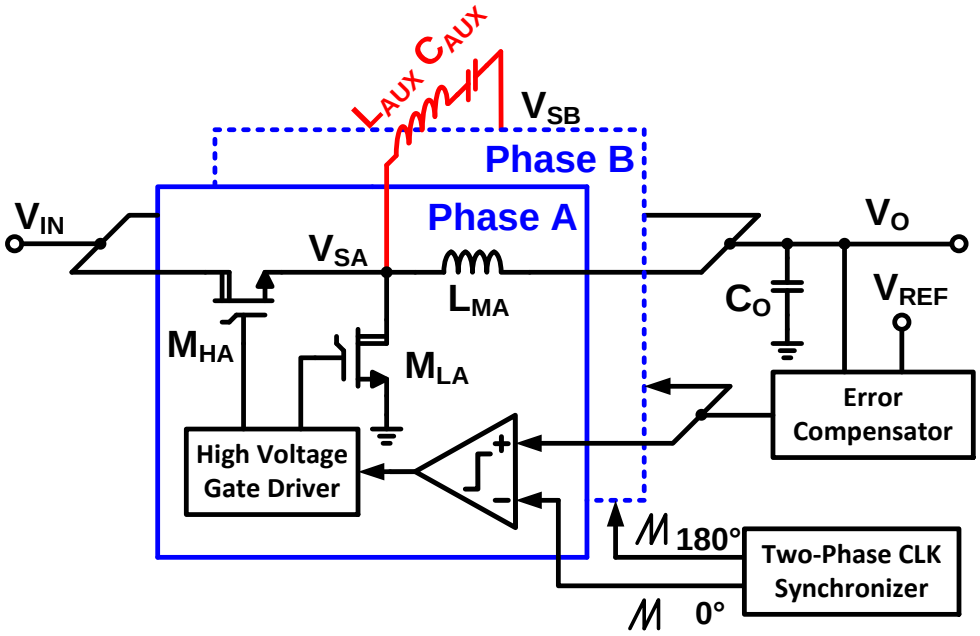



Figure 4.5. Schematic of the PS-TPZVS buck converter.

Table 4.1. Performance comparisons between the proposed PS-TPZVS and the traditional two-phase ZVS buck converters

| | Traditional Two-Phase ZVS | Proposed PS-TPZVS |
|---|---|---|
| Supply voltage ($V_{IN}$) | 72 V – 100 V | 72 V – 100 V |
| Output voltage ($V_O$) | 24 V – 48 V | 24 V – 48 V |
| Maximum output power | 144 W | 144 W |
| Inductor values and count | $L_M$: 5.6 µH x 2 (MSS1278-562)<br>$L_{AUX}$: 0.9 µH x 2 (SER2010-901) | $L_M$: 5.6 µH x 2 (MSS1278-562)<br>$L_{AUX}$: 1.2 µH (SER2010-122) |
| Capacitor values and count | $C_O$: 8.8 µF [1]<br>$C_{AUX}$: 0.47 µF [2] x 2 | $C_O$: 8.8 µF [1]<br>$C_{AUX}$: 0.47 µF [2] |
| Volume of auxiliary passives [3] | 3420 mm$^3$ | 1710 mm$^3$ |
| Total volume of passive components [3] | 6020 mm$^3$ | 4310 mm$^3$ |
| Power switches | EPC2018 (150-V eGaN) &<br>FDMS86255 (150-V MOSFET) | EPC2018 (150-V eGaN) &<br>FDMS86255 (150-V MOSFET) |
| Switching frequency | 4 MHz | 4 MHz |
| Max. power efficiency | 96% (eGaN FETs)<br>94.2% (MOSFETs) | 96.9% (eGaN FETs)<br>94.8% (MOSFETs) |

[1] $C_O$: C4532X7R2A225K230KA x 4. [2] $C_{AUX}$: C4532X7R2E474K230KA.

[3] Volume of passive components is calculated based on obtained dimension data from datasheets. Volume of an SER2010 inductor is about 1670 mm$^3$ and volume of a 0.47 µF capacitor is around 40 mm$^3$. Volume of an MSS1278 inductor is about 1220 mm$^3$ and total volume of $C_O$ is around 160 mm$^3$.

Figures. 4.6 (a) and (b) provide the steady-state waveforms of the proposed two-phase buck converter and verify proper operation of the converter under (1) different duty ratios at 4-MHz switching frequency and (2) the input voltage as high as 100 V. The simulated steady-state inductor currents of the traditional two-phase ZVS converter are provided in Figures 4.6 (c) and (d) for comparison purposes. With the use of only one auxiliary current $I_{AUX}$ in the proposed PS-TPZVS buck converter and the ripple amplitude of $I_{AUX}$ shown in Figure 4.6 (a) (or Figure 4.6 (b)) being approximately the same as that of auxiliary currents $I_{AUXA}$ and $I_{AUXB}$ in the traditional two-phase ZVS converter shown in Figure 4.6 (c) (or Figure 4.6 (d)), the proposed PS-TPZVS converter would thus have lower core loss and conduction loss of the auxiliary inductor than the traditional two-phase ZVS converter.

Figure 4.7 demonstrates ZVS operation of the proposed converter with eGaN power FETs under two extreme cases (minimum and maximum duty ratios in Figure 4.7 (a) and (b), respectively). In both figures, voltages $V_{SA}$ and $V_{SB}$ rise to $V_{IN}$ before turning on the corresponding high-side power FETs $M_{HA}$ and $M_{HB}$. Similarly, $V_{SA}$ and $V_{SB}$ fall to zero before the low-side power FETs $M_{LA}$ and $M_{LB}$ are turned on. Hence, the simulated results prove the theoretical analysis shown in Figures 4.2 – 4.4 and verify that the ZVS of all power FETs is achieved during switching transitions.

Figure 4.8 (a) provides the simulated power efficiencies of the proposed PS-TPZVS buck converter using EPC2018 under different duty ratios. The peak power efficiency of 96.9% is achieved at full load and a switching frequency of 4 MHz. The converter prototype demonstrates

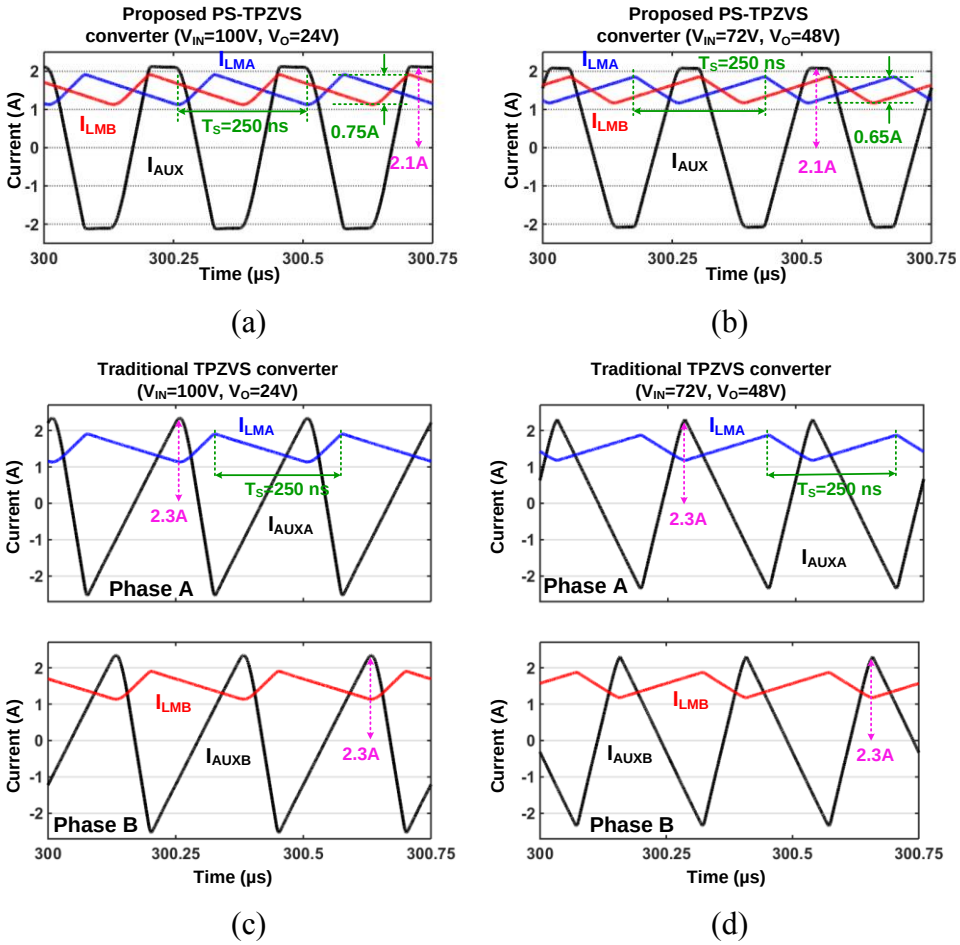



Figure 4.6. Simulated steady-state waveforms of the proposed PS-TPZVS converter under the full load of 3A: main inductor currents and auxiliary inductor current under (a) $V_{IN}$ = 100 V, $V_O$ = 24 V and (b) $V_{IN}$ = 72 V, $V_O$ = 48 V. The simulated main inductor current and the auxiliary inductor current of the traditional two-phase ZVS converter are provided in (c) and (d) with the same conditions of (a) and (b), respectively.

higher power efficiencies in two cases ($V_{IN}$ = 72 V, $V_O$ = 48 V; $V_{IN}$ = 100 V, $V_O$ = 24 V) than the other case ($V_{IN}$ = 100 V, $V_O$ = 48 V) because the current ripple of the auxiliary inductor increases as the duty ratio approaches 0.5. Figures 4.8 (b) and (c) provide comparisons of simulated power efficiencies of the proposed PS-TPZVS buck converter, the single-phase ZVS converter, and the traditional two-phase ZVS converter using both types of power FETs EPC2018 and FDMS86255. All the converters are configured as $V_{IN}$ = 100 V and $V_O$ = 24 V.

Both the traditional two-phase ZVS and proposed PS-TPZVS converters achieve higher power efficiencies across the entire load-current range than the single-phase ZVS counterpart due to the smaller amplitude of the current ripple of the auxiliary inductor and thus smaller conduction and core losses. Compared with the traditional two-phase ZVS converter, the proposed PS-TPZVS converter achieves better power efficiency under different load currents due to the saving of one auxiliary inductor and thus the reduction in the associated conduction and core losses. Specifically, for eGaN FETs, the proposed PS-TPZVS converter provides power efficiency improvements of around 0.7% and 1.2% as compared to the traditional two-phase ZVS and single-phase ZVS converters, respectively. It indicates that a total of 0.5-W – 0.9-W loss can be saved from 72-W output power with the proposed PS-TPZVS architecture.

Figure 4.9 (a) shows the simulated load transient response of the proposed PS-TPZVS buck converter with a load step changing between 0.6 A and the full load of 3 A. The output undershoots and overshoots are within 185 mV (0.39% of $V_O$ = 48 V) using a ceramic output capacitor of 8.8 µF. The output transient recovery time is within 10 µs. Figure 4.9 (b) provides the simulated transient response of the traditional two-phase ZVS buck converter with the same controller as the proposed converter for performance comparisons. The proposed PS-TPZVS converter and the traditional two-phase ZVS converter have similar load transient responses in terms of the settling time, and the transient undershoots and overshoots of the output voltage. In addition, for the converter robustness consideration, each power transistor in the proposed converter is selected in the design phase to ensure its drain-to-source voltage and gate-to-source voltage being always lower than their corresponding maximum allowable values during the load step change.

Table 4.2 provides performance comparisons of different high-voltage buck converters with similar output power. Compared to other state-of-the-art counterparts, the proposed PS-TPZVS buck converter is able to increase the switching frequency by at least 16 times while still providing comparable or better peak power efficiency. With much higher switching frequency, both the required values of the output capacitor and the normalized main inductors are significantly smaller in the proposed PS-TPZVS buck converter, thereby decreasing converter volume.

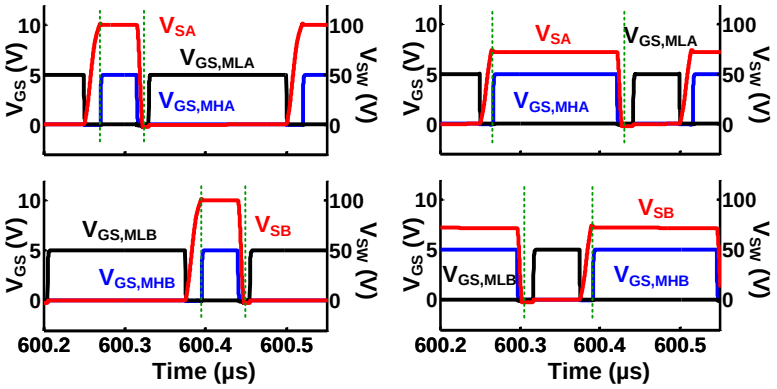



Figure 4.7. Simulated waveforms to demonstrate ZVS operation of the proposed converter under (a) $V_{IN}$ = 100 V, $V_O$ = 24 V, $I_{OUT}$ = 3 A; and (b) $V_{IN}$ = 72 V, $V_O$ = 48 V, $I_{OUT}$ = 3 A.

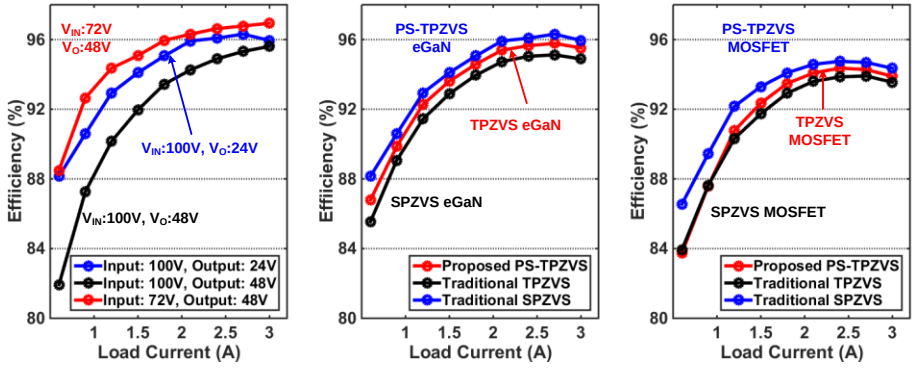



Figure 4.8. (a) Simulated power efficiency of the proposed converter vs load currents under different duty ratios (inductor core loss is included); and power efficiency comparisons among the proposed PS-TPZVS buck converter, the traditional single-phase ZVS converter, and the traditional two-phase ZVS converter under $V_{IN}$ = 100 V, $V_O$ = 24 V with (b) eGaN FETs and (c) power MOSFETs.

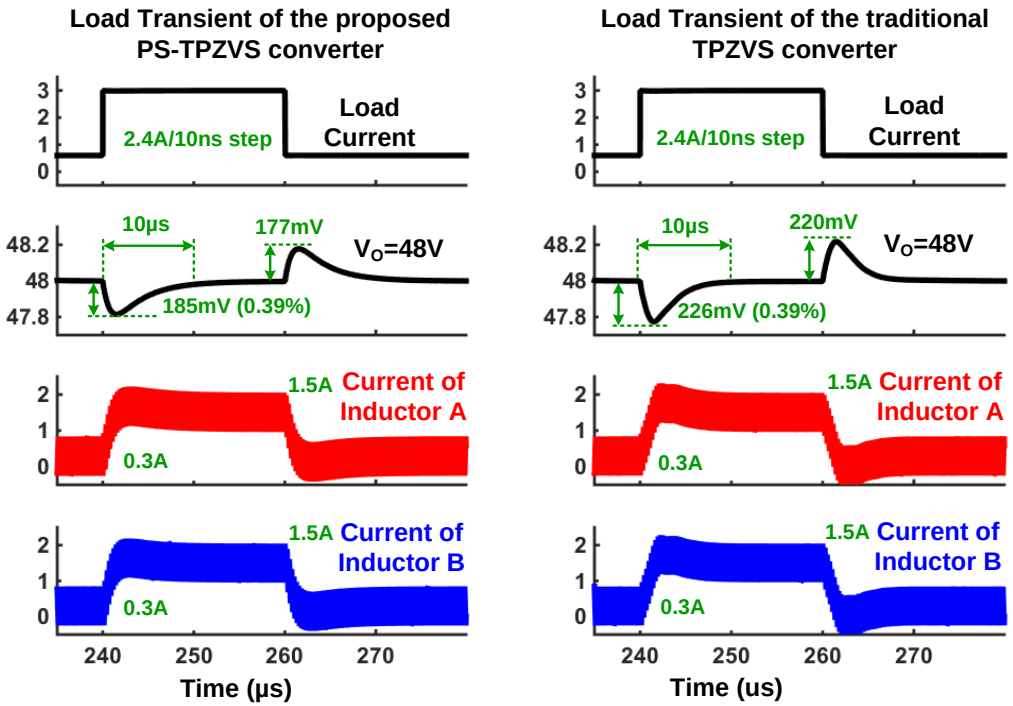



Figure 4.9. Simulated transient response of the proposed converter with a load step between 0.6 A and 3 A (load current slew rate: 2.4 A/ 10 ns) for (a) the proposed PS-TPZVS buck converter at 4 MHz and (b) traditional two-phase ZVS buck converter at 4 MHz.

Table 4.2. Performance comparisons of different high-voltage non-isolated DC-DC converters

| | LTC3810 2011 [53] | LM5117 2013 [54] | TPE 2010 [9] | TIE 2011 [55] | **This work[4]** |
|---|---|---|---|---|---|
| Topology | Single phase syn. Buck | Single phase syn. Buck | Single phase syn. Buck | Single phase syn. Buck | **Two phase syn. Buck** |
| $V_{IN}$ (V) | 15 – 100 | 15 – 55 | 80 | 48 | **72 – 100** |
| $V_O$ (V) | 12 | 12 | 30 | 24 | **24 – 48** |
| Max. output power (W) | 72 | 108 | 180 | 115 | **144** |
| Soft switching | No | No | ZVT via aux. FET and inductor | ZVS via coupled inductor | **PS-ZVS via aux. inductor** |
| Peak power efficiency | 93% [1] | 93% [2] | 96% | 94% | **96.9% (eGaN) 94.8% (MOS)** |
| Frequency (kHz) | 250 | 230 | 100 | 100 | **4000** |
| $L_M$ (μH) | 10 | 10 | 150 | 620 | **5.6 × 2** |
| Normalized $L_M$ (μH) [3] | 34 – 80 | 33 – 48 | 150 | 96 | **3.2 – 5** |
| $C_O$ (μF) | 270 | 525 | 100 | N. A. | **1 – 10** |

[1] Tested at 75-V input voltage; [2] Tested at 55-V input voltage; [3] Inductor values are normalized using the same current ripple in [9]; [4] Verified in simulation.

## 4.3 Conclusions

A passive-saving two-phase QSW-ZVS (PS-TPZVS) technique that simultaneously enables high power efficiency and high operation frequency in high-voltage non-isolated DC-DC converters is introduced, discussed and verified in this chapter. Connected between the two switching nodes, an auxiliary branch of passives in the proposed PS-TPZVS cell is simultaneously shared by two sub-converters to achieve ZVS for all power switches while saving one auxiliary inductor and one auxiliary capacitor as compared to the traditional two-phase QSW-ZVS converter. Hence, the proposed PS-TPZVS converter has smaller volume of total passives, lower core loss and conduction loss of the auxiliary inductor, and higher power efficiencies than the traditional two-phase QSW-ZVS counterpart. The proposed PS-TPZVS cell can also be used in other topologies of non-isolated DC-DC converters and extended to a *2N*-phase cell with only *N* additional ZVS-assisting branches. Simulation results verify that the proposed TPQSW-ZVS buck converter offers a peak power efficiency of ~97% at 4 MHz. Compared with state-of-the-art hard-switching and ZVS counterparts, the proposed PS-TPZVS converter achieves better power efficiency while running at a higher switching frequency. The values and volumes of passive components in the proposed converter are much smaller than those of other state-of-the-art converters.

# CHAPTER 5

# ZVT CONVERTERS WITH REDUCED NUMBER OF AUXILIARY COMPONENTS AND ADAPTIVE AUXILIARY CURRENT CONTROL FOR IMPROVED LIGHT-LOAD EFFICIENCY [1]

## 5.1 Overview

The efficiency of soft-switched non-isolated converters can be improved by using zero-voltage transition technique, which only activates the auxiliary circuitry at the vicinity of power FETs commutation. With shorter on-time and smaller RMS current in the auxiliary circuitry, the conduction loss and magnetic core loss in the auxiliary circuit can be significantly reduced [56 – 60]. With the advantage of better efficiency, ZVT converters are more preferred in the industry. This chapter demonstrates that the proposed auxiliary component sharing technique can also reduce the total number and volume of passive components in ZVT converters in Section 5.2.

In addition, in all the existing publication of ZVT converters, the on-time of the auxiliary branch is either pre-set or manually controlled. The downside of using fixed on-time of the auxiliary switch is that the power efficiency can be adversely impacted in light load condition since the auxiliary current does not scale with the load current. Therefore, in Section 5.3, an auxiliary current control scheme is proposed such that the auxiliary current ripple can be adaptively adjusted according to the load current or the peak current in the main loop. With this innovative control scheme, the power efficiency of the ZVT converters can be optimized in a wide range of load.

[1] © 2018 IEEE. Adapted, with permission, from L. Cong, J. Liu and H. Lee, A high-efficiency low-profile zero-voltage transition synchronous non-inverting buck-boost converter with auxiliary-component sharing, IEEE Transactions on Circuits and Systems I, 8/2018

## 5.2 Zero-Voltage-Transition Non-inverting Buck-boost Converter with Auxiliary-Component Sharing

The schematic of the proposed ZVT synchronous non- inverting buck-boost converter is shown in Figure 5.1. $M_1$, $M_2$, $M_3$, $M_4$ and $L_m$ form the basic non-inverting buck-boost topology. $M_a$, $D_a$ and $L_a$ form the auxiliary branch connected between $SW_1$ and $SW_2$ assisting ZVS operation of both $M_1$ and $M_2$. Similar to the traditional non-inverting buck-boost converter [61], the proposed converter operates in buck mode when $V_i >> V_o$ (i.e. $V_o$=48V and $V_i$>56V) and operates in buck-boost mode when $V_i \approx V_o$ (i.e. $V_o$=48V and 36V $\leq V_i \leq$ 56V). When operating in buck mode, $M_1$ and $M_3$ switches while $M_2$ is always off and $M_4$ is always on; when operating in buck-boost mode, all $M_1$ – $M_4$ switches with $M_1$ and $M_2$ in phase and $M_3$ and $M_4$ in phase.

### 5.2.1 Operation Principles of the Proposed Buck-Boost Converter

#### A. Operation Principles in Buck-Boost Mode

In the buck-boost operation mode, $M_1$ and $M_2$ are controlled by the same gate-drive signal with a duty ratio *D*, while $M_3$ and $M_4$ are controlled by the complementary gate-drive signal. If

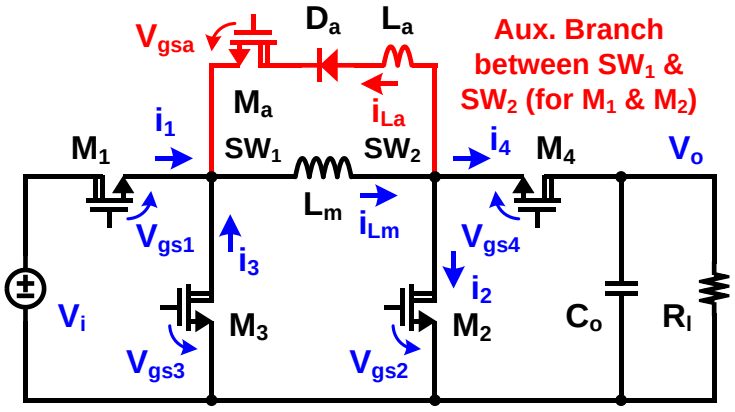



Figure 5.1. Schematic of the proposed ZVT synchronous non-inverting buck-boost converter with the shared auxiliary circuit.

the dead-time is neglected, the output voltage $V_o$ equals $V_i D/(1-D)$. In the proposed converter, the synchronous switches $M_3$ and $M_4$ can be turned on naturally under the zero-voltage condition with the assistance of the main inductor current $i_{Lm}$. ZVS operation of the active switches $M_1$ and $M_2$ requires an auxiliary current to charge the switching-node voltage $V_{sw1}$ to $V_i$ and discharge the switching-node voltage $V_{sw2}$ to 0, respectively, during the dead time. To minimize the count of auxiliary components in the proposed ZVT converter, charging $V_{sw1}$ and discharging $V_{sw2}$ are achieved by only a power switch $M_a$, a diode $D_a$ and an inductor $L_a$ connected between nodes $SW_1$ and $SW_2$. By turning on the auxiliary switch $M_a$ for a designated amount of time before the turn-off of $M_3$ and $M_4$, current $i_{La}$ of the auxiliary inductor flowing from $SW_2$ to $SW_1$ is increased to be larger than $i_{Lm}$ such that the current difference ($i_{La} - i_{Lm}$) charges $SW_1$ and discharges $SW_2$ in a resonant regime during the dead time. After $M_1$ and $M_2$ are turned on under zero-voltage condition, $i_{La}$ is decreased to zero and then $M_a$ is turned off to disable the auxiliary circuit.

The key timing waveforms and operation states are shown in Figures 5.2 and 5.3. Note that $M_1 - M_4$ can be realized by power MOSFETs or enhancement-mode GaN FETs (eGaNs). Since the reverse bias operation of eGaNs is similar to body diode of the power MOSFET, each power switch is added in parallel with a body diode and an output capacitor in Figure 5.3 for the operation analysis. Detailed descriptions of each time interval in a complete switching period are provided as follows with three assumptions: 1. Input and output voltage ripples are negligible; 2. the main inductor current $i_{Lm}$ is relatively constant as $I_{avg}$ in the switching period; and 3. all the power switches and diodes are ideal. It should also be noted that the duration from $t_1$ to $t_7$ is

intentionally enlarged in Figure 5.2 for clear illustration. In reality, the conduction time of the auxiliary switch only accounts for a small portion of the switching period.

*Subinterval 1 (Figure 5.3(a)) [$t_0 - t_1$]*: $M_3$ and $M_4$ are in the on-state, while $M_1$ and $M_2$ are in the off-state. The auxiliary circuit is disabled during this interval. The main inductor current $i_{Lm}$ goes through $M_3$ and $M_4$ to supply the load.

*Subinterval 2 (Figure 5.3(b)) [$t_1 - t_2$]*: $M_a$ is turned on at $t_1$, while $M_3$ and $M_4$ are still in the on-state during this interval. Since $V_o$ is applied across the auxiliary inductor $L_a$, $i_{La}$ increases linearly from 0 towards $i_{Lm}$, and thus the currents ($i_{M3}$ and $i_{M4}$) through $M_3$ and $M_4$ decrease to 0. Because $M_a$ is turned on under the zero-current condition, the switching loss of $M_a$ is negligible.

*Subinterval 3 (Figure 5.3(c)) [$t_2 - t_3$]*: $M_a$, $M_3$ and $M_4$ stay in the on-state, while $M_1$ and $M_2$ are in the off-state. $I_{La}$ continues to increase so as to be larger than $i_{Lm}$ until it reaches a pre-defined value $I_1$ at $t_3$, and both $i_{M3}$ and $i_{M4}$ change to negative according to the polarity definition in Figure 5.1.

*Subinterval 4 (Figure 5.3(d)) [$t_3 - t_4$]*: $M_3$ and $M_4$ are turned off at $t_3$, and the current difference ($i_{La} - i_{Lm}$) charges nodes $SW_1$ and discharges $SW_2$ at the same time. If the parasitic capacitance at each switching node is assumed to be the same as $C_p$, the resonance of $i_{La}$, $V_{sw1}$ and $V_{sw2}$ is then given as

$$i_{La} = (I_1 - I_{avg})\cos\omega_0(t - t_3) + \frac{V_o}{Z_0}\sin\omega_0(t - t_3) + I_{avg} \tag{5-1}$$

$$V_{sw1} = \frac{(I_1 - I_{avg})Z_0}{2}\sin\omega_0(t - t_3) - \frac{V_o}{2}\cos\omega_0(t - t_3) + \frac{V_o}{2} \tag{5-2}$$

$$V_{sw2} = \frac{V_o}{2} - \frac{(I_1 - I_{avg})Z_0}{2}\sin\omega_0(t - t_3) + \frac{V_o}{2}\cos\omega_0(t - t_3) \tag{5-3}$$

where $Z_0 = \sqrt{2L_a / C_p}$ and $\omega_0 = \sqrt{2/(L_a C_p)}$. With proper design of the auxiliary circuit, $V_{sw1}$ increases to $V_i$ and $V_{sw2}$ decreases to 0 by the end of this time interval.

*Subinterval 5 (Figure 5.3(e)) [$t_4 - t_5$]*: $M_1 - M_4$ are all in the off-state while $M_a$ is in the on-state. Current difference ($i_{La} - i_{Lm}$) goes through the body diodes of $M_1$ and $M_2$, maintaining $V_{ds1} = 0$ and $V_{ds2} = 0$. During this interval, input $V_i$ applies across $L_a$ such that $i_{La}$ is decreased linearly.

*Subinterval 6 (Figure 5.3(f)) [$t_5 - t_6$]*: $M_1$ and $M_2$ are turned on under zero-voltage condition at $t_5$. Auxiliary current $i_{La}$ decreases linearly to $i_{Lm}$ at $t_6$, and the negative value of $i_{M1}$ and $i_{M2}$ (polarity defined in Figure 4.1) increases to 0 accordingly.

*Subinterval 7 (Figure 5.3(g)) [$t_6 - t_7$]*: $M_1$, $M_2$ and $M_a$ are maintained in the on-state, while $M_3$ and $M_4$ are in the off-state. Auxiliary current $i_{La}$ decreases further to zero, so $i_{M1}$ and $i_{M2}$ become positive and equal the main inductor current at $t_7$.

*Subinterval 8 (Figure 5.3(h)) [$t_7 - t_8$]*: Due to reverse blocking of $D_a$, the auxiliary circuit becomes disabled naturally after $i_{La}$ decreases to 0 at $t_7$. $M_a$ is thus turned off thereafter. Currents $i_{M1}$ and $i_{M2}$ equal $i_{Lm}$ with $V_{sw1} = V_i$ and $V_{sw2} = 0$.

*Subinterval 9 (Figure 5.3(i)) [$t_8 - t_9$]*: $M_1$ and $M_2$ are turned off at $t_8$. Main inductor current $i_{Lm}$ discharges $SW_1$ and charges $SW_2$ such that $V_{sw1}$ falls from $V_i$ to 0 and $V_{sw2}$ rises from 0 to $V_o$.

*Subinterval 10 (Figure 5.3(j)) [$t_9 - t_{10}$]*: At $t_9$, body diodes of $M_3$ and $M_4$ start to conduct $i_{Lm}$, maintaining $V_{ds3} = V_{ds4} = 0$. Synchronous switches $M_3$ and $M_4$ are then ready to be turned on under the zero-voltage condition. Note that time instant $t_{10}$ is the end of this switching period and the operation sequence in the buck-boost mode will repeat from interval 1 to interval 10 thereafter.

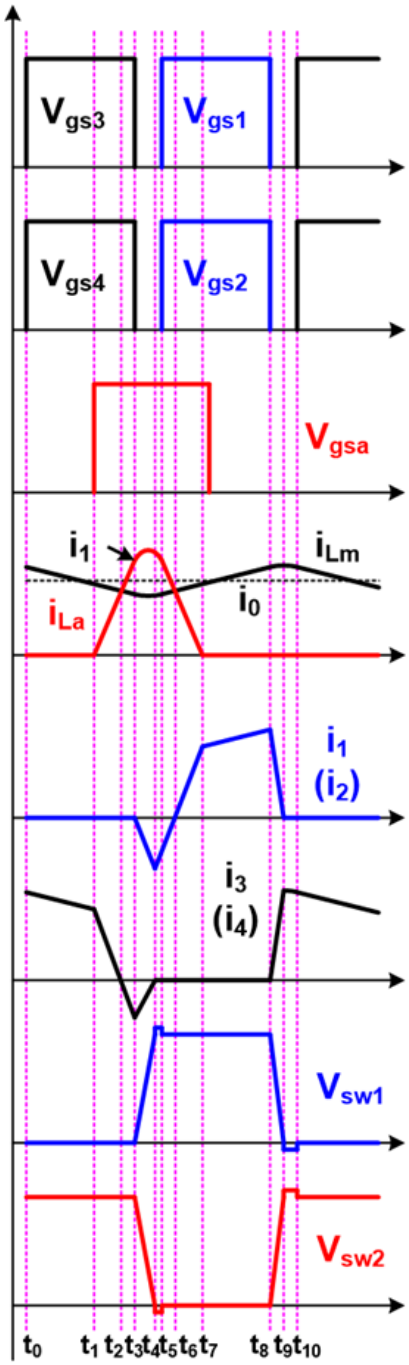



Figure 5.2. Key waveforms in the buck-boost mode.

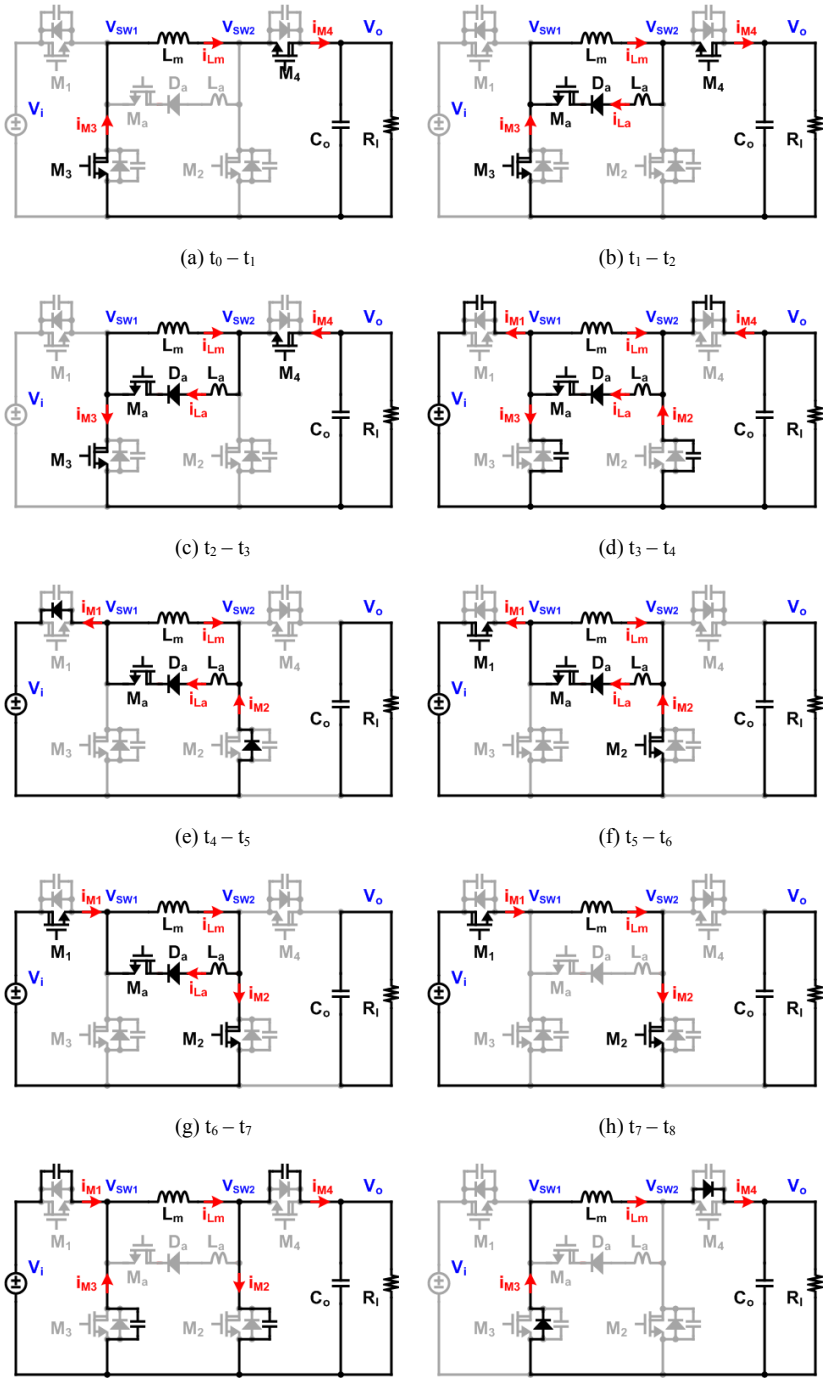



Figure 5.3. Operation states of the proposed buck-boost converter in the buck-boost mode.

## B. Operation Principles in Buck Mode

In the buck mode, each switching period also consists of 10 time sub-intervals. The key waveforms and equivalent circuits of each sub-interval are shown in Figures 5.4 and 5.5, respectively. The proposed auxiliary circuit ensures ZVS of $M_1$ and $M_3$ during their turn-on to minimize the switching power loss of the converter.

*Subinterval 1 (Figure 5.5(a)) [$t_0 - t_1$]*: $M_3$ and $M_4$ are in the on-state, while $M_1$ and $M_2$ are in the off-state. The auxiliary circuit is disabled during this interval. The main inductor current $i_{Lm}$ goes through $M_3$ and $M_4$ to supply the load.

*Subinterval 2 (Figure 5.5(b)) [$t_1 - t_2$]*: $M_a$ is turned on at $t_1$, while $M_3$ and $M_4$ are still in the on-state during this interval. Since $V_o$ is applied across the auxiliary inductor $L_a$, $i_{La}$ increases linearly from 0 towards $i_{Lm}$, and thus the currents ($i_{M3}$ and $i_{M4}$) through $M_3$ and $M_4$ decrease to 0. Because $M_a$ is turned on under the zero-current condition, the switching loss of $M_a$ is negligible.

*Subinterval 3 (Figure 5.5(c)) [$t_2 - t_3$]*: $M_a$, $M_3$ and $M_4$ stay in the on-state, while $M_1$ and $M_2$ are in the off-state. $I_{La}$ continues to increase so as to be larger than $i_{Lm}$ until it reaches a pre-defined value $I_1$ at $t_3$, and both $i_{M3}$ and $i_{M4}$ change to negative according to the polarity definition in Figure 5.1.

*Subinterval 4 (Figure 5.5(d)) [$t_3 - t_4$]*: $M_3$ are turned off at $t_3$ while $M_4$ keeps in on-state, and the current difference ($i_{La} - i_{Lm}$) charges nodes $SW_1$ towards $V_i$. If the parasitic capacitance at $SW_1$ is assumed to be the same as $C_p$, the resonance of $i_{La}$ and $V_{sw1}$ is then given as

$$i_{La} = (I_1 - I_{avg})\cos\omega_0(t - t_3) + \frac{V_o}{Z_0}\sin\omega_0(t - t_3) + I_{avg} \tag{5-4}$$

$$V_{sw1} = \frac{(I_1 - I_{avg})Z_0}{2}\sin\omega_0(t-t_3) - \frac{V_o}{2}\cos\omega_0(t-t_3) + \frac{V_o}{2} \quad (5\text{-}5)$$

where $Z_0 = \sqrt{L_a / C_p}$ and $\omega_0 = \sqrt{1/(L_a C_p)}$. With proper design of the auxiliary circuit, $V_{sw1}$ increases to $V_i$ by the end of this time interval.

*Subinterval 5 (Figure 5.5(e)) [$t_4 - t_5$]*: $M_1 - M_3$ are all in the off-state while $M_4$ and $M_a$ are in the on-state. Current difference ($i_{La} - i_{Lm}$) goes through the body diodes of $M_1$, maintaining $V_{ds1} = 0$. During this interval, input $V_i$ applies across $L_a$ such that $i_{La}$ is decreased linearly.

*Subinterval 6 (Figure 5.5(f)) [$t_5 - t_6$]*: $M_1$ is turned on under zero-voltage condition at $t_5$. Auxiliary current $i_{La}$ decreases linearly to $i_{Lm}$ at $t_6$, and the negative value of $i_{M1}$ (polarity defined in Figure 4.1) increases to 0 accordingly.

*Subinterval 7 (Figure 5.5(g)) [$t_6 - t_7$]*: $M_1$, $M_4$ and $M_a$ are maintained in the on-state, while $M_2$ and $M_3$ are in the off-state. Auxiliary current $i_{La}$ decreases further to zero, so $i_{M1}$ become positive and equal the main inductor current at $t_7$.

*Subinterval 8 (Figure 5.5(h)) [$t_7 - t_8$]*: Due to reverse blocking of $D_a$, the auxiliary circuit becomes disabled naturally after $i_{La}$ decreases to 0 at $t_7$. $M_a$ is thus turned off thereafter. Current $i_{M1}$ equals $i_{Lm}$ with $V_{sw1} = V_i$.

*Subinterval 9 (Figure 5.5(i)) [$t_8 - t_9$]*: $M_1$ is turned off at $t_8$. Main inductor current $i_{Lm}$ discharges $SW_1$ such that $V_{sw1}$ falls from $V_i$ to 0.

*Subinterval 10 (Figure 5.5(j)) [$t_9 - t_{10}$]*: At $t_9$, body diodes of $M_3$ start to conduct $i_{Lm}$, maintaining $V_{ds3} = 0$. Synchronous switch $M_3$ is then ready to be turned on under the zero-voltage condition. Note that time instant $t_{10}$ is the end of this switching period and the operation sequence in the buck mode will repeat from interval 1 to interval 10 thereafter.

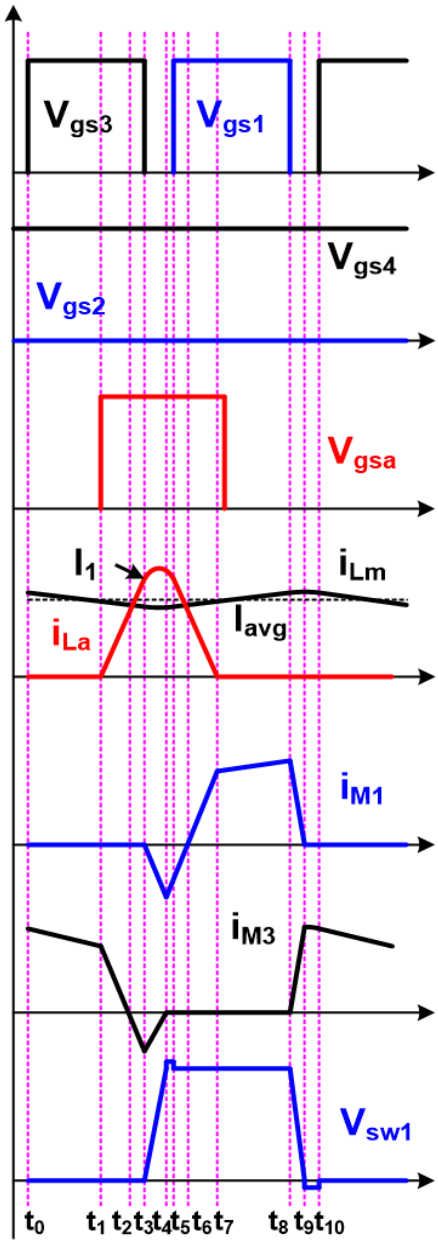



Figure 5.4. Key waveforms in the buck mode.

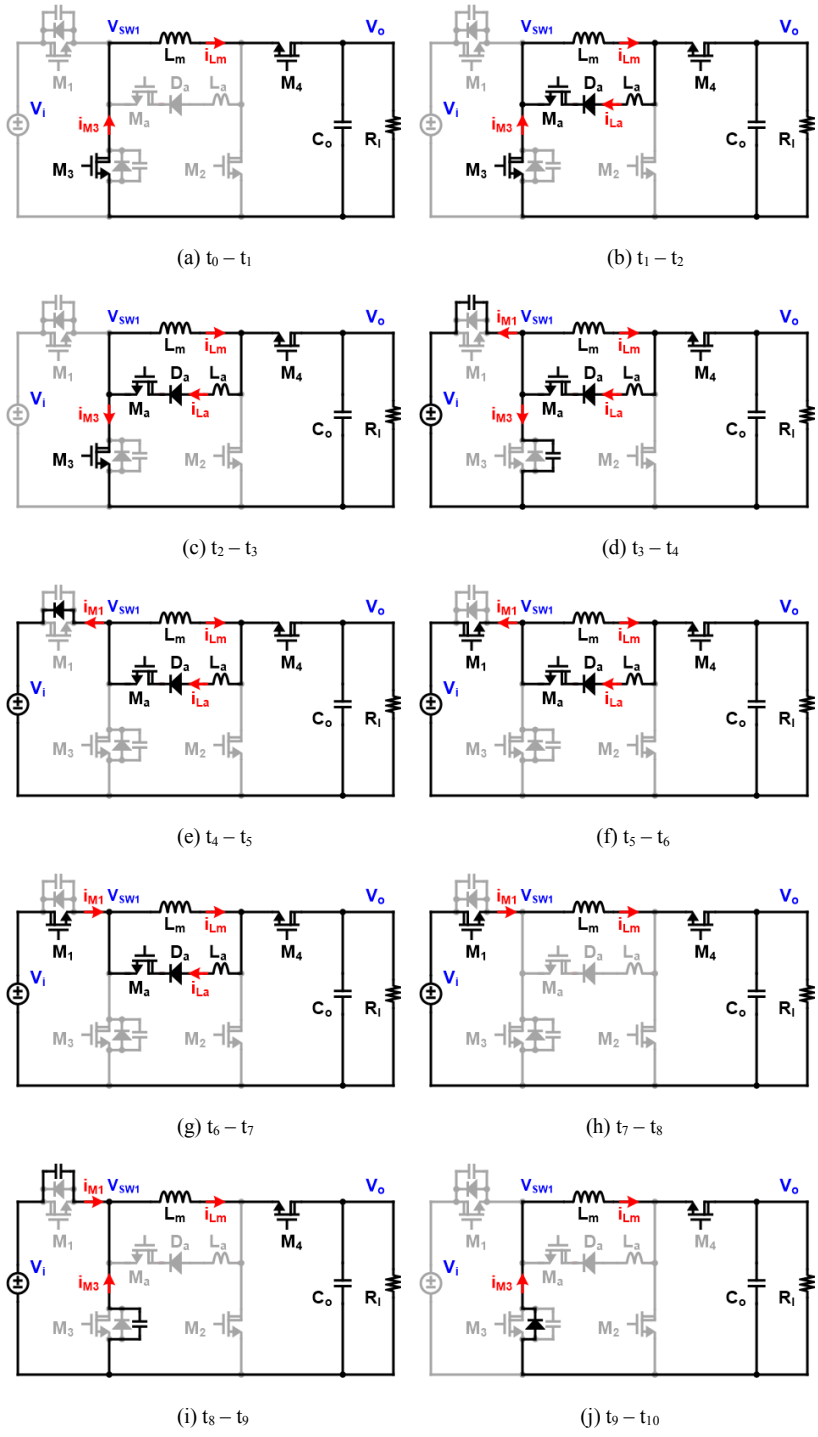



Figure 5.5. Operation states of the proposed buck-boost converter in the buck mode.

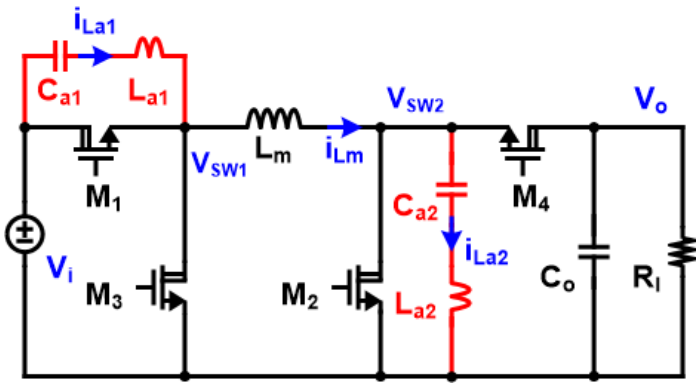
### 5.2.2 Analysis and Design Considerations

A. Area Efficiency Considerations among Different Soft-Switched Non-Inverting Buck-Boost Converters

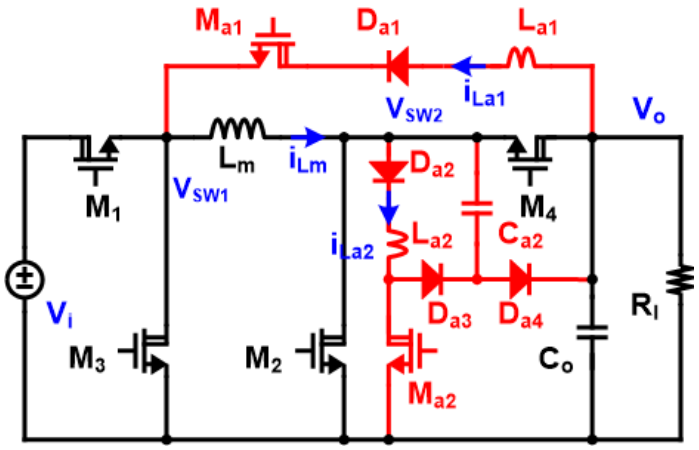
The soft-switched non-inverting buck-boost converters require the use of auxiliary components to realize ZVS of power transistors. For delivering tens-of-Watt output power, these auxiliary components including inductor, capacitor, power switch, and diode are generally discrete. Also, among different types of auxiliary components, the size of the inductor is typically the largest and will occupy a significant portion of the total board area of the converter. As a result, it is essential to minimize not only the total number of discrete auxiliary components but also more importantly the required number of the auxiliary inductor for the consideration of the converter area efficiency.

In the state-of-the-art non-inverting buck-boost converter with the QSW-ZVS technique [30] shown in Figure 5.6(a), each switching node has one dedicated LC branch to realize ZVS of the power switches. Therefore, a total of 4 auxiliary components (2 inductors and 2 capacitors) are utilized in the converter. In the previously-reported ZVT buck or boost converters [9, 56 – 60], one auxiliary branch is also merely dedicated to each switching node. The non-inverting buck-boost converter with 2 switching nodes thus requires 2 auxiliary branches. Different types of the auxiliary branch with various component counts were reported for different topologies (buck or boost). For example, if the auxiliary branches in [9] and [56] are adopted for the nodes $SW_1$ and $SW_2$, respectively, a total of 9 auxiliary components (2 inductors, 2 power FETs, 4 diodes and 1 capacitor) are required in the non-inverting buck-boost converter, as shown in Figure 5.6(b).

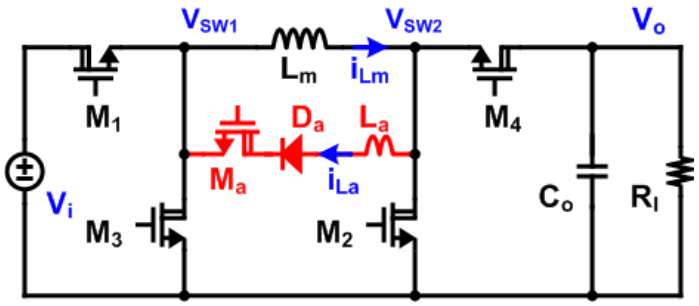
Instead of using the auxiliary branch that always connects between a switching node and a fixed-voltage node (i.e. $V_i$, $V_o$ or GND) in previously-reported soft-switching converters, the auxiliary branch is proposed to connect between two switching nodes in the non-inverting buck-boost converter as shown in Figure 5.6(c). The auxiliary branch injects current $i_{La}$ into $SW_1$ and out of $SW_2$ at the same time to enable ZVS operation during the turn-on of both active switches $M_1$ and $M_2$. In addition, ZVS operation during the turn-on of two synchronous switches $M_3$ and $M_4$ is achieved via the current $i_{Lm}$ of the main inductor. With only one auxiliary branch (1 inductor, 1 diode, 1 power FET), the proposed converter provides reductions in the required numbers of the auxiliary inductor and total auxiliary components as compared to the previous approaches. The proposed converter therefore has significant improvements in the converter volume and the system cost.




(a)




(b)




(c)

Figure 5.6. Structures of auxiliary branches in the non-inverting buck-boost converters using (a) the QSW-ZVS, (b) the traditional ZVT, and (c) the proposed ZVT.

B. Power Loss Analysis among Different Soft-Switched Non-Inverting Buck-Boost Converters

Although the switching loss is minimized in the soft-switched converters, the converter power efficiency could still be poorly affected by the additional conduction and core losses brought by the auxiliary branch/branches. This sub-section thus provides the analysis of the power loss of the auxiliary branch in the proposed ZVT non-inverting buck-boost converter and compares it

with that using the QSW-ZVS [30] and traditional ZVT [9], [56] approaches. The power loss analysis is performed based on the assumptions as follows.

First, all three soft-switched non-inverting buck-boost converters shown in Figures 5.6 (a) – (c) are configured as 48-V input, 48-V output buck-boost mode with a load current of 1.5 A. The average current $I_{avg}$ of the main inductor is around 3 A. The inductor in the auxiliary branch for all converters use model SER 1590 series [62] and its winding resistance $R_{wind}$ is assumed to be 150 mΩ. In case the auxiliary branch has a diode and a power switch, power diode with model STPS8H100G [63] is used and the on-resistance of the power switch is assumed to be 50 mΩ. Second, for the ease of analysis, the peak current of the auxiliary inductor in all converters is assumed to be $I_1$, which is barely higher than $I_{avg}$, such that ZVS operation is realized with minimized conduction loss in the auxiliary branch/branches. Finally, the conduction time of the auxiliary branch/branches in ZVT converters (Figures 5.6 (b) and (c)) is assumed to be half of a switching period $T_S$ and $T_S$ equals 1 μs for the ease of calculation, although the conduction time of the auxiliary branch/branches can be ~300 ns in the discrete prototype implementations. This assumption would thus over-estimate the power loss of the ZVT converters.

From current waveforms in Figure 5.7(a), the conduction loss of two auxiliary branches in the traditional QSW-ZVS converter is given as

$$P_{cond,1} = \frac{1}{T_S}\int_0^{T_S} (i_{La1}{}^2 + i_{La2}{}^2)R_{wind}\,dt = \frac{2}{3}I_1^2 R_{wind} \tag{5-6}$$

where both auxiliary inductors are assumed to have the same winding resistance $R_{wind}$ of 150 mΩ. For $I_1$ = 3 A, the conduction loss $P_{cond,1}$ due to the winding resistance of both auxiliary

inductors equals 0.9 W. Regarding the core loss, the total core loss of two auxiliary inductors according to Steinmetz equation [47] is given as

$$P_{core,1} = 2k_1(F_{SW})^x(\Delta I)^y = 2k_1(F_{SW})^x(2I_1)^y \quad (5\text{-}7)$$

where $k_1$ is the constant for the core material; x is the frequency exponent typically between 1 and 1.5; and y is flux density exponent typically between 2 and 3. By using the value of each auxiliary inductor of 0.9 μH based on [30] and the parameters from Coilcraft SER 1590 series [62], $P_{core,1}$ with the inductor waveforms $i_{La1}$ and $i_{La2}$ shown in Figure 5.7 (a) is about 1.17 W at 1-MHz switching frequency. Therefore, the total power loss of both auxiliary branches in the QSW-ZVS converter is 0.9 W + 1.17 W = 2.07 W.

Regarding the ZVT converter shown in Figure 5.6 (b), the conduction loss $P_{cond,2}$ of the auxiliary branch involving $M_{a1}$, $D_{a1}$ and $L_{a1}$ is given as

$$P_{cond,2} = P_{Da1} + \frac{1}{T_S}\int_0^{0.5T_S} i_{La1}{}^2(R_{wind} + R_{ds,Ma1})dt = P_{Da1} + \frac{1}{6}I_1^2(R_{wind} + R_{ds,Ma1}) \quad (5\text{-}8)$$

where $R_{ds,Ma1}$ is the on-resistance of the auxiliary switch $M_{a1}$. The conduction loss $P_{da1}$ of the diode $D_{a1}$ is provided by the manufacturer STMicroelectronics [63] as

$$P_{Da1} = 0.48I_{F(avg)} + 0.0125I_{F(RMS)}^2 \quad (5\text{-}9)$$

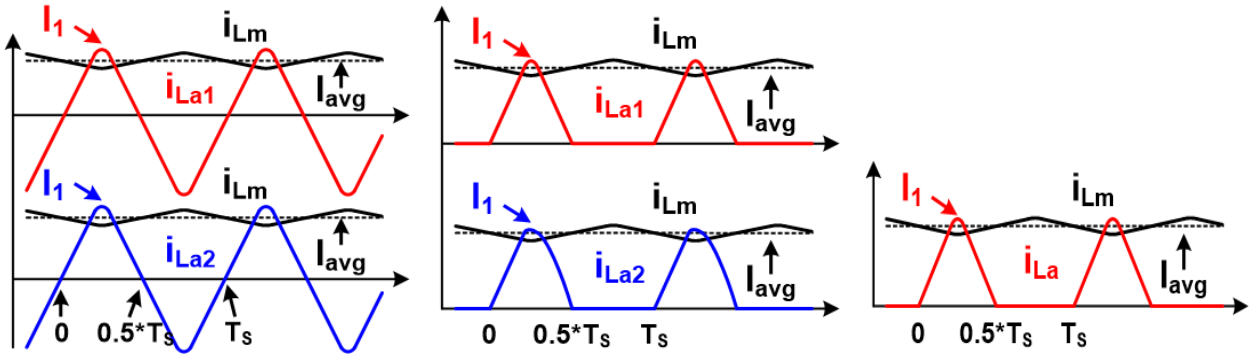
where $I_{F(avg)}$ and $I_{F(RMS)}$ stand for the average and RMS values of the forward current $i_{La1}$, and equal 0.75 A and 1.22 A, respectively. The conduction loss of $D_{a1}$ is thus ~0.37 W and the total conduction loss $P_{cond,2}$ for $D_{a1}$, $M_{a1}$ and $L_{a1}$ is around 0.67 W. Regarding the core loss $P_{core,La1}$ of $L_{a1}$ in the traditional ZVT converter, it is given as

$$P_{core,La1} = k_1(F_{SW})^x(\Delta I)^y = k_1(F_{SW})^x I_1{}^y \quad . \quad (5\text{-}10)$$

If $L_{a1}$ is 1.2 μH and the peak-to-peak current ripple of $i_{La1}$ is 3 A, $P_{core,La1}$ equals 0.12 W at 1-MHz switching frequency based on the current waveform $i_{La1}$ in Figure 5.7 (b). The total power loss of the auxiliary branch involving $M_{a1}$, $D_{a1}$ and $L_{a1}$ in Figure 5.6 (b) is thus 0.67 W + 0.12 W = 0.79 W, in which the core loss of the auxiliary inductor is significantly reduced.

Power loss of the another auxiliary branch consisting of $M_{a2}$, $L_{a2}$, $C_{a2}$ and $D_{a2}$ – $D_{a4}$ is less straightforward to derive due to the fact that current $i_{La2}$ is shared among multiple sub-branches and the conduction loss of each component is difficult to model. However, since the auxiliary current waveform in the second branch is very similar to that in the first branch involving $M_{a1}$, $D_{a1}$ and $L_{a1}$, both the core loss and the total conduction loss in the second auxiliary branch are expected to be similar to those in the first branch. Therefore, the total power loss of auxiliary branches in the traditional ZVT converter shown in Figure 5.6 (b) is approximated as twice of that in the first auxiliary branch, and equals 0.79 W * 2 = 1.58 W.

Since the current waveform of the auxiliary branch in the proposed ZVT converter is the same as the branch involving $M_{a1}$, $D_{a1}$, $L_{a1}$ in the traditional ZVT buck-boost converter, equations (5-8) – (5-10) are also the conduction and core loss of the auxiliary branch in the proposed buck-boost converter and thus the total power loss of the auxiliary circuit in the proposed converter is 0.79 W. Table 5.1 summarizes the power losses of the auxiliary branch/branches in the three converters. Compared with the other two non-inverting buck-boost converters using traditional soft-switching topologies, the proposed converter requires the minimum power loss in the auxiliary circuit.




(a) (b) (c)

Figure 5.7. Main and auxiliary inductor current waveforms of the non-inverting buck-boost converters using (a) the QSW-ZVS, (b) the traditional ZVT, and (c) the proposed ZVT.

C. Design Considerations of the Auxiliary Circuit

In order to enable full ZVS of power transistors $M_1$ and $M_2$ under different input voltages and output loads, it is important to properly select the auxiliary inductance and design a suitable overlap duration between on-time of $M_a$ and on-time of synchronous switches $M_3$ and $M_4$ (i.e. duration from $t_1$ to $t_3$ in Figure 5.2) in the auxiliary circuit. In the buck-boost mode, in order for $V_{sw1}$ to resonate up to $V_i$ and $V_{sw2}$ to resonate down to 0, a minimum value of $I_1$ is required as

$$I_1 \geq \begin{cases} I_{avg} & \text{if } V_i < V_o \\ I_{avg} + \dfrac{V_o}{Z_0}\sqrt{(\dfrac{2V_i}{V_o}-1)^2 - 1} & \text{if } V_i \geq V_o \end{cases} . \qquad (5\text{-}11)$$

Similarly, to achieve ZVS of power transistors in the buck mode, a minimum value of $I_1$ is required as

$$I_1 \geq \begin{cases} I_{avg} & \text{if } V_i < 2V_o \\ I_{avg} + \dfrac{\sqrt{2}V_o}{Z_0}\sqrt{(\dfrac{V_i}{V_o}-1)^2 - 1} & \text{if } V_i \geq 2V_o \end{cases} . \qquad (5\text{-}12)$$

Under different input and load conditions, $I_1$ is controlled by the value of $L_a$ and the duration from $t_1$ to $t_3$ that $i_{La}$ linearly increases. The value of $I_1$ is given as

$$I_1 = \frac{V_o}{L_a}(t_3 - t_1) \quad . \tag{5-13}$$

Since the conduction loss increases with the charging duration of $L_a$, it is desirable to minimize the value of $(t_3 - t_1)$ while fulfilling (5-11) and (5-12) under the full load condition. In practice, the value of $(t_3 - t_1)$ is typically selected as 10% of a switching period ($T_s$) under the full load condition. The value of $L_a$ can then be determined by (5-13). Note that the total conduction time (from $t_1$ to $t_7$ in Figure 5.2) of $L_a$ would be around 300 ns (30% of $T_s$), including design margin to accommodate component variations.

Table 5.1. Comparison of auxiliary circuit loss among different soft-switching non-inverting buck-boost converters [1]

| | QSW-ZVS[30] | Traditional ZVT [9], [56] | Proposed ZVT |
|---|---|---|---|
| Conduction loss of the auxiliary branch(es) [2] | 0.9 W | 1.34 W | 0.67 W |
| Core loss of the auxiliary inductor(s) [3] | 1.17 W | 0.24 W | 0.12 W |
| Total loss of the auxiliary branch(es) | 2.07 W | 1.58 W | 0.79 W |

1. Loss calculations are based on the assumptions made in Section 4.2.2-B. 2. The winding resistance of each auxiliary inductor is assumed to be 150 mΩ. 3. SER1590 series from Coilcraft is used to model the inductor core loss.

## D. Generation of Gate Drive Signals

Figure 5.8 shows the generation of gate drive signals for $M_1$ – $M_4$ and $M_a$ in different operation modes. $M_1$ and $M_3$ are driven by complementary PWM signals with sufficient dead time via using a non-overlapping clock generator. If the input voltage $V_i$ is lower than a scaled reference voltage (i.e. 56 V), the output of the Schmitt comparator is reset to logic “0” such that

$M_2$ ($M_4$) has the same gate drive signal as $M_1$ ($M_3$), and the converter operates in the non-inverting buck-boost mode. If $V_i$ rises to be higher than 56 V, the output of the Schmitt comparator is set to logic "1" such that $M_2$ and $M_4$ are constantly kept off and on, respectively, and the converter operates in the buck mode. Therefore, the converter can automatically transition between the buck-boost and buck modes according to different input voltage with designed hysteresis. The turn-on edge the auxiliary FET $M_a$ is determined by an R-C delay unit and the turn-off edge is controlled by a mono-stable timer.

Since the proposed auxiliary branch is only on during the switching transitions, it has negligible impact on the power stage transfer function. The conventional PWM controller for hard-switching non-inverting buck-boost converters can be used to general PWM input signal in Figure 5.8.

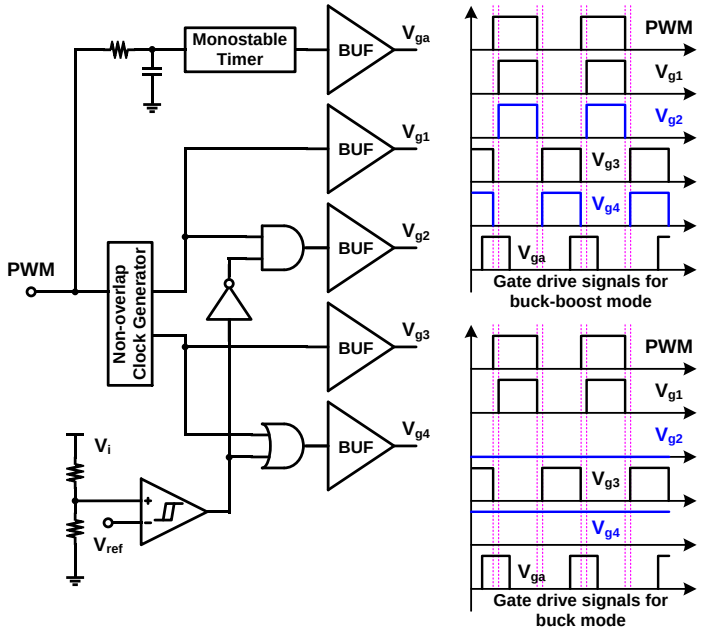



Figure 5.8. Gate driver structure of the proposed non-inverting buck-boost converter.

### 5.2.3 Measurement Results and Discussions

A hardware prototype of the proposed converter was implemented as shown in Figure 5.9 (a) to verify its performances. Figure 5.9 (b) shows the measurement setup for obtaining gate-to-source voltage of each power transistor and inductor currents of the converter. Unless otherwise stated, all power switches $M_1$ – $M_4$, $M_a$ in the proposed converter use 100-V eGaN power transistors with the model number EPC 2007 [19]. In the auxiliary branch, the inductor and diode adopt 1.2-µH SER 1590-122 [62], and Schottky rectifier STPS8H100 [63], respectively.

The proposed converter operates at a switching frequency of 1 MHz and delivers a maximum output power of 75 W. It produces an output voltage of 48 V from an input voltage range of 36 V – 90 V. Specifically, the proposed converter operates in the buck-boost mode for the input from 36 V to 56 V, and the buck mode for the input from >56 V to 90 V.

Figures 5.10 and 5.11 demonstrate the ZVS capability of the proposed converter in the buck-boost mode at $V_i$ = 48 V and the buck mode at $V_i$ = 75 V, respectively. In both Figures 5.10 and 5.11, $V_{sw1}$ and $V_{sw2}$ are voltages of switching nodes of the proposed converter. The drain-to-source voltage of each power transistor relates to the switching-node voltage. In particular, the drain-to-source voltage $V_{ds1}$ of $M_1$ equals $V_i - V_{sw1}$; $V_{ds2} = V_{sw2}$; $V_{ds3} = V_{sw1}$; and $V_{ds4} = V_{sw2} - V_o$. As shown in Figure 5.10 (a), when $V_{sw1}$ reaches $V_i$ of 48 V, $V_{ds1} = 0$ and then $V_{gs1}$ increases to turn on $M_1$. Similarly, when $V_{sw2}$ reaches $V_o$ of 48 V in Figure 5.10 (c), $V_{ds4}$ becomes 0 and then $V_{gs4}$ increases from 0 to turn on $M_4$. Since both high-side power transistors $M_1$ and $M_4$ are turned on after their drain-to-source voltages decrease to 0, $M_1$ and $M_4$ achieve ZVS during their turn-on transitions. Similarly, both low-side power transistors $M_3$ and $M_2$ also achieve ZVS during their turn-on transitions as they are turned on only after their drain-to-source voltages

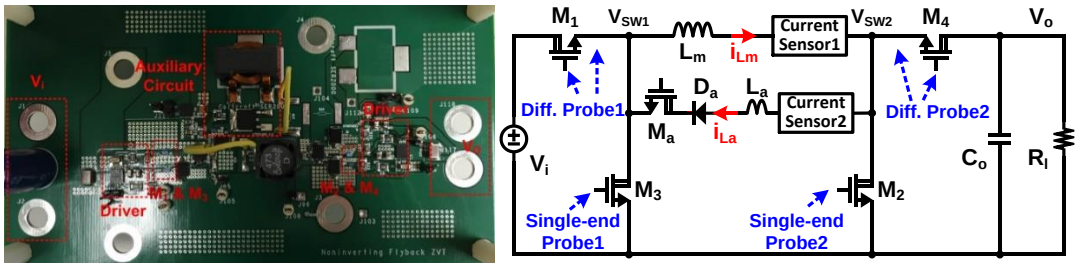
reach 0 (i.e. $V_{sw1}$ and $V_{sw2}$ decrease to 0), as shown in Figures 5.10 (b) and 5.10 (d), respectively. In addition, based on Figures 5.11 (a) and 5.11 (b), both high-side and low-side power transistors of the proposed converter in the buck mode are turned on with zero-voltage switching, thereby removing both switching and short-circuit power losses. In short, both Figures 5.10 and 5.11 verify the proposed single-branch ZVT cell to successfully establish ZVS of all the power switches $M_1 – M_4$ of the non-inverting buck-boost converter in different operation modes.

Figures 5.12 (a) – 5.12 (c) show measured waveforms of switching-node voltages and inductor currents of the proposed converter in both buck and buck-boost modes under different input voltages and the load currents. Note that $M_a$ is in series with the auxiliary inductor $L_a$, so the current of $M_a$ is the same as the current $i_{La}$ of $L_a$. Since $i_{La}$ has initial value of 0 and shows slow increase rate after $M_a$ is turned on during switching transitions, ZCS of $M_a$ is established. Moreover, due to short conduction time of the auxiliary circuit, the total loss of the auxiliary branch is reduced.

Figure 5.13 (a) shows the measured power efficiencies of the proposed converter prototype at the load current of 1.2 A under different input voltages. With eGaN FETs as power switches, the proposed converter operates in the buck-boost mode with $V_i$ from 36 V to 56 V and achieves the peak power efficiency of 92.5% at $V_i$ = 56 V. The converter is configured to the buck mode when $V_i$ is larger than 56 V and provides the peak power efficiency of 96.3% at $V_i$ = 80 V. When the power switches of the converter are changed to 100-V power MOSFETs with model FDM3622 [65], the power efficiency of the converter is always about 1 – 2% lower than that using eGaN FETs, although the efficiency still achieves above 88% for the entire input voltage range. Figure 5.13 (b) shows the power efficiencies of the proposed converter with eGaN FETs

under different load conditions. The proposed converter operated at 1 MHz achieves high power efficiency of about 90% or above over the entire load current range from 0.2 A to 1.5 A for both buck-boost and buck modes.

Table 5.2 provides the performance comparisons of the proposed converter with state-of-the-art counterparts. All converters have similar input voltage ranges, and the same output voltage and topology. Compared with the hard-switching converter in [46], the proposed converter minimizes the switching loss and thus supports a much higher switching frequency with much smaller current ripple $\Delta i_{Lm}$ of the main inductor, thereby providing significant reduction in the volumes of the main inductor and the output capacitor. Compared with the state-of-the-art QSW-ZVS non-inverting buck-boost converter with eGaN FETs [30], the proposed converter can support a higher output current and ensure soft switching of all power transistors with the reduction of the auxiliary inductor count from 2 to 1. Since the auxiliary inductor is the largest component in the auxiliary branch, the total volume of the auxiliary circuitry in the proposed converter is reduced by about 2 times as compared to [30]. In addition, the proposed ZVT converter reduces the conduction loss of the auxiliary components and auxiliary inductor core loss as compared to [30], thereby achieving improvements in the peak power efficiencies of the buck and buck-boost modes by 4% and 2%, respectively.




(a) (b)

Figure 5.9. (a) Hardware prototype and (b) measurement setup of the proposed ZVT buck-boost converter.

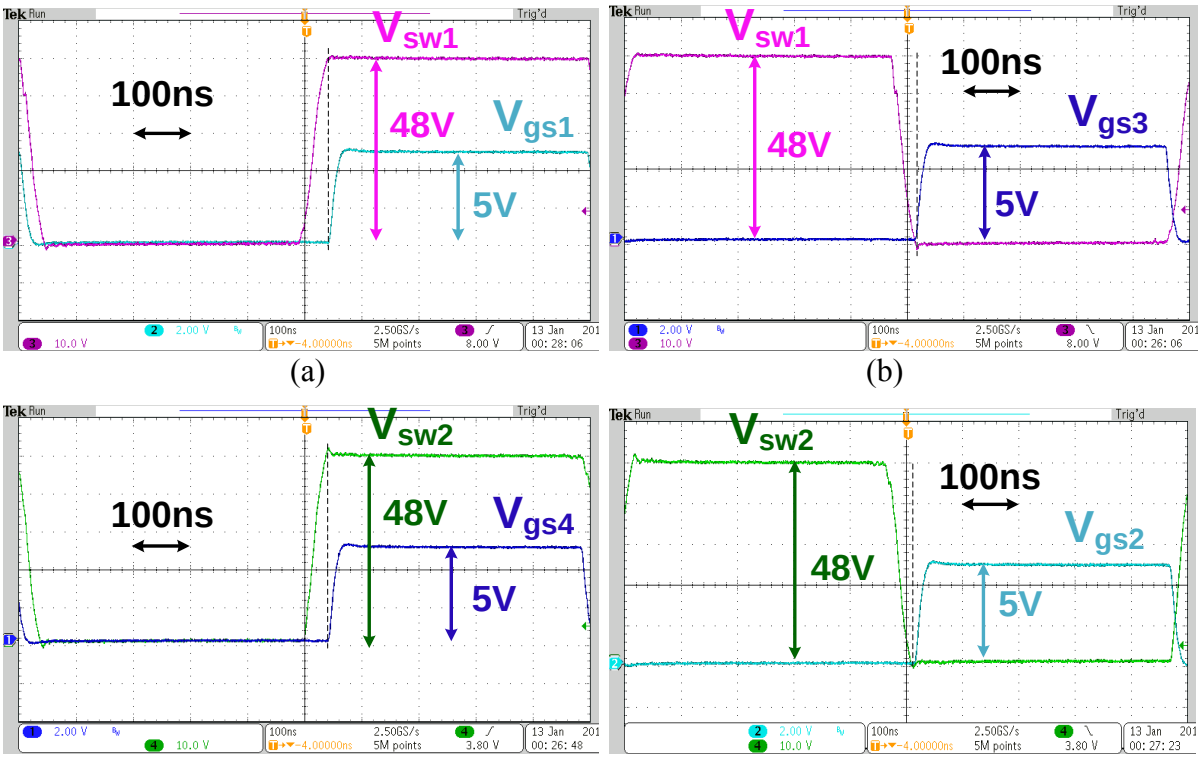



Figure 5.10. Switching transitions during the turn-on moments of (a) $M_1$, (b) $M_3$, (c) $M_4$, and (d) $M_2$ of the proposed converter in the buck-boost mode at 1-MHz frequency, 48-V $V_i$, 48-V $V_o$ and 0.2-A load current.

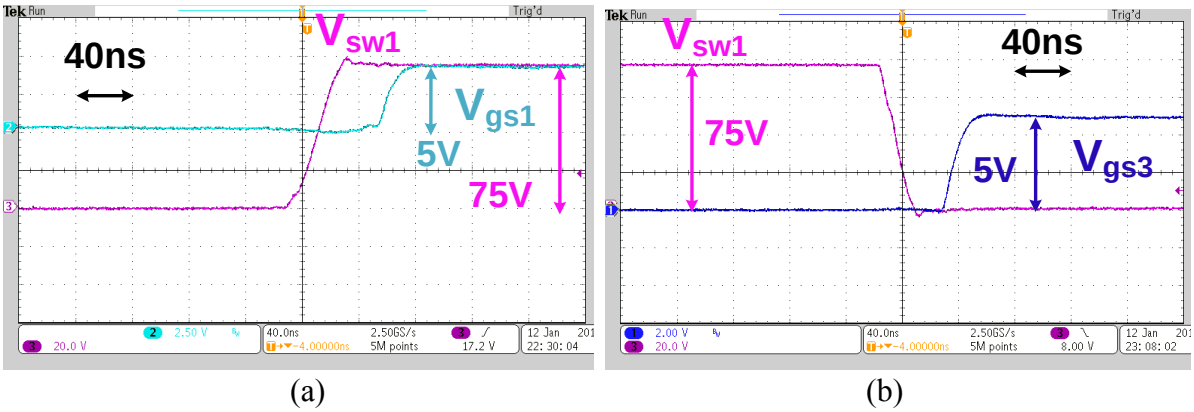



Figure 5.11. Switching transitions during the turn-on moments of (a) $M_1$ and (b) $M_3$ of the proposed converter in the buck mode at 1-MHz frequency, 75-V $V_i$, 48-V $V_o$ and 1.2-A load current.

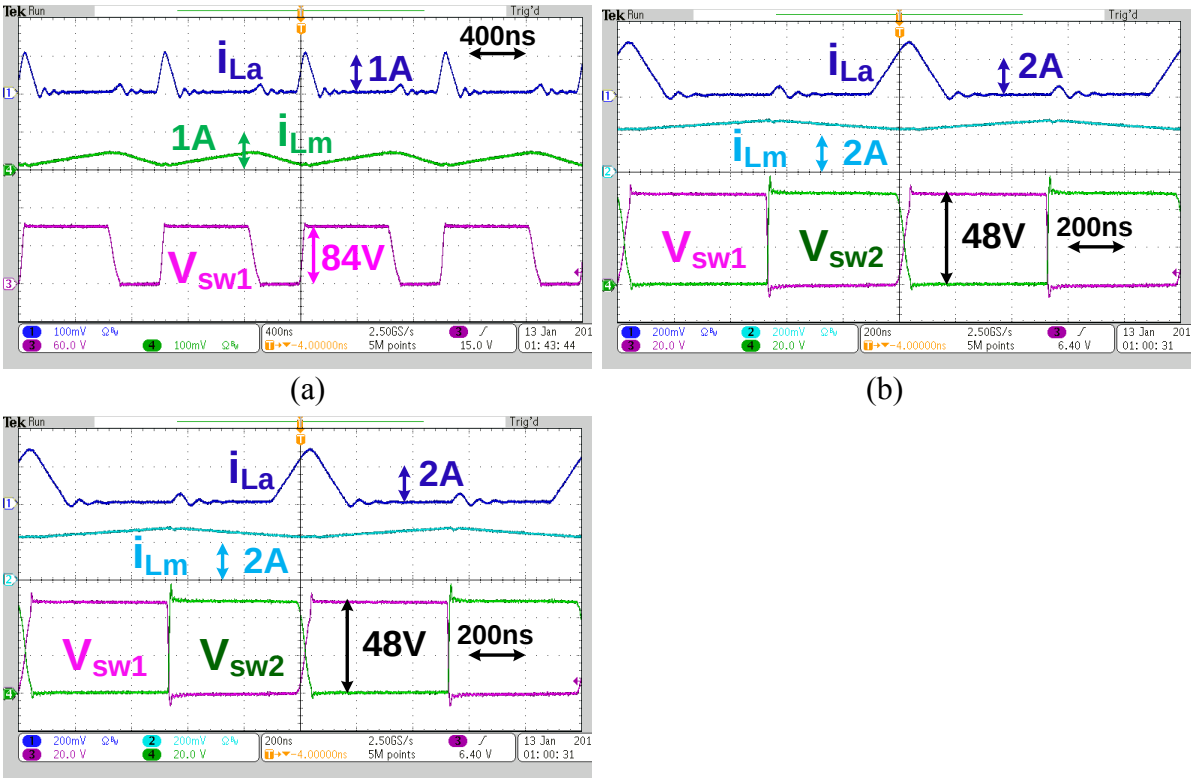



Figure 5.12. Waveforms of the proposed converter in (a) the buck mode with Vi = 84 V and the load current Io of 0.4 A, and the buck-boost mode with Vi = 48 V (b) Io = 0.2 A and (c) Io = 1.2.A.

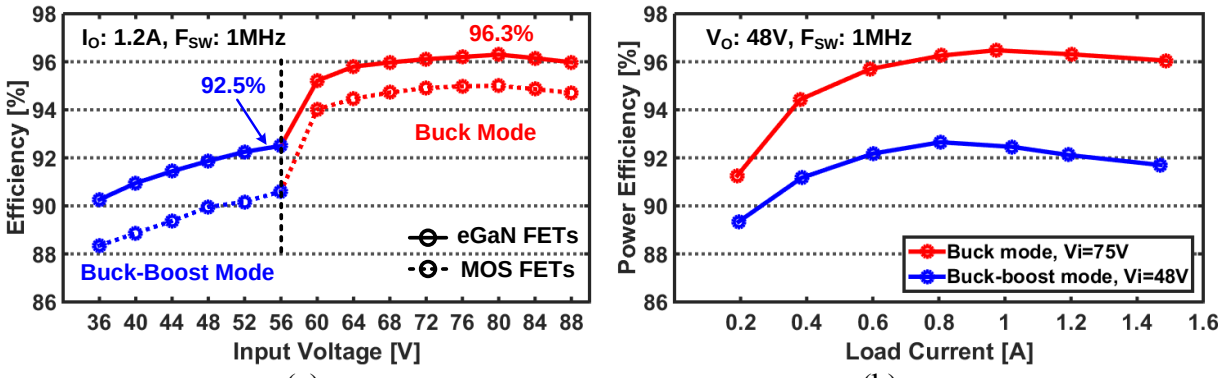



Figure 5.13. Measured power efficiencies of the proposed converter under different (a) input voltages using eGaN FETs and power nMOS FETs, and (b) output load currents with eGaN FETs.

Table 5.2. Performance comparisons of state-of-the-art non-inverting buck-boost converters

| | LT8705 [46] | TCAS II 2015 [30] | This Work |
|---|---|---|---|
| Topology | Non-inverting buck-boost | Non-inverting buck-boost | Non-inverting buck-boost |
| $V_i$ | 36 – 80 V | 24 – 80 V | 36 – 90 V |
| $V_o$ | 48 V | 48 V | 48 V |
| Max. $P_o$ ($I_o$) | 240 W (5 A) | 60 W (1.25 A) | 75 W (1.6 A) |
| Peak Efficiency | Buck: 98%<br>Buck-boost: 97% | Buck: 92.3%<br>Buck-boost: 90.4% | Buck: 96.3%<br>Buck-boost: 92.5% |
| Power FETs | MOSFETs | eGaN FETs | eGaN FETs |
| $F_{sw}$ | 200 kHz | 2000 kHz | 1000 kHz |
| Operation | Hard switching | QSW-ZVS | ZVT |
| Additional components for soft switching | N.A. | 2 aux. ind. [1] (0.9 µH x 2) and 2 aux. cap. (1 µF x 2); totally 4 components | 1 aux. ind. [1] (1.2 µH), 1 aux. eGaN FET and 1 diode; totally 3 components |
| Total volume of auxiliary components | N.A. | 3620 $mm^3$ | 1910 $mm^3$ |
| Filtering ind. $L_m$ (volume) | 22 µH<br>(SER2918H: 9800 $mm^3$) [2] | 22 µH<br>(MSS1278: 1220 $mm^3$) [2] | 30 µH<br>(MSS1278: 1220 $mm^3$) |
| Worst case $\Delta i_{Lm}$ [2] | 5.5 A | 0.56 A | 0.8 A |
| Filtering cap. $C_o$ (volume) [3] | 440 µF<br>(2700 $mm^3$ aluminum) | 15 µF<br>(80 $mm^3$ ceramic) | 30 µF<br>(160 $mm^3$ ceramic) |
| Worst case $\Delta V_o$ | Buck: 14 mV<br>Buck-boost: 55 mV | Buck: 11 mV<br>Buck-boost: 21 mV | Buck: 13 mV<br>Buck-boost: 27 mV |

1. Auxiliary inductor uses SER1590-901 with the volume of 1800 $mm^3$ per piece. 2. Obtained under the case in the buck-boost mode with $V_i = V_o$. 3. Obtained from datasheets or literature.

## 5.3 Adaptive Auxiliary Current Control for a High-Voltage High-Frequency Buck Converter with Quasi-Square-Wave ZVT Operation

As discussed in Chapter 2, non-isolated QSW-ZVS converters have alternating current ripple in the auxiliary branch that increases conduction loss while trying to remove the switching loss. QSW-ZVT converters can reduce the penalty on conduction loss since the auxiliary inductor current is in DCM form and its RMS value can be much smaller than that of QSW-ZVS counterparts. However, in all the existing QSW-ZVT converters, the on-time of the auxiliary switch is fixed and such designed that the ripple of the auxiliary current is enough to assist ZVS operation in heavy load condition. The drawback of this fixed control of the auxiliary switch is that the auxiliary conduction loss cannot scale with the loading condition, and thus the light load efficiency can be adversely affected. In this section, an adaptive auxiliary current control scheme is proposed to ensure high efficiency of a ZVT converter in very wide load range. Particularly, up to 14.5% increase in the light-load power efficiency is achieved at 2MHz frequency compared with the traditional counterparts [37].

### 5.3.1 System and Circuit Design of an Adaptive ZVT-Assisted Bus Converter

Figure 5.14 shows the structure of the AZVT-assisted Buck converter that consists of two synchronous enhance-mode GaN FETs ($M_H$, $M_L$), a main inductor $L_M$, an output capacitor $C_O$, and a ZVT branch. In light loads, ZVS turn-on of low-side $M_L$ and high-side $M_H$ are controlled by $L_M$ and the ZVT branch, respectively. In contrast to the conventional ZVS branch involving $L_{AUX}$ and $C_{AUX}$, the ZVT branch has an inductor $L_A$, a Schottky diode $D_A$, and an enhance-mode GaN FET $M_A$ connected between nodes $V_{SW}$ and $V_O$. $D_A$ and $L_A$ determine the direction and

amplitude of the auxiliary current $i_{LA}$. Since $i_{LA}$ is discontinuous and exists only when $M_A$ is on, $M_A$ achieves zero-current switching with minimal switching loss. The turn-on instant of transistor $M_A$ is further regulated by an AZVT controller to modulate the peak amplitude of $i_{LA}$ ($I_{LA,pk}$) for minimizing the power loss of the ZVT branch under different light-load conditions. Specifically, a HV high-speed filtered-based current sensor and an adaptive auxiliary current controller (AACC) are developed in the AZVT controller to sense $i_{LA}$ and adjust the on-time of $M_A$, respectively, for supporting the converter operation at 2MHz. Moreover, this bus converter would switch to the hard-switching (HS) mode in heavy loads where the conduction power loss dominates. By changing from the AZVT mode to HS mode, the bus converter can achieve high power efficiency across a wide load range.

To support AZVT operation, a fast accurate HV $i_{LA}$ sensor is required. A common inductor current sensing in the LV domain is to use the voltage drop across the inductor direct-current resistance (DCR). By ensuring $L_A/DCR = R_F*C_F$, voltage $V_{SNSO}$ across $C_F$ emulates $V_{DCR}$. Splitting DC and AC components of the sensed inductor current can further reduce the required DCR and thus the converter conduction loss [66]. However, prior LV sensors are unable to address two distinct challenges of sensing $i_{LA}$ in the ZVT branch. Since $i_{LA}$ flows away from $V_O$, $V_{SNSO}$ voltage is negative that creates the common-mode issue to the AACC. Considerable $V_O$ ripple due to small passives ($C_O$, $L_M$) and high $V_O$ DC voltage would also couple and distort $V_{SNSO}$ via $C_F$, deteriorating the sensing accuracy. To overcome these issues, a HV flipped current sensor with ripple cancellation is developed in Figure 5.15. In addition to ($C_F$, $R_F$) network, a passive branch ($C_F$, $R_{F1}$) is adopted to amplify AC component of $V_{SNSO}$ as $V_{ACA}$ with the AC gain of $R_F/R_{F1}$. Both $V_{ACA}$ signal and $V_O$ ripple are first coupled to node $V_{CPL}$ through a HV

capacitor $C_{HP1}$. The polarity of both $V_{ACA}$ signal and $V_O$ ripple are then flipped by 180° via an inverted unity-gain cell formed by transistors $M_{P1} - M_{P3}$ at the sensor output $V_{SNSA}$. Meanwhile, the $V_O$ ripple is also added to node $V_{SNSA}$ via direct AC coupling by another HV capacitor $C_{HP2}$, thereby removing $V_O$ ripple distortion at node $V_{SNSA}$. Both $C_{HP1}$ and $C_{HP2}$ are 100pF. On the other hand, the DC component of $V_{SNSO}$ is obtained by the ($C_{LP}$, $R_{LP}$) network as $V_{DCA}$. Voltage $V_{DCA}$ is first converted to current through $R_{M0}$ with a V-I converter realized by a HV folded-cascode amplifier and a HV transistor $M_{N0}$. This current is then mirrored to the sensor output branch and transformed to the DC component of $V_{SNSA}$ by the effective resistance R. By combining the amplified AC and DC components, output $V_{SNSA}$ successfully emulates $i_{LA}$ without the common-mode issue and $V_O$ ripple distortion for the proposed 2MHz HV converter.

To achieve ZVS turn-on of high-side $M_H$, current $I_r$ (= $I_{LA,pk} - I_{LM,vy}$) flows into node $V_{SW}$ to increase its voltage until $V_{IN}$. The AACC depicted in Figure 5.16 can modulate $I_{LA,pk}$ to provide sufficient $I_r$ while minimizing the power loss of the ZVT branch. Since the rising slope of $i_{LA}$ is fixed by $V_O$ voltage and the inductance of $L_A$, $I_{LA,pk}$ modulation is performed via regulating its value to a reference current level and adjusting the turn-on instant of $M_A$ accordingly. The reference level is proportional to the average main inductor current $I_{LM}$ and $I_O$. Specifically, both peak sensor output voltage $V_{LA,pk}$ (that corresponds to $I_{LA,pk}$) and $V_S$ (that corresponds to $I_{LM}$) are fed into a Gm cell with a Type II compensator to generate a stable voltage $V_{COM}$. Both references $V_{RL}$ and $V_{RH}$ set the lower and upper bounds of $V_{COM}$ to ensure proper start-up of the adaptive ZVT control. When a ramp signal $V_{RAMP}$ crosses $V_{COM}$, a set pulse ASET is generated to initiate the turn-on of $M_A$. The AACC also determines the turn-off instant of $M_A$ for enabling zero-current switching of $M_A$. The instant is defined by the reset pulse ARST triggered by the

crossover of $V_{SNSA}$ and a near-zero reference voltage $V_{REF}$. To avoid logic error of output PWMA signal, an extra reset pulse AMAXP is introduced to prevent the turn-off instant of $M_A$ from crossing the turn-on instant of the low-side GaN FET $M_L$, ensuring the system robustness. The LV PWMA signal is then transferred to the HV domain for driving $M_A$. Figure 5.17 provides the micrograph of the converter gate driver and AZVT controller in 0.5µm 120V CMOS process.

### 5.3.2 Measurement Results and Discussions

The proposed converter employs 3 100V enhance-mode GaN FETs (EPC2007C), a Schottky diode as $D_A$, 2 small-value inductors ($L_M$=1.5µH and $L_A$=0.82µH), and a 18.8µF $C_O$ to support wide $V_{IN}$ range from 48V to 80V and $I_O$ range from 0.5A to 5A at $f_{SW}$ of 2MHz. Figure 5.18 shows measured $V_{SW}$, $i_{LM}$ and $i_{LA}$ waveforms in different conditions of $V_{IN}$ and $I_O$. When $I_O$ increases, $M_A$ on-time and thus $I_{LA,pk}$ increase at $V_{IN}$ of 48V and 80V. $I_r$ is also maintained the same under different loads for each $V_{IN}$, proving proper operation of the AZVT controller. Figure 5.19 depicts that both $M_H$ and $M_L$ achieve ZVS during transitions, and turn-on and turn-on delays are within 5ns under different input voltages. Figure 5.19 further shows that the AZVT control provides the power efficiency improvements up to 14.5% (5.4%) and 8.7% (4.5%) at $V_{IN}$ of 48V and 80V, respectively, as compared to HS (ZVS). By switching between AZVT mode and HS mode, the proposed converter achieves >90% efficiency over the entire load range at $f_{SW}$=2MHz. Comparisons with the prior work of similar input and output voltages are provided in Table 5.3. With >2x increase in $f_{SW}$, the proposed converter uses smaller-value passives and provides significant improvements in light-load power efficiency compared to the prior art [67 – 69].

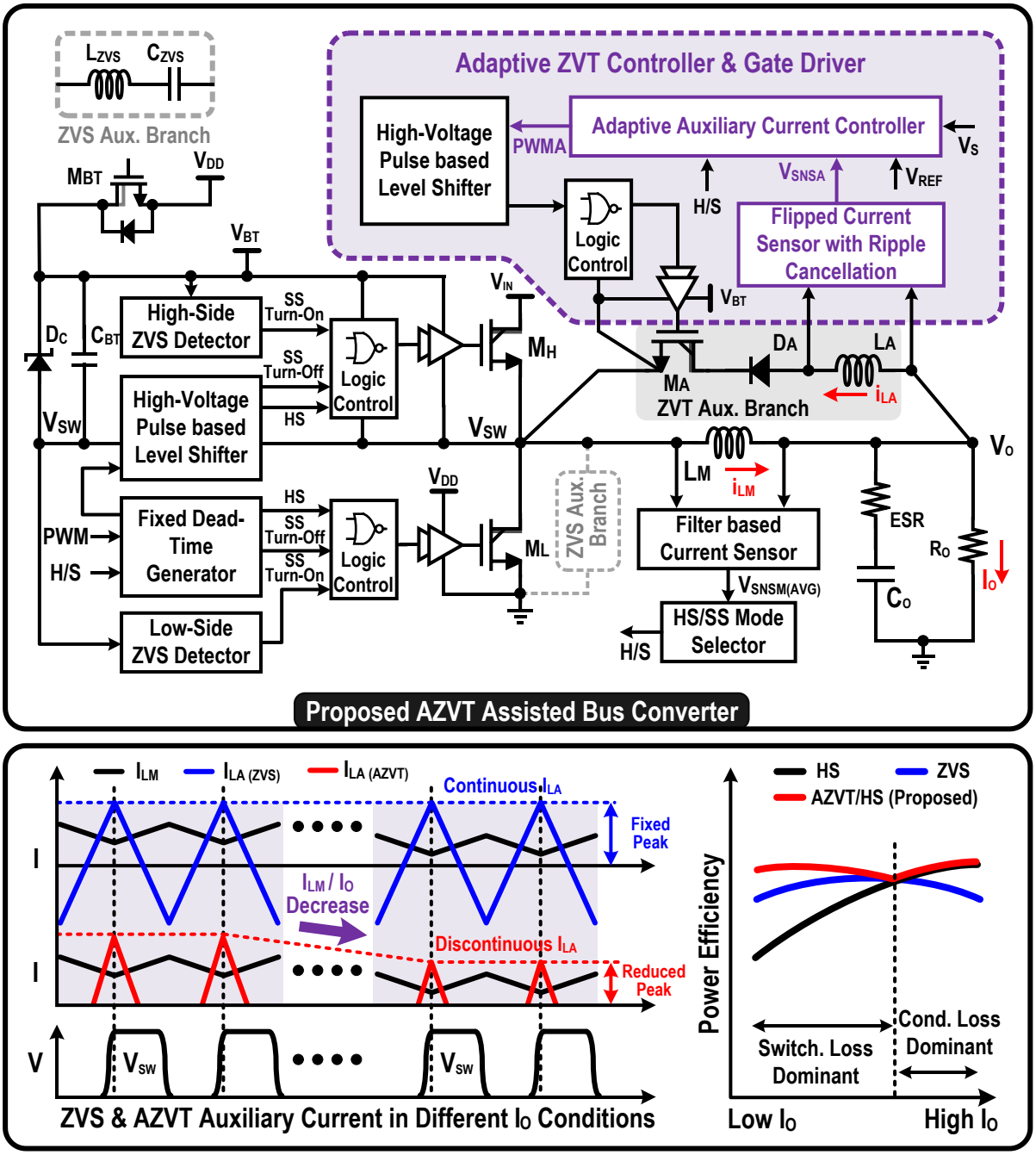



Figure 5.14. Structure of AZVT-assisted bus converter and comparison between AZVT vs ZVS in different load conditions.

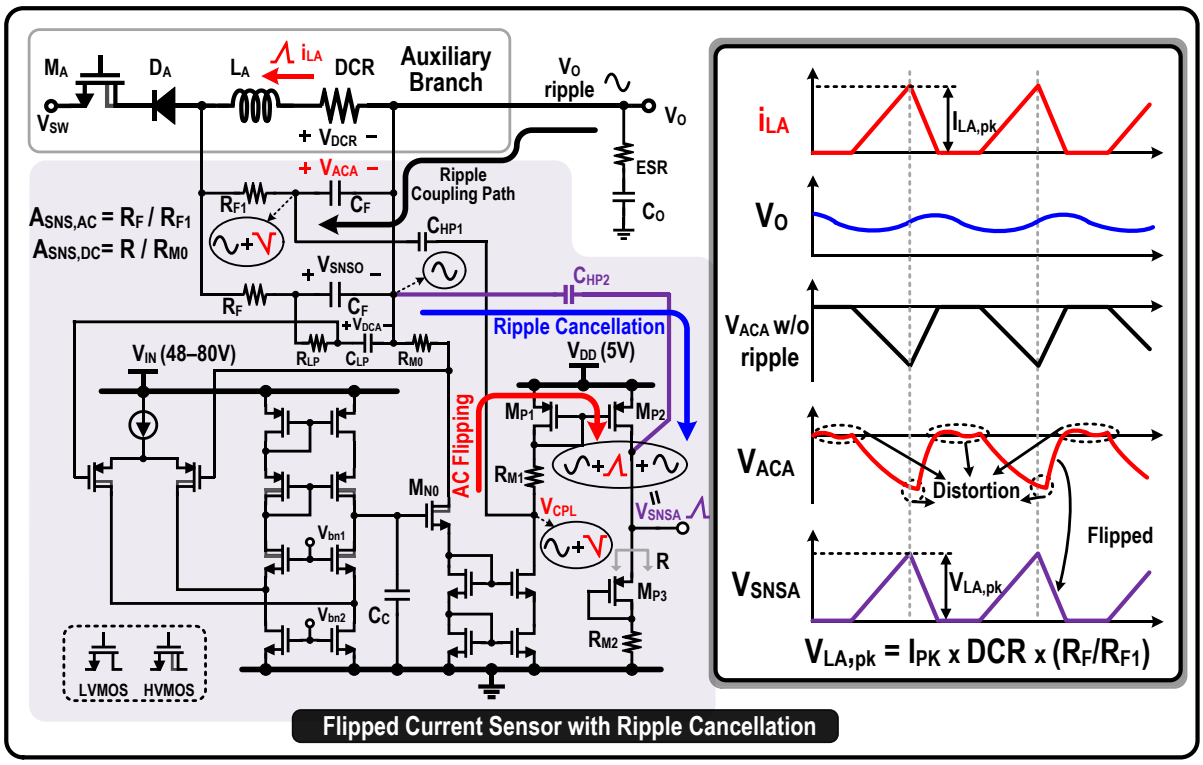



Figure 5.15. Schematic and features of proposed HV flipped current sensor with $V_O$ ripple cancellation for $M_A$.

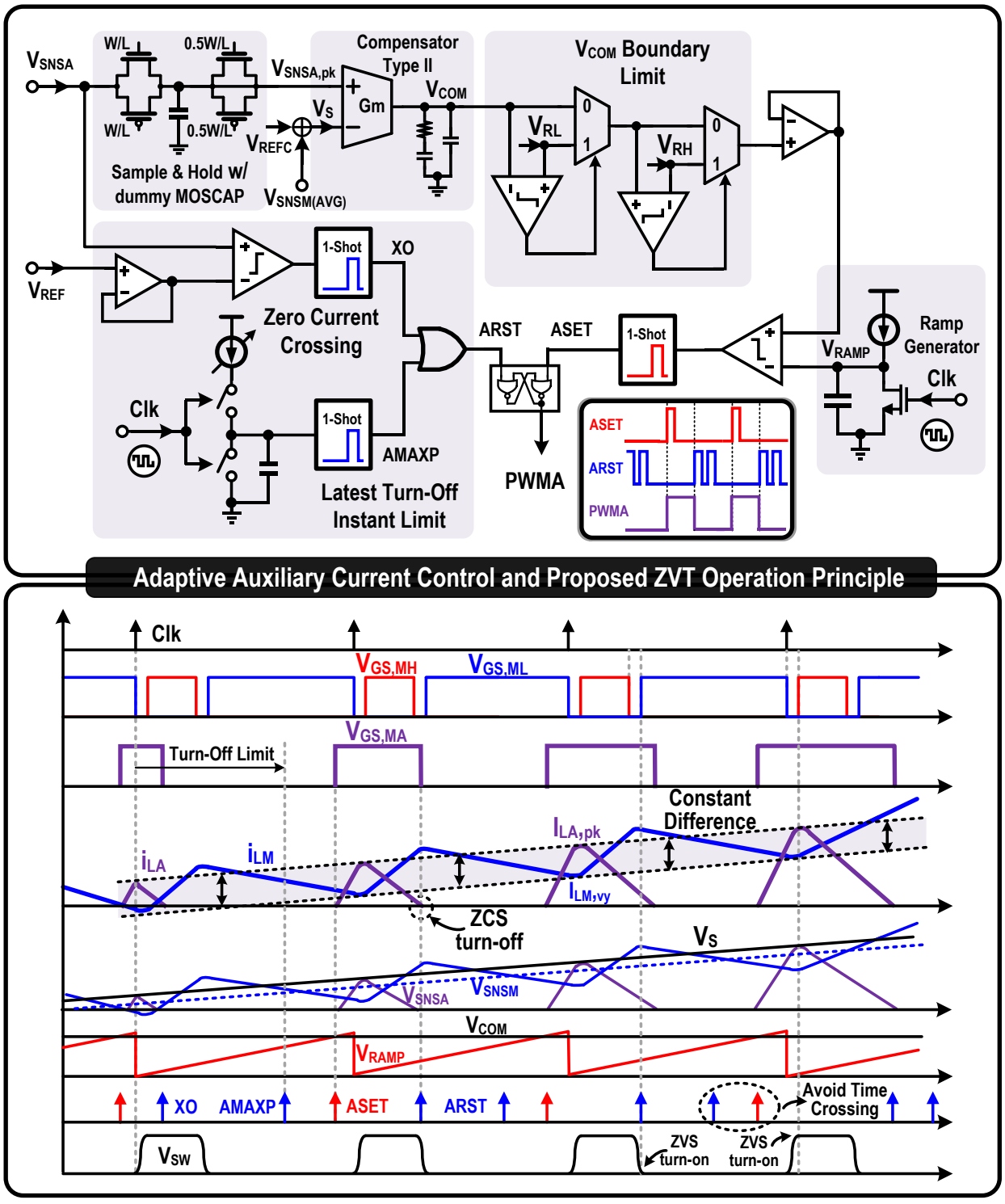



Figure 5.16. Structure and operation of the proposed adaptive auxiliary current controller.

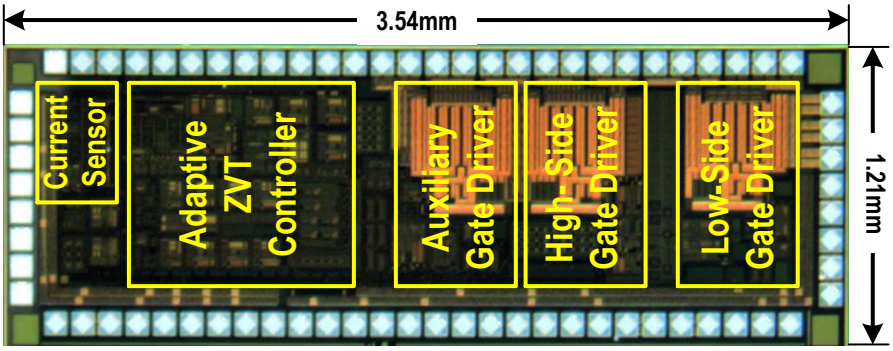



Figure 5.17.Micrograph of the proposed AZVT controller and converter gate driver in 0.5µm 120V CMOS process.

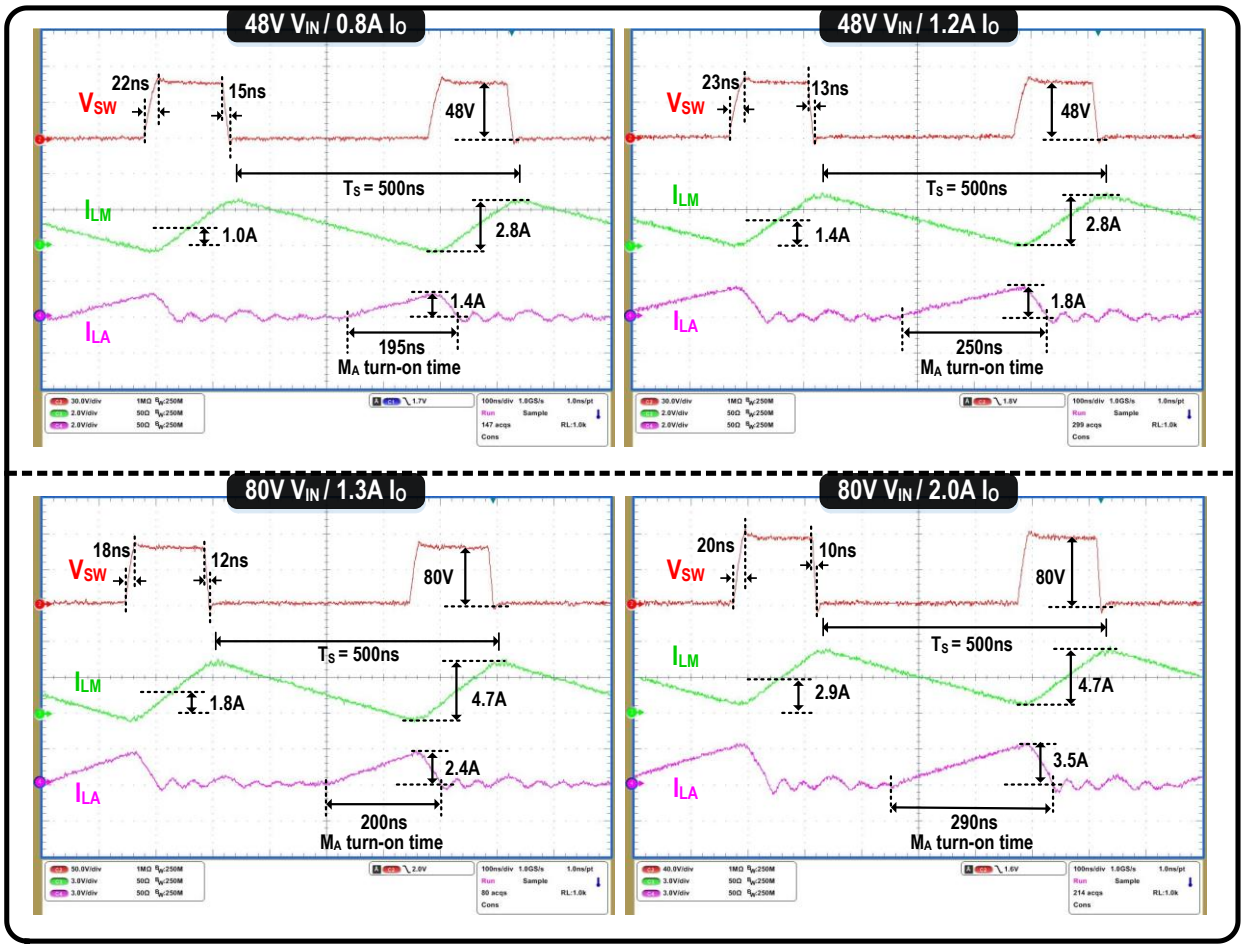



Figure 5.18. Measured steady-state waveforms under different $V_{IN}$ and $I_O$ conditions in the AZVT mode.

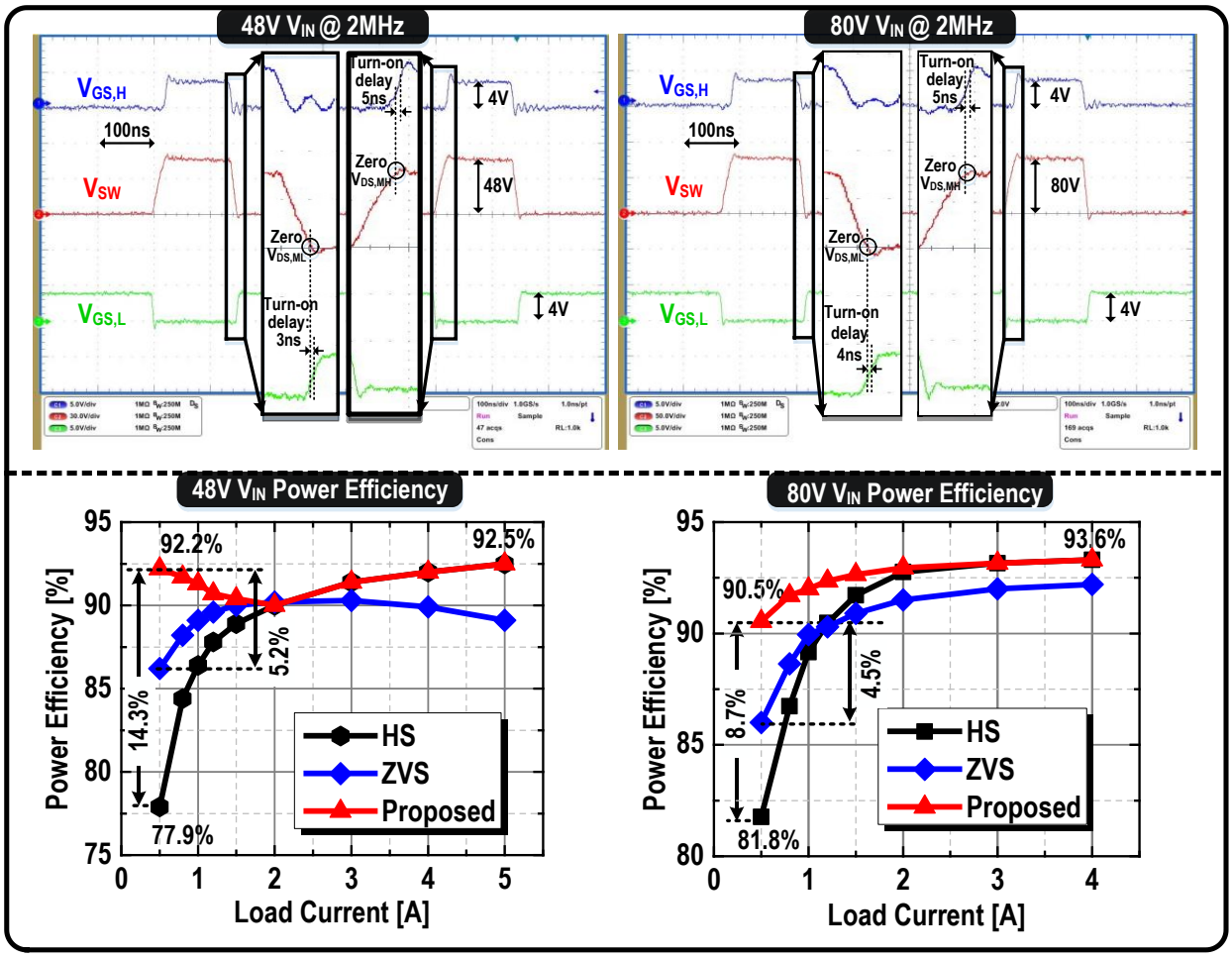



Figure 5.19. Measured ZVS operation and turn-on delays of high-side and low-side GaN FETs, and measured converter power efficiencies at 2MHz $f_{SW}$ under different $V_{IN}$ and $I_O$ conditions.

Table 5.3. Performance summary and comparisons with the prior art.

| | EPC 9205 [67] | TI-AN2149 [68] | Vicor-PI3105 [69] | **This Work** |
|---|---|---|---|---|
| Topology | Non-isolated Buck | Non-isolated Buck | Isolated Buck-Boost | **Non-isolated Buck** |
| Power Transistors | 100V GaN FET ×2 | 100V GaN FET ×2 | N/A | **100V GaN FET ×3** |
| Switching Method | HS | HS | ZVS | **HS / AZVT** |
| $V_{IN}$ (V) | 48 – 80 | 15 – 60 | 36 – 75 | **48 – 80** |
| $V_O$ (V) | 12 | 10 | 12 | **12** |
| Max. $P_O$ @48V $V_{IN}$ | 120W | 100W | 60W | **60W** |
| $F_S$ (kHz) | 700 | 800 | 900 | **2000** |
| $L_M$+$L_A$ (μH) | 2.2 + 0 | 2.7 + 0 | N/A | **1.5 + 0.82** |
| Total $C_O$ (μF) | 88 | 376 | 28.2 | **18.8** |
| Worst case $\Delta V_O$ (mV) | N/A | 75 | 175 | **100** |
| Full Load Power Efficiency | 95.8%(@48V,10A) | 93.9%(@48V,10A)<br>92.4%(@60V,7A) | 88%(@48V,5A)<br>87%(@60V,5A) | **92.5%(@48V,5A)<br>93.6%(@80V,4A)<br>@ 2MHz** |
| Light Load Power Efficiency | 86.5%(@48V,1A) | 87.5%(@48V,1A)<br>84.6%(@60V,1A) | 63%(@48V,0.5A)<br>61%(@60V,0.5A) | **92.4%(@48V,0.5A)<br>90.5%(@80V,0.5A)<br>@ 2MHz** |

## 5.4 Conclusions

A high-efficiency low-profile ZVT synchronous non-inverting buck-boost converter has been presented in Section 5.2. The proposed converter adopts an auxiliary circuit connecting between two switching nodes to create a transient current for ZVS turn-on of power transistors. Because the auxiliary circuit is only enabled in the vicinity of the transition and disabled during the rest of a switching period, the power loss of the auxiliary circuit can be minimized to improve the power efficiency of the converter. Compared with the previously-reported QSW-ZVS and traditional ZVT counterparts, the proposed converter requires smaller number of auxiliary components, resulting in significant reductions in the converter volume and power loss. The

measurement results of the hardware prototype verify proper operation of the proposed converter under different operation modes, input voltages and load currents.

In addition, a regulation loop of auxiliary current has been presented in Section 5.3. The proposed auxiliary current control scheme adaptively adjust the on-time of the auxiliary switch such that the current ripple in the auxiliary inductor is always regulated to just enough for ZVT operation of the main FETs. Furthermore, the auxiliary switch turns on under zero-current switching (ZCS) condition for minimized switching loss. The measurement results verify that the light load efficiency can be improved by 14.3% due to the contribution of the proposed auxiliary current control scheme.

# CHAPTER 6

# CONCLUSIONS

## 6.1 Conclusions

Enhancement-mode GaN FETs gain more and more popularity in DC-DC converters, and the merits of low $R_{DSON}$ and small parasitic capacitance make it also a good candidate for soft-switched converters. However, the large reverse conduction loss of GaN FETs requires adaptive dead time control in the soft-switched converters, and the ultra-fast dv/dt transition of $V_{SW}$ also requires improved reliability in HV level shifters. This dissertation proposes a slope-sensing-based ZVS detector that enables near-optimum dead time control for any loading condition (either full-ZVS operation or partial-ZVS operation). With less than 13ns ZVS detection delay, the proposed near-optimum dead time control scheme can help to reduce the power less by 1.28W at $V_{IN}$ = 150V and $f_{SW}$ = 2MHz, improving power efficiency by 0.77%. This dissertation also proposes a differential-mode noise blanker that helps to prevent the common-mode noise caused by fast dv/dt transition from propagating in the level shifter and hence increase the dv/dt noise immunity to at least 45V/ns.

Another limitation of the non-isolated soft-switched converters is the required auxiliary components. Especially, the number and volume of auxiliary components prohibits the traditional soft-switched topologies from being extended to multi-phase converters and non-inverting buck-boost converters that has more than one active switch. This dissertation proposes two types of architectural development to share one branch of the auxiliary circuit between two

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active switches. In particular, a QSW-ZVS cell is shared between the two switch nodes of two interleaved phases to assist ZVS operation of two active switches; and a QSW-ZVT cell is shared between the two switch nodes of the non-inverting buck-boost converter to assist ZVS operation of two active switches. Both new architectural development show less count and volume of auxiliary components with improved power efficiency.

Finally, although the conduction loss in a ZVT auxiliary branch can be much smaller than that in a traditional ZVS auxiliary branch, the power efficiency of a ZVT converter is still adversely affected under light load condition because the auxiliary conduction loss cannot scale with load current using the traditional fixed on-time control of the auxiliary switch. This dissertation proposes an adaptive auxiliary current control scheme such that the current ripple in the auxiliary branch is modulated by the main inductor current (or the load current) by adaptively adjusting the on-time of the auxiliary switch. Since the auxiliary current is always just enough for ZVS operation, the additional conduction loss caused by the auxiliary branch is minimized in any given load condition, and the power efficiency can be optimized in very wide range of load. Particularly, the light load efficiency can be improved by 14.5% with proposed adaptive auxiliary current control scheme

## 6.2 Future Works

It is worth to figuring out if the proposed adaptive auxiliary current control scheme can be applied in a multi-phase ZVT converter with the auxiliary components shared between the interleaved phases. If possible, the conduction loss and the BOM cost can be further reduced systematically. Also, since the auxiliary inductor current is in DCM all the time, it is possible to

regulate the on-time of the auxiliary FET instead of regulating its peak current such that the wide bandwidth current sensor in Figures 5.14 and 5.15 for the auxiliary branch can be avoided.

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## BIOGRAPHICAL SKETCH

Lin Cong was born in Beijing, China, and received a Bachelor of Science degree (with highest honor) from Beijing University of Technology, Beijing, China, in 2008. He received a Master of Science degree from Texas Tech University, Texas, USA in 2010. In the spring semester of 2013, he joined the Integrated Power Laboratory in the Department of Electrical Engineering at The University of Texas at Dallas. His research interests include driver and control circuit design for soft switched converters, especially with GaN FETs. Lin has published 4 IEEE journal papers and 9 IEEE conference papers in the area of power IC design.

In the summer of 2016, he worked as an analog design intern at Kilby Labs, Texas Instrument Inc., Santa Clara, where he focused on boot circuit design for high voltage three-level converters. Since the summer of 2017, he transitioned to the part-time PhD program at UTD and started to work as an analog designer at Texas Instruments on a full-time basis.

## CURRICULUM VITAE

## PUBLICATIONS

### Journal Papers:

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