THE SEQUENCE DETECTION ALGORITHM AND ERROR-TOLERANT ADC FOR HIGH-PRECISION DETECTION IN HIGH-ENERGY PHYSICS EXPERIMENT

by

Hongda Xu

APPROVED BY SUPERVISORY COMMITTEE:

Yun Chiu, Chair

Carl Sechen

Jingbo Ye

Andrea Fumagalli

To my wife, Siwen and our parents

THE SEQUENCE DETECTION ALGORITHM AND ERROR-TOLERANT ADC FOR HIGH-PRECISION DETECTION IN HIGH-ENERGY PHYSICS EXPERIMENT

by

HONGDA XU, BE, MS

DISSERTATION

Presented to the Faculty of

The University of Texas at Dallas

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY IN

ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT DALLAS

MAY 2017

ACKNOWLEDGMENTS

I would like to express my appreciation to all those people who helped and supported me to go through this long research journey and touch the finale.

Among those people, firstly, I would like to give my sincere appreciation to my supervisor, Professor Yun Chiu. I feel very glad to have worked under his guidance in the past few years, not only because of the knowledge he taught me, but also for the methodologies of thinking and solving problems I have learned from him, which will benefit me in my future career as well as in my life. More importantly, he led me into the analog- and mixed-signal design world, a fantastic world.

Also, I would like to thank Dr. Datao Gong from Southern Methodist University (SMU) for the beneficial discussions every week in my signal processing project. Many good ideas were inspired during those discussions. I thank Xiandong Zhao from SMU for his help to generate data for my simulations in the signal processing project. I want to thank Professor Jingbo Ye from SMU and his lab (Drs. Datao Gong, Tiankuan Liu, and Kent Liu, to name a few) for the strong support for my ADC project and help with the irradiation tests.

I would like to thank Dr. Ling Du, the visiting PhD student (at that time) from the University of Electronic Science and Technology of China. The conversation with him about the ADC project always led me to think more and to think deep, and there was a lot of fun when he shared with me his hiking experiences and plans. I thank Yongda Cai for his specialist on the FPGA programming which helped a lot on the ADC tests.

I am grateful to Mitch Newcomer at the University of Pennsylvania. He is a kind and respectable scholar. Without his selfless assistance, the two in-field irradiation tests could not have been conducted in a timely manner.

I would like to thank all of my group members: Yuan Zhou, Bo Wu, Benwei Xu, Brian Elies, Sudipta Sarkar, Yangqing Li, Hai Huang, Shuang Zhu and Yongda Cai. Miscellaneous talks with them are always instructive for my research work and enrich my life in the lab.

Last but not the least, I am sincerely grateful to my family. I am deeply indebted to my parents and my parents-in-law for their lasting support and backup. Special thanks to my wife, Siwen for her support and for accompanying me on this journey. Without her love and sacrifice, I cannot achieve my goals.

March 2017

THE SEQUENCE DETECTION ALGORITHM AND ERROR-TOLERANT ADC FOR HIGH-PRECISION DETECTION IN HIGH-ENERGY PHYSICS EXPERIMENT

Hongda Xu, PhD
The University of Texas at Dallas, 2017

Supervising Professor: Yun Chiu, PhD

The fast-moving digital-driven very large scale integration (VLSI) development enables the implementation of complex and sophisticated digital signal processing (DSP) algorithm and stimulates the generic structure of "analog-to-digital converter (ADC) plus DSP" to be applied in many application scenarios. Benefits from this general trend, the frontend electronics in the readout system and the backend DSP algorithms for the next phase ATLAS experiment at large hadron collider (LHC) is under evaluation and design for high-precision detection. This research focused on the backend DSP algorithms and the related ADC design, which is required to be error-tolerant to convey high-performance analog-to-digital (A/D) conversion in the radiation environment.

Based on the seminal work of liner optimal filter (LOF) by W. Cleland *et al*., this research devised a sequence detection algorithm with the extended LOF and decision feedback equalization (DFE) technique to remove the increasing pileup effects in the high-luminosity environment. Various Monte Carlo simulations validate the effectiveness of this proposed algorithm – neither missing detection nor false alarm is observed for medium- to high-energy

particles. The proposed algorithm maintains the same detection efficiency in the upgrade phase as that of the LOF in the current phase, demonstrating its superior performance to that of the LOF for high-luminosity detection.

As required by the proposed algorithm, high-resolution and throughput ADCs are in demand to deliver large dynamic range, high SNR and fast sample rate. The operation environment also requires the ADC to be radiation-tolerant. A two-step split successive-approximation register (SAR) ADC is proposed and implemented in 65-nm CMOS to fulfill the above requirements. The prototype measures 78.5 dB peak SNDR and over 100 dB peak SFNR at 35 MS/s sample rate and >70 dB SNDR and >88 dB SFDR up to Nyquist frequency at 75 MS/s sample rate. Besides, multiple new error detection techniques are developed and implemented. Combining with the redundancies allocated in each circuit hierarchy, the prototype demonstrated 100% error correction rate in the single event effect (SEE) test with proton beam. Less than 1 dB maximum degradation of SNDR and SFDR in the total ionizing dose (TID) with X-ray proves its long-term radiation-tolerant feature. The prototype consumes 22.2 mW at 40 MS/s and 24.9 mW at 75 MS/s sample rate.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivation

In the past few decades, benefit from the scaling advantage of complementary metal oxide semiconductor (CMOS) technology, digital driven very-large-scale integration (VLSI) designs were moving fast in term of operation speed, integration density and power efficiency, boosting the computational performance dramatically. This trend and progress enables the implementation of complex and sophisticated digital signal processing algorithms. To the contrary, analog integrated circuit (IC) designs experience increasing difficulties and challenges with technology scaling, especially in the nowadays ultra-deep submicron CMOS process nodes. The intrinsic gain of single metal oxide semiconductor (MOS) transistor decreases; and the shrink of supply voltage also reduces the signal level, resulting in deteriorate signal-to-noise ratio (SNR). Therefore, the inherent robustness of the digital circuits together with its increasing computational powers stimulates the bloom of digital-assist analog circuit designs to mitigate the impairments of analog circuit. Moreover, the "analog-to-digital (A/D) conversion plus digital signal processing" becomes a generic structure in many application scenarios, which in turn, pushes the cutting-edge analog-to-digital converter (ADC) designs advancing rapidly.

All these transformations and advancements impact and benefit the high-energy physics community the same way, for the elevated performance of electronic devices and sophisticated digital algorithms provide the basis for accurate measurements and observations in particle collision experiments.

One example is the large hadron collider (LHC) [1], as shown in Figure 1.1, operated at European Organization for Nuclear Research (CERN[1]), an international collaborative project aiming to extend the frontier of particle physics research. Constructed on the boarder of France and Switzerland, the LHC consists of a 27-kilometer ring of superconducting magnets with a number of accelerating structures to boost the energy of the particles. Inside the accelerator, two high-energy proton beams travel at close to the speed of light before they are made to collide.

To detect the collision and the associated physics activities, several large detectors such as ATLAS[2] and CMS[3] are deployed along the ring. All the facilities are built underground on an average of 100 meter deep, so they can take advantage of the crust as a shield to stop radiations

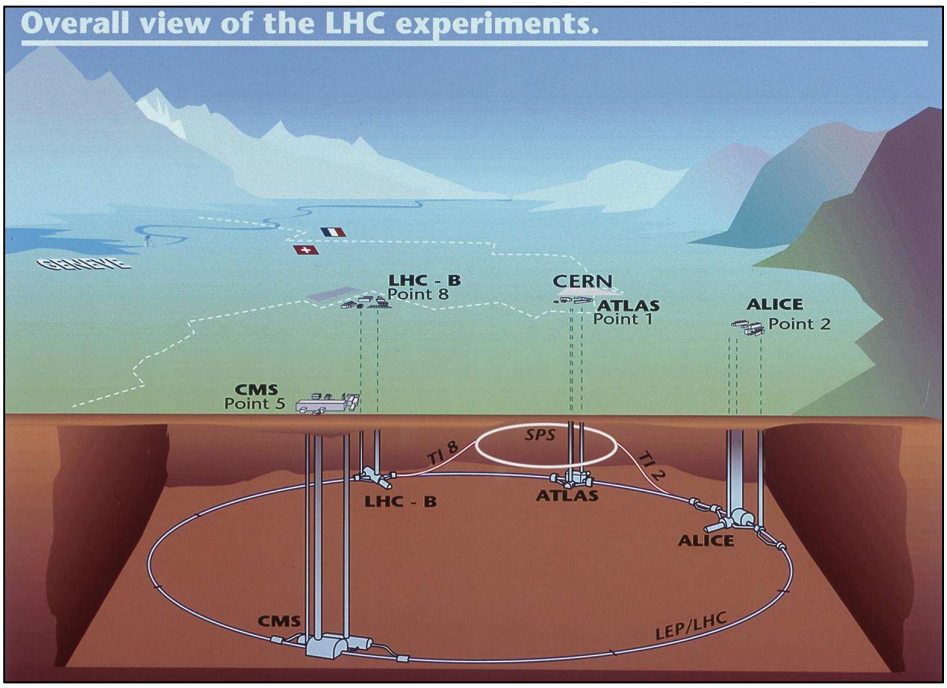


Figure 1.1. An overview diagram of the LHC [2]

[1] CERN is the acronym from its predecessor's French name – Conseil Européen pour la Recherche Nucléaire.

[2] ATLAS is the acronym of "A Toroidal LHC ApparatuS".

[3] CMS is the acronym of "Compact Muon Solenoid".

from the space. Those detectors are usually comprised of multiple layers of detector cells and signal readout system. In the readout, after the necessary signal conditioning, the analog signal is immediately sampled and quantized, having its digitized form transmitted to the backend for further processing. In the backend, digital signal processing algorithm is applied to estimate the energy of the particles that involved in the collision with those digitized data and the physical events are further reconstructed using these recovered energy information. Figure 1.2 is the diagram illustrates the ATLAS detector.

To create more interested physical events for study, the LHC is scheduled to boost the particle's energy for collision (higher luminosity) in each of its upgrade phase [3], whereas the upgrade put tighter requirements for the readout electronics and the increased physical events in each collision introduce more signal pileups, challenging the current digital signal processing

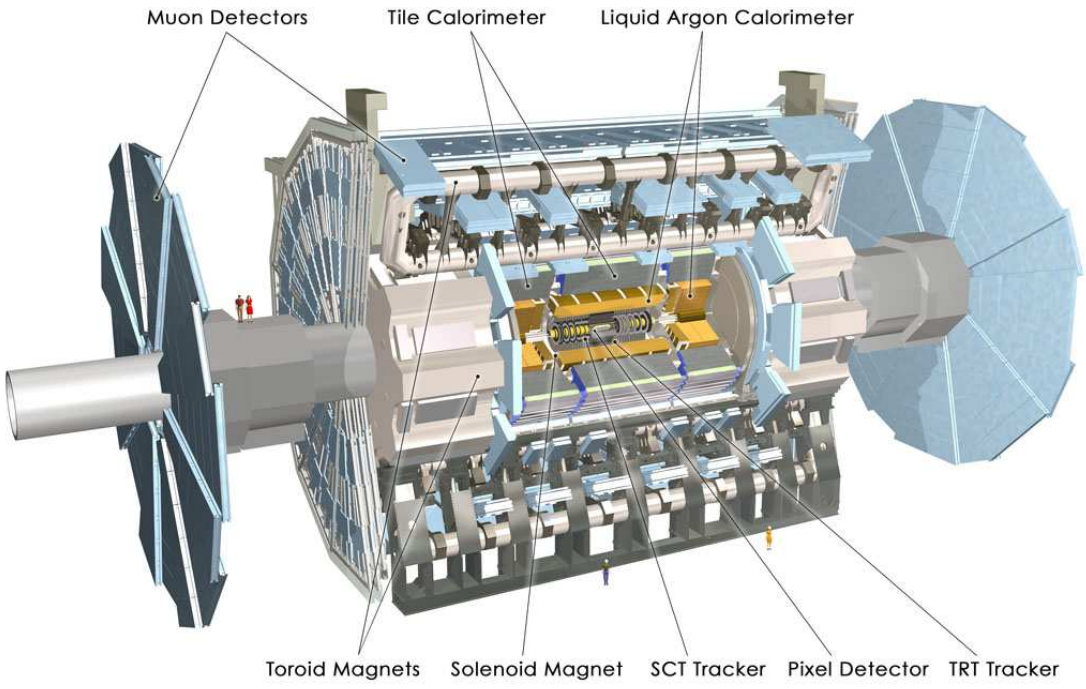


Figure 1.2. The ATLAS detector [4]

method. New or revised digital signal processing algorithm is in demand to accommodate the LHC upgrade for non-degrading detection efficiency. Meanwhile, the upgrades of the readout electronics should also be performed accordingly and considering the backend digital signal processing needs, where the A/D interface – the ADCs are the bottleneck. Large dynamic range of the detected signal and high operation speed of the LHC as well as the needs from the backend dictates the ADC to have high resolution and fast sample rate and the radiation environment requires the ADC to be error-tolerant, adding another layer of difficulties.

1.2 Research Goal

The goal of this research is to develop an optimum digital signal processing algorithm to perform high-resolution estimation on the particle's energy (in the form of signal amplitude) in high-luminosity environment after the LHC upgrade. Although the parameters used in this dissertation are from (and set for) the ATLAS experiment, the proposed algorithm can be generalized for similar readout applications.

Secondly, a high-speed, high-resolution and power efficient Nyquist ADC is aimed to be designed and implemented to accommodate the stringent LHC upgrade needs as well as the signal processing demands. More importantly, the ADC is desired to have additional radiation-tolerant feature to survive in the radiation environment.

1.3 Dissertation Outline

The dissertation is organized as follow. In chapter 2, the system configuration and model will be first briefly discussed, followed by the signal processing needs for the electronic upgrades in the system evolution. Chapter 3 reviews different estimation methods and makes a comparison.

Based on the prior arts, a sequence detection algorithm is proposed in Chapter 4 and verified by various Monte Carlo simulations. According to the signal processing requirements, a high-speed, high-resolution radiation-tolerant ADC design is presented in Chapter 5 to Chapter 7, which, in Chapter 5, error-tolerant techniques are discussed; followed by the general design issues covered in Chapter 6; and measurement results in Chapter 7. A conclusion is drawn in Chapter 8.

CHAPTER 2

SYSTEM CONSIDERATIONS

In this chapter, the current system configuration of the signal readout in the ATLAS liquid argon (LAr) calorimeter (an energy measurement apparatus) will be given firstly, followed by the LHC evolution road map. This background information will help to clarify the origin of the problems. Then, the proposed readout architecture for Phase-II upgrade [5] is presented for system modeling and all the noise and interference sources and mechanism is discussed toward the end of this chapter.

2.1 Current Readout System Configuration

Liquid ionization calorimeter is an energy-measurement detector widely deployed in many particle physics experiments [6]. In the ATLAS experiment, the medium in the calorimeter is liquid argon. The simplified readout frontend of the calorimeter is sketched in Figure 2.1, which consists of preamplifiers, shapers, switched-capacitor array (SCA), mux and ADCs. The output signal of the detector is amplified and filtered by the frontend analog circuitries and stored in the SCA. A trigger system selects part of the analog samples produced by potential "interested" physical events and those samples are digitized by the ADCs. The LHC operates at 40 MHz, i.e.

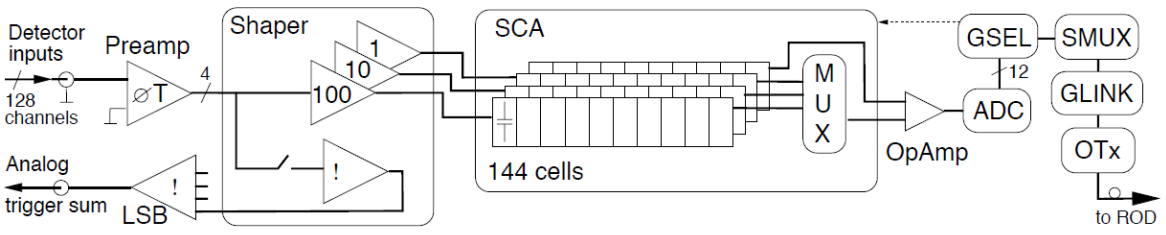


Figure 2.1. Simplified block diagram of the current readout frontend [7]

there is a collision (called bunch crossing, BC) in every 25 ns. The ADC operates at 5 MHz, and compared to that of the LHC, it does not fast enough to digitize all the analog samples at each BC. The SCA and trigger system becomes a necessity.

2.2 LHC Evolution Road Map

As described in the previous chapter, in order to obtain more "materials" for study, namely the physical events in each BC, the LHC is scheduled to increase its luminosity in each of the upgrade phase. Figure 2.2 depicts the LHC and high-luminosity LHC (HL-LHC) evolution road map. It can be seen that there are three long stops (LS1, LS2 and LS3) for the installations of electronics in each upgrade. This research focuses on the Phase-II upgrade. After this experiment upgrade, the luminosity of the LHC is intensively boosted.

2.3 Readout Frontend in Phase-II Upgrade

A simplified block diagram of the proposed Phase-II readout frontend board (FEB) [5] is shown in Figure 2.3. The FEB will include a bunch of preamplifiers, analog shapers, ADCs, and serializer/deserializer (SerDes).

One major difference to Figure 2.1 is the removal of the SCA, which reduces the analog design complexity, but requires the ADC to be clocked at higher sampling frequency to synchronize with the LHC operation frequency. Besides, the three-gain scheme (of the shapers as in Figure 2.1) is under evaluations to reduce to the two-gain scheme in the Phase-II upgrade, which translates to higher dynamic range for the ADCs. On the other hand, the removal of the SCA enables the continuous sampling, with more samples available, elaborate digital signal processing algorithm can be devised.

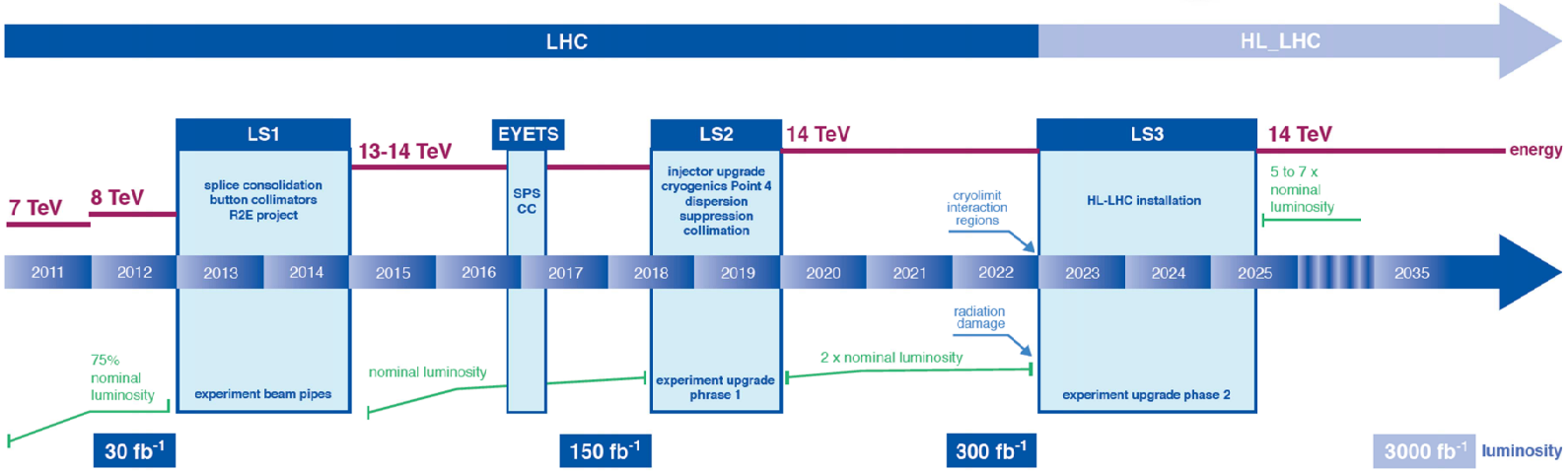


Figure 2.2. LHC and HL-LHC evolution road map [8]

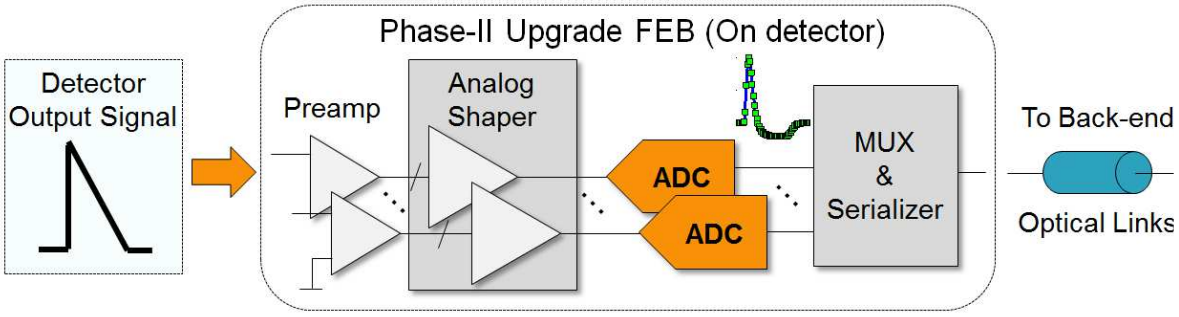


Figure 2.3. Simplified block diagram of the frontend board (FEB) in Phase-II upgrade

2.4 Signal Model and Interference Sources

In the LAr calorimeter, since the liquid gap between the electrode plates is narrow, about 2 mm, the ionization triggered by the electromagnetic shower is instantaneous and the process is followed by a drift of the electrons towards the anode plate. Thus, the detector output signal is modeled as a triangular current pulse as shown in Figure 2.3. Liquid ionization calorimeter usually exhibits a long drift time, dependent on the drift velocity and the gap size [9]. For ATLAS liquid argon calorimeter, the drift time is about 450 ns, much longer than the bunch crossing time which is 25 ns. To avoid long dead time and to reduce noise in the measurement, a CR-RC^2 pulse shaper – a chain of integrator (RC) and differentiator (CR) circuits – is employed in the analog front-end after the preamplifiers [10]. The general transfer function of a CR^m-RC^n shaper is given as follows.

$$H(s) = \frac{(s\tau_s)^m}{(1+s\tau_s)^{m+n}} \tag{2.1}$$

where τ_s is the time constant of the shaper. An intuitive way of understanding the functionality of the shaper is that the integrator limits the input bandwidth and slows down the rising edge of the current pulse for analog-to-digital conversion (ADC) while the differentiator restores the

baseline quickly by removing the long tail of the pulse to reduce the possibility of signal pileup. Carefully choosing the time constant τ_s gives a smooth shaper output waveform with minimal pedestal recovering time, which can largely relax the ADC sample rate while retaining sufficient samples for post-processing.

Figure 2.4 sketches the shaped waveform as well as the triangular current pulse from the detector. The parameters used for modeling waveforms in Figure 2.4 are extracted from [7] for ATLAS liquid argon calorimeter, e.g., a CR-RC^2 shaper with τ_s set to 13 ns, and the output peaking time is approximately 50 ns.

While detection is a general signal-processing topic that has been well studied, what we are most interested in particle physics experiments is how to precisely measure the amplitude and timing information of the sampled waveform of the detector output – the amplitude A represents

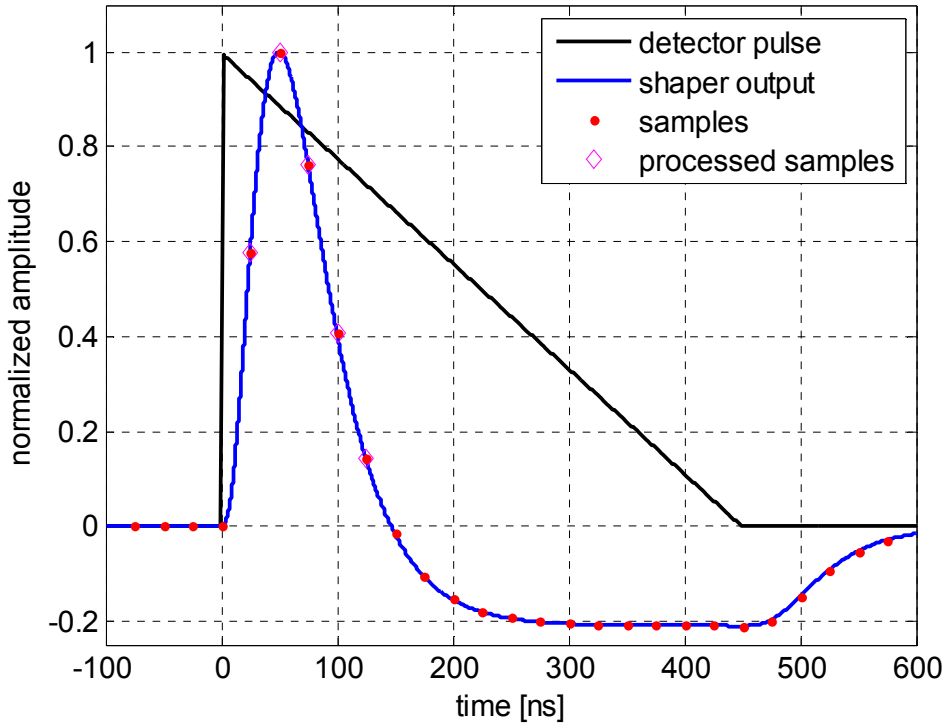


Figure 2.4. Signal waveform at the output of the detector (black) and the shaper (blue)

the energy of the incident particle shower and the timing signifies the arrival time τ of the particle thus our ability to correlate signals and events in time.

Two leading noises are typically considered in the estimation process, the electronic noise and the pileup noise. At their origin, the dominant electronic noises, e.g., thermal noise and shot noise, are white. Temporal correlation however is introduced by the detector front-end processing, particularly the pulse shaper, and needs to be considered in the optimization procedure. Unlike the stochastic deteriorating effect of the electronic noise, the signal pileup by nature is deterministic and should be treated as inter-event interference (IEI). In particle detectors operating at high luminosity levels, many events are produced at each bunch crossing. The densely packed calorimeter cells and the long tail of the detector current pulse tend to aggravate the IEI problem, leading to an equivalent model termed pileup noise to highlight the statistical property of the effect rather than its deterministic physical origin. Besides, the random pulse arrival delay at the sampling instant of the ADC introduces new errors in timing, which should be also taken into considerations.

CHAPTER 3

ESTIMATION ALGORITHMS

In line with the differing physical origins of the electronic noise, pileup noise and their effects on the detection process, we will concentrate on the amplitude and timing estimation for LAr calorimeters considering electronic noise only in the rest of this chapter. Pileup effect will be included in the discussion in Chapter 4.

3.1 χ^2 Exhaustive Search

Considering the correlation between the noise samples introduced by the shaper, the χ^2 function can be defined as follows [11]:

$$\chi^2(A,\tau) = \sum_{i\,j} \left(S_i - Ag(t_i - \tau)\right) V_{ij} \left(S_j - Ag(t_j - \tau)\right) \tag{3.1}$$

where V_{ij} is the weight matrix for the measured samples. **V** is the inverse of the noise autocorrelation matrix **R** with $R_{ij} = \langle n_i \cdot n_j \rangle$ and n_i is the noise sample.

The χ^2 function defines a non-negative quadratic error surface as a function of A and τ between the noisy samples S_i and the known pulse shape $g(t_i)$ as sketched in Figure 3.1. A straightforward approach to determine the best estimate for A and τ is to perform an exhaustive search on the error surface. Albeit not computationally efficient, the exhaustive search result establishes a baseline for the estimation approaches covered in the subsequent sections.

The Monte Carlo simulation results of the χ^2 exhaustive search are shown in Figure 3.2 and Figure 3.3 – the performance of the method is limited by the finite step size employed by the search algorithm. No obvious trend for the estimation error is observed.

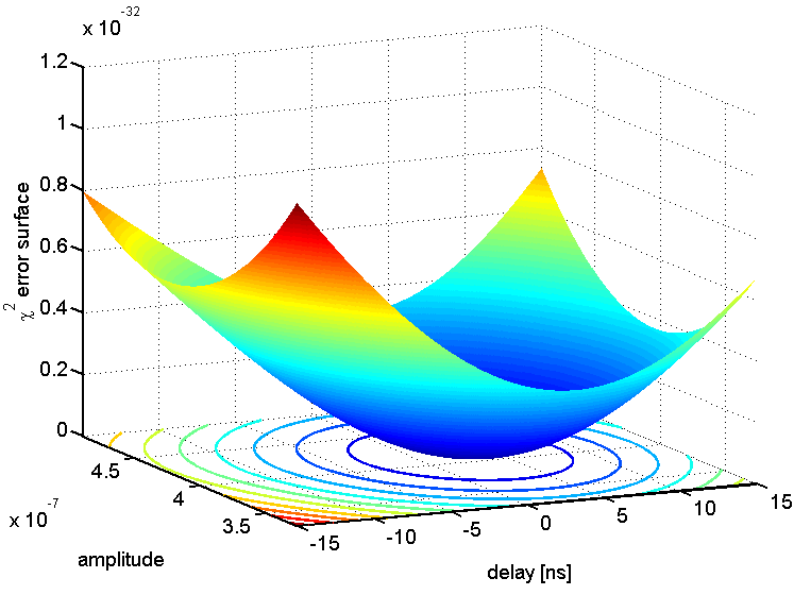


Figure 3.1. The quadratic error surface of the χ^2 function in terms of A and τ.

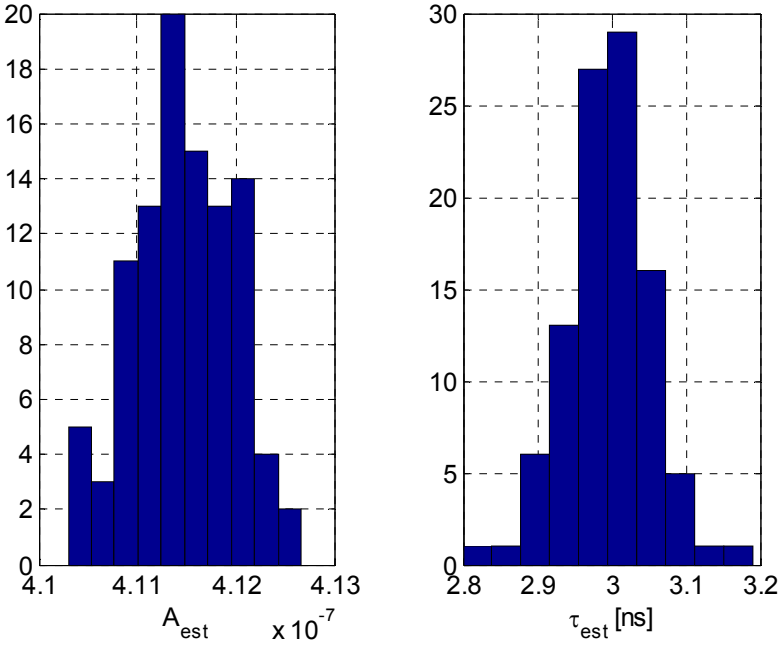


Figure 3.2. Histogram of 100 Monte Carlo runs for amplitude (left) and arrival time (right) estimation using the χ^2 exhaustive search method. The standard deviation of the detector noise is set to 10% the peak value of the detector current pulse. The sample period T = 25 ns, A_0 = 4.1134×10^{-7}, and τ_0 = 3 ns.

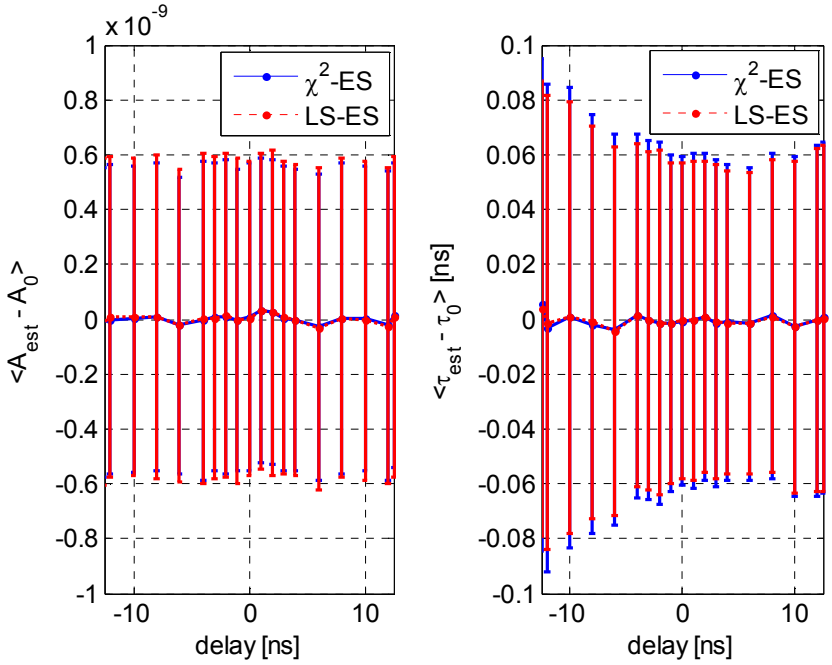


Figure 3.3. The χ^2 versus the least-square search results of 1000 Monte Carlo runs: the mean estimation error and standard deviation for amplitude A_{est} (left) and arrival time τ_{est} (right). $\tau_0 = [-T/2, T/2]$. Other simulation parameters are identical to those of Figure 3.2.

3.2 Least-Square Exhaustive Search

The derivation of the weight matrix **V** (or the noise autocorrelation matrix **R**) requires precise knowledge of the impulse response of the detector front-end. The computation of the χ^2 function in Equation (3.1) also dictates N^2 multiplications for N samples when the off-diagonal entries of **V** are nonzero. In practice, the magnitude of the off-diagonal entries of **R** can be small relative to the main diagonal entries. In such cases, the **V** matrix can be well approximated by the identity matrix. Thus, Equation (3.1) reduces to

$$\chi^2(A,\tau) = \sum_i \left(S_i - Ag(t_i - \tau)\right)^2 \tag{3.2}$$

This is identical to the least-square metrics to fit N samples to the known pulse shape $g(t)$.

In the Monte Carlo simulation, the above argument is confirmed with a CR-RC^2 pulse

shaper. Again, an exhaustive search is employed to determine the optimal fit of the five samples to $g(t)$. The estimation errors for A and τ are plotted in Figure 3.3 and overlaid with the χ^2 exhaustive search results – the two results are nearly identical.

3.3 χ^2 with First-Order Taylor Expansion

Taylor expansion can be performed on $g(t)$ in the vicinity of $\tau = 0$ to reduce the computation complexity of the χ^2 function, i.e.,

$$Ag(t_i - \tau) \approx Ag(t_i) - A\tau g'(t_i) \tag{3.3}$$

where $g'(t)$ is the first-order derivative of $g(t)$. Thus,

$$\chi^2 = \sum_{i\,j} (S_i - \alpha_1 g_i + \alpha_2 g'_i) V_{ij} (S_j - \alpha_1 g_j + \alpha_2 g'_j) \tag{3.4}$$

where $\alpha_1 = A$ and $\alpha_2 = A\tau$.

Compared to Equation (3.1), Equation (3.4) defines a first-order approximated quadratic error surface in terms of A and τ, which can be used to perform a search or to directly derive a closed-form analytical solution to the problem. The latter has been done in [11] and results are quoted as follows

$$\begin{aligned} \alpha_1 &= \frac{1}{\Delta}(Q_2 Q_4 - Q_3 Q_5) \\ \alpha_2 &= -\frac{1}{\Delta}(Q_1 Q_5 - Q_3 Q_4) \end{aligned} \tag{3.5}$$

where

$$
\begin{aligned}
Q_1 &= \sum_{ij} g_i V_{ij} g_j \\
Q_2 &= \sum_{ij} g'_i V_{ij} g'_j \\
Q_3 &= \sum_{ij} g'_i V_{ij} g_j \\
Q_4 &= \sum_{ij} g_i V_{ij} S_j \\
Q_5 &= \sum_{ij} g'_i V_{ij} S_j \\
\Delta &= Q_1 Q_2 - Q_3^2
\end{aligned}
\tag{3.6}
$$

3.4 Linear Optimal Filtering

A linear optimal filtering technique was proposed in [11] to minimize the computing effort involved in determination of the amplitude and arrival time information. The formulation of the optimal filter is quoted as follows

$$
\begin{aligned}
A &= \langle u \rangle = \left\langle \sum_i a_i S_i \right\rangle \\
A\tau &= \langle v \rangle = \left\langle \sum_i b_i S_i \right\rangle
\end{aligned}
\tag{3.7}
$$

The coefficients of a_i and b_i are given as

$$
\begin{aligned}
\mathbf{a} &= \lambda \mathbf{V}\mathbf{g} + \kappa \mathbf{V}\mathbf{g}' \\
\mathbf{b} &= \mu \mathbf{V}\mathbf{g} + \rho \mathbf{V}\mathbf{g}'
\end{aligned}
\tag{3.8}
$$

where $\lambda = Q_2/\Delta$, $\kappa = -Q_3/\Delta$, $\mu = Q_3/\Delta$, $\rho = -Q_1/\Delta$, and $\mathbf{Q}$ and Δ are defined in Equation (3.6).

The advantage of this technique is that the filter tap values are pre-calculated. Thus, the computation can be performed on the fly when data samples arrive, suitable for continuously operated detectors such as the proposed upgrade for ATLAS. It is also useful in resource-constrained implementation, e.g., FPGA or DSP, or latency-sensitive applications.

It can be shown that linear optimal filtering is equivalent to the χ^2 method of first-order approximation [11]. The simulation results of both for A and τ are illustrated in Figure 3.4. It is interesting to note that the estimation error exhibits a quadratic dependence on τ as predicted by Equations (3.3) and (3.4) for truncating the second- and higher-order terms in the Taylor expansion.

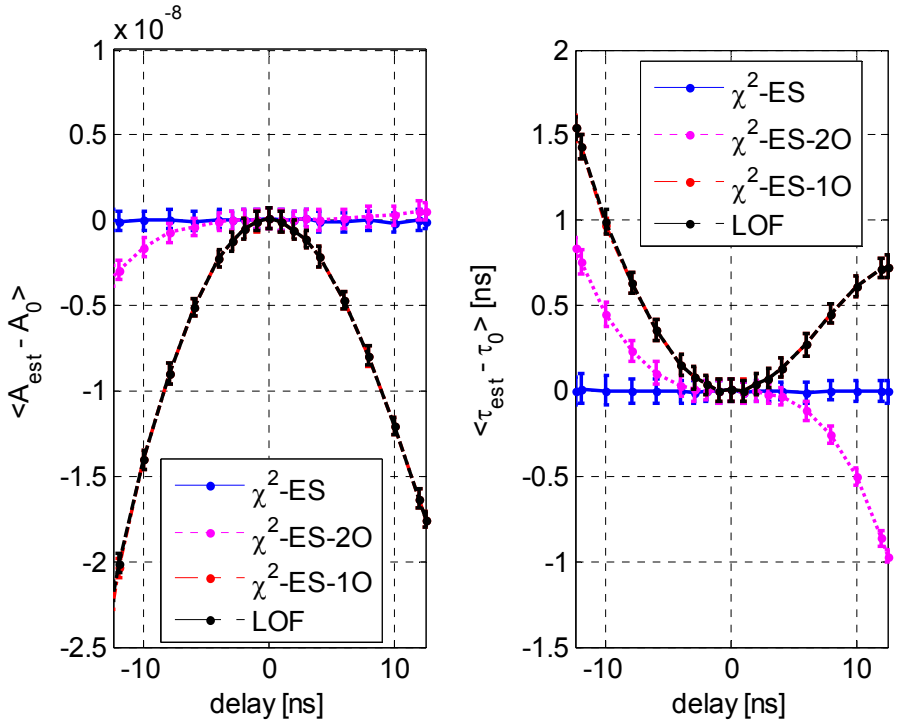


Figure 3.4. The simulation results of 100 Monte Carlo runs for the first-order χ^2 exhaustive search, linear optimal filtering, and second-order χ^2 exhaustive search: the mean estimation error and standard deviation for amplitude A_{est} (left) and arrival time τ_{est} (right). Simulation parameters are identical to those of Figure 3.3.

3.5 χ^2 with Second-Order Taylor Expansion

The first-order Taylor expansion of the χ^2 function leads to a rather large estimation error or bias when τ is large – −4.9% for amplitude and 12% for arrival time when τ reaches $\pm T/2$ in Figure 3.4. One way to mitigate the large error is to iterate the series expansion and Equation (3.4) by recalculating the **g'** and **Q** or, in the linear optimal filtering case, re-derive the filter tap values a_i and b_i and iterate Equation (3.7). Simulation results are shown in Figure 3.5 for linear optimal filtering with two iterations. There is computing overhead in either case. Another solution is to resort to a second-order Taylor expansion,

$$Ag(t_i-\tau)=Ag(t_i)-A\tau g'(t_i)+\frac{1}{2}A\tau^2 g''(t_i) \tag{3.9}$$

where $g''(t)$ is the second-order derivative of $g(t)$.

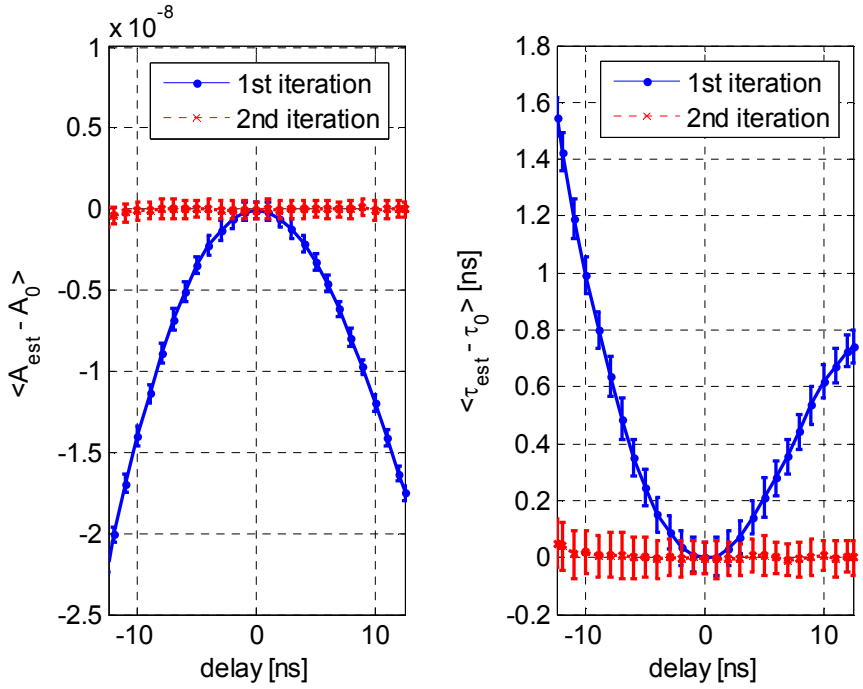


Figure 3.5. The simulation results of 100 Monte Carlo runs for the linear optimal filtering case with two iterations. Simulation parameters are identical to those of Figure 3.3.

The error surface of the second-order approximation can be similarly defined as of Equation (3.4). However, the nonlinearity of the second-order term excludes the possibility of a closed-form analytical solution. Thus, an exhaustive search is performed instead and the simulation results are shown in Figure 3.4 as well. We note that the estimation error in this case exhibits a cubic dependence on τ as the truncation error in Equation (3.9) is dominated by the third order.

Table 3.1. Efficiency comparison between gradient-descent and exhaustive search methods

Method	Gradient Descent	Exhaustive Search
Iterations	680*	603201
Computations per iteration	90 multiplications 18 additions 3 comparisons	30 multiplications 6 additions 1 comparison

*Averaged over different delay times.

3.6 Gradient Descent Approach

As simulation results evidenced so far, the exhaustive search approach produces the best estimation accuracy at the cost of high computation complexity. To improve the efficiency of the search, a gradient-descent approach is devised. As illustrated in Figure 3.1, the bowl-shaped error surface of the χ^2 function exhibits a global minimum. Starting from a random initial point on the surface, a search direction can be derived by comparing the value of the function at the current position to those offset by a step size away in both A and τ direction. The current position is then advanced in the direction that minimizes the function value. The process is iterated until convergence at the bottom of the surface. Simulations for the gradient-descent approach were performed with four random starting point and the resulting search paths are plotted in Figure 3.6. Comparing to the exhaustive search method in which the whole error surface is evaluated,

the gradient-descent approach significantly reduces the computation involved. Table 3.1 compares the typical required number of iterations for the two cases.

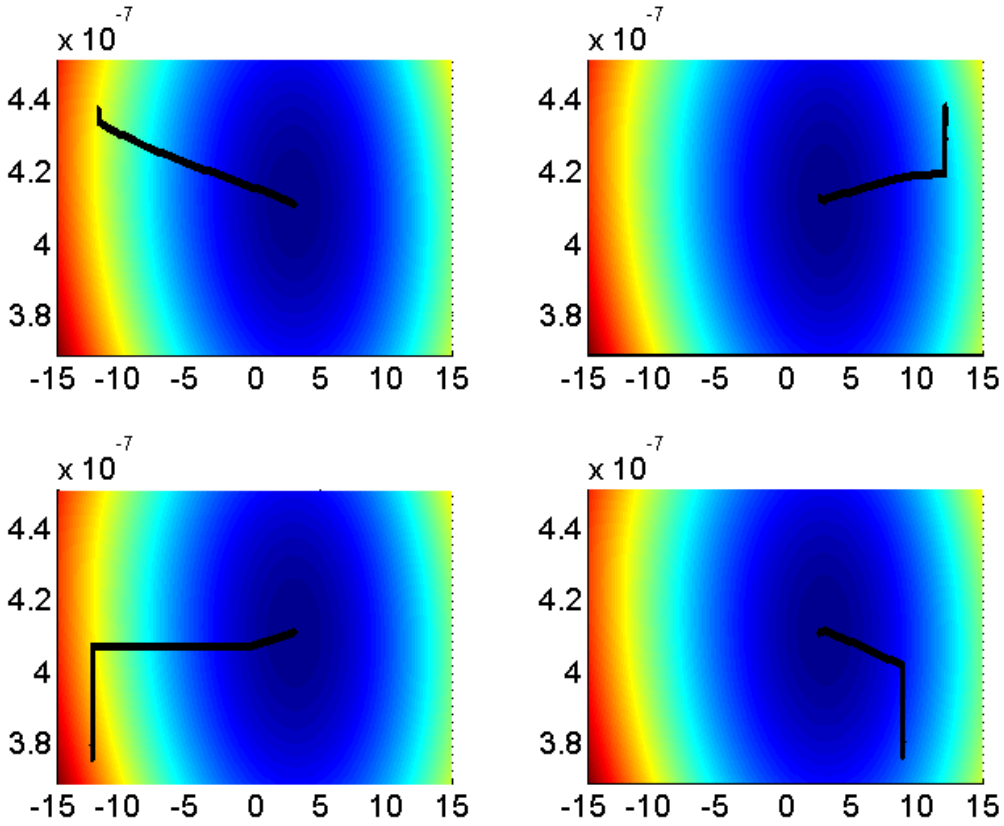
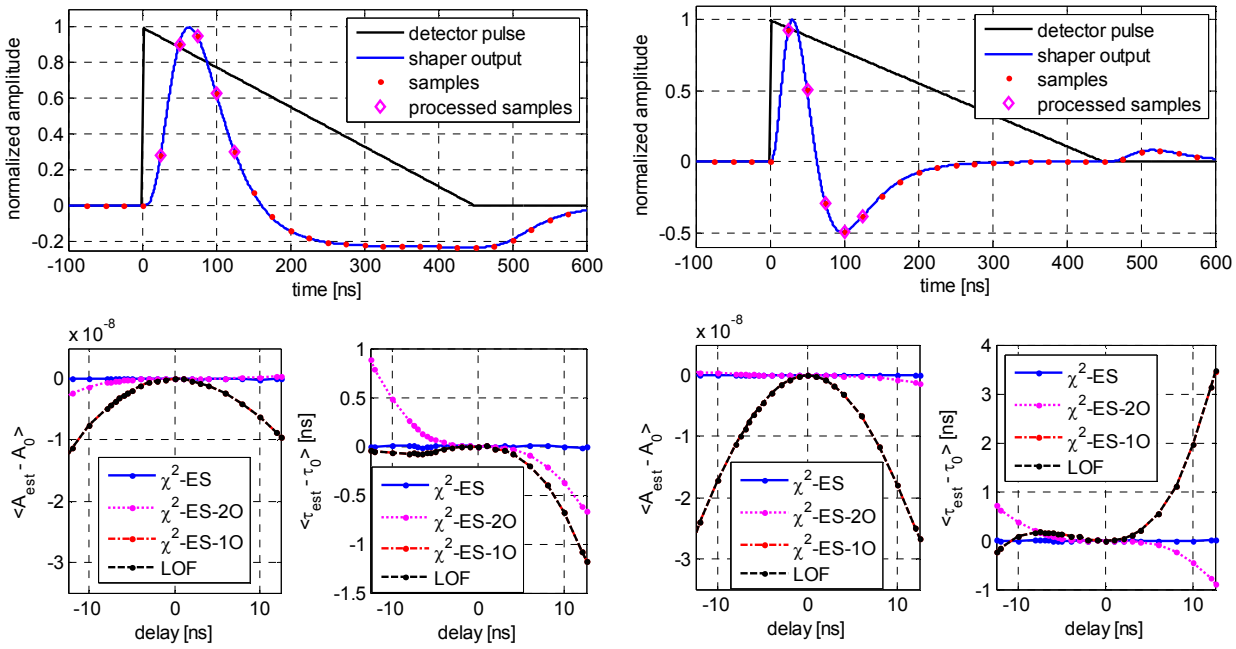


Figure 3.6. Simulated gradient-descent search paths for four random starting point on the error surface of the χ^2 function. The *x*-axes are delay (in ns) and the *y*-axes are amplitude.

3.7 Other Shapers

The amplitude and timing estimation techniques covered in the above section are also tested with CR-RC^3 and CR^2-RC^2 pulse shapers. For the 40-MHz sample rate, the peak of $g(t)$ falls in the middle between two samples in contrast to the case of the CR-RC^2 shaper in which the peak is very close to a sample point. Figure 3.7 plot the simulation results for the amplitude and timing estimation along with the input and output waveforms of the shaper. The skewed error curve reveals the asymmetry of the series expansion at off-peak sample points.



(a) (b)

Figure 3.7. (a) The simulation results of 100 Monte Carlo runs for CR-RC^3 shaper. Simulation setup is identical to that of Figure 3.3. Standard dev. bars are not shown for clarity. (b) The simulation results of 100 Monte Carlo runs for CR^2-RC^2 shaper. Simulation setup is identical to that of Figure 3.3. Standard deviation bars are not shown for clarity.

3.8 Wiener Filter[1]

Another approach to address the same estimation problem involves the application of Wiener filter [12], whose principle is demonstrated in Figure 3.8. The objective of the Wiener filter is processing the input signal $x(n)$ to maximally approximate a known signal $d(n)$ by suppressing any uncorrelated noise in the input $x(n)$. If a linear FIR filter is adopted, then the tap values of the Wiener filter can be learned adaptively by minimizing the mean square error (MSE) in Equation (3.10).

---

[1] © 2014 IEEE. Portions adapted in section 3.8 to section 3.11, with permission. H. Xu, *et. al.*, "On the performance of linear optimal filter and Wiener filter for signal detection in liquid ionization calorimeters," *IEEE Nuclear Science Symposium and Medical Imaging Conference* (*NSS/MIC*), Seattle, WA, 2014.

$$E\left[e^2(n)\right] = E\left[d(n) - y(n)\right]^2 = E\left[d(n) - \sum h(k)\,x(n-k)\right]^2, \tag{3.10}$$

where, $h(n)$ is the impulse response of the Wiener filter.

In contrast to the method of LOF, the Wiener approach does not offer a closed-form expression for the optimum filter such as that of Equation (3.7). However, it also does not require information about the noise statistics, i.e., the matrices **V** and **R**, in devising the optimal estimation filter. Once the precise information of physics from training samples is known, the only data necessary to determine the optimum filter structure are a large number of training samples, which may dictate some upfront training cycles for the filter to operate properly. In addition, there is no approximation like that of Equation (3.3) involved to arrive at a final solution, albeit the filter often still takes a linear FIR form at the end for implementation or adaptation reasons. Because of these properties, the Wiener technique of estimation does not suffer from the non-zero Δt (using Δt and τ interchangeably, same below) problem experienced by the LOF approach – the Wiener training result is actually *in situ*, i.e., it will adapt to whatever operating condition it encounters, resulting in an unbiased estimation as long as it is properly trained *a priori*.

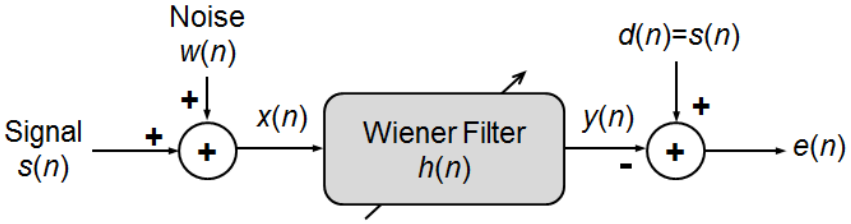


Figure 3.8. Conceptual diagram illustrating the working principle of the Wiener Filter.

Different training algorithms can be implemented to learn the filter tap values in the Wiener approach; for instance, the least mean square (LMS) algorithm or the least squares (LS) algorithm. For the single pulse case (i.e., not a sequence of pulses) examined in this chapter, the LS algorithm is adopted to exercise the learning of tap values, as described in Equations (3.11) and (3.12).

$$\begin{bmatrix} S_1(1) & S_1(2) & \cdots & S_1(n) \\ S_2(1) & S_2(2) & \cdots & S_2(n) \\ \vdots & \vdots & \ddots & \vdots \\ S_m(1) & S_m(2) & \cdots & S_m(n) \end{bmatrix} \begin{bmatrix} h(1) \\ h(2) \\ \vdots \\ h(n) \end{bmatrix} = \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_m \end{bmatrix}, \tag{3.11}$$

$$\mathbf{h} = \left(\mathbf{S}_L^T \mathbf{S}_L\right)^{-1} \mathbf{S}_L^T \mathbf{A}_L, \tag{3.12}$$

A total of m sets of signal samples produced by m sets of corresponding amplitudes $A_1,\ldots A_m$ and arrival time delays $\Delta t_1,\ldots \Delta t_m$ are organized in the matrix of $\mathbf{S}_L$ for the learning process. In each set of signal samples (each row of $\mathbf{S}_L$), n samples are collected for the learning of the n tap weights of the filter, which are obtained in one shot given by (3.12).

The constraint on the form of $H(s)$ to be invertible will pose some technical difficulty for studying the shaper function used in the ATLAS experiment, as will be seen in Section 3.11.

3.9 (Whitening + Matched) Filter

According to the optimal signal detection theory in presence of noise [13], the maximum SNR at the detection filter output is achieved when the impulse response of the filter is matched to the input signal (strictly speaking, matched to the complex conjugate of the time reversal of the input signal) when the noise is white. This gives rise to the matched filter (MF) approach in practice.

When the input noise is not white, a so-called whitening filter (WF) can be placed in front of the MF to flatten the spectrum of the shaped noise. The MF can then still be employed to treat the post-whitening samples to obtain a similar result as in the white noise case. However, the approach inherently makes the assumption that the colored noise can be whitened with a WF (that often also takes a linear FIR form). This may not be true if the transfer function of $H(s)$ contains zeros in the right half plane (RHP) or on the $j\omega$-axis – the WF thus constructed may not be stable. For the cases when $H(s)$ is invertible, we term the cascade of WF and MF the WMF in this dissertation, which is shown in the diagram of Figure 3.9.

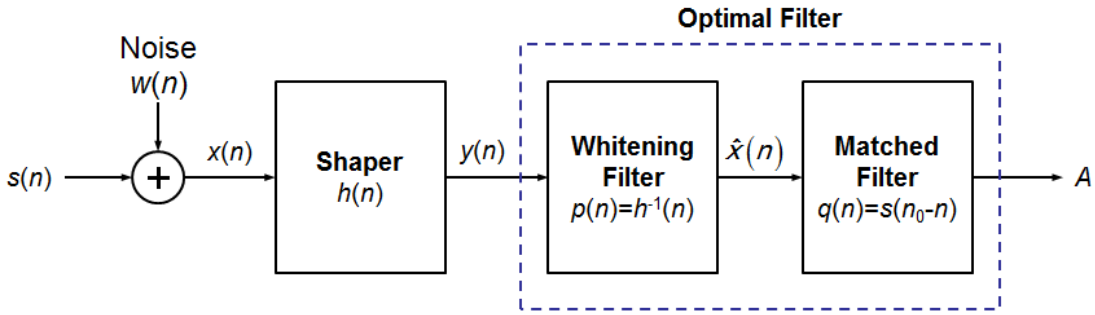


Figure 3.9. Conceptual diagram for optimal signal detection with colored noise. The optimum filter is formed by the cascade of a whitening filter (WF) and a matched filter (MF).

3.10 Equivalence between the Methods

If we recognize that the optimum estimation of the pulse amplitude is unique, then we must and should be able to relate the three filtering approaches outlined in Section 3.4, 3.8 and 3.9, namely, the LOF, the Wiener filter, and the WMF (for the case when $H(s)$ is invertible). In other words, some equivalence must be established in between the three methods. This is especially true when considering the fact that in practice the three filters all take a linear FIR form, as given in Equation (3.13).

$$A = \sum_i a_i S_i \,, \tag{3.13}$$

where a_i is the filter tap value and S_i is the signal sample.

All three filters share the same FIR form and they are all constructed to optimize certain statistics of the filtered signal samples. For the LOF, the best estimate of A in the WLS sense is obtained by minimizing the χ^2 [11]; for the Wiener filter, its tap weights are trained with the MMSE criterion [14]; while for the WMF, the combined effect of the MF and WF is to maximize the SNR of the filtered signal [9, 10]. In the following section, we resort to Monte Carlo simulations to further examine this equivalence.

3.11 Monte Carlo Simulation

3.11.1 Simulation Setup

As mentioned in Section 3.9, zeros located on the $j\omega$-axis of the shaper transfer function $H(s)$ pose problems for inversion by the WF. Unfortunately, the actual shaper employed in the ATLAS LAr calorimeter of (3.14) has four LHP poles and one zero at DC.

$$H(s) = \frac{\tau s}{(\tau_0 s + 1)(\tau s + 1)^3}, \tag{3.14}$$

Once inverted, an integrator is created as part of the WF, which cannot be efficiently modeled by a time-domain simulator. To resolve this technical difficulty, we introduced another shaper, in addition to the ATLAS shaper, with the zero relocated to a non-zero position on the negative real axis such that we have a minimum-phase transfer function that is invertible. This is given in Equation (3.15).

$$H(s) = \frac{\tau s + 0.25}{(\tau_0 s + 1)(\tau s + 1)^3}, \tag{3.15}$$

Note that the shaper function of (3.15) is totally fictitious, with the sole purpose of establishing equivalence between the three estimation methods outlined in Section 3.4, 3.8 and 3.9.

Meanwhile, the ideal triangular input waveform (depicted in Figure 2.4) of the ATLAS experiment also displays a wide spectrum due to the piece-wise linear approximation. In addition, at the transition points the curve is also not differentiable. To avoid aliasing and a differentiation problem, a smoother, slow-varying Gaussian waveform is introduced, in addition to the original triangular waveform, for comparison. Figure 3.10 depicts this Gaussian pulse and its post-shaping waveform produced by the modified shaper of (3.15).

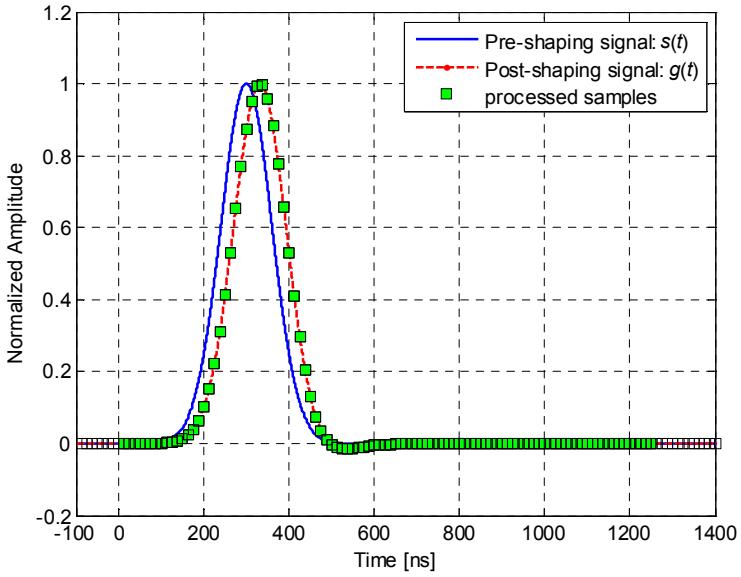


Figure 3.10. Input (solid) and post-shaping (dashed) signals of *Case-II*.

To summarize, with the original ATLAS shaper, signal waveform, and the newly introduced ones, we altogether have four combinations of cases as listed in Table 3.2. Out of the four, the non-invertible shaper with triangular waveform is denoted as *Case-I*, the most realistic

case that represents the ATLAS experiment most faithfully. In contrast, the invertible shaper with Gaussian waveform represents a fictitious but benign case, denoted as *Case-II*, used as a control group to compare with *Case-I*. Lastly, the other two combinations are not very meaningful and not considered further.

Other parameters of the simulation setup include a sample rate of 80 MSPS, a white noise added to the input of the shaper with varying power to be detailed shortly, neglected ADC quantization noise. Also, 100 signal samples are employed for estimation of A to avoid any waveform truncation error.

Table 3.2. The Four Combinations of Signal and Shapers

	Shaper with a Zero at DC (Non-invertible)	Shaper with a finite Zero (Invertible)
Triangular Waveform	Case-I	Not Considered
Gaussian Waveform	Not Considered	Case-II

3.11.2 Simulation Results

The input (pre-shaping) and output (post-shaping) signals of *Case-I* are depicted in Figure 3.11 and the filter tap values of the LOF and the Wiener filter are plotted in Figure 3.12. The LOF taps are calculated with (3.8) and the Wiener filter taps are learned with one million sets of training data with random A and Δt produced by Monte Carlo simulation. When Δt is set to zero, the two filter taps coincide with each other, representing a good agreement between the two approaches. Figure 3.13 displays the histogram of the estimate errors for these two cases – it is not surprising that the two curves overlap each other nearly exactly. For one million Monte Carlo

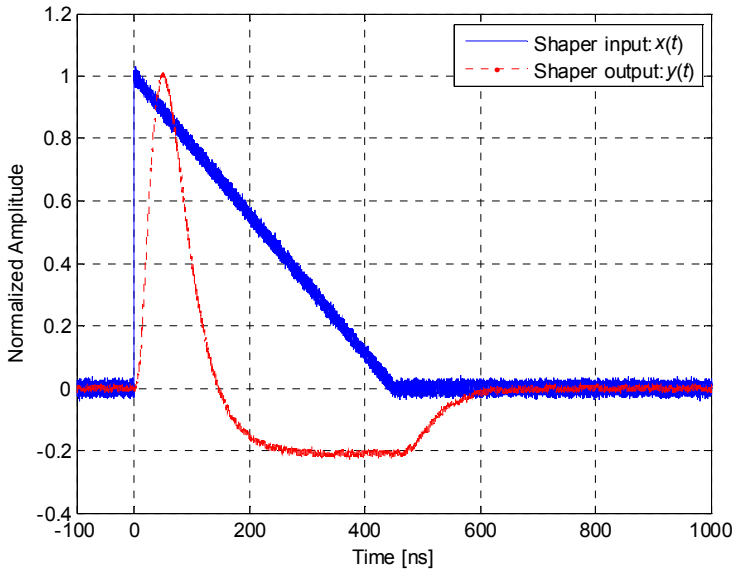


Figure 3.11. Simulated input and output signal waveforms of the shaper of the ATLAS experiment (*Case-I*).

runs, the two methods give close mean values of 1.04×10^{-5} and 1.66×10^{-5}, respectively, and the same standard deviation of 1.11×10^{-2} for the estimate error of A under the condition of a 74-dB SNR measured at the filter input (or the ADC output).

However, when the Wiener filter is trained with non-zero Δt values (from −1 ns to +1 ns and other conditions the same), its filter taps start to deviate from the LOF ones. The histogram of one million Monte Carlo runs with the same setup of the training data shows an unbiased characteristic for the Wiener method and a biased one for the LOF, as depicted in Figure 3.14. The bias of the LOF, as the analysis predicted, originates from the truncated Taylor series approximation of (3.3).

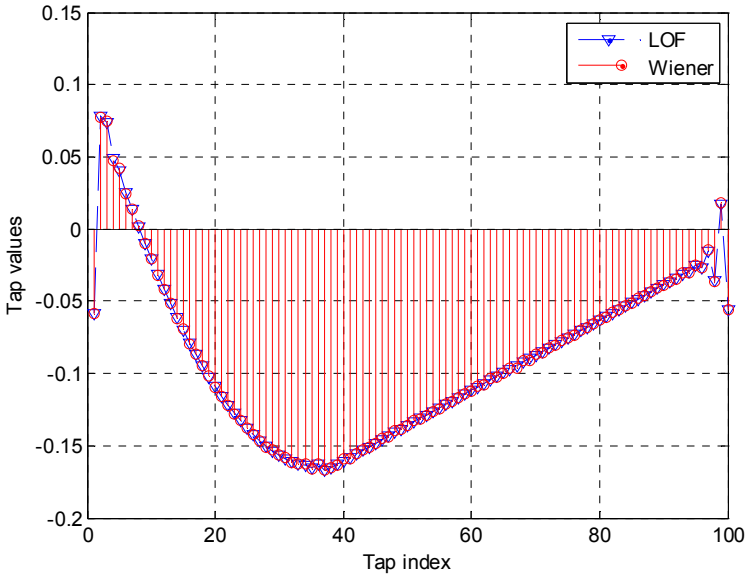


Figure 3.12. Tap values of the LOF (calculated) and of the Wiener filter (trained). The Wiener filter is trained with one million sets of events of Monte Carlo simulation with $\Delta t = 0$ and SNR = 74 dB.

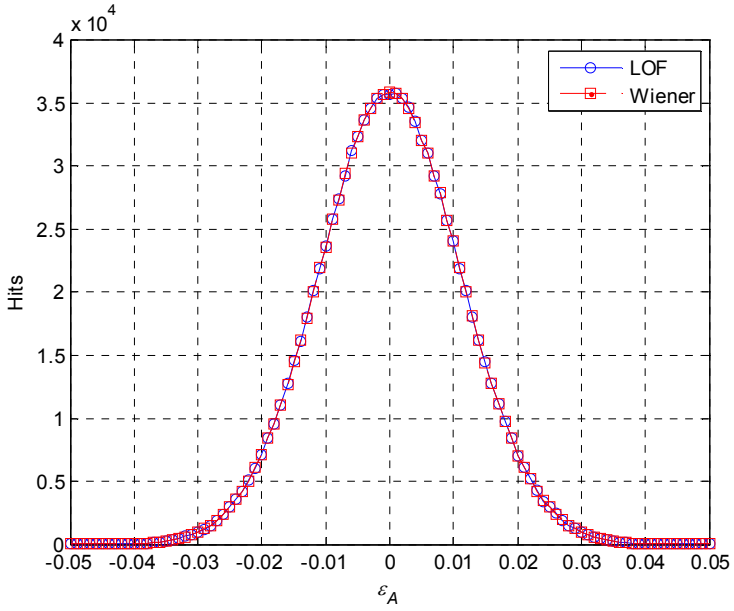


Figure 3.13. Histogram of the estimation errors of one million Monte Carlo runs using the two filters with tap values shown in Figure 3.12.

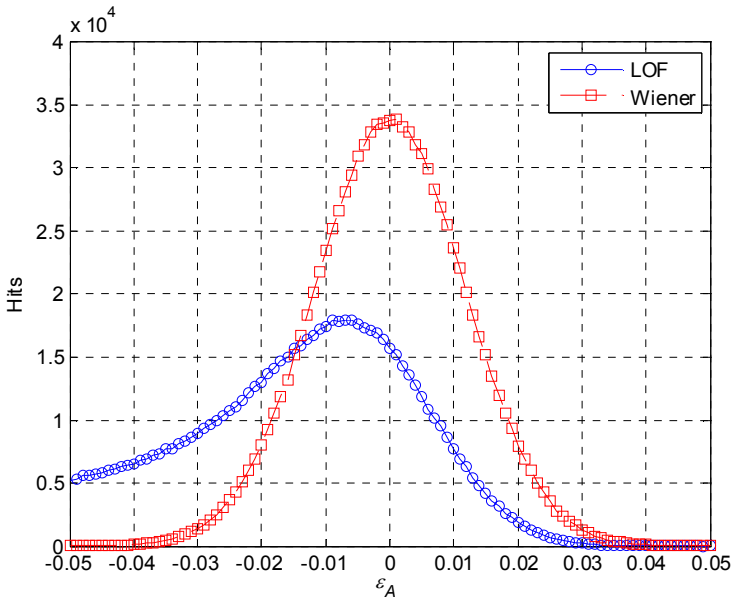


Figure 3.14. Histogram of estimation errors by repeating the simulation in Figure 3.13 with a non-zero $\Delta t \in$ U [−1 ns, +1 ns].

Another simulation is conducted to demonstrate the equivalence and difference between the Wiener and LOF, as shown in Figure 3.15. The Wiener taps are learned in two situations. In the first situation, $\Delta t = 0$ holds, and the filter is applied to the testing data sets with a non-zero Δt. The estimation results of this case display nearly identical statistic characteristics—both mean (μ) and standard deviation (σ) – as that of the LOF. Repeating the simulation with different noise power (SNR set to 62, 74, and 86 dB) does not seem to change the general behavior of the two results, proving the equivalence between the two methods with a zero arrival time delay. In the second situation, the Wiener filter is trained *in situ* with a non-zero Δt and tested with the same setup subsequently. In this case, no bias was observed in the Wiener results, and both the mean and standard deviation are much more superior to that of the LOF counterpart, as indicated in Figure 3.15.

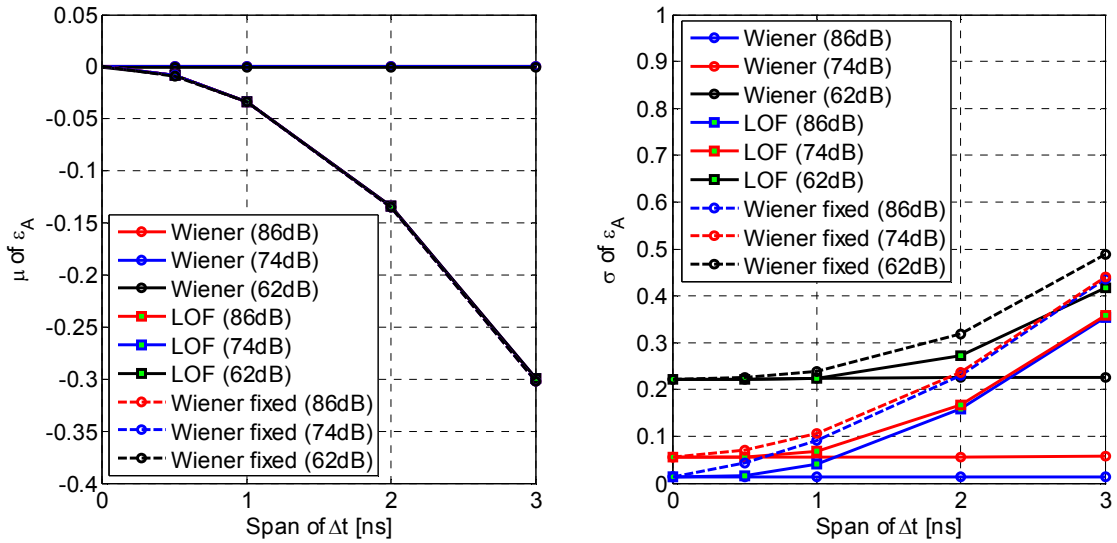


Figure 3.15. Comparison of the estimation results (mean and standard deviation) between the LOF and Wiener for two situations: 1) trained at $\Delta t = 0$ and then applied to varying cases of non-zero Δt (dashed line with round markers) and 2) *in situ* training (solid line with round markers).

Interestingly, once the Wiener filter is trained with a large Δt spread, the resulting filter can be applied to the estimation of cases with smaller Δt spreads, without degrading the estimation accuracy much (i.e., the mean and standard deviation of the estimation error are both well behaved). Figure 3.16 plots the simulation results obtained for such cases. Compared to the LOF results, although the mean and standard deviation are slightly larger for the case of $\Delta t = 0$, the estimation results are uniformly acceptable for all Δt values. Figure 3.17 depicts the evolution of the Wiener filter taps vs. Δt – we can clearly conclude that the Wiener taps can automatically adjust themselves to accommodate any non-zero Δt statistics once they are properly trained.

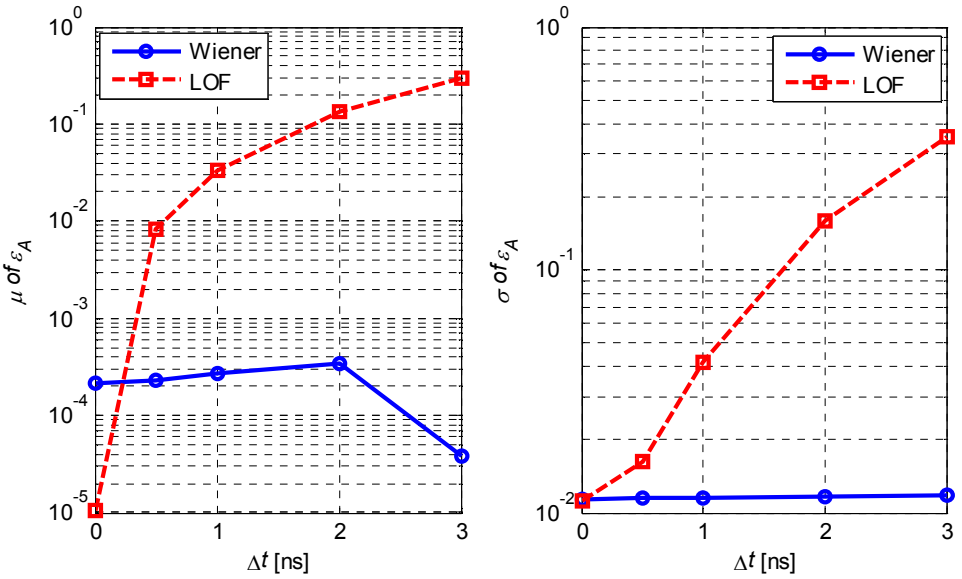


Figure 3.16. Estimation results (mean (absolute value) and standard deviation) of Wiener filter trained with fixed Δt statistics of $\Delta t \in$ U [−3 ns, +3 ns]. Five sets of data with different Δt statistics, $\Delta t \in$ U [$-t_x$ ns, $+t_x$ ns] with t_x = {0, 0.5, 1, 2, 3}, respectively, were tested. Each set contains one million Monte Carlo runs.

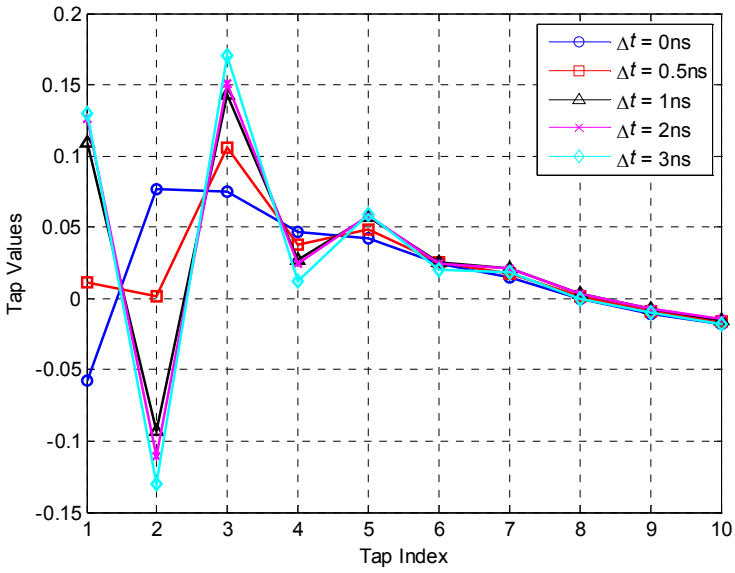


Figure 3.17. Evolution of the first ten taps of the Wiener filter as a function of the Δt of the training data for $\Delta t \in$ U [$-t_x$ ns, $+t_x$ ns] with t_x = {0, 0.5, 1, 2, 3}.

For the more benign *Case-II* (the waveforms are shown in Figure 3.10), the tap values of the Wiener, LOF and WMF are all plotted and compared in Figure 3.18 for $\Delta t = 0$. Again, all three filters highly agree to each other in this case.

For non-zero Δt values, similar simulations as those of Figure 3.15 were conducted and results are summarized in Figure 3.19. A less biased mean value and a smaller variation of the standard deviation were observed over Δt variations. This indicates that a smooth signal waveform and an invertible shaper all helped to minimize the discrepancies; however, the truncation error of (3.3) still exists, resulting in a biased estimation of the LOF. The WMF results are identical to those of the LOF.

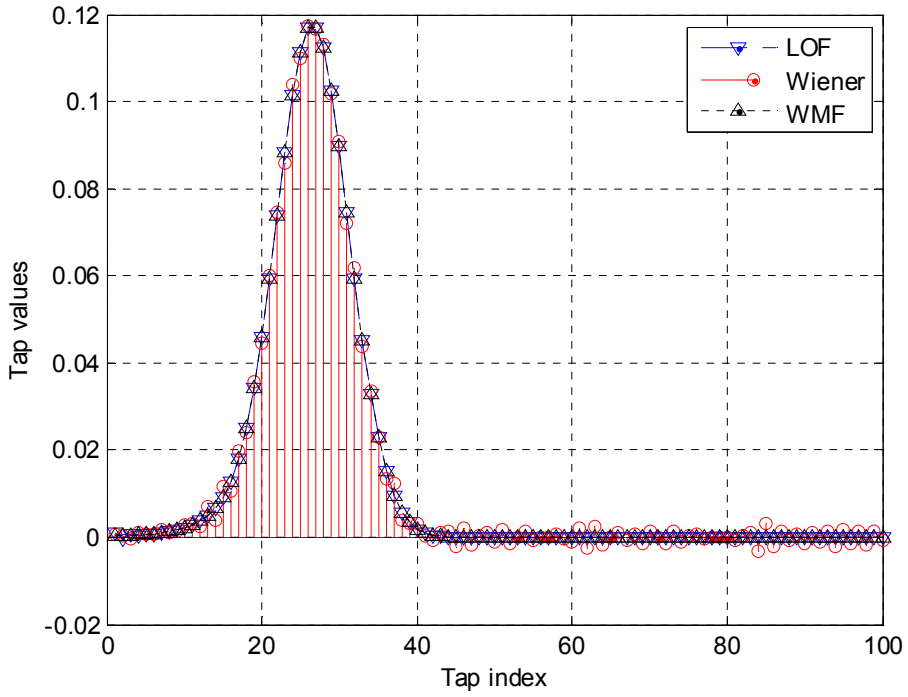


Figure 3.18. Plot of tap values of the LOF, Wiener and WMF of *Case-II*.

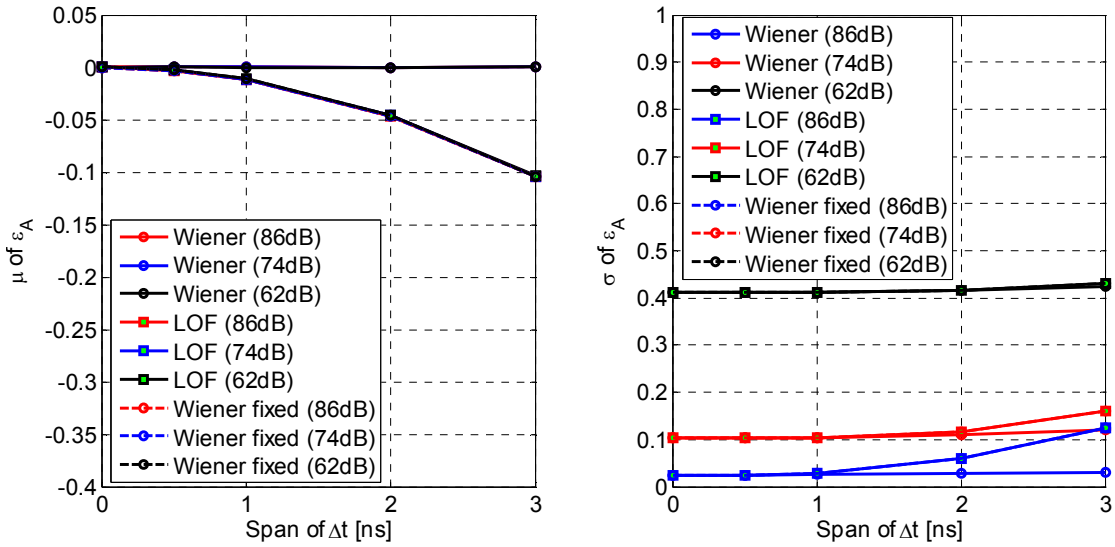


Figure 3.19. Results of the repeated simulation of Figure 3.15 for *Case-II*.

CHAPTER 4

SEQUENCE DETECTION ALGORITHM

4.1 Extended Linear Optimal Filter[1]

Without loss of generality, we consider the two-tuple out-of-time pileup case in which two shaped pulses with amplitude A_c and A_p arrive at the times $0T + \tau_c$ and $nT + \tau_p$, respectively, where T is the bunch crossing time (or the calorimeter sample period), τ_c and τ_p are the fractional part of the arrival times that satisfy τ_c, $\tau_p << T$, and n is a positive integer (n = 1, 2, …). An example of two-tuple pileup is illustrated in Figure 4.1 for n = 3.

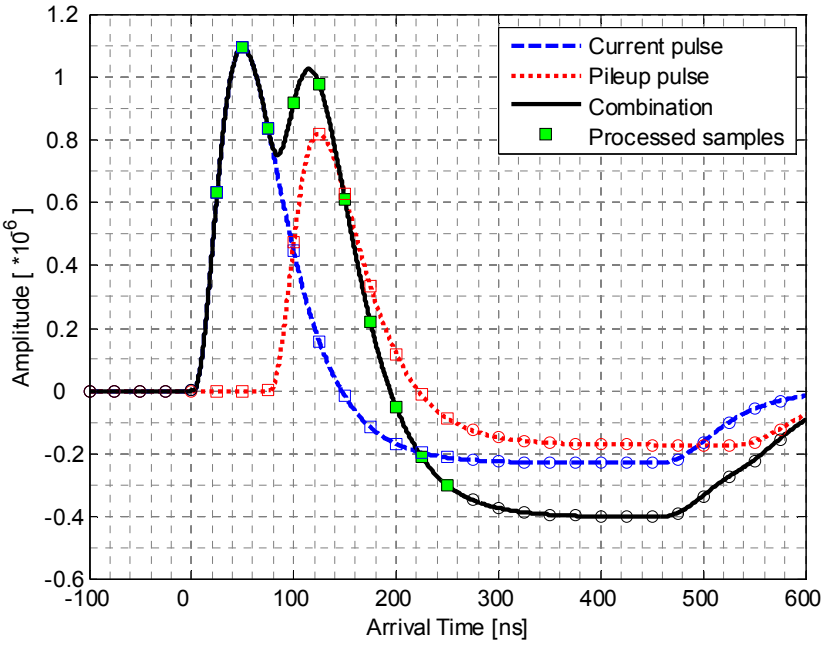


Figure 4.1. Two-tuple pileup with two pulses separated by 3T (= 75 ns). For this example, τ_c = τ_p = 0. A bipolar CR-RC^2 shaper with a time constant of 13 ns is assumed. A total of 10 signal samples are processed.

[1] © 2013 IEEE. Portions adapted, with permission. See reference [16].

Following the convention of [11], the χ^2 function for the two-tuple pileup can be defined as

$$\chi^2\left(A_c, A_p, \tau_c, \tau_p\right) = \sum_{i,j=1}^{m}\left(S_i - \sum_{c,p} Ag_i\right) V_{ij}\left(S_j - \sum_{c,p} Ag_j\right), \tag{4.1}$$

where S_i is the digitized sample acquired by the calorimeter, g_i or $g(t_i)$ is the sampled pulse shape known *a priori*, V_{ij} is the entry of the weight matrix **V**, the inverse of the autocorrelation matrix **R** of the sampled noise n_i ($R_{ij} = \langle n_i \cdot n_j \rangle$), and m is the number of samples employed. ΣAg_i contains two signal pulses and we identify the former as the current pulse and the latter as the pileup pulse, i.e.,

$$\sum_{c,p} Ag_i = A_c g\left(t_i - \tau_c\right) + A_p g\left(t_i - nT - \tau_p\right). \tag{4.2}$$

The χ^2 function defines a non-negative quadratic surface in the four-dimensional space spanned by A_c, A_p, τ_c, and τ_p. Its 2D projection in (A_c, A_p) subspace is sketched in Figure 4.2.

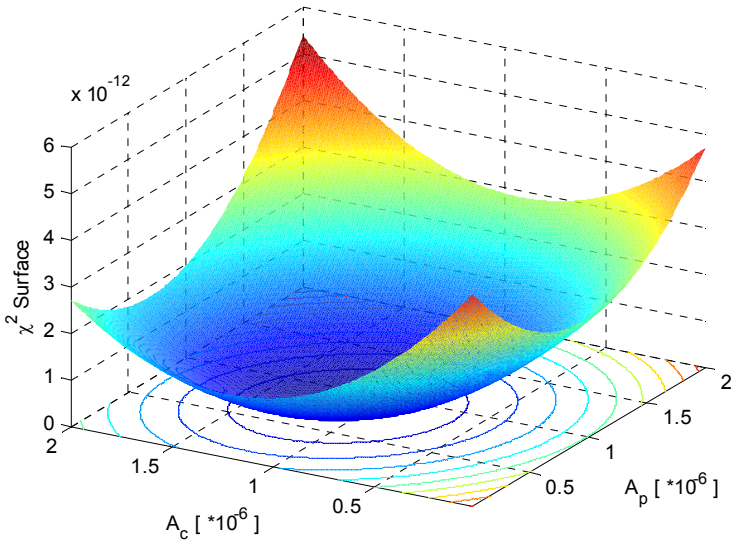


Figure 4.2. χ^2 surface versus A_c and A_p for τ_c = 1.016 ns, τ_p = -1.009 ns.

In the vicinity of integer bunch-crossing time points, i.e., $\tau_c \approx 0$ and $\tau_p \approx 0$, a Taylor expansion can be performed to linearize $g(t)$, yielding

$$\begin{aligned} A_c \cdot g\left(t_i - \tau_c\right) &\approx A_c\left[g\left(t_i\right) - \tau_c \cdot g'\left(t_i\right)\right], \\ A_p \cdot g\left(t_i - nT - \tau_p\right) &\approx A_p\left[g\left(t_i - nT\right) - \tau_p \cdot g'\left(t_i - nT\right)\right], \end{aligned} \tag{4.3}$$

where $g'(t)$ is the first-order derivative of $g(t)$, g'_c (= $g'(t)$) and g'_p (= $g'(t\text{-}nT)$) are to be evaluated at $\tau_c = 0$ and $\tau_p = 0$, respectively. Thus,

$$\begin{aligned} \chi^2\left(\alpha_1, \cdots, \alpha_4\right) \approx \sum_{i,j=1}^{m}\Big[\Big(S_i - \alpha_1 g_{ci} + \alpha_2 g'_{ci} - \alpha_3 g_{pi} + \alpha_4 g'_{pi}\Big)\cdot \\ V_{ij}\cdot\Big(S_j - \alpha_1 g_{cj} + \alpha_2 g'_{cj} - \alpha_3 g_{pj} + \alpha_4 g'_{pj}\Big)\Big], \end{aligned} \tag{4.4}$$

where we define $\alpha_1 = A_c$, $\alpha_2 = A_c\tau_c$, $\alpha_3 = A_p$, and $\alpha_4 = A_p\tau_p$. Note that g_p and g'_p are in practice to be evaluated for different values of n in (4.4). Four linear equations can be obtained by setting the partial derivatives of χ^2 to α_i to zero, i.e., $\partial\chi^2 / \partial\alpha_i = 0$,

$$\mathbf{Q\alpha} = \mathbf{G}^{\mathrm{T}}\mathbf{VS}, \tag{4.5}$$

where the column vector $\boldsymbol{\alpha} = (\alpha_1\ \alpha_2\ \alpha_3\ \alpha_4)^T$, the column vector $\mathbf{S}$ contains m measured samples, and the 4×4 matrix $\mathbf{Q}$ and the m×4 matrix $\mathbf{G}$ are given in Equation (4.6) and (4.7).

$$\mathbf{Q} = \begin{bmatrix} \sum g_i V_{ij} g_j & -\sum g_i V_{ij} g'_j & \sum g_i V_{ij} g_{j-n} & -\sum g_i V_{ij} g'_{j-n} \\ -\sum g_i V_{ij} g'_j & \sum g'_i V_{ij} g'_j & -\sum g'_i V_{ij} g_{j-n} & \sum g'_i V_{ij} g'_{j-n} \\ \sum g_i V_{ij} g_{j-n} & -\sum g'_i V_{ij} g_{j-n} & \sum g_{i-n} V_{ij} g_{j-n} & -\sum g_{i-n} V_{ij} g'_{j-n} \\ -\sum g_i V_{ij} g'_{j-n} & \sum g'_i V_{ij} g'_{j-n} & -\sum g_{i-n} V_{ij} g'_{j-n} & \sum g'_{i-n} V_{ij} g'_{j-n} \end{bmatrix}, \tag{4.6}$$

$$\mathbf{G} = \begin{bmatrix} g_1 & g'_1 & g_{1-n} & g'_{1-n} \\ g_2 & g'_2 & g_{2-n} & g'_{2-n} \\ \vdots & \vdots & \vdots & \vdots \\ g_m & g'_m & g_{m-n} & g'_{m-n} \end{bmatrix}. \tag{4.7}$$

Equation (4.5) reveals that the amplitudes and arrival times of the two pulses can be estimated by a set of linear FIR filters,

$$\boldsymbol{\alpha} = \left(\mathbf{Q}^{-1}\mathbf{G}^{T}\mathbf{V}\right)\mathbf{S}, \tag{4.8}$$

where $\mathbf{Q}^{-1}\mathbf{G}^{T}\mathbf{V}$ defines the LOF tap values.

4.1.1 Simulations

Single shot and Monte Carlo simulations are performed and the results are summarized in this section to validate the extend LOF approach described above and to present the estimation performance of the technique. The parameters used in the Monte Carlo simulation are extracted from the ATLAS experiment reports [7], [15].

Setup

Three functional blocks are established to model the behavior of the detection system: the input signal generator, the CR-RC^2 shaper, and the sampler.

The input current signal from the detector is modeled as an approximate right triangular waveform with the amplitude of 3μA/GeV—the steep rising edge is due to the rapid ionization and the slow falling ramp of 450 ns captures the charge drift process inside the electromagnetic barrel (EMB). A bipolar CR-RC^2 shaper follows the detector with a time constant of 13 ns for the differentiator and two integrators. The peaking time of the shaped output signal is thus 50 ns when the input arrives at time 0. The primary function of the shaper is to slow down the rising edge of the input pulse (by integration) for easy subsequent sampling and to shorten the slow tail of the pulse for fast baseline recovery (by differentiation). The band-pass frequency response of the shaper also rejects a large portion of the out-of-band noise. The post-shaping signal is

sampled at 40 MHz, namely, one sample per bunch crossing. Ten discrete-time signal samples are fed to the LOF, which is a ten-tap digital FIR filter, for amplitude and arrival time estimation. Additive white Gaussian (AWG) noise is imposed at the input of the shaper to imitate the thermal noise of the analog front-end circuitry for simplicity. Recovered amplitude and arrival time of the post-shaping signal is obtained at the output of the LOF.

A basic assumption in the LOF approach is that we have precise knowledge of the impulse response $h(t)$ of the shaper, and thus the post-shaping function $g(t)$ is known a *priori*. In the simulation, we will focus on the two-tuple pileup case only, and assume that the current pulse arrives approximately at $t = 0$, namely, $0T + \tau_c$, and the pileup pulse arrives at any subsequent bunch crossing times ranging from $1T$ to $4T$ (i.e., $n = 1$ to 4) with a small arrival time uncertainty τ_p.

Single shot simulation

From Equation (4.6) – (4.8), it can be seen that the coefficients of the LOF are in part determined by g_i, g'_i, g_{i-n}, and g'_{i-n}, which are $g(t)$ and $g'(t)$ sampled at t_i and t_{i-n}. Since Taylor expansion is only accurate in the vicinity of the expansion point, the LOF coefficients should be evaluated for $g(t)$ and $g'(t)$ at the corresponding $t = 0$ and $t = nT$ bunch crossings of the actual arrival times of the two pulses. However, n (= 1 to 4) is not known *a priori*.

To resolve this issue, one approach is to employ four filters in parallel to process the same set of input samples, each assuming a different value of n from 1 to 4. For every set of the samples, one of the four filters will deliver the most accurate estimates, for instance, when the pileup pulse arrives at $3T$, the estimation results will be the most accurate for the third filter. Quality Factor (QF), defined as the reciprocal of the χ^2 value, can be utilized to gauge the

estimation accuracy of the four filter outcomes. In our simulation, the one with the highest QF is selected to produce the final estimates. Figure 4.3 depicts the input and outputs of the four LOFs and displays the QF of the outcomes.

While parallelization presents a straightforward solution, it consumes much hardware resource, especially when thousands of calorimeter channels are processed with the same

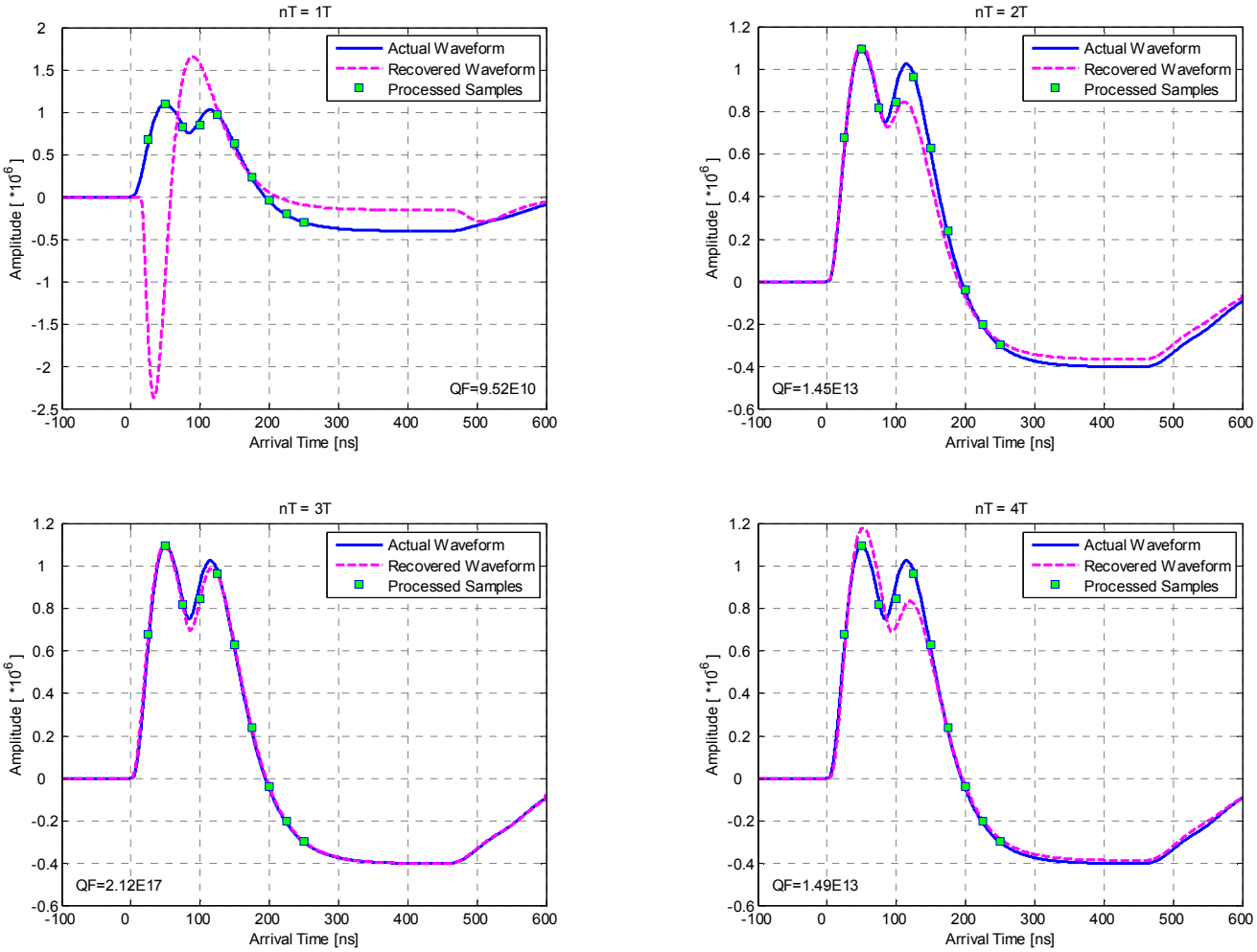


Figure 4.3. Evaluation of (4.8) for n = 1, 2, 3, 4 of the case illustrated in Figure 4.1 for τ_c = -1.276 ns and τ_p = 2.015 ns without electronic noise. The solid curves are the actual waveform of the shaper output, the dashed curves are the recovered waveforms. The processed input samples by the LOF are marked in squares.

configuration. An alternative approach is to serialize the algorithm with only one filter, i.e., through iteration. In our simulation, a two-step coarse-fine estimation process is devised, in which the arrival time of the pileup pulse is decomposed into two terms, n_0T and $(n\text{-}n_0)T + \tau_p$, and $n\text{-}n_0$ is estimated during the coarse step and τ_p is estimated during the fine step.

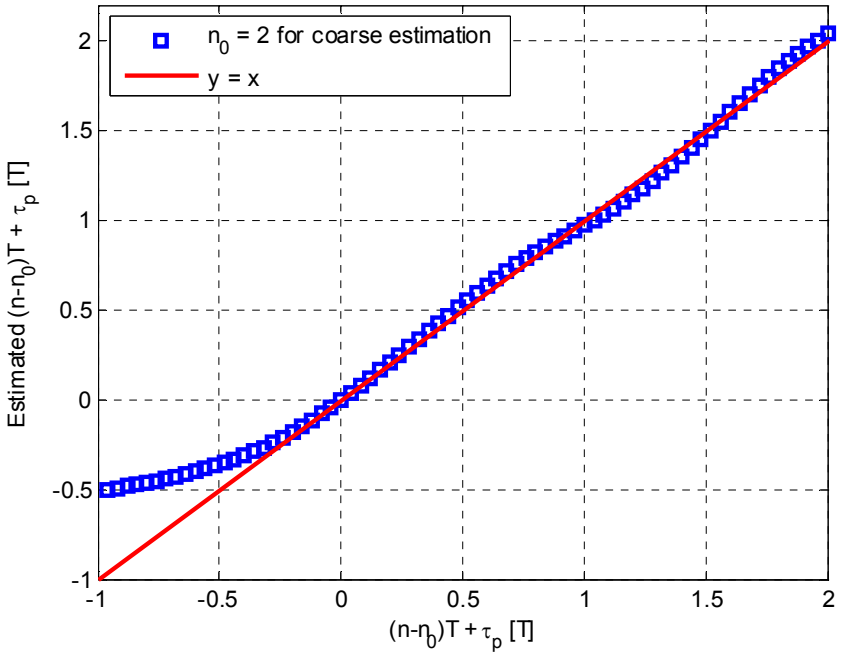


Figure 4.4. Feasibility evaluation of the coarse-fine estimation scheme. When n_0 is set to 2 in the coarse estimation, the absolute value of the estimation error of $(n\text{-}n_0)T + \tau_p$ is less than $0.5T$ when the arrival time of the pileup pulse traverses from $1T$ to $4T$.

Figure 4.4 depicts the coarse estimation outcome of $n\text{-}n_0$ of the pileup pulse when $\tau_c = 0$ and n_0 is set to 2. Even though estimation error occurs when $n\text{-}n_0 \neq 0$, the error is bounded and deterministic when n ranges from 1 to 4. Thus, a lookup table (LUT) can be constructed to accurately determine the value of $n\text{-}n_0$. When $\tau_c \neq 0$, some small deviation will arise, slightly degrading the precision of the arrival time estimation of the pileup pulse $(n\text{-}n_0)T + \tau_p$; however, the integer part $n\text{-}n_0$ is intact, and the exact value of n can be reliably determined accordingly. In

the fine step, with reloaded LOF coefficients (pre-calculated for the correct bunch crossing time nT), highly accurate results of A_c, τ_c, A_p and τ_p are produced. With this two-step iterative approach, 75% of the hardware is saved at the cost of a slightly more than doubled estimation time due to the iteration. The following section describes the results of Monte Carlo simulation conducted in this manner.

Monte Carlo Simulation

A 5000-run Monte Carlo simulation is performed using the two-step iterative estimation method. The amplitudes of the current and pileup pulses are uniformly distributed in the range of [0, 10×10^{-6}]. The fractional parts of the arrival times are uniformly distributed between -3ns and 3ns. The integer part of the arrival time of the pileup pulse n is a uniform discrete random variable taking on a value from {1, 2, 3, 4}. The standard deviation σ of the AWG noise is set to 5×10^{-7}.

Figure 4.5 graph the A_c, A_p estimation results, in which the x-axis is the actual input signal amplitude and the y-axis is the estimated amplitude. In both figures, the estimation points are closely and uniformly scattered around the line $y = x$, revealing an accurate and unbiased estimation of the LOF approach. No estimation outcome falls on either x-axis or y-axis in either plot, indicating that no false alarm or missing detection occurs in all 5000 runs of this Monte Carlo simulation.

Figure 4.6 graphs the correlation between the A_c, A_p estimation errors. A negative correlation is observed, which indicates that when the estimation of A_c experiences a positive error, say, due to noise, the estimation of A_p will likely experience a complementary negative error, and vice versa. This is not difficult to justify as the goal of the LOF is to minimize the overall value of the χ^2 function. In addition, it is also noticed that when ΔA_p decreases negatively

(ΔA_c increases positively), the correlation slightly deviates from the line $y = -x$, which probably stems from the truncation error of the first-order approximation of the LOF due to the asymmetry of the leading and trailing edges of $g(t)$.

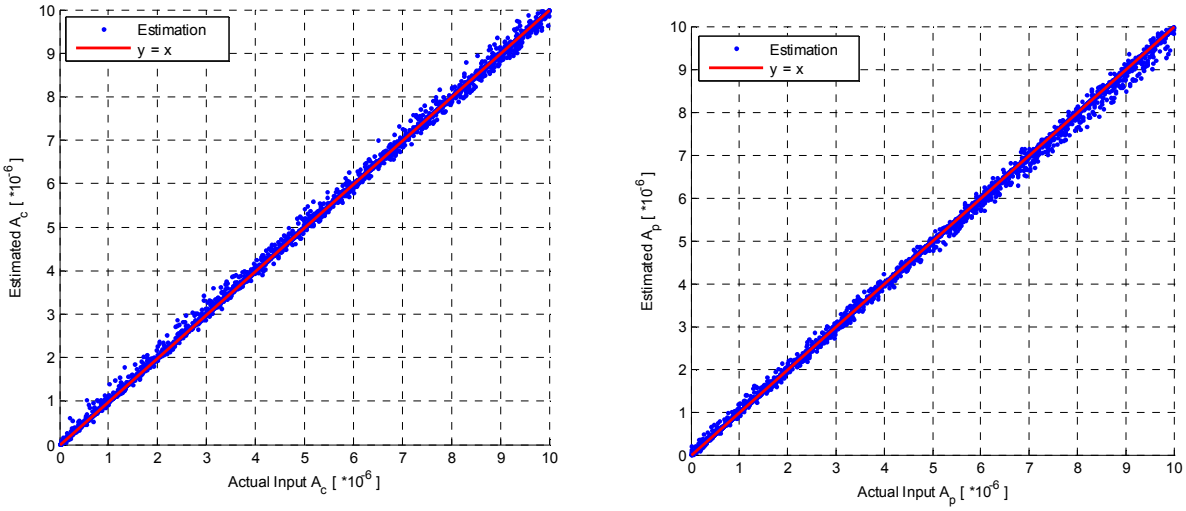


Figure 4.5. Estimated vs. actual input signal amplitudes for A_c (left) and A_p (right).

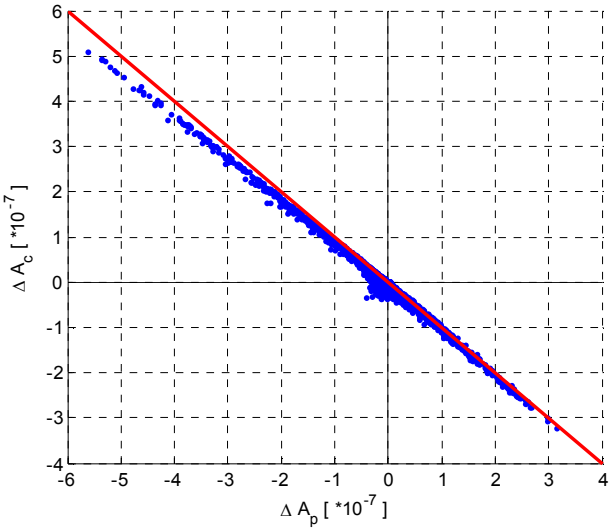


Figure 4.6. Correlation between ΔA_c and ΔA_p.

4.1.2 Further Analysis

Further analysis is conducted to examine the quality of the LOF estimation in this section.

Figure 4.7, Figure 4.8, and Figure 4.9 show the mean of the estimation errors for A_c, A_p, τ_c and τ_p, respectively, of 100 Monte Carlo runs, when τ_c and τ_p vary from -T/4 to T/4. The quadratic error profile reflects the fact that the truncation error of a first-order Taylor expansion is dominated by second-order terms. The asymmetry of the profile is due to the asymmetry of the $g(t)$ function, which exhibits a fast rising edge and a slow falling edge. With a small τ, the amplitude estimation errors of A_c and A_p are typically less than 0.5% in this simulation.

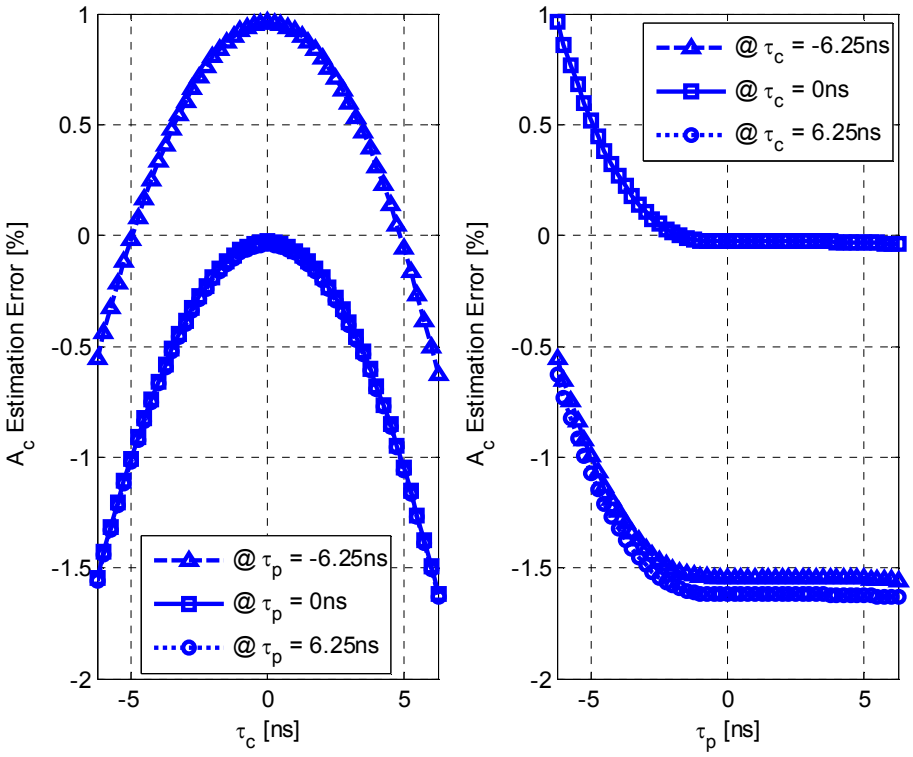


Figure 4.7. Estimation error of A_c vs. τ_c (left) and τ_p (right) from -T/4 to T/4. The σ of the Gaussian detector noise is set to 10% the peak value of the detector current pulse.

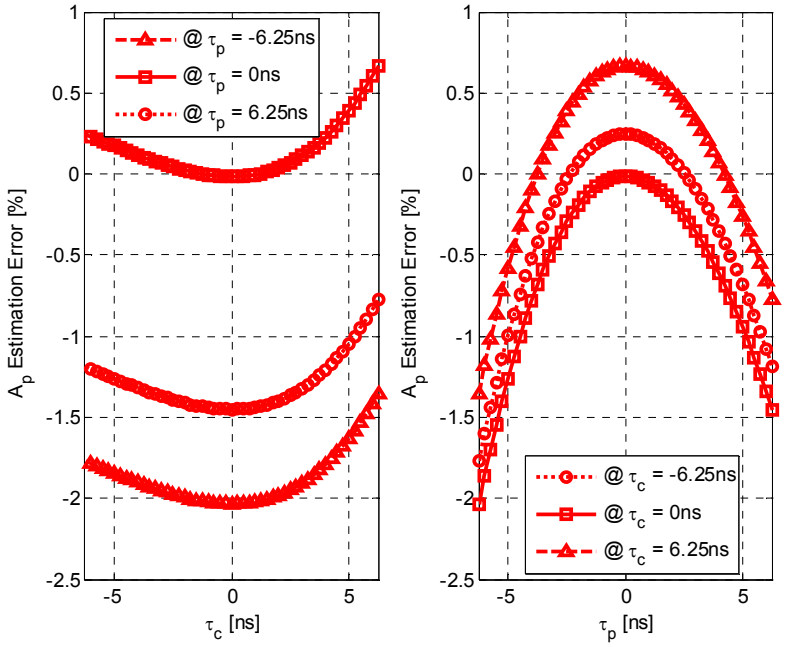


Figure 4.8. Estimation error of A_p vs. τ_c (left) and τ_p (right) from -T/4 to T/4 with the same detector noise assumed in Figure 4.7.

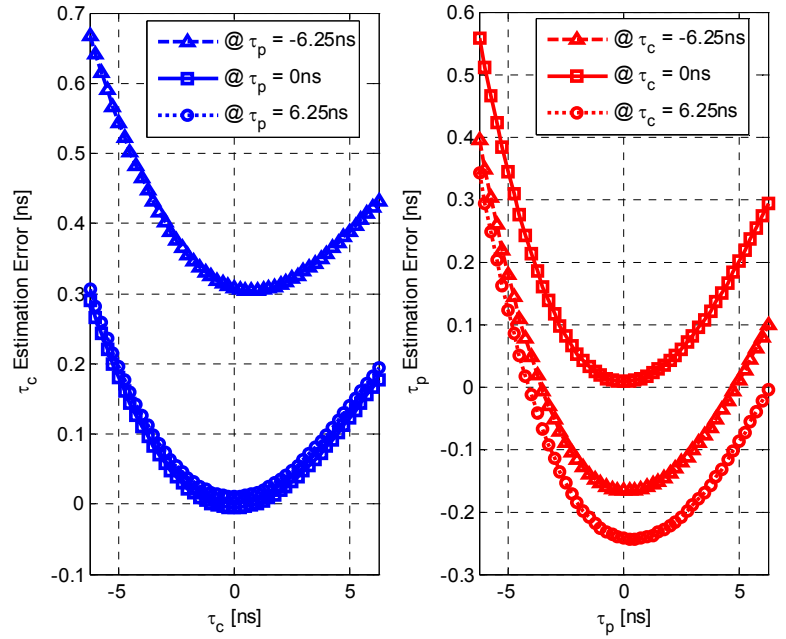


Figure 4.9. Estimation error of τ_c vs. τ_c from -T/4 to T/4 (left) and estimation error of τ_p vs. τ_p from -T/4 to T/4 (right). Simulation parameters are identical to those of Figure 4.7 and Figure 4.8.

Figure 4.10 illustrates the estimation errors of A_c, A_p, τ_c, and τ_p as a function of $nT + \tau_p$ with a coarse-fine iterative approach of the LOF ($n_0 = 3$ in this case). The periodic error pattern with exactly zero estimation error at integer multiples of T verifies the first-order approximation of the χ^2 function. A proximity effect of the error behavior is also observed in that the error ripple asymptotically dies out when the two pulses are further separated, i.e., as $nT \rightarrow \infty$. The amplitude and thus the energy resolution of the estimation will degrade when the two pulses are closely spaced, i.e., for $n < 2$ cases.

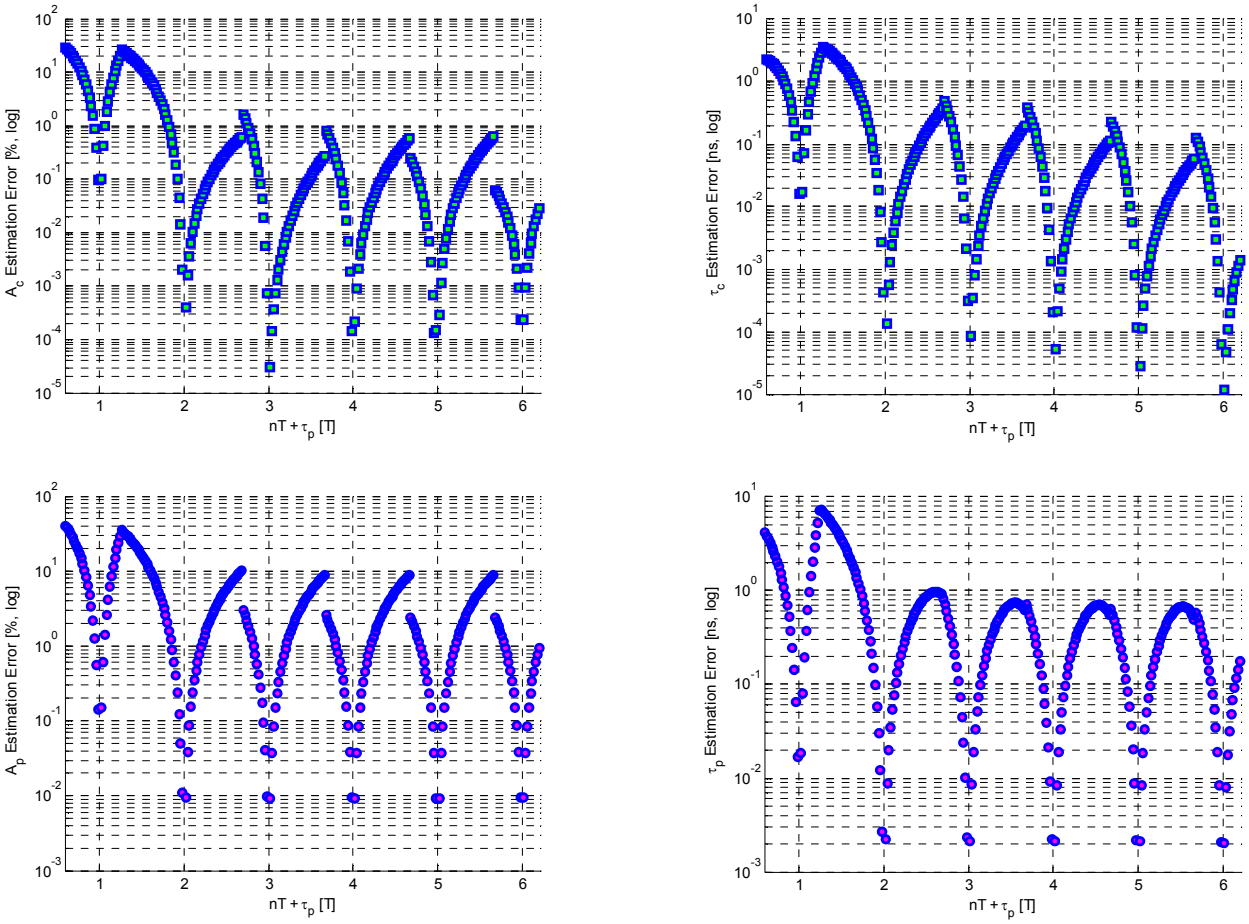


Figure 4.10. Coarse-fine iterative estimation results of A_c (top left), τ_c (top right), A_p (lower left), and τ_p (lower right) vs. $nT + \tau_p$ for $n_0 = 3$. The LOF yields accurate estimation results for nT.

4.2 Decision Feedback Equalization

After the pulse amplitude in the current BC is correctly estimated by the extended LOF, the algorithm will proceed to the next BC that has signal pulse existed. At this point, the previous amplitude estimate can be used to remove its pulse's impact on the current one under estimation as the normalized waveform is known. Thus, the decision feedback technique is carried out naturally.

Before the samples fed into the extended LOF, the signal residues from all the prior BCs will be subtracted from the current signal samples through the feedback path depicted in Figure 4.11. Therefore, all the history will be removed.

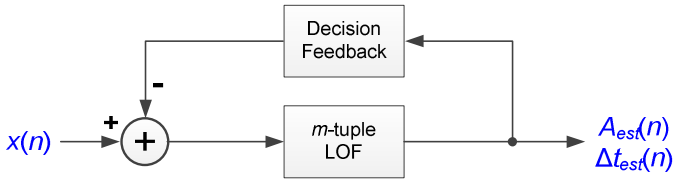


Figure 4.11. M-tuple LOF with decision feedback techniques.

There are two additional issues that need to be addressed. As mentioned before, each time after the joint estimation is performed, the algorithm will advance to the next BC that exist a signal pulse (physical event occurs). Therefore, it is necessary to identify the BC with signal pulse first. There are different ways to complete this task [16]. In this research, a 2-tap LOF is employed to provide a coarse estimation for each BC to determine the existence of the signal pulse. This coarse estimation also aided with the decision feedback scheme to avoid the pileup effect from the previous BCs.

Due to the linearization of the signal model, the estimation results also suffer a systematic error and become biased. This bias is strongly depend on the arrival time delay Δt [17] and will

become larger as the distribution of Δt spreads out. In order to mitigate this problem, an iterative estimation procedure [11], [16] is performed as illustrated in Figure 4.12. After extended LOF gives the amplitude and timing estimation, the signal model will be linearized at this estimated pulse arrival time instant and the coefficients of the iterative LOF will re-calculated with this updated signal model. Thus, the approximation error will be greatly reduced.

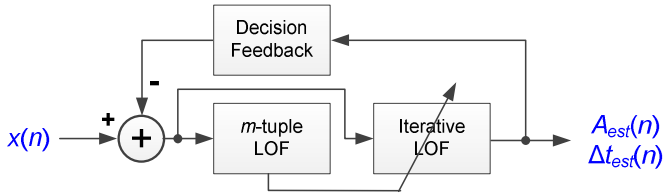


Figure 4.12. Diagram of iterative LOF.

4.3 Sequence Detection Algorithm

As the digitization module samples the post-shaping signal continuously in the future LAr calorimeter upgrade, the availability of sequence detection opens up for high precision amplitude estimation.

A typical waveform of the pulse train produced at the output of the shaper is depicted in Figure 4.13. This waveform is generated according to the occurrence of physical event at each BC from the simulation results of AREUS, an ATLAS LAr calorimeter simulation platform. The effect of arrival time delay Δt that regulates the exact peaking time of each pulse is also included with a presumption of Gaussian distribution for Δt with mean μ = 0 ns and standard deviation σ = 0.6 ns. In addition, a shaped noise of SNR = 74 dB is superposed on the waveform.

As stated before, the normalized individual pulse shape $g(t)$ is known. The unknown parameters to be determined are the amplitude A and arrival time delay Δt for each pulse corrupted by the frontend electronic noise.

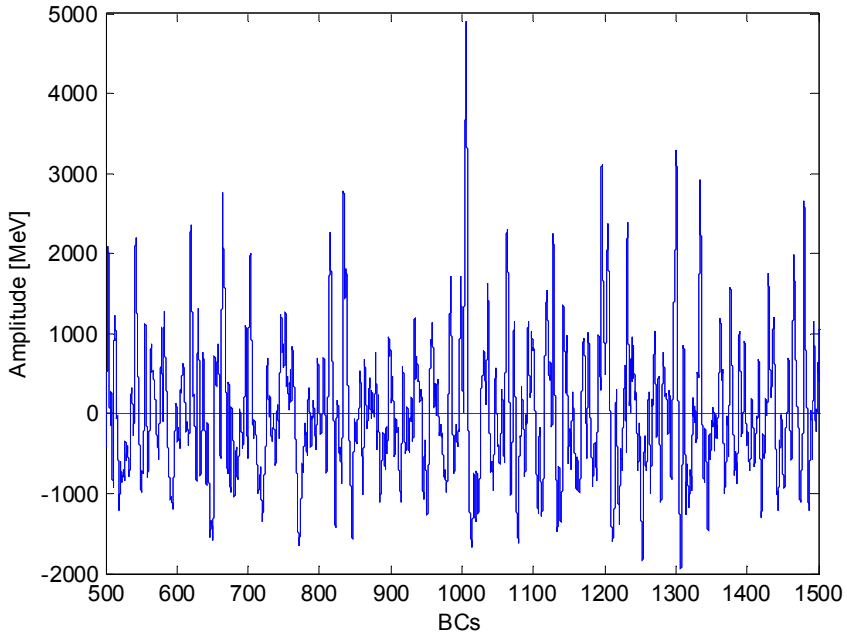


Figure 4.13. The time domain waveform of a segment of pulse sequence.

Several algorithms can be implemented to treat IEI problems in a noisy sequence, such as equalizations and maximum likelihood detection. In this research, the extended LOF with decision feedback equalization (DFE) is applied for amplitude estimation in the sequence. Although the DFE technique suffers from the error propagation effect, theoretically, it can completely remove the interference of the current event to the future one without much noise enhancement as the zero-forcing equalizer does.

4.3.1 Basic Setups

The LHC is running at a speed of 40 MHz [1] and at each BC spacing 25 ns to each other, the detector will potentially capture a physical event and produce a current pulse. For each pulse, there are two parameters, A and Δt, to be estimated. Therefore, every 25 ns, at least two samples are required for the linear system to deliver valid estimates as shown in Figure 4.14. Otherwise,

it will become an underdetermined system that gives arbitrary solutions. This fundamental rule of the linear system set a lower limit for the sampling rate of the digitization modules to be at least 80 MS/s. On the other hand, to ensure uniform sampling during each BC, the sampling rate is required to be $40 \cdot x$ MS/s ($x \geq 2$). Constrained by the realization complexity of the ADCs to multiple specifications, such as resolution and power consumption, the sampling rate cannot be too fast. Therefore, a sampling rate of 80 MS/s is adopted throughout the analysis below, i.e. at each BC, two samples are taken for processing.

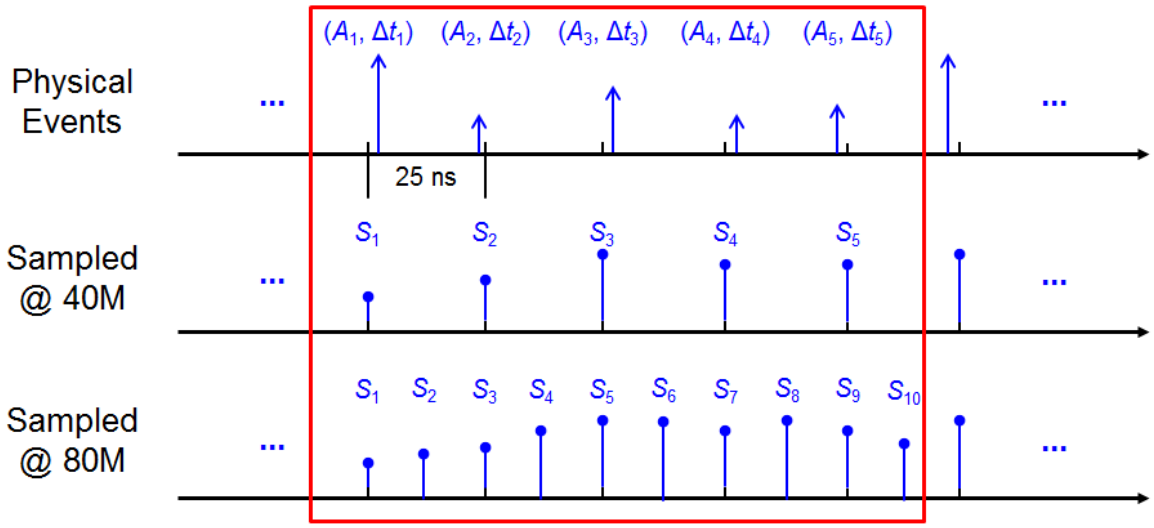


Figure 4.14. Illustration for sample rate discussion.

Another important setup is the selection of the total number of samples for the joint estimation by the LOF. Fewer samples obviously will result in deficient estimation precision, while too many samples, on the contrary, will introduce large estimation latency, which is also an undesired effect. Usually, 5 samples are chosen ([7], [11], and [14]) in a 40-MS/s sampling rate, corresponding to a 5 BCs latency. Thus, 10 samples are used in this analysis under the 80-MS/s sampling rate assumption, which has the equivalent latency to the previous work.

4.3.2 The Algorithm

To ensure valid estimates given by the extended LOF applied in the pulse sequence, several aspects should be considered in advance. First of all, LOF demands the pulse position information of an incoming pulse train, i.e. the presence of pulse in each BC; therefore, a trigger needs to be devised to fulfill this task. Secondly, the LOF does not remove any effect or impact of the previous pulse to the current one automatically, thus, the history of the pulse sequence should be subtracted based on the previous estimates. Thirdly, the estimation errors will drop off when more data samples are involved in the estimation process. Then, the estimation accuracy of the first pulse is always higher than that of the following pulse when the joint estimation is performed in a pileup event, for the first pulse includes more effective samples.

According to the above discussion, three main procedures of the proposed algorithm are carried out naturally.

The first step is to examine the presence of pulse in each BC with a simple trigger and this process need to iterate $n = 5$ times (i.e. 5 BCs) to determine the pulse pattern corresponding to the $m = 10$ samples that will be further processed by the extended LOF later.

The trigger is constructed by a 2-tap LOF processing 2 samples each time for A and Δt estimations of a single pulse in each BC. A decision feedback will also be applied to subtract the impact of the previous pulse to the current one. Due to the equality between the number of unknown parameters and the number of constrains (the samples), no more freedom exists to suppress noise. Therefore, the filtered results by the trigger would have the same SNR as the processed samples. Noise and interference superposed on the samples are considered the same way as the signal by the trigger and completely propagate to the estimated amplitude. The

estimation precision is insufficient. However, the purpose of the trigger employed at this step is only to detect the presence of the pulses and only 1-bit true-or-false information is demanded; thus, large errors can be tolerant by setting a proper threshold according to the noise level.

In the second step, a specific LOF will be selected first based on the pulse pattern provided by the trigger to estimate the amplitudes of the k ($k \leq n$) pulses precisely in n BC periods with m samples. Four possible cases encountered in a pulse sequence are illustrated in Figure 4.15 conceptually. Each stick represents a physical event happened in that BC with its height revealing the ideal amplitude that should be recovered.

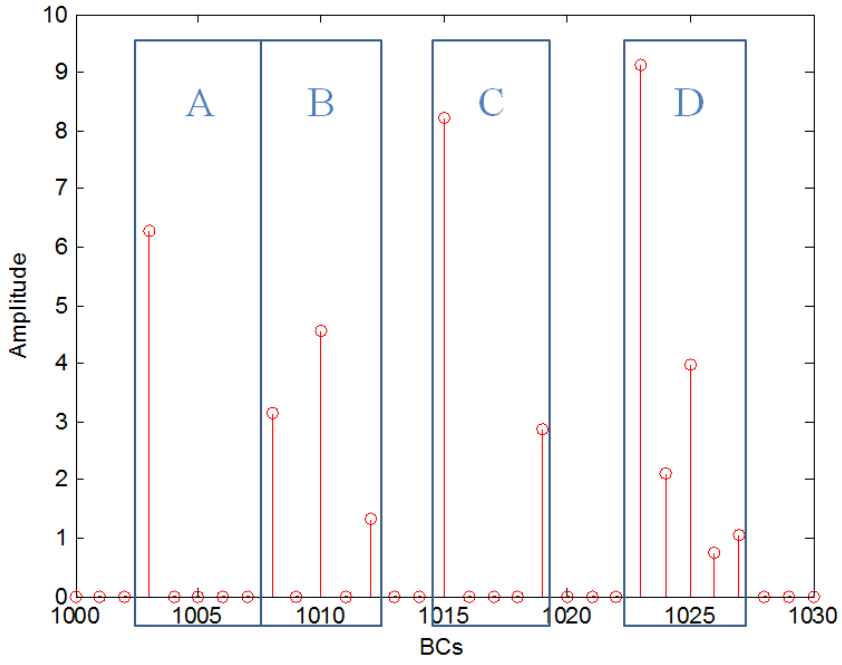


Figure 4.15. Pulse patterns

For instance, when the trigger detect a pulse pattern of [1 0 0 0 1] for 5 consecutive BC periods (*Case C*. 1 refers the presence of pulse in current BC and $A \neq 0$; 0 refers to no pulse in current BC and $A = 0$), LOF_{10001} will be picked up for amplitude estimation, whose filter taps can be calculated by (4.9).

$$\mathbf{C}_{10001} = \left(\mathbf{G}_{10001}^{T}\mathbf{V}\mathbf{G}_{10001}\right)^{-1}\mathbf{G}_{10001}^{T}\mathbf{V}, \tag{4.9}$$

where, $\mathbf{G_{10001}}$ is a four-column matrix. The first two columns are $g(n)$ and $g'(n)$ for the first pulse, and the last two columns are $g(n+4T)$ and $g'(n+4T)$ for the fifth pulse. T is the bunch crossing time.

If the trigger gives a pattern of [1 0 1 0 1] (*Case B*), then the coefficients of LOF_{10101} are given by (4.10).

$$\mathbf{C}_{10101} = \left(\mathbf{G}_{10101}^{T}\mathbf{V}\mathbf{G}_{10101}\right)^{-1}\mathbf{G}_{10101}^{T}\mathbf{V}, \tag{4.10}$$

where, $\mathbf{G_{10101}}$ is a six-column matrix with each two columns being $g(n)$ and $g'(n)$ delayed $0T$, $2T$ and $4T$ respectively for the first, third and fifth pulses.

If each of the five BCs has incoming pulse (*Case D*), then $\mathbf{G_{11111}}$ is a ten-column matrix and $\mathbf{C_{11111}}$ is a corresponding ten-row matrix with each of the two rows being the filter taps for A and Δt estimation for one pulse. This extreme represents the worst case that would potentially occur in the pulse sequence, which, the extended LOF will not gain any performance improvement for amplitude estimation compared to the 2-tap LOF used in the trigger. However, luminosity of the calorimeter in the future upgrade dictates that this extreme case happens in a rare possibility.

In the third step, the influence from the previous pulse will be diminished by subtracting the previous pulse sample values from the current samples. Then the extended LOF will conduct the estimations on the amplitudes and timings of these triggered pulses with the pre-processed samples.

It is worth to mention that for n BCs joint estimation, there are altogether $(2^n\text{-}1)$ extended

LOFs corresponding to (2^n-1) pulse patterns. When $n = 5$, then, there are 31 LOFs. However, as stated previously, more effective samples involved will boost the estimation accuracy.

In this paper, each time, trigger will pass five BCs events and the joint estimation by the LOF will only determine the first pulse's amplitude, by which, the maximum number of samples are involved for estimation, attenuating the noise power by this maximum number of samples. And always keep the current pulse for estimation in the first place, then for five BCs, there are $2^5/2-1 = 15$ patterns in total.

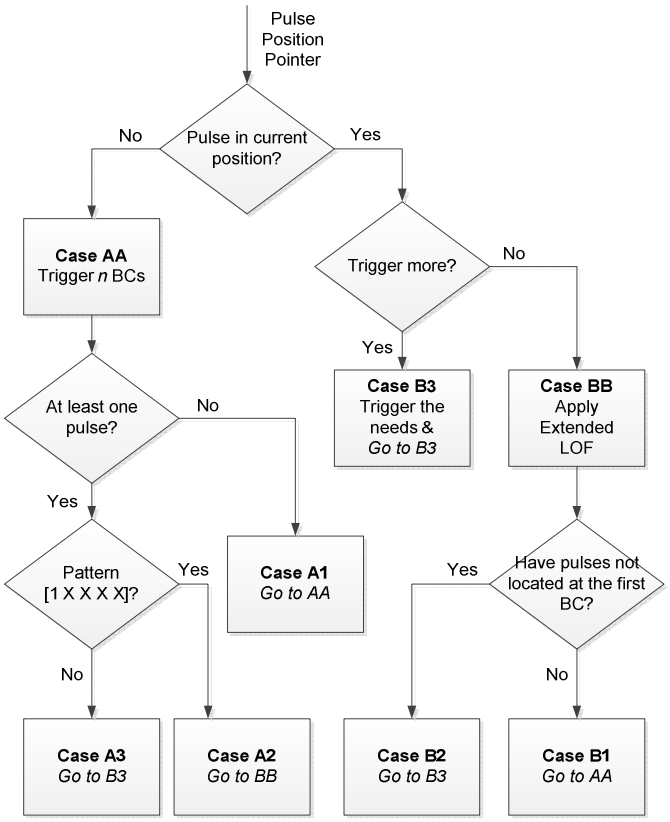


Figure 4.16. Diagram of the FSM

These estimation procedures can be easily programmed with a finite state machine (FSM) and assisted with a pointer pointing to the position of the current pulse. The states transfer diagram is shown in Figure 4.16.

4.3.3 Error accumulation and the solution

At this point, the DFE sequence detection algorithm is ready for use. But, during the simulation, it is found that the mean of the estimation errors gradually increase, leading to a non-zero mean estimation as depicted in Figure 4.17. This will make the algorithm not practical for use.

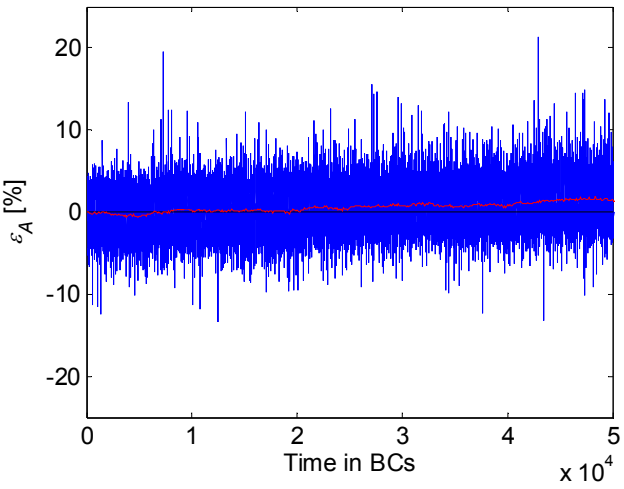


Figure 4.17. Error accumulation

Review the filter in s-domain or z-domain, the reason is revealed. It is caused by the shaper. The shaper has a CR-RC^2 form, where there is a zero at DC in the expression. All the algorithm do, is inverse the system including the shaper. Thus, to complete this task, the algorithm has to have a pole at DC to cancel the effect of zero in the shaper. Therefore, the decision feedback process in fact keeps integrating the noise and estimation errors from the previous iteration. A conceptual diagram in Figure 4.18 illustrates this noise accumulation process.

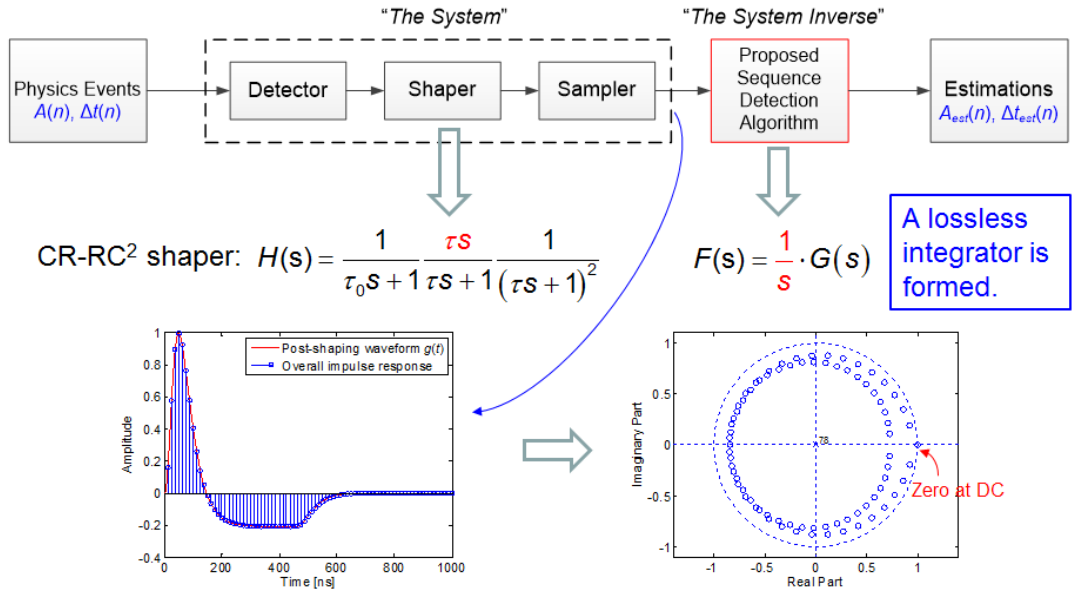


Figure 4.18. A conceptual diagram illustrating the reason of noise accumulation

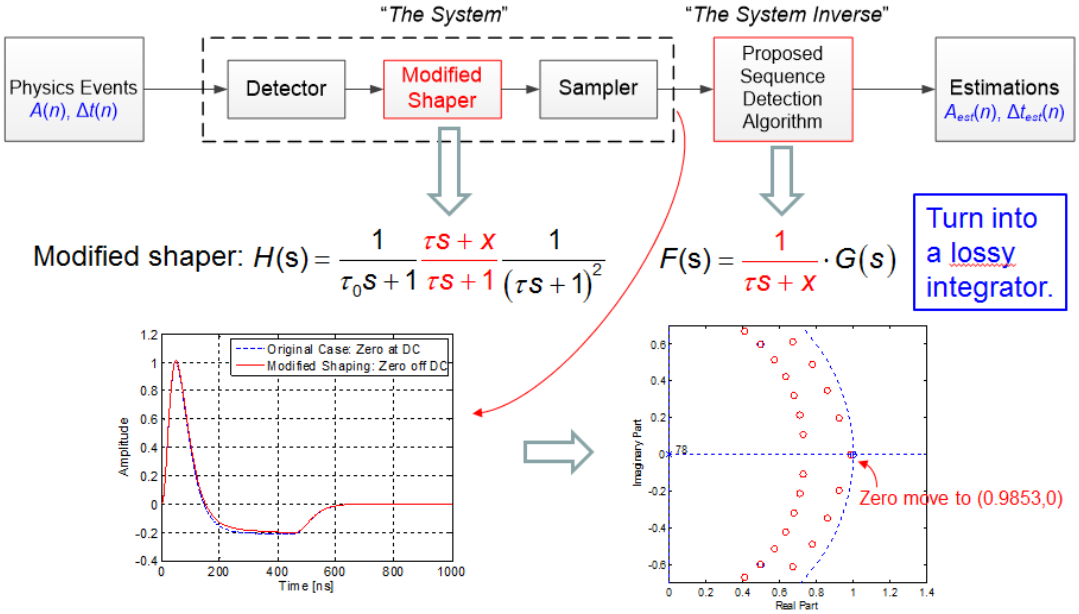


Figure 4.19. Shaper modification for the removal of noise accumulation

A simple and effective way to eliminate the problem is to modify the shaper. As long as the zero is moved off DC in the shaper, then the system inverse will no longer be an integrator. The error

accumulation effect will be removed as shown in Figure 4.19, which is verified by the simulations shown in Figure 4.20.

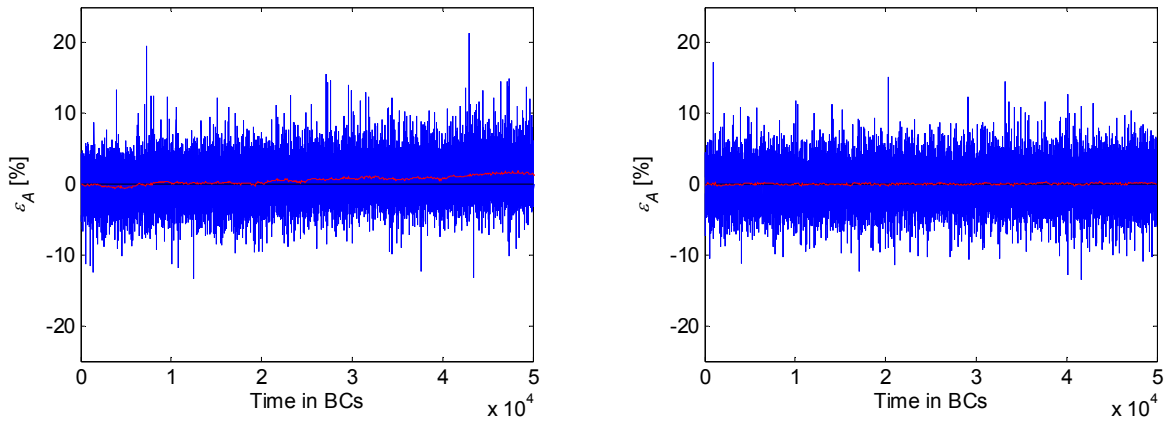


Figure 4.20. Removal of the noise accumulation with modified shaper

This modification on shaper is also easy for circuit implementation. We can add only one resistor to the current active RC shaper to get a lossy differentiator. And the resistor value is within hundred kilo-ohm range for a reasonable low frequency zero.

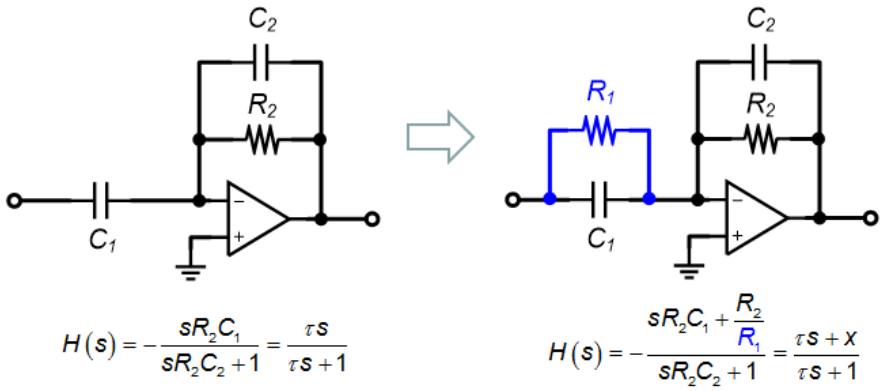


Figure 4.21. One possible circuit implementation for the shaper modification

4.3.4 Simulation Results

A set of Monte Carlo (MC) Simulations are performed to verify the algorithm proposed in the previous section.

The waveform of the input pulse sequence is depicted in Figure 4.13 and the amplitudes and noise settings are the same as them in Figure 4.13, except the arrival time delay is set to 0. The MC data length is 10^4 and μ = 200 MeV, which indicates a high luminosity of the calorimeter.

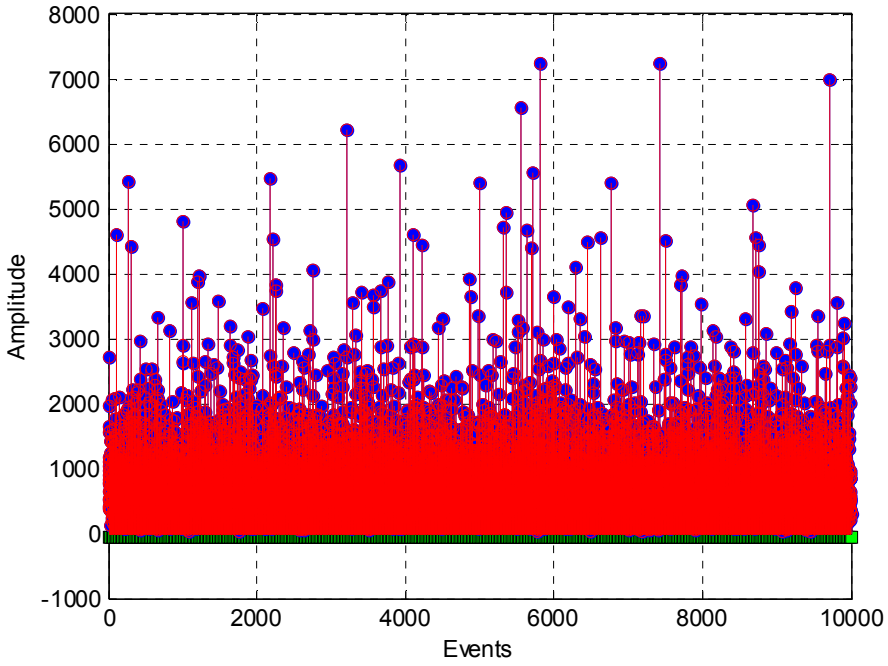


Figure 4.22. Pulse train

The amplitude estimation results (blue) overlapping on the ideal amplitudes (red) plot in the time domain is displayed in Figure 4.22. It can be observed that these condensed two color sticks well match each other, demonstrating the functionality of the proposed algorithm.

A correlation plot between ideal and estimated amplitudes is showcased in Figure 4.23, where all the dots represent the estimates. They sit closely on the $x = y$ line, revealing the high precision of the estimation qualitatively and intuitively. Missing detection and false alarming only happen at very small amplitude case; as E > 30 MeV, there is no missing detection or false alarming.

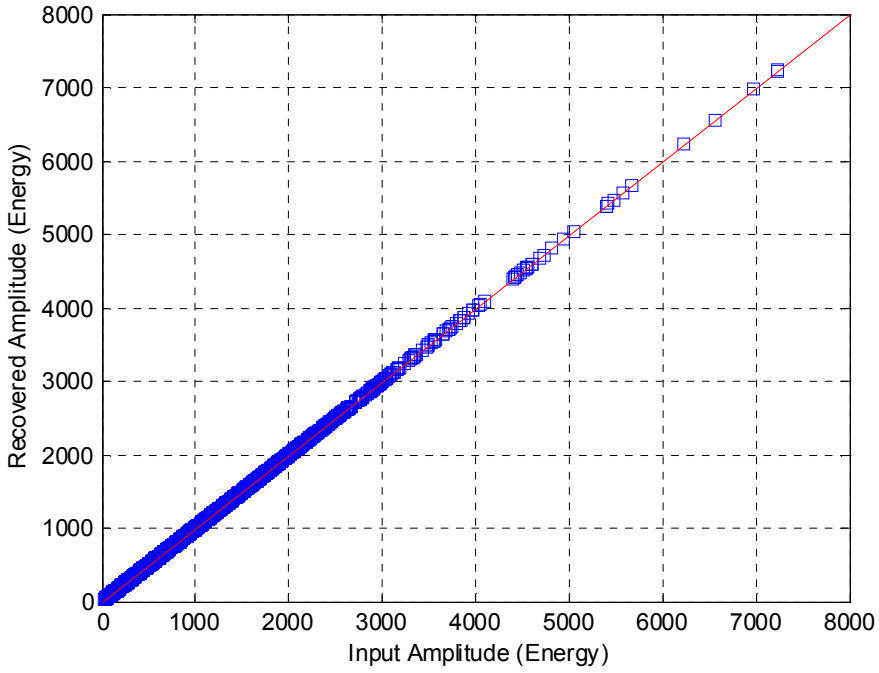


Figure 4.23. Energy Correlation

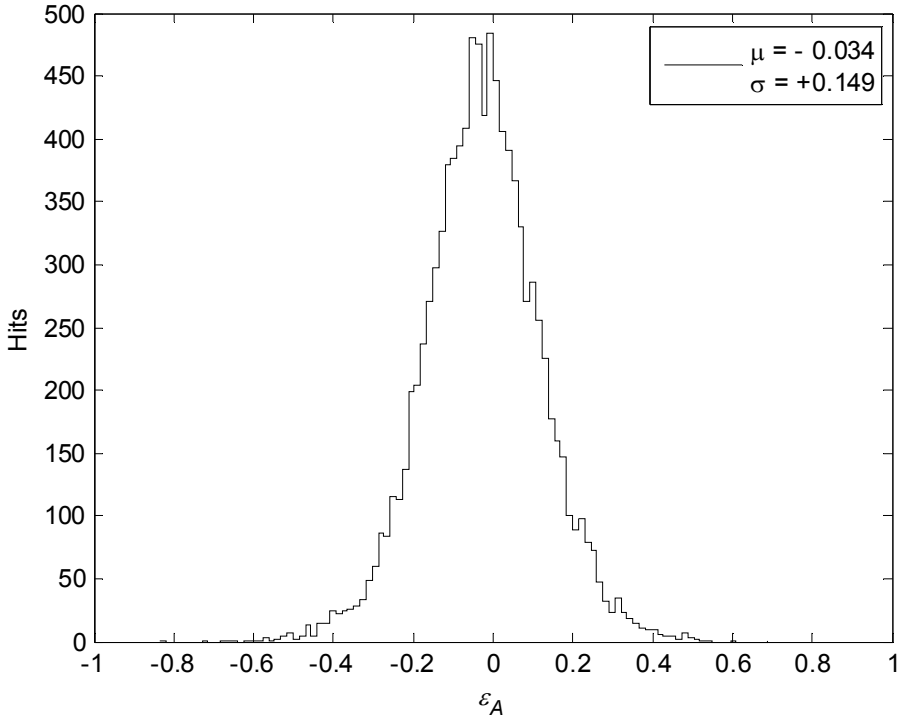


Figure 4.24. Estimation Error Distribution

A histogram displayed in Figure 4.24 measures the amplitude estimates quantitatively. The x-axis is the absolute differences between the estimates and ideal values and y-axis is the statistics over each bin. The profile of the curve has a Gaussian shape with the mean μ = -0.034 and standard deviation σ = 0.149. Thus, it is an unbiased estimation and it can be concluded that 99.7% amplitude estimation errors will fall into the segment within ±0.45, results in a maximum SNR of 84 dB and also a large dynamic range (DR).

4.3.5 Comparison to LOF and Wiener filter

In [11], pileup effect is treated as noise and it is in necessity in low luminosity. As the pileup happens more frequently, it is no longer suitable to treating pileup as noise. Left figure in Figure 4.25 plots the results obtained only by applying LOF [11] to the input sequence with 780 MeV to 18.5 GeV energy from the EM middle layer of the calorimeter in Phase-II luminosity and 150 MeV RMS white noise. Ideal trigger is assumed. It can be seen that under high-rate pileup condition, LOF generally fails to provide reliable amplitude estimates. A bias is observed. The rate of false alarms and missing detections is much higher than that of the proposed detection scheme (results are plotted in the right-hand-side figure). The deteriorate performance of the LOF encounters problem in this situation to provide high-precision estimations.

A comparison with Wiener filter [14] is also conducted. Same signal and noise conditions are applied in the simulation: 0 – 80 GeV flat energy spectrum and 200 MeV RMS white noise. From the two figures in Figure 4.26, we can see that the propose sequence detection algorithm gives more accurate estimation results with smaller deviation and no false alarm nor missing detections under the same simulation conditions.

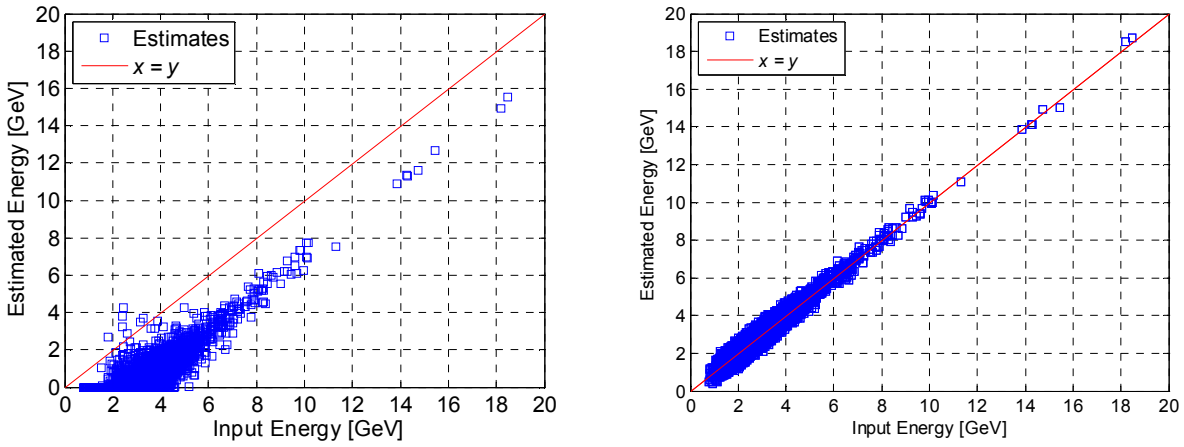


Figure 4.25. A Comparison to LOF results

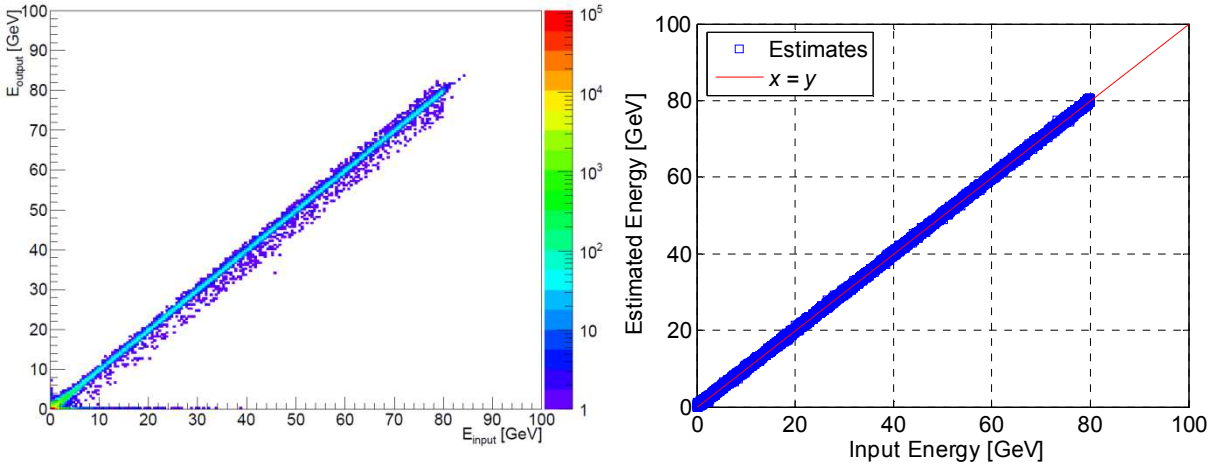


Figure 4.26. A comparison to Wiener filter results

In a summary, the proposed algorithm demonstrates good performance for high-precision energy estimation, especially under high-luminosity environments compared to the current methods. It is a potential candidate for the future readout upgrades of LHC and other similar applications in particle physics experiments.

CHAPTER 5

ERROR TOLERANT TECHNIQUES IN ADC DESIGN

5.1 Introduction

For this analog-to-digital converter (ADC) prototype design, beside the nominal specs, radiation tolerance introduced another layer of complexity. To effectively and successfully deal with this task, a basic understanding toward the error mechanism due to radiations should be first established. In this section, two categories of the radiation effects will be first briefed, followed by the ADC architecture comparisons.

5.1.1 Requirements on Radiation-Tolerant Electronics

Radiation effects categorized as single event effect (SEE) and total ionizing dose (TID) challenge the prototype design.

SEE is caused by a single, energetic particle, and can take on different forms. As stated in [18], [19], when particle traversing a silicon device, ionizing current will be induced and flow between the active region and substrate, an event such as a register bit flip or transient may occur. This will cause the malfunction of a circuit block or logic fails.

Meanwhile, in the oxide gate, electron-hole pairs keep creating over time as the radiation lasts. Electrons with higher mobility leave the oxide, while holes with lower mobility are mostly trapped in the oxide, leading to net positive charges trapped in the oxide. This cumulative ionizing, also known as TID, the total ionizing dose, will create permanent damage to the device, such as the shift of threshold voltage and gate leakage [19].

However, as the technology keeps scaling down, the thickness of the oxide is shrinking. This helps to ease the TID effect [20], [21] and the later on measurement results proved that. In this design, we are mainly focus on dealing with SEEs.

5.1.2 SAR vs. Pipelined ADC [22]

Some efforts were invested in the development of dedicated ADC for the high-energy physics (HEP) experiments ([23] – [27]). In this research, there are two principal ADC architecture choices for HEP applications. One is the SAR ADC and the other is the pipelined ADC. Both can operate at medium-to-high resolutions, while the pipeline usually displays a higher throughput than the SAR.

One challenge of implementing a pipelined ADC in scaled CMOS is that the low supply voltage in these processes makes the design of the high-gain, high-speed residue amplifier (RA) – necessary for inter-stage residue voltage transfer – difficult, thus degrading the linearity and noise performance of the ADC, which usually translate into high power consumption, large die size, and high cost ([28] – [32]).

In contrast, due to the series conversion process, a SAR ADC ([33] – [37]) is much more power and area efficient – it only contains three main components, a switched-capacitor (SC) digital-to-analog converter (DAC), a zero-crossing comparator, and some SAR logic and registers, leaving ample room for redundancy circuits to be implemented for radiation tolerance. We will show in Section II that with technology advancement, CMOS SAR ADCs now meet the conversion speed requirement for ATLAS LAr application. The characteristics of advanced CMOS technologies (e.g., a 40-nm or 65-nm process) under irradiation, showing significant decrease of the radiation-induced charge trapped in the oxide and interface states [38], also

greatly benefit the TID tolerance of the circuits. The improved conversion speed, combined with the prominent advantage in power and area consumptions, makes the CMOS SAR a suitable and perhaps preferred candidate for future HEP applications.

5.1.3 Design Challenges

The radiation operation condition coupled with the large dynamic range (>12b ENOB), 40-80MS/s sample rate and low power (for cooling system requirement) specs [39] make the design of such ADCs a very challenging task.

From the speed aspect, to realize a >50MSPS operation with 12-14 bits resolution is quite demanding (pushing the limit) for a straight SAR architecture in 65nm process. On the other hand, low power requirement rules out the multi-stage power-consuming pipelined structure. Therefore, a hybrid two-step SAR was proposed to balance the above design trade-offs. Besides, radiation tolerance spec demands additional techniques to be applied for protection.

5.2 Split Architecture and Redundancies[1]

To tolerate errors, no matter caused by radiations or metastabilities, we always incorporate some kind of redundancies to assist. TMR, triple modular redundancy is a widely used technique for the digital circuit protection. Three identical digital blocks process the same logic input and produce a final digital bit by majority voting as depicted in Figure 5.1.

Similarly, we can also apply this TMR technique in the system level [40]. Three identical sub-ADCs sample and quantize a same analog input and produce the final digital code by a

[1] © 2017 IEEE. Portions adapted in section 5.2, 5.3 and chapter 6 and 7, with permission. See reference [41].

voter. The error probability of this voted output will largely drop compared to that of the output generated by a single ADC. However, there are area and power penalties. We have to triple the number of all devices, which in turn, lower the input bandwidth. Although we have method to address these issues, which we will discuss in the later, matching between the three ADCs as well as the time skew in clock distribution are much tougher tasks to deal with.

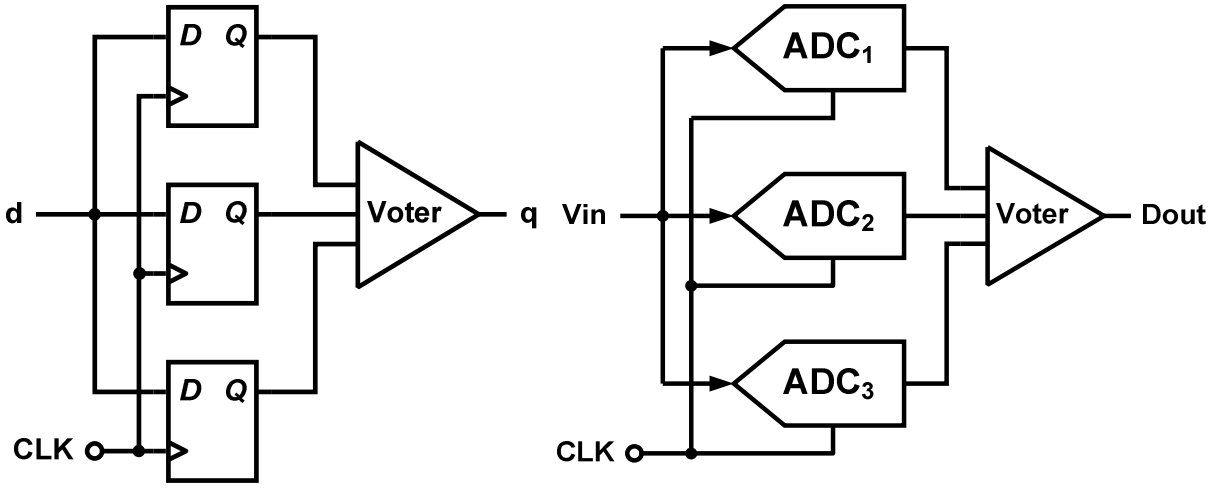


Figure 5.1. TMR in digital design (left) and in system-level design (right).

To retain the redundancies, but get rid of the short comes of the TMR in system level; the double modular redundancy (DMR) is applied in the system level design. Therefore, split ADC is proposed naturally [41], [42]. The two identical conversion paths work independently on the same input. Each sub-ADC can be the backup of the other one. If both ADCs are correct, their outputs will be averaged and taken as the final output. Figure 5.2 displays the system diagram of the proposed split SAR ADC architecture.

On the other hand, a bunch of detection circuits is invented and designed to monitor the internal nodes of each sub-ADC to identify the erroneous sub-ADC and control the 'select' signal of the MUX to output the correct one or the averaged one. To determine whether there is a

sub-ADC encountered problem, we simply subtract one ADC's outputs from the other one and monitor this difference delta Do. If both ADCs are working fine, this delta Do should be close to zero. Otherwise, the digital logics will be activated to do the selection according to those detection bits.

Besides, with the injection of the pseudo-random binary sequence (PRBS), the two transfer curves of the sub-ADCs will be slightly differed to each other, then we can take advantage of this split structure to enable the digital bit-weight calibration.

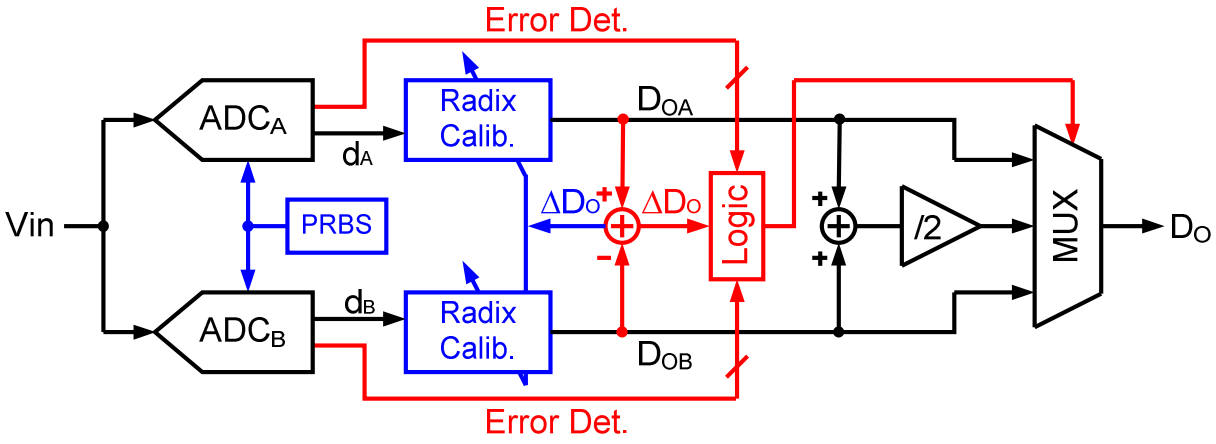


Figure 5.2. Radiation-tolerant split SAR ADC architecture.

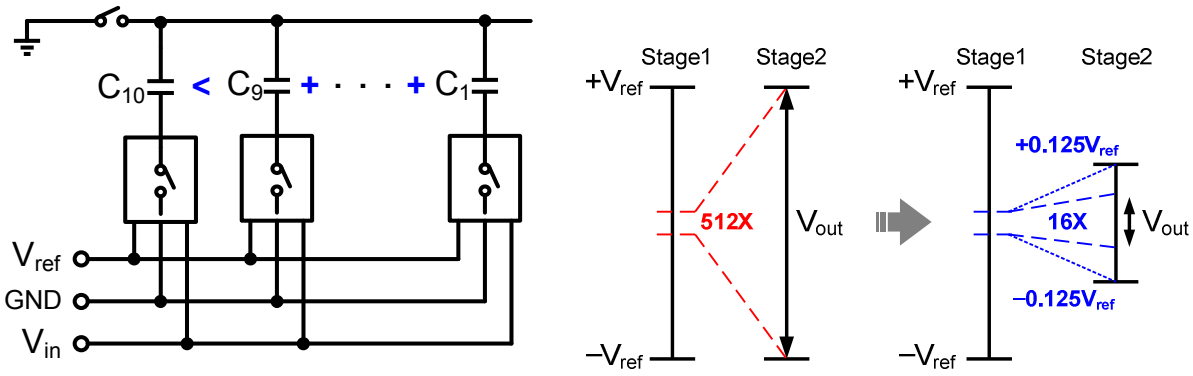


Figure 5.3. Intra- (left) and Inter-stage (right) redundancies.

Beside the architectural redundancy, there are extensive redundancies allocated in each stage and between stages. Figure 5.3 shows the intra- and inter-stage redundancies for dynamic error tolerance.

Within each stage, sub-binary DAC is used to cover wrong bit decisions caused by incomplete DAC settling or reference voltage bouncing. On the other hand, by scaling the reference voltage, gain of the residue amplifier is relaxed and inter-state redundancy is created.

5.3 Error Detection Circuits

To effectively identify the errors induced by the incident particles, the critical internal nodes of each sub-ADC are monitored by a bunch of dedicated detection circuits.

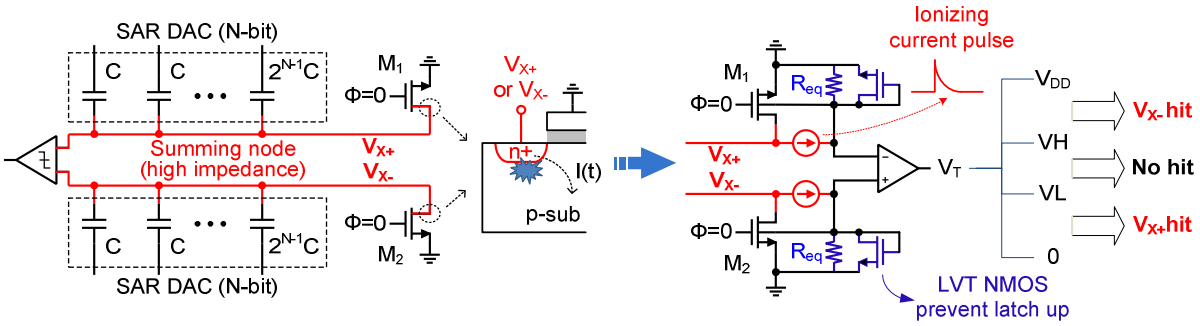


Figure 5.4. Summing node charge corruption caused by SET current and the detection circuits

5.3.1 Substrate Current Detection

Summing node is one of the most critical nodes in SAR ADC. During bit cycling, if the drain of an off summing-node switch is hit by an ionizing particle, the SET current shown in Figure 5.4 flows from the drain to the substrate. This current will irreversibly alter the total charge stored on the capacitors that represents the original input sample to be converted, resulting in a large conversion error. For a total deposited charge of 100 fC and total DAC

capacitance of 2 pF, the error voltage can be as large as 50 mV, or equivalently 340 LSB at 14-bit level.

To detect the summing nodes SEE error, the circuits shown in Figure 5.4 (right) is proposed. Two resistors are added to the substrate paths of the two summing node switches (M1 and M2), respectively. If the drain of M1 or M2 is hit, the SET current will flow through one of the two resistors, creating a temporary voltage difference between the two resistors. An amplifier then brings this voltage up to a resolvable logic level. A high threshold (VH) and a low threshold (VL) can be set to detect the amplifier output voltage—the comparison outcome thus reveals whether there is a hit. The comparison is performed by two inverters with their trip points skewed in two opposite directions by sizing as the exact value of VH and VL are not critical. To prevent latch up, a diode connected low threshold voltage (LVT) NMOS is connected in parallel with the resistor to clamp the substrate voltage to the threshold level.

5.3.2 Sampling Clock Protection

Sampling clock is also monitored to prevent potential timing errors. Two D-flip-flops (DFFs) are serial connected with their clock from the sampling clock. Within one sample period, if the sampling clock accidentally toggles twice, a triggering signal from the backend DFF will be produced to indicate the incorrect sampling operation.

5.3.3 Over- and Under-flow Detection

In the over or underflow detection, no additional circuits are designed or added. Any out-of-range errors can be identified by observing the output digital codes of the 2^{nd} stage. If all "1", we

know there is an overflow and if all "0" we know there is an underflow. Then the erroneous sub-ADC is pinpointed. An illustrative diagram is shown in Figure 5.5.

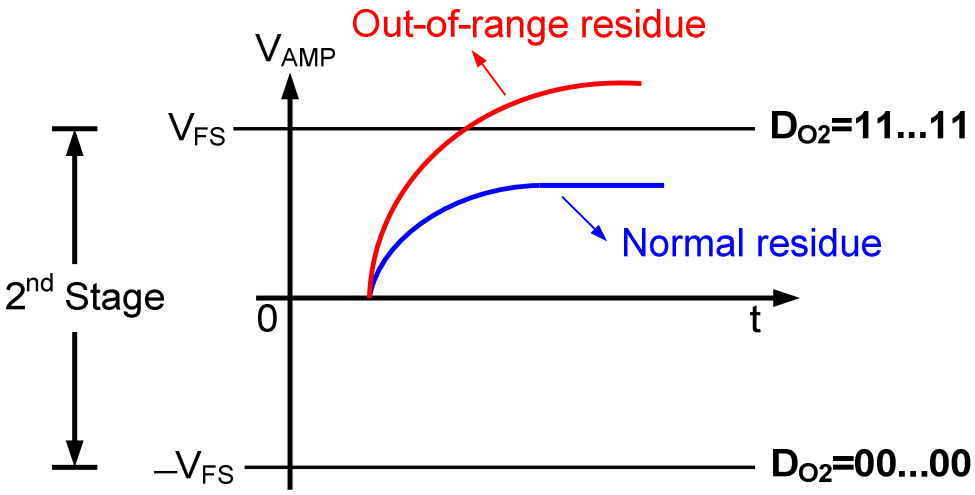


Figure 5.5. Residual curve when the bit error made by the 1st stage comparator/logics is within (blue) or out of the redundancy (red).

5.3.4 Extra Bit Cycle Detection

The second technique, also as one of the key technique we incorporated in this prototype, is the extra bit cycle for the 2nd-stage residue detection. Figure 5.6 sketches the second stage DAC. Towards the end, an extra DAC capacitor is attached to the 2nd stage summing node for an extra bit cycle [43]. Its value is set as 6 times the value of the LSB capacitor according to the statistics of ΔD_O in simulations.

The principle is illustrated in Figure 5.7. Under normal condition as the left figure shows, toward to the LSB cycle, the summing node voltage is close to zero. No matter the LSB decision is 1 or 0, after the extra switch, it will always give a decision that is opposite to the LSB decision.

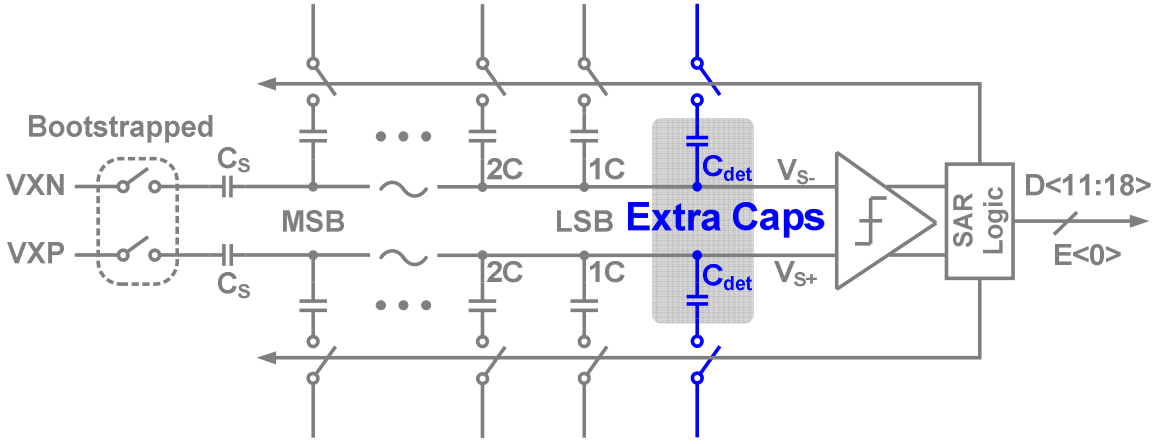


Figure 5.6. Second stage DAC including the extra capacitors for residue detection.

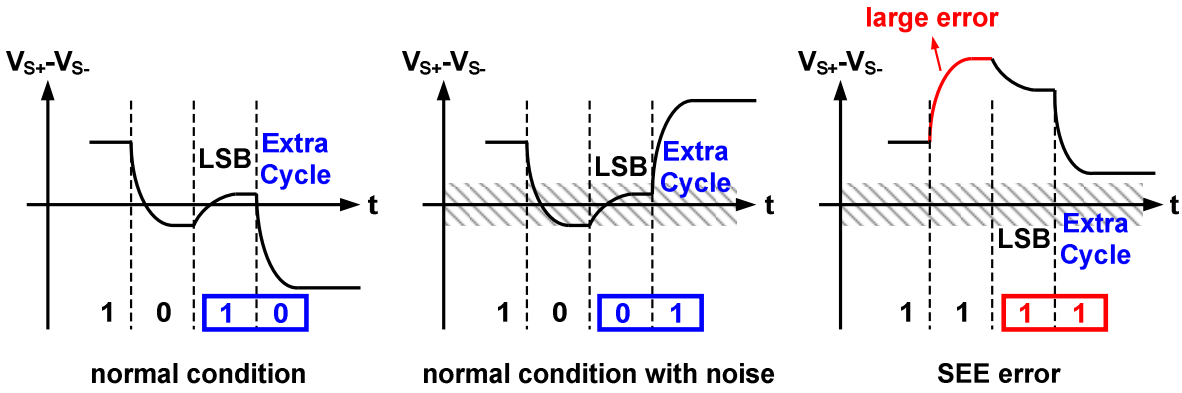


Figure 5.7. Detection principle for the extra DAC capacitors in the 2nd-stage.

Even with noise, like this middle figure shows, The LSB decision should be 1, but due to the noise affection, the actual decision is 0. Then, according to this actual decision, the summing node voltage will switch to a higher positive value, which produces a "1", still opposite to the LSB decision.

However, if due to some reason, say a striking particle disturbed the conversion process somewhere before the LSB cycle, the summing node voltage is likely to be far away from zero. Then the extra comparison tends to give an identical decision as the LSB did. Then we can take

advantage of this good property to detect the 2nd stage residue. In the later measurement, this detection produced near 100% correction rate.

5.3.5 Parity Bit Protection

For digital circuits, TMR is applied for protection. But, there is an exception in this prototype. All the data latches in the SAR loop are not TMR-protected due to the speed consideration. All the data latches are loading the comparator. If again we triple the number of latches, the SAR loop will be significantly slow down (labeled in Figure 5.8 left).

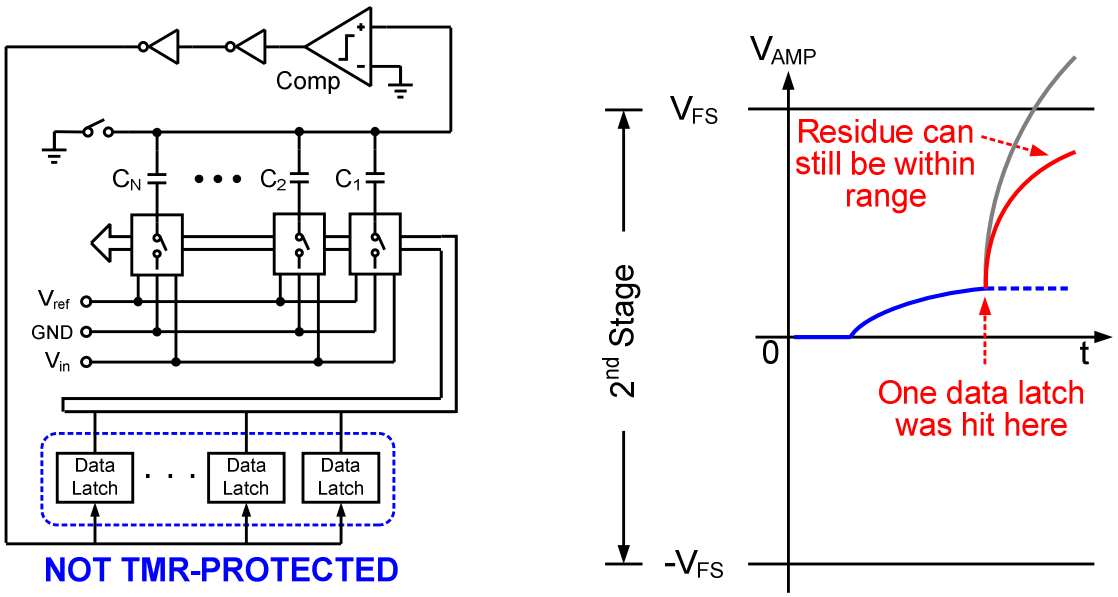


Figure 5.8. SAR loop (left) and illustrative residue transfer waveforms (right).

But if leave those latches untreated, radiations may flip the bits stored in those latches and corrupt the conversion results, because those latches directly control the DAC. However, in most cases, if the summing node voltage is disturbed by the status change of those latches, the residue voltage is likely go over the second stage searching range like the grey curve shown.

Then, by observing the second stage digital codes, we can still tell whether the sub-ADC is intact or not.

But, there is one case. If one data latch is hit toward the end of residue amplification phase, then as this red curve shows on the right of Figure 5.8, the residue may still within the redundancy, and the second stage will still converge. But, the final digital output may be far away from its correct value.

To treat this specific case, parity bit is employed for detection (Figure 5.9). The parity bit circuit follows the comparator and counts the number of 1's as soon as the comparator gives a decision. By the end of the 1st stage bit cycles, the parity bit will done its work and be stored. After the residue amplification, all the data bits are pour out. By comparing the parity bit and the actual data parity, it can be verified whether there is something wrong during the amplification phase, or whether there is status change since the digital bits are stored in the data latches.

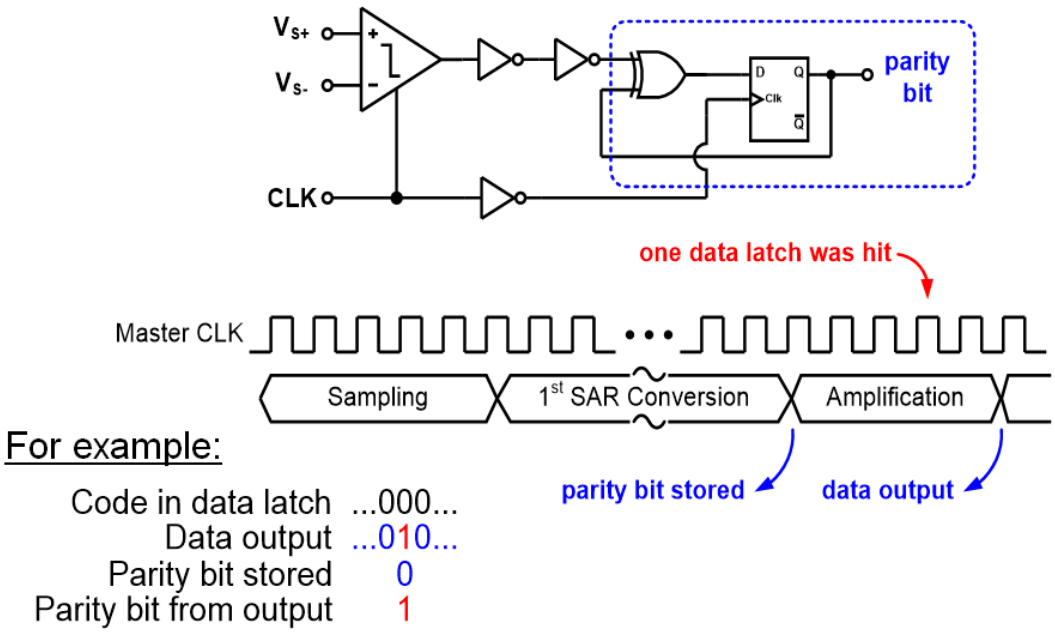


Figure 5.9. SAR loop (left) and illustrative residue transfer waveforms.

5.4 Summary

Various error detection techniques are proposed and described in this chapter. The critical internal nodes of each SAR ADC, including the summing node, the second-stage residue, sampling clock, data latch in the SAR loop, etc. are under surveillance. When one sub-ADC reports error, the digital logics will be activated to select the results from the other sub-ADC for the final output.

CHAPTER 6

PROTOTYPE DESIGN

Error detector techniques and circuit designs is discussed in the previous chapter. In this chapter, some of the ADC design considerations will be covered to increase the operation speed while maintain the resolution of the ADCs.

6.1 Two-Step Pipelined SAR

Within each sub-ADC, a 10-bit plus 8-bit two-step pipelined SAR is implemented with one bit intra-stage redundancy within each stage and two bits inter-stage redundancy. Figure 6.1 plots the block diagram of the two-step SAR sub-ADC. By pipelining the two moderate-resolution SAR, the throughput is boosted. More bits are allocated to the first stage to resolve, which helps relax the residue amplifier design and also relax the noise and linearity requirement for the second stage.

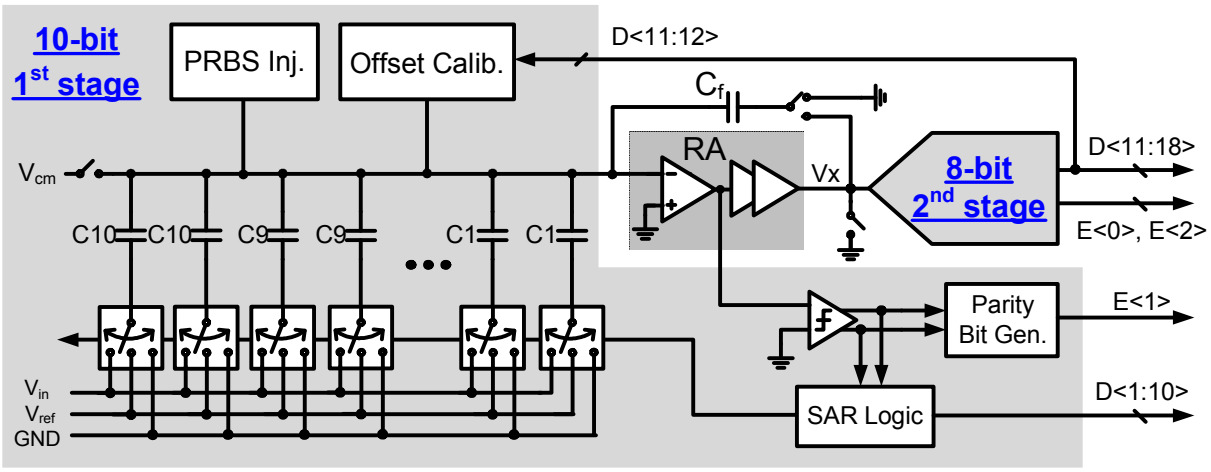


Figure 6.1. Two-step pipelined SAR ADC architecture.

6.2 RA-Comparator Offset Removal

Offset between 1st stage comparator and the residue amplifier should also be taken into considerations. For example, for a 1.2V reference voltage and the 9b + 7b configuration, the second stage full scale is 150 mV and with 2-bit inter-stage redundancy the signal would be bounded within $\pm V_{FS}/4$ in the ideal case as the blue curve shown. If the residue curve goes beyond $3V_{FS}/4$ like the grey curve shown in Figure 6.2, the residue will saturate the second stage, and large conversion errors would occur. The inter-stage gain is 16, so we can calculate that the maximum allowed offset between the first stage comparator and the RA is only 7mV, which is too small to only rely on the device matching.

Figure 6.3 shows a Monte Carlo simulation on the Δ offset between the comparator and residue amplifier. It can be seen this Δ offset can easily go beyond 7mV.

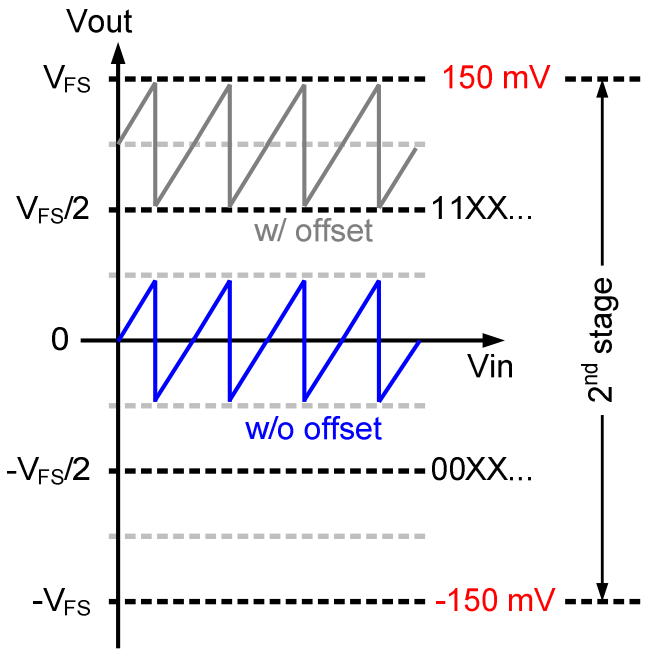


Figure 6.2. 2nd stage residue curve with (gray) and without offset (blue).

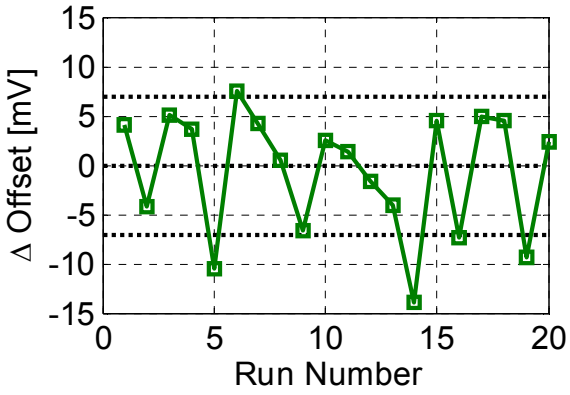


Figure 6.3. Monte Carlo simulation of offset between 1st stage comparator and RA.

Therefore, a preamp sharing scheme is proposed as sketched in the diagram of Figure 6.4. Residue amplifier is a three-stage fully differential amplifier with its first stage reused as the preamplifier for the comparator. So, the dominant part of the offset is removed by this sharing. Any offset from the second and third stage of the RA to the comparator can be viewed as the offset residue, as it will be divided by the first stage gain when input-referred.

And from the Figure 6.5, it can be observed that the Δ offset is consistently confined within ±5mV after this preamp sharing.

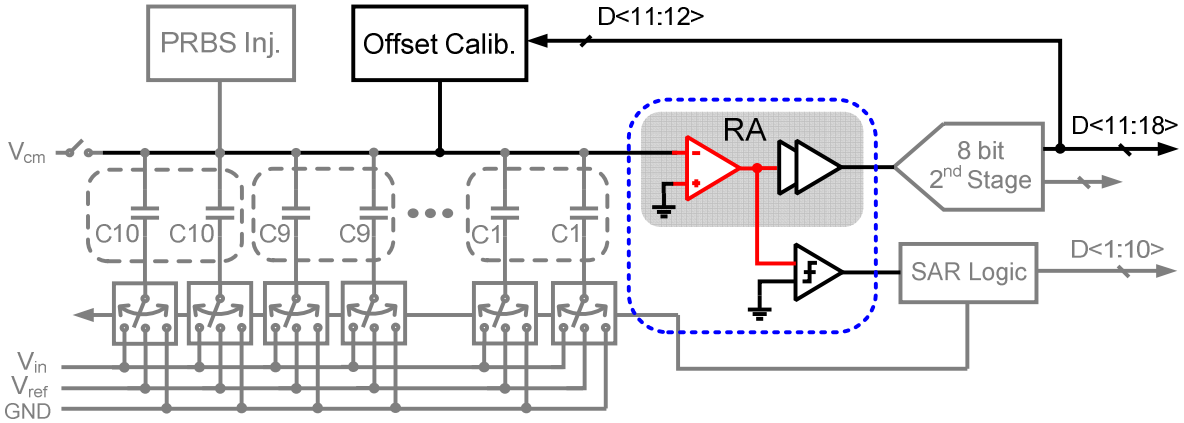


Figure 6.4. Preamplifier and residue amplifier sharing.

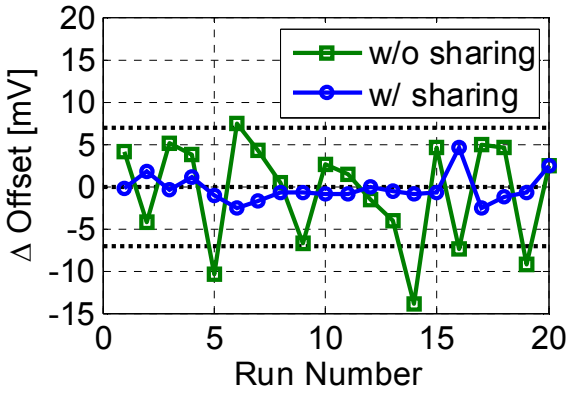


Figure 6.5. Monte Carlo simulation for offset before (green) and after (blue) the preamplifier sharing.

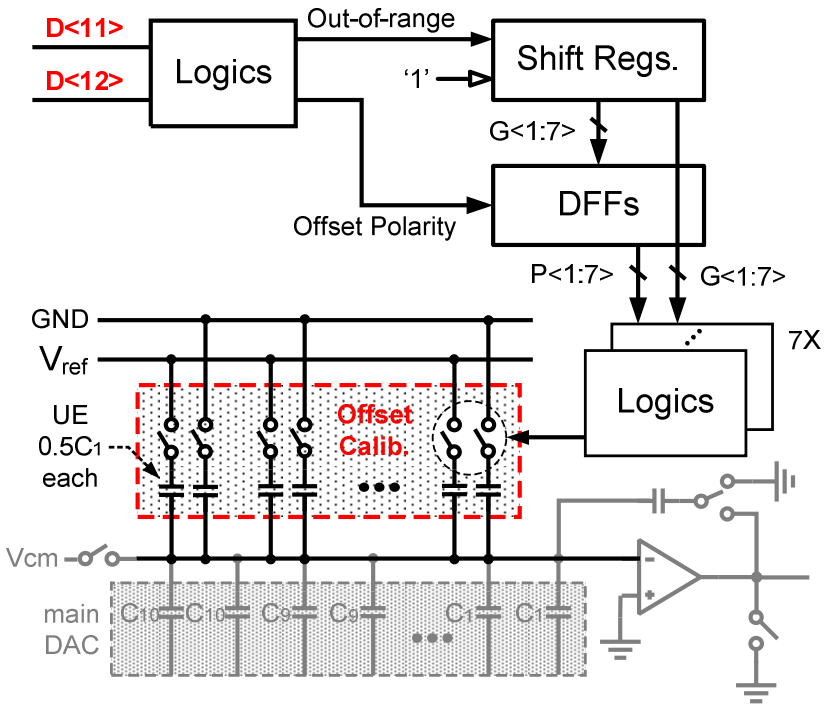


Figure 6.6. Diagram of the two-step SAR residue offset calibration circuit.

To treat the offset residue, a small unit-element DAC is attached to the first-stage summing node to combat this effect. As discussed in the previous slides, the residue voltage should be confined within $\pm V_{FS}/4$ in the ideal case and if it goes beyond $+3V_{FS}/4$ or $-3V_{FS}/4$, then an overflow or underflow will occur. Thus, by monitoring the first two MSBs of the second stage, D<11> and

D<12>, these two cases can be identified. When two of such cases continuously show up, then a small voltage will be injected into the summing node through the calibration DAC to compensate the offset as shown in Figure 6.6. Therefore, the offset residue will be removed too by this calibration circuits, leaving an offset free residue transfer.

6.3 Calibration for DAC Mismatch and RA Gain Errors

The split-ADC architecture not only provides system redundancy for SEE tolerance, but also enables digital calibration for capacitor mismatch [42]. As shown in Figure 6.7, the difference between the two digital outcomes is used as an error signal to direct the adaptation of bit weights [44]. The least mean square (LMS) equations that are used to update the bit weights can be written as follows:

$$\begin{aligned} W_{A,i}(n+1) &= W_{A,i}(n) - \mu \cdot \Delta D_O \cdot D_{A,i} \\ W_{B,i}(n+1) &= W_{B,i}(n) + \mu \cdot \Delta D_O \cdot D_{B,i} \end{aligned} \tag{6.1}$$

where $W_{A,i}/W_{B,i}$ and $D_{A,i}/D_{B,i}$ are the bit weight and bit value of the i^{th} bit respectively for ADC_A/ ADC_B; μ is a constant which determines the convergence speed; n is the number of update. Once the radices are correctly identified for both ADCs, the two calibrated outcomes d_A and d_B must be identical, leading to a zero difference ΔD_O (which halts the radix update).

The residual curves of the split-ADC must be different from each other to rule out the scenario when the two ADCs commit errors in the same way and the output difference is still zero. This is realized by injecting a small offset voltage to the summing node through a small capacitor C_{CAL}, as shown in Figure 6.8. The two residual curves are shifted in different directions near the transition points.

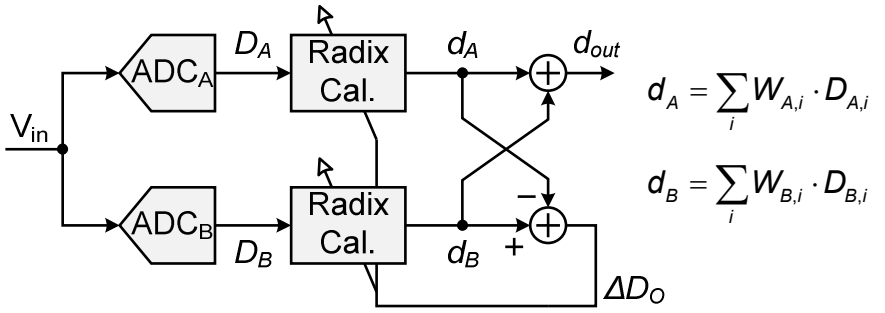


Figure 6.7. LMS digital calibration scheme.

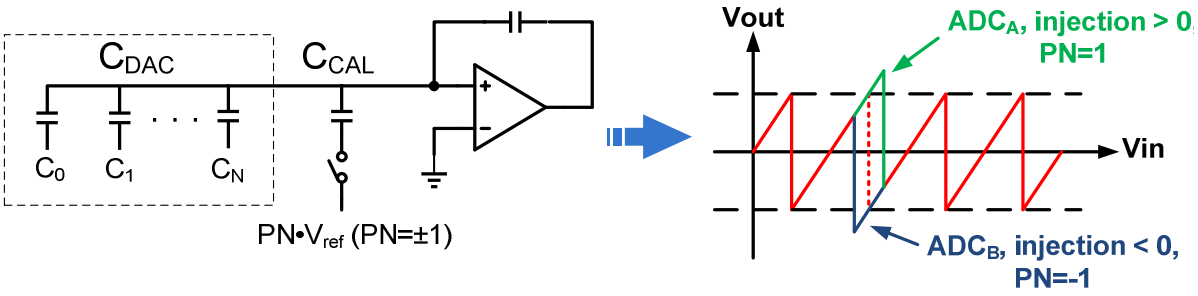


Figure 6.8. Offset injection for residual curve differentiation.

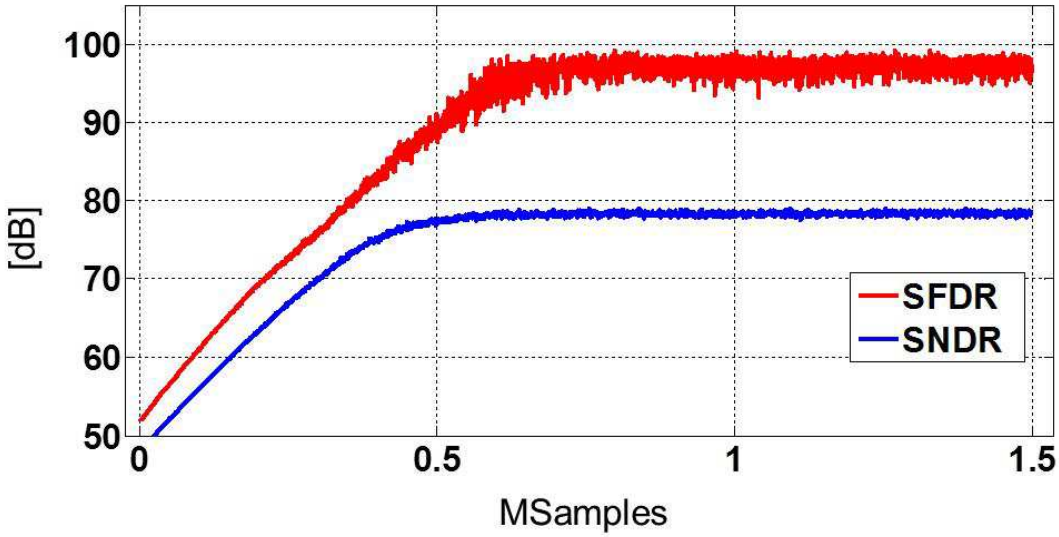


Figure 6.9. Learning curve of SNDR and SFDR.

The calibration technique has been verified by the behaviour simulation. The split-ADC model used in the simulation includes capacitor mismatches, inter-stage gain error, offset and

noise of the comparator and the amplifier. The simulation result is shown in Figure 6.9. The SNDR and SFDR increase from below 60 dB to about 79 dB and 97 dB respectively. The calibration converges fast in less than 1 million samples, corresponding to 12.5 ms under 80 MSPS conversion rate.

CHAPTER 7

EXPERIMENTAL RESULTS

Measurement results are presented in this chapter, which includes both electronic test results and the irradiation test results.

7.1 Regular Electronic Test Results

The prototype is fabricated in 65-nm CMOS process. The core is 600 µm by 570 µm, occupying 0.342 mm^2 active area. As shown in Figure 7.1, clock generation circuits and reference buffers sit in the center and the two sub-ADCs are laid out symmetrically on the side.

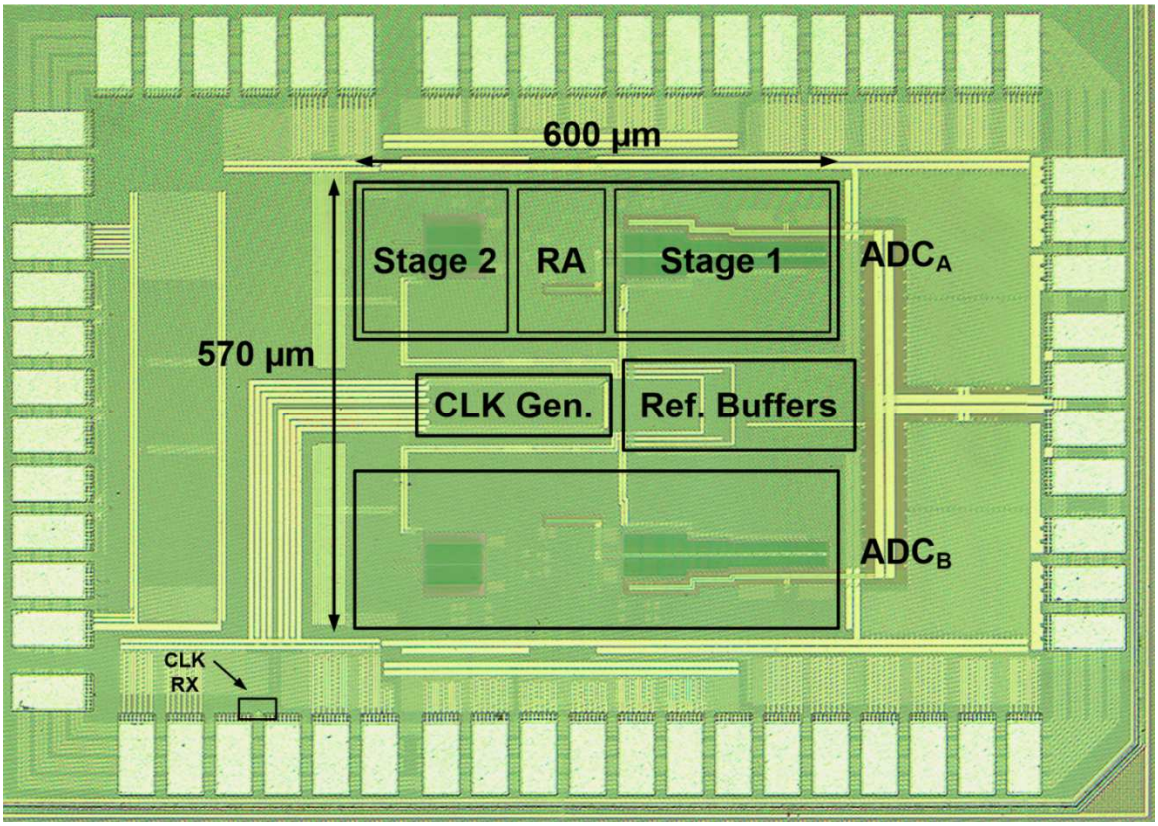


Figure 7.1. Die Photo

7.1.1 Static Linearity

Figure 7.2 shows the DNL and INL plots at 35M sample rate. DNL is within plus and minus 0.4 LSB and INL is within about plus and minus 0.5 LSB. Both indicate the good linearity of the prototype design.

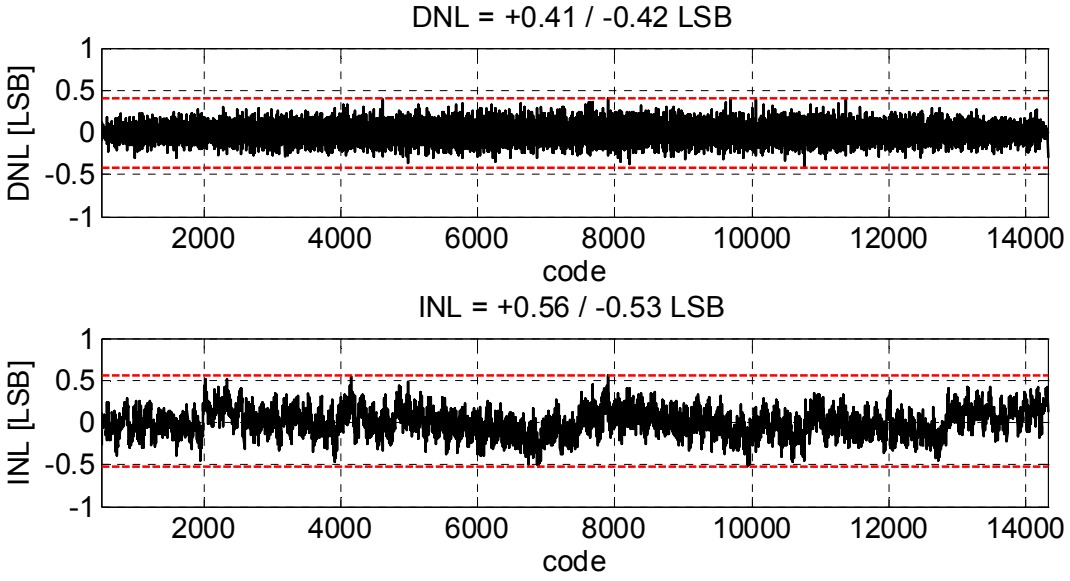


Figure 7.2. DNL and INL plots with 5-MHz input sine signal at 35MS/s sample rate.

7.1.2 Dynamic Performance

These are measured FFT spectra at 35MSPS and 40MSPS for a 5MHz sine-wave input. It demonstrates 78.5dB SNDR and 103dB SFDR after a foreground calibration of DAC mismatch and RA gain errors under 35MSPS. This results is after the averaging of the two sub-ADCs' outputs and same for the results shown in the following slides. This measurement at the low sample frequency is for comparison purpose with other work.

At 40MSPS, it demonstrates 78dB SNDR and 95dB SFDR after a foreground calibration of DAC mismatch and RA gain errors. And this sample rate is used in the ATLAS experiment.

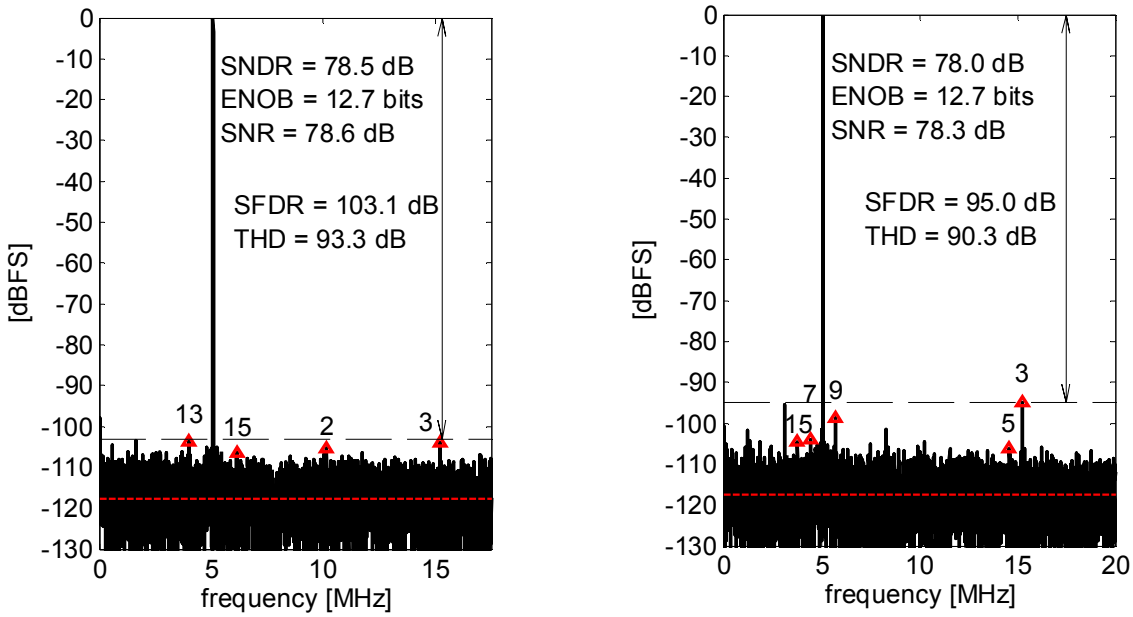


Figure 7.3. FFT spectra with 35MS/s (left) and 40MS/s (right) sample rate with 5-MHz input.

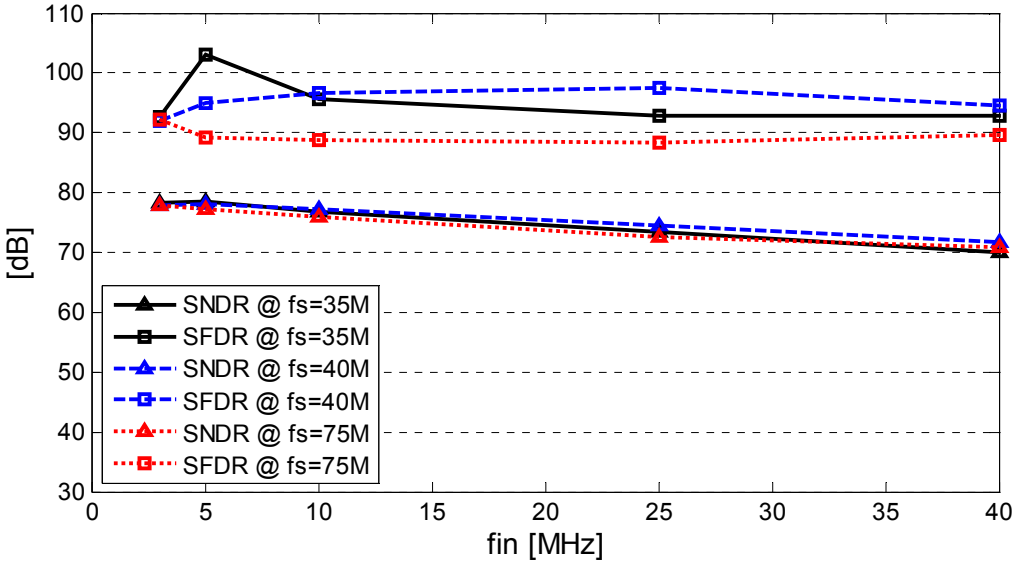


Figure 7.4. ADC Dynamic Performance

This figure plots the ADC dynamic performance at 35, 40 and 75MS/s. The amplitude of the input signal ranges between -0.5 and -2.0dBFS. At 35 and 40MS/s, the prototype measures a

>75dB SNDR and a >90dB SFDR up to the Nyquist frequency. At 75MS/s, it measures a >70dB SNDR and a >88dB SFDR up to the Nyquist.

7.1.3 Power Consumptions

Here is a power breakdown measured at 40 MSPS sample rate and also the power consumption versus sample rate plot. Most of the powers are consumed by the residue amplifiers and the reference buffer, while the digital circuit only consumes 14% of the total power in spite of the TMR applied. The total power consumption is only 24.9 mW at 75 MSPS sample rate and 22.2 mW at 40 MSPS.

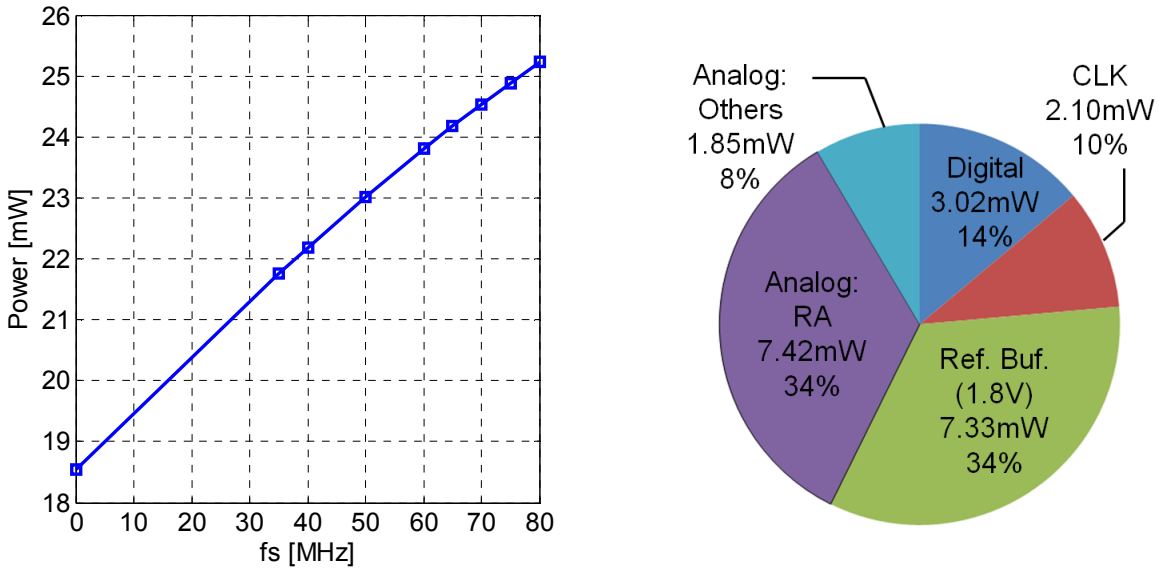


Figure 7.5. Power consumption vs. sample rate (left) and power breakdown at 40 MS/s sample rate.

7.1.4 Summary

Table 7.1 summarizes this work and compares it with other the state-of-the-art 14-bit SAR ADCs [45], [46] and a recent 12-bit radiation tolerant pipelined ADC [23].

It can be seen that in each corresponding sample frequency, this prototype measures the highest peak SNDR and peak SFDR as well as the lowest power consumption, which includes all the redundant circuits for radiation tolerance and two on-chip reference buffers. It also achieves the highest Schreier FoM and the best Walden FoM.

Table 7.1. Summary and Comparisons

		This work			ISSCC15 Kramer	JINST13 Kuppambatti	ISSCC13 Kapusta
Process [nm]		65			40	130	65
Resolution [bits]		14			14	12	14
fs [MS/s]		35	40	75	35	40	80
SNDR [dB]	@ DC	78.5	78.0	77.8	75	67.8	73.6
	@ Nyquist	75.1	74.4	70.8	74.4	67	71.3
SFDR [dB]	@ DC	103.1	95.0	92.1	99	77.8	85.7
	@ Nyquist	94.3	98.9	89.6	90	78	≥80.3
Power [mW]		21.8	22.2	24.9	54.5	55	31.1
Aera [mm^2]		0.342			0.236	n/a	0.55
FoM_1 [dB]	@ DC	170.6	170.6	172.6	163.1	156.4	167.7
	@ Nyquist	167.2	167.0	165.6	162.5	155.6	165.4
FoM_2 [fJ/c.-s.]	@ DC	90.6	85.5	52.3	338.8	685.4	99.4
	@ Nyquist	134.0	129.4	117.2	363.1	751.6	129.5

7.2 Irradiation Test results

The irradiation tests are performed in two parts. One is the SEE test with proton beams and the other one is the TID test with X-ray.

7.2.1 SEE test results

Setup

In the SEE test, proton beam is aligned to the center of the chip. The beam has a spread and the spread is in Normal distribution with its sigma of about 5mm. But the die size is only 1.5mm by 1mm, so, it is completed covered by the beam. FPGA board, power boards, and DC power supply are about 2 meters away from the beam, and three signal generators for clocks and input are also about 2 meters away from the beam. But there is no additional shielding for these instruments. Then the FPGA output is connected to the computer in the control room through a 150-feet Ethernet cable.

Table 7.2. Radiation Dose

	Time Duration (s)	Approximate Flux (protons/cm^2/s)	TID Effects
Run 1	4700	3×10^8	120 Krad
Run 2	5394	6×10^8	240 Krad
Run 3	470	10×10^8	40 Krad
Total	10564	-	400 Krad

Table 7.2 lists the radiation plan and the actual dose and dose rate in the experiment. The goal is reach a total fluence of 3.8×10^{12} protons/cm^2 which is the ATLAS LAr calorimeter spec. The experiment was divided into 3 separate runs in order to start with a low dose rate, which is the flux shown in the third column of the above table. (Flux is in the unit of protons/cm^2/s.) After these three runs, the chip actually received 5.05×10^{12} protons/cm^2 fluence. The proton energy is 120MeV.

Measured Results

Figure 7.6 shows the error records before correction and after correction when beam is on. The x- and y-axis labeled with ΔD_{OA} and ΔD_{OB}, represent the error of ADC_A and ADC_B, respectively. It can be seen from the left figure, all the large errors are located along x- or y-axis, indicating the uncorrelated characteristics of those errors and when one sub-ADC encounters problem, the results from the other ADC are always usable. This is a good sign and just as expected: the probability of both ADCs being wrong is significantly low. And not one single case was observed during the 3-4 hours test.

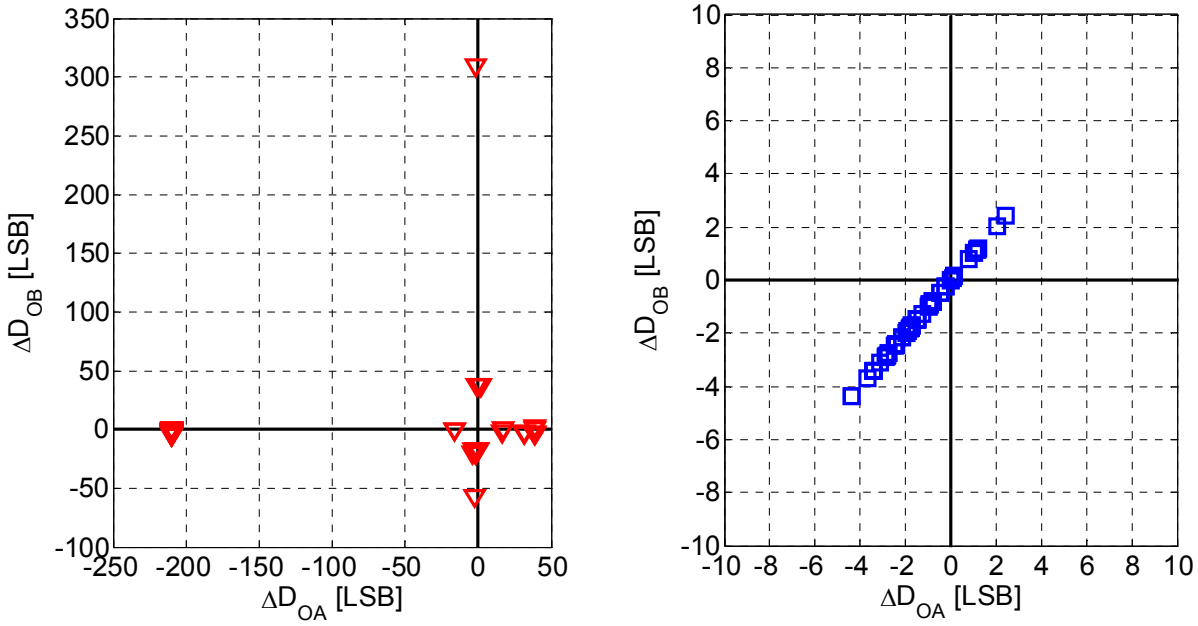


Figure 7.6. Error plot of ADC_A and ADC_B before (left) and after (right) the correction.

The right figure is the results after applied extra bit cycle and parity bit detections. In order to plot in the same figure with the same scale, the erroneous results were enforced to equal to the correct one. Therefore, the blue squares lie on the diagonal. From the right-hand-side figure, first of all, all the errors are successfully detected, reaching a 100% detection rate and

secondly, after correction, all the errors are bounded within ±4 LSBs, producing a 100% correction rate.

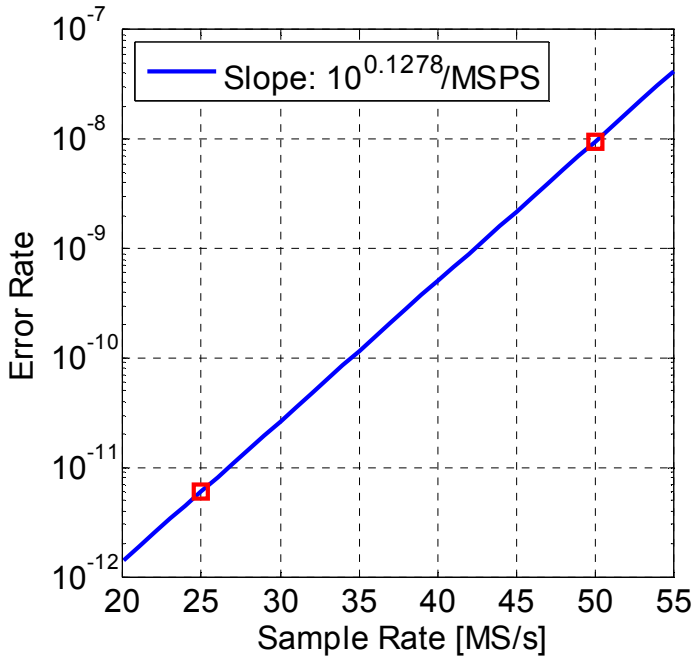


Figure 7.7. Error rate at 25 MS/s and 50 MS/s and fitted line (blue).

Another test is conducted with the same setup but no radiations. Under this condition, most of the errors should be generated by metastability.

The ADC was set to run for about 9 hours at 50MHz sample frequency for a phase-locked 10MHz sine-wave input and the experiment was repeated with 25MHz sample clock and a phase-locked 5-MHz sine-wave input. All the errors were recorded and counted. Figure 7.7 reflects the huge difference of the raw error rates under the two different sample rates.

After perform the detection and correction logic, all the errors are successfully corrected for both sample rates, leading to a less than 10^{-12} error rate. But this is limited by the observation time. The question is what the theoretic lowest error rate would be.

Theoretically speaking, after the correction is performed, the error rate will be lowered to p^2 if the raw error rate of each sub-ADC is p. So, Figure 7.8 showcases this p to p^2 relationship and interprets it into the "time domain", which is the average time to observe one error on the y-axis. The red and blue curves are the error rate to time one-on-one correspondence line of 25M and 50M sample rates respectively. Two stars represent the raw error rates before correction, which is p; and the two squares represent the error rates after correction, which is p^2.

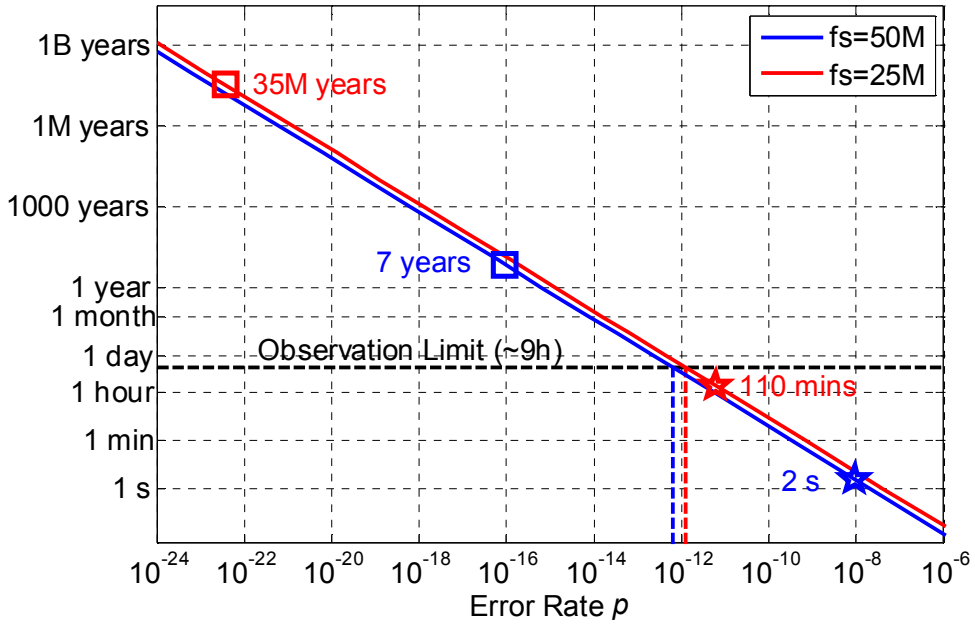


Figure 7.8. Error rate to observation time mapping

From the figure, it's clear that due to the observation time limit, we did not see one single error after the correction, because the error rate is around 10^{-12}. And if we want to observe one error after the correction is performed, then we have to wait 7 years at 50MS/s sample rate and 35 million years at 25MS/s sample rate on average, which indicates the very high reliability of the prototype with the split structure and all the detection circuits involved.

Figure 7.9 shows the raw error rate versus error threshold. It can be seen that the curve is nearly flat, indicates the weak dependence of the error rate on the threshold.

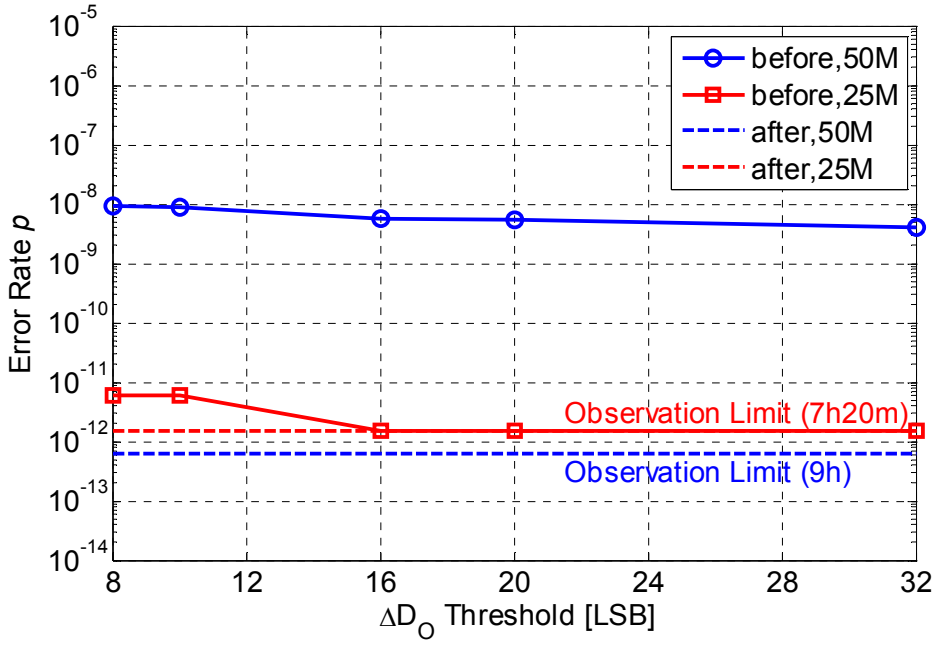


Figure 7.9. Error rate vs. error threshold

7.2.2 TID Test Results

Setup

The second part of the irradiation test is the total ionization dose test. The prototype ADC was exposed under the X-ray. During the exposure, the chip was powered up and clock was turned on but no input signal was fed in. We exposed the chip with a certain dose of X-ray each time and after the irradiation is done, we brought back the chip and measured its performance.

Measured Result

Figure 7.10 shows the TID test results. Left-hand-side figure shows the measured SNDR and SFDR after each cumulated radiation dose in kilo rad. And the right-hand-side figure is the

total power consumption of the chip after each exposure. Up to 1 Mrad, the maximum SNDR and SFDR degradation is less than 1 dB and maximum power variation is less than 1 mW. And 1 Mrad is a ten years TID with a safety factor of 25.

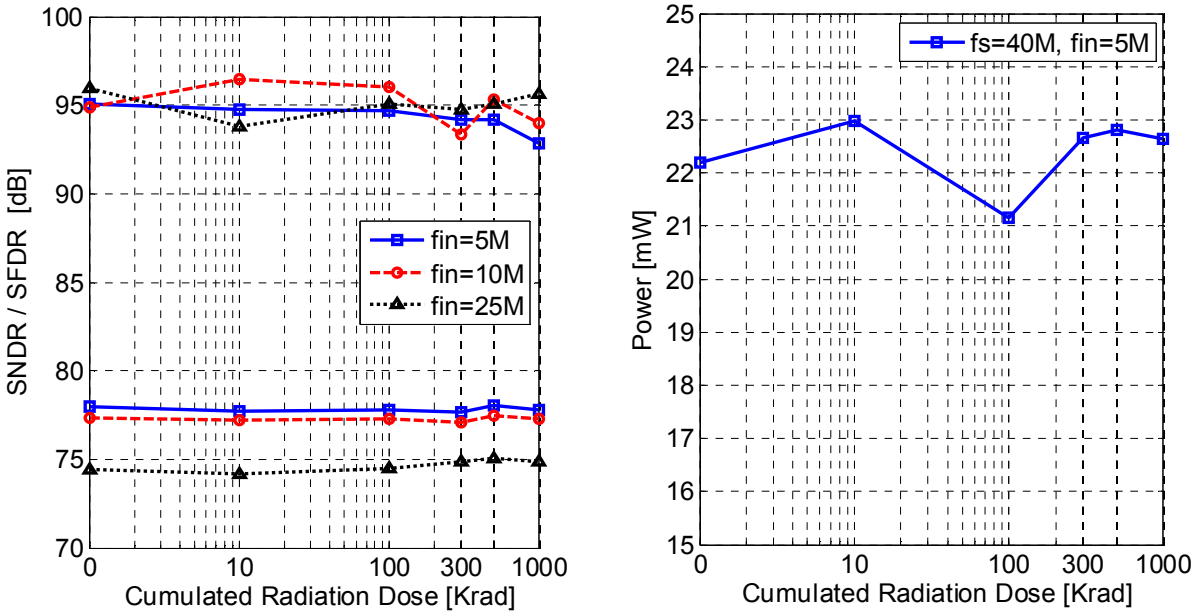


Figure 7.10. SNDR and SFDR (left) and power consumption (right) variation vs. dose rate.

CHAPTER 8

CONCLUSION

Theoretical Analysis extended from [11] to construct the extended LOF for m-tuple joint estimation is present. Decision feedback technique is employed for pileup removal. The systematic estimation error due to the first-order truncation on the signal model is mitigated by the iterative LOF. Results from Monte Carlo simulation validate the proposed algorithm and a comparison with LOF and Wiener filter is also conducted, demonstrating the superior performance of the proposed sequence detection algorithm. Error accumulation issue in the feedback equalization system is addressed with modification of the shaper in the readout system, with no significant revision on circuit implementations.

On the other hand, to accommodate the above digital signal processing needs, a low-power 14-bit radiation-tolerant ADC is proposed. Measurement results prove that redundant split SAR ADC with built-in SEE detection circuits not only provides an architecture and circuit solution to radiation tolerance, but also reduces the ADC metastability errors (both improved from p to p^2). The prototype measured 78dB SNDR and 90-100dB SFDR with less than 25mW power for 0-75MS/s. The prototype also measured a 100% correction rate for SEE and metastability errors.

REFERENCES

[1] L. Evans and P. Bryant (editors), "LHC machine," *J. of Instrumentation*, vol. 3, no. 8, Aug. 2008.

[2] CERN AC Team, 1999. Available at: https://cds.cern.ch/record/40525.

[3] B. T. Huffman, "Plans for Phase II Upgrade to the ATLAS detector," *J. of Instrumentation*, vol. 9, no. 2, Feb. 2014.

[4] ATLAS collaboration, "The ATLAS experiment at the CERN large hadron collider," *J. of Instrumentation*, vol. 3, no. 8, Aug. 2008.

[5] M. Newcomer, "New Developments for the ATLAS Liquid Argon Calorimeter Front End Electronics," internal slides, 2016.

[6] G. M. Haller, J. D. Fox, and S. R. Smith, "The Liquid Argon Calorimeter system for the SLC Large Detector," *IEEE Trans. Nucl. Sci.*, vol. 36, no. 1, 1989, pp. 675-679.

[7] H. Abreu *et al.*, "Performance of the electronic readout of the ATLAS liquid argon calorimeters," *J. of Instrumentation*, vol. 5, no. 9, Sep. 2010.

[8] Agnes Szeberenyi (CERN), "Key highlights towards the High Luminosity LHC era," 2014. Available at: http://acceleratingnews.web.cern.ch/content/recent-progress-hilumi-project-0.

[9] G. Aad *et al.*, "Drift time measurement in the ATLAS Liquid Argon electromagnetic calorimeter using cosmic muons," *European Physical Journal C*, vol. 70, no. 3, 2010, pp. 755-785.

[10] M. Newcomer, "LAPAS: A SiGe Front End Prototype for the Upgraded ATLAS LAr Calorimeter," *Topical Workshop on Electronics for Particle Physics* (*TWEPP*'09), Paris, France, Sep. 21-25, 2009, pp. 132-135.

[11] W. E. Cleland, and E. G. Stern, "Signal processing considerations for liquid ionization calorimeters in a high rate environment," *Nuclear Instruments and Methods in Physics Research. A*, vol. 338, no. 2-3, 1994, pp. 467-497.

[12] J. G. Proakis and D. G. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4th Edition, Pearson Prentice-Hall, 2007.

[13] J. Wang *et al.*, *Nuclear Electronics*, 1st Edition, Atomic Energy Press, Beijing, 1983.

[14] S. Starz, "Development and implementation of optimal filtering in a Virtex FPGA for the upgrade of the ATLAS LAr calorimeter readout," *J. of Instrumentation*, vol. 7, no. 12, Dec. 2012.

[15] T. R. Andeen *et al*., "Upgraded readout electronics for the ATLAS liquid argon calorimeters at the high luminosity LHC," *J. Phys. Conf.*, Ser. 404, 2012, 012061.

[16] H. Xu, Y. Chiu, and D. Gong, "A Linear Optimal Filtering Approach for Pileup Noise Removal in High-Rate Liquid Ionization Calorimeters," *IEEE Nuclear Science Symp*. (*NSS'*13), Seoul, S. Korea, 2013.

[17] H. Xu, D. Gong, and Y. Chiu, "A comparative study of amplitude and timing estimation in experimental particle physics using Monte Carlo simulation," *Journal of Modern Physics*, vol. 4, no. 5B, May 2013, pp. 42-47.

[18] Single Event Effect. Available at: https://radhome.gsfc.nasa.gov/radhome/see.htm.

[19] M. Dentan, "Radiation effects on electronic components and circuits," CERN Training, April 2000.

[20] L. Gonella, F. Faccio, M. Silvestri, S. Gerardin, D. Pantano, V. Re, M. Manghisoni, L. Ratti, and A. Ranieri, "Total Ionizing Dose effects in 130-nm commercial CMOS technologies for HEP experiments," *Nuclear Instruments and Methods in Physics Research. A*, vol. 582, no. 3, Dec. 2007.

[21] V. Re, L. Gaioni, M. Manghisoni, L. Ratti, V. Speziali, and G. Traversi, "CMOS technologies in the 100nm range for rad-hard front-end electronics in future collider experiments," *Nuclear Instruments and Methods in Physics Research. A*, vol. 596, no. 1, Oct. 2008.

[22] H. Xu, Y. Zhou, Y. Chiu, D. Gong, T. Liu, and J. Ye, "High-speed, high-resolution, radiation-tolerant SAR ADC for particle physics experiments," *J. of Instrumentation*, vol. 10, no. 4, April 2015.

[23] J. Kuppambatti, J. Ban, T. Andeen, P. Kinget, and G. Brooijmans, "A radiation-hard dual channel 4-bit pipeline for a 12-bit 40 MS/s ADC prototype with extended dynamic range for the ATLAS liquid argon calorimeter readout electronics upgrade at CERN LHC," *J. of Instrumentation*, vol. 8, no. 7, July 2013.

[24] A. Rivetti, G. Anelli, F. Anghinolfi, G. Mazza and F. Rotondo, "A low-power 10-bit ADC in a 0.25μm CMOS: design considerations and test results," *IEEE Trans. Nucl. Sci.*, vol. 48, no. 4, Aug. 2001.

[25] J. Verbeeck, M. V. Uffelen, M. Steyaert and P. Leroux, "A radiation hard delta sigma ADC in 130 nm CMOS," 8th *Conference on Ph.D. Research in Microelectronics and Electronics* (*PRIME*), June 2012.

[26] A. L. Sternberg, L. W. Massengill, M. Hale and B. Blalock, "Single-event sensitivity and hardening of a pipelined analog-to-digital converter," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, Dec. 2006.

[27] F. Baille, G. Borel, B. Commere, F. Roy, C. Delmas and C. Terrier, "A multi Mrad hardened 8 bit/20 MHz flash ADC," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 3, June 1992.

[28] S. Devarajan, L. Singer, D. Kelly, S. Decker, A. Kamath, and P. Wilkins, "A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS Pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, Dec. 2009.

[29] Y. Chiu, P. R. Gray and B. Nikolic, "A 1.8 V 14 b 10 MS/s pipelined ADC in 0.18 μm CMOS with 99 dB SFDR," *IEEE International Solid-State Circuits Conference* (*ISSCC*'04), San Francisco, CA, Feb. 2004.

[30] W. Yang, D. Kelly, I. Mehr, M. T. Sayuk, and L. Singer, "A 3-V 340-mW 14-b 75-Msample/s CMOS ADC With 85-dB SFDR at Nyquist Input," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, Dec. 2001.

[31] H.-S. Che, B.-S. Song, and K. Bacrania, "A 14-b 20-MSamples/s CMOS Pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, June 2001.

[32] H. Pan, M. Segami, M. Choi, J. Cao, F. Hatori, and A. Abidi, "A 3.3V, 12b, 50MSample/s A/D Converter in 0.6μm CMOS with over 80dB SFDR," *IEEE International Solid-State Circuits Conference* (*ISSCC*'00), San Francisco, CA, Feb. 2000.

[33] J. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques—Part I," *IEEE Journal of Solid-State Circuits*, vol. SC-10, no. 6, Dec. 1975.

[34] W. Liu, P. Huang and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW redundant successive-approximation-register analog-to-digital converter with digital calibration," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, Nov. 2011.

[35] C.-C. Liu, S.-J. Chang, G.-Y. Huang, and Y.-Z. Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, April 2010.

[36] C.-C. Liu, "A 0.35 mW 12 b 100 MS/s SAR-assisted digital slope ADC in 28 nm CMOS," *IEEE International Solid-State Circuits Conference* (*ISSCC*'16), San Francisco, CA, Feb. 2016.

[37] C. C. Lee and M. P. Flynn, "A SAR-assisted two-stage pipeline ADC," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 4, April 2011.

[38] W. J. Snoeys, T. A. P. Gutierrez, and G. Anelli, "A new NMOS layout structure for radiation tolerance," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 4, Aug. 2002.

[39] ATLAS collaboration, "ATLAS Letter of Intent Phase-II Upgrade," CERN, Rep. LHCC-I-023, Dec. 2012.

[40] H. Venkatram, J. Guerber, M. Gande, and U.-K. Moon, "Detection and Correction Methods for Single Event Effects in Analog to Digital Converters," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 60, no. 12, Dec. 2013.

[41] H. Xu, Y. Cai, L. Du, Y. Zhou, B. Xu, D. Gong, J. Ye and Y. Chiu, "A 78.5dB-SNDR radiation and metastability-tolerant two-step split SAR ADC operating up to 75MS/s with 24.9mW power consumption in 65nm CMOS," *IEEE International Solid-State Circuits Conference* (*ISSCC*'17), San Francisco, CA, Feb. 2017.

[42] J. McNeill, M. Coln, and B. Larivee, "A split ADC architecture for deterministic digital background calibration of a 16b 1MS/s ADC," *IEEE International Solid-State Circuits Conference* (*ISSCC*'05), San Francisco, CA, Feb. 2005.

[43] T. Miki, T. Morie, K. Matsukawa, Y. Bando, T. Okumoto, K. Obata, S. Sakiyama, and S. Dosho, "A 4.2 mW 50 MS/s 13 bit CMOS SAR ADC with SNR and SFDR enhancement techniques," *IEEE J. Solid-State Circuits*, vol. 50, no. 6, June, 2015.

[44] Y. Zhou, B. Xu, and Y. Chiu, "A 12 bit 160 MS/s two-step SAR ADC with background bit weight calibration using a time-domain proximity detector," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 4, April 2015.

[45] M. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14b 35MS/s SAR ADC Achieving 75dB SNDR and 99dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE International Solid-State Circuits Conference* (*ISSCC*'15), San Francisco, CA, Feb. 2015.

[46] R. Kapusta, J. Shen, S. Decker, H. Li, and E. Ibaragi, "A 14b 80MS/s SAR ADC with 73.6dB SNDR in 65nm CMOS," *IEEE International Solid-State Circuits Conference* (*ISSCC*'13), San Francisco, CA, Feb. 2013.

BIOGRAPHICAL SKETCH

Hongda Xu received the Bachelor of Engineering (B.E.) degree in electrical engineering from Southeast University, Nanjing, China, in 2010, and the Master of Science (M.S.) degree in electrical engineering from The University of Texas at Dallas, Texas, USA, in 2013. He has been working towards a Ph.D. degree at The University of Texas at Dallas since 2013. His main research interests include high resolution, radiation-tolerant ADC design and digital signal processing techniques for high-precision data readout in high-energy physics experiments.

CURRICULUM VITAE

Education

- **08/2013 – 05/2017:** The University of Texas at Dallas (UT Dallas), Richardson, Texas
  Ph.D. candidate in Electrical Engineering, with Texas Analog Center of Excellence (TxACE)
  - **Focus:** High-resolution error-tolerant ADCs and equalization and filtering algorithms for analog frontend (AFE) in data readout system
  - **Advisor:** Dr. Yun Chiu
- **08/2011 – 05/2013:** The University of Texas at Dallas (UT Dallas), Richardson, TX
  Master of Science in Electrical Engineering (M.S.E.E.)
  - **Track:** Circuit and System
- **09/2006 – 06/2010:** Southeast University, Nanjing, Jiangsu, China
  Bachelor of Engineering (B.E.)
  - **Major:** Electrical Engineering

Research Experience

- **09/2014 – 02/2017:** Radiation- and error-tolerant ADC design
  - A 14-bit radiation- and metastability-tolerant ADC is proposed for the applications in high-energy physics experiments. By exploiting the substantial redundancies embedded from the top-level architecture design down to each circuit block and all the proposed detection circuits/techniques, this two-step pipelined split SAR ADC demonstrates the ability to tolerant and correct conversion errors induced by radiation and metastability in the irradiation test. In the normal electronic test, this prototype measures 78.5 dB peak SNDR and over 100 dB peak SFDR at 35MS/s sample rate and it can operate up to 75 MS/s with close to 90 dB SFDR at Nyquist frequency.
- **08/2013 – 05/2015:** Digital signal processing algorithm development for AFE readout
  - A sequence detection algorithm with decision-feedback equalization (DFE) is proposed for high-precision amplitude/energy estimation in analog frontend readout system for high-energy physics experiments. By extending the linear optimal filtering algorithm and incorporating the DFE, signal pileup effect is greatly reduced, leading to unbiased minimum-deviation amplitude/energy estimation in the high-luminosity environment. The proposed algorithm is a good candidate to accommodate the signal processing needs for the next phase electronic upgrade in the LHC experiments at CERN in the near future.

Publications

- **H. Xu**, Y. Cai, L. Du, Y. Zhou, B. Xu, D. Gong, J. Ye and Y. Chiu, "A 78.5dB-SNDR radiation- and metastability-tolerant two-step split SAR ADC operating up to 75MS/s with 24.9mW power consumption in 65nm CMOS," in the International Solid-State Circuit Conference (ISSCC) 2017, San Francisco, CA, 2017.
- **H. Xu**, Y. Zhou, Y. Chiu, D. Gong, T. Liu, and J. Ye, "High-speed, high-resolution, radiation-tolerant SAR ADC for particle physics experiments," Journal of Instrumentation (JINST), 2015, 10 C04035, doi:10.1088/1748-0221/10/04/C04035.
- **H. Xu**, D. Gong, and Y. Chiu, "A sequence detection algorithm for pulse amplitude estimation in high-rate liquid ionization calorimeters," in IEEE Nuclear Science Symposium (NSS'15), San Diego, CA, 2015.
- **H. Xu**, D. Gong, and Y. Chiu, "On the performance of linear optimal filter and Wiener filter for signal detection in liquid ionization calorimeters," in IEEE Nuclear Science Symposium (NSS'14), Seattle, WA, 2014.
- **H. Xu**, Y. Chiu, and D. Gong, "A linear optimal filtering approach for pileup noise removal in high-rate liquid ionization calorimeters," in 2013 IEEE Nuclear Science Symposium (NSS'13), Seoul, S. Korea, Oct. 2013

Awards

- **02/2017** ADI Outstanding Student Designer Award
- **08/2015** Louis Beecherl, Jr. Graduate Fellowship (2015-2016 Academic Year)
- **05/2013** Erik Jonsson School Graduate Scholarship (2013-2014 Academic Year)
- **06/2010** Outstanding Graduate of Southeast University
- **04/2009** Honorable Mention in 2009 Mathematical Contest in Modeling (MCM)

Working Experience

- **08/2013 – 05/2017** Research Assistant in TxACE
- **08/2013 – 01/2014** Teaching Assistant of "EE6325 VLSI Design"