GAN-BASED DC-DC CONVERSION ACHIEVING

HIGH RELIABILITY, LOW EMI AND BALANCED SYSTEM PERFORMANCE

by

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To my wife, Li Fu, daughters, and dear family

Thank you for all the love and support

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Yingping Chen, PhD
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Supervising Professor: Dr. Dongsheng Brian Ma

DC-DC power conversion circuits improve the switching frequency consistently over the past five decades, pursuing better dynamic response and higher power density. To empower such a trend, silicon power transistors have been advancing continuously. However, they are approaching the theoretical limit of performance, slowing down the developing pace of power electronics. With superior switching characteristic, gallium nitride (GaN) high-electron-mobility transistor (HEMT) rapidly emerged, pushing the operating speed of DC-DC power circuits to a record high level. GaN technology is thus recognized as a promising candidate to enable the next-generation switching power conversion. However, it still faces formidable challenges before the industry-wide adoption, including unique reliability issues, considerable electromagnetic interference (EMI) emissions and intensified power design trade-offs. This dissertation delivers key innovations in power stage, gate driver and control scheme, intending to conquer these challenges.

To improve the reliability of GaN power stage, an online condition monitoring is developed to prognose the current-collapse (or *i*-collapse) effect in GaN HEMT, sensing its dynamic on-resistance as aging precursor. A gate leakage inspired junction temperature T_J sensor is integrated

to determine the T_J of GaN HEMT, facilitating the calibration of temperature effect on the dynamic on-resistance. As the benefit, T_J-independent online condition monitoring is accomplished, significantly improving the monitoring accuracy. Further, to enhance the system longevity, a proactive temperature frequency scaling scheme is designed to modulate the operating speed according to the thermal stress and power conditions, thereby extending the GaN lifetime while minimizing the impact on the system performance of the converter.

To reduce the conducted EMI noise, an adaptive strength gate driving scheme is developed for GaN HEMT. By modulating the driving strength at the start point of Miller Plateau during the switching transitions, it achieves an independent control of low di/dt and high dv/dt. Thus, the conducted EMI noise, mainly caused by di/dt, is reduced, while the switching power loss overhead is minimized. By such a means, the classic design trade-off between EMI noise and power efficiency is effectively balanced. To facilitate such an active control, an emulated Miller Plateau tracking scheme is proposed to identify the critical di/dt and dv/dt instants, which are susceptible to load current and power input voltage conditions. These proposed techniques are incorporated in a GaN-based buck converter for verification.

Moreover, a continuous random spread-spectrum-modulation (C-RSSM) technique is utilized to scatter the EMI spectra evenly and continuously, attenuating the EMI further. For demonstration, the proposed C-RSSM scheme is applied to a GaN-based buck converter with peak current mode control. In the meantime, a one-cycle on-time rebalancing scheme is designed to overcome the crossover frequency limit existing in the conventional PWM control, thereby stabilizing the duty ratio under frequency modulation. Beneficially, the output jittering effect induced by RSSM is removed, balancing the trade-off between EMI and output regulation.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

This chapter gives a general introduction to the research background and major contributions of this dissertation. In more specific, Section 1.1 introduces the critical role of power electronics in modern industry and society. Section 1.2 describes the generic principle of switching power conversion for efficient energy delivery. Then, Section 1.3 traces the advances of power semiconductor devices, which are mainly accredited to device structure innovation and material revolution. This translates into continuous switching frequency elevation in power delivery systems. Based upon these discussions, Section 1.4 outlines the major challenges encountered in the next-generation power electronics from the perspectives of device- and circuit-level reliability, intense electromagnetic interference (EMI) noise and inherent power design trade-offs. Subsequently, Section 1.5 summarizes the research works devoted to overcoming the above challenges. It is followed by the organization of this dissertation in Section 1.6.

1.1 Power Electronics Impact

According to the data from the U.S. Energy Information Administration (EIA), up to 38% of the total amount of U.S. energy consumed in 2018 was transformed to electrical energy first and then transferred to the end-use applications [EIA-19]. Power electronics is the key enabling technology to control the electrical energy flow from source to load. In fact, since its advent around the mid-20th century [Brown-90, IBM-58, Paynter-62], power electronics has found a broad spectrum of applications in modern industry and society. By virtue of efficient power delivery, it enables power management to improve energy conservation in transportation, industrial systems and consumer electronics. Meanwhile, with the capability of controlling energy bidirectionally, it

is extensively utilized to feed the renewable energy sources into the main electricity grid. Further, power electronics also performs an essential role in saving energy and volume of military platforms and aerospace systems, such as radar, fighter jets and satellites, in which the space, weight and power are generally limited. Benefitting from the wide applications, the power electronics industry was valued at a global market size of USD 35 billion in 2017 [RAM-18]. Moreover, in the next decade, the power electronics market is expected to own a rapid growth in a compound annual growth rate (CAGR) of 7.1% [RAM-18]. This is mainly attributed to the large demand from electrical vehicles (EVs), which cater very well for the sustainable development with zero green-house gas emissions. In addition, the rapid developments of renewable energy sources, internet of things (IoTs) and the fifth-generation (5G) communication technique would also contribute greatly to the growing demands of power electronics.

1.2 Basic Principle of Efficient Power Conversion

Before 1960s, power electronics heavily relied on linear regulators for energy delivery. The linear regulators work in continuous mode to conduct the power flow between the energy source and load [Unitrode-86]. However, for regulation, they brutally dump the surplus energy from the source in the form of useless heat, therefore inducing considerable power losses. To overcome this drawback, switching network is involved to achieve efficient electrical energy delivery [Lutz-18], leading to the advent of switching power converters. Power switch, together with proper control scheme, is employed to control the electrical power flow. Specifically, when the power switch, which is virtually realized using semiconductor device, switches on, the energy is transferred from the source to the load. In addition to fulfill the power requirement by the load, the extra energy drawn from the source is stored temporarily in passive components such as

inductors and capacitors. After the power switch is turned off, the power flow from the energy source is thus terminated. In this case, the power requirement by the load is completely afforded by the stored energy in the passive components. The switching-on and -off behaviors of the power switch are managed properly via a control unit, such as to adaptively satisfy the power demand of the load. From the processing perspective, switching power converter breaks down the power flow out of the source into small power packets. Then, it transforms theses packets into continuous format for the load. Hence, switching power converter is also considered as power processor [Lutz-18]. By such a power processing means, the direct heat dissipation due to the power gradient between the source and load is eliminated. Therefore, switching power converters possess a notable advantage of high power conversion efficiency over the linear regulators, resulting in the prevalent utilizations.

Over the past fifty years, switching power conversion has experienced a great progress, steadily improving the main characteristics, including power efficiency, dynamic response and power density. In this period, the switching power circuits are dominated by silicon semiconductor. However, the silicon-based power systems are approaching the theoretical limit, inevitably slowing the rate of performance improvement. To circumvent such a fundamental crisis, wide band-gap (WBG) semiconductor is attracting great research interests and considered as a promising alternative to silicon [Lidow-15]. By virtue of its superior characteristics over silicon, WBG semiconductor is highly expected to enable the next-generation power electronics.

1.3 Evolution of Power Semiconductor Devices

Power semiconductor device performs an essential role in the power electronics, which implements the power switch to regulate the power flow in power converter. In fact, the power

semiconductor devices fundamentally define the physical limit of the switching power circuits. Basically, they are expected to act as ideal switches to control the power flow required by the loads without any power consumptions. It implies that the power switches should conduct the load currents in on-state with zero voltage drops, resulting in no conduction losses. During the off-state, they must block high voltages without any leakage currents. In addition, the ideal power switches are also able to change between conduction states instantaneously without any switching power losses. Unfortunately, the practical power devices, which have been serving in power electronics industry for well over five decades, still cannot be considered as ideal switches. While they dissipate negligible power during the off-state with very small leakage currents, the power devices produce conduction losses when conducting currents, because of their finite on-resistances. Also, they require finite time intervals to switch the states, introducing the switching power losses. In fact, the heat dissipations by power devices account for majority of power losses in power conversions. Improving the conversion efficiency markedly motivates great efforts on driving power devices towards ideal switches.

In order to measure the actual switching performance of a power device, a figure of merit (FOM) is commonly accepted, which is defined as the area-normalized specific on-resistance, denoted as R_{ON_SP} and expressed in unit of $m\Omega\text{-}cm^2$ [Baliga-19]. For any given design, R_{ON_SP} describes the inverse relationship between on-resistance and active transistor die area. A superior R_{ON_SP} indicates a lower on-resistance providing the same breakdown voltage and device area, leading to less conduction power loss and thus improving the overall switching performance. It is worthy to note that the ideal specific on-resistance, $R_{ON\_SP\_IDEAL}$, is determined fundamentally by the semiconductor material following the equation below [Baliga-19]:

$$R_{ON\_SP\_IDEAL} = \frac{4 \times V_{BR}^2}{\varepsilon_0 \times \varepsilon_r \times \mu_n \times E_C^3}. \quad (1.1)$$

Here, V_{BR} is the breakdown voltage. ε_0 and ε_r are the vacuum permittivity and relative permittivity, respectively. E_C is the critical electric field of the avalanche breakdown.

From a great extent, the advance of power devices can be accredited to the consistent efforts to reduce R_{ON_SP}, resulting in a well-known evolution roadmap in power device design [Baliga-88, Deboy-98, Williams-94]. Initially, the bipolar junction transistors (BJTs) were invented and then utilized as power switches in 1950s to supersede the vacuum tubes, starting the solid-state device era in power electronics. Since the mid-1970s, the power metal-oxide-semiconductor field-effect transistors (MOSFETs) developed rapidly and subsequently supplanted BJTs as the main-stream power switches. To meet the growing requirements from diverse applications, the FOMs of silicon power MOSFETs have been improved continuously. This mainly benefits from the innovations in device structures, such as double-diffused MOSFET (D-MOSFET), trench-gate double-diffused MOSFET (U-MOSFET) and super-junction MOSFET (SJ-MOSFET, or Cool-MOSFET).

After nearly five decades development, the silicon power transistors are asymptotically reaching the theoretical performance limits defined by Equation (1.1). Although the improvements are still undertaken due to the invention of super-junction devices, the rate has slowed down. With superior characteristics, gallium nitride (GaN) is considered as a suitable silicon successor for the next-generation power transistors. According to the comparisons among key electrical parameters between silicon and GaN [Lidow-15], as a wide band-gap semiconductor material, GaN has a three time higher band-gap (E_G) over silicon. As a result, GaN has at least one order of magnitude improvement in critical electric field (E_C). On the other hand, both silicon and GaN have similar

values for electron mobility and relative permittivity. Thus, according to Equation (1.1), the ideal specific on-resistance for GaN power transistors can be theoretically reduced by at least three orders of magnitude over the silicon counterparts. Such superior FOM has been notably driving the rapid developments in GaN-based power circuits.

1.3.1 Power Bipolar Junction Transistor (BJT)

Historically, bipolar junction transistor (BJT) is the first semiconductor device to be used as power switch. Take an NPN power BJT [Baliga-19]. Basically, it consists of two PN junctions in close proximity. Apart from the N^+ emitter and P-base region for the conventional bipolar structure [Streetman-06], the power BJT requires a lightly doped N-epitaxial layer to serve as drift region, allowing the transistor to block high voltage. When a positive voltage is imposed at the collector terminal, the PN junction across the based and collector terminals is reverse biased and sustains the high voltage. The voltage rating for the power BJT relies on the doping concentration and thickness of the N-epitaxial layer. In order to improve the breakdown voltage of the transistor, the N-epitaxial layer needs to be doped more lightly and produced thicker. On the other hand, this increases the on-resistance of the device. Such a compromise between breakdown voltage and on-resistance due to the drift region in power semiconductor devices is the origin to define R_{ON_SP} as the device FOM for performance comparison [Baliga-19].

The current conduction mechanism in power BJT relies on the transport of minority carriers. As the PN junction across the base and emitter terminals is forward biased, a number of electrons in the emitter are thus injected into the base region. These electrons, which are minority carriers for the P-type region, diffuse through the base area and arrive at the collector-base junction. When this PN junction is reversed biased, the electrons are thus swept rapidly by the electric field through

the depletion region, generating the collector current. In order to support the collector current, a certain amount of base current is required, implying that the power BJT is a current-controlled device. To accommodate this mechanism, a relatively complicated driver stage is required. In addition, the BJT changes from its on-state to off-state by reversing the bias applied across the base-emitter junction. As a minority carrier device, some charge is stored in the base region during the on-state. Moreover, a substantial amount of charge is also stored within the N-epitaxial region. To turning off the BJT switch, it requires to remove this charge, which prolongs the commutation time and thereby limits the switching frequency of power BJT [Baliga-19].

1.3.2 Vertical-channel MOSFET (V-MOSFET)

To address the shortcomings of bipolar power transistors, unipolar devices, such as metal-oxide-semiconductor field-effect transistors (MOSFETs), are highly desirable to be used as power switches. The first MOSFET was fabricated in 1960s for signal processing [Kahng-60]. However, its lateral structure is not feasible for power processing due to the low mobility of carriers on silicon surface. This situation changed in 1970s when vertical architecture was developed for the first time to handle high voltage and high current. This eventually leaded to the advent of the first power MOSFET, known as vertical-channel MOSFET (V-MOSFET) [Baliga-19, Salama-77]. Compared to BJTs, V-MOSFETs are voltage-controlled devices, simplifying the gate driver design [Heftman-05]. Moreover, they are majority carrier devices, facilitating the high-speed operations. As a result, they allow the power circuits to switch beyond 100kHz [Philips-91].

From the device physics perspective, the fabrication of the V-MOSFET involves a double diffusion process to define the N^+ source and P-body regions, followed by a V-groove etching to expose the gate area. The drain region locates at the opposite side of the device, forming the

vertical structure. In order to block high voltage, a lightly doped N-epitaxial layer is deposited to serve as the drain. The conduction channel can be induced at the surface of the P-body region beneath the gate oxide. Thus, the electrons can move from the source electrode to the drain one in a vertical direction. With less scattering effect, the carriers in the bulk have higher mobility than those on the surface, significantly lowering the specific on-resistance of the V-MOSFET and thus facilitating the efficient power processing.

Essentially, V-MOSFETs open the field of using unipolar semiconductor devices as the power switches. However, the manufacturing difficulties and instabilities in the structure seriously impeded their commercialization.

1.3.3 Double-diffused MOSFET (D-MOSFET)

To mitigate the fabrication and structure issues in V-MOSFET, the vertical double-diffused MOSFET (knows as D-MOSFET or VD-MOSFET) with planar structure was thus developed [Baliga-19, Lidow-79]. With superior performance and easy fabrication, it rapidly became commercially available in the mid-1970s. Similar to V-MOSFET, it is fabricated based upon a heavily doped N-type substrate for ohmic contact of drain terminal. Then, a lightly doped N-type epitaxial layer is grown as drain for high-voltage handling. The channel area is formed through double-diffused process of P-body and N^+ source regions. Subsequently, the gate is deposited over the channel region to control the device conduction. Compared to V-MOSFET, the D-MOSFET eliminates the requirement of 3-D fabrication process, improving the structure stability and reducing the device cost.

When the device gate is zero biased, D-MOSFET is able to block high drain-source voltage. In this case, the PN junction between the P-body and drain is reverse biased due to the positive

voltage applied at the drain. Since the dopant concentration in the N-epitaxial layer is lighter than in P-body region, the PN junction depletion region between them mainly spread into the thick N-epitaxial layer, increasing the punch-through breakdown voltage. When a positive bias is imposed on the gate, an inversion layer is formed in the P-body below the gate oxide, inducing a path for electrons transport from source to drain. Through the lateral channel, the electrons in the source region enter the upper surface of the N-epitaxial region. Then, they are transported vertically through the narrow region (known as JFET region) between the two P-body regions [Baliga-19]. Afterward, the electrons spread into the entire device width and arrive the drain terminal eventually, completing the current conduction. From the transport mechanism of electrons, the narrow JFET region in the D-MOSFET induces nonuniform current distribution within the drift region. This increases the internal resistance of the device, preventing the specific on-resistance from ideal limit.

1.3.4 Trench-gate Double-diffused MOSFET (U-MOSFET)

To overcome the structure limitation existing in D-MOSFET, the channel is highly desirable to be vertical for electron conduction from source to drain. To achieve this, trench-gate double-diffused MOSFET (also referred to as U-MOSFET) was developed in 1980s by leveraging the available technology for etching trenches in silicon [Baliga-19, Blanchard-88, Williams-96, Williams-17]. As same as in D-MOSFET fabrication, double diffusion process is applied for U-MOSFET to form the source and P-body regions. Then, a trench is etched from the upper surface of the device through the source and P-body regions into the N-epitaxial layer. The trench is subsequently oxidized to grow the gate oxide, followed by placing the gate electrode within it. By applying a positive bias at the gate, an inversion layer is induced at the surface of the P-body region along the vertical sidewalls of the trench gate. Through this path, the electrons in the source can

be transported into the drift region of N-epitaxial. Afterward, the electrons spread into the entire device width. Thus, the electrons are transported vertically, avoiding the narrow JFET region in D-MOSFET. By virtue of such conduction mechanism, the current distributes much more uniformly within the drift region. Thereby, it reduces the specific on-resistance and further improves the switching performance of the device towards the ideal limit.

1.3.5 Super-junction MOSFET (SJ-MOSFET)

As indicated earlier, a thick drift region of lightly doped N-epitaxial is required in order to support high voltage for both D-MOSFET and U-MOSFET. As a consequence, this region contributes significantly to the on-resistance of the power device. In order to alleviate this compromise and expand the performance limit of silicon power device, super-junction MOSFET (SJ-MOSFET, also known as Cool-MOSFET) is developed by using the principle of charge compensation [Baliga-10, Deboy-98, Lorenz-99, Williams-17]. According to the charge compensation principle, if a reversed biased PN junction is fully depleted before reaching the avalanche critical electrical field, then the doping concentration of the drift region can be improved without influencing the breakdown voltage [Williams-17]. This is significantly beneficial to reduce the specific on-resistances of silicon power devices.

As to the device structure, different from the D-MOSFET, deep trenches are fabricated into the N-type drift region. Afterward, these trenches are filled with P-type drift region to compensate the negative charges in N-epitaxial. When a zero voltage and a high positive voltage are respectively applied at the gate and drain, both the lateral PN junction between N-epitaxial and P-epitaxial, and the vertical PN junction between the P-epitaxial and N^+ drain contact are depleted. Thus, the drift region acts like the lightly doped region, capable of sustaining a high voltage. When

a positive voltage is applied at the gate, an inversion layer is formed in the P-body beneath the gate oxide, providing a channel for electron transport. Since the N-type drift region is higher doped compared to the D-MOSFET, the conduction on-resistance is thus reduced significantly.

1.3.6 Gallium Nitride High-electron Mobility Transistor (GaN HEMT)

Enhancement-mode GaN high-electron mobility transistor (HEMT) emerges in recent years due to its superior switching performance [Lidow-15]. The device starts with a silicon substrate. Then, an AlGaN buffer layer is utilized to create the transition from the substrate to the GaN crystal. This is the foundation on which the GaN transistor is built. Further, a thin AlGaN barrier layer is grown over the GaN crystal, generating a heterojunction between them. Finally, insulator and metallization layers are fabricated to complete the transistor structure. Because of the GaN piezoelectric property and strain at the heterojunction interface, a 2-dimensional electron gas (2DEG) layer is created underneath the AlGaN barrier layer. When a voltage is applied across the drain and source, the 2DEG is able to efficiently transport the electrons. The high concentration of electrons in 2DEG with very high mobility forms the ground for GaN HEMT.

1.4 Challenges in Designing GaN-based DC-DC Power Conversion System

As addressed in the previous section, the specific on-resistance of power devices reduces continuously. Lower specific on-resistance means that the power device needs smaller active area to retain the same on-resistance and breakdown voltage, resulting in less gate charge for the power device to switch. Therefore, from the design viewpoint, it eventually facilitates the switching frequency improvement in power circuits. Specifically, in the early days, the power converters were constructed using power BJTs. Due to large storage time of minority carriers in the base and drift region, they require long commutation transitions to change the conduction states, thereby

limiting the operation frequency at around tens of kHz [ADI-89]. Rather than BJTs, MOSFETs are majority carrier devices, facilitating the high-speed operations. As a result, they allow the power converters to switch beyond 100kHz [Philips-91]. Further, benefiting from the inventions of advanced power MOSFETs, such as D-MOSFET, U-MOSFET and SJ-MOSFET, the DC-DC converters are able to switch beyond 2MHz in recent years [TI-19]. Thanks to the emerging of GaN HEMTs, the switching frequencies in the DC-DC power converters are even improved to beyond 10MHz [TI-15]. Considering such a development just began less than a decade ago, it is widely believed that the GaN technology is inspiring a profound revolution in power electronics.

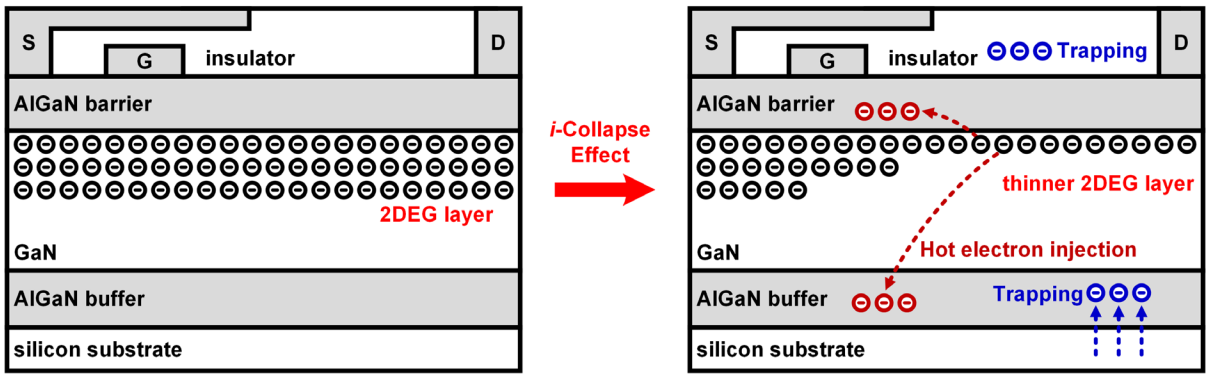
However, it is worthy to note that the GaN technology still faces severe challenges to navigate. First, the reliability issues significantly impede the industry-wide adoption of GaN technology. To control the power flow, power devices are subject to high-voltage, large-current and harsh thermomechanical stresses, making them the most prone to fail in a switching power system. According to an industrial survey, they account for over 34% of power system failures on average [Oh-15]. As an emerging technology, GaN HEMT suffers an even worse situation due to the unique device structure and operation mechanisms. The reliability concern on GaN technology is also attracting significant attentions from the industry. Supported by main-stream semiconductor companies, the JC-70 committee for WBG semiconductor in Joint Electron Device Engineering Council (JEDEC) released the first GaN reliability standard JEP173 in January 2019, specifying the dynamic on-resistance measurement for GaN HEMT to assess the current-collapse effect properly [JEDEC-19]. Overall, to address the GaN reliability challenges demands significant efforts from both academia and industry.

Second, as address earlier, the power flow at the source side is broken down into small

packets for efficient energy exchange. However, the discontinuous power flow induces discontinuous current or voltage, generating abundant harmonics and hence electromagnetic interference (EMI) noise. As the switching frequencies are improved significantly, the GaN-based power circuits suffer from much more severe EMI emissions. It is well known that EMI noise could induce malfunctions in electronic systems, from the annoying cell phone interference to lethal failure of life support equipment in the hospital. In order to ensure that the EMI source will not cause harmful interference to other devices operating within its expected operating environment, several EMI standards are imposed to regulate the permissible levels of conducted and radiated EMI emissions generated by an end product [CISPR-16, IEC-15, FCC-19, Regan-04, Hegarty-18]. Any single frequency violating such limits would fail the compliance tests of the products. Thus, EMI is an increasingly significant and challenging topic for GaN-based power converters. Traditionally, the EMI performance is evaluated after the chip design has been accomplished and the PCB has been fabricated. When the compliance test fails, larger EMI filter is added to repeat the evaluation process. Such an iterative strategy is quite time consuming and would significantly delay the time to market of the product. Thus, it is highly desirable to solve the EMI issue at the source with active control means.

At last but not the least, the inherent power design trade-offs pose more challenges on the implementations of high-frequency and high-performance GaN-based power circuits. For example, in order to reduce the EMI emissions, slew rate control is commonly utilized to slow down the switching transitions. However, this would induce more power loss, creating a design trade-off between EMI and power efficiency. It is necessary to balance such compromises to achieve high-performance power conversion.

1.4.1 Device- and Circuit-level Reliability Issues



(a) (b)

Figure 1.1. Device-level aging mechanism in GaN power switches: (a) healthy state and (b) *i*-collapse effect due to hot electron injection and charge trapping.

While GaN device aging and failure mechanisms are not as well-studied as silicon counterpart, its unique structure and operation also induce new aging and failure problems. As shown in Figure 1.1(a), because of the GaN piezoelectric property and strain at the heterojunction interface between GaN region and AlGaN barrier layer, a 2-dimensional electron gas (2DEG) layer is created underneath the AlGaN barrier layer. By virtue of high electron mobility and concentration, the 2DEG layer is highly conductive, contributing to low device on-resistance. This attribute offers valuable potentials for GaN-based switching power converters to operate at much higher switching frequencies than conventional silicon counterparts, while retaining comparable if not better efficiency. However, caused by the unique structure, the GaN HEMTs suffer from a major aging mechanism of *i*-collapse effect, which originates from the hot electron injection during the switching transitions and charge trapping in the off states as shown in Figure 1.1(b). Consequently, the free carrier density in the 2DEG layer reduces and hence the dynamic on-resistance r_{DS_ON} increases. Such an increased r_{DS_ON} generates higher conduction loss in the GaN HEMT, deteriorating the thermal condition and potentially causing the device to fail prematurely

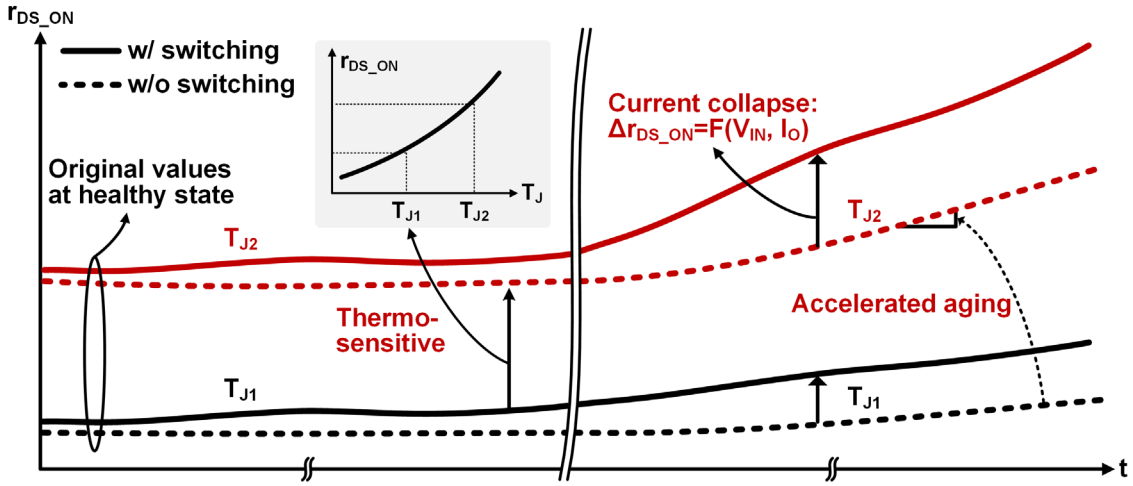


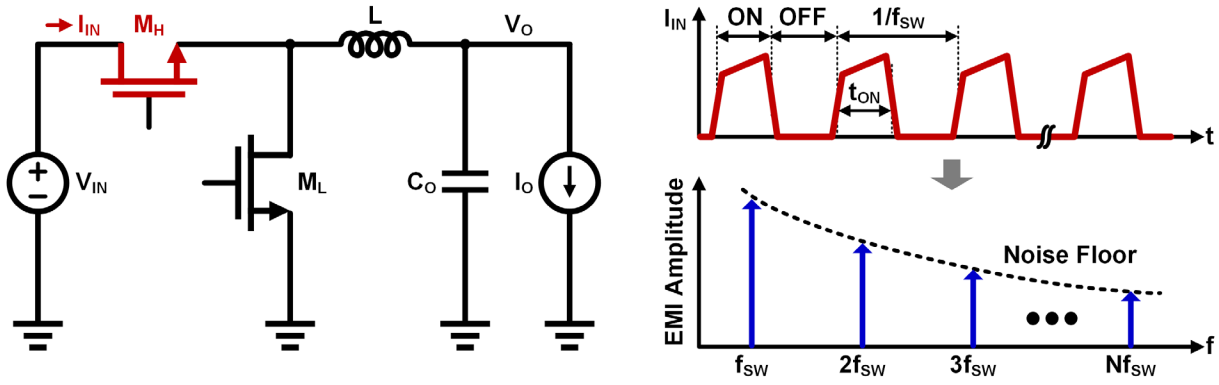
Figure 1.2. Dependence of dynamic on-resistance r_{DS_ON} on switching conditions and junction temperature T_J.

[Bahl-16]. To improve the GaN HEMT reliability, it is of critical importance to monitor the *i*-collapse effect by taking r_{DS_ON} as the aging precursor. Unfortunately, r_{DS_ON} of GaN HEMT varies along with the specific switching conditions, such as the switching frequency, input voltage and load current. Such switching-condition dependence of r_{DS_ON} precludes the use of conventional offline condition monitoring approaches for GaN HEMT because the switching conditions between offline and online can be significantly different. Moreover, as shown in Figure 1.2, r_{DS_ON} is sensitive to the junction temperature T_J, requiring real-time T_J determination for temperature effect calibration for monitoring accuracy consideration. However, this is quite challenging for discrete GaN power devices.

Apart from the *i*-collapse effect, another GaN reliability issue stems from the fact of deteriorated positive thermal feedback loop, which unintentionally accelerates the GaN aging procedure. As illustrated in Figure 1.1(a), to achieve an economy-efficient solution, the power GaN HEMTs are usually manufactured on low-cost silicon substrate. To smooth the lattice transition between the substrate and GaN active region, an AlGaN buffer layer is deposited

between them. However, such a device structure makes the heat dissipation more difficult, leading to higher junction temperature T_J. As T_J rises, r_{DS_ON} increases as illustrated in Figure 1.2, generating more heat to elevate T_J further. According to Arrhenius' Law [Paine-15], as T_J increases, the device lifetime reduces exponentially. Therefore, it is favorable to improve the GaN longevity through active approaches.

1.4.2 Intense Electromagnetic Interference (EMI) Noise Emissions



(a) (b)

Figure 1.3. Illustration of EMI issue: (a) DC-DC buck converter and (b) conducted EMI noise due to switching actions.

By virtue of switching operations, the switching power circuits gain markedly superior power efficiencies over the linear regulators, making them prevalent in a variety of applications [Unitrode-86]. Consider a synchronous DC-DC buck converter as shown in Figure 1.3(a). It converts an unregulated DC input V_{IN} to a lower but regulated DC output V_O, regardless of the variations of load current I_O. To accomplish such a step-down conversion, the two power transistors, M_H and M_L, are controlled to switch on and off complementarily at a predetermined frequency f_{SW}. When M_H switches on, V_{IN} is connected to the input of the LC filter consisting of an inductor L and a capacitor C_O, imposing a positive voltage drop across the inductor. Thus, the inductor current rises to store the energy. After a certain duty cycle, M_H is turned off while M_L is

turned on synchronously, applying a nearly zero voltage to the input of the LC filter. As a result, the inductor current decreases. Thus, its stored energy is transferred to the load. Through such a repetitive switching, a periodic rectangular waveform is generated at the switching node. As its pulse width can be modulated by controlling the duty cycle of M_H, the average and thereby the output V_O can be precisely regulated. Acting as power switches, M_H and M_L work in deep linear regions when they are conducting, sustaining very low voltage drops. They are otherwise completely non-conducting only except for short commutation transitions. Beneficially, the power dissipations in the converter are suppressed effectively, gaining a high conversion efficiency.

On the other side, however, frequent switching actions unintentionally incur severe EMI noise in the power stage, causing a major downside for switching power circuits. As shown in Figure 1.3(b), when it is turned on to conduct the induct current, M_H draws a large inrush current I_{IN} from the input line. While the duty cycle t_{ON} expires, M_H switches off, resulting in a steep current decline. Such rapid changes of the input current contribute directly to conducted EMI noise [Blank-15, Meng-06, Musumeci-97]. As the EMI level elevates in interested frequency bands, circuit reliability for both signal and power processing deteriorates substantially, inducing potential malfunction to the system. To decrease the conducted noise and thus fulfill the regulatory standards, EMI filters consisting of inductors and capacitors are commonly deployed at the input sides of switching power circuits [Majid-12]. However, such a bulky solution increases the overall system volume and hence limits the power density. Moreover, it could also degrade the transient response of the converter and even cause stability problem to regulation loop [Zhang-19].

For even worse, the significantly improved switching frequencies in GaN-based power circuits present more challenges for dealing with EMI issues, which can be explained from three

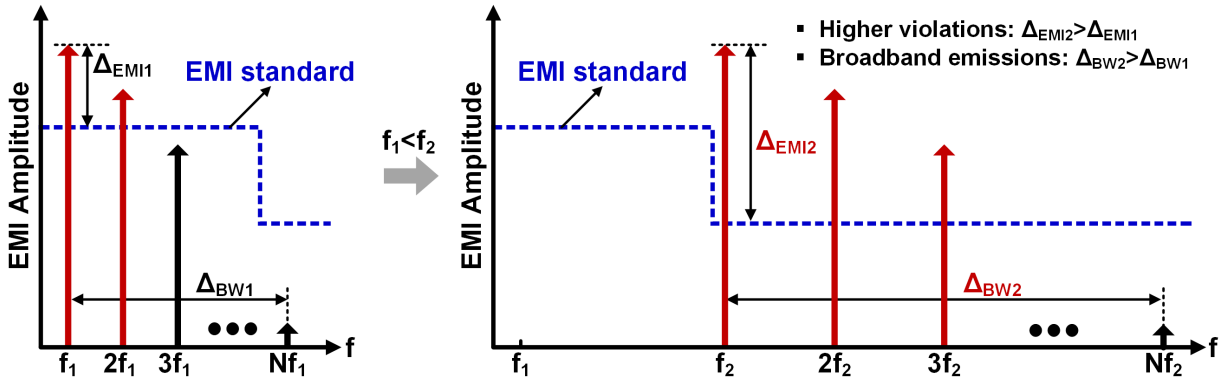


Figure 1.4. EMI spectra comparison under (a) low switching frequency and (b) high switching frequency in switching power circuits.

aspects by using Figure 1.4. First, with faster switching speed, the positions of EMI spurs are shifted up to higher frequencies. Because the total energy at the fundamental frequency and each harmonic does not change, thus the EMI spectrum at each specific harmonic remains the same amplitude, regardless of the switching frequency [Carson-22]. However, the emission limits imposed by the EMI standards are generally more restrictive at higher frequencies [TI-18]. As a result, more efforts are needed for EMI reduction to meet the requirements. Second, high switching frequency results in broadband EMI noise, demanding a relative wider noise suppression range for the EMI filter. Unfortunately, as a dilemma, the EMI filter based on LC network has a narrower functional bandwidth along with the increased frequency [Murata-19]. Consequently, as the noise frequencies are elevated, it is more challenging to tackle the EMI issue by solely using filtering means. At last, from the application perspective, more and more functional modules are assembled on board or even packed together with the switching power circuits for economic considerations. When it is produced at higher frequencies, the EMI noise would be more easily transmitted into the sensitive modules through parasitic passives, causing severe interference problems. Hence, due

to these ensuing issues, the EMI emission has become a tremendous hindrance in developing high-frequency GaN power circuits.

1.4.3 Inherent Power Design Trade-offs

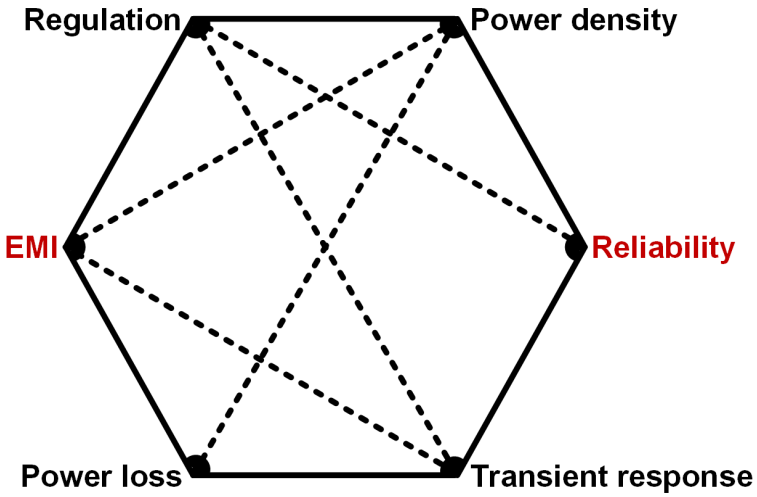


Figure 1.5. Power design hexagon.

From the design aspect, the switching power circuits entail a multidimensional design space, which is depicted in the "power design hexagon" of Figure 1.5. In addition to the EMI emission and reliability, another four properties in a power system are of great interest as well, including the output regulation, power loss, load transient response and power density. These essential parameters usually trade with each other, presenting more challenges on the design of high-performance GaN-based switching power circuits.

As addressed earlier, rapid switching actions deteriorate the EMI performance of GaN power systems. With the capability of smoothing the steep edges of the input surge currents, slew rate controls prove effective to reduce the peak EMI noise [Musumeci-97]. Unfortunately, they inevitably prolong the switching transitions and thus generates more switching power loss, implying a design trade-off between EMI and conversion efficiency. To achieve an optimum

design for the EMI-efficiency trade-off, active slew rate controls are in urgent demand, which are able to shape the commutation transitions based on switching timings, realizing a targeted EMI reduction with minimum power efficiency cost. Tradition approaches commonly rely on comparators for timing detections [Musumeci-97, Wang-14]. However, the long delay times prevent them from utilizations in high-frequency GaN-based power circuits.

In addition to slew rate controls, spread-spectrum-modulation techniques are also widely employed to attenuate the EMI noise [Gonzalez-07, Ho-10, Ke-17, Tao-11, Tse-02, Yang-18]. By varying the switching frequency along with time, they are capable of spreading the EMI spectra into lower levels. However, when the switching frequency changes, the converter needs finite time to reach a new equilibrium state. Limited by the loop bandwidth which is usually constrained at fifth to tenth of the switching frequency, the loop response lags far behind the frequency modulation speed. It is equivalent that the converter continuously experiences transient events, resulting in jittering effect at the output [Tao-11, Yang-18]. These observations reveal a trade-off between EMI and output regulation. Fundamentally, the classical control schemes, such as pulse-width-modulation (PWM) and pulse-frequency-modulation (PFM) controls, are incapable of alleviating this trade-off because they are all built upon a basic assumption that at a specific steady state, the converter always switches at a certain constant frequency. Hence, to accommodate the frequency modulations and thereby mitigate the design trade-off between the EMI and output regulation trade-off, innovations in control schemes are required.

As discussed in the previous section, condition monitoring is imperative to improve the GaN reliability. To serve on this purpose, it is necessary to sense some critical device parameters, such as voltage drop and conducting current, to determine the aging precursor. Conventional

detections usually require unintentional interruptions on the normal switching operations of the converters, thereby influencing the regulation functions. In addition, to enhance the system reliability through control, reducing the operation speed is generally utilized to decrease the heat generation and hence the thermal stress. Apparently, this counters the initial purpose of improving the switching frequency, thus degrading the load transient response and power density. To deal with these reliability relevant trade-offs, non-intrusive detections are highly desirable. Also, active thermal management, which takes both the thermal condition and power conditions into account, is a necessity.

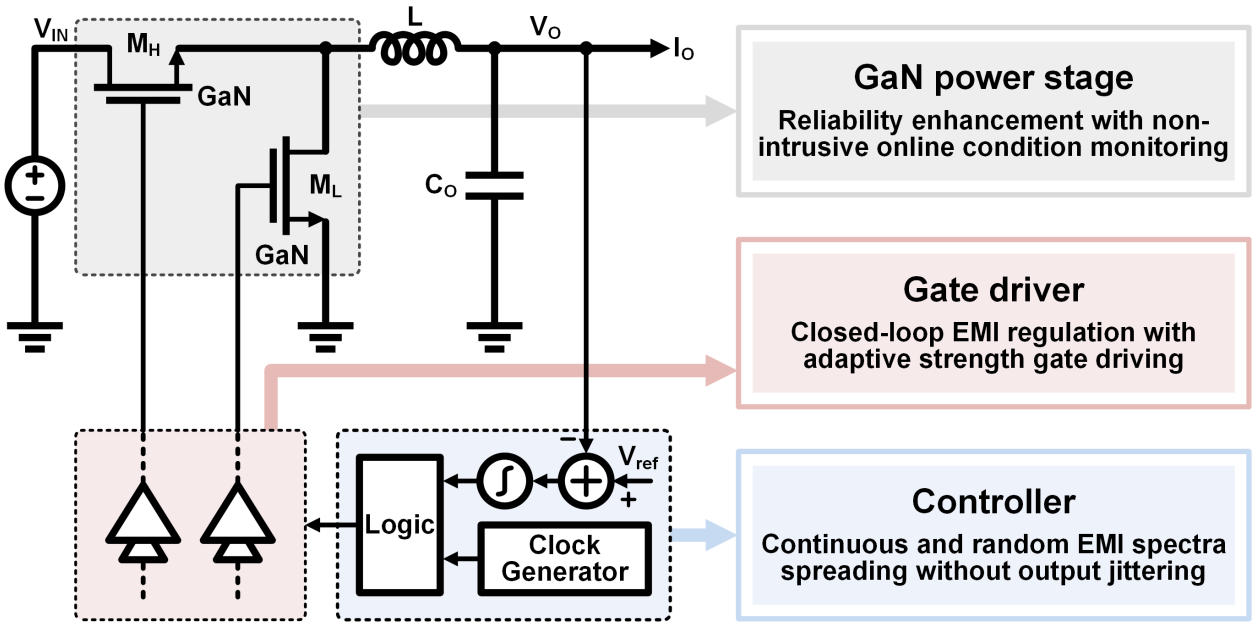


Figure 1.6. Summary of research contributions.

1.5 Research Goals and Contributions

The major research object of this study is to overcome the aforementioned challenges in terms of reliability, EMI and trade-offs for designing high-frequency and high-performance GaN-based DC-DC power converters. Specifically, as shown in Figure 1.6, technical innovations are

respectively conducted in power stage, gate driving and control scheme to improve the system reliability and suppress the EMI noise emissions. In the meantime, the relevant design trade-offs are comprehensively optimized, minimizing the influences on the system performance. The key contributions of this study are described as follows:

(1) Reliability Enhancement with Non-intrusive Online Condition Monitoring

(1.1) Developed an online condition monitoring scheme to prognose the *i*-collapse effect of GaN power switch, improving the power-stage reliability. To reach this goal, the dynamic on-resistance of the GaN device is sensed online as the aging precursor because its change directly relates to the *i*-collapse effect. Specifically, both the drain-source voltage and drain current of GaN device are detected simultaneously when the power device is conducting. Then, they are delivered to a divider for dynamic on-resistance computing. In addition, for the accuracy concern, the temperature effect on the dynamic on-resistance is calibrated further, which is enabled by an instant GaN device junction temperature sensing. As such a temperature-independent aging precursor increases beyond a predefined threshold, the aging event is triggered to terminate the switching of the power converter, protecting the entire system from a potential catastrophic failure [Chen-19a].

(1.2) Developed a gate-leakage-inspired, cross-die junction temperature sensing technique to facilitate the temperature effect calibration on the aging precursor, significantly suppressing the false monitoring rate. To acquire the junction temperature of the discrete GaN power switch, the gate leakage, which does not depend on aging effect, is identified as the feasible thermal-sensitive electrical parameter. To achieve a non-intrusive sensing, a dynamic detection is developed by floating the device gate for a short time and then

recording the gate-source voltage drop due to the gate leakage. Accordingly, the device junction temperature is extracted. Further, the aging precursor, namely the dynamic on-resistance, is thus calibrated to achieve a junction-temperature-independent online condition monitoring, improving the monitoring accuracy by 19 times [Chen-19a].

(1.3) Developed a proactive temperature frequency scaling scheme to slow down the aging process whenever possible, hence enhancing the circuit longevity. The online condition monitoring and sensed junction temperature information facilitate the design of a proactive measure of circuit longevity improvement. In order to balance the reliability and power regulation performance, the operation speed and thus heat generation of the converter is modulated jointly by performance parameters (e.g. load current, transient speed and efficiency) and junction temperature. Specifically, at a low level of junction temperature, the converter is regulated by the feedback regulation loop and optimized for the system performance. When the junction temperature rises beyond a predefined threshold, active thermal management is activated to reduce the thermal stress. To achieve optimal operation between performance and thermal aging, instant load condition is monitored. When the load current changes, the high performance mode is enabled, minimizing the transient delay and voltage damping. The measurements prove that the junction temperature of the GaN power switch is suppressed by 16˚C with a typical GaN thermal resistance of 82˚C/W, lowering the risk of aging greatly. By enabling the high-performance mode, load current step-up and -down transient responses are improved by 50% and 70% respectively, achieving optimal system performance [Chen-19a].

(2) Closed-loop EMI Regulation with Adaptive Strength Gate Driving

(2.1) Developed an adaptive strength gate driving scheme for GaN power devices to attain a balanced design trade-off between EMI noise and power efficiency. Rather than the conventional implementation with a fixed driving ability, the proposed design adjusts the gate driving strength adaptively. At the initial stage, the proposed gate driver applies a low driving strength to slow down the input current change (di/dt), reducing the conducted EMI noise mainly caused by di/dt. Once the di/dt transition terminates at the Miller Plateau starting point, the proposed gate driver enhances the driving strength significantly to speed up the drain-source voltage slew rate (dv/dt), avoiding extra switching power loss overhead. With such an independent control of low di/dt and high dv/dt, the EMI-efficiency trade-off is effectively optimized. The measurements demonstrate that the proposed gate driving strategy reduces the EMI noise by 19dBμV in Band B (<30MHz) and over 9dBμV in Band C/D (from 30MHz to 3GHz), trading with only 2.44% of power efficiency [Chen-17].

(2.2) Developed an emulated Miller Plateau tracking scheme to sense the Miller Plateau voltage of the power switches in one switching cycle, regardless of the instant load current and input voltage. The adaptive strength gate driving control necessitates the detection of the Miller Plateau starting point. However, the GaN power switch has an extremely short Miller Plateau duration in several nanoseconds. In addition, the Miller Plateau voltage varies along with the load current and input voltage. These factors pose serious challenges on the conventional Miller Plateau sensing approaches, which suffer from either long delay time or low accuracy. To overcome these issues, it is discovered that in a buck converter, the Miller Plateau voltage of the high-side GaN switch can be emulated the same as the

gate-drain voltage of the low-side one during the dead time. Moreover, the same I-V characteristic of both devices eliminates the dependence of Miller Plateau voltage on the electrical parameters. Based on these discoveries, the emulated Miller Plateau tracking scheme is thus invented by sensing the switching node through appropriate timing control. To improve the accuracy further, two compensations are employed to calibrate the errors due to GaN device structure and channel length modulation effect, respectively [Chen-17].

(2.3) Developed a closed-loop driving control scheme to command the operation of the adaptive strength gate driver. Due to the high frequency switching in GaN-based converter, open-loop control generally suffers from delay issue. To mitigate this, closed-loop regulation is developed in this design, precisely synchronizing the driving strength enhancement and the Miller Plateau starting point in each switching cycle. To achieve this, the emulated Miller Plateau voltage is used as a dynamic reference. In the meantime, the high-side gate-source voltage is sampled at the instant when the driving strength is enhanced. The sample voltage is then applied as a feedback signal. By regulating the feedback signal to equal the reference, the instant of enhancing the driving strength is exactly allocated at the Miller Plateau starting point, facilitating the control of low di/dt and high dv/dt. To accurately implement such a closed-loop regulation, a noise-isolated feedback link is designed to avoid the switching noise interference between the high-voltage domain and low-voltage domain. The basic idea is to sample the feedback voltage in high-voltage domain during the high-side switching-on transition. In this period, the two domains are isolated to avoid noise interference. When the low-side switch is turned on, the feedback voltage is transferred into the control domain. In this way, the regulation accuracy is guaranteed [Chen-17].

(3) Continuous and Random EMI Spectra Spreading without Output Jittering

(3.1) Developed a continuous random spread-spectrum modulation scheme to scatter the EMI spectra almost uniformly, thereby attenuating the EMI noise effectively. To serve on this purpose, a Markov-chain-based random clock generator is designed on the ground of a chaotic piecewise-linear one-dimensional map. Since the chaotic map is characterized by two linear equations, the clock generator can be implemented with standard analog blocks, simplifying the circuits design and improving the robustness. By generating a random-distributed switching frequency in analog domain, it overcomes the finite frequency resolution issue existing in the digital counterpart. Moreover, based on the mathematical analysis, the frequency variation range can be conveniently tuned by designing the electrical parameters, thereby removing the necessity of periodic signal processing required in thermal-noise-based random clock generator. The design is incorporated in a GaN-based buck converter operating at a nominal frequency of 8.3MHz. With a frequency modulation range of ±10%, the EMI measurements show that the peak EMI is reduced from 66dBμV to 35dBμV at the fundamental frequency and from 62dBμV to 27dBμV at the third-order harmonic [Chen-19b, Chen-19c].

(3.2) Developed a one-cycle on-time rebalancing scheme to eliminate the output jittering effect due to the frequency modulation, hence balancing the design trade-off between EMI and output regulation. To conquer the bandwidth limitation without influencing the loop stability in the conventional pulse-width-modulation (PWM) control, the one-cycle on-time rebalancing scheme senses the instant switching frequency. In the meantime, through time-to-voltage conversion, it extracts the duty-ratio determined by the feedback loop.

Based on the acquired information, the proposed design recalculates and thus modulates the on-time instantly, remaining a constant duty-ratio even though the switching frequency varies randomly from cycle to cycle. Thereby, the output jittering effect is removed without compromising the EMI spectra spreading. Compared to the conventional PWM control, the proposed design suppresses the amplitude of the output jittering from 240mV to below 10mV [Chen-19b, Chen-19c].

(3.3) Developed a high-speed capacitive-coupled current sensor for peak current mode control, taking the advantages of fast load transient response and simplified compensation network over the voltage mode control. In the implementation, the direct-current resistor (DCR) current sensing strategy is adopted. Then, a differential capacitive-coupled sensing stage is employed to capture the voltage drop across the DCR of the inductor. Subsequently, a source-follower-based amplifier is connected to convert the sensed voltage into a single-ended output, featuring high-speed operation and hence facilitating a 20ns minimum on time of the converter. Moreover, by virtue of dynamic capacitive-coupled sensing, the common-mode input of the sensor is independent on the output of the converter, thereby supporting a wide output range from 1.2V to 5.0V [Chen-19c].

1.6 Dissertation Organization

The remainder of the dissertation is organized as follows. Chapter 2 discusses solutions to improve the GaN reliability. To illustrate the severe reliability challenges facing the GaN technology, *i*-collapse effect is explained from the perspectives of device structure and switching operations of GaN power devices. As a major cause of GaN aging, *i*-collapse effect needs to be monitored for reliable operation. However, as it heavily depends on the switching conditions, such

as input voltage, load current and switching frequency, online condition monitoring is mandatary, posing challenges on accurate precursor measurement without interfering the voltage regulation. In addition, because of relatively high thermal resistance of GaN power device, the positive thermal-aging procedure is intensified, requiring active measures to prolong the device lifetime. In view of these issues, an online condition monitoring is designed by sensing dynamic on-resistance of GaN switch as the aging precursor, thereby prognosing the GaN health condition properly. In the meantime, to achieve a reliable monitoring, the junction temperature of GaN switch is determined instantly for temperature effect calibration on the dynamic on-resistance. Thus, the false monitoring rate is effectively suppressed. Further, a proactive temperature frequency scaling scheme is proposed to reduce the thermal stress of the GaN switch, while minimizing the compromise to the system performance. By integrating these modules, a high-reliability GaN-based buck converter is designed using a 0.18-μm high-voltage CMOS process, which is verified by measurements.

Chapter 3 presents technical strategies to reduce peak conducted EMI noise while with minimum power efficiency overhead in GaN-based switching power converter. To gain an insight into the classic design trade-off between EMI and power loss, the switching behaviors of high-side power switch in buck converter is analyzed in detail. Based on the analysis, several concrete design challenges are illustrated, including the instant Miller Plateau detection, intensified EMI-efficiency compromise due to high frequency operation, and smart gate driving for active switching transition shaping. To mitigate these challenges, two key techniques are then proposed. Among them, a novel emulated Miller Plateau tracking scheme is developed for cycle-by-cycle sensing of the Miller Plateau voltage, despite of load current and input voltage. The basic principle behind this technique

is to replicate the Miller Plateau voltage by sensing the switching node during the current freewheeling period, which is successfully implemented with a low-power negative voltage sensor. Further, using the emulated Miller Plateau voltage as a dynamic reference, an adaptive strength gate driving scheme is developed to implement the independent control of low di/dt and high dv/dt to optimize the EMI-efficiency trade-off. In the actual design, a noise-isolated feedback link is developed based on timing control to generate a clean feedback signal immune from the switching noise. These techniques are incorporated in a 10MHz GaN-based buck converter that is fabricated in a 0.35-μm BCD process for demonstration.

Chapter 4 focuses on the application of spread-spectrum-modulation (SSM) techniques in switching power converters, aiming to mitigate the EMI issue further. According to Carson's rule, the energy carried by a signal remains the same despite the frequency modulation. This forms the theoretical basis of SSM techniques. Rather than fixing the operation speed, the SSM scheme modulates the switching frequency within a certain band. As a result, the EMI spectra are spread into lower levels. Although they have been widely adopted in power electronics, the conventional SSM approaches have to bear limited EMI attenuation capabilities. In more specific, periodic SSM is incapable of spreading the EMI spectra uniformly, and digital random SSM suffers from finite frequency resolution issue. On the other hand, due to the constantly frequency change, the duty ratio of the power converter varies from cycle to cycle, inducing low-frequency output ripples with considerable amplitudes. To overcome these performance limitations, two schemes are proposed. First, an analog random SSM scheme is designed using a Markov-chain-based random clock generator, spreading the EMI spectra continuously and nearly uniformly. As the benefit, it accomplishes a comparable EMI reduction but using a much narrower frequency dithering range

than its digital counterpart, cutting down the silicon area significantly. Second, a one-cycle on-time rebalancing scheme is introduced to replace the classical PWM control. By detecting the instant switching frequency and duty ratio, it adjusts the on-time dynamically to stabilize the output even with frequency modulation. To validate the design principles, a GaN-based buck converter with peak current mode control is implemented in a 0.18-μm high-voltage CMOS process. Then, the measurements are taken to verify the performance in terms of EMI and output regulation.

Finally, Chapter 5 concludes this dissertation, followed by the discussions of the future research directions.

CHAPTER 2

GAN RELIABILITY IMPROVEMENT USING ONLINE CONDITION MONITORING AND PROACTIVE TEMPERATURE FREQUENCY SCALING*

Due to its unique structure and operation, the GaN HEMT suffers from current-collapse (or *i*-collapse) effect, which depends on the specific switching conditions. To avoid catastrophic failure, it is necessary to monitor the *i*-collapse caused device aging. Moreover, to prolong the device lifetime, it is highly desirable to reach an active thermal management without influencing the system performance. In this chapter, Section 2.1 reviews the design challenges of online condition monitoring, including the aging precursor measurement and temperature effect calibration. The accelerated thermal-aging procedure of GaN HEMT is also discussed in this section. Section 2.2 discusses the requirements of aging precursor selection. Then, the proposed online condition monitoring scheme is introduced, followed by the circuit implementation. In order to remove the temperature effect on the aging precursor, a gate leakage current inspired junction temperature sensor is designed, which is elaborated in Section 2.3. Further, to enhance the circuits longevity, a proactive temperature frequency scaling scheme is presented in Section 2.4, followed by the experimental results in Section 2.5.

2.1 Design Challenges in GaN Reliability Improvement

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) have much lower specific on-resistance than silicon power MOSFETs, because of superior characteristics of GaN

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semiconductor over silicon [Baliga-13]. Beneficially, they enable the switching power circuits to operate efficiently at much higher frequencies [Chen-17, Guz-18], thereby promising some notable advantages such as fast dynamic response and system miniaturization. However, the commercialization of GaN technology is still hindered seriously by reliability issues [Bahl-16]. In order to control energy flow from source to load, the power devices must sustain high-voltage, large-current and harsh-thermomechanical stresses due to the frequent switching actions, making them the most vulnerable components in power systems. Based on industrial survey, the power devices are responsible for around 34% of power system failures on average [Oh-15]. The situation is even worse for GaN HEMTs. While GaN device aging and failure mechanisms are not as well-studied as silicon counterpart, its unique structure and operation also induce new aging and failure problems. Use GaN switch M_H in a buck converter of Figure 2.1 as an example. As a high-side switch, it faces large-switching-current and high-input-voltage stress in each charge phase. After repetitive switching actions, a number of electron carriers in the channel can be injected into the AlGaN barrier and buffer layers, known as hot electron injection. In discharge phase, M_H is off, but the low-side switch M_L becomes conductive and shorts the source of M_H to ground, creating high drain-source voltage (V_{DS}) stress on M_H. This induces charge traps in the insulator and buffer layers, known as charge trapping. As a joint effect of both mechanisms, trapped or injected electrons in the insulator, AlGaN barrier and buffer layers repel the free electrons in the channel when M_H is on, weakening the 2-dimensional electron gas (2DEG) layer at the heterojunction interface between GaN region and AlGaN barrier layer. This effect, known as current collapse or *i*-collapse for short, degrades the channel conductivity, increases the dynamic on-resistance r_{DS_ON}, and is a major cause of GaN switch aging and failure [Bahl-16]. To prognose the course of *i*-

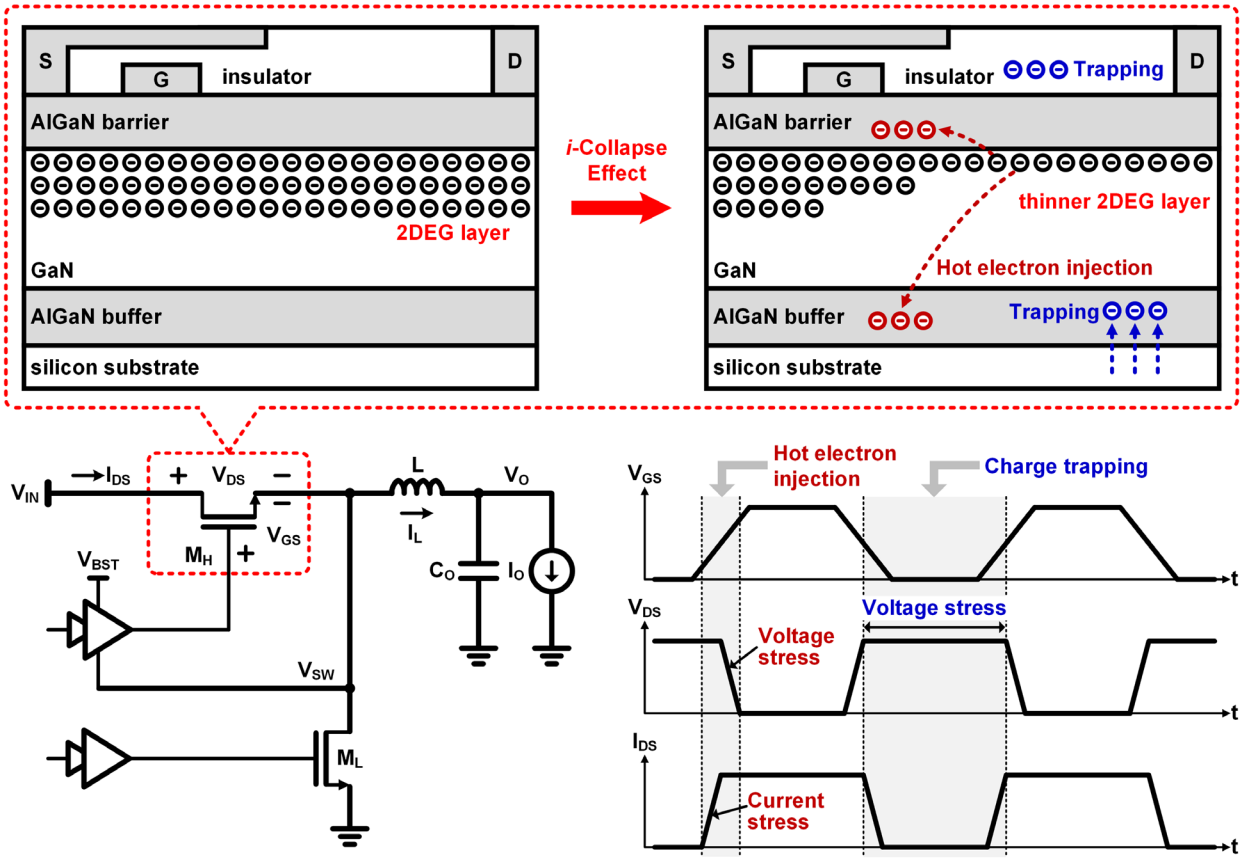


Figure 2.1. Device- and circuit-level *i*-collapse aging mechanisms in GaN power switches.

collapse caused device failure, it is of crucial importance to monitor the condition of GaN switch. For this, r_{DS_ON} is highly desirable as the precursor, because its change is directly related to *i*-collapse effect. A similar but simplified approach was reported in [Smet-11] using collector-emitter voltage V_{CE} as the actual precursor for IGBTs. However, it is only feasible for a fixed and small current and thus can only be accomplished offline, inconveniently requiring frequent interruption on operation. This can be very inaccurate and impractical since operation conditions between offline and online can largely differ, leading to high false monitoring rate (FMR). Hence, online condition monitoring is highly preferable. A design in [Dusmez-16] reported an in-situ condition monitoring by observing pole variation in loop gain for power MOSFETs. However, the

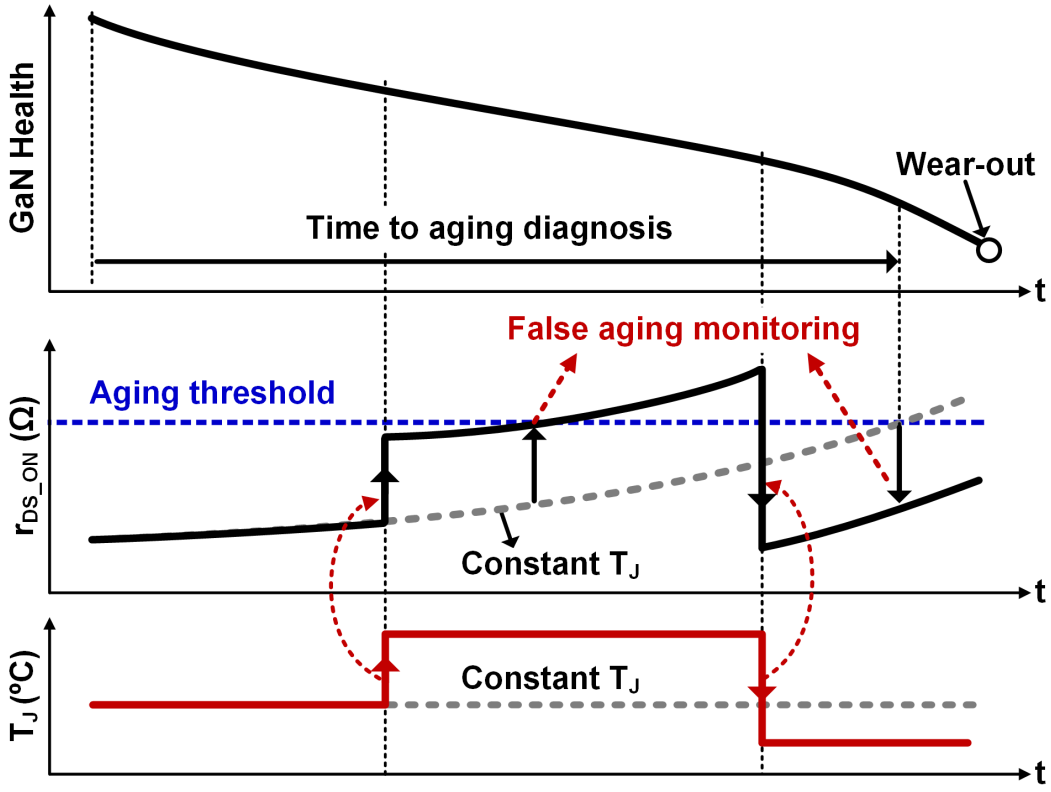


Figure 2.2. False aging monitoring induced by temperature fluctuations.

implementation of pole location precursor is highly sophisticated and noise-sensitive, resulting in high FMR. An alternative approach was reported in [Pu-19] based on switching transient measurement for SiC MOSFET. Unfortunately, it requires designated period for precursor measurement, which counters the initial purpose of online monitoring.

In addition, the aging precursors are generally sensitive to junction temperature T_J of power switch, presenting another challenge on GaN device failure prognosis. As the ambient temperature T_A varies, T_J fluctuates accordingly. Furthermore, the power switch dissipates power losses when conducting load current I_O for power delivery, inducing self-heating effect on the power switch itself. Thus, T_J also depends on I_O. As shown in Figure 2.2, when T_J rises due to T_A or I_O increasing, the aging precursor r_{DS_ON} shifts to higher level, even the aging condition of the power switch

remains the same. Consequently, r_{DS_ON} might surpass the predefined aging threshold even though the power switch still works healthily. This would trigger the aging alert by false, practically shortening the service lifetime of the power switch. On the other hand, as T_J reduces due to T_A or I_O decreasing, r_{DS_ON} jumps to a lower level. In this scenario, it remains below the aging threshold even though the power switch's condition has degraded significantly. Such an overlooked aging alert would eventually result in a catastrophic failure to the entire system. Apparently, to avoid these false aging monitoring events, online T_J effect calibration has to be accomplished in GaN condition monitoring. However, conventional temperature sensing circuits such as PTAT are not applicable in this scenario, because most GaN switches are not monolithically integrated on a silicon where the controller and other sensing blocks are built. Hence, the chip temperature fundamentally differs from T_J of GaN switch. To overcome this, the on-resistance is detected in [Dusmez-16] to determine the T_J for power MOSFET. Unfortunately, the on-resistance also relies on the aging condition, leading to accuracy degradation of this method along with time. Thereby, a new T_J sensing approach is in urgent demand for GaN switch, which should be aging independent and feasible for on-chip implementation.

Apart from the *i*-collapse effect, another aging cause of GaN switch is thermal effect, which is usually evaluated by T_J. To reduce manufacture cost and improve technology compatibility, it is common to fabricate GaN HEMTs on silicon substrate. However, it is difficult to directly deposit GaN crystal on silicon because of their lattice mismatch and thermal expansion coefficient difference [Lidow-15]. Accordingly, an AlGaN buffer layer is often inserted as shown in Figure 2.1. Unfortunately, this increases the junction-to-ambient thermal resistance $R_{\theta JA}$. Besides, GaN HEMT can attain a comparable conduction capability with smaller device size compared with the

silicon power MOSFET. This feature benefits the reduction of device gate charge, hence facilitating the switching frequency improvement. The downside is that smaller device size results in higher $R_{\theta JA}$. Furthermore, GaN semiconductor has lower thermal conductivity than silicon [Lidow-15], also contributing to $R_{\theta JA}$ elevation. As a result, the relatively high $R_{\theta JA}$, together with the increased r_{DS_ON} due to *i*-collapse effect, causes higher power and heat generation in GaN HEMT, elevating T_J. According to Arrhenius' Law, as T_J increases, the mean time to failure (MTTF) drops exponentially [Paine-15]. For even worse, the elevated T_J deteriorates the *i*-collapse effect with even higher r_{DS_ON}, significantly reducing the device lifetime. This makes the thermal management essential in GaN-based power system. It is achieved in [Wang-10] by adjusting the power distribution among parallel-connected converters. Although it is able to minimize the thermal stress placed on the system as a whole, this solution heavily relies on a pre-built electrothermal model, requiring extra hardware resources for complicated computations. In [Prasobhu-18], a smart gate driver is utilized to control the switching power loss through modulating the switching transitions. However, the control is sensitive to device parameters such as threshold voltage and output capacitance, which are hard to measure accurately. In [Broeck-19], an active thermal control is realized by adapting the switching frequency to T_J. Higher T_J leads to lower frequency, suppressing the thermal stress. One of the shortcomings existing in this approach is that T_J is determined indirectly by sensing power losses, sacrificing the resolution. Another one is that it inevitably compromises the system performance such as dynamic response. In view of these issues, it is highly desirable to develop an active thermal management methodology to improve the GaN longevity with high robustness while minimizing the influence on the system characteristics.

2.2 Dynamic On-resistance-based Online Condition Monitoring

In order to prognose the *i*-collapse caused failure in GaN HEMTs, it is necessary to sense the dynamic on-resistance r_{DS_ON} online as the aging precursor. Moreover, junction temperature-independent condition monitoring is in highly desirable to achieve high accuracy.

2.2.1 Aging Precursor Discussions

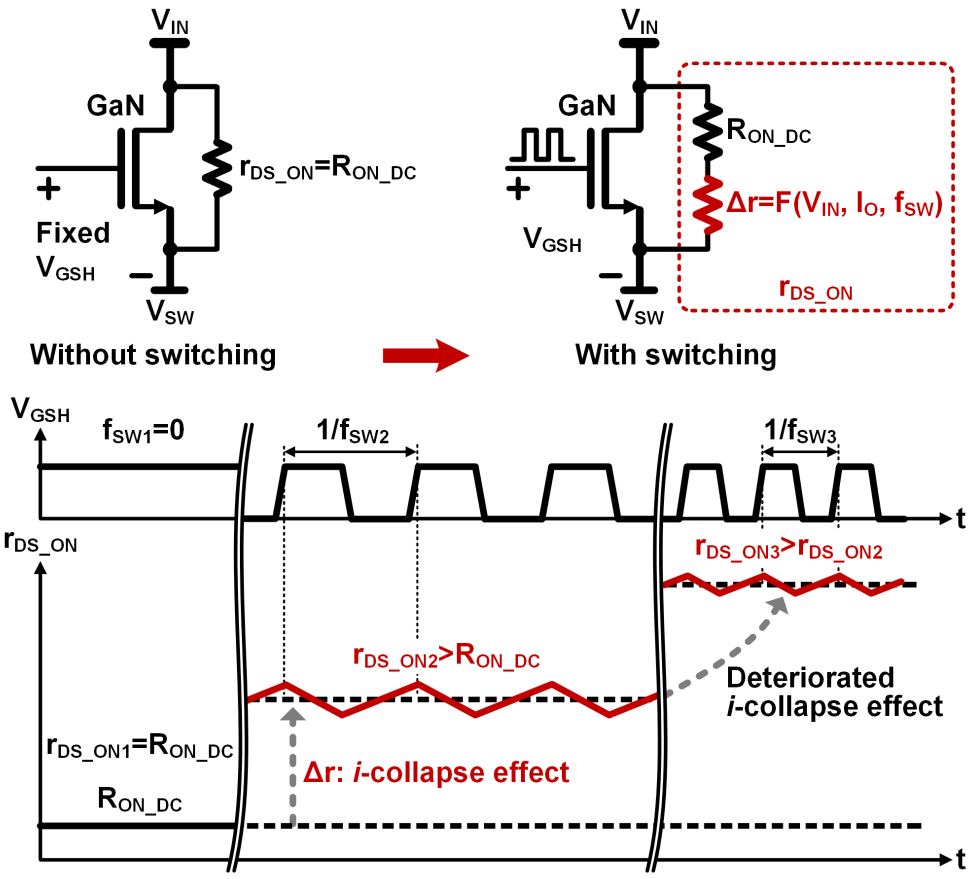


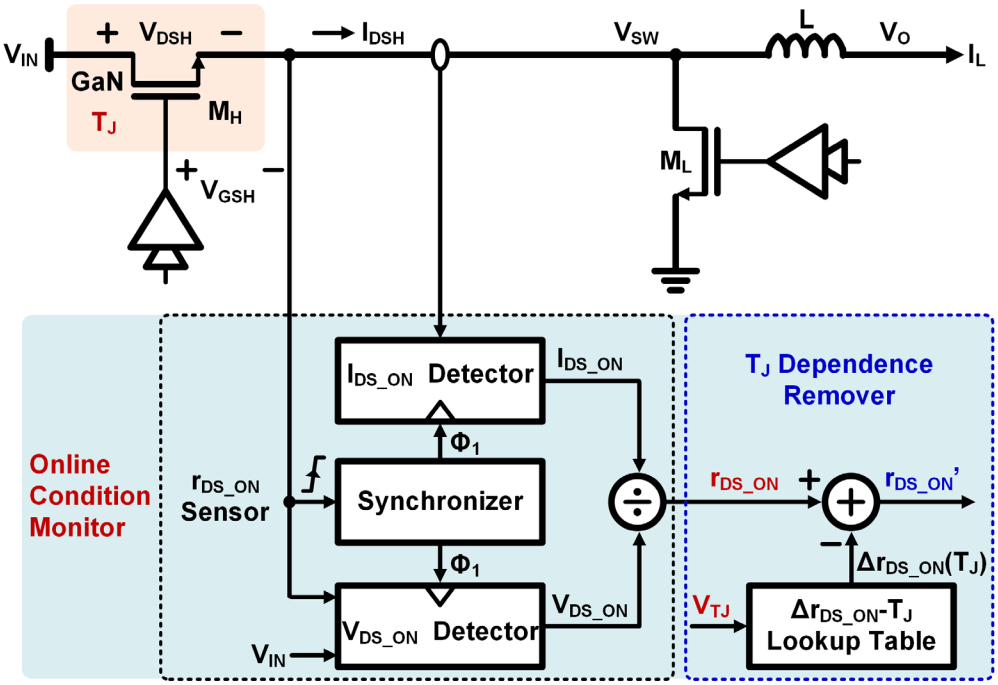
Figure 2.3. Dependence of dynamic on-resistance on specific switching conditions.

Basically, an electrical parameter is feasible to serve as the aging precursor if it changes monolithically along with the device degradation procedure. Moreover, its change needs to be gradual before the wear-out state. Satisfying these requirements, the dynamic on-resistance r_{DS_ON} of GaN switch is a suitable candidate for *i*-collapse caused device failure prognosis. In addition to

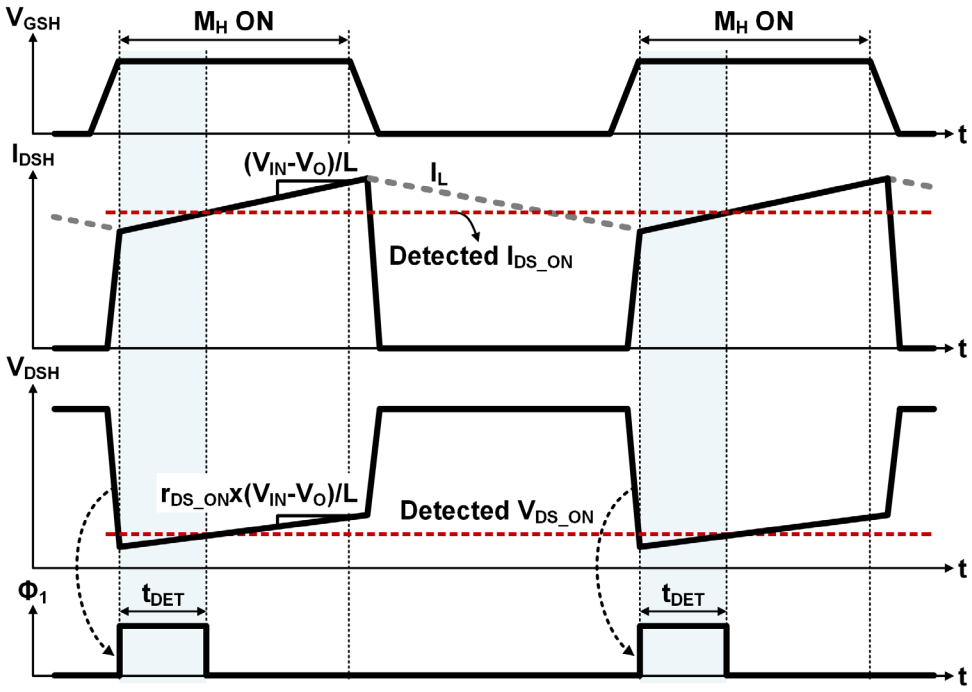
these perspectives, the measurement of r_{DS_ON} also requires special considerations because r_{DS_ON} not only relates to the device property but also depends on the switching conditions of the power circuits. As shown in Figure 2.3, when it conducts current constantly without any switching actions, namely the switching frequency f_{SW1}=0, the GaN switch are not exposed to either high-voltage or large-current stress. As a result, it does not experience *i*-collapse effect, with a dynamic on-resistance r_{DS_ON1} identical to the static one R_{ON_DC}. While it starts to switch at a non-zero frequency f_{SW2}, the GaN switch has to endure high-voltage and large-current stresses, resulting in *i*-collapse effect as explained earlier. Hence it induces a higher r_{DS_ON} than R_{ON_DC}. Higher V_{IN} and larger I_O intensify the *i*-collapse effect, elevating r_{DS_ON}. Furthermore, when the switching frequency rises ($f_{SW3}>f_{SW2}$), the number of commutation transitions increase proportionally in a given time interval. Consequently, the *i*-collapse effect is deteriorated accordingly [Cai-17, Cappello-18, Hwang-13, Li-19]. As a result, r_{DS_ON} shifts to an even higher level ($r_{DS\_ON3}>r_{DS\_ON2}$). In view of these discussions, r_{DS_ON} is a strong function of the switching conditions, including V_{IN}, I_O and f_{SW}. For the same GaN switch, the health level varies largely if the switching conditions change. Thus, in order to properly assess the device status, it becomes mandatory to measure r_{DS_ON} in real time under the actual operation scenario.

2.2.2 Design Aspects

Figure 2.4(a) shows the block diagram of the proposed online condition monitor to prognose the *i*-collapse caused failure of GaN switch. To sense the precursor r_{DS_ON} online, both the instant high-side on-voltage V_{DS_ON} and on-current I_{DS_ON} are measured using respective detector circuits. As shown in the timing diagram in Figure 2.4(b), after M_H switches on, the input voltage V_{IN} is imposed at the switching node V_{SW}. As a result, the high-side current I_{DSH}, which is



(a)



(b)

Figure 2.4. Proposed r_{DS_ON}-based online condition monitor. (a) Circuit block diagram and (b) timing diagram.

identical to the inductor current I_L during this phase, ramps up with a slope of $(V_{IN}-V_O)/L$. Correspondingly, the high-side drain-source voltage V_{DSH} increases with a slew rate of $r_{DS\_ON}\times(V_{IN}-V_O)/L$. Because both V_{DSH} and I_{DSH} are not constant during the on phase of M_H, V_{DSH} and I_{DSH} must be measured simultaneously in order to determine r_{DS_ON} precisely. For this, a time synchronizer is designed to synchronize the two detectors. As to the timing in Figure 2.4(b), when V_{SW} is charged rapidly from nearly ground to a high voltage due to M_H switching on, the synchronizer captures such quick rising edge of V_{SW}, setting the enable signal Φ_1 to activate the detections of V_{DSH} and I_{DSH}. After a time interval t_{DET}, Φ_1 switches to low, terminating the detection phase. At this instant, both V_{DSH} and I_{DSH} are sampled and hold as V_{DS_ON} and I_{DS_ON}, respectively. They are then fed into a divider for computing r_{DS_ON} further. Meanwhile, as the fluctuation of T_J causes large variations on r_{DS_ON}, its influence must be removed. To accomplish this, T_J of M_H is sensed and translated into a voltage signal V_{TJ} by an on-chip T_J sensor, which would be addressed in the next section. Accepting V_{TJ} as the input and using a lookup table, the T_J effect remover in Figure 2.4(a) determines the r_{DS_ON} variation, $\Delta r_{DS\_ON}(T_J)$, induced by T_J changing with respective to a reference temperature (e.g. 25°C). This $\Delta r_{DS\_ON}(T_J)$ is then subtracted from the sensed r_{DS_ON}, thereby acquiring a T_J-independent aging precursor, denoted as r_{DS_ON}'. This allows the T_J-independent online condition monitoring and significantly improves the prognosis accuracy.

Figure 2.5 details the circuit implementation of r_{DS_ON} sensor. To implement the I_{DS_ON} detection, a direct current resistance (DCR) current sensor is utilized. To replicate the voltage drop across the direct-current resistance R_{DCR} of the inductor L, a RC filter consisting of R_F and C_F is deployed in parallel with L. By designing the time constant $R_F\times C_F$ to be equal to L/R_{DCR}, the

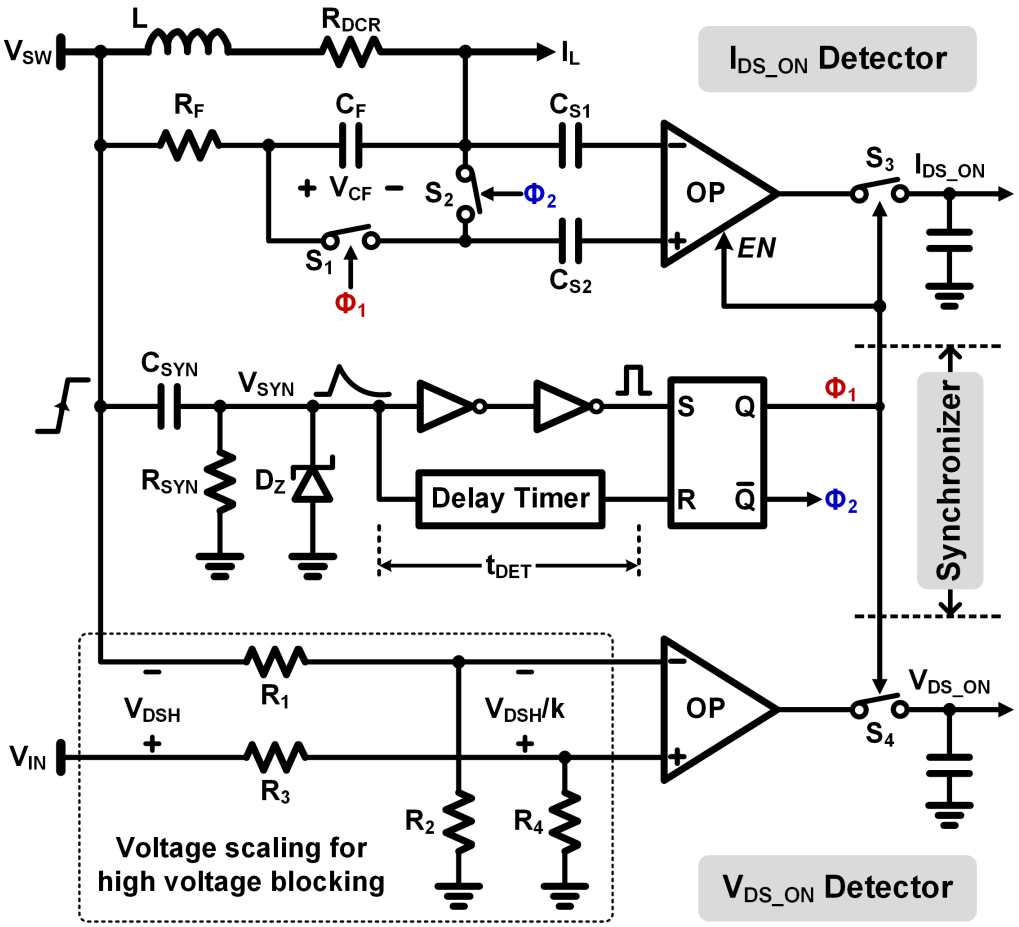


Figure 2.5. Schematic of dynamic on-resistance r_{DS_ON} sensor.

voltage difference V_{CF} between C_F exactly emulates that between R_{DCR}, which is proportional to I_{DSH} during the on phase of M_H. Further, to capture V_{CF}, a capacitive-coupled sensing stage is designed using two capacitors, C_{S1} and C_{S2}, together with two switches, S_1 and S_2 [Herzer-09]. During the sensing period, the switch S_1 is connected while S_2 is disconnected. The voltage rising of V_{CF} due to I_L increasing is ac-coupled by C_{S1} and C_{S2} to the inputs of an operational amplifier. At the end of the detection, the output of the amplifier is sampled and hold as I_{DS_ON} by controlling the switch S_3. For V_{DS_ON} detection, both V_{IN} and V_{SW} are scaled down to block the high voltage from the sensing circuits. The scaled voltage, V_{DSH}/k, is further amplified and sampled as V_{DS_ON}

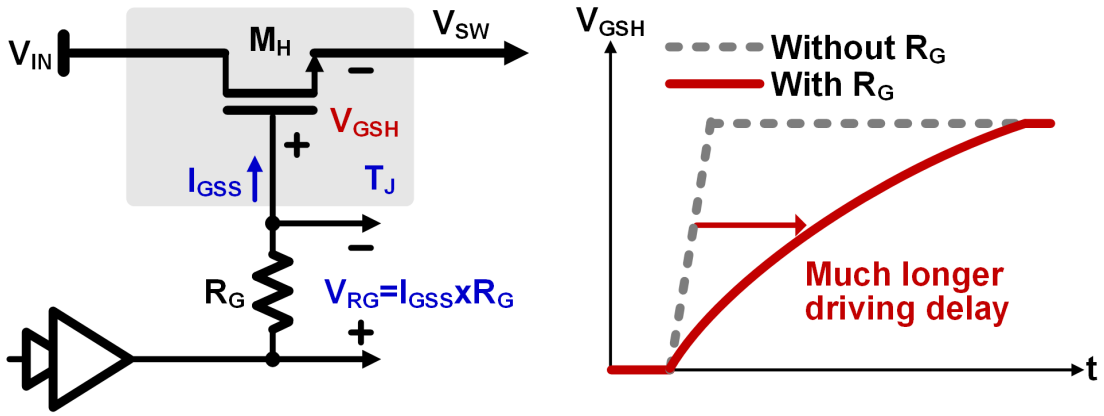
using the switch S_4. To synchronize these two detections, the synchronizer is designed by employing a capacitor C_{SYN} to sense the sharp rising edge of V_{SW} during the switching-on transition of M_H. Accordingly, the detection signal Φ_1 is set to high through an SR latch. In the meantime, a delay timer is initialized. After the timer expires, Φ_1 is reset to terminate the detection phase. In such a way, I_{DS_ON} and V_{DS_ON} are ensured to be detected at the same instant. In the synchronizer, a Zener diode D_Z is connected to clamp the voltage range of the node V_{SYN}.

2.3 Gate Leakage Inspired Junction Temperature Sensing

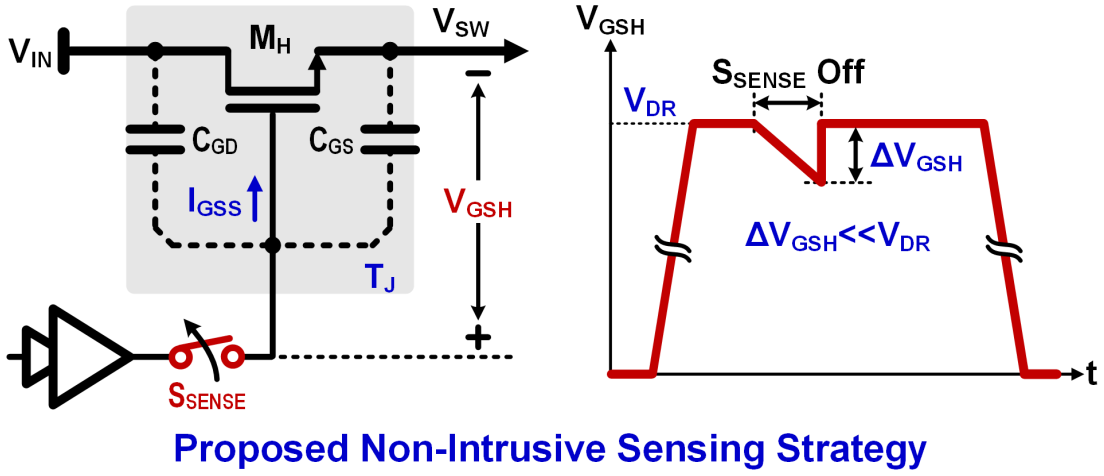
As addressed earlier, the aging precursor r_{DS_ON} is sensitive to the junction temperature, which would degrade the condition monitoring accuracy. To eliminate this issue, the sensing for junction temperature is needed to calibrate the temperature effect on r_{DS_ON}. For this, a gate leakage I_{GSS}-inspired, aging-independent, cross-die junction temperature sensor is designed.

2.3.1 Design Principle

As addressed earlier, because GaN HEMTs are commonly discrete power devices, it is challenging to determine the device junction temperature T_J remotely. To overcome this issue, a cross-die sensing approach is proposed by detecting the GaN gate leakage current I_{GSS}. Device physics study proves that I_{GSS} is temperature sensitive and aging independent [Poze-19, Xu-18], which becomes a perfect sensing parameter in this scenario. Furthermore, as I_{GSS} can be accurately measured on board level [Roschatt-15], T_J of a GaN switch is thus successfully obtained regardless of its placement to the die. As shown in Figure 2.6(a), a straightforward way to sense I_{GSS} of GaN switch M_H is using a series resistor R_G which is connected in series with the gate driving path. The voltage difference across R_G, namely V_{RG} that is proportional to I_{GSS}, can be sensed to extract the T_J information. However, to level shift V_{RG} in a reasonable range for accuracy consideration, a



(a)



(b)

Figure 2.6. Comparison between (a) conventional gate resistor-based I_{GSS} sensing and (b) proposed non-intrusive I_{GSS} sensing.

large R_G is required. For example, with a typical I_{GSS} at the order of 0.1mA [Poze-19, Roschatt-15, Xu-18], a minimum 100Ω is required for R_G to ensure V_{RG} higher than 10mV. This unintentionally enlarges the gate driving delay, thereby limiting the minimum on-time and consuming more switching power loss. To mitigate these, a non-intrusive sensing methodology is proposed as shown in Figure 2.6(b). Compared to a regular gate driver, only one sensing switch

S_{SENSE} is added. During the switching-on transition of M_H, S_{SENSE} is connected without degrading the driving capability. After V_{GSH} stabilizes at the final drive voltage V_{DR}, S_{SENSE} is disconnected. In such case, the gate capacitance consisting of C_{GS} and C_{GD} is discharged by I_{GSS}, creating a voltage drop on V_{GSH}, denoted as ΔV_{GSH}. As the sensing time t_{SENSE} expires, S_{SENSE} is connected to recover V_{GSH}. Hence, the voltage drop ΔV_{GSH} can be calculated as:

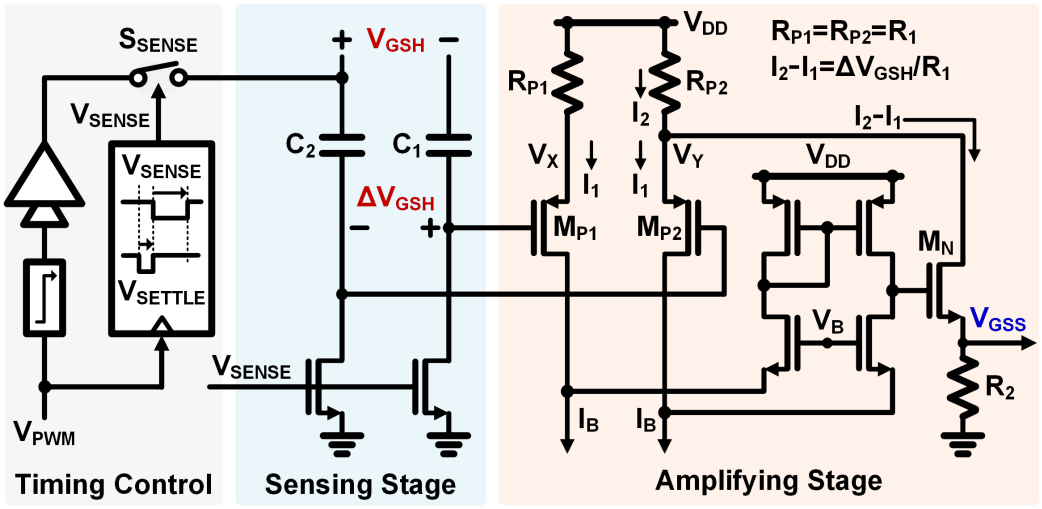
$$\Delta V_{GSH} = I_{GSS} \times t_{SENSE} \times (C_{GS} + C_{GD}). \quad (2.1)$$

Based on Equation (2.1), I_{GSS} can be determined to identify T_J. In the implementation, t_{SENSE} can be controlled such that ΔV_{GSH} is much lower than V_{DR}, minimizing the impact on gate driving.

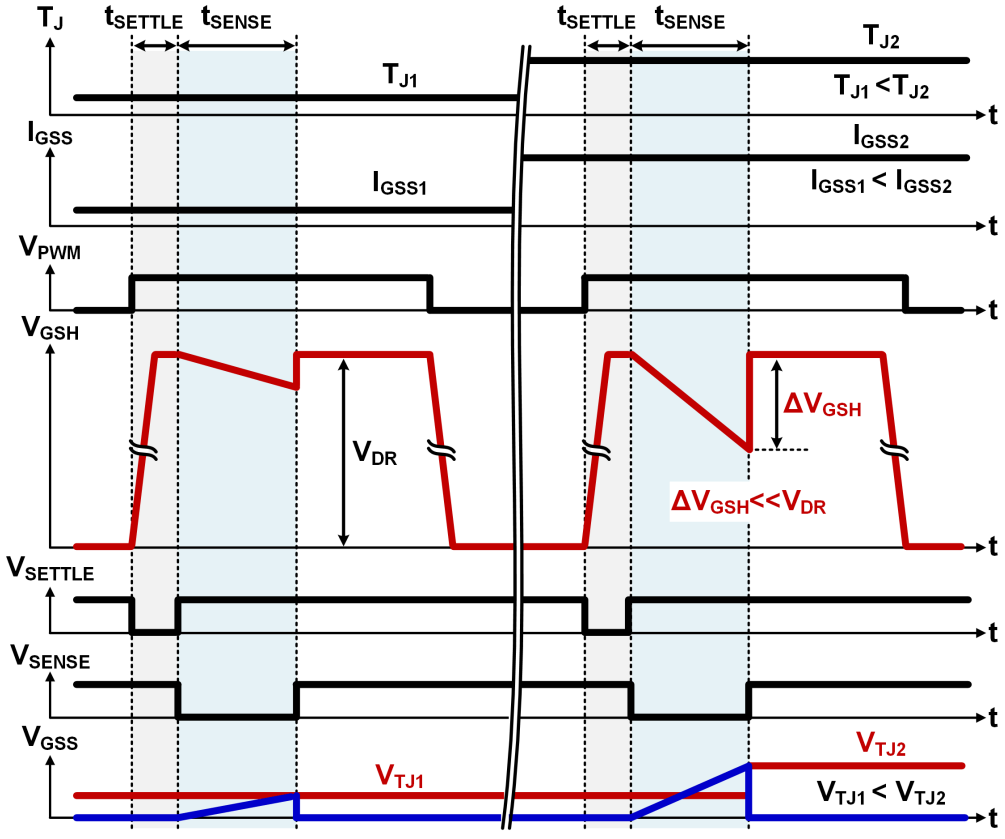
2.3.2 Circuit Implementation

Figure 2.7(a) shows the circuit implementation of the proposed I_{GSS}-inspired, cross-die T_J sensor. It consists of a timing control stage, a sensing stage and an amplifying stage. As for the operation, as shown in the timing diagram of Figure 2.7(b), at the beginning of each charge phase, the feedback control signal V_{PWM} triggers the gate driver to turn on M_H, which also turns on the sensing timer. After a time of t_{SETTLE}, the timer turns off the switch S_{SENSE} to initialize I_{GSS} sensing. At this instant, the gate of M_H is disconnected from the buffer driver. Because of I_{GSS}, its gate capacitor C_G (=C_{GS}+C_{GD}) is discharged at a rate of I_{GSS}/C_G, causing the gate voltage drop of ΔV_{GSH}. Due to the ac-couple of two capacitors (C_1 and C_2) in the sensing stage, ΔV_{GSH} is delivered to the differential input pair of the amplifying stage, M_{P1} and M_{P2}. Note that M_{P1} and M_{P2} perform as source followers. In addition, the cascode current mirror ensures that the currents conducted by M_{P1} and M_{P2} are equal, both denoted as I_1. Hence, M_{P1} and M_{P2} have identical gate-source voltage. Thus, the difference between V_X and V_Y exactly follows ΔV_{GSH}, leading to the equation below:

$$V_X - V_Y = \Delta V_{GSH}. \quad (2.2)$$



(a)



(b)

Figure 2.7. Proposed gate leakage I_{GSS}-inspired junction temperature sensing. (a) schematic and (b) timing diagram.

Furthermore, the current I_1 conducted by M_{P1} is induced by the voltage difference across the resistance R_{P1} (=R_1), resulting in the equation as below:

$$I_1 = \frac{V_{DD} - V_X}{R_1}. \tag{2.3}$$

The current I_2 in the right branch is induced by the voltage difference imposed on R_{P2} (=R_1):

$$I_2 = \frac{V_{DD} - V_Y}{R_1}. \tag{2.4}$$

As V_Y is lower than V_X, then I_2 is larger than I_1. Because M_{P1} and M_{P2} are forced to conduct the same current I_1, the excess current at the node V_Y, which equals (I_2-I_1), is redirected to the output transistor M_N for balance. Such output current is derived by combing (2.2), (2.3) and (2.4) as below:

$$I_2 - I_1 = \frac{V_X - V_Y}{R_1} = \frac{\Delta V_{GSH}}{R_1}. \tag{2.5}$$

Equation (2.5) indicates that the amplifying stage realizes the operation of voltage subtraction through the voltage-to-current conversion. The output current further flows through a resistance R_2, generating the output voltage V_{GSS}:

$$V_{GSS} = \frac{R_2}{R_1} \times \Delta V_{GSH}. \tag{2.6}$$

At the end of the sensing period t_{SENSE}, V_{GSS} is sampled as the eventual signal V_{TJ}. By inserting (2.1) into (2.6), the relation between V_{TJ} and I_{GSS} is acquired as:

$$V_{TJ} = \frac{R_2}{R_1} \times t_{SENSE} \times (C_{GS} + C_{GD}) \times I_{GSS}. \tag{2.7}$$

From (2.7), V_{TJ} is proportional to I_{GSS}. Hence, it carries the T_J information of M_H, suitable for temperature effect remove on the aging precursor r_{DS_ON} as illustrated in Figure 2.4. After the sensing period, the switch S_{SENSE} is connected to recover the regular gate driving. As shown in the

waveforms, since the sensing is cycle-by-cycle, the T_J change could be detected in real time for temperature effect calibration on r_{DS_ON}, sustaining the T_J-independent online condition monitoring regardless of the switching conditions and ambient temperature.

2.4 Longevity Enhanced GaN Power System

In order to mitigate the intensified positive thermal-aging feedback existing in GaN power switch, a proactive temperature frequency scaling scheme is proposed to reduce the GaN thermal stress. At the same time, the power conditions are also sensed to minimize the influence on the system performance. Both the online condition monitoring and temperature frequency scaling are integrated into a GaN-based buck converter, improving the reliability of power conversion.

2.4.1 Proactive Temperature Frequency Scaling

The proposed online condition monitoring and T_J sensing facilitate the design of a proactive measure of device longevity improvement through a temperature frequency scaling scheme. Figure 2.8 depicts the circuit implementation of the temperature frequency scaling engine, which is built around a switching frequency f_{SW} modulator. The operation principle is illustrated in Figure 2.9. The basic idea is to modulate the operation speed and thus heat generation of the converter according to the performance parameters (e.g. load current, transient speed and efficiency) and T_J. In more specific, at low level of T_J, the aging stress is the least significant. In this scenario, the converter switches at the highest frequency, suppressing the output ripple and facilitating the fast dynamic response. When T_J rises beyond a predefined threshold T_{SCL}, the output of the comparator CMP1 flips low, setting the mode signal V_{LE} to high. Thus, the switch S_{LE} is turned on to enable the longevity enhancement (LE) mode. Under this mode, the voltage-controlled modulation current I_{MOD} is connected to tune the clock charge current I_{CLK} in the f_{SW}

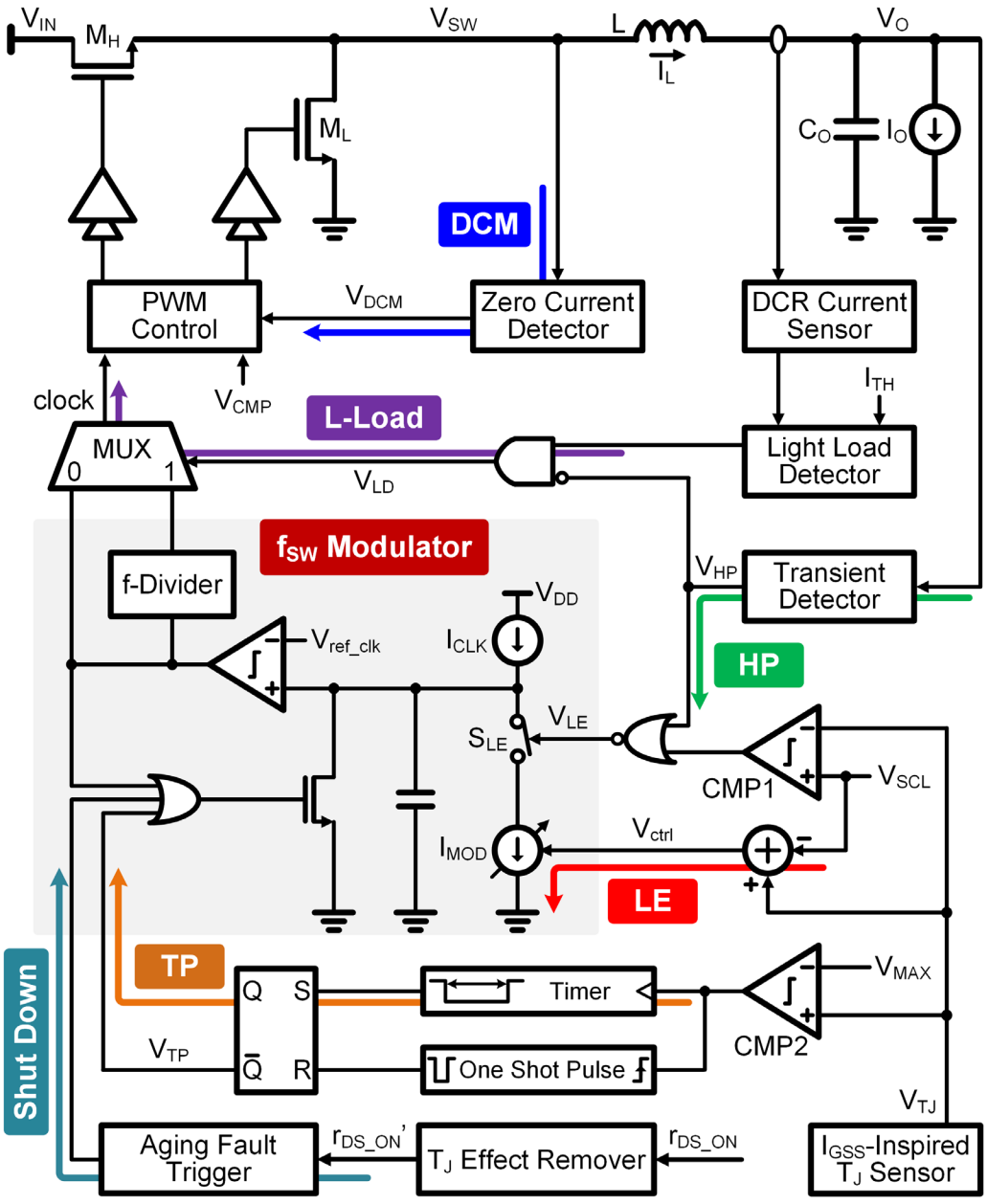


Figure 2.8. Circuit schematic of proactive temperature frequency scaling scheme.

modulator. As I_{MOD} is proportional to the difference between V_{TJ} and V_{SCL}, the switching frequency is thus modulated inversely against the T_J increasing, facilitating the suppression of the heat generation. In the meantime, to achieve optimal operation between performance and thermal aging, instant load condition is monitored. When load current I_O changes, fast response is required

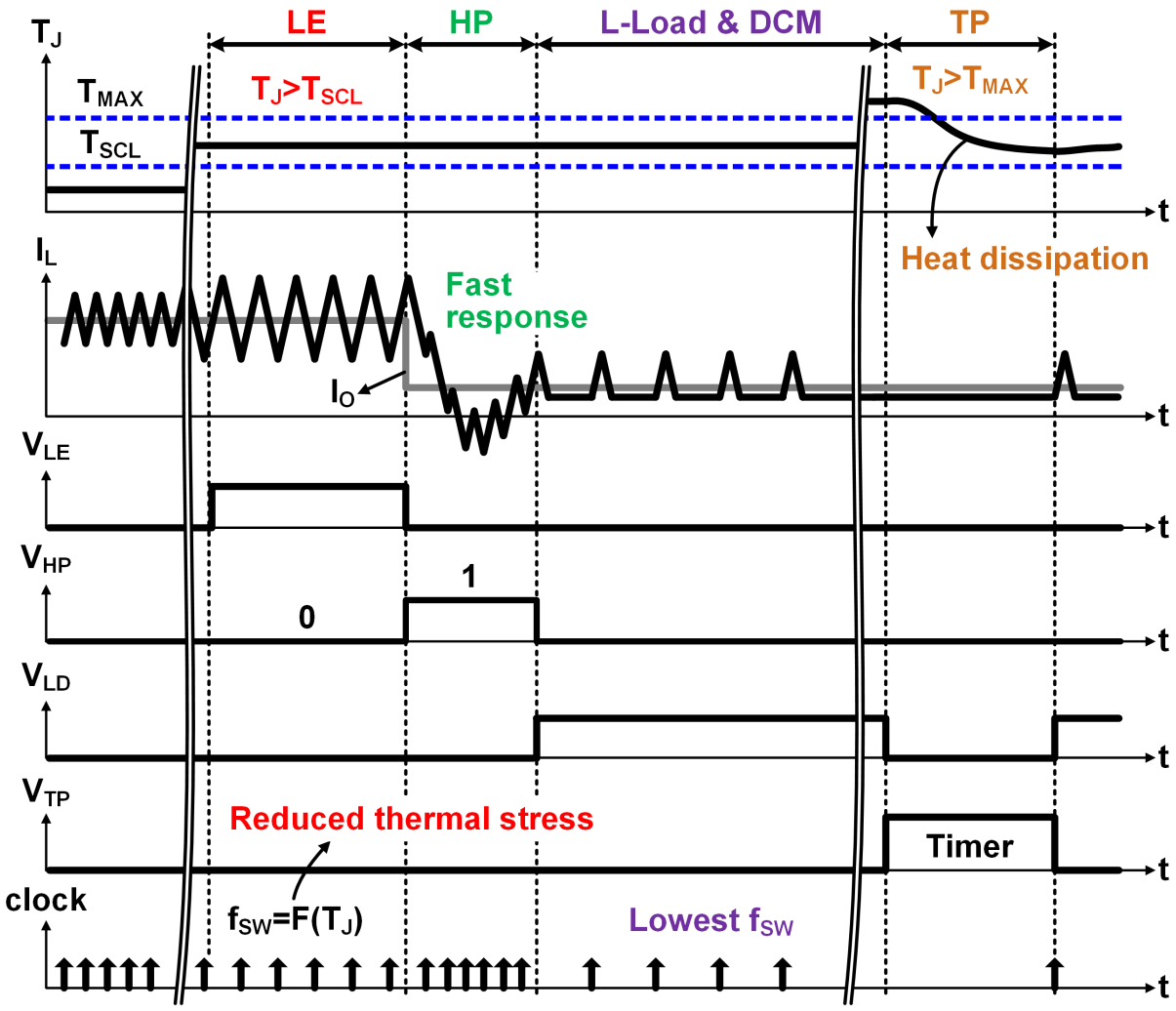
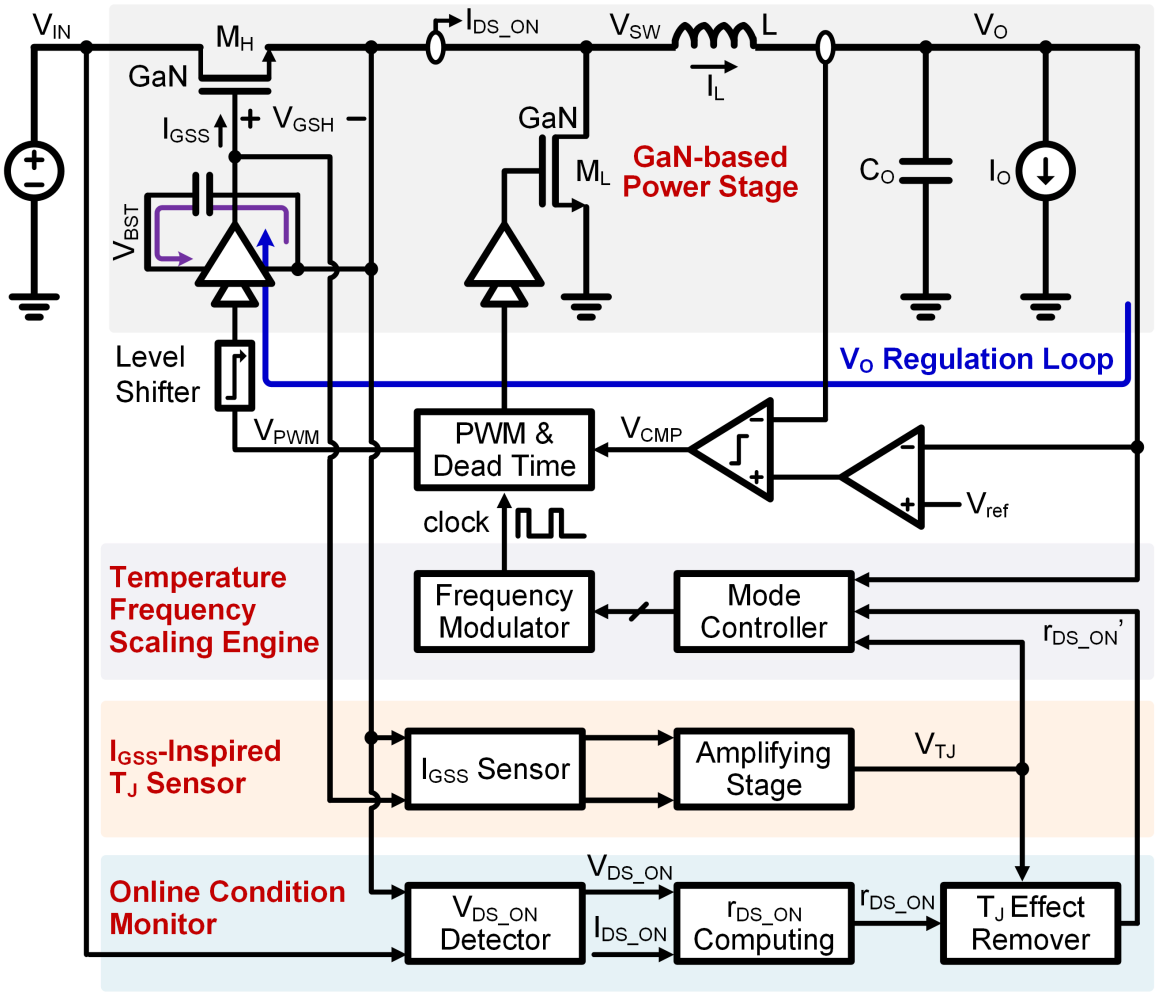


Figure 2.9. Operation principle of proactive temperature frequency scaling scheme.

to avoid V_O overshoot/undershoot, which cause potential malfunctions on load modules. In this situation, the transient detector captures the V_O variation to set the mode signal V_{HP}, triggering the high-performance (HP) mode. The switch S_{LE} is thus forced off, applying the maximum switching frequency for operation. Hence, the dynamic response is enhanced, minimizing the transient delay and voltage damping. At light load, the switching frequency decreases and the discontinuous conduction mode (DCM) is imposed, improving the power conversion efficiency. On the opposite, when T_J exceeds the allowed operation limit T_{MAX}, the output of the comparator CMP2 flips high,



(a)

Design Performance	TIE 2011 [6]	TIE 2016 [7]	This Design
Power device	IGBT	MOSFET	GaN HEMT
Aging precursor	V_{CE}	Pole location	r_{DS_ON}
i-collapse prognosis	No	No	Yes
Condition monitoring method	Offline	In-situ	Online
T_J dependence	Low	High	Low
Implementation	Discrete level	Discrete level	Integrated circuit
False monitoring rate	High	High	Low
Longevity improvement	No	No	Yes

(b)

Figure 2.10. Full system implementation of proposed GaN switching power converter. (a) Block diagram and (b) design summary.

inducing the one shot pulse generator to produce a narrow negative pulse. As a result, the thermal protection (TP) signal V_{TP} is triggered to high, terminating the switching clock for heat dissipation. When T_J drops down to lower than T_{MAX}, the normal operation of the converter is resumed. By this way, the converter is protected from thermal run-away. Moreover, along with the operating time, if the aging precursor r_{DS_ON}' rises beyond the aging threshold, the converter would be shut down, avoiding permanent system damage.

2.4.2 Full System Implementation

Figure 2.10 shows the full system implementation as well as the design summary in comparison with the prior arts. Two enhancement-mode GaN HEMTs are used as the power switches, enabling the converter to switch at 10MHz efficiently. The proposed online condition monitor senses the dynamic on-resistance r_{DS_ON} of GaN switch as aging precursor. Compared to offline and in-situ monitoring methodologies, it is capable of prognosing the *i*-collapse caused GaN device failure. In addition, a junction temperature T_J sensor is integrated on-chip by detecting the GaN gate leakage current I_{GSS} that is thermal sensitive and aging independent. By such means, the sensor can determine the T_J of GaN switch remotely and in real time, facilitating the temperature effect calibration on r_{DS_ON}. Thus, it helps achieve the T_J-independent condition monitoring, significantly suppressing the false monitoring rate. Compared to the prior works, this design is implemented in integrated circuits, making the solution compact and economical. Furthermore, to enhance the system longevity actively, the temperature frequency scaling scheme is employed to slow down the aging process whenever possible without degrading the system performance. Overall, the three techniques require no interruption on conventional closed-loop voltage regulation and are completely non-intrusive.

2.5 Experimental Verification

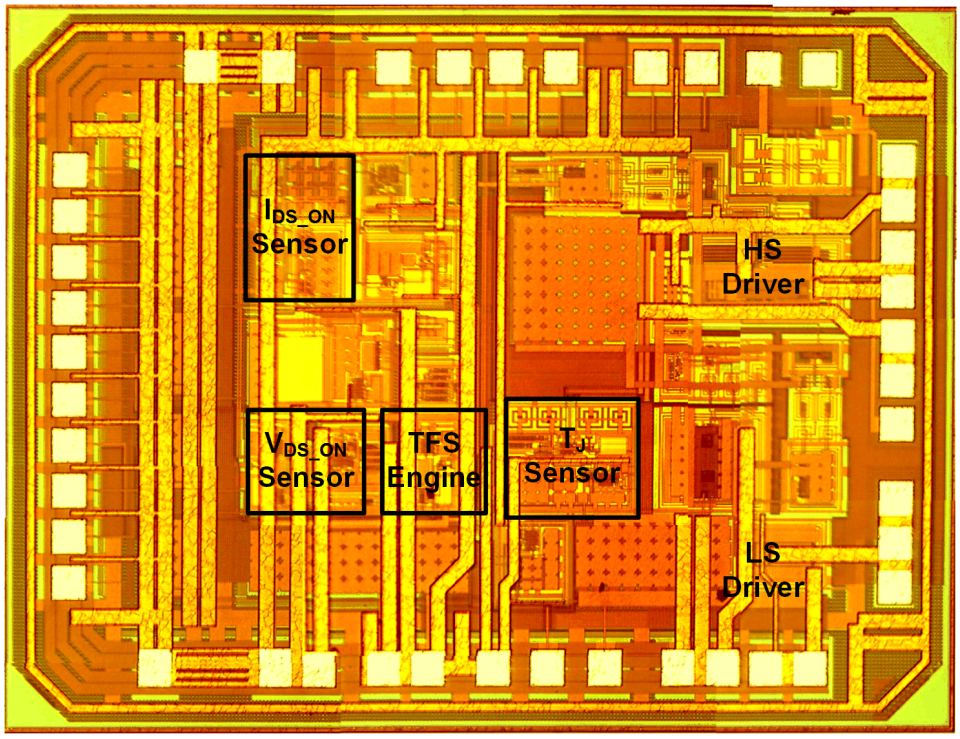
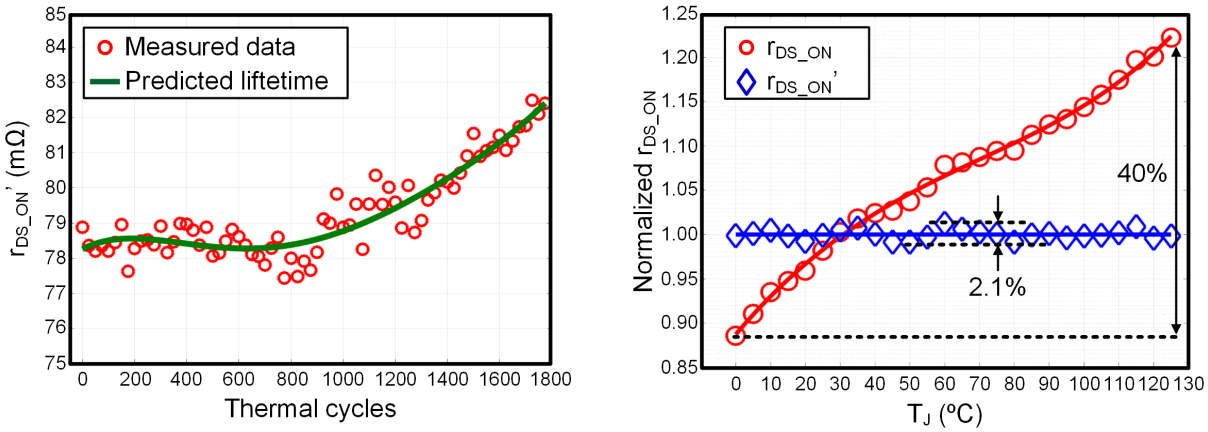


Figure 2.11. Chip micrograph.

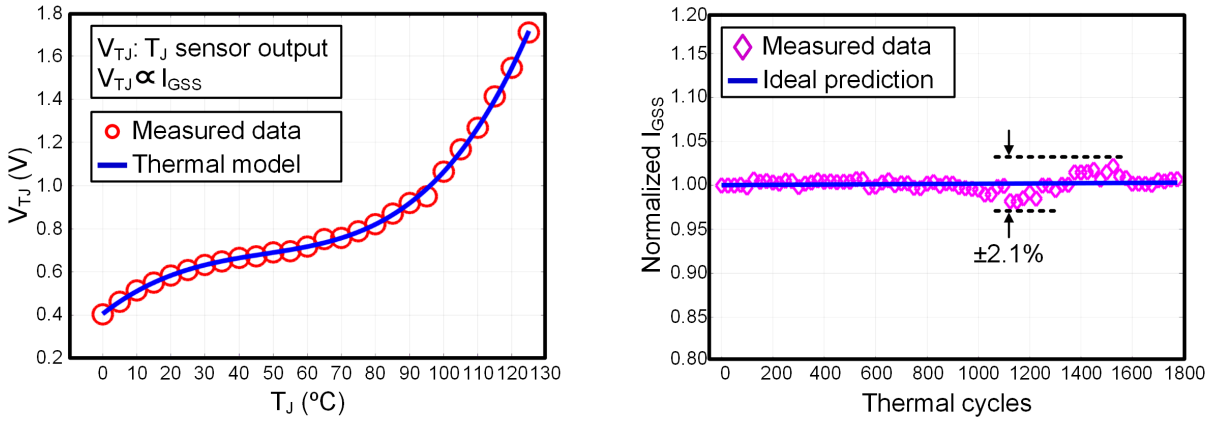
An experimental prototype of the design presented in this paper was fabricated in a 0.18-µm HV CMOS process, using two enhancement-mode GaN HEMTs (EPC8009) as M_H and M_L [Chen-19a]. The chip micrograph is shown in Figure 2.11, with an active die area of 1.56mm^2. The sensing circuits and proactive temperature frequency scaling engine are fully integrated. Switching at 10MHz, the converter delivers a maximum power of 6W over an input of 5 to 40V.

To verify the aging precursor definition, thermal stress test is set up with the GaN-based converter switching at 10MHz in a temperature chamber. The input and output voltages are used as 12V and 5V, respectively. The load current is 1A. The chamber temperature is varied between 0°C and 125°C periodically. The on-resistance of the high-side GaN switch are measured at the reference temperature 25°C every 25 cycles. Since it is taken under the normal switching of the



(a) (b)

Figure 2.12. Measured results on aging precursor r_{DS_ON}: (a) thermal stress test and (b) temperature dependence calibration.



(a) (b)

Figure 2.13. Measured results on the gate leakage I_{GSS}-inspired T_J sensing: (a) on-chip sensed voltage V_{TJ} versus T_J, and (b) I_{GSS} versus thermal cycles.

converter, the measured on-resistance represents the dynamic one r_{DS_ON} of GaN switch. Figure 2.12(a) shows the results, in which r_{DS_ON} increases gradually after a certain number of thermal cycles, offering clear and accurate tracking on the course of aging. Moreover, with the sensed junction temperature T_J, the T_J dependence of the on-resistance r_{DS_ON} is removed, reducing the T_J-dependence of r_{DS_ON} from 40% to 2.1% between 0°C and 125°C, acquiring an almost T_J-independent aging precursor r_{DS_ON}'. Thus, the false monitoring rate is suppressed by 19 times.

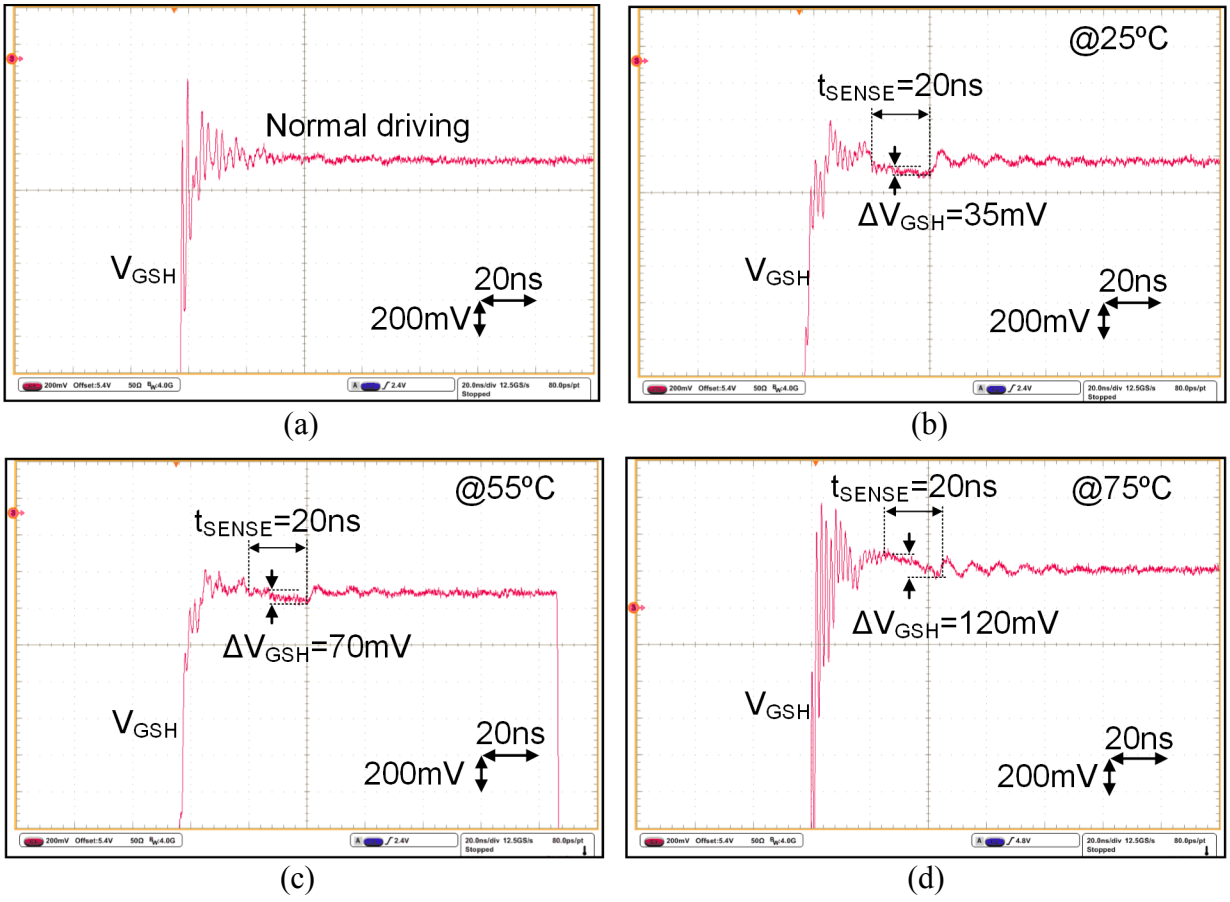


Figure 2.14. Measured GaN switch gate voltage waveforms with (a) normal driving, and T_J sensing at different temperatures of (b) 25°C, (c) 55°C and (d) 75°C.

The performance of the I_{GSS}-inspired T_J sensor is tested in Figure 2.13(a). The on-chip sensed voltage V_{TJ} increases as T_J rises. The measurement data coincide well with the thermal model, which is used by T_J effect remover to perform T_J calibration on sensed r_{DS_ON}. On the other hand, as shown in Figure 2.13(b), the I_{GSS} versus thermal cycles test proves that I_{GSS} aging dependence is below ±2.1%, much lower than conventional precursors. To validate the operation principle of I_{GSS}-inspired T_J sensor, Figure 2.14 shows the transient measurements on V_{GSH} at various temperatures. For normal driving in Figure 2.14(a), V_{GSH} is constantly powered by the driver stage and has no voltage drop. With T_J sensing, V_{GSH} drops during a constant 20ns sensing

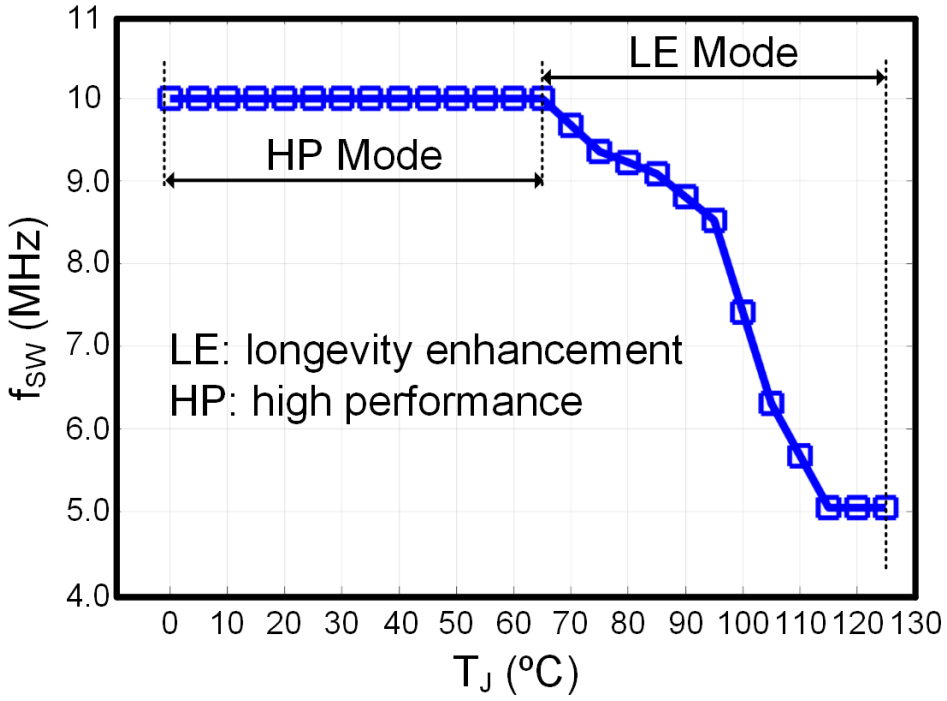
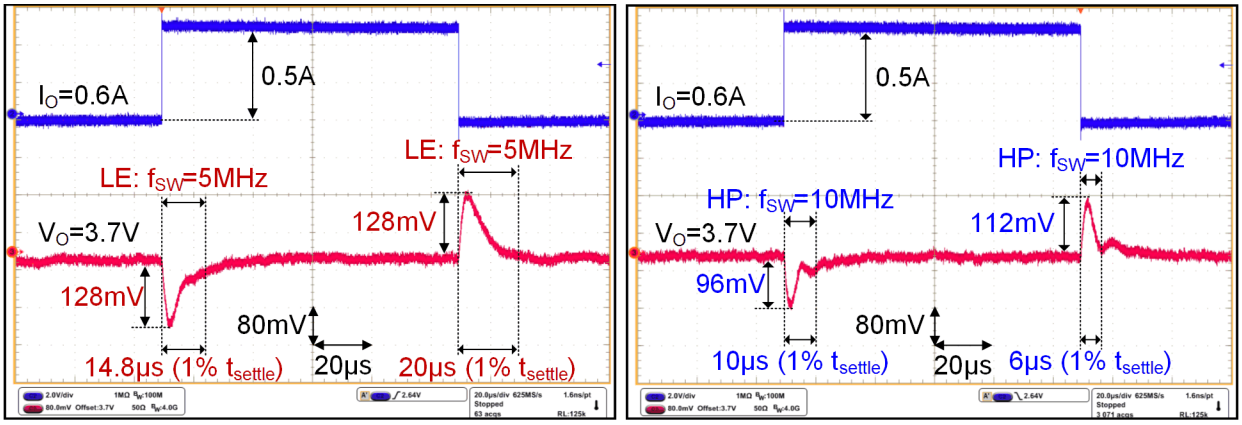


Figure 2.15. Measured results on the temperature frequency scaling scheme.

period, in which the gate capacitor C_G is discharged by I_{GSS}. At 25°C, 55°C and 75°C, the voltage drops are 35mV, 70mV and 120mV, respectively. Apparently, ΔV_{GSH} gets larger as temperature rises, but is still much smaller than the gate drive voltage (5V).

To validate the proactive temperature frequency scaling scheme, the switching frequency f_{SW}-T_J test is given in Figure 2.15. As T_J increases, f_{SW} scales across operation zones to reach an optimal operation between performance and aging. With power loss P_{LOSS} measurements, the longevity enhancement (LE) mode reduces P_{LOSS} by 200mW in maximum and T_J by 16°C with a typical GaN $R_{\theta JA}$ of 82°C/W, lowering the aging risk greatly. As addressed in the design, high-performance (HP) mode is enabled during load transient to optimize the system performance. Figure 2.16 shows the comparison of the dynamic response between the LE mode and HP mode, with input of 12V and output of 5V. In response to 500-mA I_O step-up change, the converter



(a) (b)

Figure 2.16. Comparison of load transient response under (a) longevity-enhancement (LE) mode and (b) high-performance (HP) mode.

achieves a 1% settling time t_{settle} of 14.8µs under LE mode. By enabling HP mode, t_{settle} reduces to 10µs, improving the transient response by 50%. As to the I_O step-down case, the 1% settling time reduces from 20µs to 6µs by switching the mode from LE to HP, improving the transient response by 70%. These measurements indicate that the temperature frequency scaling scheme balances the system performance.

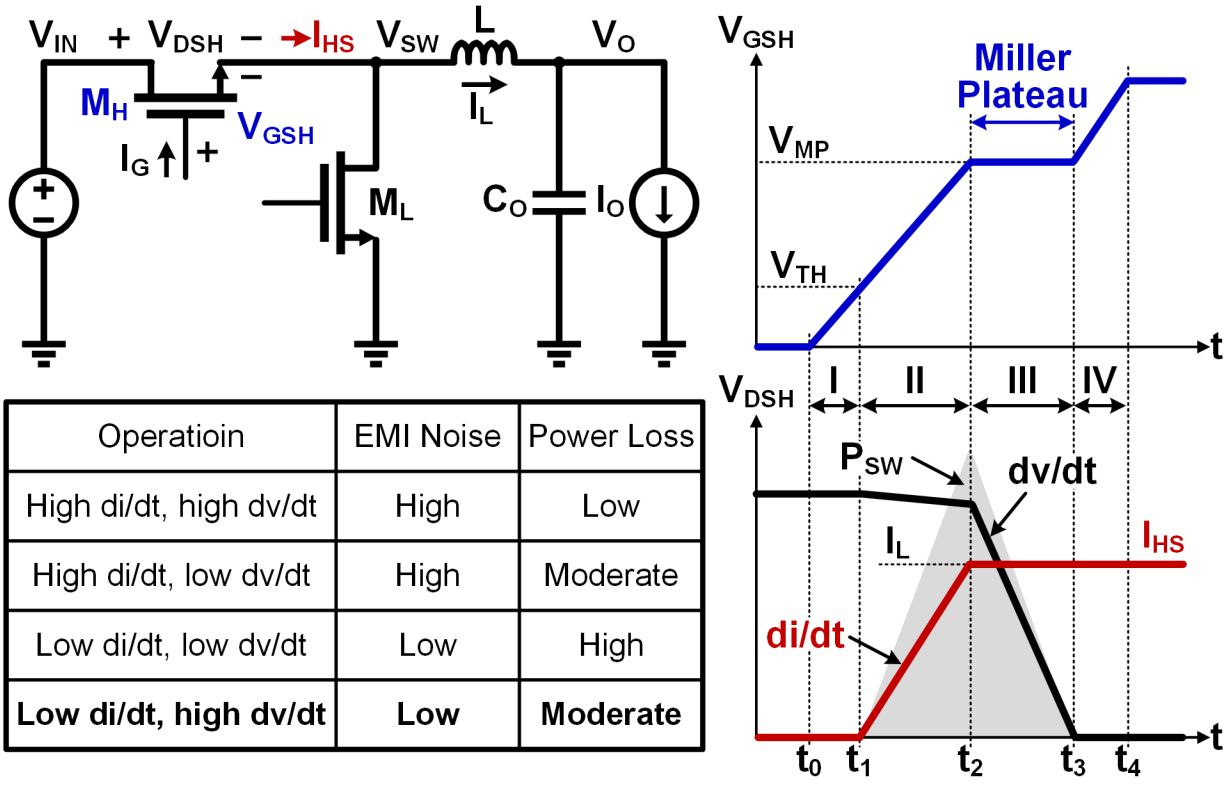
CHAPTER 3

CLOSED-LOOP EMI REGULATION USING EMULATED MILLER PLATEAU TRACKING AND ADAPTIVE STRENGTH GATE DRIVING*

In this chapter, a closed-loop EMI regulation methodology is presented and further demonstrated in a 10-MHz GaN-based buck converter. Through shaping the switching transitions actively, it balances the classic design trade-off between EMI and power efficiency. Section 3.1 discusses the EMI-efficiency trade-off and the design challenges to achieve a balanced performance. Section 3.2 introduces the system architecture and key design techniques, including the emulated Miller Plateau tracking scheme for instant Miller Plateau voltage detection and adaptive strength gate driving to implement the independent control of low di/dt and high dv/dt. Subsequently, Section 3.3 elaborates the circuit implementations, followed by the experimental results in Section 3.4 to validate the design.

3.1 Design Challenges in Slew Rate Control for EMI Reduction

Efficient power delivery is paramount to energy efficiency of integrated systems. Its implementation usually involves switching power circuits, whose frequent switching actions, unfortunately, induce drastic di/dt and dv/dt changes, accounting for major electromagnetic interference (EMI) noise generation. Slowing down switching speeds of these circuits can essentially reduce di/dt and dv/dt, and thus suppress the EMI emission. However, this usually come at the cost of switching power loss.



Operatioin	EMI Noise	Power Loss
High di/dt, high dv/dt	High	Low
High di/dt, low dv/dt	High	Moderate
Low di/dt, low dv/dt	Low	High
Low di/dt, high dv/dt	**Low**	**Moderate**

Figure 3.1. Switching V-I characteristics of the high-side switch M_H in a buck power converter demonstrating design trade-off between EMI and power loss.

To illustrate such, Figure 3.1 depicts the switching action of a high-side power switch M_H in a classic buck switching converter. The action can be divided into four key operation periods. In the period I from t_0 to t_1, the gate-source voltage V_{GSH} rises due to the gate charge current I_G. As V_{GSH} is still below the threshold voltage V_{TH} in this stage, M_H is off, leading to a constant drain-source voltage V_{DSH} and zero drain current I_{HS}. From t_1 to t_2, V_{GSH} surpasses V_{TH} and continues rising. Consequently, I_{HS} increases rapidly and eventually matches instant inductor current I_L at t_2. Such fast di/dt transition induces current ripples at input power source V_{IN}, which has been considered a major cause of conducted EMI noise [Consoli-96, Huang-16, Idir-06, Meng-06, Musumeci-97, TI-13, Wang-14]. In the Period III from t_2 to t_3, M_H conducts constant current I_L in

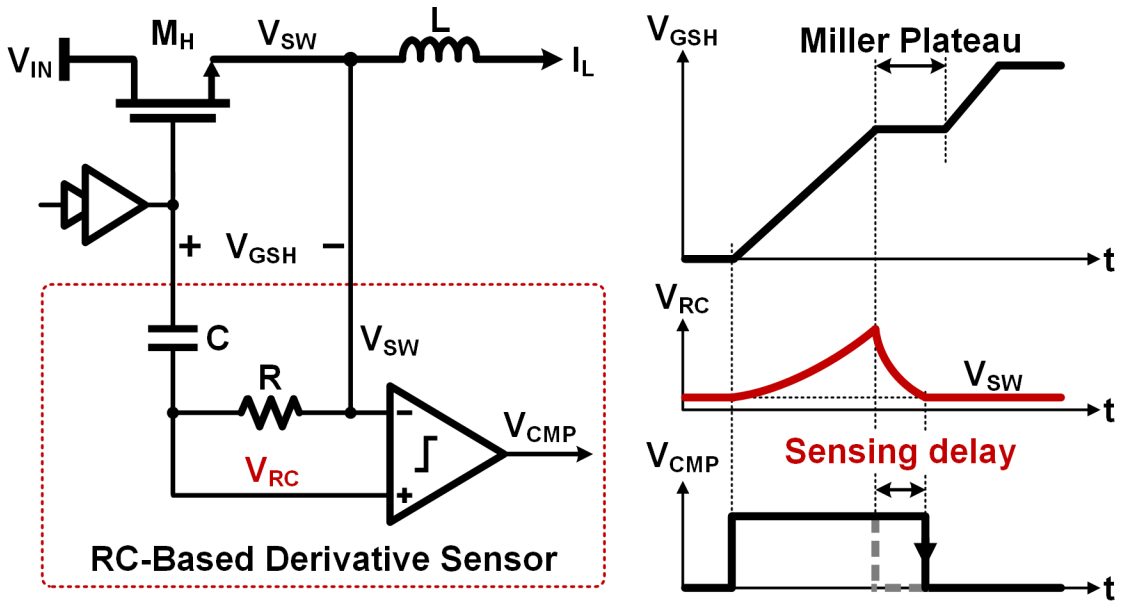
saturation region. Because of the Miller effect of its gate-drain capacitor, M_H presents a very large gate capacitance. As a result, V_{GSH} remains flat even though the I_G keeps charging the gate. This flat region is named as the Miller Plateau. It is in this period that V_{DSH} drops from higher than V_{IN} to nearly 0, leading to drastic dv/dt transition. Note that both V_{DSH} and I_{HS} are non-zero during the Period II and III, causing switching power loss P_{SW}. Apparently, P_{SW} is positively correlated with the time duration from t_1 to t_3. In the Period IV from t_3 to t_4, V_{GSH} is charged quickly to the final drive voltage, retaining a low on-resistance of M_H. These observation reveals that extending the switching transition period is beneficial for EMI compression due to lower current slew rate. However, it causes higher P_{SW} and lower power efficiency because of longer I-V overlap time.

As summarized in Figure 3.1, four gate driving strategies can be utilized to shape the switching transitions based on the rates of di/dt and dv/dt, which lead to different performances on EMI noise and power loss [Consoli-96, Huang-16, Idir-06, Meng-06, Musumeci-97, TI-13, Wang-14]. The first strategy of high di/dt and high dv/dt is capable of minimizing power loss. However, it suffers the worst EMI noise performance. The second one solely reduces dv/dt, inevitably increasing P_{SW} but without benefitting the EMI compression, which should be avoided in pragmatical designs. The third operation of low di/dt and low dv/dt could effectively suppress EMI noise. Unfortunately, it sacrifices excessive power loss due to low dv/dt. To optimize the trade-off between EMI and power loss, the fourth operation of low di/dt and high dv/dt is favorable, which is able to compress EMI generation while minimizing the compromise to power loss. To independently control di/dt and dv/dt, it is required to adjust the gate driving strength by taking the Miller Plateau starting point as the inflection instant. In particular, a low driving strength is applied initially to drive the power device gate, obtaining a low di/dt operation. After the gate-

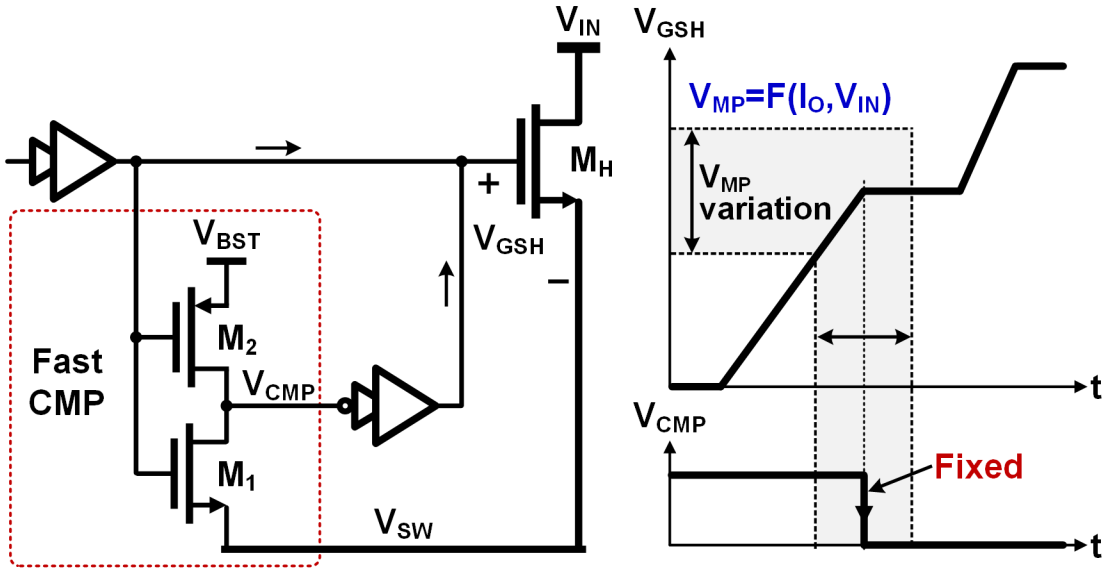
source voltage reaching the Miller Plateau starting point, the driving strength is enhanced abruptly to speed up dv/dt. However, such an active control methodology heavily relies on Miller Plateau sensing, which imposes a major challenge on the implementation.

From the analysis of the switching-on behavior in Figure 3.1, the Miller Plateau voltage represents the minimum gate-source voltage for the power switch to conduct the inductor current. Thus, it varies along with the load current I_O and power input voltage V_{IN}. To sense the Miller Plateau accurately, as illustrated in Figure 3.2(a), the first order derivative of either V_{GSH} or I_{HS} can be detected by using a differentiator such as a RC network [Musumeci-97, Wang-14]. When their values cross zero, then the Miller Plateau starting point can be identified, independent of operation conditions. However, such approaches are rather time-consuming because of derivative computing. As a result, they are confined to merely low frequency applications.

In addition, the significantly elevated switching frequencies in contemporary power converters present further challenges on Miller Plateau sensing. Driven by unprecedented power density and speed of modern electronic systems, silicon power MOSFETs are approaching the theoretical limit of performance. On the other hand, with superior figure of merits, GaN HEMTs have been demonstrated as promising power devices for high-frequency and high-performance switching power circuits [Baliga-13, Ke-17, Lidow-15, Song-15]. In recent years, GaN power converters have been reported to operate efficiently at or above 10MHz [Ke-17, Song-15]. Such high switching frequency considerably improves the load transient response of the converter. In the meantime, it allows the use of much smaller passive components for power delivery, facilitating system miniaturization. However, to accommodate the beyond 10MHz operation, the switching transitions must be completed within several nanoseconds, intensifying the EMI



(a)



(b)

Figure 3.2. Miller Plateau sensing mechanisms using the methods of (a) first-order derivative detection [Musumeci-97, Wang-14], and (b) fixed-reference fast prediction [Song-15].

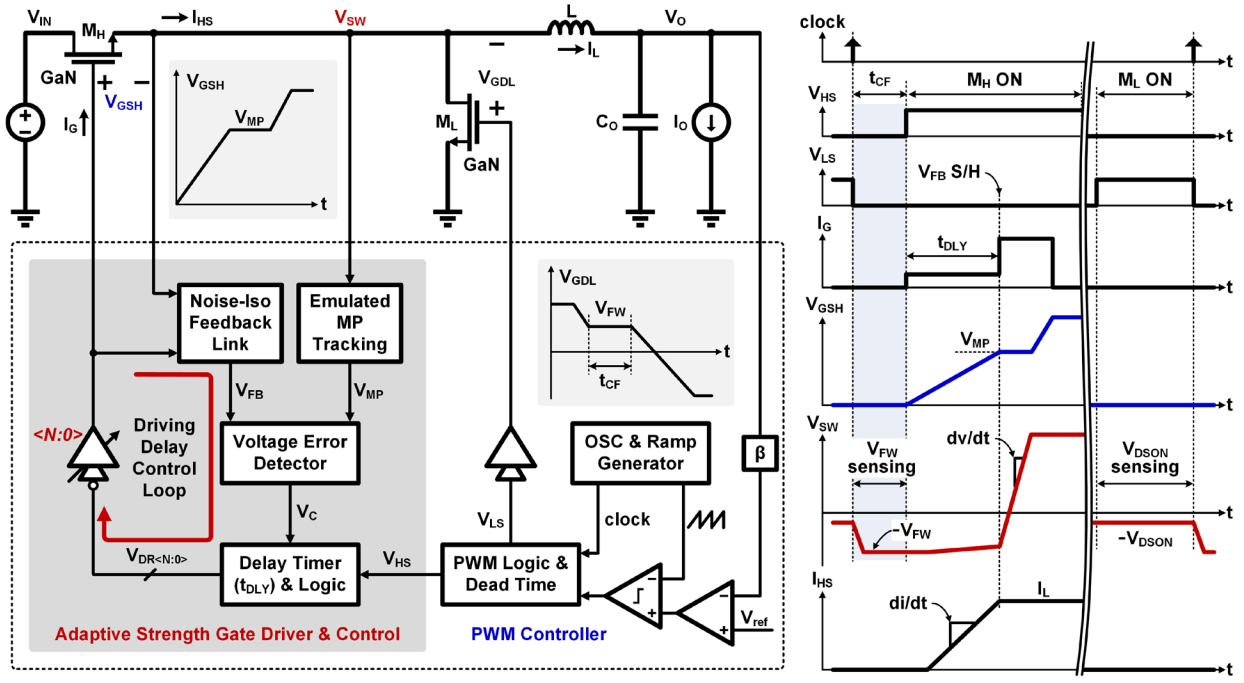
emissions. This makes the optimization of the EMI-efficiency trade-off much more urgent through the operation of low di/dt and high dv/dt. Paradoxically, the extremely narrow switching transitions

make it much harder to identify the Miller Plateau due to the considerable propagation delay in the sensing loop. To overcome these issues, as shown in Figure 3.2(b), a logic-gate-based fast comparator was employed to instantly predict the Miller Plateau starting point, with its threshold as a pre-defined reference [Song-15]. Although it minimizes the sensing delay, it is susceptible to I_O and V_{IN}, thus significantly compromising the sensing accuracy.

3.2 System Architecture and Operation Strategies

3.2.1 System Architecture

The overall system design is shown in Figure 3.3(a). The dedicated adaptive strength gate driver and control module is developed to actively regulate the switching behaviors of M_H, aiming to reduce the conducted EMI noise while with minimum switching power loss penalty. The power stage is constructed with two enhancement-mode GaN HEMTs as the power switches, M_H and M_L, respectively. A pulse-width-modulation (PWM) controller is employed to regulate the output V_O of the converter tightly. The system operation in steady state is illustrated in Figure 3.3(b). The clock resets the low-side duty signal V_{LS}, thus turning off M_L. To avoid shoot-through current from the power input to ground, there is a dead time imposed before turning on M_H. As a result, the switching node V_{SW} is floated and thus discharged rapidly to $-V_{FW}$. In this way, the GaN switch M_L, which lacks PN junction body diode, is conducting reversely to freewheel the inductor current I_L. During this period t_{CF}, the emulated Miller Plateau (MP) tracking block senses V_{FW} to replicate the Miller Plateau voltage V_{MP} instantly. Afterward, the high-side duty signal V_{HS} flips to high. Consequently, it initializes the high-side gate driver to charge V_{GSH}, inducing the current rise of I_{HS} subsequently. During this stage, the gate charging current I_G is remained at low level, obtaining the operation of low di/dt. As I_{HS} reaches I_L, then V_{GSH} enters the Miller Plateau zone. Thanks to

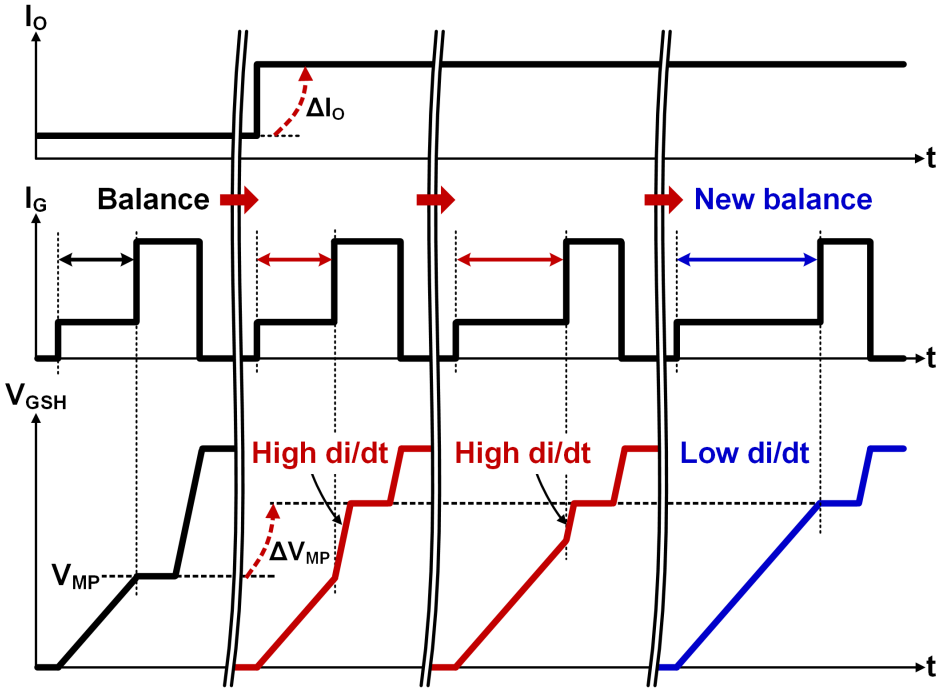


(a) (b)

Figure 3.3. (a) System architecture of the proposed GaN buck converter, and (b) operation waveforms in steady state.

the proposed adaptive strength gate driving scheme, I_G is enhanced synchronously at this moment to speed up V_{SW} rising process, hence achieving the desired high dv/dt operation to suppress the switching loss. Note that the delay from the beginning of V_{GSH} rising to I_G enhancement is denoted as t_{DLY}, which is the regulation variable of the driving delay control loop. When the on duty expires, M_H is turned off and M_L is subsequently turned on by V_{LS}. Then, V_{SW} reduces to a slightly negative voltage $-V_{DSON}$. As addressed later, this voltage is sensed to calibrate the emulated Miller Plateau tracking scheme. When a new clock signal arrives, the switching cycle repeats.

From the steady state operation, the emulated Miller Plateau tracking block functions cycle by cycle to generate the reference V_{MP}. Thus, as the switching conditions (including I_O and V_{IN}) change, it can detect the V_{MP} variation in real time. Meanwhile, the noise-isolated feedback link



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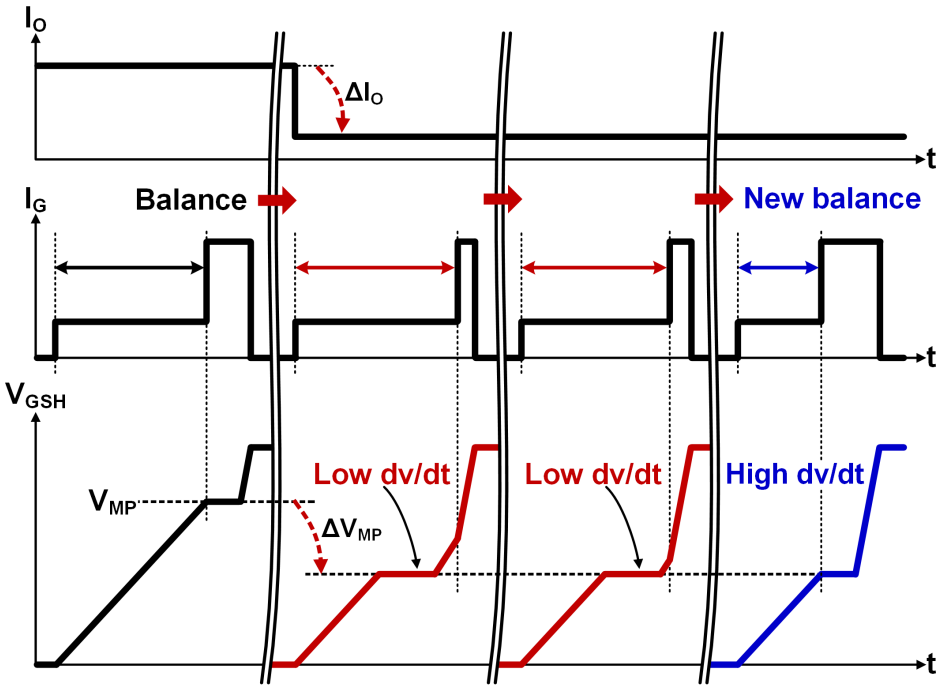


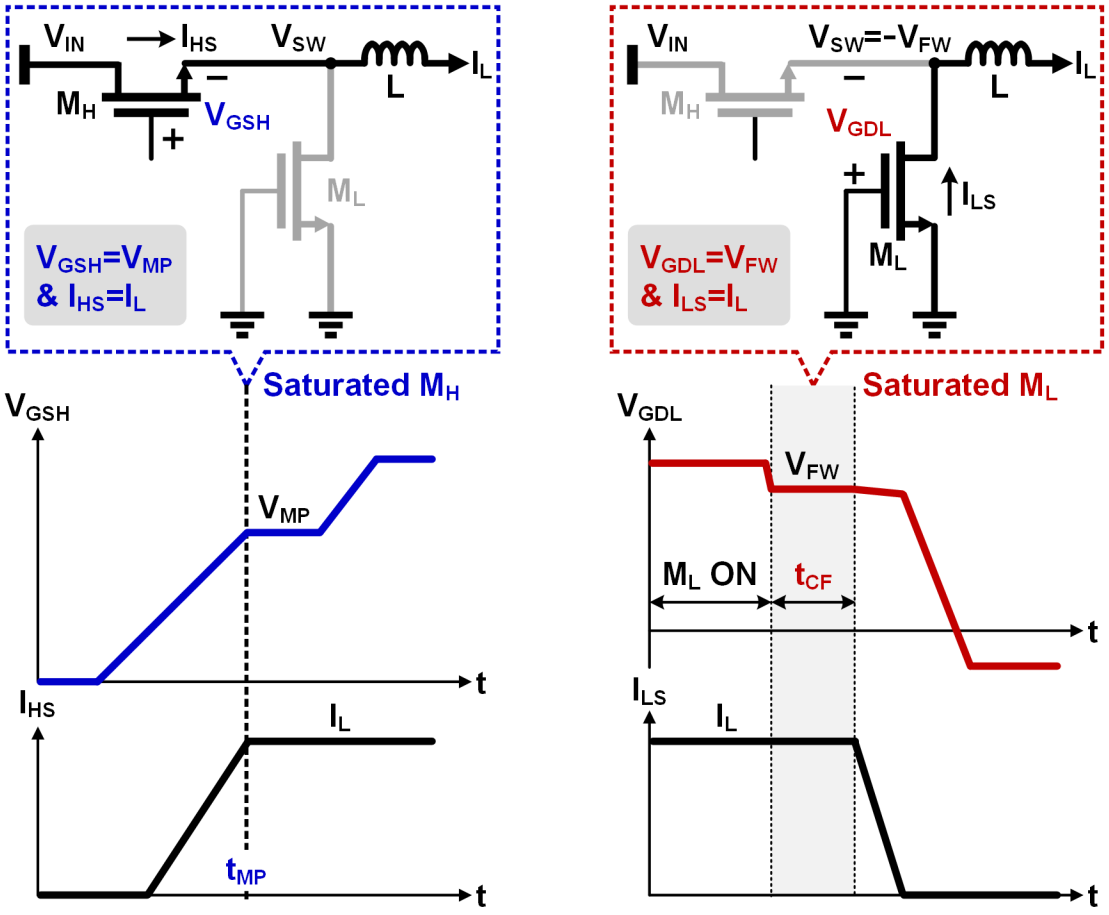
(b)

Figure 3.4. Adaptive strength gate driving control loop responses to (a) V_{MP} step-up due to I_O increase, and (b) V_{MP} step-down due to I_O decrease.

samples V_{GSH} at the instant when I_G is enhanced and then translates it into the feedback signal V_{FB}. The driving delay control loop regulates t_{DLY} to make sure that V_{FB} is equal to V_{MP}, thereby stabilizing the system operation. Figure 3.4 shows the loop responses to the V_{MP} transients. As shown in Figure 3.4(a), if V_{MP} rises due to I_O increase, the operation varies from the steady state, leading to high di/dt operation and thus deteriorating the EMI emissions. In such a scenario, the instant of I_G enhancement would be continuously delayed until eliminating the unintentional high di/dt transition. Similarly, as shown in Figure 3.4(b), when V_{MP} shifts to a lower level due to a lower I_O, the I_G is improved behind the Miller Plateau, resulting in low dv/dt operation. It elevates the switching loss but does not contribute to the EMI compression. In this case, t_{DLY} is reduced gradually to rule out low dv/dt, improving the power efficiency. By this way, optimum trade-off between EMI and power efficiency is ensured independent of power conditions.

3.2.2 Emulated Miller Plateau Tracking Scheme

Figure 3.5 depicts the basic principle of the emulated Miller Plateau tracking scheme. As analyzed in the previous section, the high-side power switch M_H starts to conduct the full amount of the inductor current I_L at the Miller Plateau starting point t_{MP} (Figure 3.5(a)). At this instant, M_H operates in saturation region with gate-source voltage V_{GSH}=V_{MP}. On the other hand, as shown in Figure 3.5(b), the low-side power switch M_L is turned off at the end of each discharge phase. At the beginning of the dead time before turning on M_H, both M_H and M_L are off, floating the switching node V_{SW}. As a result, V_{SW} is discharged continuously by I_L which cannot change instantaneously. In conventional scenario where silicon MOSFETs are used as power switches, V_{SW} would be clamped to a negative PN junction forward voltage by the body diode of M_L. However, such PN junction body diodes are absent in GaN FETs. In such case, V_{SW} is eventually



(a) (b)

Figure 3.5. Basic principle of emulated Miller Plateau tracking scheme: (a) M_H switching behavior at Miller Plateau starting point t_{MP}, and (b) M_L switching behavior during current freewheeling period t_{CF}.

discharged to a much more negative voltage $-V_{FW}$, forcing M_L to conduct for current freewheeling. During this period (namely t_{CF} in Figure 3.5(b)), M_L carries the inductor current I_L with a gate-drain voltage $V_{GDL}=V_{FW}$. Moreover, M_L is diode-connected and hence operates in saturation region. If the utilized GaN FETs are drain-source symmetrical and the channel length modulation effect can be ignored, then M_L during t_{CF} emulates the state of M_H at t_{MP}, leading to the equation as below:

$$V_{MP}=V_{FW}. \tag{3.1}$$

Equation (3.1) implies that V_{MP} could be replicated by V_{FW}, which forms the foundation of the emulated Miller Plateau tracking scheme. As addressed earlier, it is challenging to sense V_{MP} directly due to the narrow Miller Plateau duration. On the other hand, V_{FW} can be conveniently acquired by sensing V_{SW} during t_{CF}, expanding the applicability to high switching frequency operation. Another key benefit is that V_{FW} varies with I_O in the same way as V_{MP}. Thus, the emulated Miller Plateau tracking scheme inherently adapts to I_O variation.

It is worthy to note that the utilized GaN FETs are not drain-source symmetrical. To practically block high voltage, the power device's drain terminal is often extended compared to the source one, resulting in a higher drain resistance R_D than the source resistance R_S. Such an asymmetrical device structure induces an error ΔV_{ASY} between V_{MP} and V_{FW} in Equation (3.1). When the GaN FET conducts the inductor current I_L, ΔV_{ASY} can be straightforwardly derived as the difference between the voltage drops across R_D and R_S, leading to the equation below:

$$\Delta V_{ASY}=V_{GD}-V_{GS}=I_L\times(R_D-R_S). \tag{3.2}$$

Technically, with Equation (3.2), ΔV_{ASY} can be determined by sensing I_L, R_D and R_S. However, R_D and R_S are intrinsic device parameters, which are hard to measure accurately through external circuits. To mitigate this issue, the relation between on-voltage V_{DSON} and on-resistance R_{DSON} is considered here:

$$V_{DSON}=I_L\times R_{DSON}=I_L\times(R_D+R_S). \tag{3.3}$$

By combining the equations of (3.2) and (3.3), the Equation (3.4) is derived further:

$$\Delta V_{ASY}=\frac{R_D-R_S}{R_D+R_S}\times V_{DSON}=\frac{k-1}{k+1}\times V_{DSON}. \tag{3.4}$$

Here, the coefficient k is the ratio between R_D and R_S. According to the physical model from the device manufacturer, k is determined as 3 [EPC-19]. Thus, the Equation (3.9) is simplified as:

$$\Delta V_{ASY}=\frac{1}{2}\times V_{DSON}. \quad (3.5)$$

With the Equation (3.5), ΔV_{ASY} can be compensated precisely through sensing V_{DSON}. Apparently, the compensation is naturally adaptive to I_O.

In addition to ΔV_{ASY}, the other error between V_{MP} and V_{FW} in the Equation (3.1) is induced by channel length modulation effect. As shown in Figure 3.5, the drain-source voltage of M_H is equal to (V_{IN}+V_{TH}) at t_{MP}, whereas the source-drain voltage of M_L is equal to V_{FW} during t_{CF}. Their difference causes error due to the finite output impedance of GaN switch. Note that the voltage difference is dominated by V_{IN}. Thus, to mitigate this error, a compensation is added in proportional to V_{IN} with a coefficient α.

By including the above two error compensations, the Equation (3.3) is thus revised as:

$$V_{MP}=V_{FW}-\frac{1}{2}\times V_{DSON}-\alpha\times V_{IN}. \quad (3.6)$$

Hence, with the Equation (3.6), the Miller Plateau voltage V_{MP} can be accurately emulated, generating an accurate Miller Plateau reference for further processing.

3.2.3 Adaptive Strength Gate Driving

To perform the independent operation of low di/dt and high dv/dt, an adaptive strength gate driver is designed, which is controlled by a delay time regulation loop to automatically adjust the gate charging current during the switching-on transition. By accepting the emulated Miller Plateau voltage V_{MP} as a variable reference, the control loop is able to synchronize the gate driving strength enhancement with the Miller Plateau starting point, regardless of I_O and V_{IN}. Compared to the open-loop control using comparator, the proposed approach eliminates the long propagation delay issue [Huang-13, Lee-11], thereby ensuring the operation accuracy.

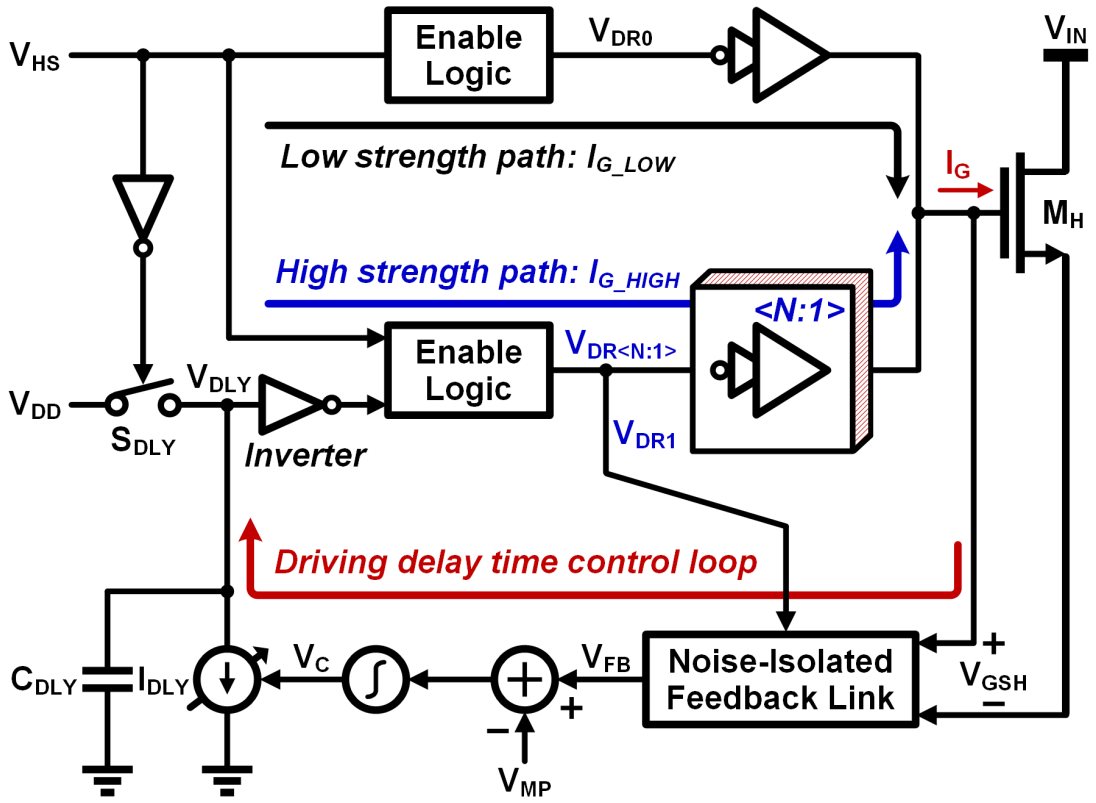


Figure 3.6. Block diagram of adaptive strength gate driving scheme.

Figure 3.6 shows the block diagram of the adaptive strength gate driver for high-side power switch M_H. Rather than the conventional structure with a fixed driving capability, the proposed design consists of a low strength driving path (supplying a low gate charging current I_{G_LOW}) and a high strength driving path (supplying an improved gate charging current I_{G_HIGH}). They are activated by the duty signal V_{HS} and the controlled delay signal V_{DLY}, respectively. While V_{HS} is generated by the feedback loop of the converter, the timing of V_{DLY} is modulated by the dedicated gate driving control loop primarily consisting of a noise-isolated feedback link, a voltage error detector and a voltage-controlled delay timer. As to the operation in Figure 3.7, at the beginning of each switching-on period t_0, the driving signal V_{DR0} is reset by the leading edge of V_{HS}. Accordingly, the low strength driving path is engaged first, producing I_{G_LOW} to slowly charge the

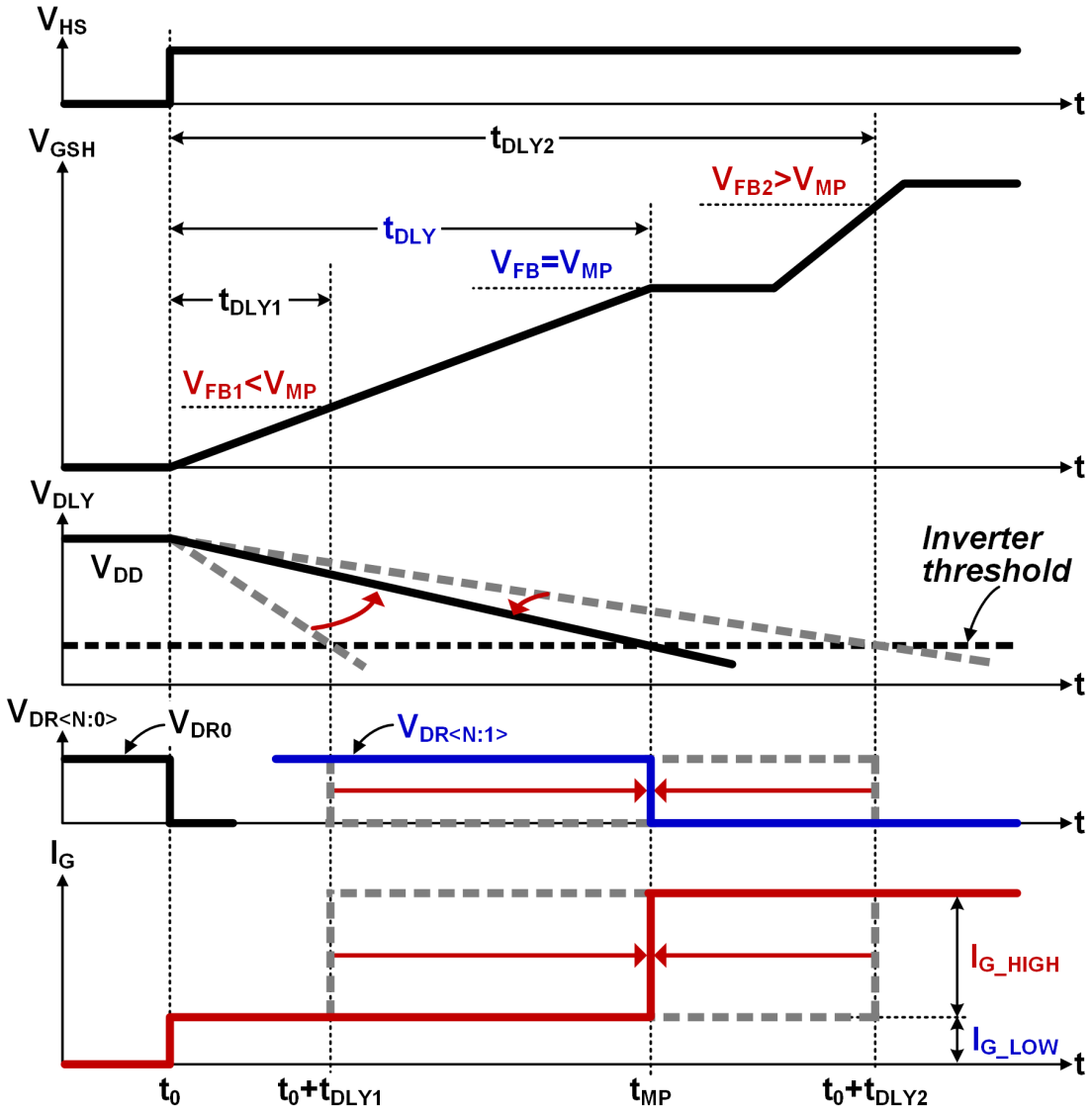


Figure 3.7. Operation principle of adaptive strength gate driving scheme.

gate of M_H. Thereby, V_{GSH} begins to ramp up. In the meantime, V_{HS} also initializes the delay timer by disconnecting the switch S_{DLY}. Thus, the voltage V_{DLY} drops down in a constant rate due to the discharge current I_{DLY}. When V_{DLY} is discharged to cross the inverter threshold, the output of the inverter flips from high to low, subsequently resetting the driving signals $V_{DR<N:1>}$. Hence, the high strength driving path is engaged to increase the gate charging current by I_{G_HIGH}. In equilibrium,

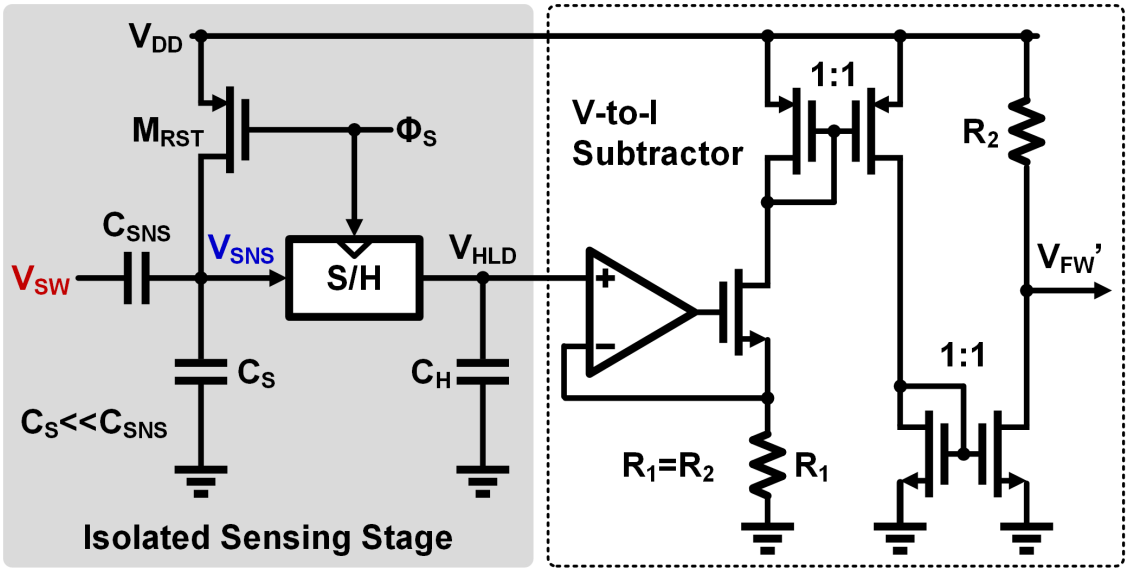
the delay time t_{DLY} between the activations of two driving paths is equal to the rising time of V_{GSH} from 0 to V_{MP}. It implies that the gate driving strength is enhanced just at the Miller Plateau starting point t_{MP}, achieving the desired operation of low di/dt and high dv/dt for targeted EMI and switching loss optimization.

On the other hand, when I_G is not improved at the Miller Plateau starting point, the gate driving control loop would continuously modulate t_{DLY} until the steady state is achieved. As show in Figure 3.6(b), if the high strength driving path is activated at the instant of (t_0+t_{DLY1}) to enhance I_G, earlier than the Miller Plateau starting point, then the delay time t_{DLY1} is insufficient compared to the target value t_{DLY}. In this case, triggered by the trailing edge of V_{DR1}, the noise-isolated feedback link would capture a lower feedback signal V_{FB1} than the reference V_{MP} (V_{FB1}<V_{MP}). Such a discrepancy between V_{FB} and V_{MP} is thus detected and integrated by the voltage-error detector to reduce V_C. Accordingly, the current I_{DLY} decreases to slow down the discharge of V_{DLY}. Consequently, t_{DLY1} gradually increases until it reaches t_{DLY}. Similarly, as the gate charging current I_G is improved later than the Miller Plateau due to a longer t_{DLY2}, the captured feedback signal V_{FB2} would be higher than V_{MP}. Such positive error increases V_C to speed up the discharge of V_{DLY}. Eventually, t_{DLY2} is stabilized at t_{DLY}. By means of such active control, the adaptive strength gate driver ensures the operation of low di/dt and high dv/dt, despite the switching conditions.

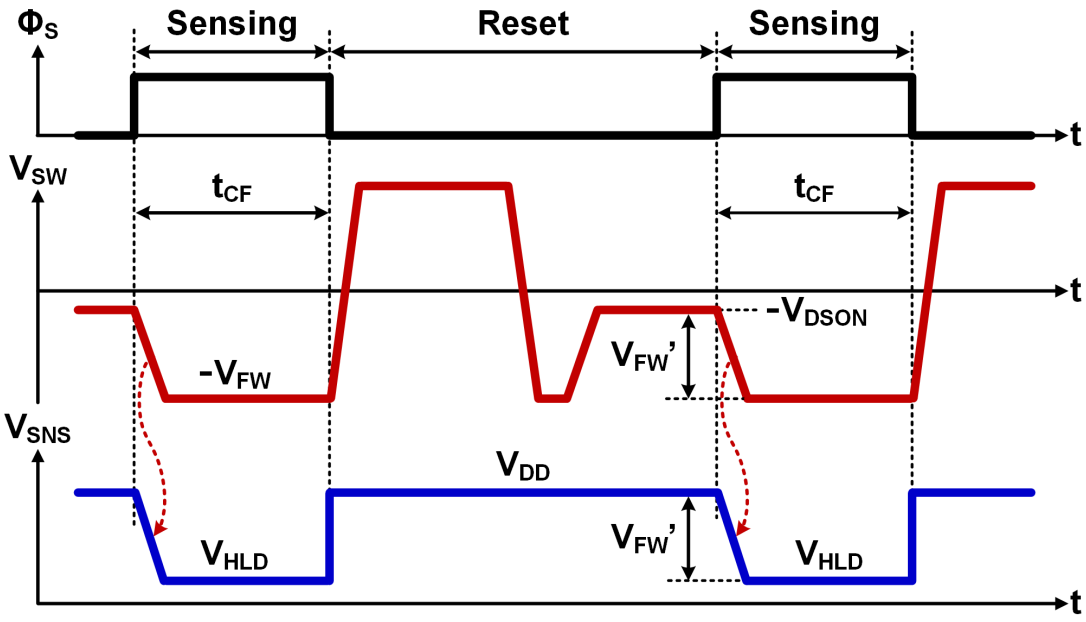
3.3 Circuit Implementations

3.3.1 Isolated Negative Voltage Sensor

To implement the emulated Miller Plateau tracking scheme as described in Equation (3.6), it is necessary to extract the current freewheeling voltage V_{FW}. However, as the amplitude of -V_{FW} is several times higher than a single PN junction forward voltage, direct sensing of such a deep



(a)



(b)

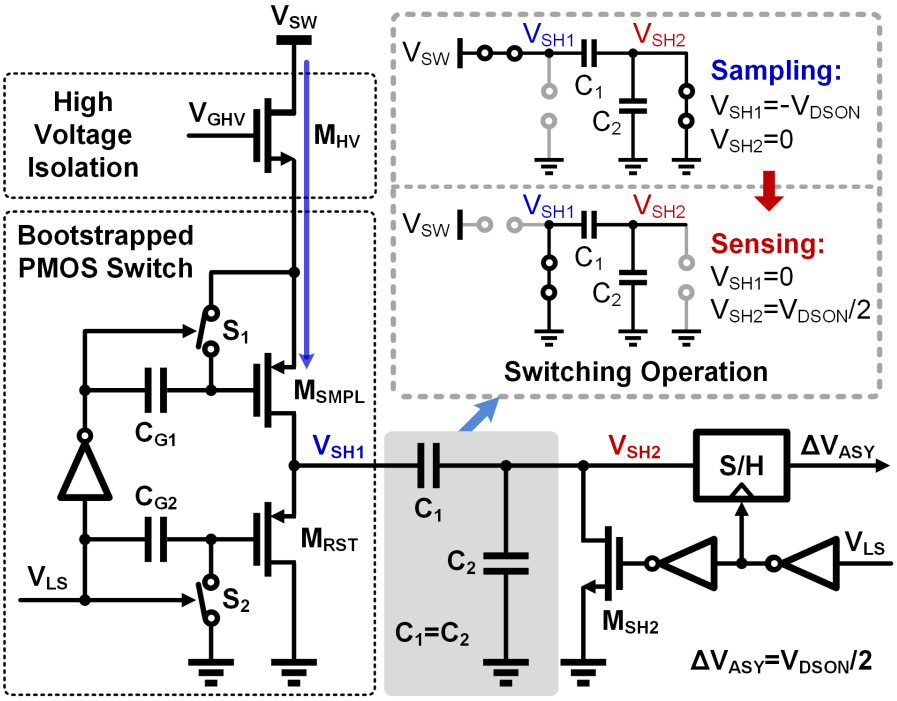
Figure 3.8. Circuit implementation of proposed emulated Miller Plateau tracking scheme: (a) schematic, and (b) operation waveforms.

negative voltage may turn on the parasitic junction transistors due to the high leakage current, leading to high power consumption and causing severe reliability issues. To combat these issues

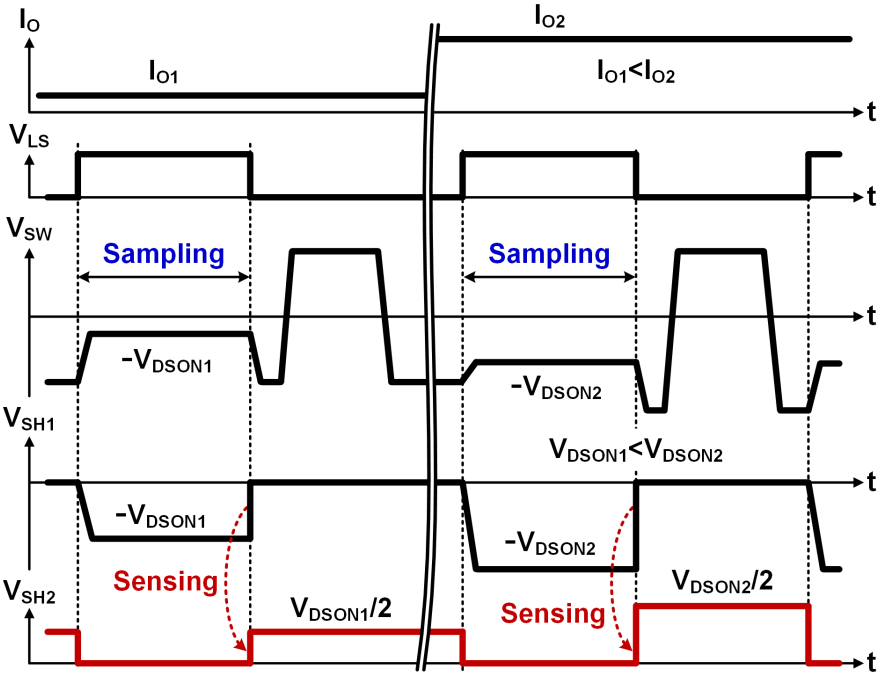
without increasing the circuit complexity, an isolated negative voltage sensor is designed as shown in Figure 3.8(a). To isolate the sensing circuits from the negative voltage, a sensing capacitor C_{SNS} is applied to detect the step-down transition of V_{SW}. Figure 3.8(b) illustrates the operation principle. As the low-side power switch M_L is turned off, V_{SW} drops down rapidly from the initial value -V_{DSON} to -V_{FW} due to discharge of I_L. To capture this voltage change, the sampling signal Φ_S switches to high, floating the sensing node V_{SNS} at the bottom plate of C_{SNS}. Accordingly, through C_{SNS}, the step-down transition at V_{SW} is AC-coupled to V_{SNS}. Thus, V_{SNS} changes from the initial value V_{DD} to (V_{DD}-V_{FW}+V_{DSON}). After the current freewheeling period t_{CF}, Φ_S is reset to sample and hold V_{SNS} to the node V_{HLD}. Afterward, V_{SNS} is reset to the reference V_{DD} for the next sensing period. To extract the absolute value of V_{FW} further, a voltage-to-current subtractor is used to subtract V_{HLD} from V_{DD}, acquiring the output V_{FW}' as (V_{FW} -V_{DSON}). Compared to the desired voltage V_{FW}, the output V_{FW}' has a DC offset of V_{DSON}, which would be cancelled out by the same term in the feedback signal V_{FB} from the noise-isolated feedback link.

3.3.2 Sensing Error Compensator

A sensing error compensator is designed to eliminate the discrepancy ΔV_{ASY} (=0.5×V_{DSON}) between V_{MP} and V_{FW}, which is induced by the asymmetrical GaN device structure. To sense V_{DSON}, as shown in Figure 3.9(a), a bootstrapped PMOS switch M_{SMPL} is used to sample V_{SW} when M_L switches on. Compared to its NMOS counterpart, the bootstrapped PMOS switch removes the body bias issue induced by the large swing range at V_{SW}. Then, a capacitive divider consisting of C_1 and C_2 is connected subsequently to scale down the sensed voltage. To isolate the low-voltage sensing circuits from high voltage at V_{SW}, a DENMOS M_{HV} is inserted between them. The operations are detailed in Figure 3.9(b). The leading edge of V_{LS} triggers to turn on M_L, thus setting



(a)



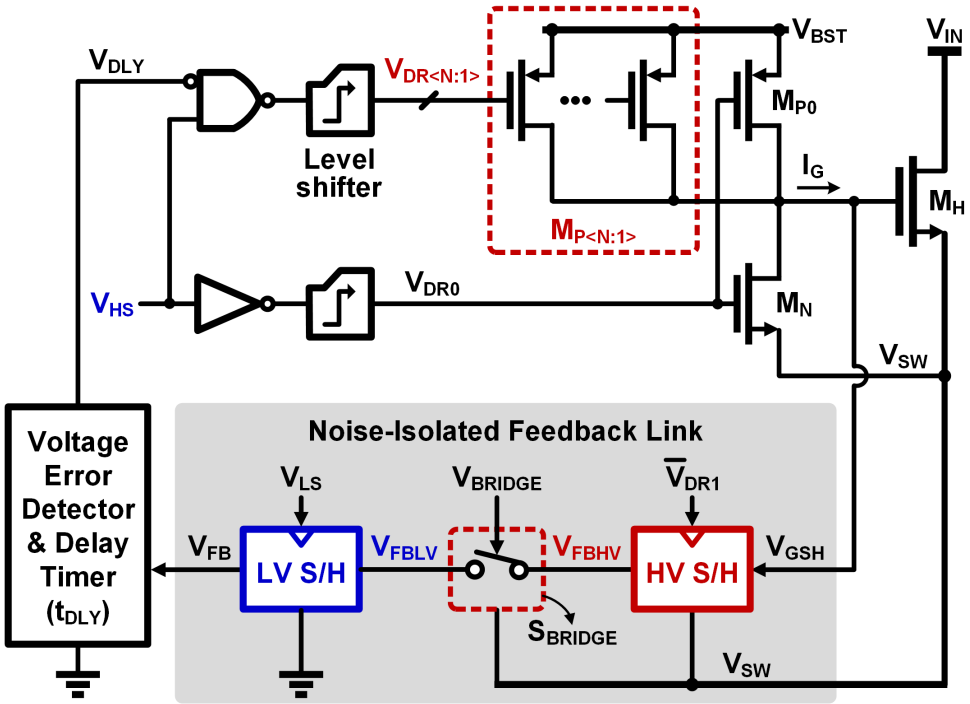
(b)

Figure 3.9. Compensation of GaN device structure induced error in emulated Miller Plateau tracking scheme: (a) schematic, and (b) operation waveforms.

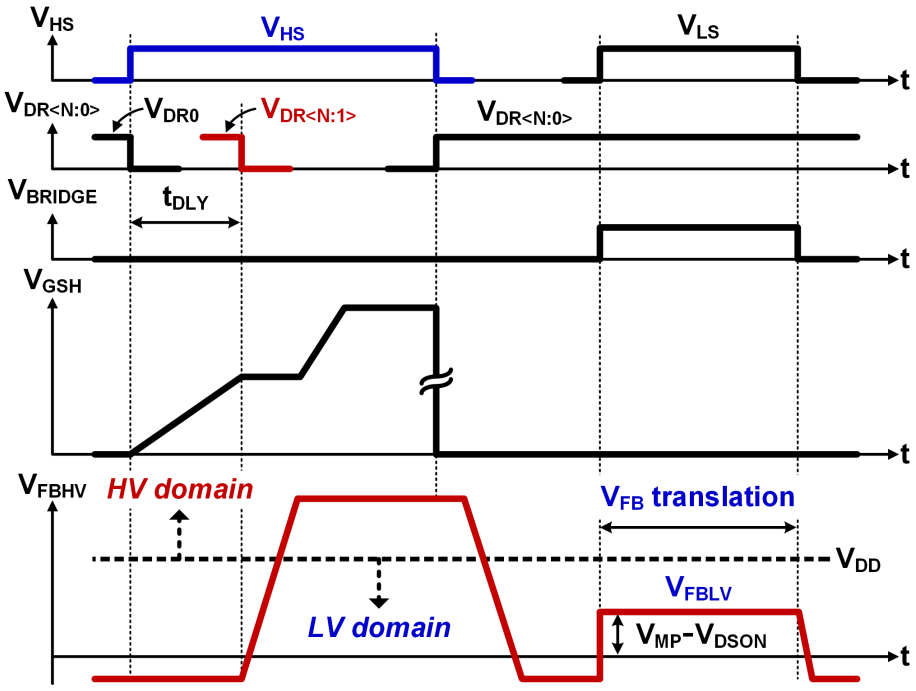
V_{SW} to $-V_{DSON}$. Meanwhile, it initializes the sampling phase by connecting the switch M_{SMPL}. Thus, $-V_{DSON}$ is delivered to the input of the divider, namely V_{SH1}. During this period, the output of the divider, namely V_{SH2}, is reset to ground by M_{SH2}. As the trailing edge of V_{LS} triggers to turn off M_L, M_{SMPL} is also disconnected to terminate the sampling phase. Then, V_{SH1} is reset by M_{RST} from $-V_{DSON}$ to ground. Note that V_{SH2} has been floated by disconnecting M_{SH2} at this moment. Hence, due to the AC-couple of C_1 as well as voltage division of C_2, V_{SH2} changes from 0 to $0.5\times V_{DSON}$. Controlled by V_{LS}, V_{SH2} is delivered to the output as ΔV_{ASY} for error compensation. As shown in the waveforms, when I_O changes, ΔV_{ASY} varies proportionally, attaining a dynamic compensation.

3.3.3 Noise-isolated Feedback Link

Figure 3.10 (a) shows the circuit implementation of the adaptive strength high-side gate driver. To provide a programmable gate driving, the driving-up stage is divided into (N+1) units, $M_{P<N:0>}$. They are respectively controlled by the active low driving signals $V_{DR<N:0>}$. Moreover, the noise-isolated feedback link is also detailed here, which is critical for the adaptive strength gate driving control. As addressed earlier, to achieve closed-loop t_{DLY} regulation, V_{GSH} needs to be sampled as the feedback signal. The design challenge lies in the fact that the V_{GSH} locates in the bootstrapped high-voltage (HV) domain with respect to V_{SW}, whereas the control circuits are in low-voltage (LV) domain with respect to ground. Traditionally, an analog level shifter can be employed to translate analog voltage between two voltage domains [TI-11]. However, due to the finite bandwidth and limited PSRR of the analog level shifter, this approach suffers from severe switching noise interference between HV and LV operation domains. To avoid this issue, the noise-isolated feedback link is designed on the ground of timing control, consisting of two S/H modules allocated in HV and LV domains, respectively. They are bridged up by a switch S_{BRIDGE}



(a)



(b)

Figure 3.10. Implementation of adaptive strength gate driver and its control: (a) schematic, and (b) operation waveforms.

for voltage translation. Figure 3.10(b) shows the operation waveforms of the adaptive strength gate driving. The leading edge of V_{HS} triggers to reset the driving signal V_{DR0}, activating M_{P0} to charge up V_{GSH}. After t_{DLY}, the remained driving signals $V_{DR<N:1>}$ are reset to enable $M_{P<N:1>}$, enhancing the driving strength. In the meantime, triggered by the trailing edge of V_{DR1}, the HV S/H module in the noise-isolated feedback link samples V_{GSH} as V_{FBHV} in HV domain. After M_H switches on completely, V_{SW} is charged up to nearly V_{IN}. Accordingly, V_{FBHV} switches up to a higher level than V_{IN} with respect to the ground. During this period, S_{BRIDGE} remains off, isolating the switching noise in HV domain from LV domain. When M_L is turned on by V_{LS}, V_{SW} drops to nearly zero. As a result, V_{FBHV} switches down to a lower level than the power supply V_{DD}. In this case, S_{BRIDGE} is connected to transfer V_{FBHV} into LV domain as V_{FBLV}. Further, through the LV S/H module, V_{FBLV} is sampled as the eventual feedback signal V_{FB}, accomplishing the voltage translation. From the operation, S_{BRIDGE} is disconnected during the switching transitions. Thus, the switching noise interference is minimized to only the couple effect of the parasitic capacitance of S_{BRIDGE}. As a sampling switch, S_{BRIDGE} could be designed small enough to sufficiently suppress the noise interference, thereby ensuring the feedback accuracy. Note that V_{FB} has an offset of V_{DSON} compared to the magnitude of V_{FBHV}. This offset compensates the same one in the output of the emulated Miller Plateau tracking module.

3.4 Experimental Verification

An experimental prototype of this paper was designed in a 0.35-μm HV BCD process with an active chip area of 0.9mm^2 [Chen-17]. Figure 3.11 shows the testing board and chip micrograph. Two enhancement-mode GaN HEMTs (EPC8002) are employed as the power switches. The converter operates at 10MHz and supports a wide input range of 5V to 40V and an output range

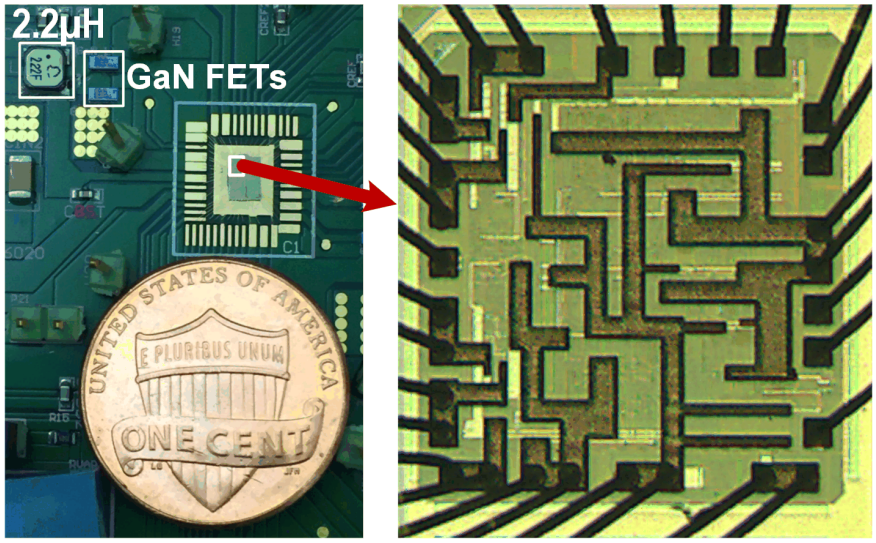
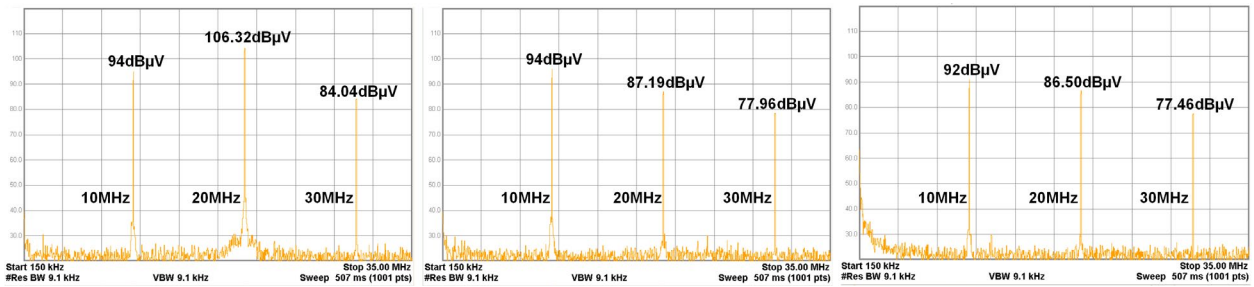
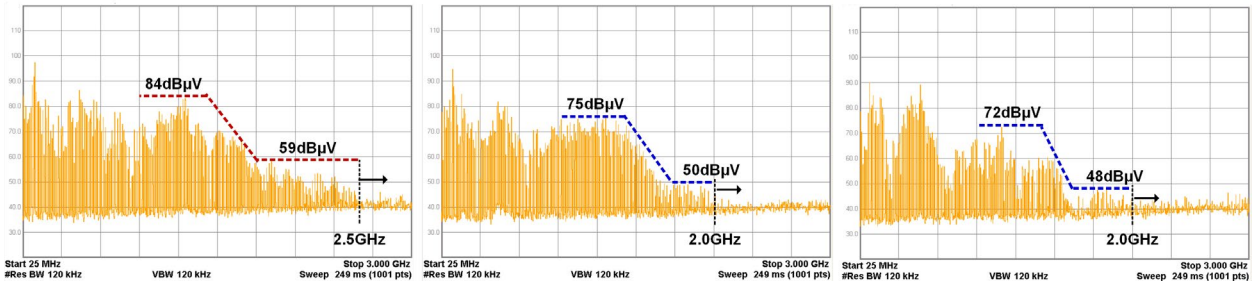


Figure 3.11. Chip micrograph.



(a) (b) (c)

Figure 3.12. Measured EMI spectra in Band B (< 30MHz) under different operation modes: (a) high di/dt and high dv/dt, (b) proposed work with low di/dt and high dv/dt, and (c) low di/dt and low dv/dt.



(a) (b) (c)

Figure 3.13. Measured EMI spectra in Band C/D (> 30MHz) under different operation modes: (a) high di/dt and high dv/dt, (b) proposed work with low di/dt and high dv/dt, and (c) low di/dt and low dv/dt.

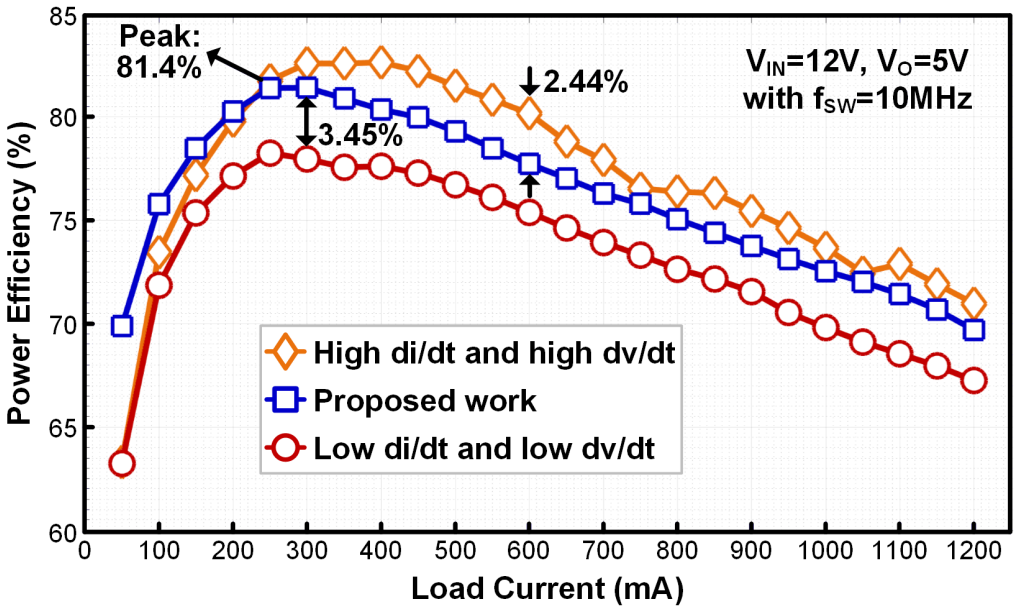


Figure 3.14. Measured efficiency.

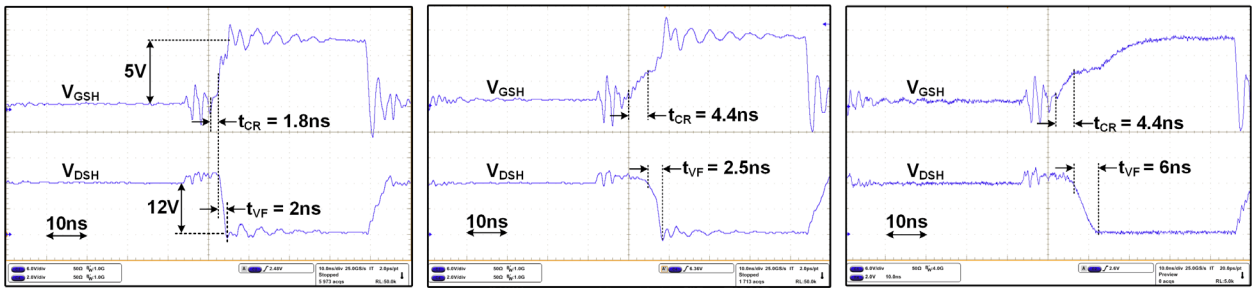
of 3.3V to 5V, with a maximum load current of 1.2A.

To evaluate the feasibility of the proposed design, Figure 3.12 and Figure 3.13 show the comparison of the measured conducted EMI noise spectra in Band B (<30MHz) and Band C/D (>30MHz), respectively. Compared to the high di/dt and high dv/dt operation, the proposed design reduces the peak EMI level by up to 19.23dBμV in the Band B and stays at least 9dBμV lower through the Band C/D. In the meantime, it should be noted that the EMI noise is not suppressed further if the dv/dt is reduced as well, illustrated in EMI spectra with the operation of low di/dt and low dv/dt.

As a design trade-off to EMI noise, the power efficiency plots under the three operation modes are shown in Figure 3.14. As the cost of EMI reduction, the power efficiency of this work drops by 2.44% compared to the high di/dt and high dv/dt operation. But it is up to 3.45% higher than that of the low di/dt and low dv/dt operation. Combined with the EMI noise measurements, it

proves that the proposed work successfully strives a balance between EMI noise and power efficiency.

To evaluate the operations in time domain further, Figure 3.15 shows the measured waveforms of the high-side gate-source voltage V_{GSH} and drain-source voltage V_{DSH}. In comparison to the high di/dt and high dv/dt operation, the proposed design extends the initial rising time t_{CR} of V_{GSH} by 2.4 times from 1.8ns to 4.4ns, while it remains the almost same voltage falling time of V_{DSH}. These measurements illustrate that di/dt is reduced correspondingly without influencing the high dv/dt operation. On the other hand, the proposed work reduces the voltage falling time t_{VF} of V_{DSH} by 2.4 times from 6ns to 2.5ns while with the same initial rising time of V_{GSH}. With these measurements, it implies that the proposed design precisely realizes the desired control of low di/dt and high dv/dt.



(a) (b) (c)

Figure 3.15. Measured waveforms of high side gate-source voltage V_{GSH} and drain-source voltage V_{DSH} under different operation modes: (a) high di/dt and high dv/dt, (b) proposed work with low di/dt and high dv/dt, and (c) low di/dt and low dv/dt.

Table 3.1 compares the design in this work with the prior arts. Compared to the conventional active Miller Plateau sensing approaches, the proposed emulated Miller Plateau tracking scheme is able to sense the Miller Plateau in real time without compromise to the sensing accuracy. Moreover, the closed-loop gate driving control is capable of adjusting the driving

strength in synchronous with the Miller Plateau starting point without propagation delay issue, suitable for GaN-based applications in high switching frequencies (≥10MHz). Implemented on chip, this work facilitates the system miniaturization, thereby improving the power density and reducing the overall cost.

Table 3.1. Performance comparison.

Design	Musumeci-97	Wang-14	This Work
Power Device	IGBT & MOSFET	IGBT	GaN HEMT
Switching Frequency	< 33kHz	< 280kHz	10MHz
Miller Plateau Detection Way	RC-based derivative sensing	Digital differentiator	Emulated Miller Plateau tracking
Detection Delay	Long (related to RC network)	Short	Instant detection
Gate Driving Strength Control	Closed loop	Open loop	Closed loop
Control Propagation Delay	Short	Long	Short
Overall Detection Accuracy	Moderate	Low	High
EMI-efficiency Trade-off Optimization	Not reported	Not reported	Yes
Implementation	Discrete level	Discrete level	Integrated circuit

CHAPTER 4

EMI SUPPRESSION USING CONTINUOUS RANDOM SPREAD-SPECTRUM MODULATION AND ONE-CYCLE ON-TIME REBALACNING*

This chapter presents continuous random spread-spectrum modulation (SSM) scheme to mitigate the EMI issue in GaN-based power converter. In Section 4.1, the limited EMI attenuation in the conventional SSM techniques is reviewed. Specifically, the periodic SSM could not scatter the EMI spectra uniformly, while the digital random SSM has finite frequency resolution. Moreover, the compromise of EMI spreading to the output regulation of power converter is illustrated in detail. To mitigate these issues, Section 4.2 proposes a Markov continuous random SSM (C-RSSM) for GaN-based buck converter. By using a random clock generator based on a Markov chain, it is able to redistribute the EMI spectra almost uniformly and continuously. In Section 4.3, a one-cycle on-time rebalancing scheme is utilized to avoid the jittering effect at the output node due to RSSM, balancing the design trade-off between EMI compression and output regulation. The system architecture with the proposed two techniques is introduced in Section 4.4. Also discussed in this section is a capacitive-coupled current sensor for peak current mode control. The chip is implemented in a 0.18-μm HV CMOS process. The experimental results are provided in Section 4.5 to verify the proposed design.

4.1 Design Challenges of Applying SSM Schemes in Switching Power Circuits

As addressed earlier, the high switching frequencies in GaN-based power circuits cause

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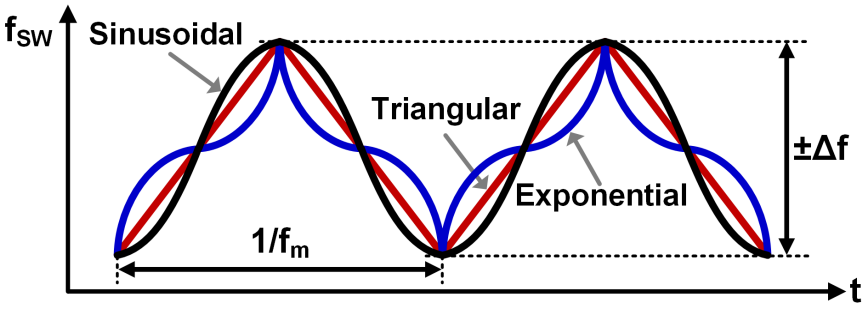
much higher current and voltage slew rates in the power stage, considerably contributing to the EMI emissions [Blank-15]. This would induce malfunctions and even safety risks in the electronic modules around the source. To prevent such scenarios, a variety of EMI standards, e.g. CISPR 25, are imposed to strictly limit the EMI values [Regan-04]. The electronic products must pass the compliance tests in the interested frequency range. Hence, to achieve the industry-wide adoption of GaN technology, it is essential to mitigate the EMI issue in fast-speed GaN-based switching power systems.

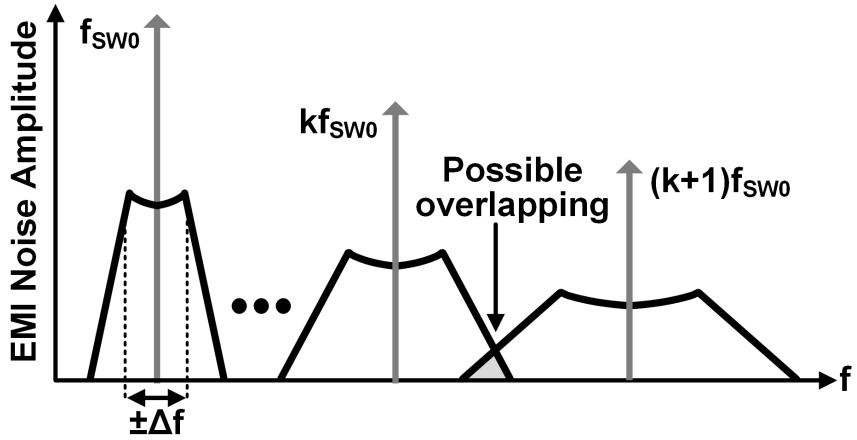
Spread-spectrum modulation (SSM) techniques have been demonstrated successfully in power converters to suppress the EMI generations [Gonzalez-07, Ho-10, Ke-17, Tao-11, Tse-02, Yang-18]. Traditionally, the power converters operate at constant frequencies, resulting in EMI noise concentrated at the switching frequency and its harmonics with notable peak values. On the other hand, the Carson's Rule [Carson-22] reveals that the total energy carried by a signal is not influenced by frequency modulation. Based on this, SSM techniques are thus developed and applied in switching power circuits. Instead of fixed-frequency switching, the SSM techniques distribute the switching frequency f_{SW} within a certain sideband. Thus, the EMI energy originally concentrating at the fundamental frequency and its harmonics is scattered into lower level. In [Gonzalez-07, Tse-02], periodic SSM (PSSM) approaches were explored by varying f_{SW} repetitively (following triangular, sinusoidal or exponential pattern), as illustrated in Figure 4.1(a). To characterize the performance, a modulation index m_f is defined and widely used:

$$m_f=\frac{\Delta f}{f_m}, \tag{4.1}$$

where Δf is the modulation range of f_{SW}, and f_m is the modulation frequency. Higher m_f results in lower peak EMI values. Thus, it is practical to improve EMI performance using either a lower f_m,



(a)



(b)

Figure 4.1. Conventional periodic SSM schemes: (a) repetitive modulation profiles, and (b) potential spectral overlapping.

or a higher Δf, or both. However, the variation ranges of both f_m and Δf are constrained strictly by several physical factors. First, to obtain reliable measurements, f_m is specified in the EMI standards [Deutschmann-13, Shepherd-12]. Particularly, f_m is required to be above the resolution bandwidth of the testing devices in peak detector value reading. Second, to void audible noise in applications, f_m should be larger than 20kHz which is the audible frequency. Third, Δf should be selected to ensure the loop stability of the switching power converter. Finally, increasing Δf might induce overlapping as shown in Figure 4.1(b), leading to counter effects on the EMI compression. Because of these reasons, PSSM techniques have limited EMI attenuation.

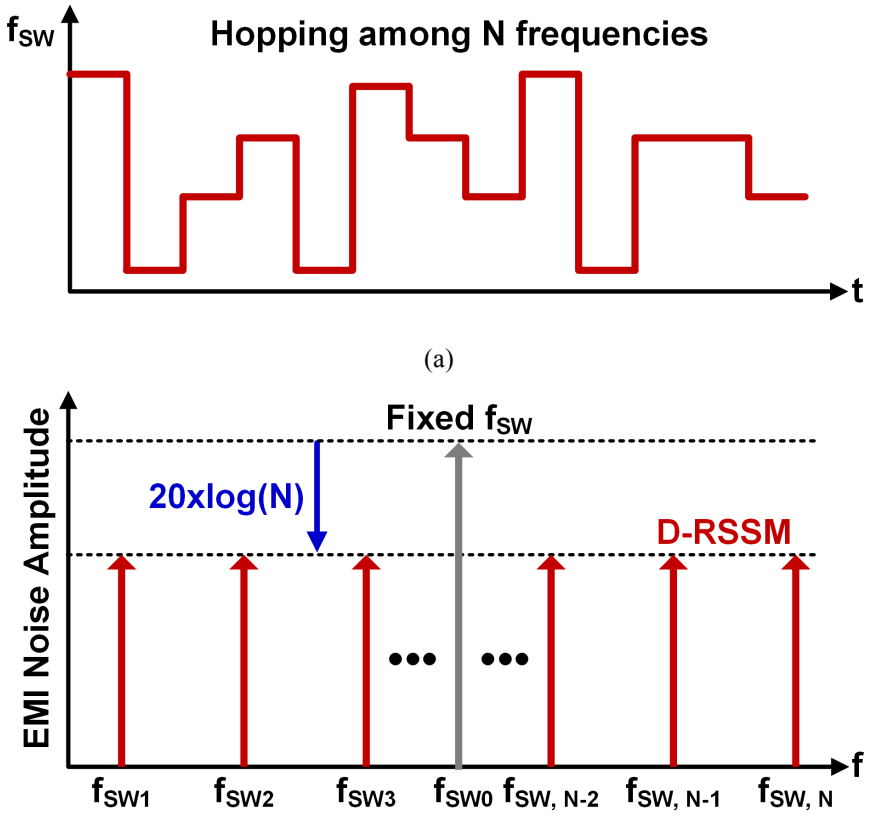


Figure 4.2. Conventional discrete RSSM (D-RSSM) technique: (a) frequency hopping within finite values, and (b) EMI spectral redistribution.

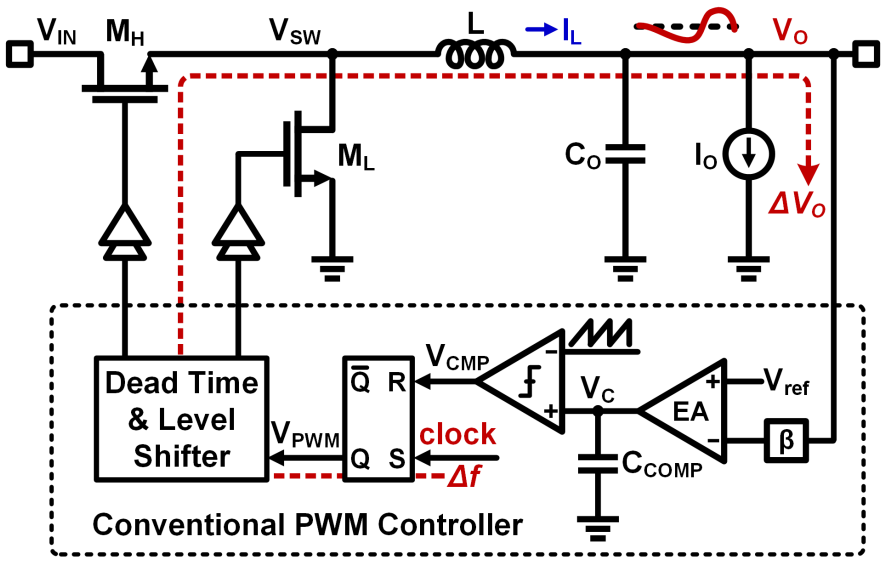
As an alternative, random SSM (RSSM) schemes are developed to improve the EMI attenuation. Rather than PSSM, RSSM modulates the switching frequency of a circuit in a random pattern. In this way, it thus scatters the EMI spectra almost evenly within the frequency dithering range, improving the EMI attenuation performance over the PSSM counterparts [Tse-02]. To fulfill the purpose of randomizing the switching frequency, it is critical to design an effective random clock generator. Traditionally, such a functional block is completed using digital circuits due to the simplicity [Tao-11, Yang-18], thus leading to a discrete RSSM (D-RSSM). As shown in Figure 4.2(a), assuming the switching frequency alters randomly among N values from f_{SW1} to

$f_{SW,\,N}$ with the same probability, then the spur at the original frequency f_{SW0} is distributed into N smaller ones. The EMI amplitude reduction (ΔEMI) can be related to the number N as below:

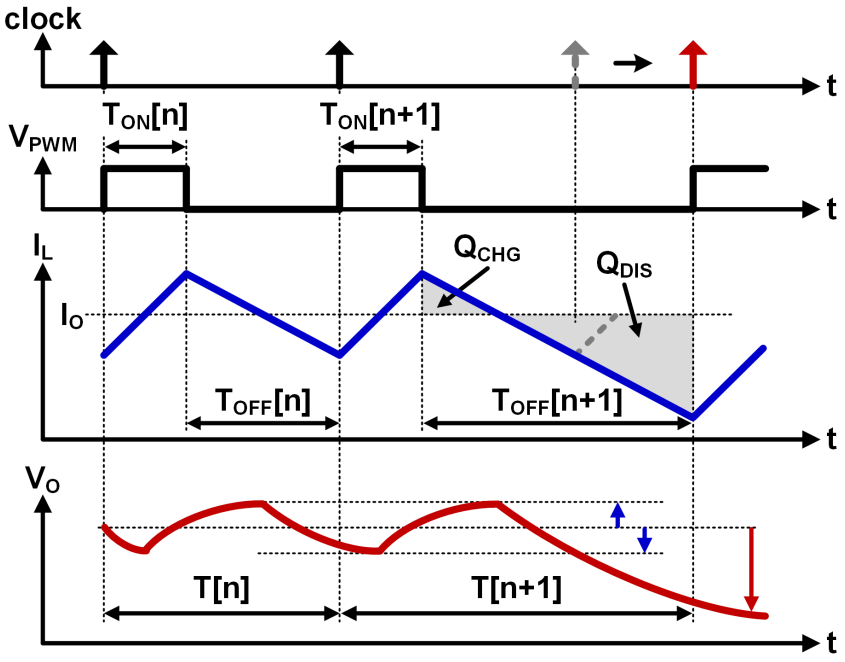
$$\Delta_{EMI}=20\times\log N\ (dB), \tag{4.2}$$

The EMI reduction can be controlled by tuning the number N. Higher N results in larger EMI attenuation. The main issue is the hardware and power consumption overhead, which is positively associated with the number N. To circumvent this issue, a thermal noise random clock generator, which captures thermal noise of semiconductor components as the random source, was reported [Ke-17]. It is intended to facilitate a continuous RSSM (C-RSSM) by generating the switching frequency in the analog domain. However, thermal noise heavily relies on the temperature and the noise range is quite difficult to predict. As the consequence, post signal processing becomes necessary to constrain the frequency modulation range for practical applications. Apparently, this makes it less attractive considering the circuit complexity and more importantly the degraded EMI attenuation performance.

As a design trade-off to the EMI attenuation when applying RSSM techniques, the output regulation of the switching power converter is degraded [Tao-11, Yang-18], which can be elaborated by referring to the operations of a buck converter as in Figure 4.3. By virtue of random frequency dithering, the operation period changes randomly from cycle to cycle, e.g. from T[n] to T[n+1], where n and n+1 represent the n^{th} and the subsequent cycle in respective. According to the control theory, the crossover frequency of the converter's feedback loop is designed much lower than f_{SW} considering the loop stability. Hence, the loop response lags far behind the frequency modulation. The consequence is T_{ON} remains the same even the switching cycle has altered ($T[n]\neq T[n+1]$). Thus, the inductor current I_L ramps in the same time interval. However, as



(a)



(b)

Figure 4.3. Illustration of degraded output regulation due to RSSM in (a) a buck converter with PWM control, and (b) jittering effect at the output node V_O.

shown in Fig. 4.3(b), T[n+1] is longer than T[n] in frequency modulation. In this case, the inductor L experiences a longer discharge phase over the previous one in T[n]. Consequently, the energy

stored in L is over discharged, deviating from the equilibrium and thus inducing an output voltage V_O damping. Similarly, with a shorter cycle of T[n+1] than T[n], the charge in the inductor cannot be released sufficiently, causing a temporary increasing of V_O. Seen from a long run, V_O would vary from the nominal value with a considerable high amplitude, degrading the regulation. This is referred to as V_O jittering effect. This problem can be partly solved using a larger output capacitor C_O. The downside is the deteriorated dynamic response of the converter. Moreover, it also induces larger PCB board area and higher system cost, which cancels out partly the benefits provided by fast operation in GaN-based power converters as aforementioned. Instead, a dedicated control scheme was developed to overcome this issue [Ho-10], but it suffers a limited performance and is only applicable for voltage mode power converters.

4.2 Markov Continuous RSSM

4.2.1. Mathematical Principle

As addressed earlier, to mitigate the finite frequency resolution existing in D-RSSM, it is essential to develop a proper C-RSSM scheme, which entails an analog random clock generator. This is usually achieved by measuring an intrinsically random physical process. However, such an approach suffers from the uncontrollable appearance of the random states. Alternatively, chaotic system characterized by Markov partition has been explored mathematically to develop an effective analog random source [Addabbo-06, Stojanovski-01]. Analyzed by Markov source state transition probabilities, the characteristic parameters can be optimized to shape the output distribution. Therefore, it is chosen in this work for random clock generation. Specifically, a random clock generator is designed based on a Markov chain, namely a chaotic piecewise-linear one-dimensional, or a PL1D map [Stojanovski-01], as described as:

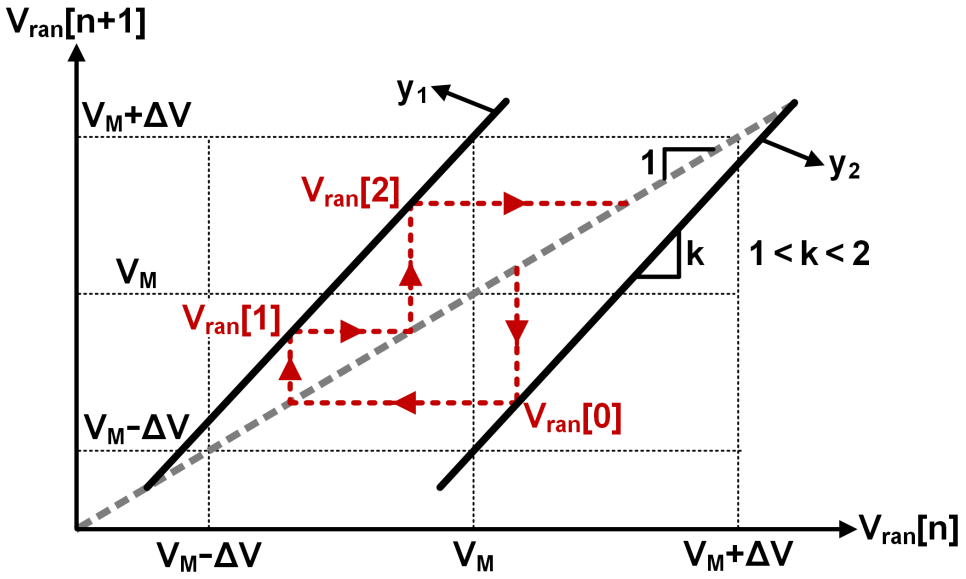


Figure 4.4. Chaotic piecewise-linear one-dimensional (PL1D) map for designing Markov-chain-based random voltage source.

$$V_{ran}[n+1]=\begin{cases} kV_{ran}[n]+[(1-k)V_M+\Delta V], & V_{ran}[n]<V_M \\ kV_{ran}[n]+[(1-k)V_M-\Delta V], & V_{ran}[n]\leq V_M \end{cases}. \quad (4.3)$$

Here, V_{ran} is the random output, V_M and ΔV are the central value and the variation boundary, respectively, and k represents the slope shared by the two lines. Such a chaotic dynamic system is further detailed intuitively in Figure 4.4. The state space is separated into two regions with V_M as the threshold, referred to as Markov partition. The boundary of the state space is constrained by defining ΔV. The stochastic property of the state transitions is determined by the value of k, which should locate in the range from 1 to 2 to ensure the generated states within the predefined state space [Stojanovski-01]. Meeting this requirement, k is preferable to be close to 2, benefitting the uniform distribution of the random states. It is worthy to note that the seed state $V_{ran}[0]$ needs to be initiated among the range of $[V_M-\Delta V, V_M+\Delta V]$. In this way, a random sequence $\{V_{ran}[n]\}$ can be generated automatically, which can be utilized for subsequent signal processing.

Mathematically, it can be proved that the state transitions of the sequence $\{V_{ran}[n]\}$ satisfy

the Markov character, presenting a complex and unpredictive behavior. In addition, based on the Equation (4.3), the state transition of V_{ran} is in the analog way. Hence, the value set of V_{ran} is analogous in the bounded voltage range. Thus, a boundless number of random states can be produced to tune the switching frequency. As the benefit, it conques the resolution issue in the discrete counterpart. Moreover, the boundary of the state space is constrained by $V_M - \Delta V$ and $V_M + \Delta V$, regardless of the random hopping. As a result, the dithering range can be limited precisely by properly defining both V_M and ΔV, without any impact on the random character. Beneficially, the proposed clock generator does not require any post signal processing as in the random clock generator based on thermal noise sensing, thus facilitating the improvement of the EMI attenuation without increasing the design efforts.

4.2.2 Design Consideration

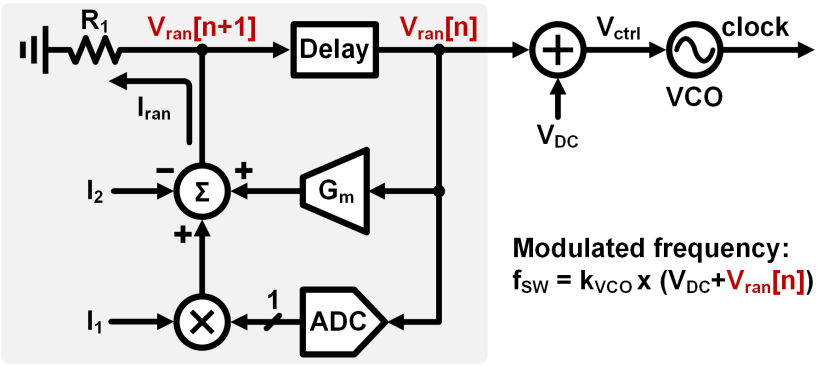


Figure 4.5. Block diagram of the proposed random clock generator based on Markov chain with fundamental analog modules.

From the design perspective, because the chaotic dynamic system is characterized in two linear equations, it can be conveniently designed using a standard CMOS process. Figure 4.5 illustrates the block diagram, employing five fundamental analog modules in addition to an output resistor R_1. Specifically, an analog-to-digital converter (ADC) is used to determine the region of

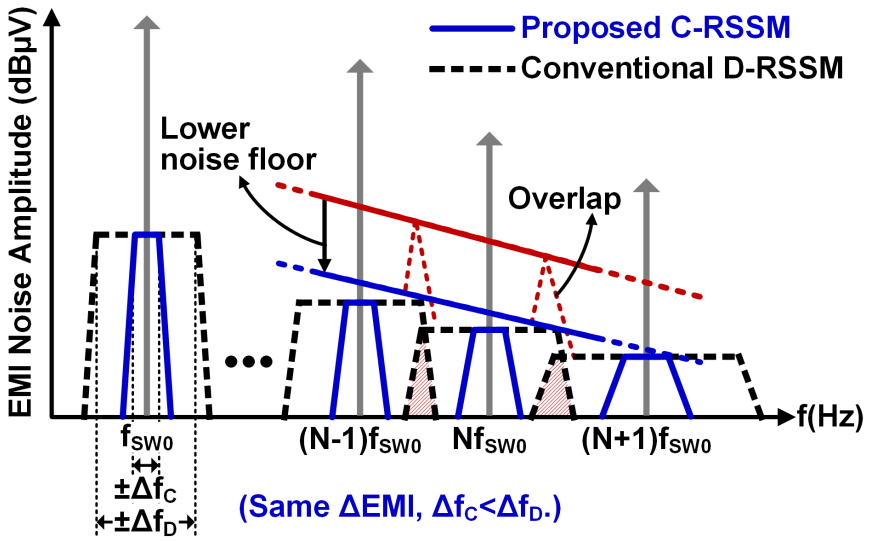


Figure 4.6. Illustration of the proposed Markov C-RSSM compared to D-RSSM.

$V_{ran}[n]$. Subsequently, the digital output of the ADC is quantized into the analog domain using a binary multiplying with a current I_1, thus completing the Markov partition. In this design, the order of the Markov partition is 2, only requiring a 1-bit ADC in the implementation. Thus, the circuits design is simplified. Further, assisted by a voltage-to-current converter (namely the G_m-cell in Figure 4.5), an adder realizes the fundamental operation of adding through current summation. As to defining the system characteristics in the Equation (4.3), the value of ΔV is determined by using a constant current I_2. Based on the operations illustrated in Figure 4.5, it can be derived that the intercepts of both lines in the Equation (4.3) are determined accordingly. Then, the random current I_{ran} crosses the resistor R_1, updating the random state to $V_{ran}[n+1]$. Apparently, the slop k in Equation (4.3) can be decided by choosing the values of R_1 and the transconductance G_m of the G_m-cell. After a sampling delay, the random state is relayed to the subsequent blocks as the voltage sequence $\{V_{ran}[n]\}$. From these discussions, the relations between the circuitry parameters (i.e. I_1, I_2, G_m and R_1) and the system ones (i.e. V_M, ΔV and k) can be derived as below:

$$\begin{cases} I_1=\dfrac{[(k-1)\times V_M+\Delta V]}{R_1} \\ I_2=2\times\dfrac{\Delta V}{R_1} \\ k=G_m\times R_1 \end{cases} . \quad (4.4)$$

Based on the Equation (4.4), the design parameters I_1, I_2 and R_1 can be determined in order to fully define the random state space. Meanwhile, by controlling the slope k, the stochastic property of the chaotic system can be optimized practically. One of the remarkable benefits of such a random source generation is that not only the random range but also the randomness of V_{ran} could be predefined conveniently with proper circuits design. The output V_{ran} of the random source is further relayed to the input of a voltage-controlled-oscillator or VCO, accomplishing the modulation of the switching frequency. By incorporating this random clock generator into power converter, it is capable of conducting SSM continuously and thus spreading the spurious noise at the central frequency and the harmonics evenly, satisfying the C-RSSM. As shown in Figure 4.6, in comparison with the conventional D-RSSM, the proposed Markov C-RSSM can reduce the peak EMI values comparatively but with a narrower modulation range ($\Delta f_C < \Delta f_D$). This leads to the advantage of avoiding the spectral overlapping in lower harmonics, significantly mitigating the noise floor elevation. Benefitting by C-RSSM, the EMI amplitude is compressed sufficiently while minimizing the elevation of the noise floor and the increasing of the silicon area.

4.2.3 Circuit Design

The key aspect of the proposed C-RSSM scheme is the random clock generator based on Markov chain, which is implemented as shown in Figure 4.7. To compute the next random state $V_{ran}[n+1]$, the present state $V_{ran}[n]$ is converted into a current I_{gm} by the G_m-cell. The transconductance G_m equals $1/R_2$. The current I_{gm} is then conducted into a summation node Σ. In

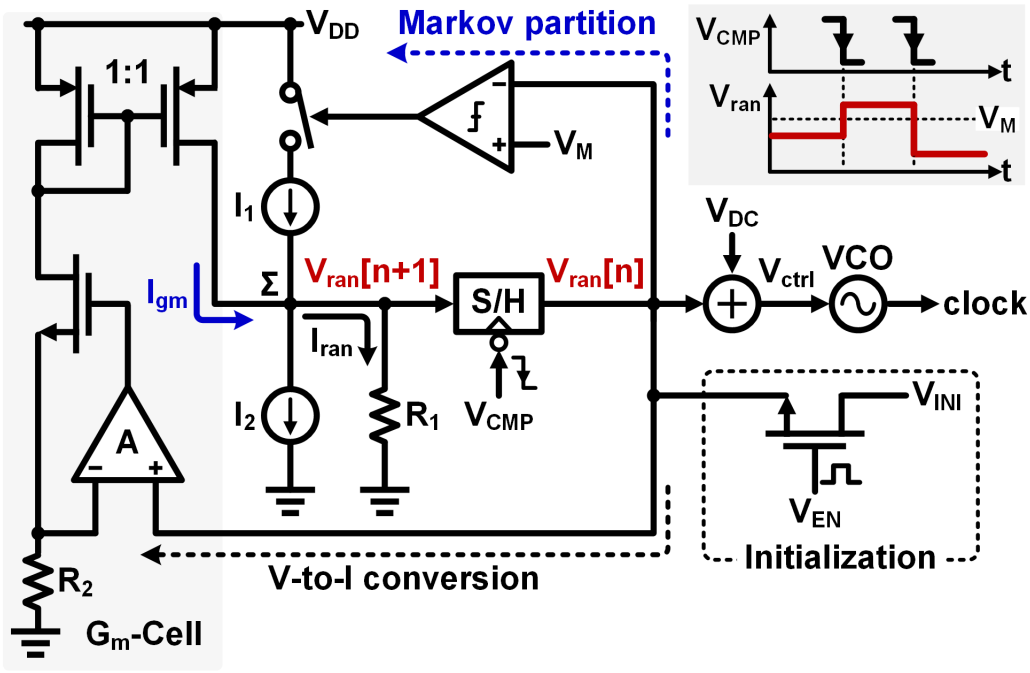
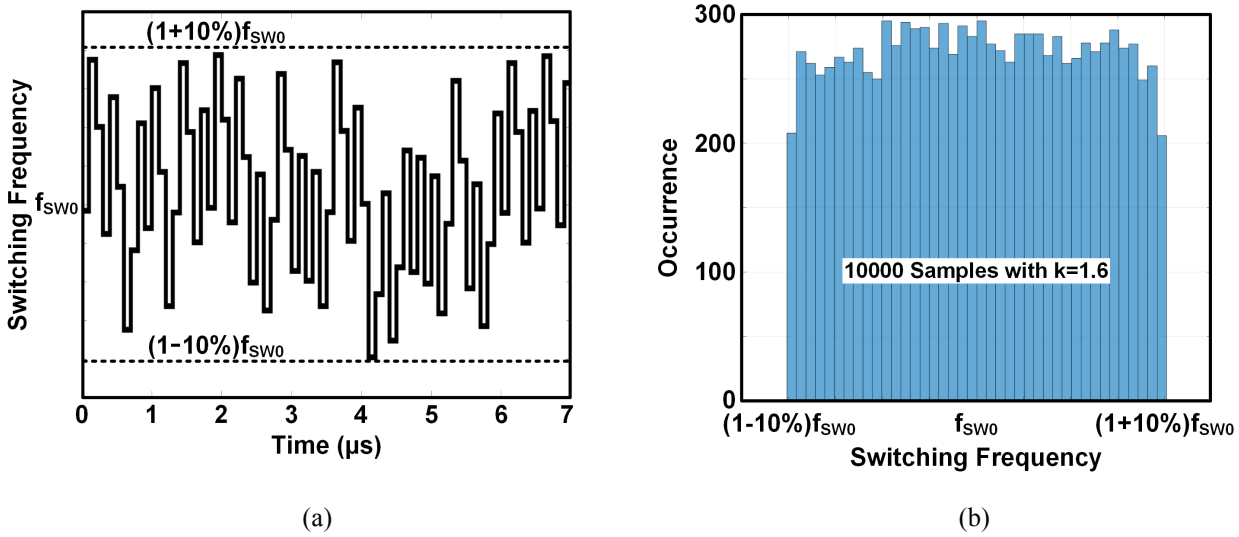


Figure 4.7. Circuit design of the proposed random clock generator based on Markov chain.

the meantime, $V_{ran}[n]$ is compared to V_M using a single comparator. The output of the comparator controls the current I_1 to implement the Markov partition. At last, a current sink I_2 is connected to the node Σ, generating the random current I_{ran}. This leads to the eventual random state $V_{ran}[n+1]$ ($=I_{ran}\times R_1$). The division of R_1 over R_2 determines the slope k in the Equation (4.3). Its range can be defined precisely through layout matching these two resistors, preventing the convergence issue. The updated state $V_{ran}[n+1]$ is delivered to the input of VCO, which happens at the falling transition of V_{CMP} from the PWM control loop. Correspondingly, the clock frequency is altered. Benefitting by Markov state transitions, V_{ctrl} varies randomly within $\pm\Delta V$ centered at ($V_{DC}+V_M$) and the switching frequency is modulated accordingly. In the practical design, the initial state of V_{ran} requires careful consideration as well in order to avoid the zero state after startup. To avoid this issue, $V_{ran}[n]$ is set up to an initial value, denoted as V_{INI}, when the circuits are powered on. As shown in Figure 4.4, V_{INI} is located within the desirable randomization range [$V_M-\Delta V$,

$V_M+\Delta V$]. From the simulations of the switching frequency f_{SW} modulation in time domain as shown in Figure 4.8(a), f_{SW} jumps stochastically but is limited within $f_{SW0}\pm\Delta f_C$, producing a random dithering profile in an analog manner. To circumvent the convergence problem of V_{ran} because of the PVT variations, the value of k is defined as 1.6. System-level simulations of the occurrences out of 10000 samples as shown in Figure 4.8(b) reveal an almost uniform distribution of the switching frequency. Thus, the EMI noise is redistributed evenly in the frequency domain.



(a) (b)

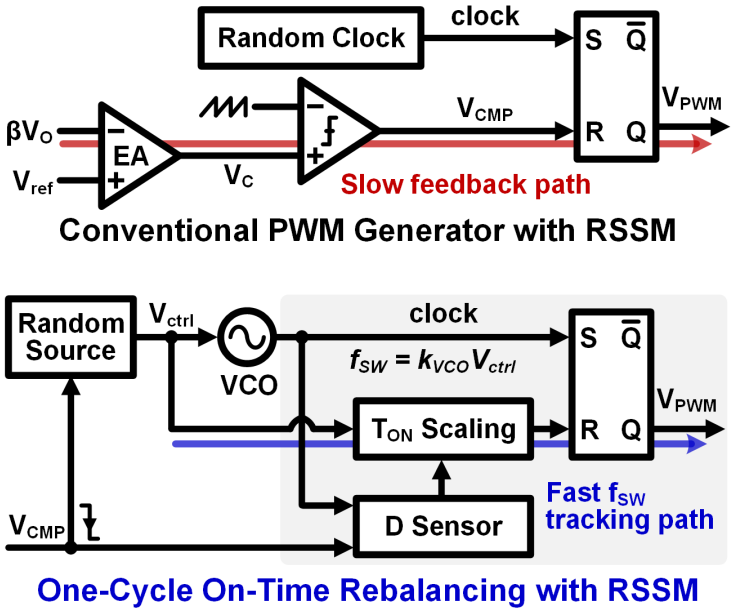
Figure 4.8. Simulations of the random clock generator based on Markov chain: (a) switching frequency deithering in time domain, and (b) switching frequency distribution.

4.3 One-cycle On-time Rebalancing

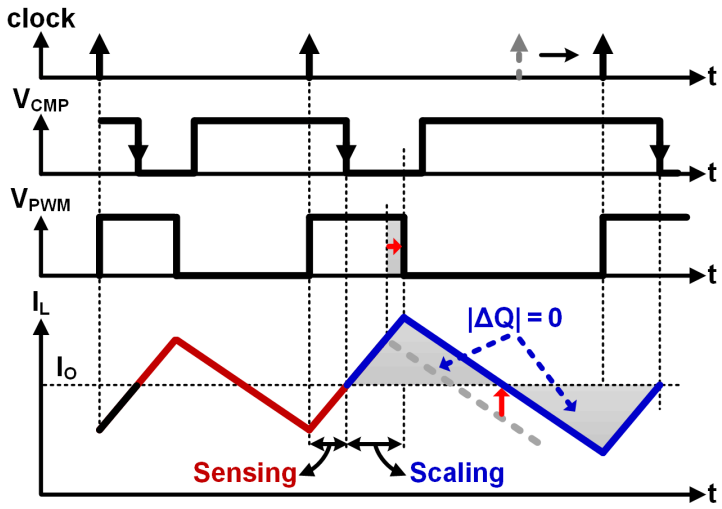
4.3.1. Design Principle

RSSM is beneficial for improving the EMI performance. However, it is worthy to note that this is at the cost of deteriorated output regulation, which can be analyzed from the control perspective in power conversion. Traditional controls, including both PWM and PFM schemes, are developed for constant f_{SW}. They can always generate a duty signal with a proper duty ratio D to regulate V_O tightly. However, this is not applied when RSSM scheme is employed because of

two reasons. One reason is that the regulation loop is not aware of the disturbance on D due to f_{SW} turning. Thus, it cannot correct the on-time T_{ON} in real time adaptively. The other one is that the loop response is slow, making the situation worse. To overcome the issue, a one-cycle on-time



(a)



(b)

Figure 4.9. One-cycle on-time rebalancing scheme: (a) block diagram, and (b) operation waveforms with random f_{SW} dithering.

rebalancing scheme is constructed to accommodate f_{SW} modulation, fundamentally removing the jittering effect at the output node without influencing EMI noise compression. Figure 4.9(a) reveals the structure. To circumvent the slow response encountered in the classic PWM control, an additional fast switching frequency (f_{SW}) tracking path is added to relay the instant f_{SW} for adaptive on-time adjusting. The basic principle can be detailed using Figure 4.9(b), which includes a two-step operation in each charge phase. Specifically, in the first phase, the instant D is detected using a sensor. In such a way, the output regulation is remained. Then, in the second phase, with the acquired values of D and f_{SW} from the random clock generator based on Markov chain, the T_{ON} scaling module tunes the on-time of the power converter dynamically. Therefore, T_{ON} and thus D of the power converter are rebalanced to the randomly altered f_{SW} in each cycle. The eventual benefit is preventing the jittering effect at the output node.

4.3.2 Circuit Design

The schematic of the one-cycle on-time rebalancing scheme is shown in Figure 4.10(a), consisting of three stages. More precisely, a phase detector is designed to achieve online duty-ratio D sensing by detecting the phase difference between the rising edge of the clock signal and the falling edge of V_{CMP}. Subsequently, a charge pump is connected for on-time T_{ON} scaling in adaptive to the instant f_{SW} that is controlled by the VCO input V_{ctrl}. Followed that is a PWM logic module to generate a proper duty signal V_{PWM}. The basic operation is revealed in Figure 4.10(b). From the introduction to the random clock generator based on Markov chain, the clock frequency is altered at the trailing edge of V_{CMP}. Hence, the converter's switching cycle is characterized by the falling edges of V_{CMP}. Two general such cycles, T[n] and T[n+1], are denoted in the operation waveforms to help understand the basic principle. A proportional equation is employed to denote

the relation with a coefficient α:

$$T[n+1]=\alpha\times T[n]. \tag{4.5}$$

In equilibrium, the on-time T_{ON} in a single charge phase is divided into t_{on1} and t_{on2} as

$$t_{on1}=t_{on2}. \tag{4.6}$$

The basic principle could be illustrated by investigating the operations during $t_{on2}[n]$ and $t_{on1}[n+1]$. The clock signal initiates V_{PWM} and $t_{on2}[n]$. The inductor current I_L then ramps up. Meanwhile, the phase detector sets V_{UP} to high, starting to charge C_{cp} with the current I_{UP}. Controlled by the VCO input $V_{ctrl}[n]$, I_{UP} is inversely proportional to T[n]. The $t_{on2}[n]$ is terminated until V_{CMP} triggers low by the feedback loop and then V_{UP} is reset to stop charging C_{cp}. Thus, the variation of the converted charge pump voltage ΔV_{cp} is derived as

$$\Delta V_{cp}=\frac{\gamma}{C_{cp}}\times\frac{t_{on2}[n]}{T[n]}. \tag{4.7}$$

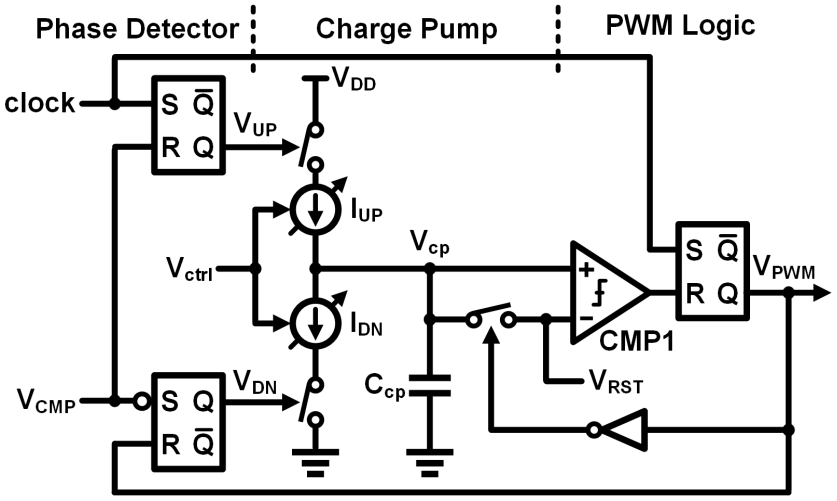
Here, γ represents the inverse proportionality constant of I_{UP} to the switching period T[n]. Further, using the Equation (4.6), the duty ratio in the n^{th} cycle, denoted as D[n], is computed as:

$$D[n]=2\times\frac{t_{on2}[n]}{T[n]}. \tag{4.8}$$

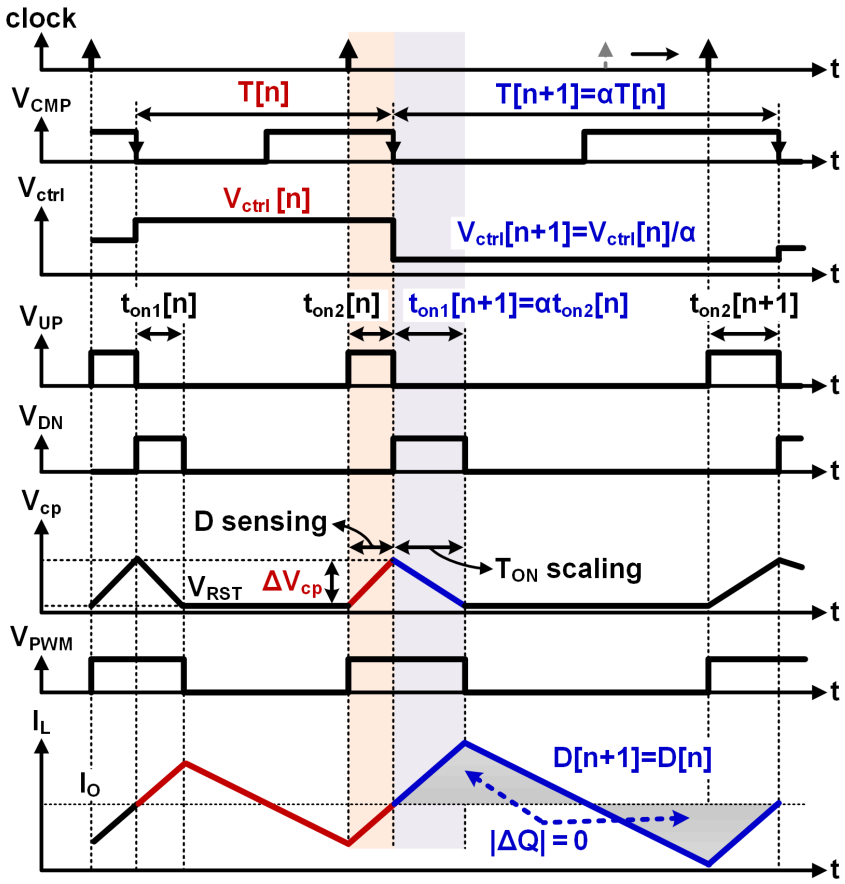
With the Equation (4.7) and (4.8), a linear relation between ΔV_{cp} and D[n] is determined as

$$\Delta V_{cp}=\frac{\gamma}{C_{cp}}\times 0.5\times D[n]. \tag{4.9}$$

Equation (4.9) suggests that D[n] is converted into the voltage variation ΔV_{cp}, implementing the D detection. The next cycle T[n+1] begins at the trailing edge of V_{CMP}. I_L ramps continuously as V_{PWM} remains high. I_{DN} is enabled in the meantime to discharge C_{cp}. As the falling edge of V_{CMP} updates the V_{ctrl} from $V_{ctrl}[n]$ to $V_{ctrl}[n+1]$, I_{DN} is proportional to 1/T[n+1]. As V_{cp} drops to V_{RST},



(a)



(b)

Figure 4.10. (a) Design, and (b) operation of the one-cycle on-time rebalancing scheme.

the comparator CMP1 in the PWM logic module flips to low, terminating $t_{on1}[n+1]$ and thus resetting V_{PWM}. According to the charge conservation of the capacitor C_{cp}, it leads to

$$t_{on1}[n+1]=\alpha\times t_{on2}[n]. \tag{4.10}$$

Further, the D value in the $(n+1)^{th}$ period can be considered as:

$$D[n+1]=2\times\frac{t_{on1}[n+1]}{T[n+1]}. \tag{4.11}$$

Combining the Equations (4.5), (4.8), (4.10) and (4.11), the relation below sustains generally:

$$D[n+1]=D[n]. \tag{4.12}$$

This equation implies that the D value of the converter is stabilized in each cycle regardless of the frequency dithering. Thus, the inductor charge is rebalanced.

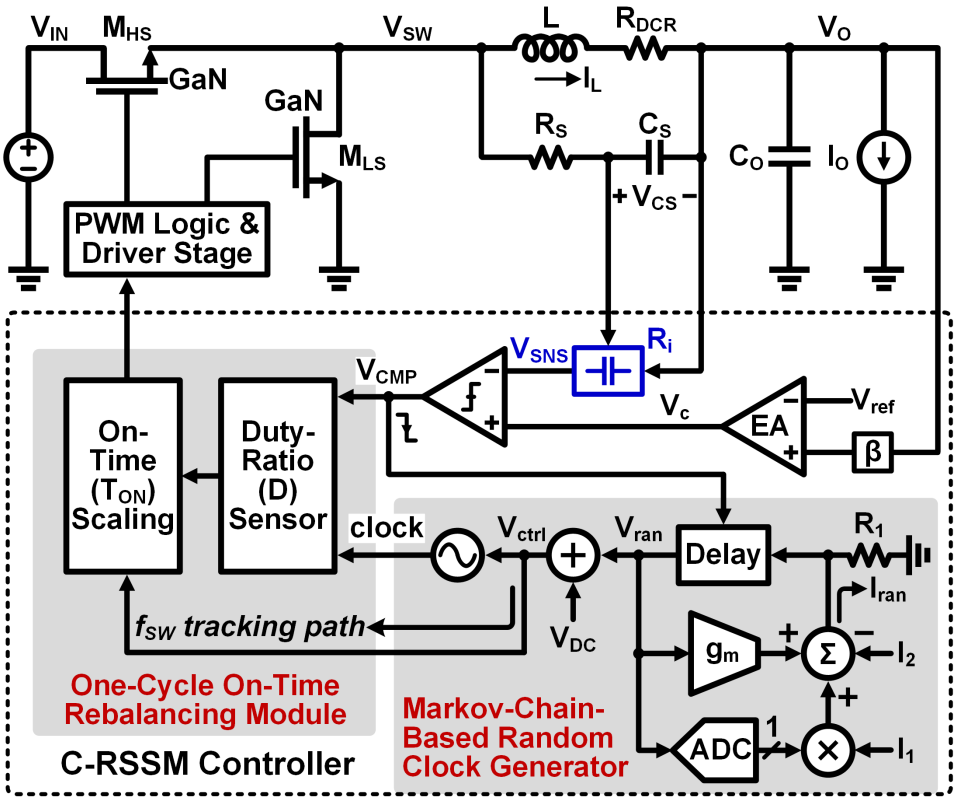


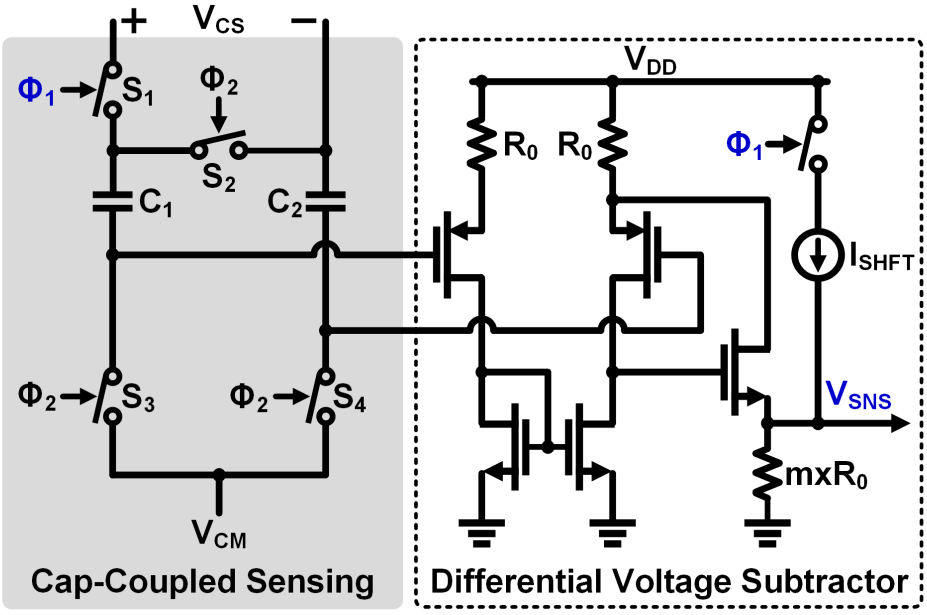
Figure 4.11. Block diagram of the GaN power system with C-RSSM control.

4.4 System Architecture

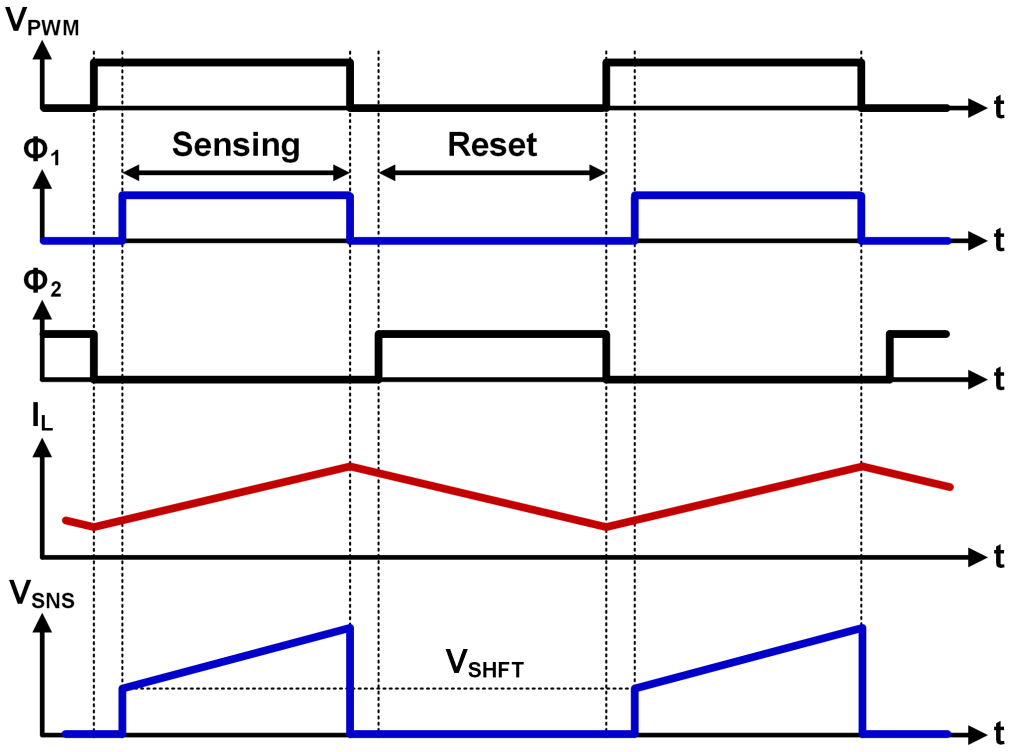
The proposed two schemes are incorporated into a buck converter, illustrated in Figure 4.11. The Markov-chain-based random clock generator replaces the traditional fixed-frequency clock generator, achieving analog switching frequency modulation within a range of $f_{SW0}\pm\Delta f_C$. Thereby, it spreads the EMI noise uniformly and continuously in the frequency domain. The one-cycle on-time rebalancing module supplants the classical PWM generator, eliminating the V_O jittering effect in the converter. Two enhancement-mode GaN HEMTs consist the power switches, namely M_{HS} and M_{LS}. For fast dynamic consideration, peak current mode control is employed in the design. A DCR current sensing strategy is used as shown in Figure 4.11. In the circuits, a RC filter, consisting of R_S and C_S, replicates the voltage difference across the direct-current resistance R_{DCR} of the inductor L. As a result, the voltage V_{CS} between C_S equals ($I_L\times R_{DCR}$) if the equation below is satisfied:

$$R_s\times C_S=\frac{L}{R_{DCR}}. \tag{4.13}$$

Then a current sensor R_i with high bandwidth is integrated on chip to implement the current sensing. The circuit design and operations are shown in Figure 4.12. An isolated sensing structure using capacitors [Herzer-09] is built to detect V_{CS} via the ac-coupling of C_1 and C_2. The acquired signal is further converted into a single-ended output V_{SNS} by a voltage subtractor. Using source follower as the input stage, the subtractor features fast operation. In practical design, a DC offset of V_{SHFT} is superimposed on V_{SNS} by a current denoted as I_{SHFT}, ensuring that V_{SNS} satisfies the operational range of the EA's output V_C. This is because V_{SNS} is compared to V_C in the control loop for V_O regulation. The operations are clearly illustrated in the waveforms. In more detail, the duty signal V_{PWM} flips to high, turning on the GaN power HEMT M_{HS}. This initialize the charge



(a)



(b)

Figure 4.12. (a) Design, and (b) operation of the capacitive-coupled peak current sensor.

phase. As a result, the current I_L begins to rise. Among such a period, the switch S_1 in the insolated coupling stage is connected whereas S_2, S_3 and S_4 are open, detecting the voltage V_{CS}. Once the charge phase ends, V_{PWM} flips low and M_{HS} switches off. Meanwhile, it issues a signal to disconnect S_1. The other three switches S_2, S_3 and S_4 are closed, terminating the sensing function. Consequently, both the top plates of C_1 and C_2 are connected to the output and their bottom plates are reset to a common reference V_{CM}. This determines the common-mode input of the voltage subtractor as V_{CM}. As it is independent of V_O, the current sensor can support a wide output range.

4.5 Experimental Verification

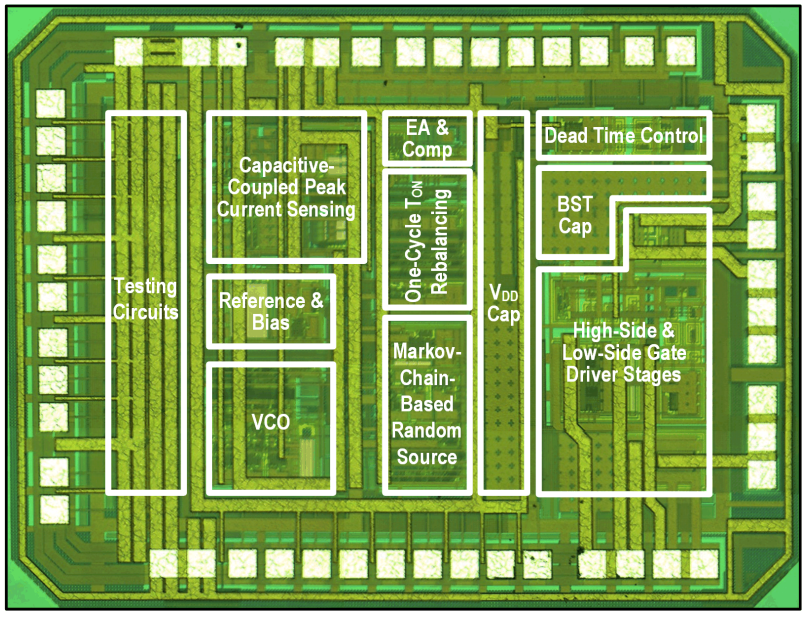
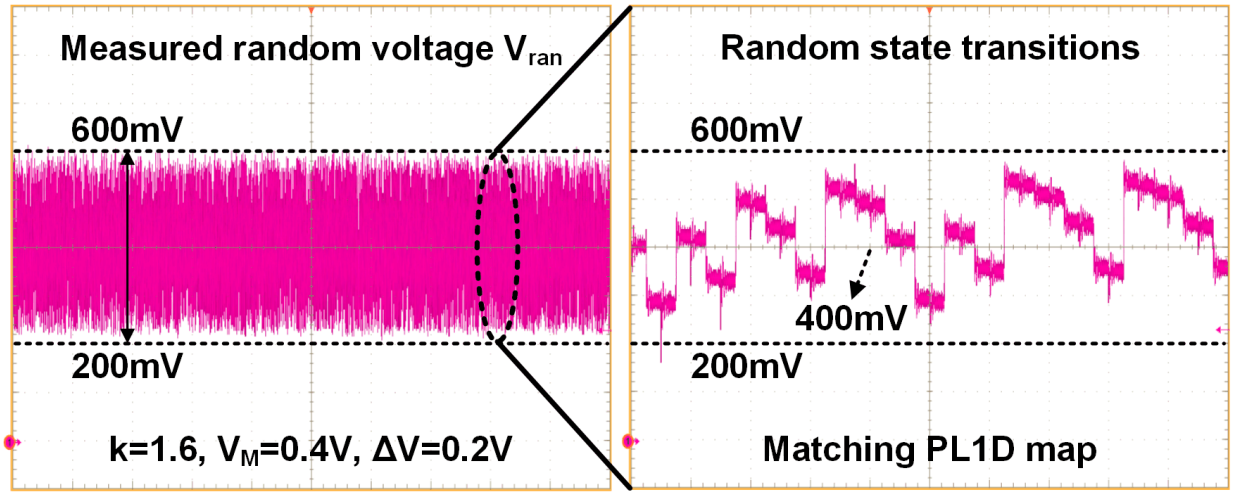


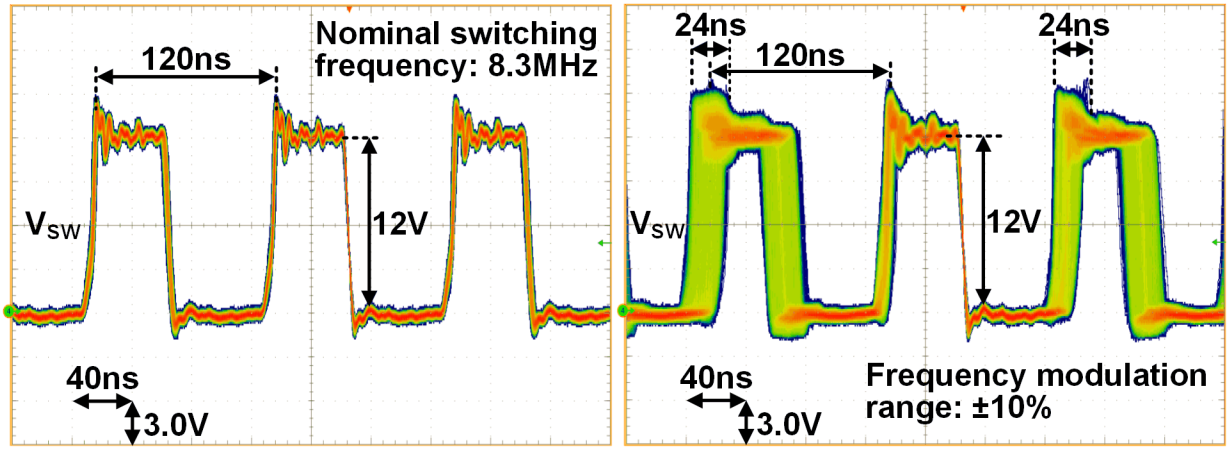
Figure 4.13. Chip micrograph.

The design was implemented in a 0.18μm HV CMOS process [Chen-19b, Chen-19c]. The chip photo is provided in Figure 4.13. The effective area is 1.54mm^2. The area of the random clock generator based on Markov chain is 0.08mm^2. Two E-mode GaN HEMTs are soldered on board as the power semiconductor devices for measurements. The designed power system supports a



(a) (b)

Figure 4.14. Measured random voltage V_{ran} in the random clock generator based on Markov chain: (a) state space boundary, and (b) state transitions.

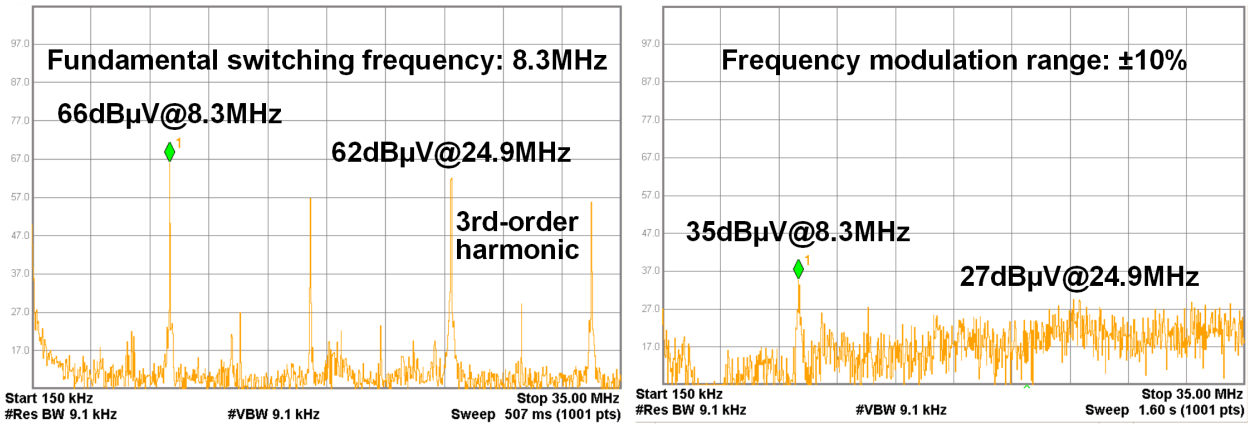


(a) (b)

Figure 4.15. Measured waveforms at the switching node V_{SW}: (a) without, and (b) with the Markov C-RSSM scheme.

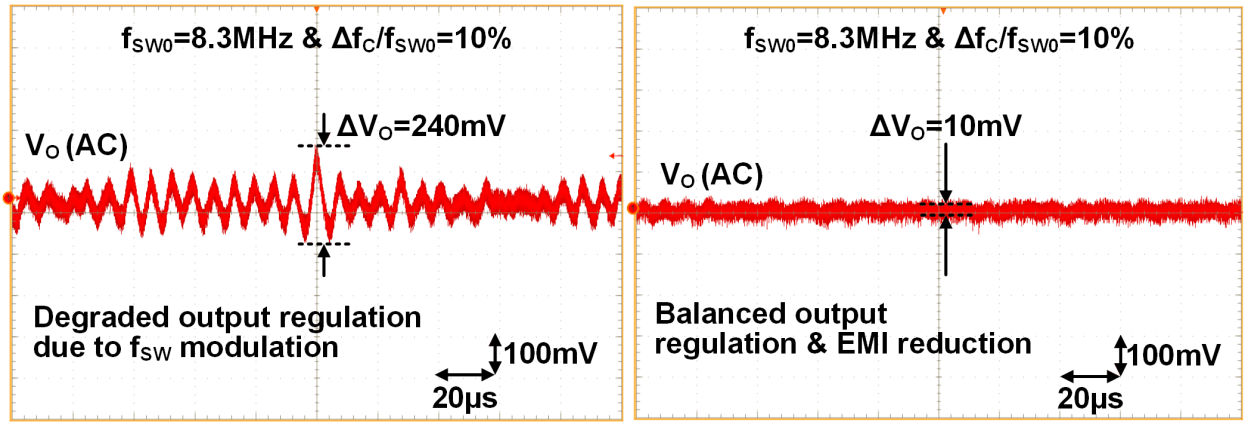
maximum I_O of 1.5A and a broad range of input from 3V to 40V.

To demonstrate the effectiveness of the random generator with Markov character, the output V_{ran} of the random source is measured as shown in Figure 4.14. In consistence with the simulations, V_{ran} changes within the defined state space with a boundary of 200mV and 600mV.



(a) (b)

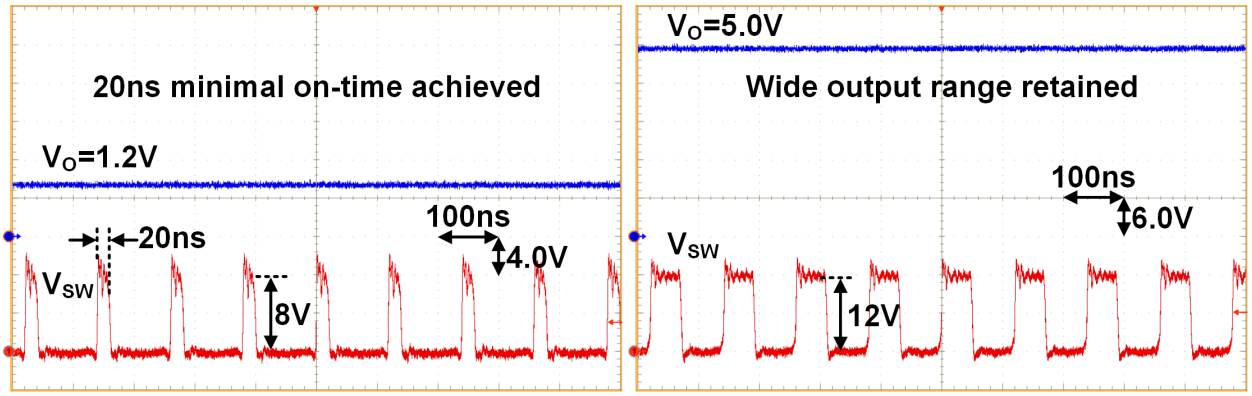
Figure 4.16. Measured conducted EMI in the frequency range below 30MHz: (a) without, and (b) with the Markov C-RSSM scheme.



(a) (b)

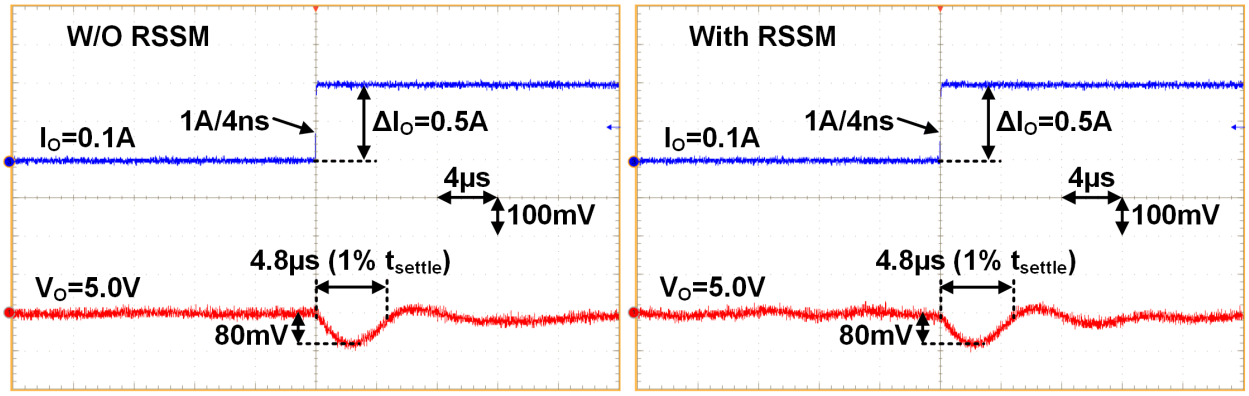
Figure 4.17. Measured jittering effect at the output node when applying RSSM with (a) classical PWM scheme, and (b) designed one-cycle on-time rebalancing methodology.

Its transient behavior matches the dynamic system depicted in Equation (4.3). The measured V_{SW} waveforms are provided in Figure 4.15. With Markov C-RSSM scheme, the switching frequency is tuned within the boundary of (1±10%)×8.3MHz. To verify the noise attenuation by C-RSSM, the conducted EMI noise is measured using a line impedance stabilization network (LISN) that is inserted between the input power supply and power switch M_{HS}. The LISN couples and relays the input voltage ripple to a spectrum analyzer for characterizing. The EMI spectra are given in



(a) (b)

Figure 4.18. Measured switching node V_{SW} with reference to variable output voltages: (a) V_O=1.2V, and (b) V_O=5.0V.



(a) (b)

Figure 4.19. Measured dynamic performance of the power converter with load current rising: (a) without, and (b) with the proposed Markov C-RSSM.

Figure 4.16 when the V_{IN} is equal to 12V and load current I_O is 1A at a V_O of 5V. Compared to the classical PWM operation under fixed frequency, the Markov C-RSSM scheme compresses the peak value of the EMI spectra by 31dBµV at the frequency of 8.3MHz and 35dBµV at the frequency of 24.9MHz.

To demonstrate the one-cycle on-time rebalancing scheme, the jittering effect at the output node V_O is measured as shown in Figure 4.17. Under the traditional PWM control, the maximum amplitude of the jittering effect at the output node is as high as 240mV. The proposed one-cycle

on-time rebalancing scheme suppresses the jittering to less than 10mV, satisfying the design.

Figure 4.18 gives the routine switching waveforms with various V_{IN} and V_O values to reveal the fundamental regulation performance of the conversion system. By virtue of the high-bandwidth isolated current sensor, the system is able to operate normally at a minimal T_{ON} of 20ns. Note that this is achieved with peak current mode control. The current sensor has an independent common-mode input range of V_O, facilitating a broad range of V_O from 1.2V to 5.0V.

The dynamic performance of the system is measured as in Figure 4.19 when the load current rises in a 500mA amplitude. As measured, the 1% settling time t_{settle} of the converter is 4.8μs with a peak undershoot voltage of 80mV. These results have slight differences from those when the converter works under fixed frequency of 8.3MHz. From these measurements, it can be concluded that the C-RSSM possesses a negligible impact on the dynamic performance. The peak conversion efficiency is 86.8% with 1.25A load current as revealed in Figure 4.20. The efficiency discrepancy due to C-RSSM is lower than 0.6%.

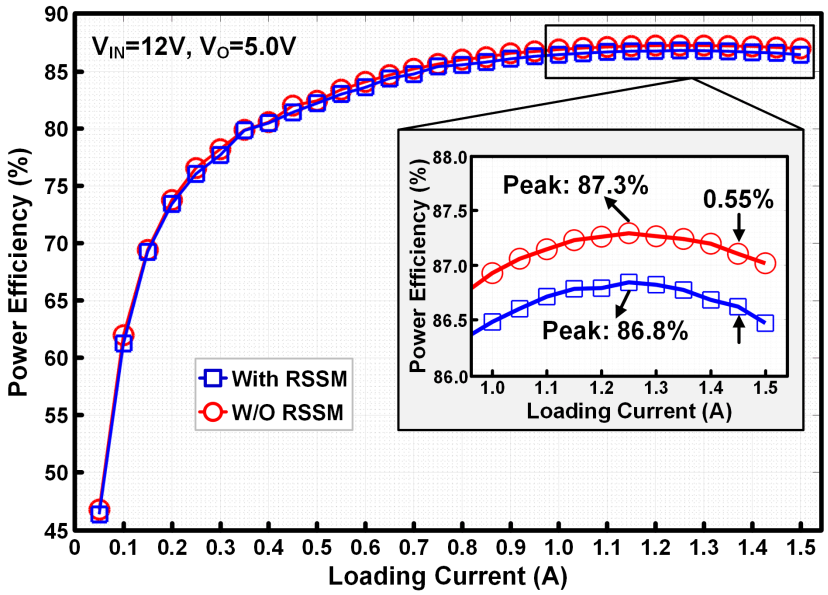


Figure 4.20. Measured efficiency.

Finally, the performance comparisons are listed in Table 4.1. To achieve the same spurious noise compression of 35dBμV, the proposed Markov C-RSSM approach reduces the frequency dithering range by half over the D-RSSM counterpart in [Yang-18]. This leads to a 53% less die area of the analog random clock generator over the digital implementation. Meanwhile, the design here demonstrates a 119% higher EMI compression and 3 times larger jittering effect mitigation at the output node, in comparison with the C-RSSM technique in the reference of [Ho-10].

Table 4.1. Performance comparison

Design		Yang-18	Ke-17	Ho-10	This Work
Process		55nm CMOS	0.35μm HV BCD	0.35μm HV BCD	0.18μm HV CMOS
Power Switch		MOSFET	GaN HEMT	MOSFET	GaN HEMT
Control Mode		Hysteresis current mode	PWM voltage mode	PWM voltage mode	PWM current mode
Central Switching Frequency		1MHz	10MHz	1MHz	8.3MHz
Frequency Modulation Way		Discrete RSSM	Triangular modulation	Continuous RSSM	Continuous RSSM
Random Clock Generator Area		($0.17mm^2$)[1]	Not reported	Not reported	$0.08mm^2$
Frequency Modulation Range		-21%/+22%	±9%	±20%	±10%
Peak EMI Attenuation		35dBμV	33dBμV	16dBμV	35dBμV
V_O Jittering Reduction	Amplitude	Not reported	Note reported	18.1dB	>27.6dB
	Method	Pseudo hysteretic window	Not reported	Ramp compensation	One-cycle on-time rebalancing

[1] Estimated through the chip photo

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In the past half century, the operation speed of the switching power circuits has been improved continuously benefiting from the advances of power devices and control circuits. As the silicon power devices are approaching the fundamental limit of performance, GaN HEMTs sustain the frequency evolution trend by virtue of their superior specific on-resistance. Specifically, they enable the power converters efficiently switch at or even beyond 10MHz. High switching frequency brings about several key advantages. It fundamentally extends the crossover frequency of the converter, improving the dynamic response. Besides, it allows the use of small passives for power delivery, miniaturizing the system size and reducing the overall cost. However, fast switching also induces serious challenges which need to be tackled for the wide applications of GaN technology. First, due to the unique device structure and conduction mechanisms, GaN HEMTs face device- and circuit-level reliability issues, such as *i*-collapse effect and accelerated aging process. Second, fast switching actions generate severe EMI noise, degrading the system performance and even inducing safety problems. Third, the inherent power design trade-offs present more design challenges on achieving optimum solutions. For even worse, the high frequency operation intensifies these compromises. To overcome these challenges, innovations are conducted to facilitate the development of high-frequency GaN-based DC-DC power conversation, featuring high reliability, low EMI and balanced system performance.

In order to improve the GaN reliability, an online condition monitoring is developed to prognose the *i*-collapse caused failure in GaN switch by sensing its dynamic on-resistance as the

aging precursor. Since the dynamic on-resistance is sensitive to the junction temperature of the GaN switch, a gate leakage inspired, cross-die junction temperature sensor is designed to facilitate the remove of temperature effect on the aging precursor. A remote sensing methodology is developed to achieve a non-intrusive detection. Further, a proactive temperature frequency scaling scheme is employed to modulate the operation speed of the GaN switch at high thermal stress, thus extending the device life span. These techniques are incorporated in a GaN-based buck converter, which is implemented in a 0.18-μm HV CMOS process. It switches at 10MHz with an input range from 5V to 40V and an output range from 3.3V to 5V over the temperature range from 0°C to 125°C. The measurements prove that the monitoring accuracy is improved by 19 times with the junction-temperature-independent condition monitor. The temperature frequency scaling scheme reduces the junction temperature of GaN power device by 16°C with a typical GaN junction-to-ambient thermal resistance of 82°C/W.

To balance the classic design trade-off between EMI noise and power efficiency, a closed-loop EMI regulation technique is developed for GaN DC-DC power conversion. Through shaping the switching behaviors of GaN power switch, it reduces the conducted EMI noise while the power efficiency degradation is minimized. To reach this goal, an emulated Miller Plateau tracking scheme is invented to sense the Miller Plateau voltage cycle by cycle, independent of the load current and input voltage. By sensing the switching node voltage during the current freewheeling period, the Miller Plateau voltage is thus replicated precisely. In the implementation, a low-power negative voltage sensor is designed to avoid the potential latch-up issue. Two items are generated dynamically to compensate the errors due to the asymmetrical GaN device structure and channel length modulation effect, respectively, ensuring the emulation accuracy. Further, based on such an

advanced detection method, an adaptive strength gate driving scheme is developed to implement the individual control of low di/dt and high dv/dt. In more detail, a noise-isolated feedback link is designed based on timing control to achieve a closed-loop control, mitigating the long delay time issue in conventional open loop methodology. A prototype chip of GaN-based buck converter was manufactured in a 0.35-μm BCD process. Two enhancement-mode GaN HEMTs are used as the power switches for testing. The implemented converter switches at 10MHz with a wide input range from 5V to 40V. The measurements demonstrate that the proposed design reduces the peak EMI noise by 19dBμV under 30MHz and 9dBμV from 30MHz to 3GHz, while degrading the power efficiency by only 2.44%.

To attenuate the EMI noise further, a continuous random spread-spectrum-modulation (C-RSSM) scheme is developed. By using a Markov-chain-based random clock generator, it is able to distribute the EMI spectra continuously and almost uniformly, reducing the EMI noise effectively while with minimum noise floor elevation and die area overhead. A GaN-based buck converter with peak current mode control is designed as a platform to verify the proposed design. In the meantime, a one-cycle on-time rebalancing control is presented to stabilize the duty ratio, regardless of the frequency variation due to C-RSSM. Thus, the output jittering effect of the converter is mitigated, optimizing the design trade-off between EMI and output regulation. The proposed controller was implemented in a 0.18-μm HV CMOS process, controlling two GaN HEMTs for power delivery. The converter operates at a nominal frequency of 8.3MHz. When the switching frequency varies within a range of ±10%, the measured EMI noise is reduced by 31dBμV at the fundamental frequency and 35dBμV at the third-order harmonic. The one-cycle on-time rebalancing scheme reduces the output jittering amplitude from 240mV to 10mV.

In this research, all the proposed solutions to the gate driver, control scheme and power stage have been fabricated and measured successfully. Their effectiveness has been successfully demonstrated by the measurements. All these lead to the conclusion that the high-frequency GaN-based DC-DC power conversion has been accomplished successfully with high reliability, low EMI and balanced system performance.

5.2 Future Work

This work has provided the groundwork to address various design challenges in high-frequency and high-performance GaN-based DC-DC converters. Based on these works, the future research directions can be navigated into the areas as follows: autonomous aging prediction through online data collection and machine learning, smart gate driving and control for precise regulation on EMI amplitude, and monolithic GaN power converter.

The device variations of GaN power switches necessitate the calibration for each sample when prognosing the aging conditions. To eliminate such a tedious step, autonomous condition prediction through machine learning is favorable. The online aging precursor detection and cross-die junction temperature sensing as addressed in this research can be used for data collection. The collected data are further delivered to a machine learning agent for aging model training. Such training procedure can be continued during the whole device lifetime. Based on the trained model, the aging condition can be predicted. In such a means, the device variations are absorbed by each specific model, achieving a self-aging prediction.

Before entering the market, the switching power circuits have to pass a variety of EMI standards. Currently, trial-and-error is the common way to solve this problem. However, such an iterative approach consumes considerable time and inevitably prolongs the time to market of the

product, increasing the cost and cutting down the revenue. With the already developed adaptive strength gate driving and C-RSSM, a smart control scheme can be developed further to precisely regulate the EMI emission to exactly fulfill the requirements. Specifically, with the emulated Miller Plateau tracking scheme, the di/dt period during the switching transition of the power switch can be identified. Based on such timing information, the conducted EMI amplitude can be further determined by sensing the voltage ripple at the input line. This acquired EMI value is compared to the reference defined in the standard, generating a control signal to modulate the driving strength and frequency dithering range. Eventually, the EMI noise can be always regulated to right at the required value.

Lastly, to fulfill the promise by the GaN technology, it is highly desirable to accomplish monolithic GaN power converters. In these systems, both the controller and power stage are implemented in GaN process. Consequently, the delay times in the control circuits and driver stages would be reduced significantly, removing the last bottleneck of developing very-high-frequency (VHF) switching power circuits. However, the issues related to EMI, reliability and design trade-offs still exit. Thus, the proposed techniques in this research can be leveraged and implemented for high-performance monolithic GaN DC-DC converters.

REFERENCES

[Addabbo-06] T. Addabbo, M. Alioto, A. Fort, S. Rocchi and V. Vignoli, "A feedback strategy to improve the entropy of a chaos-based random bit generator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 2, pp. 326-337, Feb. 2006.

[ADI-89] Analog Devices, Linear Technology – LT1070/LT1071, "5A and 2.5A high efficiency switching regulators," Datasheet, 1989.

[Baliga-88] B. J. Baliga, "Evolution of MOS-bipolar power semiconductor technology," *Proceedings of the IEEE*, vol. 76, no. 4, pp. 409-418, April 1988.

[Baliga-10] B. J. Baliga, "Advanced power MOSFET concepts," Springer, 2010.

[Baliga-13] B. J. Baliga, "Gallium nitride devices for power electronic applications," *Semicond. Sci. Technol.*, vol. 28, no. 7, Jun. 2013, Art. no. 074011.

[Baliga-19] B. J. Baliga, "Fundamentals of power semiconductor devices," 2nd Ed. Springer, 2019.

[Bahl-16] S. R. Bahl, J. Joh, L. Fu, A. Sasikumar, T. Chatterjee and S. Pendharkar, "Application reliability validation of GaN power devices," in *IEEE International Electron Devices Meeting* (*IEDM*), San Francisco, CA, 2016, pp. 20.5.1-20.5.4.

[Blanchard-88] R. A. Blanchard, "Method for making planar vertical channel DMOS structures," US Patent 4,767,722, Aug. 1988.

[Blank-15] M. Blank, T. Glück, A. Kugi and H. Kreuter, "Digital slew rate and S-shape control for smart power switches to reduce EMI generation," *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5170-5180, Sept. 2015.

[Broeck-19] C. H. van der Broeck, L. A. Ruppert, R. D. Lorenz and R. W. De Doncker, "Methodology for active thermal cycle reduction of power electronic modules," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 8213-8229, Aug. 2019.

[Brown-90] M. Brown, "Practical switching power supply design," Academic Press, 1st Ed., pp. 17-17, 1990.

[Cai-17] Y. Cai, A. J. Forsyth and R. Todd, "Impact of GaN HEMT dynamic on-state resistance on converter performance," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 1689-1694.

[Cappello-18] T. Cappello, A. Santarelli and C. Florian, "Dynamic R_{ON} characterization technique for the evaluation of thermal and off-state voltage stress of GaN switches," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3386-3398, April 2018.

[Carson-22] J. R. Carson, "Notes on the theory of modulation," *IEEE Proc. Institute of Radio Engineers*, vol. 10, no. 1, pp. 57-64, Feb. 1922.

[Chen-17] Y. Chen, X. Ke and D. B. Ma, "A 10MHz 5-to-40V EMI-regulated GaN power driver with closed-loop adaptive miller plateau sensing," in *IEEE Symposium on VLSI Circuits*, Kyoto, 2017, pp. 120-121.

[Chen-19a] Y. Chen and D. B. Ma, "A 10MHz *i*-Collapse Failure Self-Prognostic GaN Power Converter with T_J-Independent In-Situ Condition Monitoring and Proactive Temperature Frequency Scaling," in *IEEE International Solid-State Circuits Conference* (*ISSCC*), San Francisco, CA, USA, 2019, pp. 248-249.

[Chen-19b] Y. Chen and D. B. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle T_{ON} rebalancing for 27.6dB V_O Jittering Suppression," in *IEEE International Solid-State Circuits Conference* (*ISSCC*), San Francisco, CA, USA, 2019, pp. 250-252.

[Chen-19c] Y. Chen and D. Ma, "EMI-Regulated GaN-Based Switching Power Converter with Markov Continuous Random Spread-Spectrum Modulation and One-Cycle On-Time Rebalancing," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3306-3315, Dec. 2019.

[CISPR-16] CISPR, CISPR 25:2016, fourth edition. Oct. 2016. [Online]. Available: https://webstore.iec.ch/publication/26122.

[Consoli-96] A. Consoli, S. Musumeci, G. Oriti and A. Testa, "An innovative EMI reduction design technique in power converters," *IEEE Transactions on Electromagnetic Compatibility*, vol. 38, no. 4, pp. 567-575, Nov. 1996.

[Deboy-98] G. Deboy, N. Marz, J. -. Stengl, H. Strack, J. Tihanyi and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," in *International Electron Devices Meeting* (*IEDM*), San Francisco, CA, USA, 1998, pp. 683-685.

[Deutschmann-13] B. Deutschmann, "Spread spectrum clocking for emission reduction of charge pump applications," in *International Workshop on Electromagnetic Compatibility of Integrated Circuits* (*EMC Compo*), Nara, 2013, pp. 123-128.

[Dusmez-16] S. Dusmez, M. Bhardwaj, L. Sun and B. Akin, "In situ condition monitoring of high-voltage discrete power MOSFET in Boost converter through software frequency response analysis," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7693-7702, Dec. 2016.

[EIA-19] U.S. Energy Information Administration (EIA), U.S. Energy Facts Explained. Apr. 2019. [Online]. Available: https://www.eia.gov/energyexplained/us-energy-facts/.

[EPC-19] Efficient Power Conversion (EPC), EPC8009, Enhancement Mode Power Transistor Datasheet. June 2019. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC8009_datasheet.pdf.

[FCC-19] FCC, Electronic Code of Federal Regulations, Title 47, Chapter I, Subchapter A, Part 15, Subpart B –Unintentional Radiators, Section 15.107, Conducted limits. Dec. 2019. [Online]. Available: https://www.ecfr.gov/cgi-bin/text-idx?SID=67d6b185b7d98e2a4bca2aafdefd8193&mc=true&node=sp47.1.15.b&rgn=div6.

[Gonzalez-07] D. Gonzalez *et al*., "Conducted EMI reduction in power converters by means of periodic switching frequency modulation," *IEEE Transactions on Power Electronics*, vol. 22, no. 6, pp. 2271-2281, Nov. 2007.

[Guz-18] M. Guz *et al*., "IEEE ITRW working group position paper-system integration and application: gallium nitride: identifying and addressing challenges to realize the full potential of GaN in power conversion applications," *IEEE Power Electronics Magazine*, vol. 5, no. 2, pp. 34-39, June 2018.

[Heftman-05] G. Heftman, "PWM: from a single chip to a giant industry," Oct. 2005. [Online]. Available: https://www.powerelectronics.com/technologies/power-management/article/21861353/pwm-from-a-single-chip-to-a-giant-industry.

[Hegarty-18] Timothy Hegarty, "An overview of conducted EMI specifications for power supplies," Feb. 2018. [Online]. Available: http://www.ti.com/lit/wp/slyy136/slyy136.pdf.

[Herzer-09] S. Herzer, S. Kulkarni, M. Jankowski, J. Neidhardt and B. Wicht, "Capacitive-coupled current sensing and auto-ranging slope compensation for current mode SMPS with wide supply and frequency range," in *IEEE Proceedings of ESSCIRC*, Athens, 2009, pp. 140-143.

[Ho-10] E. N. Y. Ho and P. K. T. Mok, "Ramp signal generation in voltage mode CCM random switching frequency Buck converter for conductive EMI reduction," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2010, pp. 1-4.

[Huang-13] C. Huang and P. K. T. Mok, "An 84.7% efficiency 100-MHz package bondwire-based fully integrated Buck converter with precise DCM operation and enhanced light-load efficiency," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2595-2607, Nov. 2013.

[Huang-16] X. Huang, J. Feng, F. C. Lee, Q. Li and Y. Yang, "Conducted EMI analysis and filter design for MHz active clamp flyback front-end converter," in *IEEE Applied Power Electronics Conference and Exposition* (*APEC*), Long Beach, CA, 2016, pp. 1534-1540.

[Hwang-13] I. Hwang *et al.*, "Impact of channel hot electrons on current collapse in AlGaN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 34, no. 12, pp. 1494-1496, Dec. 2013.

[IBM-58] IBM, IBM Customer Engineering Reference Manual: 736 Power Supply, 741 Power Supply, 746 Power Distribution Unit, pp. 60-17, 1958.

[Idir-06] N. Idir, R. Bausiere and J. J. Franchaud, "Active gate voltage control of turn-on di/dt and turn-off dv/dt in insulated gate transistors," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 849-855, July 2006.

[IEC-15] IEC, International Special Committee on Radio Interference (CISPR) Guidance for Users of the CISPR Standards. Feb. 2015. [Online]. Available: https://www.iec.ch/emc/pdf/cispr_guide_2015.pdf.

[JEDEC-19] JEDEC, Dynamic on-resistance test method guidelines for GaN HEMT based power conversion devices, version 1.0. Jan. 2019. [Online]. Available: https://www.jedec.org/standards-documents/docs/jep173.

[Ke-17] X. Ke, J. Sankman, Y. Chen, L. He and D. B. Ma, "A 10MHz 3-to-40V V_{IN} tri-slope gate driving GaN DC-DC converter with 40.5dBμV spurious noise compression and 79.3% ringing suppression for automotive applications," in *IEEE International Solid-State Circuits Conference* (*ISSCC*), San Francisco, CA, 2017, pp. 430-431.

[Kahng-60] Kahng D, Atalla MM, “Silicon-silicon dioxide field induced surface devices,” in *IRE Solid State Device Research Conference*, 1960.

[Lee-11] S. Lee, S. Jung, J. Huh, C. Park, C. Rim and G. Cho, “Robust and efficient synchronous buck converter with near-optimal dead-time control,” in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 392-394.

[Li-19] R. Li, X. Wu, S. Yang and K. Sheng, “Dynamic on-state resistance test and evaluation of GaN power devices under hard- and soft-switching conditions by double and multiple pulses,” *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1044-1053, Feb. 2019.

[Lidow-79] A. Lidow, T. Herman and H. W. Collins, "Power MOSFET technology," in International Electron Devices Meeting (IEDM), Washington, DC, USA, 1979, pp. 79-83.

[Lidow-15] A. Lidow, J. Strydom, M. Rooij, and D. Reusch, “GaN transistors for efficient power conversion,” 2nd Ed. West Sussex, UK. John Wiley & Sons, 2015.

[Lorenz-99] L. Lorenz, G. Deboy, A. Knapp and M. Marz, “COOLMOS^{TM}-a new milestone in high voltage power MOS,” in *International Symposium on Power Semiconductor Devices and ICs*, Toronto, Ont., Canada, 1999, pp. 3-10.

[Lutz-18] J. Lutz and U. Scheuermann, “Semicondcutor power devices-physics, characteristics, reliability,” 2nd Ed. Springer, 2018.

[Majid-12] A. Majid, J. Saleem, H. B. Kotte, R. Ambatipudi and K. Bertilsson, “Design and implementation of EMI filter for high frequency (MHz) power converters,” in *International Symposium on Electromagnetic Compatibility - EMC EUROPE*, Rome, 2012, pp. 1-4.

[Meng-06] J. Meng, W. Ma, Q. Pan, L. Zhang and Z. Zhao, “Multiple slope switching waveform approximation to improve conducted EMI spectral analysis of power converters,” *IEEE Transactions on Electromagnetic Compatibility*, vol. 48, no. 4, pp. 742-751, Nov. 2006.

[Murata-19] Murata: “Noise suppression products/EMI suppression filters,” 2019. [Online]. Available: https://www.murata.com/en-global/products/emc/emifil/knowhow/basic/chapter01-p1.

[Musumeci-97] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo and M. Melito, "Switching-behavior improvement of insulated gate-controlled devices," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, pp. 645-653, July 1997.

[Oh-15] H. Oh, B. Han, P. McCluskey, C. Han and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: a review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413-2426, May 2015.

[Paine-15] B. M. Paine, S. R. Polmanter, V. T. Ng, N. T. Kubota and C. R. Ignacio, "Lifetesting GaN HEMTs with multiple degradation mechanisms," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 4, pp. 486-494, Dec. 2015.

[Paynter-62] D. A. Paynter, "Transistor converter," US Patent 3,067,378, Dec. 1962.

[Philips-91] Philips Semiconductors – UC3842, "Current-mode PWM controller," Datasheet, 1991.

[Poze-19] A. Poze, S. Zhang, and R. Strittmatter, "EPC eGaN FETs reliability testing: phase 10," Accessed: 2019. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/Reliability%20Report%20Phase%2010.pdf.

[Prasobhu-18] P. Kumar Prasobhu, V. Raveendran, G. Buticchi and M. Liserre, "Active thermal control of GaN-based DC/DC converter," *IEEE Transactions on Industry Applications*, vol. 54, no. 4, pp. 3529-3540, July-Aug. 2018.

[Pu-19] S. Pu, E. Ugur, F. Yang, G. Wang and B. Akin, "In-situ degradation monitoring of SiC MOSFET based on switching transient measurement," *IEEE Transactions on Industrial Electronics*, pp. 1-1, July 2019.

[RAM-18] Research and Markets, "Power Electronics - Global Market Outlook (2017-2026)," Oct. 2018. [Online]. Available: https://www.researchandmarkets.com/reports/4667929/power-electronics-global-market-outlook-2017.

[Regan-04] T. Regan and D. La Porte, "Easy-to-use spread spectrum clock generator reduces EMI and more," *Linear Technol. Mag.*, pp. 6-12, Feb. 2004.

[Roschatt-15] P. M. Roschatt, R. A. McMahon and S. Pickering, "Temperature measurements of GaN FETs by means of average gate current sensing," in *IEEE 11th International Conference on Power Electronics and Drive Systems*, Sydney, NSW, 2015, pp. 673-677.

[Salama-77] C. A. T. Salama, "V-groove power field effect transistors," in *International Electron Devices Meeting*, Washington, DC, USA, 1977, pp. 412-415.

[Shepherd-12] J. Shepherd, C. Marot, B. Vrignon and S. B. Dhia, "Near-field scan-State of the art and standardisation," in *Asia-Pacific Symposium on Electromagnetic Compatibility*, Singapore, 2012, pp. 1-4.

[Song-15] M. K. Song, L. Chen, J. Sankman, S. Terry and D. Ma, "A 20V 8.4W 20MHz four-phase GaN DC-DC converter with fully on-chip dual-SR bootstrapped GaN FET driver achieving 4ns constant propagation delay and 1ns switching rise time," in *IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, 2015, pp. 302-303.

[Stojanovski-01] T. Stojanovski and L. Kocarev, "Chaos-based random number generators-part I: analysis [cryptography]," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 3, pp. 281-288, March 2001.

[Streetman-06] B. G. Streetman, S. K. Banerjee SK, "Solid state electronic devices," 6th Ed. Prentice Hall, New Jersey, 2006.

[Tao-11] C. Tao and A. A. Fayed, "Spurious-noise-free buck regulator for direct powering of analog/RF loads using PWM control with random frequency hopping and random phase chopping," in *IEEE International Solid-State Circuits Conference*, San Francisco, CA, 2011, pp. 396-398.

[TI-11] Texas Instrument (TI): XTR111, "Precision voltage-to-current converter/transmitter," June 2011. [Online]. Available: http://www.ti.com/lit/ds/symlink/xtr111.pdf.

[TI-13] Texas Instrument (TI) Application Report: SNVA489C, "Simple success with conducted EMI from DC-DC converter," Apr. 2013. [Online]. Available: http://www.ti.com/lit/an/snva489c/snva489c.pdf.

[TI-15] Texas Instrument (TI) – LMG5200, "48V to 1V/40A single stage converter," Datasheet, 2015.

[TI-18] Texas Instrument (TI): "An overview of conducted EMI specifications for power supplies," Design note, 2018.

[TI-19] Texas Instrument (TI) – LM5143-Q1, "LM5143-Q1 3.5-V to 65-V low I_Q, dual synchronous buck DC/DC controller," Datasheet, 2019.

[Tse-02] K. K. Tse, Henry Shu-Hung Chung, S. Y. Ron Hui and H. C. So, "A comparative study of carrier-frequency modulation techniques for conducted EMI suppression in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 3, pp. 618-627, June 2002.

[Smet-11] V. Smet *et al*., "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, pp. 4931-4941, Oct. 2011.

[Unitrode-86] Unitrode, "Applications handbook 1987-88," Accessed: 1986. [Online]. Available: http://bitsavers.trailing-edge.com/components/unitrode/_dataBooks/1987_Unitrode_Applications_Handbook.pdf.

[Wang-10] H. Wang, A. M. Khambadkone and X. Yu, "Control of parallel connected power converters for low voltage microgrid—part II: dynamic electrothermal modeling," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, pp. 2971-2980, Dec. 2010.

[Wang-14] Z. Wang, X. Shi, L. M. Tolbert, F. Wang and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3720-3732, July 2014.

[Williams-94] R. K. Williams, K. Owyang, H. Yilmaz, M. Chang, and W. Grabowski, "Complementary trench power MOSFET s define new levels of performance," in *Proc. 16th Internationale Fachmesse für Bauelemente Baugruppen Der Elektronik* (*Electronica*), Munich, Germany, Nov. 1994, pp. 1–7. [Online]. Available: http:// www.pe2bz.philpem.me.uk/pdf%20on%20typenumber/0-9/4902.pdf.

[Williams-96] R. K. Williams, W. Grabowski, M. Darwish, H. Yilmaz, M. Chang and K. Owyang, "A 30-V P-channel trench gated DMOSFET with 900 $\mu\Omega$-cm^2 specific on-resistance at 2.7 V," in *International Symposium on Power Semiconductor Devices and ICs* (*ISPSD*) *Proceedings*, Maui, HI, USA, 1996, pp. 53-56.

[Williams-17] R. K. Williams, M. N. Darwish, R. A. Blanchard, R. Siemieniec, P. Rutter and Y. Kawaguchi, "The trench power MOSFET: part I—history, technology, and prospects," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 674-691, March 2017.

[Xu-18] C. Xu, E. Ugur, F. Yang, S. Pu and B. Akin, "Investigation of performance degradation in enhancement-mode GaN HEMTs under accelerated aging," in *IEEE 6th Workshop on Wide Bandgap Power Devices and Applications* (*WiPDA*), Atlanta, GA, 2018, pp. 98-102.

[Yang-18] W. Yang *et al*., "An enhanced-security buck DC-DC converter with true-random-number-based pseudo hysteresis controller for internet-of-everything (IoE) Devices," in *IEEE International Solid - State Circuits Conference* (*ISSCC*), San Francisco, CA, 2018, pp. 126-128.

[Zhang-19] H. Zhang, "Simple solution for input filter stability issue in DC/DC converters," *Texas Instruments Application Report*, pp. 1-16, April 2019.

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Yingping Chen received an ME degree in micro-electronics and solid-state electronics from the University of Chinese Academy of Sciences, Beijing, China, in 2012 and a BE degree in polymer materials and engineering from Beijing Institute of Technology, Beijing, China, in 2008. Currently he is working toward a PhD degree in electrical engineering at The University of Texas at Dallas, Richardson, TX, USA.

From January 2012 to October 2014, he worked in Sigma Microelectronics, Beijing, China, as an analog engineer, focusing on DC/DC converter, LED driver, and constant-current/constant-voltage AC/DC controller. During this period, he took part in developing two DC-DC Buck converters. One of them is a constant on-time synchronous Buck, featuring fast load transient response. The other one is a PWM controlled Buck with peak current-mode control. In addition, he was responsible for developing a flyback controller for LED driver and charger. Then he joined Dialog Semiconductor, Beijing, China, in November 2014, working as an analog engineer. In Dialog, he took part in a LED driver with digital control scheme. He was responsible for the analog part design, including bandgap circuit, internal LDO and high-performance comparators.

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GaN Reliability Improvement Using Junction-Temperature-Independent Online Condition Monitoring and Proactive Temperature Frequency Scaling

- Developed a temperature-independent online condition monitoring scheme to prognose current-collapse effect for GaN HEMT, sensing dynamic on-resistance as aging precursor.
- Developed a proactive temperature frequency scaling scheme for active thermal management, enhancing the longevity of GaN power system.

EMI Suppression Using Markov Random Spread-Spectrum Modulation (RSSM)

- Developed a Markov RSSM mechanism to spread EMI spectra continuously and randomly, employing a Markov-chain-based random clock generator.
- Developed a one-cycle on-time rebalancing scheme to replace the conventional PWM control method, avoiding RSSM-induced output jittering effect in switching power circuits.

Closed-Loop EMI Regulation Using Smart Power Driving

- Developed an emulated Miller Plateau tracking scheme to sense Miller Plateau voltage for GaN HEMT in one switching cycle, regardless of operating conditions of switching power circuits.
- Developed an adaptive strength gate driving mechanism to achieve independent control of low di/dt and high dv/dt, balancing the classical EMI-efficiency trade-off.

PUBLICATION LIST

- Y. Chen, and D. B. Ma, "EMI-regulated GaN-based switching power converter with Markov continuous random spread-spectrum modulation and one-cycle on-time rebalancing," *IEEE J. Solid-State Circuits* (*JSSC*), vol. 54, no. 12, pp. 3306-3315, Dec. 2019. (*Invited*)

- Y. Chen, and D. B. Ma, "An 8.3MHz GaN power converter using Markov continuous RSSM for 35dBμV conducted EMI attenuation and one-cycle T_{ON} rebalancing for 27.6dB V_O jittering suppression," in *IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) *Dig. Tech. Papers*, Feb. 2019, pp. 250-251.

- Y. Chen, and D. B. Ma, "A 10MHz *i*-collapse failure self-prognostic GaN power converter with T_J-independent in-situ condition monitoring and proactive temperature frequency scaling," in *IEEE IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) *Dig. Tech. Papers*, Feb. 2019, pp. 248-249.

- Y. Chen, X. Ke, and D. B. Ma, "A 10MHz 5-to-40V EMI-regulated GaN power driver with closed-loop adaptive Miller Plateau sensing," in *IEEE Proc. Symp. VLSI Circuits* (*VLSI*) *Dig. Tech. Papers*, Jun. 2017, pp. C120-C121.

- Y. Chen, X. Ke, and D. B. Ma, "Integrated isolated power converter using active rectification and closed-loop CRM control for secondary side regulation in E-meters," in *IEEE Appl. Power Electronics Conf.* (*APEC*), March 2017, pp. 3432-3435.

- Y. Chen, and D. B. Ma, "Modulation range impact on EMI attenuation by frequency dithering schemes in GaN-based DC-DC Buck converters," in *21th Annual TECHCON*, Sept. 2019.

- Y. Huang, Y. Chen**,** and D. B. Ma, "A self-health-learning GaN power converter using on-die logarithm-based analog SGD supervised learning and online T_J-independent precursor measurement," in *IEEE IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) *Dig. Tech. Papers*, Feb. 2020 (Accepted).

- X. Ke, J. Sankman, Y. Chen, L. He, and D. B. Ma, "A tri-slope gate driving GaN DC-DC converter with spurious noise compression and V_{SW} ringing suppression," *IEEE J. Solid-State Circuits* (*JSSC*), vol. 53, no. 1, pp. 247-260, Sept. 2017.

- X. Ke, J. Sankman, Y. Chen, L. He, and D. B. Ma, "A 10MHz 3V-to-40V V_{IN} tri-slope gate driving GaN DC-DC converter with 40.5dBμV spurious noise compression and 79.3% ringing suppression," in *IEEE Int. Solid-State Circuits Conf.* (*ISSCC*) Dig. Tech. Papers, Feb. 2017, pp. 430-432.