RELIABILITY AND CONDITION MONITORING OF

SIC POWER MOSFETS

by

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Dedicated to my family.

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by

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As electrical devices are becoming an indispensable part of our lives and pretty much of all industries, efficient and reliable operation of power converters which energize these devices is also becoming crucial. Todays modern power converters commonly utilize silicon (Si) semiconductor devices to perform high speed switching operation, and therefore their performance is limited by the material properties of Si. The latest potent alternative semiconductor technology for high voltage and high temperature applications is silicon carbide (SiC) due to their higher voltage ratings, higher maximum operating temperatures, and higher thermal conductivity. Although SiC devices provide a solution to overcome the physical limitations of Si, their market adoption remains limited. Reliability of SiC devices is one of the main barriers preventing their high penetration into the market.

Therefore, it is essential to investigate progressive degradation and parameter shifts in SiC devices to develop condition monitoring tools which can recognize failure precursors at the earliest stage and increase the system reliability. This dissertation presents a comprehensive long-term reliability analysis of commercially available SiC MOSFETs under high temperature operation. For this purpose, discrete SiC devices are power cycled and variation of electrical parameters throughout the aging is presented in order to assess the key precursor parameters and their correlation with the state of device aging. Discussions regarding

aging precursors are supported by detailed failure analysis. It has been revealed that the most popular precursor parameter, on-state resistance, reveals the combination of gate oxide and packaging related degradation while threshold voltage mainly depicts gate oxide related issues. Unlike these two parameters, the body diode voltage drop is found to be independently indicating device state of health (SOH) both for packaging and gate oxide degradation. Based on this finding a new condition monitoring method is proposed for SiC MOSFETs which deploys reverse body diode voltage drop at different gate bias levels. The proposed condition monitoring method is implemented on a gate driver circuit and experimental results are presented. The proposed method can be integrated into a gate driver or can be implemented at converter level to monitor the SOH of devices.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 Motivation

With the growing demand in electrical power in our lives, performance and reliability requirements for power converters are also increasing. Since the power converters deploy semiconductor devices to perform high speed switching operation, their performance and lifetimes are dependent upon the properties and condition of the switch. Even though silicon (Si) based power MOSFETs and IGBTs have dominated the power electronic market with their steadily improving performance for over three decades, the rate of improvement has slowed down in recent years as Si approaches its theoretical limits [1]. Moreover, the increasing demand for higher temperature and higher frequency operation has prompted a lot of efforts to find alternatives to Si-based power devices.

Wide bandgap (WBG) devices are the enabling semiconductor technology for high voltage, high frequency and high temperature applications [2]. Among the possible WBG semiconductor materials, Silicon Carbide (SiC) and Gallium Nitride (GaN) fabrication technologies have achieved enough maturity enabling their commercial availability. Compared to Si, SiC has a higher electric breakdown field with higher thermal conductivity, whereas GaN has a higher breakdown field with higher electron mobility [3]. The high critical electric breakdown strength of these materials allows to design devices with thinner drift region which decreases the specific on-state resistance. The high thermal conductivity of SiC makes them very popular for high power and high temperature applications [4]. Although GaN lacks good-quality bulk substrates needed for vertical devices so far, GaN based High Electron Mobility Transistors ($HEMTs$) are appealing in high-frequency, high- voltage power electronics converters due to the low conduction and switching losses [5, 6].

Although WBG devices provide a solution to overcome the physical limitations of Si, they do not necessarily improve the reliability. In fact, as a relatively new technology com-

pared to the mature and very well established Si technology, WBG devices raise significant reliability concerns. In addition to real reliability problems due to manufacturing technology limitations, absence of field application data regarding the long-term reliability creates potential uncertainties. Eventually, the reliability concerns of WBG devices is one of the main barriers preventing their high penetration into the market [7].

The power semiconductor devices are always subjected to various mechanical and electrical stresses, wear, temperature extremes and vibration during operation that contribute to an increased potential for equipment failure [8]. In industrial applications, a component failure not only causes maintenance costs but also inflicts much higher operational costs due to unexpected interruptions. In critical applications, unexpected interruptions may cause serious safety issues which may lead to property damage or even loss of life. According to a recent survey, the power semiconductor failures account for 72% of the total failures in dc-dc converters in industry [9].

Traditional engineering practices used to improve power converter and system reliability by utilizing costly fault tolerant topologies and hardware redundancy [10]. However, with continuously increasing high power density and low cost requirements, it is not feasible solution to increase the size and the cost of the converter to obtain higher reliability. Therefore, to enhance the reliability for WBG adoption and minimizing catastrophic failures in real time applications, it is essential to continuously monitor and evaluate the incipient failure of the state-of-art WBG devices. However, current diagnostic engineering tools are not mature enough to detect or identify failure precursors in real time, leading to a major reliability gap in WBG-based power conversion systems. In order to move WBG technologies forward reliably, it is crucial to investigate progressive structural degradations and parameter shifts in WBG devices as well as to develop online degradation monitoring tools and smart gate drivers with early failure warning feature.

1.2 Research Objectives

The primary goal of this work is to evaluate the reliability of commercially available SiC MOSFETs under high temperature operation and to identify failure precursors in order to develop condition monitoring tools. The objectives of the research are:

- To comprehensively analyze long-term reliability of commercially available SiC MOSFETs under high temperature operation and high temperature swing by means of accelerated power cycling.
- To capture the variation of electrical parameters throughout the aging.
- To assess the correlation between the variation of electrical parameters and the aging/degradation state of the switch.
- To conduct detailed failure analysis in order to understand of the root cause of the aging.
- To define the precursor variation pattern for each degradation mechanism in order to develop model for predicting the remaining useful lifetime.
- To define the suitability of electrical parameters as an aging precursor parameter.
- To develop new condition monitoring method for SiC MOSFETs.

In addition to scientific objectives, this dissertation also aims to provide an overview of SiC MOSFETs including the reliability aspects as a guideline to the power electronics engineers who are not very familiar with the device physics.

1.3 Key Research Contributions

The original research contributions in this thesis are summarized as follows:

- It is demonstrated that on-state resistance of SiC MOSFETs reveals the combination of gate oxide and packaging related degradation while the threshold voltage mainly depicts gate oxide charge trapping related issues.
- It is identified that the gate threshold voltage increases logarithmically throughout the aging due to the gate oxide interface charge trapping.
- The bond wire heel cracking is found to be the most common packaging related failure mechanism for discrete SiC power MOSFETs.
- It is demonstrated that SiC power MOSFETs with single source bond wire shows an exponential on-state resistance variation with bond wire degradation. However, devices with multiple bond wires, manifests the bond wire lift-off by sudden increases in on-state resistance, and body diode voltage drop under negative gate bias.
- A unique secondary conduction mode of SiC MOSFETs in third quadrant operation is discovered which is illustrated with a proposed body diode transfer characterization curve.
- For the first time, the unique third quadrant conduction mode of SiC MOSFETs is analyzed in T-CAD simulation and the details of this conduction mode are revealed.
- It is discovered that the body diode voltage drop independently indicates device state of health (SOH) both for packaging and gate oxide degradation.
- A new condition monitoring method for SiC MOSFETs is invented which deploys reverse body diode voltage drop at different gate bias levels.

1.4 Thesis Outline

In Chapter 2 the material properties of SiC which gives them an edge for power electronics applications is reviewed. This is followed by a realistic assessment of the materials challenges and a discussion of reliability issues related to SiC material as a bulk and within MOSFET device structure. The most common degradation mechanisms in SiC MOSFETs are introduced. Then reliability test methods, first developed for Si power devices and later adopted by SiC technologies, are summarized.

In Chapter 3 the long-term degradation mechanisms of commercially available SiC MOSFETs is comprehensively evaluated under high temperature operation and high temperature swing. The basic operating principle of the accelerated power cycling test setup and the aging condition of the devices are introduced. A systematic static parameter evaluation of each device is performed at room temperature with the aid of the Keysight B1506A curve tracer. According to variations of electrical parameters throughout aging, parameter shift assessment and aging precursors identification is carried out. The suitability of these parameters as aging precursors is investigated considering implementation issues.

In Chapter 4 a detailed failure analysis (FA) is conducted in order to have a better understanding of the root cause of the aging.

In Chapter 5 an improved condition monitoring method is proposed for SiC MOSFETs which can monitor both gate interface degradation and package related degradation independently by only capturing the body diode voltage drop at different gate bias values. A comprehensive evaluation of variations in commonly used precursor parameters and effect of each degradation mechanism is presented. Due to the unique two different conduction modes feature of SiC MOSFETs in third quadrant operation, i.e., the MOSFET path conduction and the PiN path conduction, varying body diode voltage drop is revealed by the proposed body diode transfer characteristic curve. The body diode voltage drop variations captured

throughout aging at 0V and -5V gate voltage bias and it found that contact resistance variations can be monitored with PiN diode path conduction while the gate oxide degradation can be detected during MOSFET path conduction. Therefore, it is concluded that just by capturing body diode voltage drop at different gate biases, a complete state of health of SiC devices can be obtained. Experimental results are presented to demonstrate that the designed condition monitoring circuit can accurately detect both gate oxide degradation and the package related degradation.

In Chapter 6 in this chapter, the theory of third quadrant operation of SiC MOSFET is explained. A detailed T-CAD simulation analysis of SiC MOSFET third quadrant operation has been provided for the first time in the literature. Finally, effect of the gate voltage on the reverse recovery characteristic of SiC MOSFET body diode is discussed.

In Chapter 7 a hybrid secondary lifetime extension control scheme for three-phase inverters based on the identified failure precursors which dynamically changes the modulation scheme and adjusts the switching frequency. The tradeoff between the THD and achievable lifetime extension is addressed, and a control algorithm is proposed which maximizes the lifetime with feasible lowest THD.

In Chapter 8 the conclusions and summary of the dissertation are presented.

CHAPTER 2

OVERVIEW OF SILICON CARBIDE POWER DEVICES

Since the introduction of the first power MOSFET in 1976, the performance of Si power devices has steadily improved and kept pace with growing need for higher efficiency and lower cost. However, as the technology gets mature, Si based devices are now approaching to their performance limits mandated by their fundamental material properties. In order to achieve further performance progress, WBG semiconductor materials has been proposed. As a WBG material, SiC power devices have been drawing enormous attention for various power electronics applications at a wide range of operating temperatures. This is due to their superior physical properties compared to Si counterparts like higher bandgap, higher breakdown electric field strength and higher thermal conductivity. In addition to these properties, SiC is the only WBG material which has silicon dioxide (SiO_2) as its stable native oxide [1]. Although these unique properties make SiC highly suitable for power electronics applications, they also make it a challenge to process SiC material and manufacture switching devices [4]. Crystal growth challenges and the small market size have been keeping the SiC costs high and limiting the commercialization of SiC power MOSFETs. Therefore, it is necessary to evaluate the superior material properties of SiC realistically with the difficulties it introduces for semiconductor device development.

In this chapter, the material properties of SiC which gives the material an edge for power electronics applications will be reviewed first. This will be followed by a realistic assessment of the materials challenges and a discussion of reliability issues related to SiC material as a bulk and within MOSFET device structure. Then reliability test methods, first developed for Si power devices and later adopted by SiC technologies, will be summarized.

2.1 Material Properties of Silicon Carbide

SiC crystalline structure exhibits two-dimensional polytypism. Polytypism is the phenomenon where a material crystal structure can accept different stacking sequence without changes in chemical composition [1]. SiC polytypes are classified by the number of Si-C layers in the unit cell before the sequence repeats itself and the resulting structure of the crystal (C for cubic, H for hexagonal, and R for rhomohedral) [4]. Among more than 200 different SiC polytypes, due to better material quality, hexagonal crystal structure polytypes (4H-SiC and 6H-SiC) have been the most commonly grown and studied polytypes [11]. However, it was only 4H-SiC which has successfully became a commercial product for power device applications. The substantially higher carrier mobility and having identical mobilities along both planes of the semiconductor crystal makes 4H-SiC is more favorable compared to 6H-SiC [12]. Therefore, in this dissertation, only 4H-SiC will be covered and hereafter "SiC" means 4H-SiC unless specified.

The desired characteristics for a semiconductor to be used for power electronics applications include high efficiency, easy control, high switching speed, reliable operation, good thermal conductivity, high-temperature operation capability and reasonable costs [5, 13]. Without meeting these requirements altogether, a semiconductor material will not be viable for power conversion applications, no matter how good is the material in all other properties. In Table 2.1, the selected material properties of the most popular semiconductor materials in power applications, i.e. Si, SiC and GaN, are summarized. One way of interpreting these basic material parameters into a comparison of device performance is to determine the best theoretical performance achievable for each of the three semiconductor materials [5]. In the next section, the most important material characteristics in Table 2.1 and their impact on the device performance will be reviewed.

Table 2.1. Major Material Properties of Si, SiC, and GaN [10, 1, 14, 13]

Properties	Si	4H-SiC	GaN-on-Si
Energy Bandgap (E_G) (eV)	1.12	3.23	3.39
Breakdown Electric Field (E_B) ($MV.cm^{-1}$)	0.3	2.8	2
Thermal Conductivity (λ) ($W.cm^{-1}K^{-1}$)	1.5	3.9	1.3
Relative Dielectric Constant (ε_r)	11.8	9.7	9
Electron Mobility (μ_n) ($cm^2/V^{-1}s^{-1}$)	1420	900	2000
Hole Mobility (μ_p) ($cm^2/V^{-1}s^{-1}$)	470	110	200
Saturation Drift Velocity v_S (cm/s^{-1}) $x10^7$	1	2.7	2.5
Thermal Expansion Coefficient (CTE) (x$10^{-6}K^{-1}$)	2.6	4.3	3.17
Youngs modulus (E) (GPa)	162	501	181
Melting point (°C)	1414	2730	2500

2.1.1 Energy Bandgap (E_G)

As a WBG semiconductor, the most evident property of SiC is its wide bandgap. The electrons creating covalent bonds in the outermost shell of atoms occupy a band of energy levels, called as the valence band. The next higher band of allowed energy levels is known as the conduction band and separated from the valence band by a forbidden energy gap (Eg). When an electron in the valance band gains sufficient energy, it will break the covalent bond and jump from the valance band to the conduction band, leaving behind an unoccupied energy level as a hole. Both of these particles (charge carriers) are mobile and will contribute to electric current [15]. In conductor materials, the conduction and the valence bands are merged so the forbidden energy bandgap do not exist. On the other hand, insulators has this band so wide that a very high amount of energy is required to break the covalent bonds and make electrons to jump up into the conduction band [16]. Semiconductors have smaller energy bandgap than insulators. The bandgap of Si is 1.12 eV at room temperature while the bandgap for SiC is 3.23 eV, which is the reason why SiC is classified as a wide bandgap semiconductor [10].

As it will be discussed in more detail later, the wide bandgap of SiC translates into several improvements for power devices. However, the most immediate outcomes are lower intrinsic leakage currents and higher operating temperatures. At zero absolute temperature ($T \approx 0K$), there would be no broken covalent bonds in a semiconductor, and all the electrons would be in the valence band. At $T > 0$ though, the thermal energy of the electrons will increase and a certain number of valence electrons will gain sufficient energy (E_G) to break the covalent bond and elevate into the conduction band. With increasing temperature, more and more electron-hole pairs will be created by thermal generation. At thermal equilibrium, the number of electrons in the conduction band (or the number of holes in the valence band) per unit volume in a semiconductor, i.e., the intrinsic carrier concentration (n_i) can be calculated by (2.1)

$$n_i = \sqrt{n.p} = \sqrt{N_C N_V}.e^{-(E_G/2kT)} \tag{2.1}$$

where k is Boltzmanns constant ($1.38 \times 10^{-23} J/K$), T is the absolute temperature, and N_C and N_V are the density of states in the conduction and valence bands [2].

Intrinsic carrier concentration is one of the key parameters for power semiconductor devices as it determines not only the maximum operating temperature, but also its leakage current. As it can be seen from (2.1), n_i exponentially decreases with bandgap and exponentially increases with the temperature. As the state densities for Si and SiC are similar, it is obvious that at any given temperature, the n_i for SiC will be far smaller than for Si due to the large difference in their energy bandgaps. The intrinsic carrier concentration of Si and SiC can be calculated as a function of temperature by (2.2) and (2.3) respectively [2].

$$n_i = 3.87 \times 10^{16}\, T^{3/2}\, e^{-(7.02\times 10^3)/T} \tag{2.2}$$

$$n_i = 1.70 \times 10^{16}\, T^{3/2}\, e^{-(2.08\times 10^4)/T} \tag{2.3}$$

At room temperature ($300K$), n_i of Si is $1.4x10^{10}cm^{-3}$ while it is only $6.7x10^{-11}cm^{-3}$ for SiC which means much lower leakage currents for SiC devices. Fig. 2.1 shows plots of the intrinsic carrier concentrations for Si and SiC as a function of temperature.

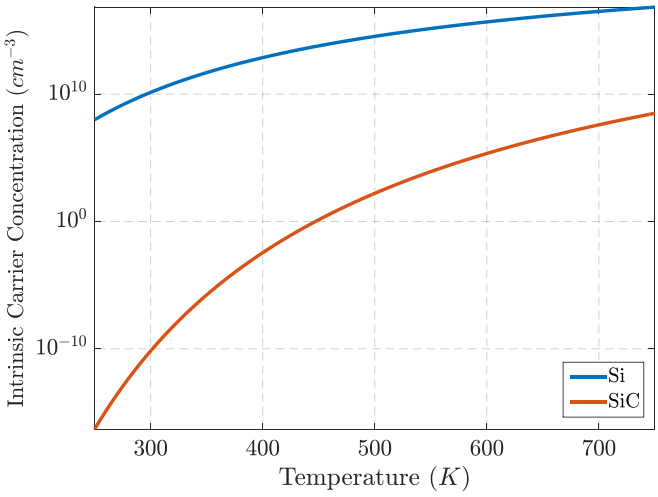


Figure 2.1. Intrinsic carrier concentration for Si, and SiC as a function of temperature

In order to increase the conductivity of semiconductors, impurities can be added to the intrinsic (pure) semiconductor by doping process. According to the type of dopant, n-type or p-type extrinsic semiconductor can be produced. At lower temperatures, carrier generation is dominated by ionization of dopant atoms which is called majority carriers. However, at high temperatures, thermal bulk generation of carriers can approach the doping concentration of the drift region and can become the dominant process for carrier generation and therefore change the electrical property of the semiconductor. When n_i becomes the dominant process, its exponential increase with temperature together with positive thermal feedback, can lead to destruction of the device. As an example, for a Si power device with 1000 V blocking voltage and $10^{14}cm^3$ doping density, the junction temperature must remain below 190 °C in order to avoid thermal runaway. If the same design is implemented with SiC, temperatures of more than 800 °C would be allowed. However, in practice, the maximum

operating temperature for a SiC power device is rather limited by the packaging materials and interconnect technology [10].

As a summary, the bandgap of the device is linked to the strength of covalent bonds and it defines intrinsic leakage current and maximum operating temperature of a semiconductor device. The wider the bandgap is, the higher the temperatures at which power devices can operate or the lower the leakage current at any given temperature. This reasoning is also valid for radiation hardening as it can also excite an electron to move to the conduction band. As a result of its wide bandgap, SiC devices can operate at higher temperatures without losing their electrical characteristics. With the ability to operate at higher temperatures, SiC devices will also enable a significant reduction in the cooling system requirements.

Besides thermal excitation, free electrons in semiconductors can also be generated by an external electric fields high enough to break the covalent bond. In next subsection, electric field strength of SiC devices will be discussed.

2.1.2 Breakdown Electric Field Strength (E_B)

The most remarkable and beneficial property of SiC for power semiconductor devices is its higher breakdown electric field strength. Power devices are designed to withstand high voltages across a depletion layer formed with a P-N junction structure by depositing a low-doped epitaxial layer [2]. During forward voltage blocking, when an electron and/or hole enters the depletion layer, it is accelerated by the electric field and gains kinetic energy. As the electron moves through the depletion layer, it may collide with the lattice atoms. When the applied voltage is increased, the electron may acquire sufficient kinetic energy from the electric field so that, when it collides with the lattice atoms, it can break the covalent bonds and generate an electronhole pair. Since the generated electron-hole pair is under the same electric field, they also gain sufficient kinetic energy and create further pairs of electrons and holes [10]. The generation of electron-hole pairs due to kinetic energy gained from the

electric field is referred to as *impact ionization*. This process is a multiplicative process where newly generated carriers in the depletion layer ionize other atoms, leading to an avalanche breakdown. Therefore, the maximum electric field strength in the depletion layer, at which breakdown occurs, is called as the *critical electric field strength* (E_C) or *breakdown electric field strength* (E_B) [1].

The main factor defining the critical field strength is the bandgap of the semiconductor. As the bandgap increases a higher critical electric field is needed to initiate impact ionization, thus high bandgap devices will have higher E_B [10]. Besides the bandgap, E_B is also dependent on the temperature and doping concentration. As temperature increases, the phonon scattering in the depletion layer also increases and this reduces the average distance between two collisions. Therefore, the carriers gain less energy from the electric field at higher temperatures and therefore a higher electric field will be necessary to initiate an avalanche breakdown [15]. In a similar fashion, when doping concentration is increased, the mean free transport path for carriers to be accelerated becomes short which increases the E_B. The E_B can be expressed at room temperature ($300K$) as a function of doping concentration by

$$E_B(Si) = \frac{4 \times 10^5}{1 - (1/3) \cdot log_{10}(N_D/10^{16})} \tag{2.4}$$

where N_D is the donor doping concentration in cm^{-3} [17]. Similarly, the E_B for SiC at 300K can be found by [18]

$$E_B(SiC) = \frac{2.49 \times 10^6}{1 - (1/4) \cdot log_{10}(N_D/10^{16})}. \tag{2.5}$$

Fig. 2.2 shows plots of the critical electric field values at room temperature as a function of the doping concentration for Si and SiC. It can be seen in the figure that for $N_D = 10^{15}cm^3$, E_B for Si is 0.3 MV/cm, while it is 1.992 MV/cm for SiC. This shows that E_B of SiC at $N_D = 10^{15}cm^3$ is 6.64 times that of Si. This values contradicts frequently mentioned 10 times higher critical field strength of SiC as well as E_B values of SiC listed in Table 2.1.

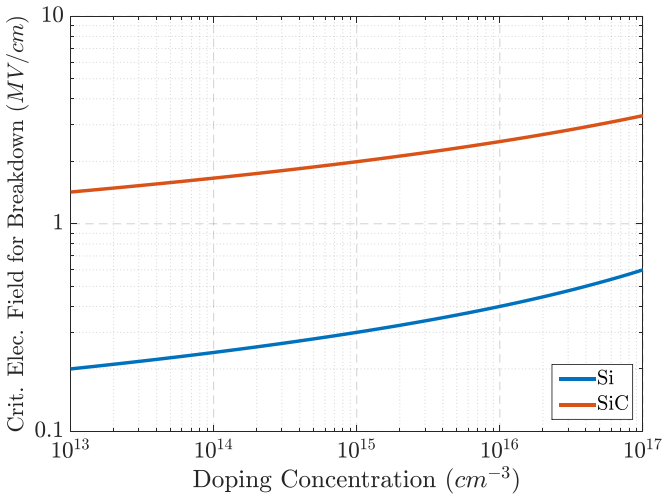


Figure 2.2. Critical breakdown electric field in Si and SiC as a function of doping concentration

This discrepancy is caused by the difference in typically used doping densities. For example, if $N_D = 10^{15} cm^3$ is in a Si device constructed for a blocking voltage, a SiC device would be constructed with $N_D = 3.10^{16} cm^3$ and therefore E_B will approximately be 2.8 MV/cm. This is the reason why the critical field strength of SiC is often given as 10 times higher than of Si. When one side of a P-N junction diode is doped with very high doping concentration compared to the other side, it is called as an abrupt P-N junction and the highly doped side is specified with a (+) superscript. For example in a P^+-N abrupt junction diode, P side is highly doped and N side is lightly doped. In an abrupt P-N junction structure, it can be assumed that the voltage is supported across only lightly doped side of the structure and the depletion region extends primarily in the lightly doped region. Such a case is illustrated in Fig. 2.3 for a P^+-N junction where the applied voltage V_B is supported across lightly doped N-region by forming a depletion region together with the generation of a strong electric field. The electric field in the depletion region can be determined using Poissons equation by

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{\rho(x)}{\varepsilon_r \varepsilon_0} = -\frac{qN_D}{\varepsilon_r \varepsilon_0} \qquad \text{for} \quad 0 \leq x \leq w_N \tag{2.6}$$

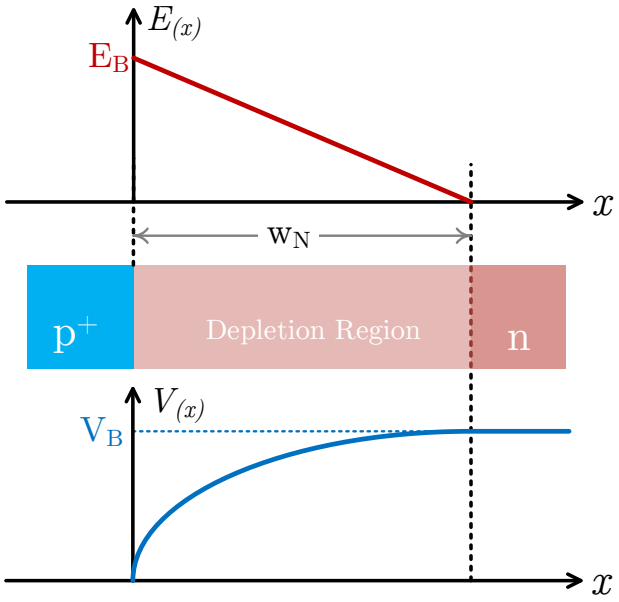


Figure 2.3. Electric field and potential distribution for an abrupt P^+-N junction

where ρ is the space charge volume density, ε_r is the relative permittivity of the semiconductor, $\varepsilon_0 = 10^9/36\pi = 8.8542 \times 10^{14} F/cm$ and $q = 1.60218 \times 10^{19} C$ is the magnitude of the electron charge [17]. If we assume that the semiconductor is doped uniformly, we can integrate (2.6).

$$\int_{E_x}^{E_{w_N}} dE = \int_0^{w_N} \frac{q.N_D}{\varepsilon_r \varepsilon_0} dx \tag{2.7}$$

Since the electric field at is $x = w_D$ is zero, we obtain

$$E(x) = -\frac{qN_D}{\varepsilon_r \varepsilon_0}(w_N - x) \qquad \text{for} \qquad 0 \leq x \leq w_N. \tag{2.8}$$

Then we can find the maximum field E_B at $x = 0$

$$E_B = \frac{qN_D w_N}{\varepsilon_r \varepsilon_0}. \tag{2.9}$$

As it can be seen from Fig. 2.3, we can find V_B by integrating the area under $E(x)$, which is

$$V_B = -\int_0^{w_N} E(x)dx = \frac{E_B w_N}{2}. \tag{2.10}$$

Then if we get w_N from (2.9) and write it in (2.10) we can obtain the breakdown voltage for abrupt P^+-N junctions as

$$V_B = \frac{E_B^2 . \varepsilon_r \varepsilon_0}{2qN_D}. \tag{2.11}$$

In Fig. 2.3, it is assumed that the lightly doped semiconductor is thick enough to support the maximum depletion layer width at breakdown. In order to block higher voltages, either thickness of the lightly doped region needs be increased or the doping concentration should be further decreased. However, the lightly doped region inevitably increases the series resistance of the device. Therefore, in power devices, there is no need to lightly dope the whole substrate (needed for mechanical strength only), since its significant thickness would introduce a large series resistance [15].

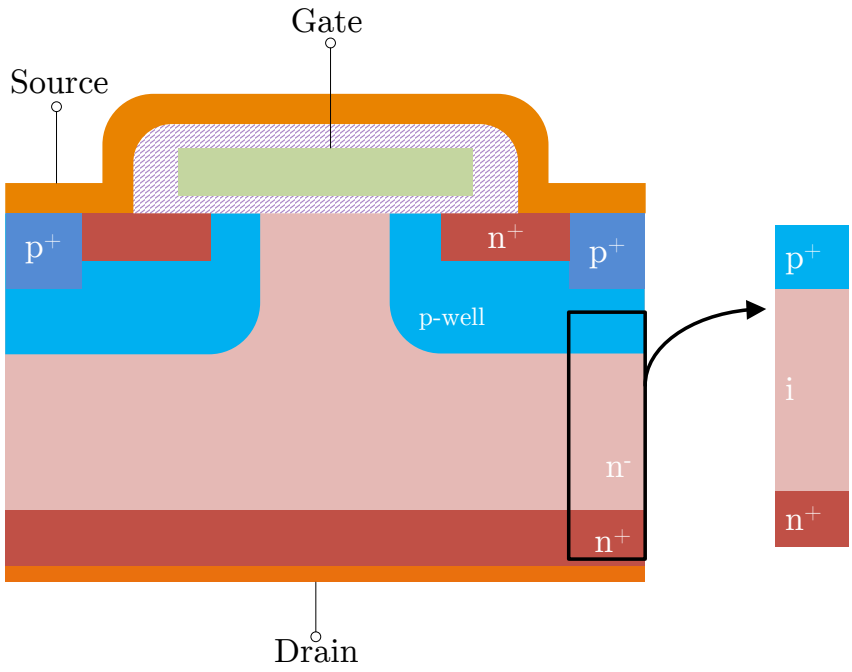


Figure 2.4. A planar power MOSFET structure

A planar power MOSFET structure is illustrated in Fig. 2.4. At the lowest level, the N^+ structure shows a heavily doped substrate. On top of the substrate, a very lightly doped

epitaxial layer is deposited (N^- drift region) which is necessary to achieve the high breakdown voltage. On top of the drift region there is a heavily doped layer P^+ layer. The low-doped drift layer, sandwiched between the N^+ and P^+ layers, is also referred to as an i-region implying that it is intrinsic in nature and acts like an insulator. In the sandwich structure, which also forms the PiN diode, a large concentration of minority carriers are injected into the drift region during on-state current flow, which strongly reduces the on-resistance [10]. The electric field distribution for the P-i-N structure is illustrated in Fig. 2.5. Since the depletion layer reaches the n^+ substrate, this configuration for the drift region is referred to as the punch-through design. Since the electric field distribution takes a trapezoidal shape instead of triangular shape, about twice the voltage for the same drift region width can be supported with the punch through design compared to the non-punch through design. Consequently, by utilizing the punch-through design, the thickness of the drift region and on-state resistance can be reduced.

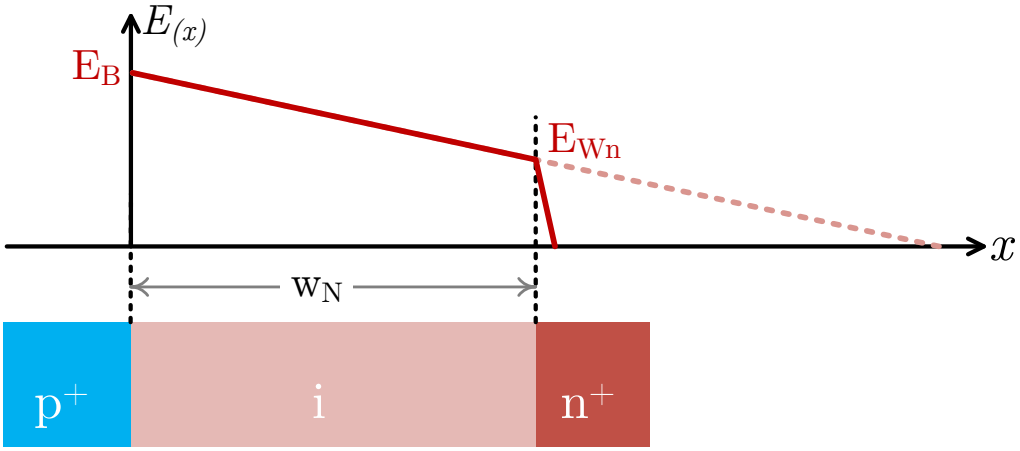


Figure 2.5. Electric field distribution for a PiN junction structure

Since the electric field at is $x = w_N$ is not zero in the punch-through design, we need to re-integrate (2.6).

$$\int_0^x dE = \int_0^x \frac{q.N_D}{\varepsilon_r \varepsilon_0} dx = E(x) \tag{2.12}$$

As the electric field at is $x = 0$ is E_B, we obtain

$$E(x) = -\frac{qN_D}{\varepsilon_r \varepsilon_0} x + E_B. \tag{2.13}$$

Then we can find the electric field at $x = 0$ as

$$E_{W_N} = E_B - \frac{qN_D}{\varepsilon_r \varepsilon_0} w_N. \tag{2.14}$$

Similarly V_B can be found by integrating the area under $E(x)$ as it is seen from Fig. 2.5,

$$V_B = \frac{E_B + E_{W_N}}{2} w_N. \tag{2.15}$$

Substituting (2.14) in (2.15) yields the breakdown voltage for the punch-through design as

$$V_B = E_C w_N - \frac{qN_D w_N^2}{2\varepsilon_r \varepsilon_0}. \tag{2.16}$$

The breakdown voltages for the Si and SiC PiN structures calculated using (2.11) for non-

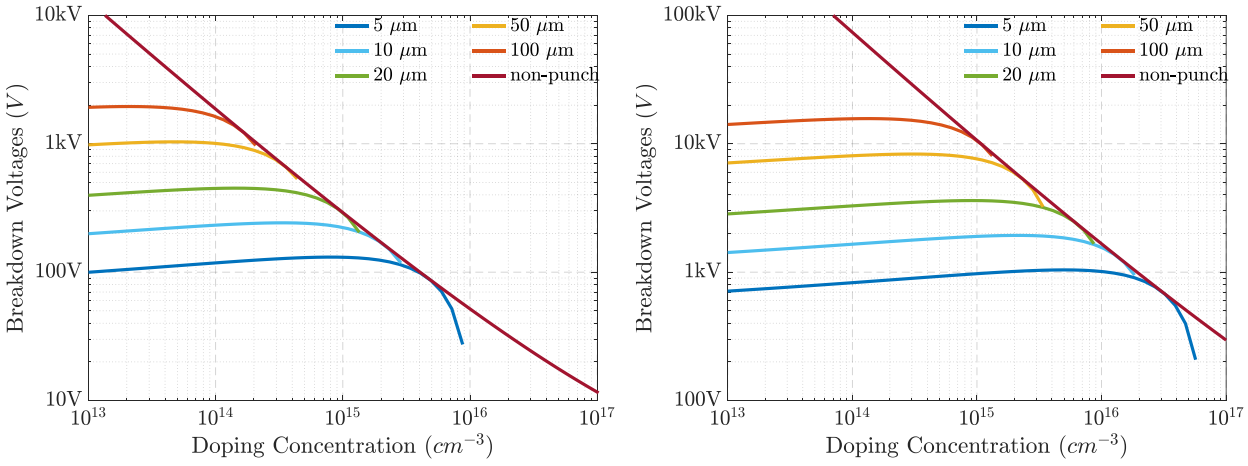


Figure 2.6. Breakdown voltages for a) Si and b) SiC punch-through PiN structures as a function of doping concentration

punch-through design and (2.16) for punch-through designs at various drift region thicknesses are shown in Fig. 2.6. As it can be seen from the comparison, with the SiC PiN structure,

it is possible obtain a breakdown voltage of $1000\,V$ with a drift region thickness of about $5\,\mu m$, while a drift region thickness of $50\,\mu m$ would be required with the Si PiN structure. In addition, for a given the drift region thickness, almost 10 times higher doping concentration can be used for SiC PiN structure compared to Si PiN. This means further on-state resistance reduction for SiC MOSFETs [2].

2.1.3 Bulk Carrier Mobilities

In semiconductor devices the movement of the carriers (electrons and holes) is the basis of the conductivity. When an external electric field is applied to a semiconductor, free carriers are accelerated by the electric field and, they travel along the direction of electric field. During movement of carriers due to an electric field, which is called drift, their velocity increase and they gain kinetic energy until they collide with ionized impurity atoms or with thermally vibrating lattice atoms [15]. When carriers are involved in collisions, or scattering events, they lose most or all, of its energy. Then the carrier will again start to accelerate and gain kinetic energy until it is again involved in a scattering process. Throughout this repeating acceleration process, the carriers will gain an average drift velocity (v_{dr}) which, for low electric fields, is directly proportional to the electric field (E) We may then write

$$v_{dr} = \begin{cases} -\mu_n E & \text{electrons,} \\ \mu_p E & \text{holes} \end{cases} \tag{2.17}$$

where μ_n and μ_p are the electron and hole mobilities, respectively. Therefore, the carrier mobility is defined as the proportionality coefficient of drift velocity on the applied field, which has the unit as $((m/s)/(V/m) = m^2/V.s)$. A higher mobility describes how easy a carrier will move in the lattice due to an electric field.

The mobility is directly proportional to the scattering time and inversely proportional to the effective mass of the carrier. Since electrons and holes have different effective masses,

their mobility in the same semiconductor is different. For scattering time, as mentioned above, there are two collision or scattering mechanisms that dominate in a semiconductor bulk and affect the bulk carrier mobility: phonon or lattice scattering, and ionized impurity scattering [19].

In lightly doped semiconductors, lattice scattering is the dominating scattering mechanism and thereby the mobility is restricted by lattice scattering. The radius of the lattice atom vibrations is a function of the temperature and it increases with an increase in the temperature. When the vibration radius of the lattice atoms increases, the probability of carriers to collide with vibrating atoms also increases. Therefore, the phonon scattering limited mobility decreases as the temperature increases.

As mentioned above, another scattering mechanism affecting the carrier mobility is ionized impurity scattering. When doped impurity atoms are ionized, they repel or attract the carriers that travel in their vicinity. This interaction is also referred to as Coulomb scattering and it causes the charge carriers to be involved in collisions or it alters the motion direction of the carriers. At higher temperatures, the thermal velocity of the carriers is higher and the carriers spend less time in the vicinity of a Coulomb force. As less time spent in the vicinity of a Coulomb force, the scattering effect will be smaller, which will increase the Coulomb scattering limited mobility [15].

Another factor affecting the Coulomb scattering limited mobility is the impurity doping concentration [19]. As the doping density increases, the number of ionized impurity centers also increases. This will increase the probability of a carrier encountering Coulomb scattering which will reduce the Coulomb scattering limited mobility.

In overall, if the mean time between two collisions due to a scattering mechanism is τ_m, then probability of a scattering event occurring due to that scattering mechanism in a differential time dt is dt/τ_m. Then, by using concept of probability, the total probability of scattering can be calculated as the sum of the probability of two scattering mechanisms. By

using this concept, the total bulk mobility μ can be found by Mathieson's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_i} - \frac{1}{\mu_l}. \tag{2.18}$$

where μ_i is the ionized impurity scattering limited mobility and μ_l is the phonon scattering limited mobility.

Since the temperature has opposite effects on the μ_i and μ_l, temperature dependence of bulk mobility is not a straightforward function. At very high doping concentrations, Coulomb scattering becomes the dominating scattering mechanism, and the overall mobility continuously increases with the temperature as Coulomb scattering effect is lower. At lower doping concentrations, phonon scattering becomes the dominating scattering mechanism at higher temperatures and the overall mobility decrease with the temperature due to strengthened phonon scattering [15].

At around room temperature, the mobility for Si can be empirically calculated as a function of temperature by [2]:

$$\mu_n(Si) = 1360 \left(\frac{T}{300}\right)^{-2.42} \qquad \text{for electrons,} \tag{2.19}$$

$$\mu_p(Si) = 495 \left(\frac{T}{300}\right)^{-2.20} \qquad \text{for holes.} \tag{2.20}$$

Similarly, the mobility for SiC can be empirically calculated as a function of temperature by

$$\mu_n(SiC) = 1140 \left(\frac{T}{300}\right)^{-2.70} \qquad \text{for electrons,} \tag{2.21}$$

$$\mu_p(SiC) = 120 \left(\frac{T}{300}\right)^{-3.4} \qquad \text{for holes.} \tag{2.22}$$

The variation of the mobility for electrons and holes in Si and SiC at around working temperature conditions are shown in Fig. 2.7 for low doping concentrations ($< 10^{15} cm^{-3}$) [2]. As seen, the mobility almost decreases by a factor of 2 between $25C$ and $125C$ for both Si

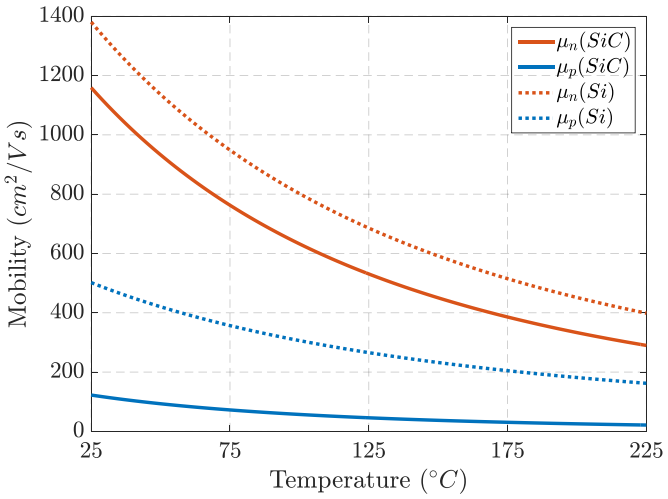


Figure 2.7. Temperature dependence of the mobility for electrons and holes in Si and SiC

and SiC which is within safe operating area for both semiconductor.

For doping concentrations below $10^{15} cm^{-3}$ and room temperature, the effect of doping concentration on the mobility is small. At larger doping levels, the mobility of electrons and holes in Si at room temperature can be empirically modeled as a function of the doping concentration by [20]:

$$\mu_n(Si) = 92 + \frac{1268}{1 + \left(\frac{N_D}{1.3 \times 10^{17}}\right)^{0.91}} \qquad \text{for electrons,} \tag{2.23}$$

$$\mu_p(Si) = 54.3 + \frac{406.9}{1 + \left(\frac{N_D}{6.3 \times 10^{16}}\right)^{0.88}} \qquad \text{for holes.} \tag{2.24}$$

Similarly, the mobility for SiC can be empirically calculated as a function of the doping concentration by [1]:

$$\mu_n(SiC) = \frac{1020}{1 + \left(\frac{N_D}{1.8 \times 10^{17}}\right)^{0.6}} \qquad \text{for electrons,} \tag{2.25}$$

$$\mu_p(SiC) = \frac{118}{1 + \left(\frac{N_D}{2.2 \times 10^{18}}\right)^{0.7}} \qquad \text{for holes.} \tag{2.26}$$

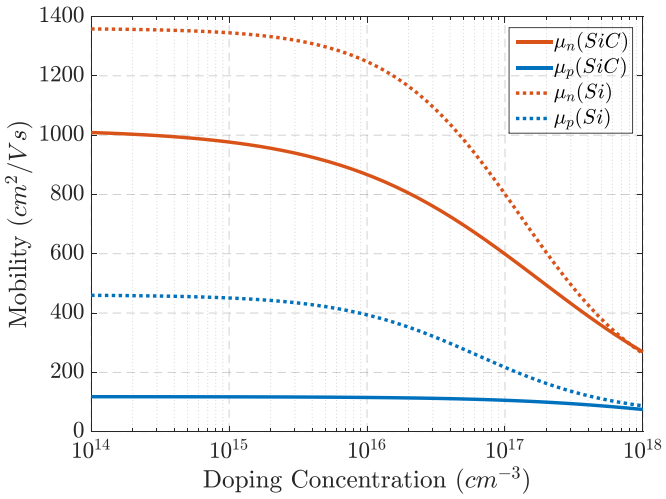


Figure 2.8. Bulk mobility for electrons and holes in Si and SiC as functions of doping concentration at T = 300 K

As seen both from Fig. 2.7 and Fig. 2.8, although the electron mobility of SiC is lower than that of Si, it is still comparable. However, for hole mobility, that is not the case. The hole mobility of SiC is more than four times lower than that of Si, which makes it hard to utilize p-type semiconductor.

2.1.4 Specific On-Resistance

An ideal power semiconductor device would be able to conduct any amount of current with zero on-state voltage drop in on-state, and it would be able to hold off any value of voltage with zero leakage current during off-state. Therefore, a good way of evaluating the performance capabilities of different semiconductor materials for high-power electronics is calculating the relationship between the specific resistance and the blocking voltage for each semiconductor.

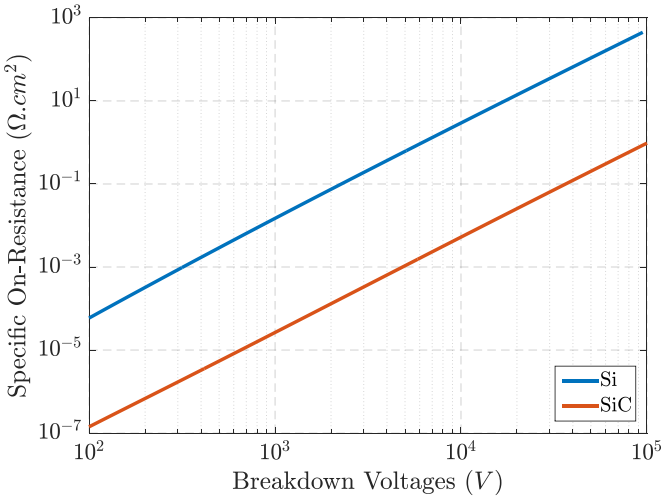


Figure 2.9. Drift region specific on-resistance ($R_{D,sp}$) as a function of breakdown voltage for Si and SiC devices

The specific on-state resistance of a power device in the drift region can be calculated as

$$R_{D,sp} = \rho.w_D \tag{2.27}$$

where ρ is resistivity and w_D thickness of the depletion region. The resistivity of the n-drift region is a function of electron concentration and mobility and can be expressed as

$$\rho = \frac{1}{q\mu_n N_D}. \tag{2.28}$$

From (2.10) we can write

$$w_N = \frac{2V_B}{E_B} \tag{2.29}$$

and from (2.11) we can write

$$N_D = \frac{E_B^2.\varepsilon_r\varepsilon_0}{2qV_B}. \tag{2.30}$$

If we combine (2.28)-(2.30) into (2.27) we can obtain the $R_{D,sp}$ as

$$R_{D,sp} = \frac{4V_B^2}{\mu_n\varepsilon_r\varepsilon_0 E_B^3}. \tag{2.31}$$

The relationship between the specific on-resistance and the blocking voltage based on (2.31) is given in Fig. 2.9 at room temperature for Si and SiC devices. For an ideal drift region, the $R_{D,sp}$ increases as the square of the blocking voltage and is inversely proportional to the cube of the critical field. since E_B is almost ten times higher in SiC compared to Si, $R_{D,sp}$ in SiC is nearly 1000 times lower as seen from Fig. 2.9. This could be utilized as much smaller drift layer resistance for the same blocking voltage or as higher blocking voltages with reduced on resistances.

2.1.5 Comparison of the Material Properties

In Table 2.1, the selected material properties of the most popular semiconductor materials in power applications, i.e. Si, SiC and GaN, are summarized. One way of interpreting these basic material parameters into a comparison of device performance is to determine the best theoretical performance achievable for each of the three semiconductor materials [5]. In overall, the energy bandgap of SiC is three times larger than that for silicon. This results in much lower the leakage currents at any given temperature, as well as much higher operation temperatures. Therefore, their higher bandgap make SiC devices a better solution for high-temperature operation compared to Si.

The higher bandgap of SiC also results in much smaller impact ionization coefficients at any given electric field, which benefits the SiC with ten times higher critical electric field strength. The higher breakdown field strength of SiC devices allows much less drift layer thickness and specific on-resistance for power devices. Therefore, SiC devices have much lower conduction losses compared to Si devices.

Another superiority of SiC as a material is its higher conductivity. The thermal conductivity for SiC is two to three times higher than silicon, which improves the heat spreading and dissipation capabilities of SiC devices. In order to graphically compare the critical material properties, a proportional comparison of six key material properties are given in Fig. 2.10 as a radar chart.

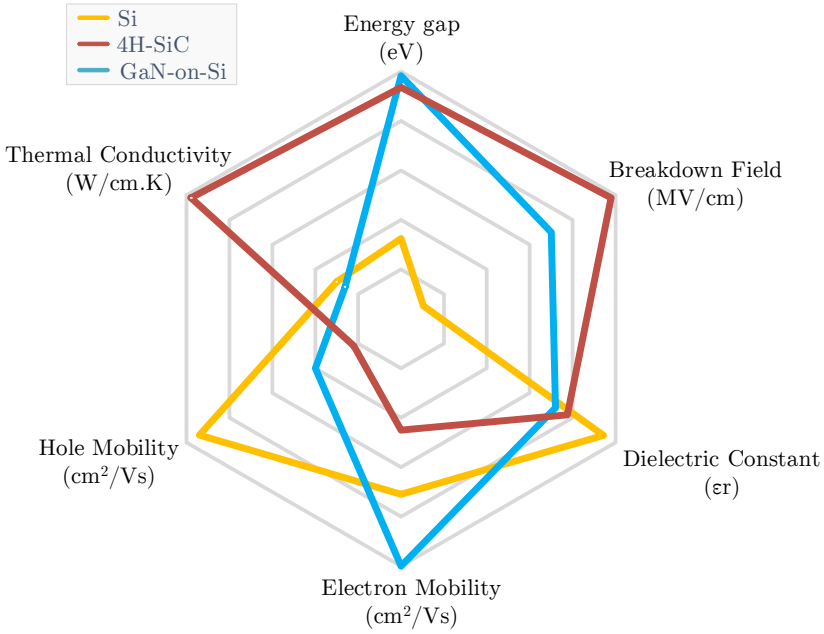


Figure 2.10. Comparison of major material properties of Si, SiC, and GaN

2.2 Reliability and Performance Issues of SiC MOSFETs

The superior features of SiC MOSFTETs such as low leakage current at high temperature make them highly promising for automotive power train, oil & gas down-hole tractors and some military applications where the junction temperature is higher than 175°C. Operating in such a harsh environment, SiC MOSFETs are subjected to various thermo-mechanical stress, electrical stress, and even mechanical vibrations. Since it is a relatively new technology, limited information is available regarding the long-term reliability of SiC MOSFETs from the field application. Therefore, to provide feedback for technology improvement and minimizing destructive failures in the device, it is essential to evaluate the long-term reliability of the state-of-art SiC MOSFETs, especially in high temperature environment. The degradation mechanisms in a semiconductor device can be classified into two main categories: package related degradation mechanisms and die related degradation mechanisms. In this section, the most common degradation mechanisms in SiC MOSFETs are introduced.

2.2.1 Package Related Degradation Mechanisms

In practical power converter applications, the power semiconductor devices always heat up and cool down due to varying load conditions, switching actions, electrical cycles, etc. This temperature cycling leads to thermo-mechanical stresses on the adjacent layers due to the differences in coefficient of thermal expansion (CTE) and eventually wears out the contact points. The temperature cycling related stress may cause packaging related degradation mechanisms such as the bond wire crack, bond wire lift-off, and die attach solder degradation [8].

Due to high costs of SiC, the size of the chips are usually much smaller compared to Si devices at the same voltage level [21]. Hence, for the same power level, the SiC chips have higher power density and they require better heat dissipation and cooling design in order to handle higher local current densities. This makes the SiC devices more prone to packaging related degradation. Due to largest CTE mismatch between SiC die and the aluminum bond wire, the most critical interface is the bond wire attachment. Being bonded directly onto the active chip surface, particularly the bond pad interface is exposed to the full thermal swing with varying load conditions. The most common packaging related failure mechanism is formation of a crack at the tail of the bond, which then propagates within the wire material which gradually lead to loss of electrical conductivity [22].

2.2.2 Gate Oxide Related Degradation Mechanisms

The major reliability concern for SiC MOSFETs is the gate oxide degradation. The degradation can be either interface or oxide related with different outcomes. Both of these issues are very critical for SiC MOSFETs, while the first one degrades the device performance drastically, the latter may increase the gate leakage current or further lead to device breakdown.

The interface related degradation is very severe in SiC MOSFETs due to several reasons. Firstly, during thermal oxidation of SiC, the carbon atoms need to be removed from the

system. Since it has not been possible to remove all C atoms, remaining one may lead to traps at the SiC/SiO_2 interface. Moreover, the larger bandgap property of SiC decreases the conduction and valance band offsets between the SiC semiconductor and the SiO_2 dielectric and makes them susceptible to higher Fowler-Nordheim tunneling currents. Finally, high temperature operation of SiC MOSFETs with a positive gate bias aggravates the SiC/SiO_2 interface traps and expedites the gate oxide degradation [23]. All of these issues are also affecting the oxide reliability.

In addition to these issues, the oxide reliability is further aggravated in SiC MOSFETs, due to the requirement of a thinner gate oxide layer in order to keep the gate voltage threshold at reasonably low values. This makes SiC devices more sensitive to higher drain voltage gradients and high temperature pulses which can result in high gate leakage currents and makes them particularly susceptible to gate leakage failures. From the failure mode statistical distribution in SiC MOSFETs under short circuit robustness tests, the breakdown of the gate oxide is found to be the most common failure mode (62% of the 40 reported failures)[24]. Since oxide degradation is only detectable with high gate leakage close to the failure, it cannot be monitored through lifetime [25]. Therefore, in this study, only interfacial degradation will be monitored and from now on, it will be referred as gate oxide degradation.

CHAPTER 3

DEGRADATION ASSESSMENT AND PRECURSOR IDENTIFICATION FOR SIC MOSFETS UNDER HIGH TEMP CYCLING

Regarding the long-term reliability of the SiC MOSFETs, the SiC/SiO_2 interface charge trapping related gate threshold voltage drift is a major concern. It is mainly caused by the decrease in the conduction band offset at semiconductor crystal - SiO_2 interface [23, 26], and it can degrade under thermo-mechanical or electrical stress especially under high-temperature environment and drastic temperature variation. Previously, to study SiC MOSFETs reliability under high temperature, high temperature gate bias (HTGB), gate switching and high temperature stress tests at 175°C and 200°C have been carried out [27, 28]. Nonetheless, the thermo-mechanical stress due to temperature variation is not studied in detail and the feasibility of long-term operation is not evaluated. To obtain a more comprehensive evaluation, power cycling tests (PCTs) are preferred, and a few studies have investigated the long term reliability of SiC MOSFETs [29, 30, 31]. It is observed that the on-resistance is increased as the devices are aged. However, it is still not clear whether this on-resistance is because of the package-related degradation or the gate interface degradation induced threshold voltage change. Also, the maximum junction temperature is below 175°C and cannot represent the high temperature operation condition for SiC MOSFETs. Therefore, a long-term reliability study of SiC MOSFETs under high temperature operation and high temperature swing is needed through various power cycling tests.

This chapter comprehensively evaluates the long-term degradation mechanisms of commercially available SiC MOSFETs under high temperature operation and high temperature swing. In addition to parameter variation analysis throughout aging, parameter shift assessment and aging precursors identification are equally important for real-time or in-situ health monitoring of the SiC MOSFETs in power converters. For example, based on the parameter shifts in Si devices (such as on-resistance, threshold voltage, gate leakage current,

and switching transient variation), different detection circuits have been implemented in the converter system to monitor the parameter variation and indicate the device aging [32]. Similarly, the early fault diagnosis circuits and algorithms can be developed for SiC MOSFETs as well. Nonetheless, before deploying a certain parameter as an aging precursor, it is meaningful to evaluate and compare their feasibility in terms of practical implementation and their correlation to degradation mechanisms.

The chapter is organized as follows: In Section 3.1, the basic operating principle of the power cycling test setup and the aging condition of the devices are introduced. An accelerated power cycling test method is performed based on a custom-designed test bed. Afterwards, in Section 3.2, the variations of the devices intrinsic parameter are investigated, and the experimental results are presented. Considering both device physics aging and package-related degradation, a complete analysis is provided as well to explain each parameters variation. In Section 3.3, the suitability of these parameters as aging precursors is investigated considering implementation issues. Lastly, the conclusions are given in Section 3.4 summarizing the experimental results and analysis.

3.1 Accelerated Power Cycling Tests

Temperature and power cycling are two widely acknowledged test methods to investigate the effect of periodical temperature changes on the device packaging. The temperature cycling changes the device temperature by varying the environmental temperature between the upper and the lower limits. This testing method is preferred to test interfaces with a large area like the baseplate solder in power modules, and the testing conditions are quite different from the actual operation conditions. On the other hand, power cycling method uses active heating where the devices are heated up by the power loss within the chips, and are cooled down with the traditional cooling methods. This provides a thermal and stress

distribution similar to real application conditions. By controlling the current or on/off time, the temperature can also be regulated during the heating and the cooling phases [29].

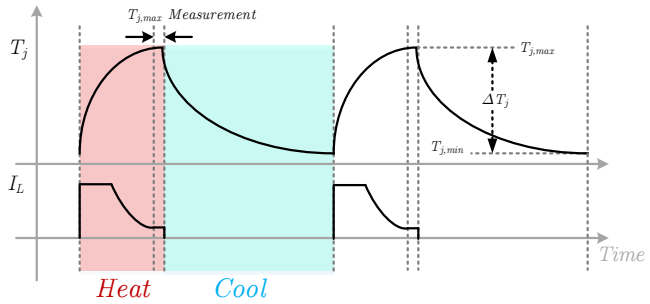


Figure 3.1. Operation principle of the power cycling test setup.

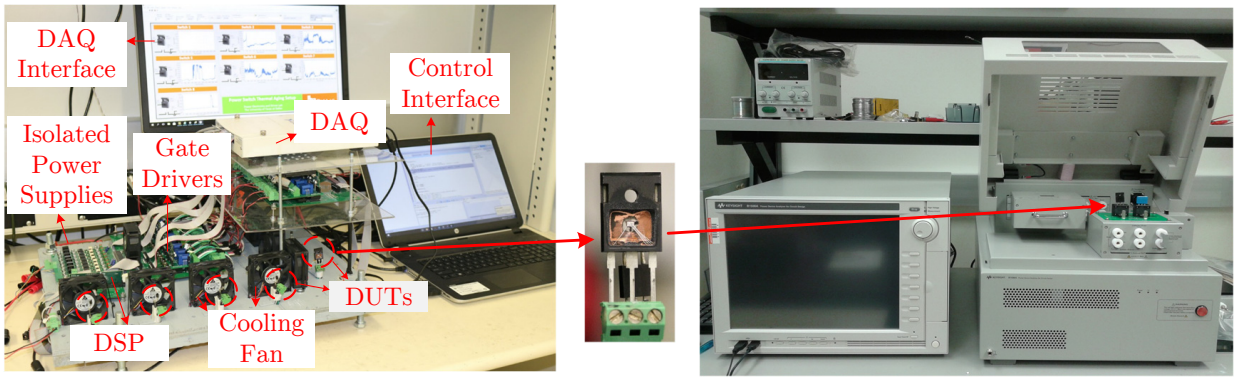


Figure 3.2. Illustration of the test-bed; (a) custom designed aging setup, (b) curve tracer.

In order to accelerate the aging process, various accelerated power cycling test schemes are used to mimic the field conditions as much as possible [33, 34]. However, acceleration of aging process requires both high temperature swings and short cycling periods. In most of the studies, this is achieved by mounting the devices under test (DUTs) on a cooling system, and injecting a relatively high load current. This approach increases the thermo-mechanical stress on the bond wires, and bond lift or heal crack is more easily observed. In this study, the devices are actively heated up without a heat sink to achieve a high junction temperature at relatively small current values without causing overstresses in the

wire bond. The injected current is controlled within the rated current value of the DUT and the timing is adjusted by a closed loop system comparing the reference and estimated junction temperatures. Specifically, the heating current is selected to be half the rated current in all aging conditions. Forced air-cooling through fans is implemented to cool down the DUTs [35].

During the aging tests, it is essential to acquire an accurate junction temperature T_j from each DUT as a feedback for close-loop junction temperature control. Various methods like thermocouple-based sensor, contactless IR setup and temperature-dependent electric parameter (TSEP) estimation have been proposed to obtain junction temperature [36]. Each of these methods has particular advantages and disadvantages. Using a TSEP is the most popular method for discrete devices since it is non-invasive and does not require de-capsulation. The on-state resistance, gate threshold voltage and reverse body diode voltage are the most commonly used TSEP parameters. However, recent studies shows that these parameters change as devices degrade [30, 31] and periodic recalibration is required.

In this study, a simple solution is proposed by estimating the T_j from the thermocouples directly attached to the metal tab of the device. To minimize the difference between the measured case temperature from the thermocouple and the devices junction temperature, the generated power loss is reduced by lowering drain current during the junction temperature measurement period as indicated in Fig. 3.1. Specifically, when the voltage of a switch rises up to its defined limit, the drain current is decreased to a small value. Then, according to (3.1), the measured case temperature can represent the junction temperature of the device if the drain current is kept relatively small. Furthermore, the temperature readings are periodically calibrated with IR camera measurements to improve the accuracy of the temperature measurements. The calibrated parameter values are updated at certain cycles to eliminate possible errors due to variation of thermal impedances through aging [35].

$$T_j = T_{case} + R_{jc}(I_{ds}^2.R_{ds,on}) \tag{3.1}$$

The power cycling tests are performed on a configurable custom-designed test setup as shown in Fig. 3.2 (a). For this study, 1.2 kV/11 A discrete SiC MOSFETs are aged with a junction temperature swing from 30°C to 200°C. The devices are actively heated up with a constant current of 4.5A and then cooled down until they reach to the minimum temperature limit. 7 devices are tested at the same time but with independent temperature controls. In this configuration, a complete cycle typically takes around three minutes (60 sec heating and 120 sec cooling). After each cycle, the drain to source voltage, case temperature and drain current data of each switch are stored by the data acquisition system for online on-state resistance ($R_{ds,on}$) measurement. After each 250 aging cycling, the devices are tested on the Keysight B1506A curve tracer for parameter evaluations and comparisons at different aging cycles as indicated in Fig. 3.2 (b).

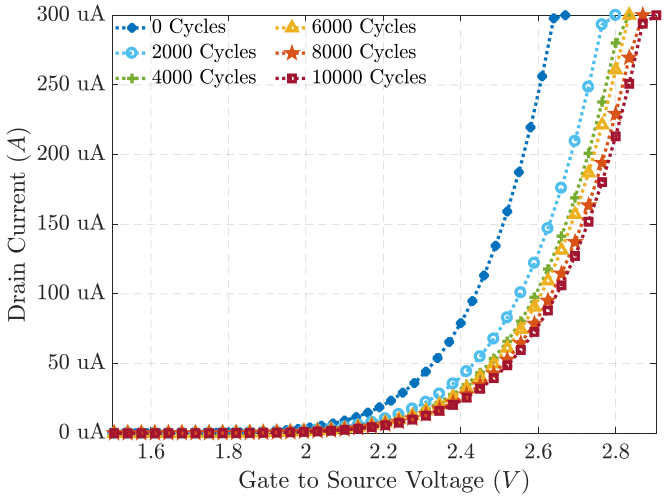


Figure 3.3. Transfer characteristic measurements for 2C-5 versus power cycles.

3.2 Variation of Static Electrical Parameters

Generation-II SiC MOSFETs are used in the accelerated aging tests which last for several weeks. The devices under test (DUT) are named as *2C-x* where *2C* depicts the set of devices from the same batch and aged under same conditions and x shows the item number. At

each 250 cycle interval, the cycling is stopped and a systematic static parameter evaluation of each device is performed at room temperature with the aid of the Keysight B1506A curve tracer. In the following sections, the static parameter variations are presented.

3.2.1 Variation of Threshold Voltage (V_{th})

The gate oxidation trap is a well-known issue in SiC MOSFETs, and it can cause the threshold voltage instability. Moreover the threshold voltage (V_{th}) is often presented as a precursor parameter for Si devices in the literature. Therefore, the V_{th} variation over aging is presented first as a transfer characteristic I-V curve for one of DUTs in Fig. 3.3 and as quantitative data for all DUTs in Fig. 3.4. From Fig. 3.3, it is clear that transfer characteristic of 2C-5 is shifting to the right side throughout the aging which means that threshold voltage is increasing. The quantitate threshold voltage data in Fig. 3.4 shows an increase of the threshold voltage by 7.1% to 10.7% at the end of the aging test. Theoretically, the threshold voltage of the SiC MOSFET can be calculated by [37]:

$$V_{th} = V_{th0} - \frac{Q_{ot}}{C_{ox}} + \frac{qN_{it}}{C_{ox}} \tag{3.2}$$

where Q_{ot} is oxide trapped charge, q is the fundamental electronic charge. N_{it} is interface trap density, and C_{ox} is oxide capacitance. The ideal threshold voltage V_{th0} can be found by:

$$V_{th0} = \frac{\sqrt{4\varepsilon_s kTN_A ln\left(N_A/n_i\right)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{3.3}$$

where ε_s dielectric constant in SiC, k is Boltzmanns constant, T is the absolute temperature, N_A is the p-well region doping, and n_i is the intrinsic carrier concentration of SiC.

The reason for this gradual increase in threshold voltage is suspected to be caused by the gate oxidation degradation related interface trapped charge (Q_{it}). As can be seen from (3.2), the existence of near interface trapped charge can increase the threshold voltage. For SiC devices, the SiC/SiO_2 interface can cause reliability problems and several studies have

demonstrated the gate threshold voltage instability in SiC devices [23, 26]. While it is not a problem for Si devices, the gate oxide interface issue in SiC devices is caused by different phenomenons related to material properties of SiC devices. Although both Si and SiC based MOS devices use SiO_2 as the gate dielectric, the consequential barrier height and conduction band offset difference between SiC and SiO_2 is smaller than that of Si counterpart. This phenomenon leads to the enhanced tunneling current through the gate oxide. The second reason is the high electric field in the gate oxides in SiC MOS devices considering the high blocking capability of SiC. Lastly, SiC has a higher defect density in the substrate and in the gate oxide compared to the Si devices. Although these properties do not bring serious reliability concerns under normal operation conditions, high temperature operation with a positive gate bias aggravates the SiC/SiO_2 interface traps and expedites the gate oxide degradation. From the experimental results, a positive shift of threshold voltage is always observed over the aging cycles.

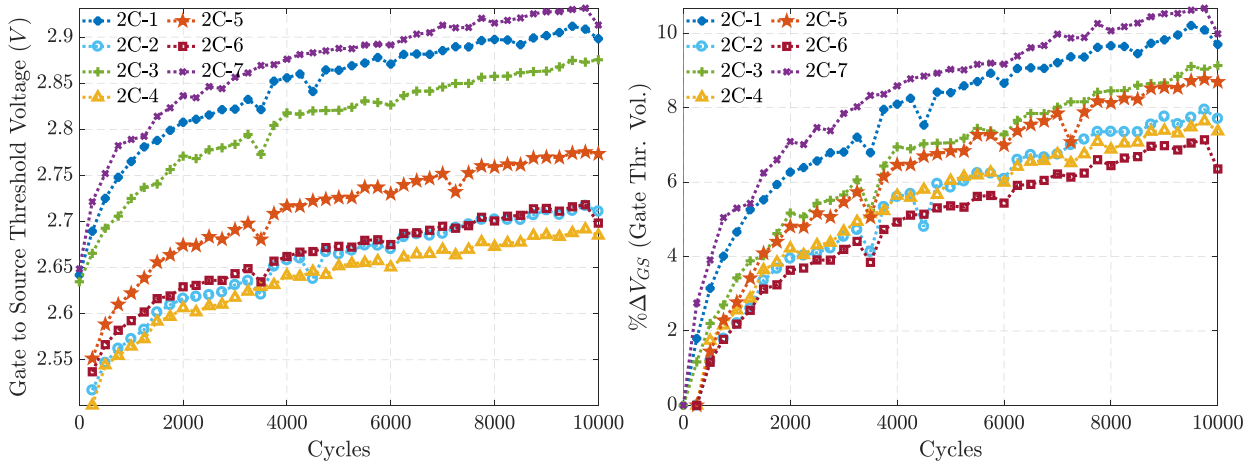


Figure 3.4. Threshold voltage shift over power cycles (@$Id = 250\mu A$) (a) Absolute value (b) Variation in percentage .

3.2.2 Variation of On-resistance ($R_{ds,on}$)

Another parameter that is often presented as an aging precursor for both Si and SiC MOSFETs is the on state resistance. The on-resistance variation over the aging cycles for the DUTs is presented in Fig. 3.5. A gradual increase is observed for all the devices before the first 6500 cycles. This trend is similar to the threshold variation except that the percentage of the increase is different. To explain this steady increase of on-resistance, the composition of $R_{ds,on}$ is explored as indicated in (3.4):

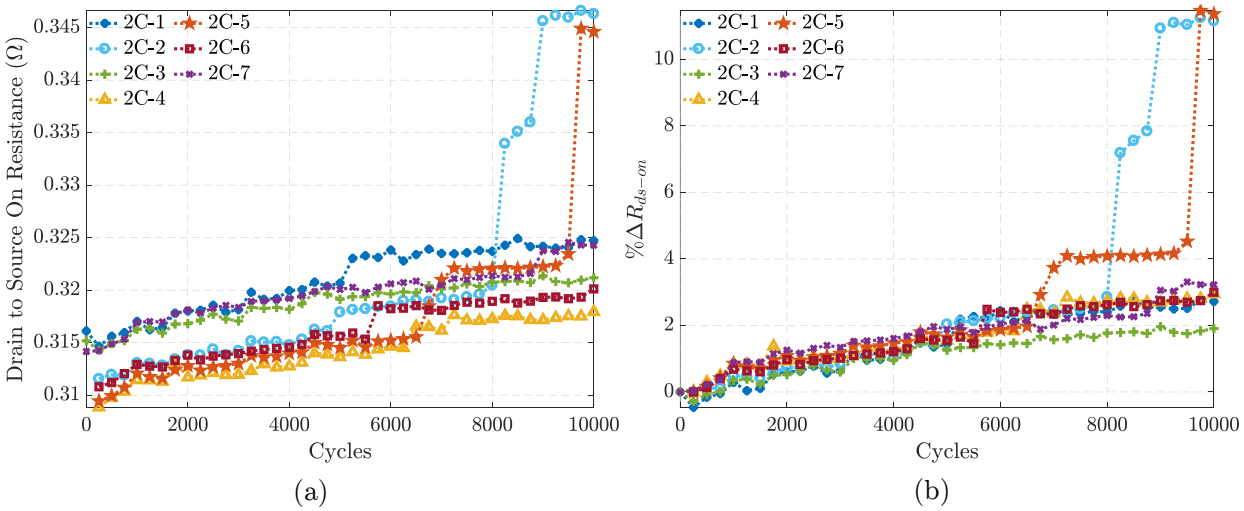


Figure 3.5. On-resistance shift over power cycles ($@Id = 4.5A$, $@V_{gs} = 20V$) (a) Absolute value (b) Variation in percentage.

$$R_{ds,on} = R_S + R_{ch} + R_A + R_{JFET} + R_D + R_{subs} \tag{3.4}$$

where R_S is the source contact resistance, R_{CH} is the channel resistance, R_A is the accumulation region resistance, R_{JFET} is the resistance of the JFET region, R_D is the resistance of the drift region, and R_{subs} is the resistance of the $N+$ substrate. The physical meaning of all these resistances is illustrated in Fig. 3.6. Among the different components of on-state resistance, only R_{CH} and R_A are dependent on V_{th}. Specifically, the channel resistance and accumulation region resistance are represented by

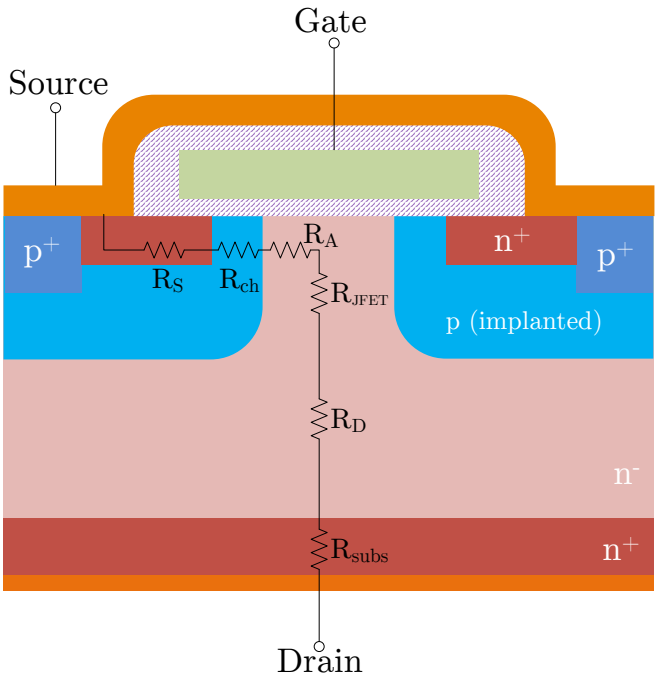


Figure 3.6. Physical composition of on-resistance in a power MOSFET.

$$R_{ch} = \frac{L_{ch}}{W_{ch}.\mu_n.C_{ox}\,(V_{gs} - V_{th})} \tag{3.5}$$

$$R_A = \frac{L_A}{W_A.\mu_{nA}.C_{ox}.\,(V_{gs} - V_{th})} \tag{3.6}$$

where L_{ch} is the channel length, W_{ch} is the channel width, μ_n is the electron mobility of the inversion layer channel in SiC material, L_A is the accumulation region length, W_A is the accumulation region width, μ_{nA} is the electron mobility of the accumulation layer and V_{gs} is the gate drive voltage.

During the aging process, the channel length and width are assumed to be constant as these parameters are mainly determined by the manufacturing process and are constant over aging. The oxide capacitance can possibly change because of the degradation in the gate oxidation. However, as it can be seen from the experimental results of Cox for sample 2C-5 in Fig. 3.7, C_{ox} remains almost constant over the aging cycles.

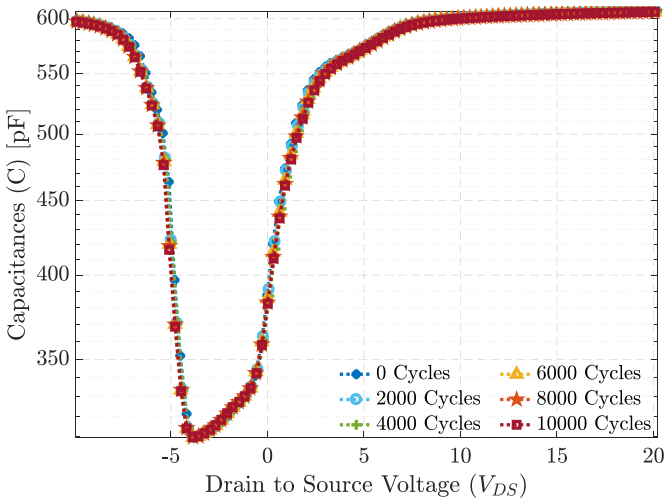


Figure 3.7. Variation of C_{ox} over aging cycles.

However, as discussed previously, the V_{th} is always increasing during the aging process. Consequently, according to (3.5) and (3.6), the R_{CH} and R_A are increasing due to the V_{th} drift. This provides a possible explanation for the steady increase of $R_{ds,on}$ in experiment. In order to magnify the effect of V_{th} drift on $R_{ds,on}$, the $(V_{gs} - V_{th})$ term in (3.5) can be lowered by decreasing the gate voltage. With a reduced gate voltage, the channel resistance becomes more dominant compared to the 20 V case where the channel is fully on and $R_{ds,on}$ is dominated by the drift region resistance R_D. As a result, the on-resistance increases more rapidly over the aging process at lower gate voltages as indicated in Fig. 3.8. These results are consistent with assumptions and verify that the steady increase of $R_{ds,on}$ mainly caused by V_{th} drift. In addition, as it mentioned above, the threshold voltage increase by 7.1% to 10.7%. Correspondingly, the channel resistance R_{CH} can be calculated to increase by 1% to 1.7% at the 20 V gate bias. However, ignoring the sudden increases of on-resistance in two DUTs, the real on-resistance is increased by 1.9% to 3.3% at a gate voltage of 20 V. This calculation shows that the V_{th} shift is not the only factor causing $R_{ds,on}$ increase. In reality, the electron mobility in the equations of the R_{CH} and R_A can be also affected by the

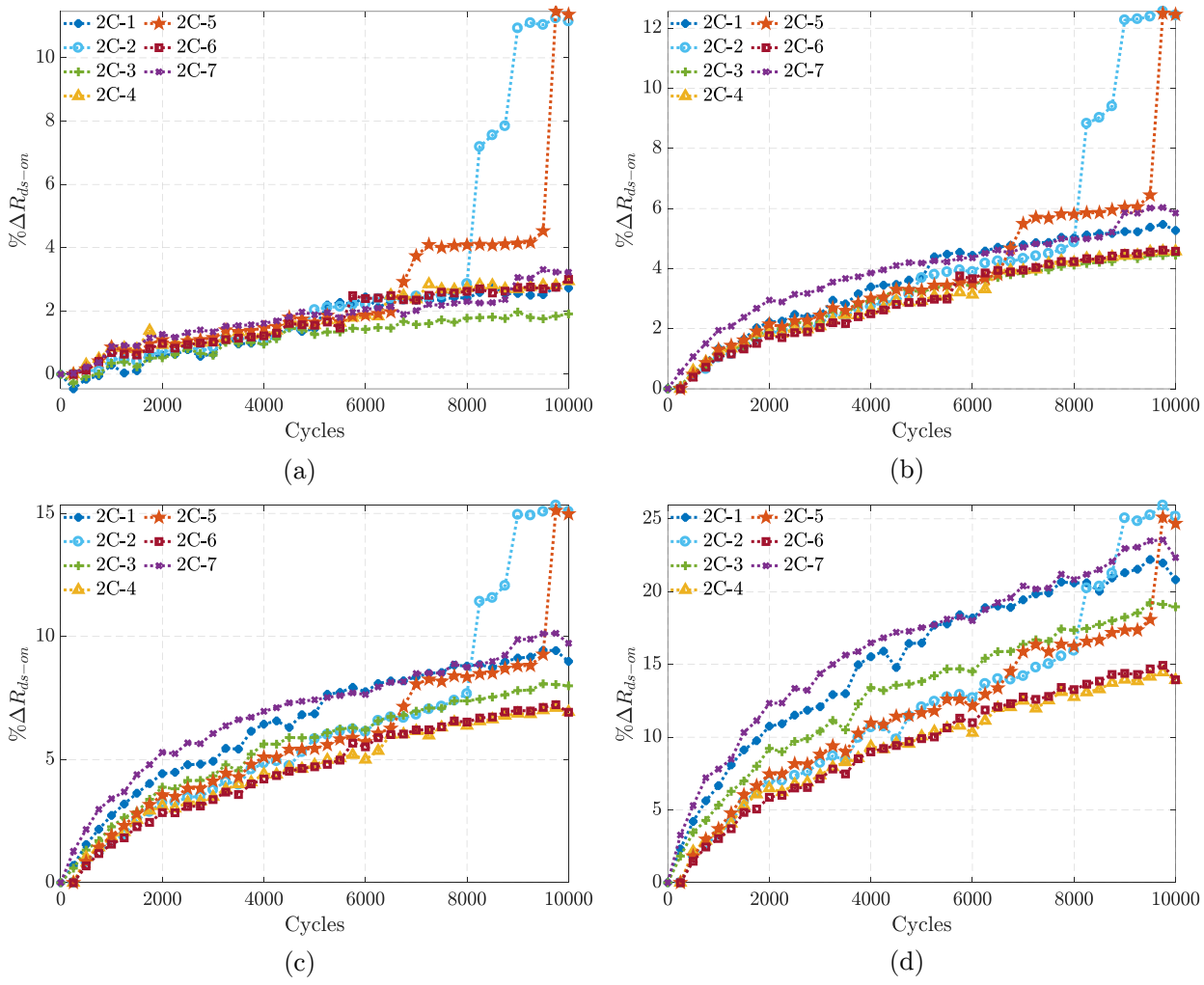


Figure 3.8. Comparison of on-resistance increase at different gate voltages (@$Id = 4.5A$) (a) $V_{gs} = 16V$ (b) $V_{gs} = 14V$ (c) $V_{gs} = 12V$.

trapped charges. Specifically, the electron mobility of a layer can be calculated as

$$\mu = \frac{\mu_0}{1 + \frac{\alpha_0 Q_{ot}}{q} + \frac{\alpha_1 Q_{it}}{q}} \tag{3.7}$$

where μ_0 is the mobility without oxide trapped charge and interface traps, and α_0 and α_1 are the model parameters. As it can be seen from (3.7), the existence of near interface trapped charge decreases the mobility which further increases the R_{CH} and R_A. From these calculations, it can be concluded that the steady increase of $R_{ds,on}$ is caused by both the positive V_{th} shift and the decreased mobility.

Besides the threshold voltage and electron mobilitys impact on $R_{ds,on}$, the package-related degradation can also affect the on-resistance. As can be seen from Fig. 3.5 and Fig. 3.8, a sudden increase of on-state resistance is observed for 2C-2 and 2C-5. Mostly, the bond wire crack, bond wire lift-off or solder degradation on the drain side of the device contribute to this sudden on-resistance increase.

3.2.3 Variation of Body Diode Characteristics (V_{SD})

Another precursor parameter which is commonly used in the literature for Si devices is the body diode voltage. The variation of body diode voltage drop at $-3A$ drain current and -10V gate bias through aging is given in Fig. 3.9. As it can be seen from the figure, the variation in body diode voltage drop is almost negligible over power cycles for most of the devices. However, devices 2C-2 and 2C-5 shows a jump after 6500 cycles which is consistent with the sudden increases of on-state resistances. The results of body diode voltage variation support our hypothesis that the sudden increase in on-state resistance is related to the degradation in packaging. To be specific, at a negative voltage of -10V, the current path of the diode conduction does not include the channel, and consequently the threshold voltage drift would not affect the body diodes voltage drop. Although on-state resistance is constantly increasing, steady trend of body diode voltage shows that constant increase in on-state resistance is caused by channel resistance component of it. Therefore, it is suspected that the sudden increase of body diodes voltage is mainly caused by the package-related degradation. This assumption needs to be validated through further evidence as discussed in Chapter 4.

3.2.4 Variation of Drain to Source Leakage Current (I_{dss})

At every measurement interval, the drain-to-source leakage current I_{dss} of the switches is recorded at different drain to source voltages. Typically, I_{dss} is within μA range at the

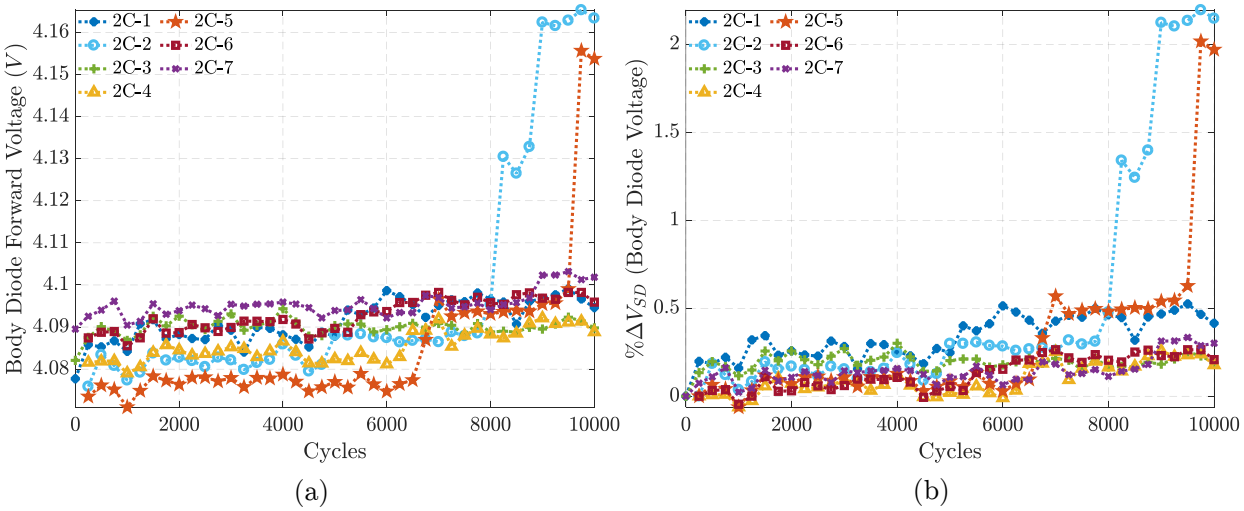


Figure 3.9. Reverse body diode voltage drop variation over power cycles (@$Id = -3A$, @V_{gs} $= -10V$) (a) Absolute value (b) Variation in percentage.

nominal blocking voltage. In order to detect any possible leakage issue more easily, the leakage current is measured at a higher voltage than the nominal blocking voltage. The variation of I_{dss} over aging cycles is given in Fig. 3.10 at 1450 V. As can be seen, the drain leakage current is negligible and well under the manufacturer acceptable limits. From these results, it can be concluded that all switches are functional with good blocking capabilities by the end of the aging cycle.

3.2.5 Variation of Gate Leakage Current (I_{gss})

In SiC MOSFETs, the gate oxide layer thickness is lower than that of Si devices in order to keep the gate threshold voltage at a reasonably low value. This makes SiC devices more sensitive to higher drain voltage gradients and high temperature pulses which can result in high gate leakage currents (I_{gss}) and makes them particularly susceptible to gate leakage failures. From the failure mode statistical distribution in SiC MOSFETs under short circuit robustness tests, the breakdown of the gate oxide is found to be the most common failure mode (62% of the 40 reported failures) [24]. In another study, I_{gss} is found to be increasing

with the aging of the devices under high drain current pulses (40A) [25]. Therefore, the variation of I_{gss} throughout the aging is given in Fig. 3.11 at the gate bias of 25V. As it can be seen, the gate-leakage currents were negligible and well under the manufacturer acceptable limits. Consequently, its concluded that the gate leakage does not show an increasing trend with aging.

However, as reported earlier [25], a sudden increase of gate leakage current is found in SiC MOSFETs. It is mainly because, in case of short circuit or high drain current pulse stresses, the local temperature rise under the bond wires can cause degradations in the gate oxide layer which leads to increased leakage current to flow and eventually result in the failure in the gate. In this study, the current value is kept at the half rated current and the bond wires are not overstressed. Correspondingly, the gate leakage problem is not observed.

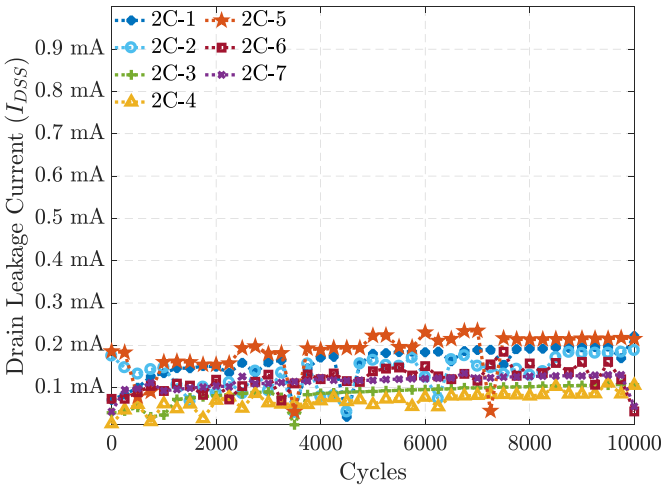


Figure 3.10. Variation of drain leakage current over aging cycles ($@V_{ds} = 1450V$).

3.2.6 Variation of Parasitic Capacitances

Another parameter presented as a precursor in the literature both Si MOSFETs is the parasitic capacitances. In Fig. 3.12, the variation of input capacitance (C_{iss}), output capacitance (C_{oss}), and reverse capacitance (C_{rss}) are plotted over aging cycles for all blocking voltage

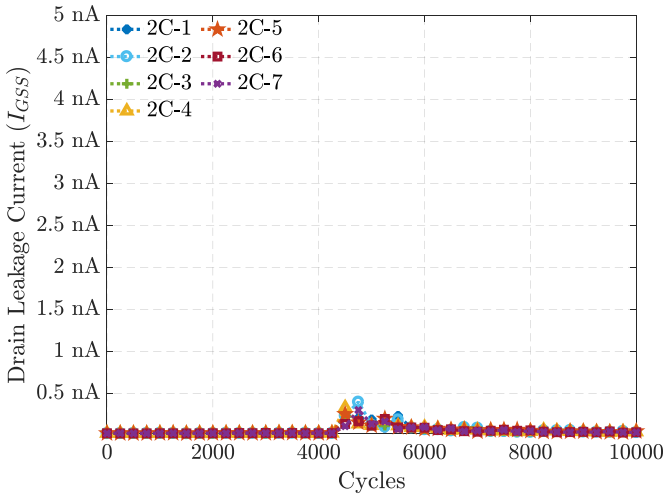


Figure 3.11. Variation of gate leakage current over aging cycles ($@V_{gs} = 25V$).

range. If this is evaluated together with C_{ox} parasitic capacitance, it can be concluded that the parasitic capacitances do not show a noticeable variation over aging.

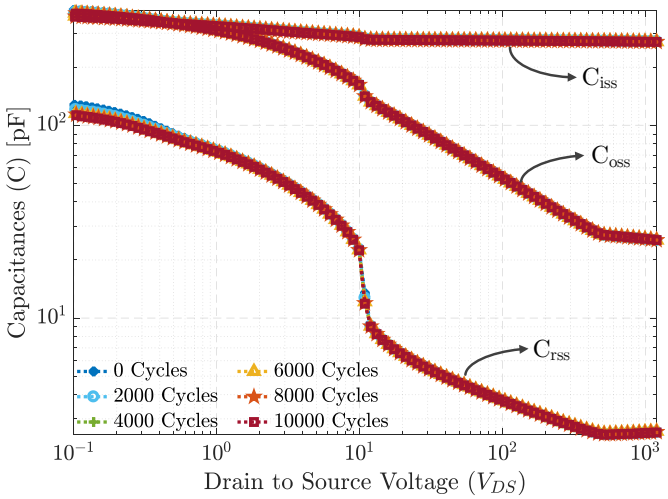


Figure 3.12. Variation of input, output and reverse capacitances over aging cycles.

3.3 Comparison of Failure Precursors for Condition Monitoring

As shown in Section 3.2, three potential failure precursors for SiC MOSFETs, i.e., the threshold voltage V_{th}, the on-state resistance $R_{ds,on}$, and the body diode voltage V_{SD} are

found to be changing over the aging process. In this section, these parameters are evaluated to find out their suitability as aging precursors in terms of practical implementation issues.

The precursors are evaluated in terms of measurement feasibility when the power converter is operating. Among the three parameters, the $R_{ds,on}$ measurement is relatively more straightforward then others. Yet, there are some challenges to carry out the $R_{ds,on}$ measurement during converter operation. Specifically, the $R_{ds,on}$ values are significantly low in SiC devices, therefore, the measurement circuit is required to have a high resolution to obtain the variation of on-state resistance in the range of several milliohms. In addition, the circuit needs to block the high voltage when the device is in the off state, which makes the measurement circuit complicated.

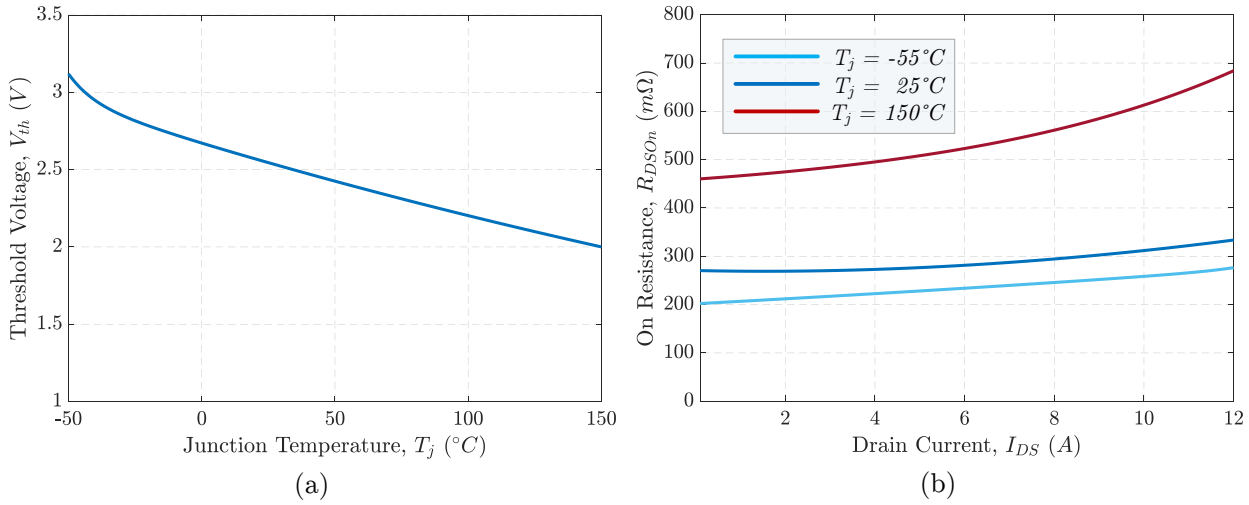


Figure 3.13. Variation of electrical parameters according to operating conditions (a) Variation in threshold voltage vs.temperature (b) Variation in on resistance vs.current for various temperatures.

The second criterion is the dependence of the parameter on the electrical and thermal conditions. When the converter is operating, the drain current and the junction temperature are determined by the load profile and the cooling design, and these conditions are changing all the time. In Fig. 3.13(a), the variation of the V_{th} over junction temperature is presented.

To use V_{th} as a failure precursor, the measurements should be carried out at an identical junction temperature or the measured value needs to be calibrated according to the junction temperature. Although the calibration may seem straightforward, the precise measurement of junction temperature is challenging. In Fig. 3.13(b), the variation of the $R_{ds,on}$ at different drain current and junction temperature is presented. As can be seen here, the $R_{ds,on}$ depends on both the drain current and the junction temperature. Similar observation also applies to the V_{SD} characteristics. Consequently, using $R_{ds,on}$ or V_{SD} as a failure precursor would require the measurements at identical load current and junction temperature conditions. Otherwise, a calibration procedure should be conducted both for drain current and junction temperature to compensate operating condition dependencies.

Another criteria for assessing the feasibility of the failure precursor is its variation in each degradation mechanism, i.e. gate oxide aging and packaging-related aging. As it is discussed in Section III, V_{th} drift only reflects the gate-oxide degradation and it exhibits a fairly good sensitivity to detect the aging. However, V_{th} is immune to packaging-related degradation and it is less feasible to use to detect packaging-related aging. The variation of the $R_{ds,on}$ unveils both chip-related and packaging-related degradation mechanism since $R_{ds,on}$ is affected by both the channel resistance and ohmic contact resistances. However, when the channel is fully on, the channel resistance constitutes a small part of the $R_{ds,on}$, and this reduces the sensitivity of it to the gate oxide degradation. To be more specific, the $R_{ds,on}$ variation due to die-related aging is calculated between %1.9-3.3 while it increases by %8.2-9.3 due to package-related aging from the experimental results. To improve the sensitivity of the gate oxide degradation detection using on-resistance, the gate voltage can be reduced to make the channel resistance more distinguishable as indicated in Fig. 3.8. But, this requires the availability of different gate voltage levels and might not be feasible for all applications. Moreover, since the $R_{ds,on}$ is influenced by both types of degradation, it is not possible to detect the root cause of the degradation by monitoring the $R_{ds,on}$. The variation of V_{SD} only

reflects packaging-related degradation while it is immune to the gate oxide aging. Although the sensitivity of this indicator seems fairly low, its ability to show the quality of contact resistances can be promising. All the above discussions are summarized in Table 3.1.

As it is pointed out in the first two criteria, it is more challenging to measure these parameters during converter operation. Since all there indicators are junction temperature dependent, implementing in-situ monitoring is easier where current level can be controlled and the average junction temperature is relatively stable. Moreover, in case of in-situ monitoring, it is not necessary to halt the converter operation and these measurements can be carried out as a subroutine of the startup procedure. Since V_{th} and V_{SD} indicates condition of chip-related and packaging-related degradation respectively, it is suggested to monitor these two indicators simultaneously. In this case, condition monitoring setup will be capable of capturing both degradation mechanisms independently. If the root cause determination is not big importance and different voltage levels are available in the gate driver, then $R_{ds,on}$ can also be used to monitor the overall condition of the switch.

Table 3.1. Practical Implementation Feasibility of Parameters

Precursor	% Variation		Temperature Dependency	Load Dependency	Operation Disruption
	Die aging	Package aging			
V_{th}	$7-11$	$-$	Yes	No	Yes
R_{ds}	$1.9-3.3$	$8.2-9.3$	Yes	Yes	No
V_{sd}	$-$	$2-2.3$	Yes	Yes	No

3.4 Conclusion

In this chapter, a comprehensive reliability and aging evaluation of SiC MOSFETs is presented for high temperature applications. The power switches are exposed to high temperature power cycling, and key parameters are measured using an automated curve tracer

at certain intervals and variations of electrical parameters with respect to aging cycles are presented. It has been shown that on-state resistance, and gate threshold voltage are the electrical parameters that remarkably increases with aging for all devices. On the other hand, body diode voltage drop under -10V gate bias suddenly increased only for two devices which is consistent with the rapid increases in on-state resistances of the same devices. After a detailed analysis, the threshold voltage drift and continuous increase in on-state resistance is found to be related to the gate oxide degradation. On the other hand, it is concluded that sudden increases in body diode voltage drop and on-state resistance are due to packaging-related issues. These findings are also verified with a detailed failure analysis. Since all parameters are closely related to operation conditions, in-situ monitoring with the ability to control electrical and thermal conditions is proposed. Simultaneously monitoring the threshold voltage and body diode voltage drop yield a better result in order to distinguish different failure mechanism any of which could be the main aging mechanism for the specific application.

CHAPTER 4

FAILURE ANALYSIS

In this chapter, first a complete degradation monitoring and failure analysis procedure is provided. Then, the details of the performed failure analysis (FA) on DUTs which potentially have packaging related degradation is provided in order to evaluate the root cause of the degradation.

4.1 Complete Failure Analysis Methodology

Incipient fault detection and degradation monitoring of wide band-gap (WBG) semiconductor devices requires a number of high-end instrumentation and consists of several steps. If the devices under test (DUTs) are off-the-shelf packaged devices, pre-stress tests needs to be carried out to define brand-new conditions of the DUT to be able to monitor the variations with aging. Therefore, static and dynamic electrical parameters as well as the packaging integrity of the DUT should be tested to detect the condition of the device as brand new. The static electrical parameters like I-V characteristics and parasitic capacitances can be extracted very precisely using the power device analyzer (Keysight B1506A). The switching related dynamic parameters like turn-on time, turn-off time and switching losses can be obtained with double pulse tester and high bandwidth oscilloscope. In addition these static and dynamic electrical parameters can be tested at different junction temperatures utilizing forced air environmental chamber. Finally, the packaging integrity of the device can be screened with non-destructive scanning acoustic microscope (SAM) to be able to examine any manufacturing related voids and delamination in the package.

After initial test, DUTs are aged with a custom-designed accelerated power cycling testbed. Some of the essential aging precursors are saved continuously through data acquisition system, such as on-state resistance. During aging tests, junction temperature can be monitored by temperature sensitive electrical parameters which should be calibrated periodically

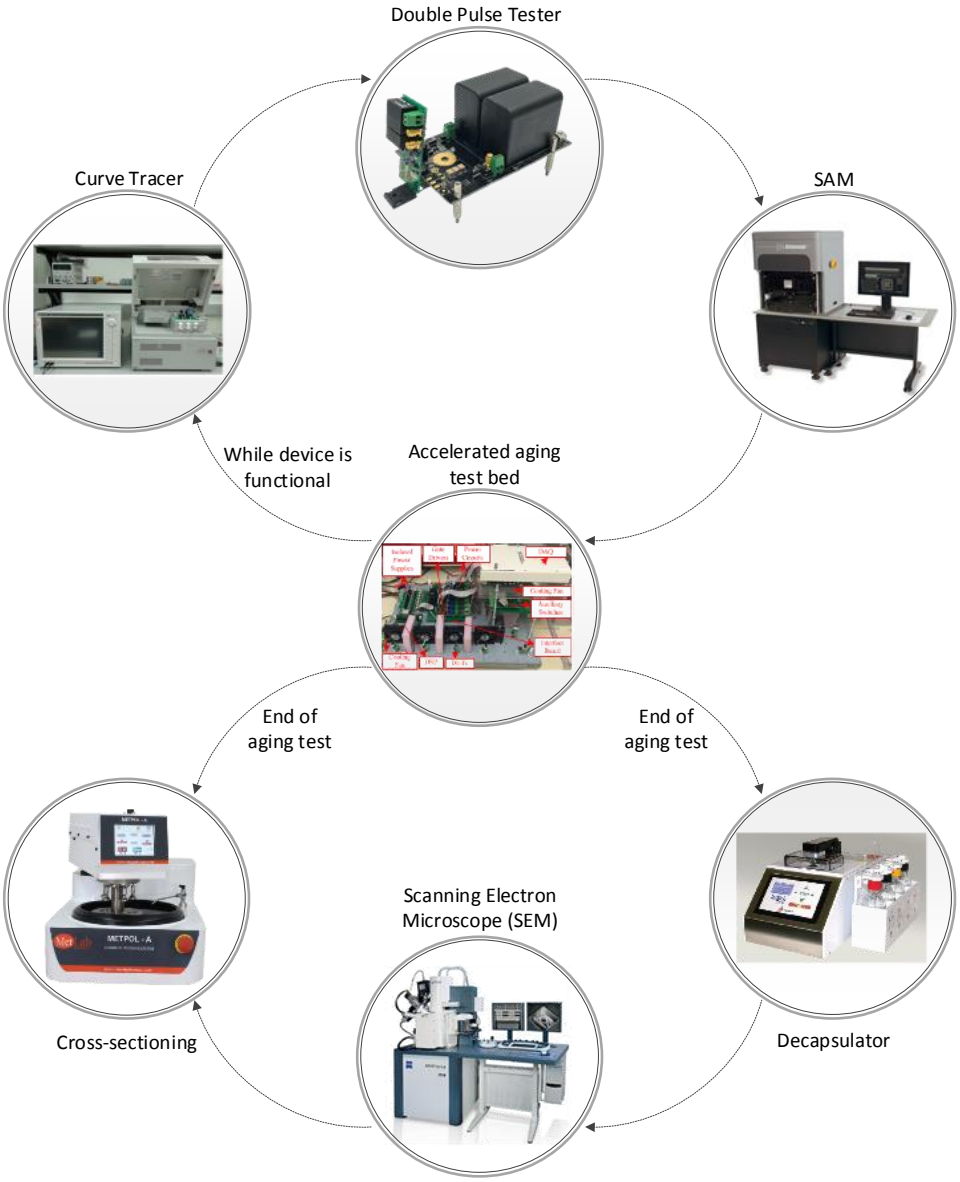


Figure 4.1. Degradation monitoring procedure.

using forced air oven or thermal plate. For power modules, junction temperature can be directly monitored with science grade high-resolution longwave infrared (LWIR) camera. The test cycles should periodically paused to monitor the variations in static and dynamic electrical parameters as well as the packaging integrity of the DUT. The outputs of this step are very useful to identify the aging patterns on electrical characteristics.

At the end of aging test, destructive failure analyses, like decapsulation or cross-sectioning are executed in order to find root cause of degradation. In order to expose the die to analyze the damage on the upper metallization layer, gate oxide degradation and cracks on or close to the end termination rings, the mold compound encapsulation should be removed with a combined utilization of laser ablation and automated decapsulation system. As another option, cross-section of the switches is analyzed for possible bond-wire cracks and/or lift-offs with a polisher/grinder. Both failure analyses require high resolution images obtained from the Scanning Electron Microscope (SEM). The complete degradation monitoring and failure analysis procedure is shown in Fig. 4.1.

4.1.1 Accelerated Aging Setup

The aging setup which is shown in Fig. 4.2 applies thermal cycles to multiple discrete power FETs simultaneously. Throughout aging test, the junction temperature of devices is estimated independently with thermocouples attached to the metal tab of each switch. Variables, such as drain-source voltage, drain current and case temperature are saved continuously. These measurements are used to control thermal cycles and calculate on-state resistances of each switch, which is one of the essential failure precursor for die attach solder degradation, deformation on the metals and contacts.

When the switch is turned on, it is actively heated up to the defined maximum limit with the adjusted constant current. When the switch is turned off, no current passes through the device and it is cooled with fans till they reach to the minimum temperature limit. The estimated junction temperatures are compared with the defined maximum and minimum temperature references, and a hysteresis band is developed in software for every switch. After each cycle, the drain to source voltage, case temperature and drain current data of each switch are stored by the data acquisition system for online on-state resistance ($R_{ds,on}$) measurement.

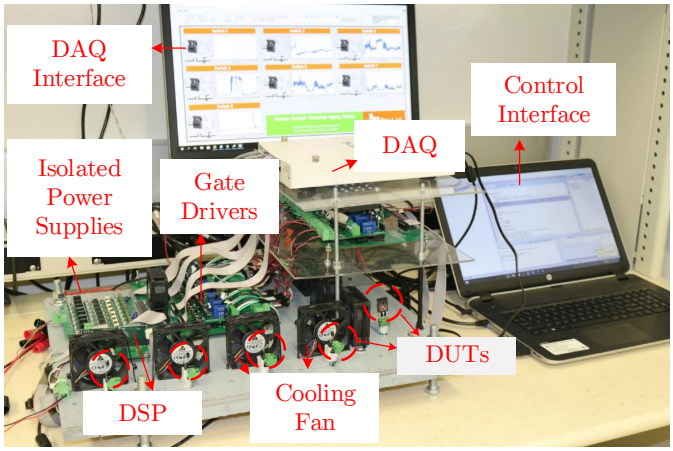


Figure 4.2. Accelerated aging test setup.

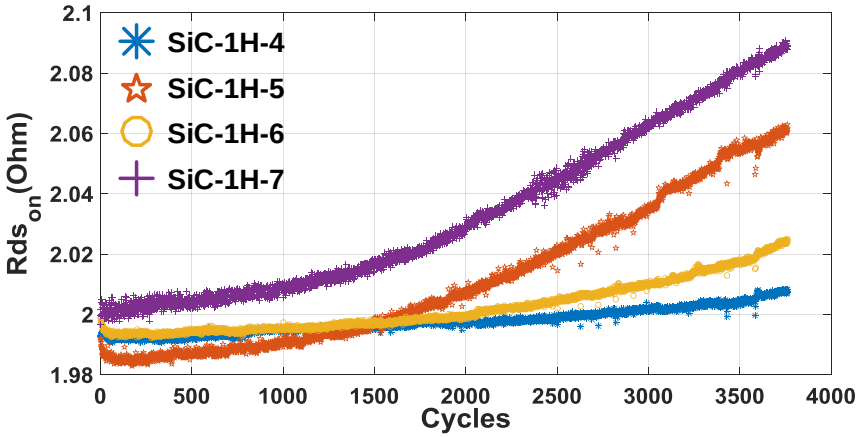


Figure 4.3. Continuous $R_{ds,on}$ monitoring.

Fig. 4.3 provides experimental $R_{ds,on}$ variations of SiC MOSFETs under low frequency, high temperature swing tests. The results suggest that $R_{ds,on}$ continuously increases throughout aging. The root-cause of this increment may involve more than one aging mechanism including die attach solder degradation, electro-migration of metals, damage on upper source metallization, bond-wire degradation, gate-oxide degradation. To narrow down the possible root causes, other I-V characteristics such as gate threshold voltage, parasitic capacitances need to be analyzed. Furthermore, a number of failure analysis tools should be run on the failed devices.

4.1.2 Keysight B1506A Automated Curve Tracer

The test cycles are paused periodically to extract static electrical parameters for parameter evaluations and comparisons at different aging cycles using Keysights B1506A automated curve tracer, shown in Fig. 4.4. The following parameters are analyzed with the help of the curve tracer; gate threshold voltage, transfer characteristics, output characteristics, on-state resistance, breakdown voltage, gate leakage current, output leakage current, body diode forward voltage, gate charge, gate resistance, parasitic capacitances. Monitoring these variations through curve tracer not only suggests root-cause of the failures but also helps identifying aging precursors that can be used to monitor the aging in power devices.

Figure 4.4. Keysight B1506A automated curve tracer.

4.1.3 Forced Air Environmental Chamber

Thermal performance of the DUTs is of particular importance, since the reliability is required under all working conditions. In addition to understanding general device characteristics over temperature, it may also be necessary to screen devices across temperature since devices that look fine at room temperature can sometimes be out of spec at low or high temperature. Power device evaluation over temperature range requires not only test equipment but also

a thermostatic chamber. In order to obtain temperature uniformity and precise calibration forced air environmental chamber is used for static electrical parameter measurement, as shown in Fig. 4.5(a). However since the oven necessitates the use of long connection cables between test equipment and the chamber it is not used for dynamic parameter measurement.

Figure 4.5. (a) TestEquity model FH5 forced air oven (b) inTest thermal platform.

4.1.4 Thermal Platform (Hot Plate)

In order to decrease the cable length which adversely affect dynamic measurements a temperature controlled hot plate test fixture is used , as shown in Fig. 4.5(b). The platform permits automated control of plate temperature, from enclosure ambient to 250°C, for characterization of power devices. The plate system comprises the thermal platform and controller, which can also interface with the Keysight Analyzer via a connection harness incorporated in the analyzer. The plate can be placed in the analyzers test fixture, minimizing cable length and risk of oscillation. To efficiently transfer heat from the thermal plate to the DUT requires the use of a contact sheet or thermal grease. Although this method is quick and simple the temperature around the device is not necessarily uniform. Part of the hot plate is exposed to the air which results in temperature loss via heat radiation and convection. Additionally, heat transfer through device test leads is another source of temperature non-uniformity.

4.1.5 High-Resolution Infrared Camera

For power modules, junction temperature can be directly monitored with science grade high-resolution longwave infrared (LWIR) camera. Fig. 4.6 shows the decapsulated power module which involves six FETs in three half-bridge structures. Here, the decapsulation is necessary to better observe the thermal differences of each die in order to develop lifetime extension strategies to provide thermal relief on the degraded switch. For instance, in one of the proposed techniques, the modulation scheme of the inverter is changed from SVPWM to DPWMmax to lower the thermal stress on the degraded bottom three switches. The thermal distribution information is significant in quantifying the achieved lifetime extension for the degraded switches. Without high-resolution infrared camera, it is not possible to observe the thermal distribution and response of the package.

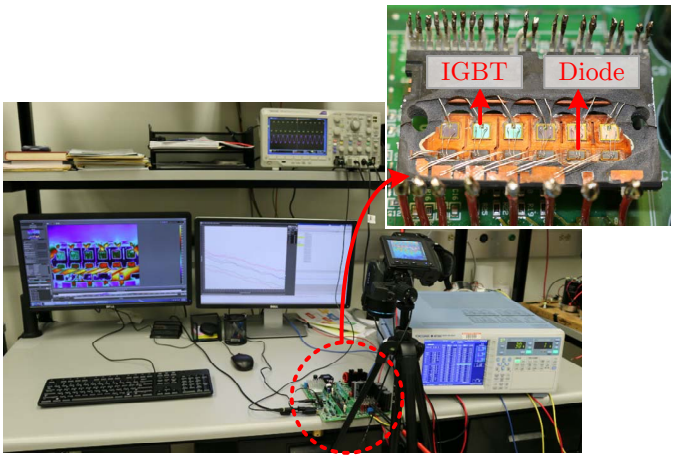


Figure 4.6. Decapsulated switch with the high resolution thermal camera.

4.1.6 Scanning Acoustic Microscope (SAM)

Scanning acoustic microscopy (SAM) utilizes ultrasound to non-destructively examine internal structures, interfaces and surfaces of a device. Sonoscan D9600 CSAM system shown in Fig. 4.7(a) while a schematic diagram of SAM is shown Fig. 4.7(b). Practically, an acoustic

microscope is based on a source of pulsed ultrasonic waves of fixed frequency, produced by a piezoelectric crystal transducer equipped with an acoustic lens to focus the waves in a spot. The transducer inside is the most important part of the microscope. The transducer creates a pulse of ultrasound and sends as a focused beam of ultrasound by narrowing it to the spot size on a small point on the sample. High frequency sound waves cannot propagate through air. Because of that the transducer and sample are immersed in a fluid coupling medium to carry the high frequency sound waves through the sample. De-ionized water is typically used since it is a safe, non-hostile environment for most packages [38].

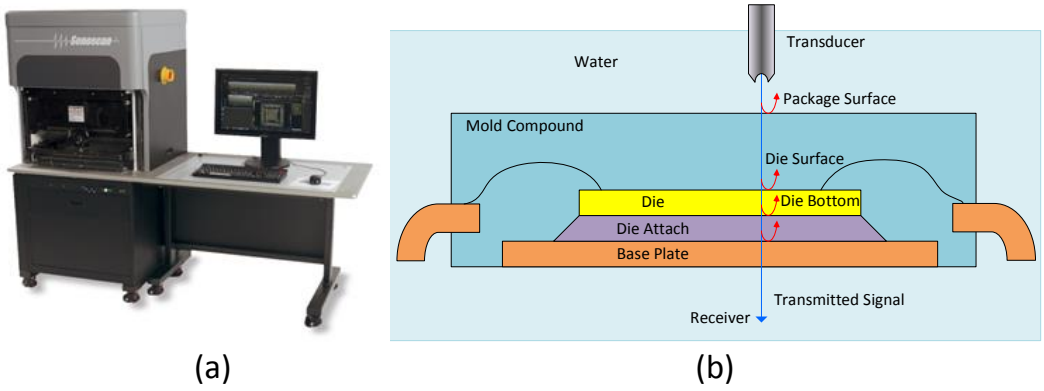


Figure 4.7. (a) Sonoscan D9600 SAM (b) Schematic diagram of SAM.

Commercial SAM is capable of imaging in four modes: A-scan, B-scan, C-scan and T-scan. The A-scan displays the reflected or transmitted signals from the interfaces within the chip. The C-scan, B-scan and T-scan utilize these signals from the A-scan to form images. In A-scan acquisition, the transducer remains stationary at a single point above the sample and is focused to a specific depth within the sample. In B-scan acquisition, the transducer mechanically raster scans in the x direction and increments in the z direction. The B-scan is particularly useful in observing crack propagation in the mold compound of a pop-corn effect and also the location of mold voids in the package. In C-scan acquisition, the transducer mechanically raster scans in the x-direction and increments in the y-direction. Thus, C-scan will generate a x-y planar image at a specific depth within the package. Using

transmitted ultrasonic signals like x-ray inspection, T-scan is a simple ultrasonic inspection method that measures transmitted sounds loss. It is particularly useful in the configuration of delamination and pop-corn crack [38]. Some example SAM images are shown in Fig. 4.8(a) which reveals the extent and location of defects through aging. The pictures as brand new devices, at the middle and at the end of the cycling tests are indicated as pre-stress, mid-stress and post-stress, respectively.

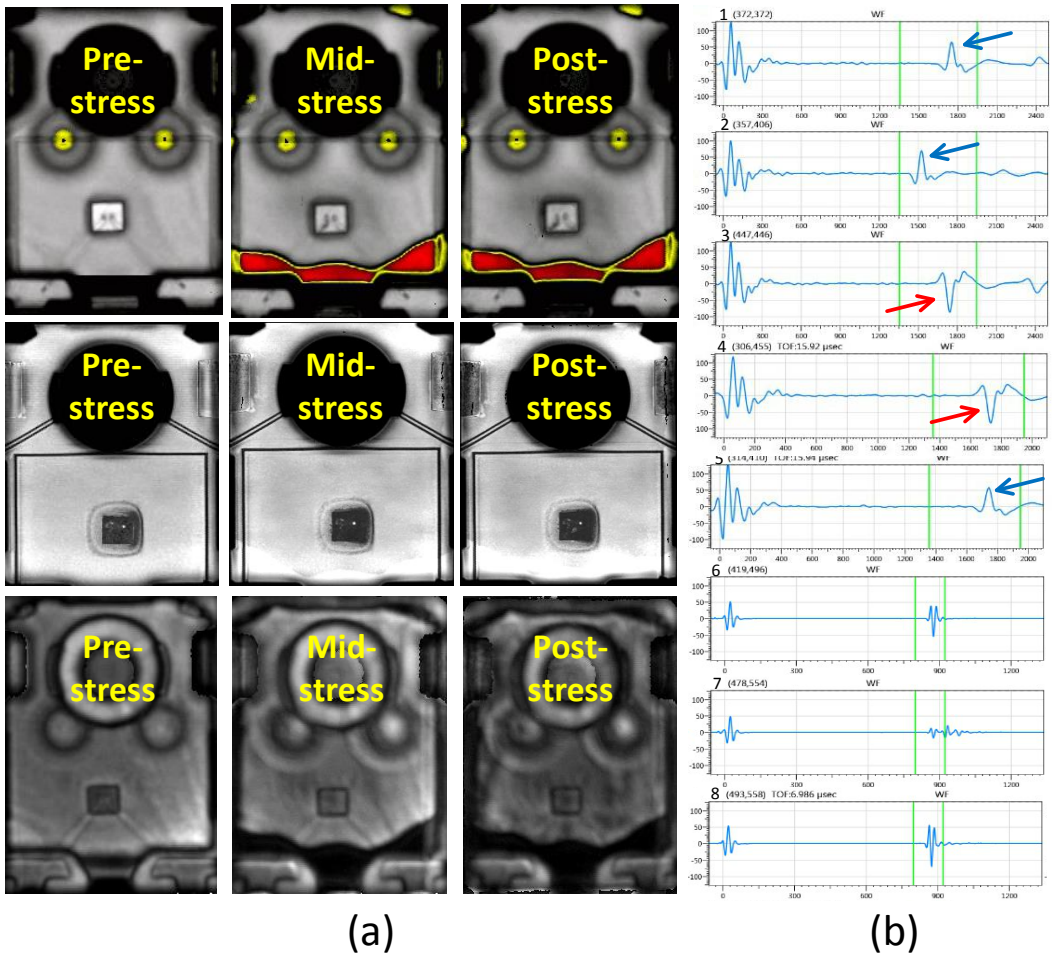


Figure 4.8. (a) SAM images through power cycling: C-SAM form topside, C-SAM from back side, and T-SAM (b) Example waveforms corresponding to the blue arrows.

The images were generated by focusing the ultrasound through the top (encapsulated) and back (heat sink) sides of the components. The topside images display the encapsulant

to die surface, heat sink and lead frame interfaces. The leads are at a different height within the parts than the die/heat sink level, so the images were generated in two scans at two different focus levels, but are displayed in a single image. The color scale displays areas of good adhesion in gray/white and delaminations appears as red/yellow. The backside images were focused through the heat sink to the die attach level. In these pictures, dark gray indicates good adhesion and light gray/white indicates voiding. The T-SAM images display the condition of the entire thickness of the parts. It was generated with the top (encapsulant) side up. Light gray indicates good material continuity while black areas indicate a separation at some level within the device. Example waveforms were captured for a few locations and given in Fig. 4.8(b) with the corresponding number of each location. The green bars in the waveforms indicate the gate corresponding to the level of focus. Negative reflections in the graphs indicate delamination on the heat sink while the positive reflections indicate a good adhesion.

4.1.7 Decapsulation System

For optical analysis of die surface, it is necessary to expose the die surface by decapsulation. Decapsulation is the process of removing mold compound from the die surface of a plastic encapsulated device. Typically, the mold compound is removed only in the area above the die and bond wires. There are different approaches for exposing the die in various package types. Decapsulation process can be used in a number of ways, but is most commonly seen in semiconductor failure analysis and counterfeit protection during the verification process. Die exposure is critical to the failure analysis industry, as a die in this state lends itself best to a wide number of types of tests.

Hot fuming sulfuric and nitric acids are the most commonly used decapsulating agents. Jet etch systems employing these acids or mixtures of these acids have become the dominant method for decapsulation. Jet etchers provide a safer alternative to the older techniques as

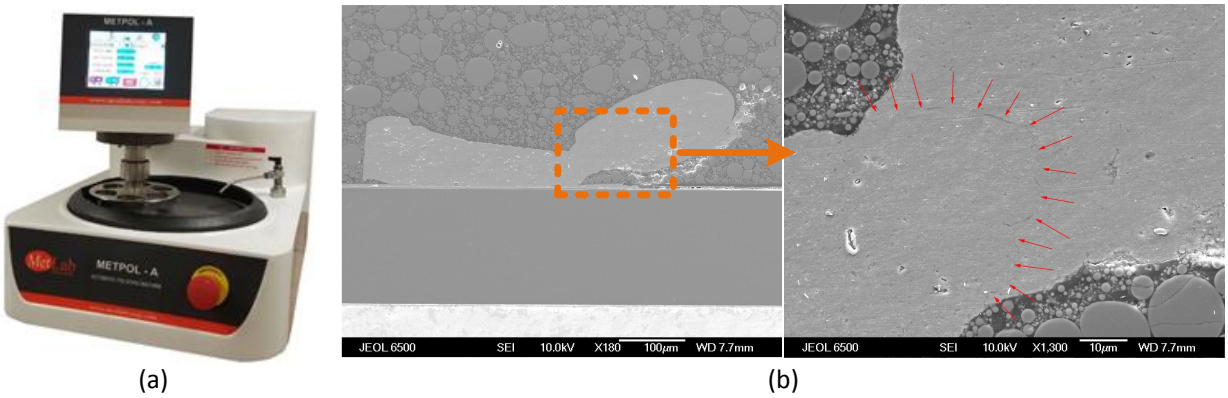
well as a more consistent delivery of the hot decapsulation agent. A low-level vacuum is used to create the jet and hold the inverted device in place. The hole in the fluorocarbon vacuum seal for the device provides a masking effect to control the size of the decapsulation hole. The consistent delivery of hot acid is essential for reducing the decapsulation time. In addition to impacting productivity, long exposure of the mold compound to the acid can result in absorption of the acid. This can lead to swelling of the mold compound and mechanical damage to the bond wires [39].

Figure 4.9. Nisene JetEtch Pro decapsulator.

4.1.8 Polisher/Grinder (Cross Sectioning)

Cross-sectioning is another destructive failure analysis tool which is important particularly in analyzing the bond-wire failures. It is also used to observe the delamination between layers. Bond-wire failures are one of the most observed failure mechanism particularly in power module structures that include direct-bonded-copper (DBC) layer. DBC introduces a large thermal capacity to the layers underneath the active die region; thus, making bond-wire and bond pad interface a primitive location for failure. The source bond-wire cross-section image of a failed device is given in Fig. 4.10. The cross-section of the bond-wire shows that

a crack has been initiated on the tail. At higher frequency thermal swings, more bond-wire lift-offs are observed.



(a) (b)

Figure 4.10. (a) Automated polishing/grinder machine (b) Cross-section of the bond-wire of an aged FET.

4.2 Non-destructive Failure Analysis

After the aging cycle is finished, a failure analysis is performed to evaluate the packaging-related degradations. Two devices, one assumed to have packaging-related degradation (2C-2) and the other one assumed to have no packaging-related degradation (2C-3) are chosen for failure analysis. To have a better understanding the root cause of the degradation, a detailed failure analysis (*FA*) has been carried out. The devices are first inspected with non-destructive analysis methods using the C-Mode Scanning Acoustic Microscopy (*C-SAM*) and the THRU-Scan Acoustic Microscopy (*T-SAM*) in order to detect internal defects. The C-SAM images of both devices are presented in Fig. 4.11. The images were generated by focusing the ultrasound through the top (encapsulated) and back (head sink) sides of the components. A combined image of the mold compound to heat sink and mold compound to leads interface form topside for switches 2C-2 and 2C-3 are shown in Fig. 4.11 (a) and (b), respectively. The leads are at a different height within the parts than the die/heat sink level,

so the images were generated in two scans at two different focus levels, but are displayed in a single image. The color scale marks the areas with good adhesion in gray/white and the delaminations in red/yellow. As it can be seen from the figures, both devices show some anomalies around die surface Additionally, Fig. 4.11 (b) reveal an evident delamination at the mold compound to heat sink interface for device 2C-3 as indicated by the red spots. The backside images for switches 2C-2 and 2C-3 are given in Fig. 4.11 (c) and (d) respectively, where the focus is adjusted to the heat sink to the die attach level. In these pictures, dark gray indicates good adhesion and light gray/white indicates voiding. Backside images show that die attachments of both devices are well bonded.

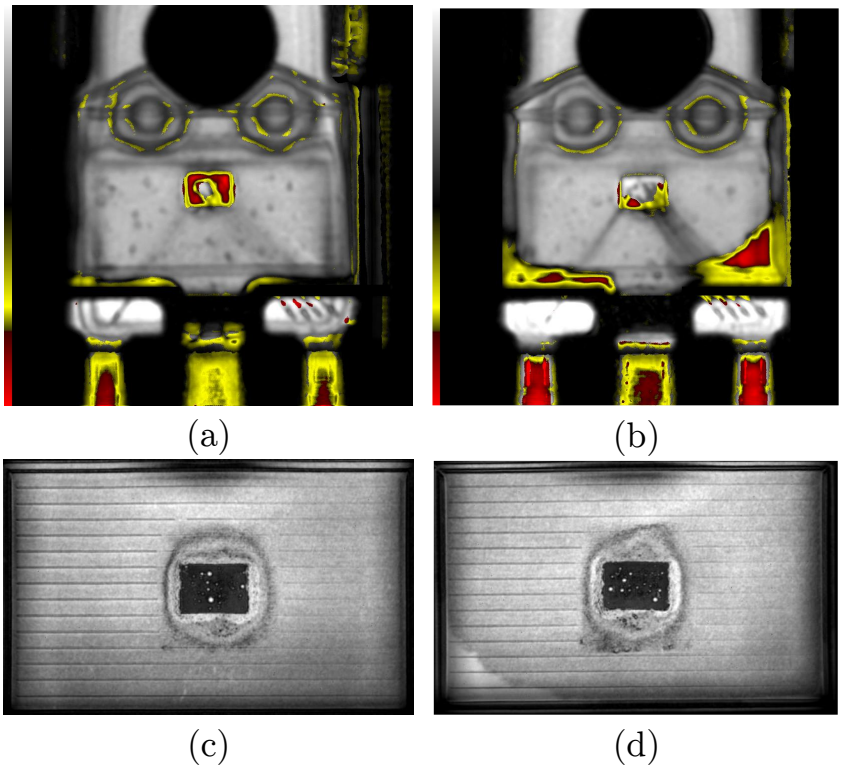
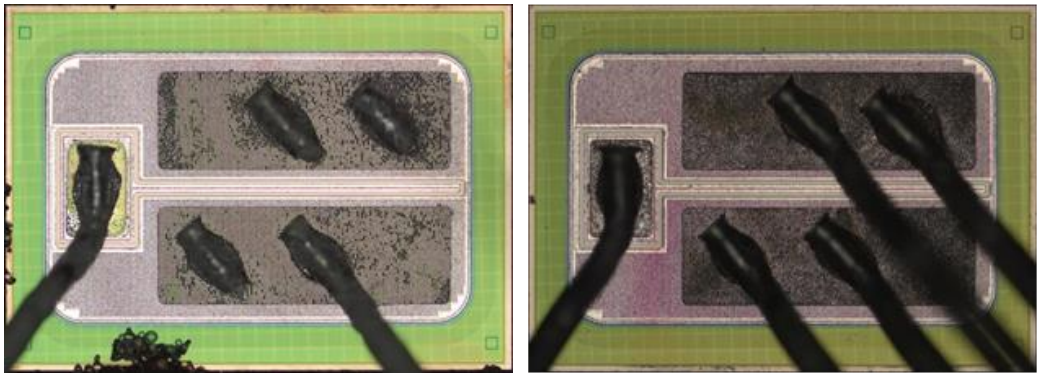


Figure 4.11. C-SAM images of the switches after power cycling. (a) Topside C-SAM image of 2C-2 (b) Topside C-SAM image of 2C-3 (c) Backside C-SAM image of 2C-2 (d) Backside C-SAM image of 2C-3.

4.3 Destructive Failure Analysis

Following the non-destructive analysis, the devices are inspected through the destructive analysis to find other physical failure mechanisms. Both devices were decapsulated for optical inspection using a combination of laser ablation and sulfuric acid at 120C. The optical inspection is carried out after the decapsulation of the mold compound as shown in Fig. 4.12. The inspection reveals that three bond wires are detached for device 2C-2 while all four bond wires are well attached for 2C-3. Since the same decapsulation process is applied for both devices, the appearance of the crack in device 2C-2 indicates that the crack is not caused by decapsulation process but due to the thermal-mechanical stress during the aging process. This finding helps to explain that the sudden increases in on-state resistance and reverse body diode voltage drop are caused by the wedge bond heel cracks.



(a) (b)

Figure 4.12. Optical images of die surfaces after decapsulation for the samples (a) 2C-2 (b) 2C-3.

For further analysis, DUT-2 is chosen for decapsulation while DUT-5 is selected for cross sectioning analysis. DUT-2 is decapsulated for die surface inspection using a combination of laser ablation and sulfuric acid at 120°C. During decapsulation of the mold compound, it is observed that three bond wires were detached in DUT-2 which is a sign of bond wire heel cracking. After decapsulation, scanning electron microscope (SEM) inspection was

carried out which is presented in Fig. 4.13. As shown at the full die image, three wedge bonds were detached from the wire terminations. Higher magnification SAM images of the attached bond wire are also shown from two different angles. These images present a thin heel cracking at the same location where the crack fully developed in other wires. A brand-new control unit that had not undergone any stress testing is also decapsulated to inspect the wire bonds and no crack was observed. This indicates that the heel cracking is a result of the thermo-mechanical stress that occurred due to temperature cycles and it is not caused by decapsulation process.

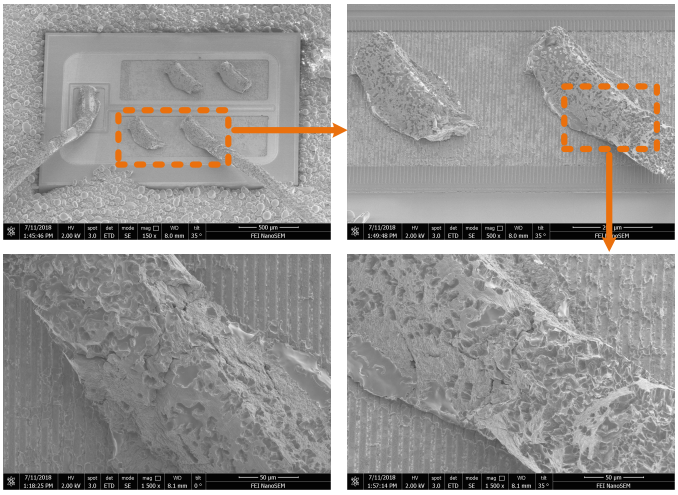


Figure 4.13. SEM inspection of DUT-2 as full die image and higher magnification images of the attached bond wire from two different angles.

The cross section analysis of DUT-5 is shown in Fig. 4.14 where bond wire attachment has been analyzed. Analysis reveals that a small crack forms at the heel of the bond wire. Another brand-new control unit is also cross-sectioned with the same process for comparison. When compared with the control unit, it is evident that thermo-mechanical stress triggered deformation around the wire termination also in DUT-5. Consistency of damage location indicates that the heel of the bond wire might be weakened due to the bonding process. Consequently, FA findings proves that the sudden increases in $R_{ds,on}$ and V_{SD} are indeed due to packaging related degradation which is caused by the wedge bond heel cracking.

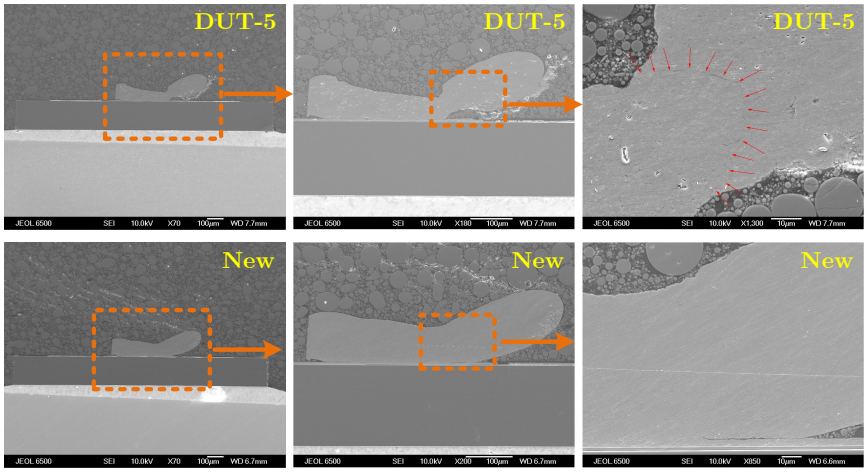


Figure 4.14. SEM inspection of cross-sectioned bond wire images of DUT-5 and a brand-new control unit.

CHAPTER 5

AN IMPROVED CONDITION MONITORING METHOD FOR SIC POWER MOSFETS

Reliability of SiC device is one of the main barriers preventing their high penetration into the market. Since it is a relatively new technology, limited information is available regarding the long-term field application of SiC MOSFETs which raise significant reliability concerns. Therefore, it is essential to properly monitor the device state-of-health (SOH) to reduce reliability concerns and minimize catastrophic failures in real time applications.

The hardware redundancy can be utilized as an easier solution to increase the system reliability. However, taking SiC costs into consideration, monitoring the SOH and reporting impending faults at very early stage can be a more cost effective solution. The condition monitoring (CM) approach aims to track variations in the electrical parameters which are indication of device degradation or incipient faults [40]. Since monitoring all of the electrical parameter is not feasible in an end-product, specific parameters should be identified depending on the dominant aging mechanism. Then, the SOH of the switch can be estimated by tracking the pre-defined parameters and corresponding prognostic algorithms [41].

In recent years, various studies have focused on aging precursors identification for Si devices [32]. Among them a gradual variation in the ON-state resistance ($R_{ds,on}$) of MOSFETs [33] and in saturation voltage of IGBTs [34] are the most commonly used parameters as an aging indicator. Unlike Si devices, there are substantially less studies focusing on the failure precursors in SiC MOSFETs. The major reliability concerns for SiC MOSFETs are the gate oxide degradation and the bias-temperature-instability (BTI) [26, 23]. Therefore, most SiC MOSFET reliability studies focus on failure precursor identification for gate oxide related issues. The threshold voltage (V_{th}) is the most commonly utilized precursor to monitor gate oxide charge trapping [42, 43, 44]. The gate leakage current is found to increase suddenly before gate oxide breakdown and proposed as a signature in order to detect the gate oxide

degradation [25]. Recently, the gate plateau (or miller) voltage [45], the gate plateau time [46] and turn-on time [47] are also proposed as precursor of gate oxide degradation. Although $R_{ds,on}$ is well-known as a precursor for packaging related degradation, the gate oxide charge trapping is also found to be varying $R_{ds,on}$ due to its dependence on V_{th} [26]. Other major reliability concern for SiC MOSFETs are packaging related issues such as bond wire crack, bond wire lift-off, and die attach solder degradation. Although some new packaging technologies are introduced especially for power modules to enhance the reliability [48], still, conventional packaging and wire bonding techniques are utilized for the majority of commercial SiC devices. The packaging degradation of SiC MOSFETs are evaluated by means of an accelerated high temperature power cycling test and an increasing trend in ON-state resistance was observed during the aging process [35]. The body diode voltage drop (V_{SD}) and thermal impedance are also identified as precursors for packaging related degradation [32].

Although different aging precursors are identified for gate oxide and packaging related degradation, each failure precursor (except $R_{ds,on}$) indicates only one degradation mechanism. On the other hand, the dominant degradation mechanism in a real application depends on the packaging technology and the application conditions. Moreover, each degradation mechanism can be the cause or result of the other one. Therefore, in case of utilizing one of these failure precursors, a complete CM system cannot be achieved. Even though the variation of the $R_{ds,on}$ unveils both gate oxide related and packaging related degradation mechanism, it is not straightforward to distinguish whether the variation is because of the package or gate interface degradation.

In this chapter, a complete CM method is proposed for SiC MOSFETs by monitoring only the reverse body diode voltage drop at different gate bias levels. Using this method, both gate oxide degradation and the packaging related degradation can be monitored independently with a single precursor. In order to validate the proposed method, a gate driver circuit board with complete CM feature is designed and experimentally tested.

The rest of this chapter is organized as follows: In Section 5.1, the variations of common precursor parameters is provided under accelerated aging. Considering both gate oxide degradation and package related degradation, a complete analysis is provided to investigate the correlation between precursor parameters and degradation mechanisms. Based on unique two different conduction modes in third quadrant mode, an improved condition monitoring method is proposed for SiC MOSFETs in Section 5.2. Implementation of the proposed method on a phase leg configuration is given with experimental results in Section 5.3. Lastly, the conclusions are summarized in Section 5.4.

5.1 Failure Precursors

In order to investigate the variation of electrical parameters during the aging/degradation of SiC MOSFETs, accelerated aging test can be used [35]. In this study, a high temperature power cycling is utilized in order to trigger both package related and gate oxide related degradation mechanisms. This enables to track variations in electrical parameters throughout the aging for both degradation mechanisms which allows to build a complete CM system.

Seven discrete SiC MOSFETs are aged with a junction temperature swing from 30°C to 200°C for 10000 cycles. The operating principle of the power cycling test utilized in this study is given in Fig. 5.1 [49]. After each 250 aging cyclings, a systematic static parameter evaluation of each device is performed at room temperature with the aid of the Keysight B1506A curve tracer. In the following sections, variations the static parameters which can be utilized as a precursor are presented for all devices under test (DUT).

5.1.1 Variation of Threshold Voltage (V_{th})

Since V_{th} is often presented as a precursor parameter for gate oxide degradation in the literature [13], the V_{th} variation over aging is presented for all DUTs in Fig. 5.2. The quantitate V_{th} data shows an increase of the threshold voltage by 7.1% to 10.7% at the end

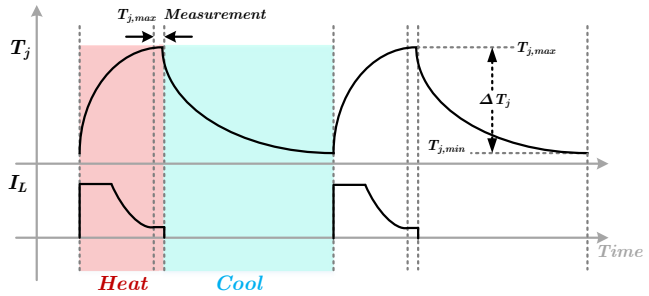


Figure 5.1. Operation principle of the power cycling test setup.

of the aging test. The reason for this gradual increase in threshold voltage is suspected to be caused by the interfacial trapped charge (Q_{it}). Theoretically, the V_{th} of the SiC MOSFET can be calculated by [37]

$$V_{th} = V_{th0} - \frac{Q_{ot}}{C_{ox}} + \frac{qN_{it}}{C_{ox}} \tag{5.1}$$

where Q_{ot} is oxide trapped charge, q is the fundamental electronic charge. N_{it} is interface trap density, and C_{ox} is oxide capacitance. As can be seen from (5.1), the existence of near interface trapped charge can increase the threshold voltage. Therefore, V_{th} can be utilized as an aging precursor for gate oxide degradation.

5.1.2 Variation of ON-state resistance ($R_{ds,on}$)

Another parameter that is often presented as an aging precursor for both Si and SiC MOSFETs is the $R_{ds,on}$. The $R_{ds,on}$ over the aging cycles for the DUTs is presented in Fig. 5.3. A gradual increase is observed for all the devices for the first 7000 cycles. This gradual increase shows a very similar trend to V_{th} variation and assumed to be related to the gate oxide degradation. Because of the low inversion carrier mobility of SiC MOSFETs the channel resistance (R_{ch}) represents a significant portion to the $R_{ds,on}$ and it can be calculated as [26]

$$R_{ch} = \frac{L_{ch}}{W_{ch}.\mu_n.C_{ox}\left(V_{gs} - V_{th}\right)} \tag{5.2}$$

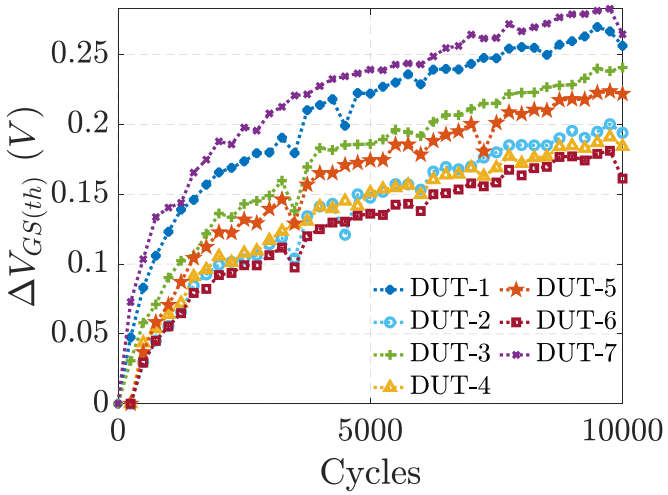


Figure 5.2. Threshold voltage shift over power cycles ($@Id = 250\mu A$) (a) Absolute value (b) Variation from the initial value.

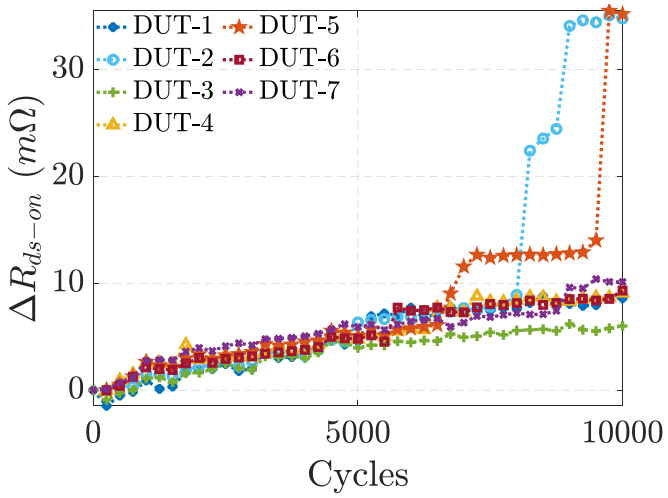


Figure 5.3. ON-state resistance shift over power cycles ($@Id = 4.5A, Vgs = 20V$) (a) Absolute value (b) Variation from the initial value.

where L_{ch} is the channel length, W_{ch} is the channel width, μ_n is the electron mobility of the inversion layer channel in SiC material, and V_{gs} is the gate drive voltage. As it can be seen from (5.1), increasing V_{th} and decreasing mobility with the interfacial charge trapping will both increase the R_{ch}. However, in addition to R_{ch}, the package related degradation will also affect the $R_{ds,on}$. As can be seen from Fig. 5.3, a sudden increase of ON-state resistance is

observed for DUT-2 and DUT-5. Most commonly, the bond wire crack or bond wire lift-off contributes to this type of sudden $R_{ds,on}$ increase.

5.1.3 Variation of Body Diode Voltage (V_{SD})

Another precursor parameter which is commonly used in the literature is the V_{SD}. The variation of the V_{SD} at -3A drain current and -5V gate bias through aging is given in Fig. 5.4. As it can be seen from the figure, the variation in the V_{SD} is almost negligible over power cycles for most of the devices. However, devices DUT-2 and DUT-5 shows jumps in V_{SD} values after 7000 and 8000 cycles which is consistent with the sudden increases of the $R_{ds,on}$. The results of the V_{SD} variation support our hypothesis that the sudden increase in the $R_{ds,on}$ is related to the degradation in packaging. To be specific, at a negative voltage of -5V, the current conduction is only through the PiN diode and does not include the channel, and therefore the threshold voltage drift would not affect the body diode's voltage drop.

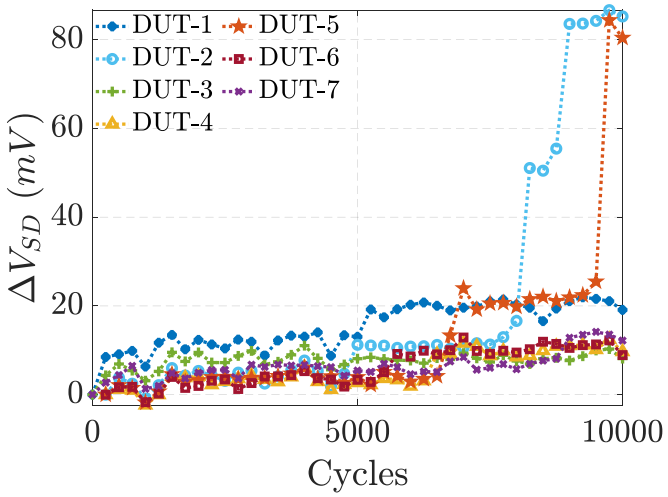


Figure 5.4. Reverse body diode voltage drop variation over power cycles ($@Id = -3A, Vgs = -5V$) (a) Absolute value (b) Variation from the initial value.

However, there is a secondary conduction mode in third quadrant operation, which is unique to SiC MOSFETs. When the gate bias is between 0V to -4V, the current flows

through the MOS channel instead of the PiN diode [50, 51]. Both PiN path and MOSFET paths for SiC MOSFETs in third quadrant operation is presented in Fig. 5.5. In order to clarify existence of two conduction path in SiC devices and scale the influence of the gate voltage on the conduction path, a new I-V characteristic curve is proposed.

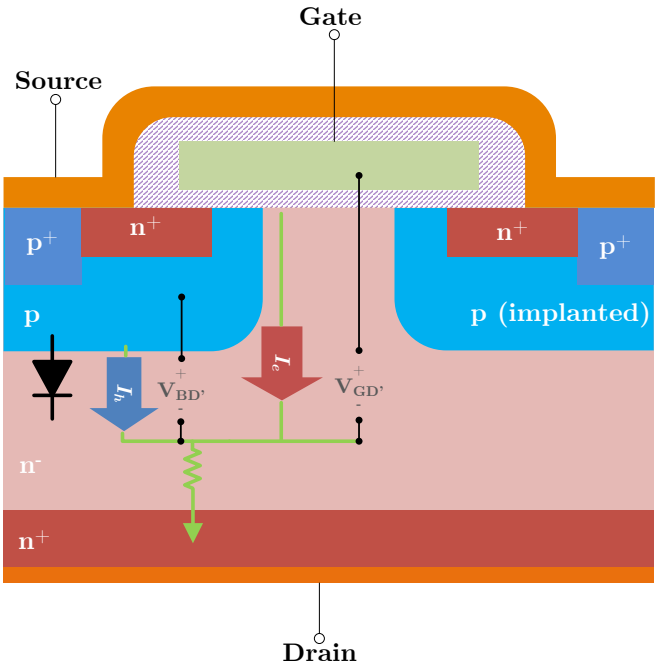


Figure 5.5. The current flow paths for SiC MOSFETs in the third quadrant.

For this characterization, constant current pulses is conducted through the device in the reverse direction and the gate to source voltage is swept from negative maximum bias to positive maximum bias. Since it shows resemblance to the MOSFET transfer characteristic, the proposed I-V characteristic curve is named as "body diode transfer characteristic".

The circuit setup to obtain the body diode transfer characteristic is shown in Fig. 5.6(a). The body diode transfer characteristics of different Si and SiC MOSFETs from different manufacturers are presented in Fig. 5.6(b). As can be seen form the figure SiC MOSFETs exhibits very different body diode transfer characteristic compared to Si devices. The body diode transfer characteristic can be divided into three parts as diode conduction, transition

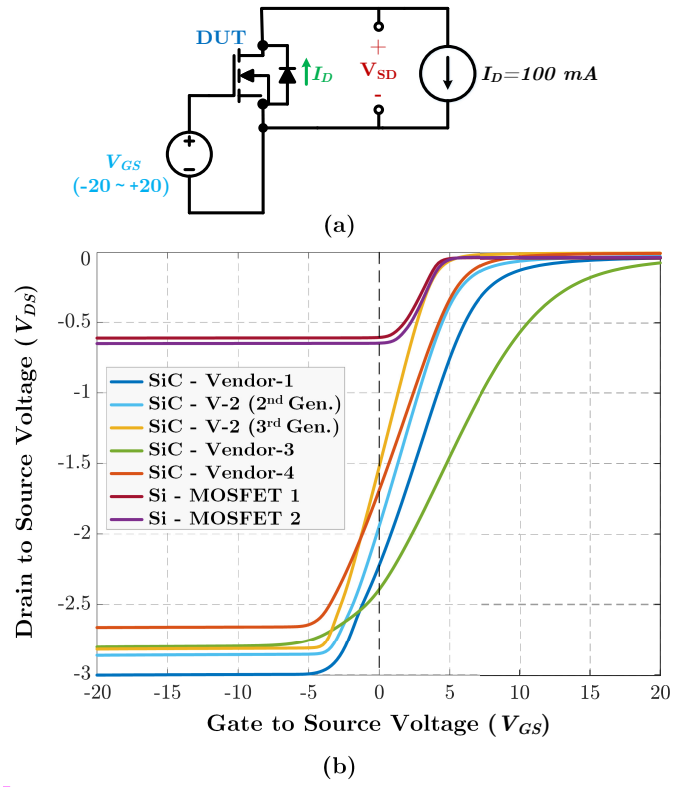


Figure 5.6. (a) Body diode transfer characterization circuit (b) Body diode transfer characteristics of different Si and SiC MOSFETs.

and MOS channel conduction. Firstly, for all SiC devices, V_{SD} is latched at much higher PiN diode voltage drop during diode conduction compared to Si devices which is a result of their higher bandgap. Less anticipated difference however, is the larger transition range in SiC devices that starts at negative gate bias values. In Si MOSFETs, the V_{SD} value stays constant at P-N junction voltage drop around 0.6V for all lower gate bias values, until the gate bias reaches to the V_{th} and channel starts to conduct. On the other hand, in SiC MOSFETs, the V_{SD} value starts to decrease substantially when the gate bias is above a knee voltage, which is around -5V to -4V for most of the devices. With increasing gate bias, the V_{SD} value keeps decreasing, until the gate bias reaches to the positive V_{th} value and channel fully turns on. The variation in V_{SD} value -starting from negative bias values- is caused by formation of a conductive path through the MOS channel which is triggered by

the V_{th} reduction with the influence of body effect [50, 51]. During this transition period, SiC MOSFET is mostly conducting through the MOS channel.

5.2 Proposed Condition Monitoring Method

The unique conduction mode of SiC MOSFET through the MOS channel at negative gate bias values can be utilized to monitor the package related degradation and the gate interface degradation independently. When the device is conducting through the channel path, the value of V_{SD} will be dependent to condition of the MOS channel. As the gate interface degrades, the R_{ch} and therefore the V_{SD} will increase. On the other hand, when PiN diode path is conducting, the channel is not involved in the conduction path and therefore only contact resistance variations will change the V_{SD} value. For that reason, if V_{SD} values can be measured at two different gate voltages; one enables MOSFET path conduction and the other forces to conduct through the PiN path, a complete CM can be obtained by monitoring only one precursor parameter.

In order to verify the proposed CM method idea, the V_{SD} values are captured also at 0V gate bias throughout the aging in addition to already presented values at -5V gate bias. As it can be seen in Fig. 5.6(b), 0V gate bias enables the MOSFET path conduction, while at -5V gate bias current conducts through the PiN path. The variation of the V_{SD} at -5V gate bias through aging is already presented in Fig. 5.4. As it's indicated before, the current path of the PiN diode conduction does not involve the channel, and therefore the V_{SD} values stays constant over power cycles for most of the devices. Only devices DUT-2 and DUT-5 shows a jump after 7000 cycles which is assumed to be related to the package related degradation. The variation of the V_{SD} at 0V gate bias through aging is given in Fig. 5.7. As it can be seen from the figure, the V_{SD} at 0V gate bias shows perfect resemblance to the V_{th} drift depicted in Fig. 5.2(b).

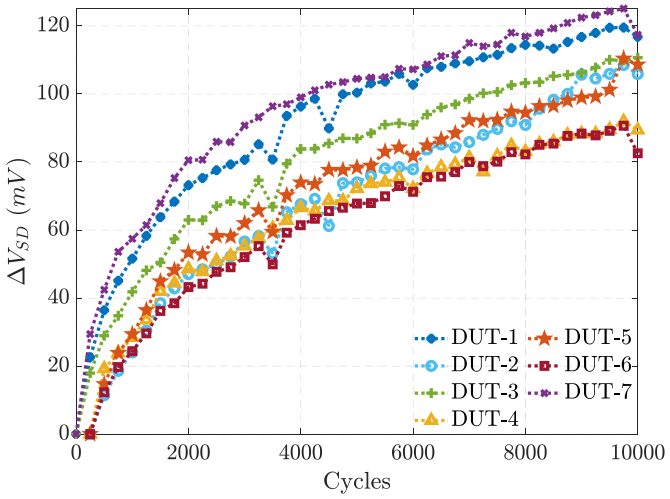


Figure 5.7. Reverse body diode voltage drop variation over power cycles ($@Id = -0.5A, Vgs = 0V$).

These results proves that with the proposed method, we can independently monitor the package related degradation and the gate interface degradation by tracking the V_{SD} at two different gate voltages. Here, it should be noted that for some SiC MOSFETs, the complete transition from the MOSFET path to the PiN path may not be obtained at -5V gate bias as it can be seen from Fig. 5.6(b). Therefore, the negative gate voltage value should be defined properly for the specific device to ensure the PiN path conduction.

In addition to the value of negative gate bias value, another important parameter is the drain current value at which the monitoring will be carried out. In order to test the influence of detection current value on the monitoring, the V_{SD} measurements at both 0V and -5V gate bias are obtained at different drain currents. The V_{SD} variation in DUT-2 throughout aging is depicted in Fig. 5.8(a) for different drain currents at -5V gate bias. As it can be seen from the figure, the sensitivity of the signal increases with the drain current. This is an anticipated result and indeed it is an additional evidence for our previous assumption that the sudden increase of $R_{ds,on}$ and V_{SD} at -5V gate bias is due to ohmic contact resistance increase. In Fig. 5.8(b) V_{SD} variation in DUT-2 throughout aging is given at 0V gate bias

for different drain currents. At 0V gate bias, the sensitivity of the signal to the gate oxide degradation slightly decreases with increasing drain current.

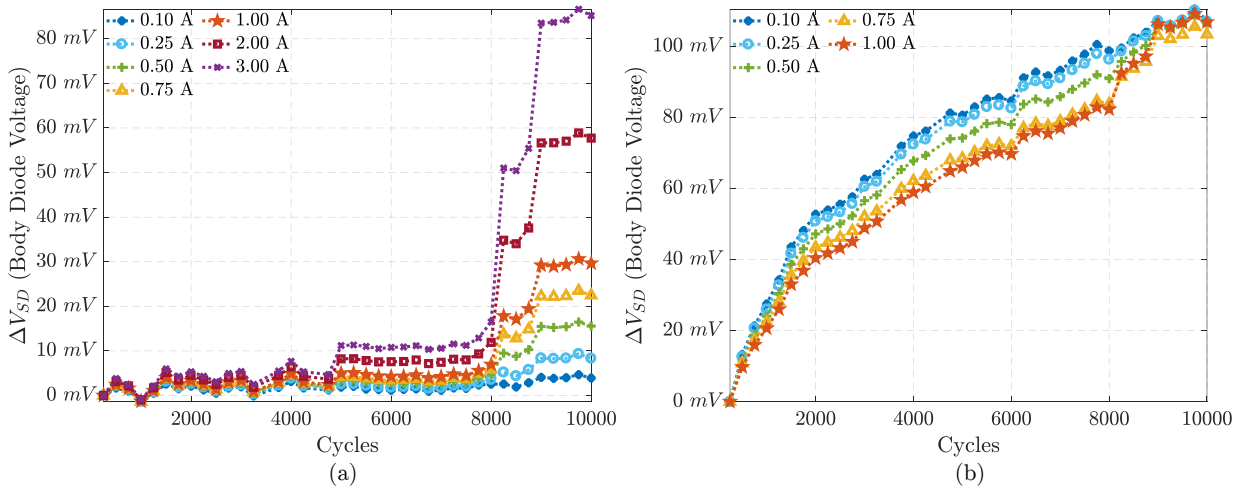


Figure 5.8. Reverse body diode voltage drop variation of device DUT-2 over power cycles at different current values (a) @$Vgs = -5V$ (b) @$Vgs = 0V$.

Moreover, in this figure an indication of the ohmic contact resistance increase is observed at drain current values higher than 0.5A. Therefore, it is suggested to use lower drain current values (<0.5A) to monitor the gate oxide degradation and higher drain current values (≥0.5A) for the packing related degradation. This will prevent a possible influence of the ohmic contact resistance increase on the gate oxide degradation monitoring and ensures monitoring of both degradation mechanism with high sensitivity.

One issue of the proposed condition monitoring method is the dependence of the V_{SD} on the drain current and the junction temperature. In Fig. 5.9, the variation of the V_{SD} at different drain currents and junction temperatures is presented. Therefore, the CM should be carried out at identical diode currents throughout the aging which requires current source as a part of detection circuit. For temperature dependency, measurements can be carried out at the same temperature or otherwise calibration can be conducted to compensate the measurements according to the junction temperature. In addition, for the converter config-

urations where the diode conduction would require interruption of the converter operation, this method can only provide in-situ monitoring capability.

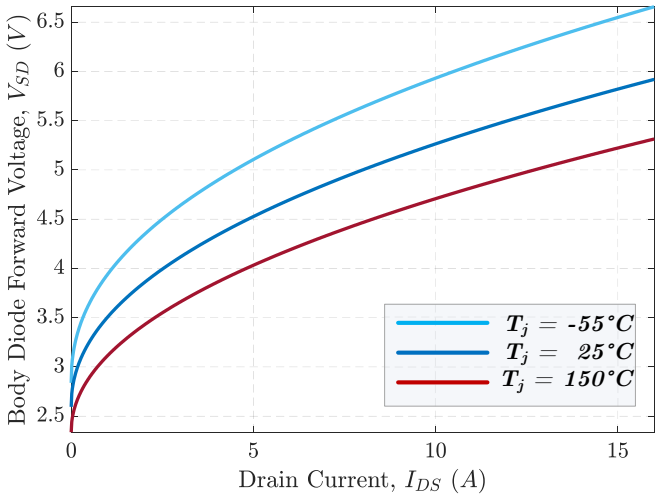


Figure 5.9. Variation of the V_{SD} vs. drain current for various temperatures ($@Vgs = -5V$).

Another possible issue related the proposed condition monitoring method is power modules with paralleled dies. In case of paralleled dies, this method will be able to monitor the overall variation of the packaging degradation in case of all dies having similar body diode knee voltage. However, for the gate oxide degradation, the method will only be able to monitor the variation in the die with lowest threshold voltage. Therefore, the utilization of the method in case of paralleled dies requires further investigation.

Finally, the proposed CM method monitors the package and gate oxide degradation based on the assumption of robust body diode. Although the body-diode of early generation of SiC MOSFETs had suffered serious reliability problems, with the improvement of substrate quality and optimized epitaxial layers the bipolar degradation of the body diode becomes less concerned. [52]

5.3 Experimental Validation

In order to validate the proposed CM method, a gate driver circuit board with complete CM feature is designed and experimentally tested. Although this method can be implemented in different ways for different applications, in this study, implementation on a phase leg configuration is given as an example. Here, the circuit diagram of the designed setup is only given for low-side switch in Fig. 5.10; however, the circuit can be used for both high and low sides. In this circuit, connection to the drain pin of the switch is required. Since the drain voltage is typically a high voltage, a high voltage/low current switch is used for protecting the current supply and sensing circuits. This switch can replace the desaturation diode in a real application, which is commonly used for short circuit protection. Although two different controlled current sources are shown in the circuit diagram for illustrating the operation principle, in real circuit one current source with adjustable current level is used. 0.1A and 0.5A are chosen for monitoring the gate oxide related degradation and packing related degradation respectively.

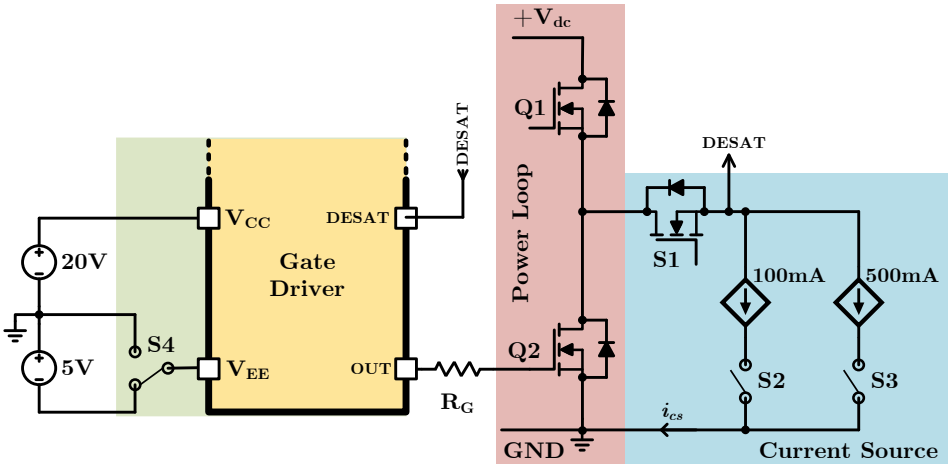


Figure 5.10. Circuit diagram of the gate driver circuit board with proposed complete CM feature for low-side switch.

The experimental gate driver circuit is shown in Fig. 5.11 as plugged into a double pulse tester. The detailed operation diagram of the circuit is illustrated in Fig. 5.12 in three

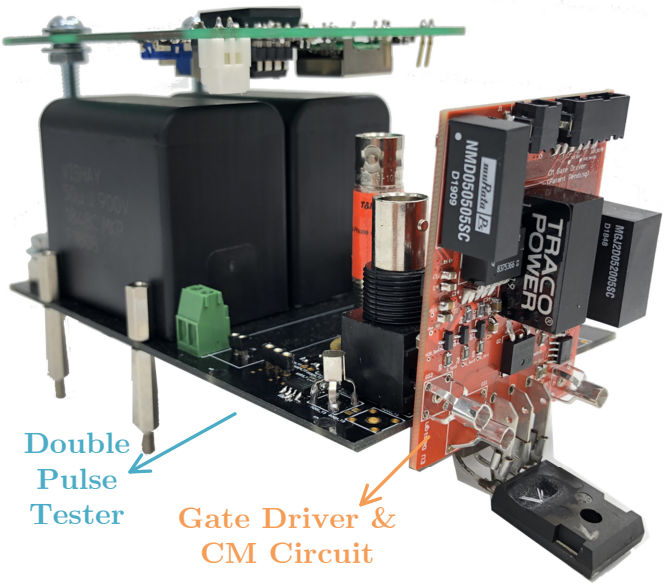


Figure 5.11. Experimental gate driver circuit setup as plugged into a double pulse tester

modes, i.e., gate oxide degradation monitoring, packing degradation monitoring and normal operation mode. During monitoring modes, both switches on the power loop are turned off. For gate oxide degradation monitoring, the protection switch S_1 and 0.1A current level set switch S_2 are turned on. In order to allow current conduction through the MOS channel, S_4 selection switch is toggled to the high position to apply 0V as gate bias as shown in Fig. 5.13(a). Once the supplied current (i_{cs}) is stable, V_{SD} value is captured as a signature of gate oxide degradation.

For the second operation mode, S_2 is turned off and S_3 is turned on and ics is set as 0.5A. In order to force the current conduction through the PiN diode, S_4 selection switch is toggled back to the low position to apply -5V as gate bias as shown in Fig. 5.13(b). Since, channel is not included in conduction path, V_{SD} value reflects packing related degradation. After completion of monitoring mode, S_1 is turned off and the circuit can switch to normal operation mode.

In order to verify the independently monitoring capability of the circuit, it is required to test devices which has only gate interface degradation or packaging degradation. Since it is

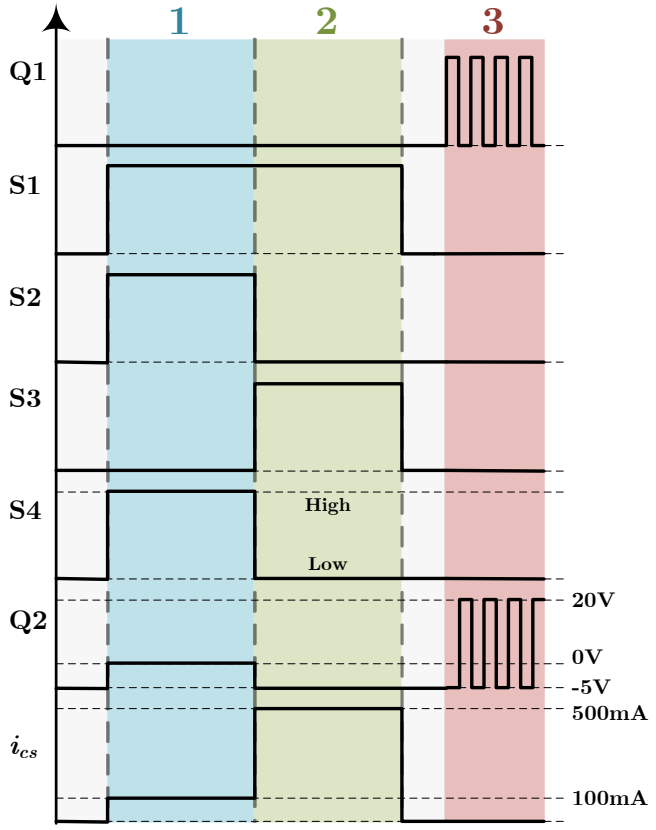


Figure 5.12. Operation diagram of the gate driver circuit board with complete CM feature.

very unlikely to individually trigger these degradation mechanisms under normal conditions, they are artificially created for testing purpose.

For gate oxide degradation, high temperature gate bias (HTGB) is applied on a switch at 150°C for 40 hours to trigger interfacial charge trapping. In order to show the effect more explicitly, a SiC MOSFET suffered from negative V_{th} drift is used and measure-stress-measure procedure is applied at each 10 hours.

Fig. 5.14 shows experimental oscilloscope waveforms of the switch during CM procedure of the designed circuit at two different HTGB cycles. As can be seen, there is a variation in V_{SD} value during gate oxide degradation monitoring while V_{SD} stays same during packaging degradation monitoring. At each measurement cycle, the V_{th} and V_{SD} (at 0.1A and 0V gate bias) values are also measured with the curve tracer as given in Fig. 5.15(a) and (b). These

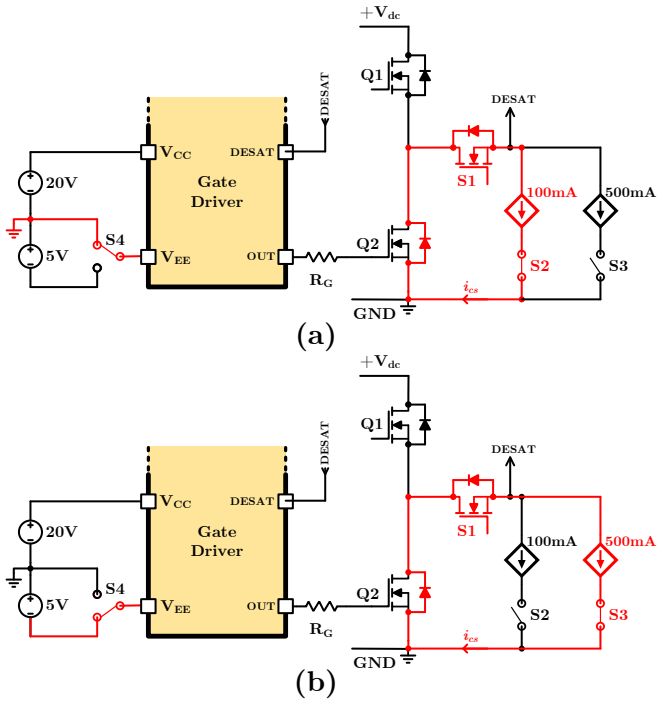


Figure 5.13. Circuit diagram of the gate driver circuit board with complete CM feature during (a) Gate degradation monitoring (b) Package degradation monitoring.

results verify that the detection circuit can measure the V_{SD} with a small offset and it can monitor the gate oxide degradation independently.

In order to verify the package degradation monitoring, a small area of mold compound -close to the source lead- is decapsulated in another SiC MOSFET, just to expose bond wires. Then bond wires are cut one by one and the switch is tested with monitoring circuit and V_{SD} values are captured. Additionally, $R_{ds,on}$ and V_{SD} (at 0.5A and -5V gate bias) values are measured with the curve tracer as given in Fig. 5.15(c) and (d). Results clearly show that V_{SD} values reflect the $R_{ds,on}$ variation and detection circuit can measure it accurately. It should be noted that a small offset in both V_{SD} measurements are due to $R_{ds,on}$ of the blocking switch. Experimental test results demonstrate that both degradation mechanisms can be monitored independently with the proposed method and the designed circuit can accurately detect the SOH of the device.

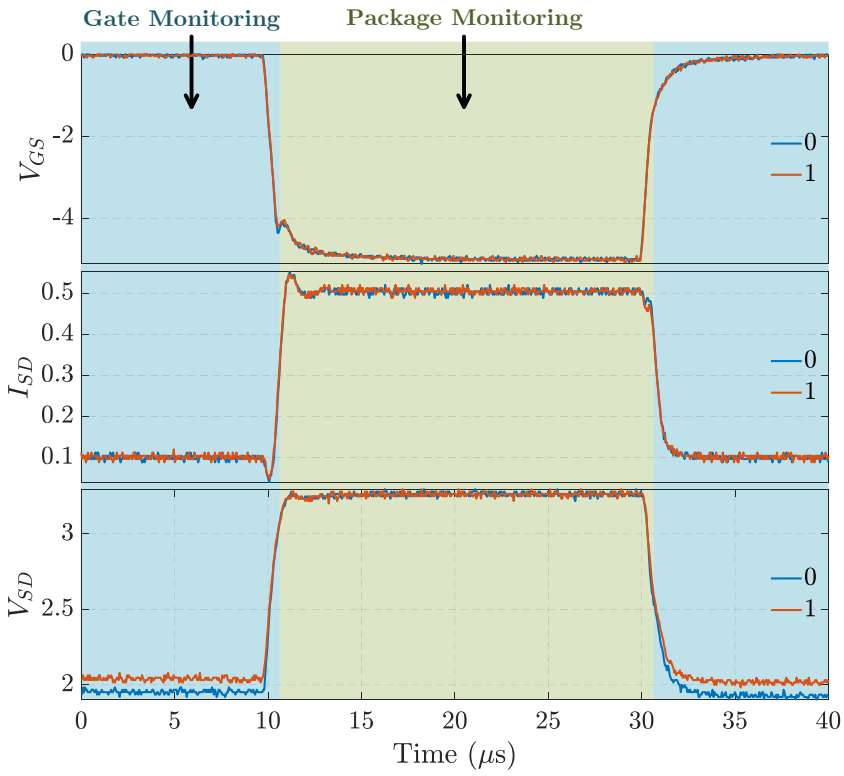


Figure 5.14. Experimental oscilloscope waveforms at two different HTGB cycles.

5.4 Conclusion

In this chapter, an improved condition monitoring method is proposed for SiC MOSFETs which can monitor both gate interface degradation and package related degradation independently by only capturing the body diode voltage drop at different gate bias values. A comprehensive evaluation of variations in commonly used precursor parameters and effect of each degradation mechanism is presented. Specifically, the SiC MOSFETs are exposed to high temperature power cycling, and key parameters are measured using an automated curve tracer at certain intervals. It has been shown that the gate threshold voltage increases logarithmically throughout the aging due to the gate oxide interface charge trapping. The ON-state resistance shows a very similar trend to the gate threshold voltage except two devices showing sudden increases after 7000 cycles. These jumps in ON-state resistance values

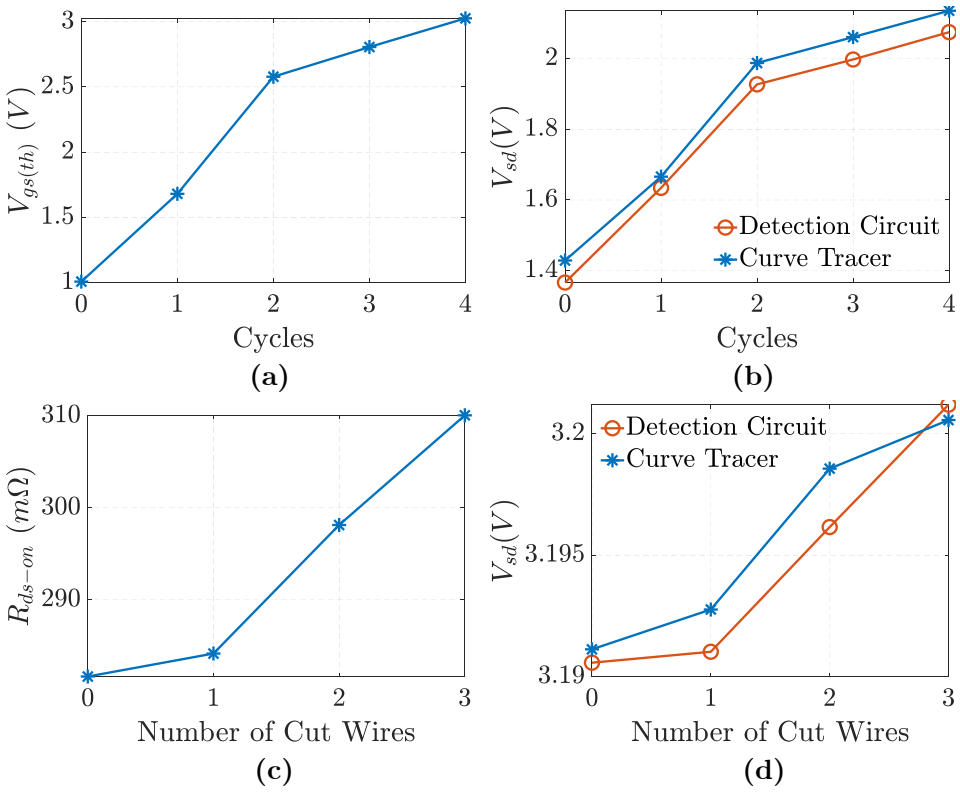


Figure 5.15. Experimental results for artificially degraded switches (a) V_{th} shift with gate stress (b) Comparison of V_{SD} measurements with monitoring circuit and curve tracer for gate stress (c) $R_{ds,on}$ shift with number of cut wires (d) Comparison of V_{SD} measurements for cut bond wire.

for two devices are also observed at body diode voltage drop with -5V gate voltage bias and both are attributed to the package related degradation. This assumption is verified with a detailed failure analysis and the root cause of the packing related degradation is found to be the wedge bond heel cracking. Due to the unique two different conduction modes feature of SiC MOSFETs in third quadrant operation, i.e., the MOSFET path conduction and the PiN path conduction, varying body diode voltage drop is revealed by the proposed body diode transfer characteristic curve. The body diode voltage drop variations captured throughout aging at 0V and -5V gate voltage bias and it found that contact resistance variations can be monitored with PiN diode path conduction while the gate oxide degradation can be detected during MOSFET path conduction. Therefore, it is concluded that just by capturing

body diode voltage drop at different gate biases, a complete state of health of SiC devices can be obtained. Based on this finding, the new condition monitoring method is invented and experimental implementation circuit is provided as an example. Experimental results are presented to demonstrate that the designed condition monitoring circuit can accurately detect both gate oxide degradation and the package related degradation. The main contribution of this invention is providing a method and experimental circuit to monitor both package and gate oxide degradation mechanisms with a single precursor and being able to distinguish the contribution of each.

CHAPTER 6

A DETAILED THIRD QUADRANT OPERATION ANALYSIS OF SIC MOSFET BODY DIODE

Until recently, one of the most severe reliability problems in SiC MOSFETs was bipolar degradation, which originates from basal plane dislocation (BPD) defects and expands with forward biasing of body diode [53]. This made the use of anti-parallel SiC schottky barrier diodes (SBD) required for dead time operation. However, with recent improvements in SiC processing technologies, BPD free SiC epitaxy, and stable body diode operation has been achieved [54]. Therefore, now, it is possible to utilize the body diode of SiC MOSFET for reverse conduction and to reduce SiC semiconductor cost by a factor of 1.5 to 2 by eliminating the need for anti-parallel SiC SBDs [50].

In order to effectively utilize the SiC MOSFET body diodes, it is crucial to understand their third quadrant operation in details. Unfortunately, as the use of SiC MOSFET body diodes has been avoided for a long time, literature covering their operation is scarce. Although two unique third quadrant conduction modes have been reported in the literature, a clear explanation on the physics behind two conduction modes has not been provided yet. The purpose of this chapter is to analyze the third quadrant operation of SiC MOSFETs using a commercial drift-diffusion simulation package [55] to provide a better insight for two different conduction modes, through the PiN path and MOSFET path.

The third quadrant I-V characteristic SiC MOSFET body-diodes is depended on the applied gate voltage. In Chapter 5, it is mentioned that there is a secondary conduction mode in third quadrant operation, which is unique to SiC MOSFETs. This behavior has been explained by the existence of two different conduction modes: 1) the PiN path when the gate voltage is less than -4V, and 2) the MOSFET path when the gate voltage is above -4V. However, there is no available T-CAD simulation study in order to verify the reported conduction modes and provide an understanding on how they are formed. Therefore, in

this chapter, the theory of third quadrant operation is explained firstly. Later, a detailed T-CAD simulation analysis of SiC MOSFET third quadrant operation has been provided for the first time in the literature. Finally, effect of the gate voltage on the reverse recovery characteristic of SiC MOSFET body diode is discussed.

6.1 Theory of Third Quadrant Operation

Due to their structure, Power MOSFETs have an integral PiN diode, which is formed between the p-well, the drift region, and the n^+ drain. In Si power MOSFETs, when MOSFET is at off-state and a negative voltage is applied to the drain contact with respect to the source contact, PiN diode starts to conduct with a voltage drop around 0.6V.

As long as the MOS channel is not turned on by applying a positive gate bias, PiN diode is the only mean of current conduction. Therefore, any gate to source voltage below threshold voltage does not influence diode forward voltage drop. However, in SiC MOSFETs, the body diode voltage drop changes with the gate to source voltage. For VGS values above approximately -4V. In order to clarify the difference between Si and SiC power MOSFET body diode voltage characteristic, a new I-V curve characterization is proposed.

For this characterization, constant current pulses is conducted through the device in the reverse direction and the gate to source voltage is swept from negative maximum bias to positive maximum bias. Since it shows resemblance to the MOSFET transfer characteristic, the proposed I-V characteristic curve is named as "body diode transfer characteristic".

The circuit setup to obtain the body diode transfer characteristic is shown in Fig. 6.1(a). The body diode transfer characteristics of different Si and SiC MOSFETs from different manufacturers are presented in Fig. 6.1(b). As seen, SiC MOSFETs exhibits very different body diode transfer characteristic compared to Si devices. The body diode transfer characteristic can be divided into three parts as: diode conduction, transition and MOS channel

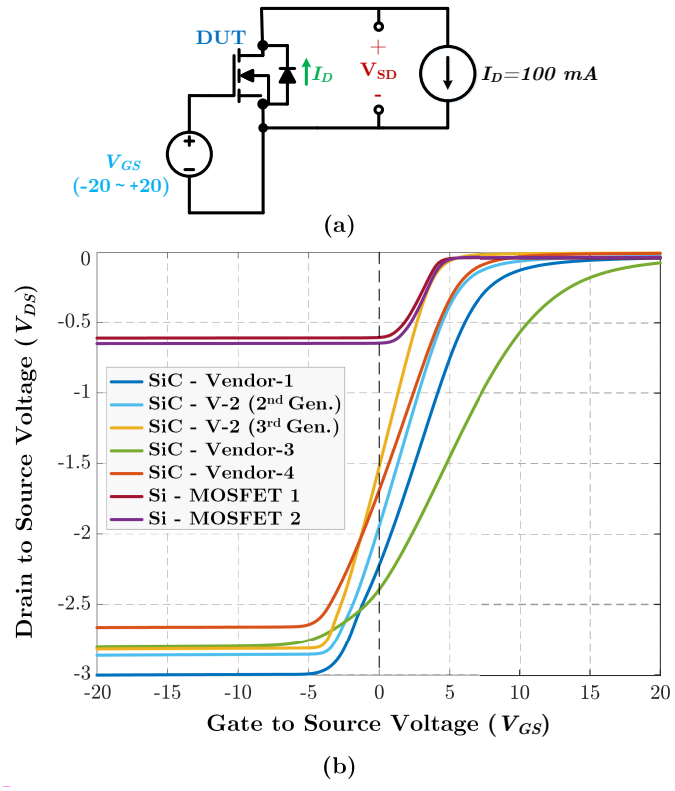


Figure 6.1. (a) Body diode transfer characterization circuit (b) Body diode transfer characteristics of different Si and SiC MOSFETs.

conduction. Firstly, for all SiC devices, V_{SD} is latched at much higher PiN diode voltage drop during diode conduction.

In SiC PiN diodes, the on-state voltage drop is substantially higher than that of Si. The build-in electric voltage across P-N junction diode is given by

$$V_{bi} = V_t.ln\frac{N_D N_A}{n_i^2} = \frac{2kT}{q}.ln\frac{N_D N_A}{n_i^2} \tag{6.1}$$

where V_t is thermal voltage, N_A is the acceptor concentration in the p region, N_D is the donor concentration in the n region, and n_i is the intrinsic carrier concentration. The injected carrier concentration in a SiC device can be assumed to be similar to those in Si devices. However, as it is described in Chapter 2, n_i of Si is $1.4x10^{10}cm^{-3}$ at room temperature $(300K)$, while it is only $6.7x10^{-11}cm^{-3}$ for SiC as a result of its higher bandgap. The large

difference in the intrinsic carrier concentrations results in a much higher forward voltage drop in SiC devices. For example, for the injected carrier concentration values producing $0.6V$ P-N junction voltage drop in Si, SiC P-N junction voltage drop will be $3.02V$. This explains the higher V_{SD} voltage drop in all SiC devices compared to Si for gate voltages lower than $-4V$.

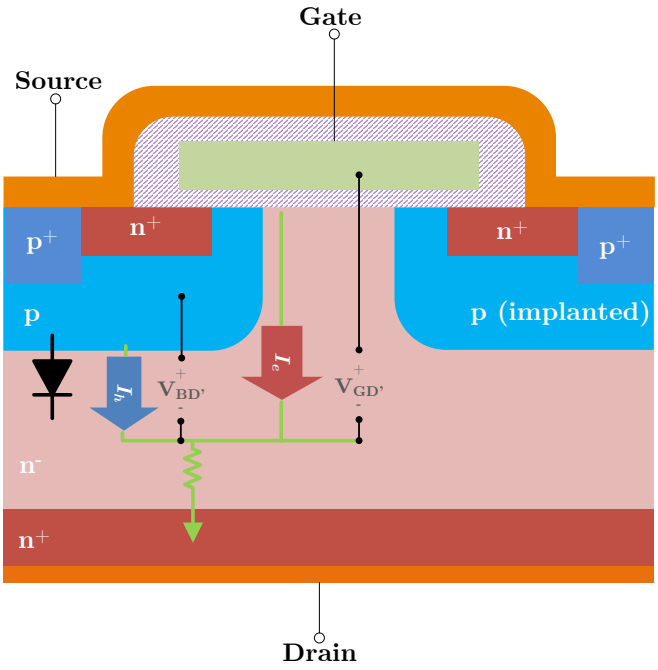


Figure 6.2. The current flow paths for SiC MOSFETs in the third quadrant.

Less anticipated difference however, is the larger transition range in SiC devices that starts at negative gate bias values. In Si MOSFETs, the V_{SD} value stays constant at P-N junction voltage drop around 0.6V for all lower gate bias values, until the gate bias reaches to the V_{th} and channel starts to conduct. On the other hand, in SiC MOSFETs, the V_{SD} value starts to decrease substantially when the gate bias is above a knee voltage, which is around -5V to -4V for most of the devices. With increasing gate bias, the V_{SD} value keeps decreasing, until the gate bias reaches to the positive V_{th} value and channel fully turns on. The variation in V_{SD} value -starting from negative bias values- is caused by formation of

a conductive path through the MOS channel, which is triggered by the V_{th} reduction with the influence of body effect [50, 51]. During this transition period, SiC MOSFET is mostly conducting through the MOS channel. In order to explain different conduction paths of SiC MOSFETs in the third quadrant operation, two different conduction paths, PiN path and MOSFET path, is presented in Fig. 6.2.

The third quadrant operation occurs for a power MOSFET when the current flows from the source to the drain terminal. During the third quadrant operation, the drain terminal has the lowest electrical potential and supplies electrons to the channel. Therefore, in reverse conduction, the physical drain terminal of the device becomes the electrical source. On the other hand, the source terminal is at a higher potential and removes electrons from the channel, and therefore it behaves electrically as the drain [56].

Although the p-well is shorted to n^+ source on the p^+ side, with the reverse current conduction, the p-well voltage at channel side (body voltage) will be lower than the source terminal voltage. Then, if the gate to source voltage is zero, the lower body voltage behaves effectively same as applying a positive gate bias. This effect is known as the body effect, and it will reduce the threshold voltage. The threshold voltage considering body effect can be found as:

$$V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_P - V_{SB}} - \sqrt{2\phi_P} \right) \tag{6.2}$$

$$V_{th0} = V_{FB} + 2\phi_P + \frac{\sqrt{4\varepsilon_S q N_A \phi_P}}{C_{ox}} \tag{6.3}$$

$$\phi_P = \frac{kT}{q} ln \left(\frac{N_A}{n_i} \right) \tag{6.4}$$

$$\gamma = \frac{\sqrt{2\varepsilon_S q N_A}}{C_{OX}} \tag{6.5}$$

where V_{th0} is zero bias threshold voltage, V_{SB} is the source to body voltage, V_{FB} is the flatband voltage, ϕ_P is the surface potential, γ is the body effect coefficient, and N_A is the

effective channel doping [57]. From (6.2), it can be seen that as V_{SB} increase with reverse current conduction, effective V_{th} voltage will drop.

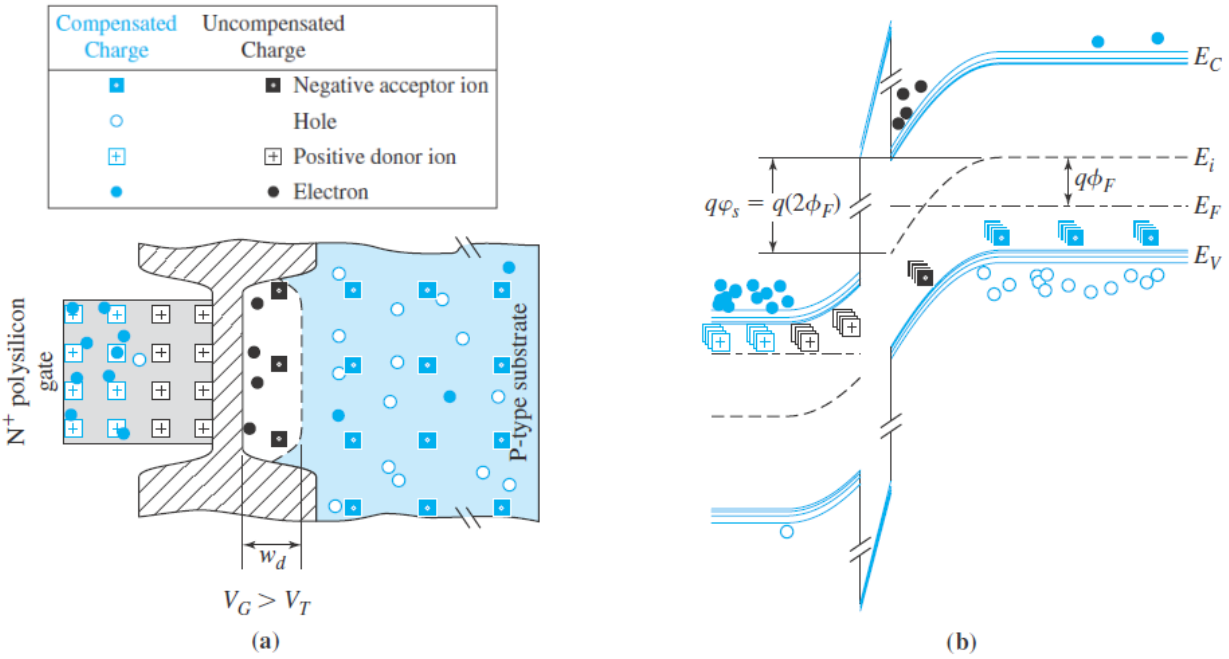


Figure 6.3. MOS channel in strong inversion (a) Cross section illustrating the types of charges. (b) The energy-band diagram (Reproduced with permission of the Licensor through PLSclear [15]).

To understand the effect clearly, we can re-visit the operation of n-channel lateral MOSFET. When a positive gate bias beyond the threshold voltage is applied to the gate terminal, the produced electric field attracts electrons to the channel surface and inverts the channel. Fig. 6.3(a) and Fig. 6.3(b) illustrates the channel inversion at the p-well surface as a response to a gate voltage increase beyond the threshold voltage [15].

In Fig. 6.3, only one dimension of the MOSFET operation, which is the direction from the silicon surface into the silicon body is shown. This dimension depicts the effect of the gate voltage on the channel inversion. However, a real MOSFET is not a one-dimensional structure. There is a second dimension along the silicon surface controlled by the drain-to-source voltage. For a better illustration, a two-dimensional energy-band diagram for an

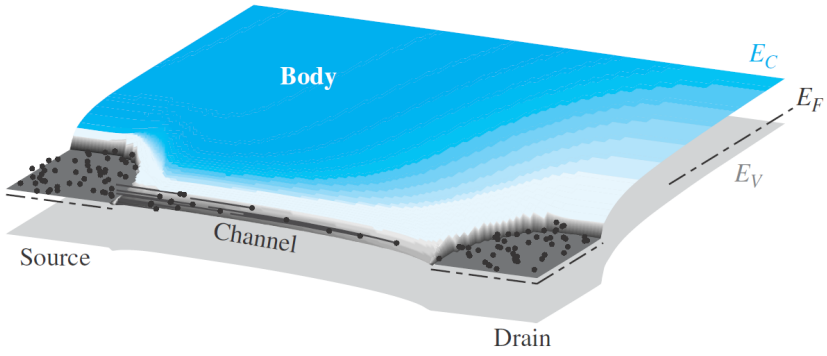


Figure 6.4. Two-dimensional energy-band diagram for an N-channel MOSFET in on mode (Reproduced with permission of the Licensor through PLSclear [15]).

N-channel MOSFET in on mode is shown in Fig. 6.4 [15]. The two colors in the conduction band indicate the concentrations of electrons and holes: darker colors correspond to higher carrier concentrations, whereas the nearly white areas indicate depleted regions. As seen from the figure, while the MOS channel is inverted with the positive gate bias, if an electric field is applied by means of a positive V_{DS}, the electrons from the source can flow through the channel into the drain. During this operation the body and the source terminals of the MOSFET are assumed to be short-circuited, which is the default case for the most applications.

Now lets assume that a negative body voltage V_{SB} is deliberately applied to the body contact or appeared as a voltage drop due to the current conduction in forward mode. In this case, the negative V_{SB} (or the p-body voltage with respect to the gate) increases the barrier between the electrons in the source and the drain. In Fig. 6.5, this effect is shown as a two-dimensional band diagram. In this case, the surface potential needs to be at least $2\phi_F + V_{SB}$ for channel inversion, compared to the surface potential of $2\phi_F$ for channel inversion when V_{SB}=0. This two-dimensional band diagram clearly shows how the V_{th} increases with the negative V_{SB}. However, in third quadrant operation, the current conduction is in reverse direction, which cause a positive V_{SB} voltage drop and therefore decreases the V_{th}.

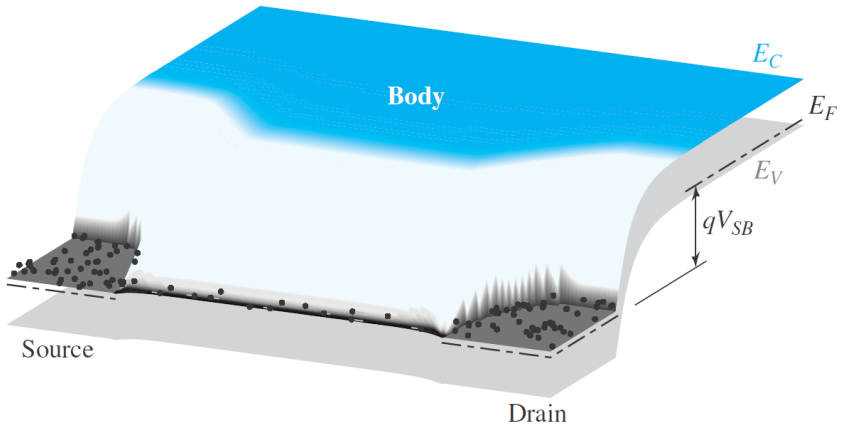


Figure 6.5. Illustration of the body effect: The surface potential needed to form the channel is $2\phi_F + V_{SB}$ (Reproduced with permission of the Licensor through PLSclear [15]).

To enable the channel conduction due to the body effect, the absolute value of V_{SB} should be higher than the absolute value of V_{th}. Only then, the positive V_{SB} voltage will have the effect of applying a positive gate bias beyond V_{th} and enable the channel conduction. Moreover, even if the V_{SB} value is less than the V_{th} but close to the absolute value of V_{th}, the body effect can still cause subthreshold conduction through the channel. In Si power MOSFETs, since the P-N junction forward voltage is small compared to the V_{th} voltage, the body effect alone is almost never able to cause the conduction through the channel. But, in SiC MOSFETs, due to the higher P-N junction forward voltage and lower threshold voltages, the body effect alone -without applying any gate bias- is able to create a channel inversion and provide current conduction through the channel. Furthermore, SiC MOSFET specific design implementations, like high deep p-well concentration, and depleted/lightly doped channel region, make the body effect more pronounced in SiC MOSFETs. In addition, low hole mobility cause very high p-well sheet resistance, which amplifies the V_{SB} voltage drop [1, 10]. Another factor causing more pronounced the body effect in SiC MOSFETs is the sub-micron channel lengths commonly utilized in modern SiC trench MOSFETs in order to reduce the channel resistance [58].

6.2 Physics-Based Computer-Aided Device Simulation

Since there is no available physics-based T-CAD simulation study in order to verify the reported conduction modes and provide an understanding on how they are formed, in this section a detailed T-CAD simulation analysis of SiC MOSFET third quadrant operation is presented for the first time in the literature. A SiC vertical D-MOSFET is modeled and simulated using complete cell structure in T-CAD simulation [55]. The cross-section of the simulated SiC MOSFET with critical dimensions is shown in Fig. 6.6. The MOSFET structure is designed for a rated blocking voltage of 1200V. The 2D MOSFET cell structure is designed for active area of $5\mu m^2$ with $5\mu m$ cell pitch and the default Z dimension depth of $1\mu m$. The n^+ substrate is $8\mu m$ deep and heavily doped with a donor concentration of $3.5 \times 10^{18} cm^{-3}$. The drift region thickness is designed as $10\mu m$ and uniformly doped with varying doping concentrations.

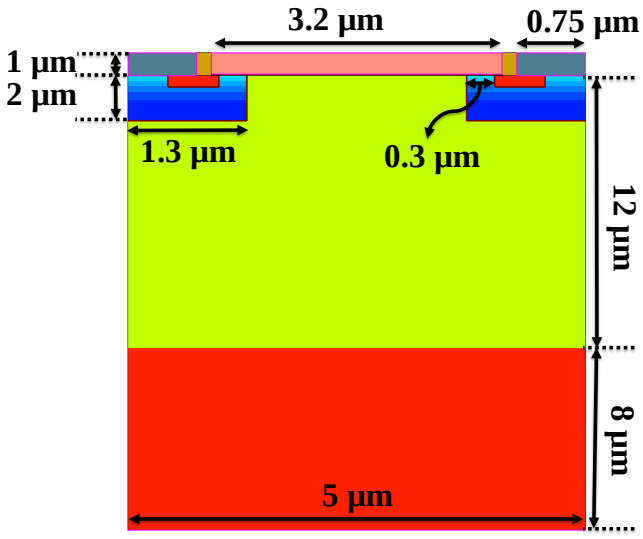
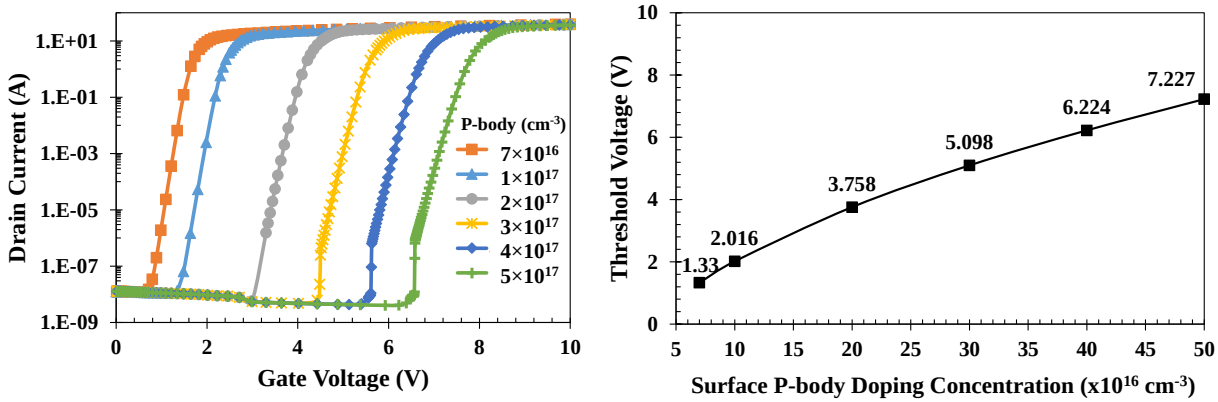


Figure 6.6. Cross-section of the simulated n-channel power SiC MOSFET with the indicated critical dimensions.

First of all, a systematic doping concentration optimization for n-type drift region (n_{drift}) and p-type body region (p_{body}) is performed to achieve a favorable device characteristics. In



(a) (b)

Figure 6.7. (a)Transfer characteristic (I_D-V_{GS}) of SiC MOSFET with uniformly doped n-drift region and Gaussian profile doped p-type body regions with varying surface doping concentration (b) Calculated V_{th} @I_D=250μA with varying $P_{surface}$.

the optimization process, first the effect of Gaussian profile doping for p-type body regions is investigated. For this, n-drift region doping concentration (N_{drift}) is fixed at $3 \times 10^{15} cm^{-3}$ with uniform doping. A deep p^+ layer is formed using Gaussian doping profile with a fixed deep p-well acceptor doping concentration (P_{bottom}) of $1.0 \times 10^{18} cm^{-3}$ at $2\mu m$ depth from the surface. The surface doping concentration of p-well ($P_{surface}$) is swept from $7 \times 10^{16} cm^{-3}$ to $5 \times 10^{17} cm^{-3}$. The transfer characteristics (I_D-V_{GS}) of SiC MOSFET with varying $P_{surface}$ is given in Fig. 6.7. The transfer characteristics shows that the threshold voltage (V_{th}) increases with increasing $P_{surface}$. Lightly doped channel region by utilizing the Gaussian doping distribution results in a lower V_{th}. V_{th} is calculated at a constant drain current I_D=250μA and V_{th}=2.0V is achieved when $P_{surface}$ is $1.0 \times 10^{17} cm^{-3}$.

Next, P_{bottom} and $P_{surface}$ are fixed at $1.0 \times 10^{18} cm^{-3}$ and $1.0 \times 10^{17} cm^{-3}$ respectively and N_{drift} is swept from $2.5 \times 10^{15} cm^{-3}$ to $5 \times 10^{15} cm^{-3}$. The transfer characteristics of SiC MOSFET with varying N_{drift} is given in Fig. 6.8, which shows that V_{th} is independent of drift doping concentration.

As another analysis, the effect of n-drift region doping concentration and p-well surface doping concentration on the output characteristic is investigated. First, P_{bottom} and $P_{surface}$

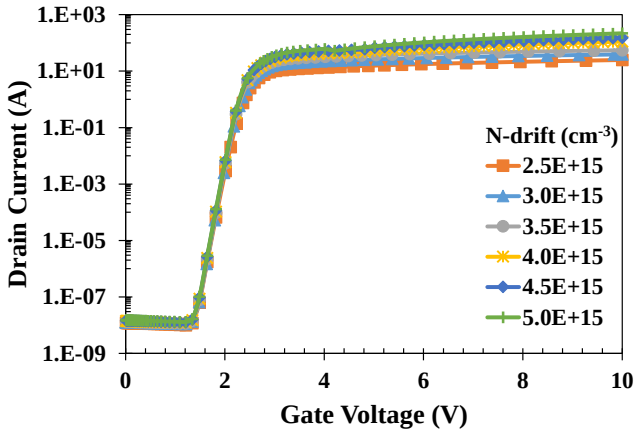


Figure 6.8. I_D-V_{GS} of SiC MOSFET with fixed P_{bottom} and $P_{surface}$ at $1.0 \times 10^{18} cm^{-3}$ and $1.0 \times 10^{17} cm^{-3}$ respectively and N_{drift} is varying.

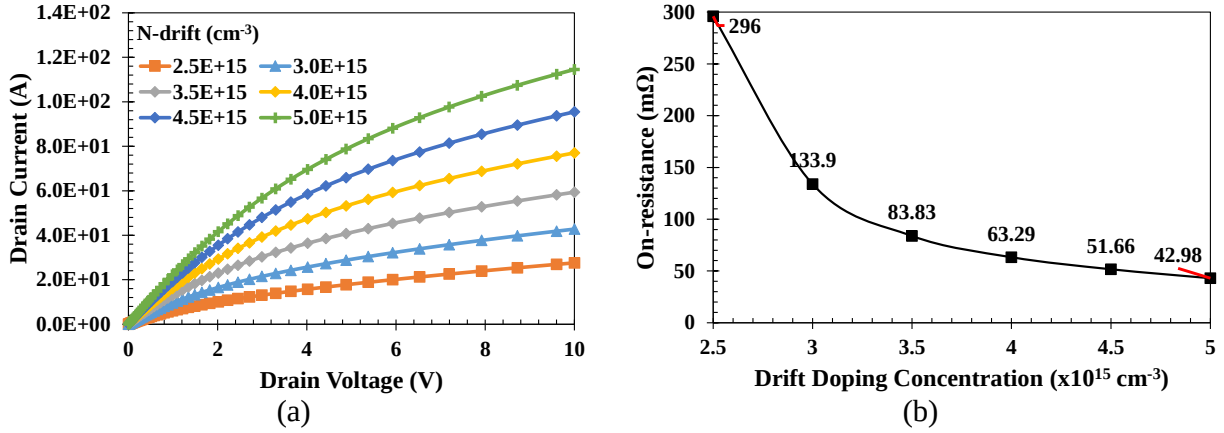


Figure 6.9. The effect of varying N_{drift} of SiC MOSFET on (a) I_D-V_{DS} output characteristics @V_{GS}=20V (b) Calculated R_{DS-on} @20A.

are fixed at $1.0 \times 10^{18} cm^{-3}$ and $1.0 \times 10^{17} cm^{-3}$ respectively and N_{drift} is swept from $2.5 \times 10^{15} cm^{-3}$ to $5 \times 10^{15} cm^{-3}$. The output characteristics (I_D-V_{DS}) of SiC MOSFET with varying N_{drift} is given in Fig. 6.9(a), which shows that on-state resistance (R_{DS-on}) increases by increasing N_{drift}. The calculated R_{DS-on} values with varying N_{drift} is given in Fig. 6.9(b). The aimed R_{DS-on} of $80m\Omega$ is obtained at N_{drift}=$3.5 \times 10^{15} cm^{-3}$. Second, P_{bottom} and N_{drift} are fixed at $1.0 \times 10^{18} cm^{-3}$ and $3.0 \times 10^{15} cm^{-3}$ respectively and $P_{surface}$ is swept from $7.0 \times 10^{16} cm^{-3}$ to $5.0 \times 10^{17} cm^{-3}$. The output characteristics of SiC MOSFET with varying

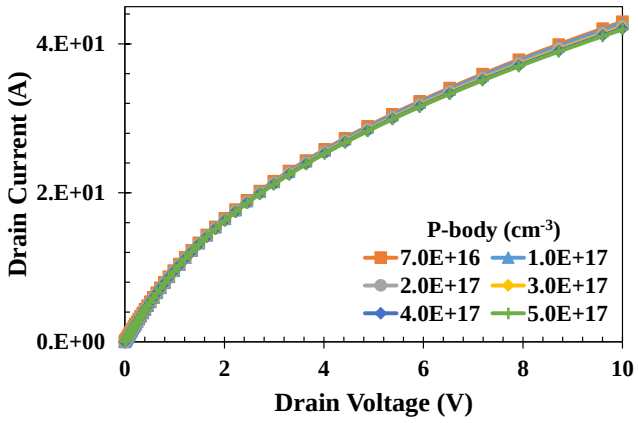


Figure 6.10. The effect of varying $P_{surface}$ of SiC MOSFET on I_D-V_{DS} output characteristics @V_{GS}=20V.

P_{bottom} is given in Fig. 6.10, which does not show any major difference in the R_{DS-on} with changing P_{bottom}.

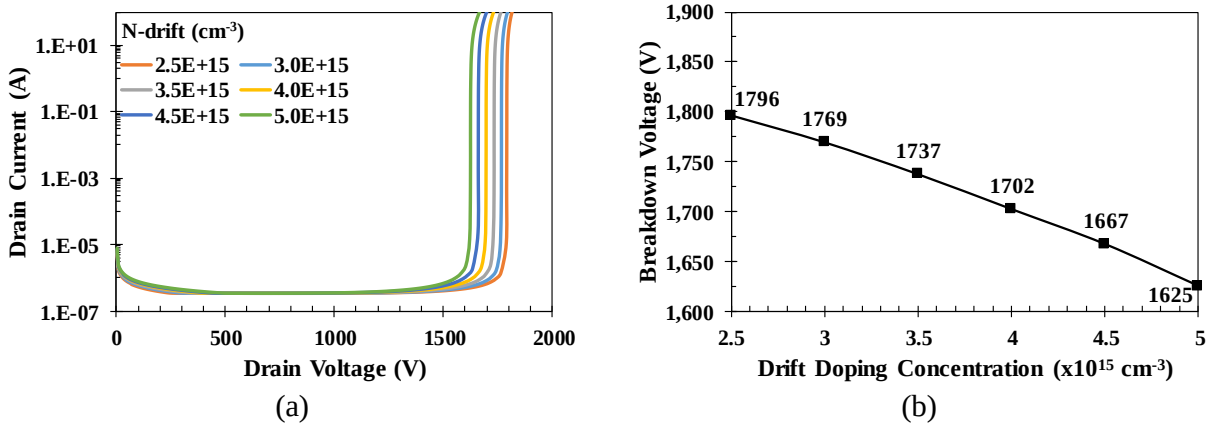


Figure 6.11. The effect of varying N_{drift} of SiC MOSFET on (a) I_{DSS}-V_{DS} drain leakage current characteristic @V_{GS}=0V (b) Calculated BV_{DSS} @I_D=100μA.

As a final step in doping concentration optimization, the effect of n-drift region doping concentration and p-well surface doping concentration on breakdown voltage is investigated. First, P_{bottom} and $P_{surface}$ are fixed at $1.0 \times 10^{18} cm^{-3}$ and $1.0 \times 10^{17} cm^{-3}$ respectively and N_{drift} is swept from $2.5 \times 10^{15} cm^{-3}$ to $5 \times 10^{15} cm^{-3}$. The drain leakage current characteristic (I_{DSS}-V_{DS}) of SiC MOSFET with varying N_{drift} is given in Fig. 6.11(a), which shows that

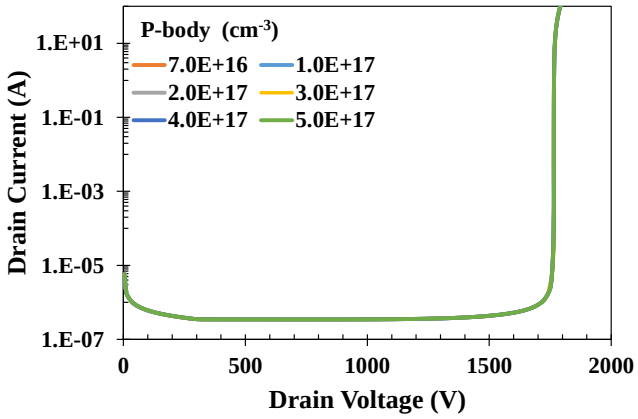


Figure 6.12. The effect of varying $P_{surface}$ of SiC MOSFET on I_{DSS}-V_{DS} drain leakage current characteristic @V_{GS}=0V.

breakdown voltage (BV_{DSS}) decreases with increasing N_{drift}. The calculated BV_{DSS} values with varying N_{drift} is given in Fig. 6.11(b). Second, P_{bottom} and N_{drift} are fixed at $1.0 \times 10^{18} cm^{-3}$ and $3.0 \times 10^{15} cm^{-3}$ respectively and $P_{surface}$ is swept from $7.0 \times 10^{16} cm^{-3}$ to $5.0 \times 10^{17} cm^{-3}$. The drain leakage current characteristic of SiC MOSFET with varying P_{bottom} is given in Fig. 6.12, which does not show any major difference in the BV_{DSS} with changing P_{bottom}.

As a result of systematic doping concentration optimization, the doping densities are fixed as: N_{drift}=$3.5 \times 10^{15} cm^{-3}$, P_{bottom}=$1.0 \times 10^{18} cm^{-3}$, and $P_{surface}$=$1.0 \times 10^{17} cm^{-3}$.

After the doping concentration optimization, the effect of the junction temperature (T_J) is also investigated. First, the effect of T_J on the transfer characteristic behavior of SiC MOSFET at V_{DS}=10 V is investigated. For this, the transfer characteristic behavior is simulated at different junction temperatures and the simulation results are shown in Fig. 6.13(a). In Fig. 6.13(b) the calculated V_{th} values at various T_J is given which shows that V_{th} decreases by increasing temperature.

Second, the effect of T_J on the output characteristic of SiC MOSFET at V_{GS}=20 V is investigated. For this, the output characteristic behavior is simulated at different junction temperatures and the simulation results are shown in Fig. 6.14(a). In Fig. 6.14(b) the

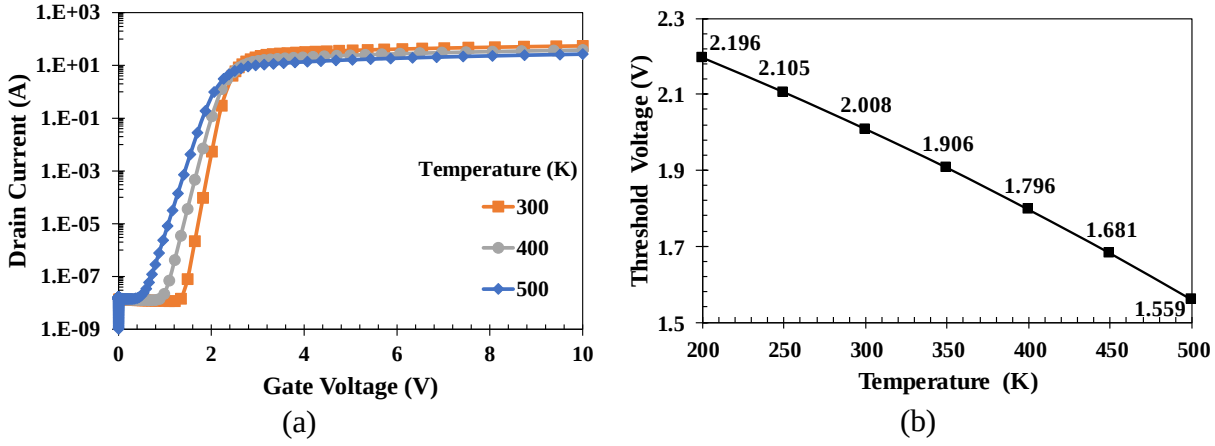


Figure 6.13. (a)Transfer characteristic (I_D-V_{GS}) of SiC MOSFET at different junction temperatures (b) Calculated V_{th} vs. T_J.

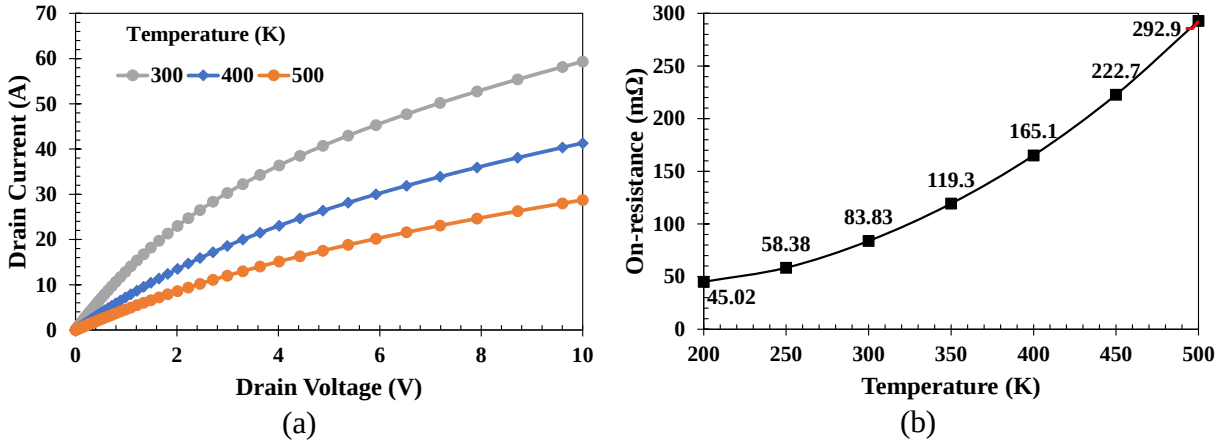


Figure 6.14. (a)Output characteristic (I_D-V_{DS}) of SiC MOSFET at different junction temperatures (b) Calculated R_{DSon} vs. T_J.

calculated R_{DSon} values at various T_J is given which shows that R_{DSon} substantially increases when T_J is increased.

Finally, the effect of T_J on the breakdown behavior of SiC MOSFET at V_{GS}=0 V is investigated. For this, the breakdown behavior is simulated at different junction temperatures and the simulation results are shown in Fig. 6.15(a). In Fig. 6.13(b) the calculated BV_{DSS} values at various T_J is given. As seen, BV_{DSS} has a minimum around $250K$ and increases at the temperatures below and above this point.

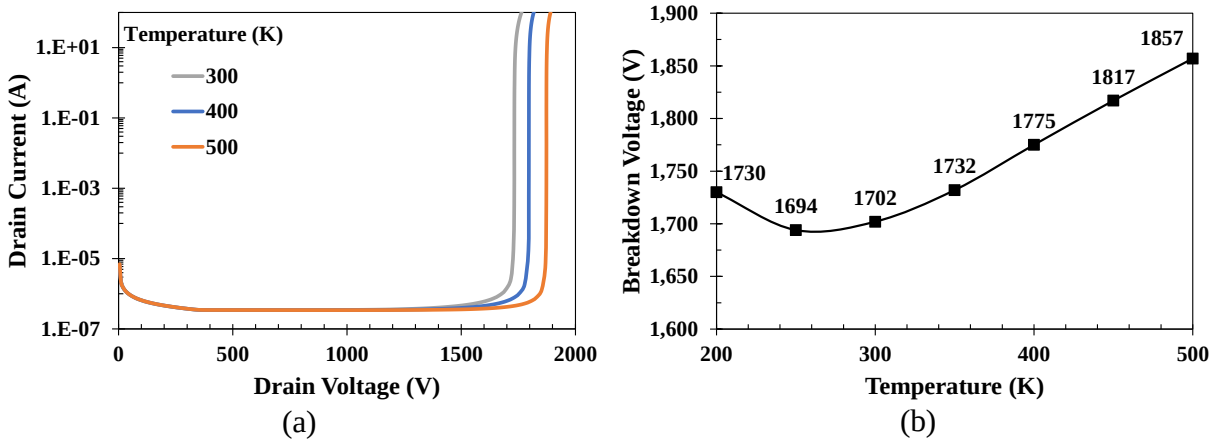


Figure 6.15. (a)Drain leakage current characteristic (I_{DSS}-V_{DS}) of SiC MOSFET at different junction temperatures (b) Calculated BV_{DSS} vs. T_J.

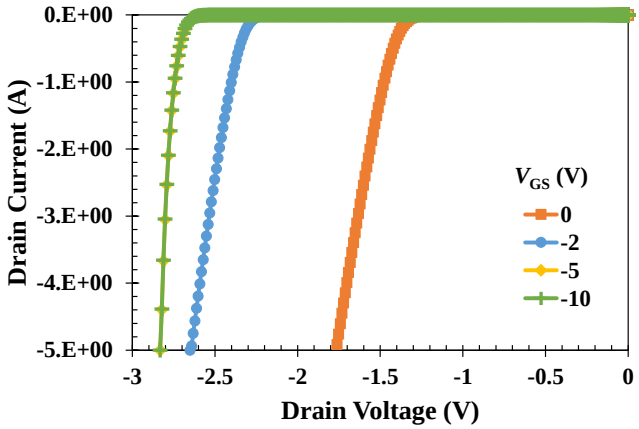


Figure 6.16. Body diode characteristic as a function of gate bias for n-channel SiC MOSFET.

With the completion of the doping concentration optimization and the junction temperature effect verification, as the primary goal of this T-CAD simulation study, the third quadrant operation of SiC MOSFET is analyzed in T-CAD simulation. With optimized MOSFET design, the body diode characteristic is simulated at T_J=300K. The simulation results of SiC MOSFET third quadrant characteristic is presented in Fig. 6.16 for different negative gate bias values. The simulation result shows that the third quadrant characteristic of the SiC MOSFET is changing for the gate bias values higher than -5V. At V_{GS}=0V, V_{SD} knee voltage is much smaller than the built-in P-N junction voltage drop. As we decrease

the gate bias from 0V through -10V, V_{SD} knee voltage increases with decreasing V_{GS}, until V_{GS} becomes -5V. However, there is no difference between the third quadrant characteristic for V_{GS}=-5V and V_{GS}=-10V. The simulation result perfectly coincides with the commercial SiC MOSFET datasheets and the measurement results provided in previous chapters. This concurrence verifies that the developed T-CAD model can simulate SiC MOSFET third quadrant operation accurately.

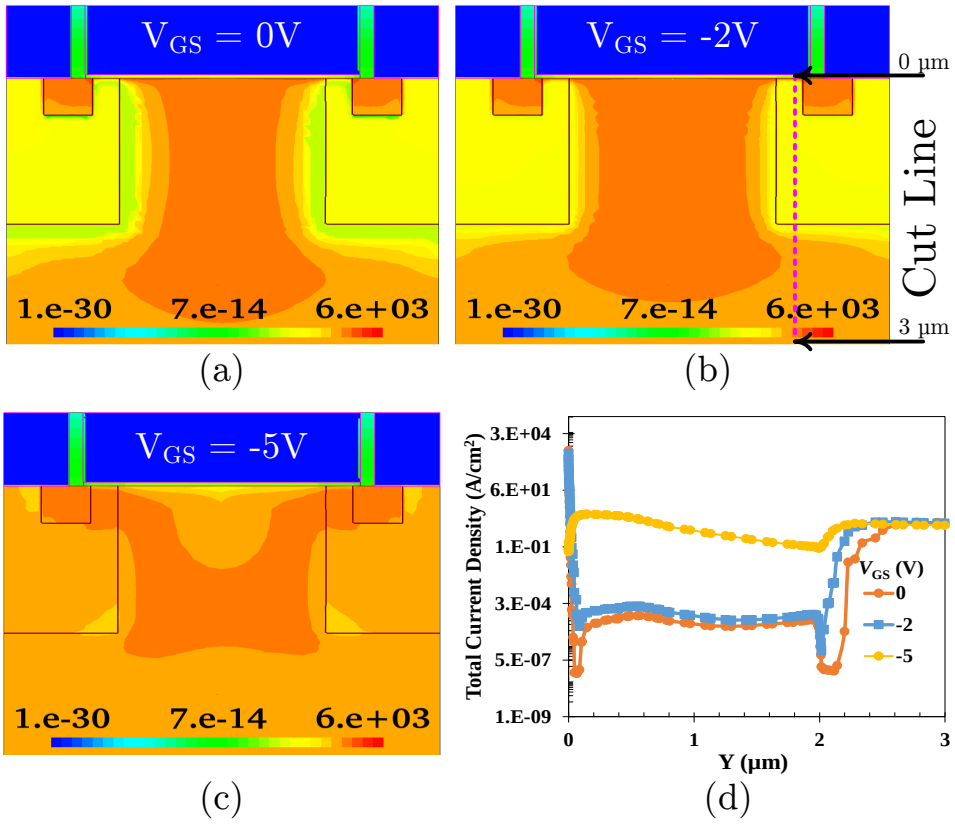


Figure 6.17. (a-c) Total current distribution at low current density (I_{SD}=100mA) for different V_{GS} values. (d) Total current profile along the Y-axis cutline at middle of the channel (as shown in (b)).

After verifying third quadrant operation simulation, the current density distribution during reverse conduction is analyzed. First, total current density distribution is simulated at low current density (I_{SD}=100mA) for three different V_{GS} values, i.e., 0V, -2V, and -5V. Two-dimensional T-CAD simulation of total current density distribution at low current density

is illustrated in Fig. 6.17 (a)-(c) for three different V_{GS} values and total current profile along the Y-axis cutline at the middle of the channel is shown in Fig. 6.17 (d). For V_{GS} values of 0V and -2V, the channel is still on and conduction most of the current. The very high peak current density close to Y=0μm along the Y-axis cutline also verifies the channel conduction. When V_{GS}=-5V, the channel is completely blocked, and the current density spreads across the P-N junction and has more uniform distribution along the Y-axis cutline except for the channel region.

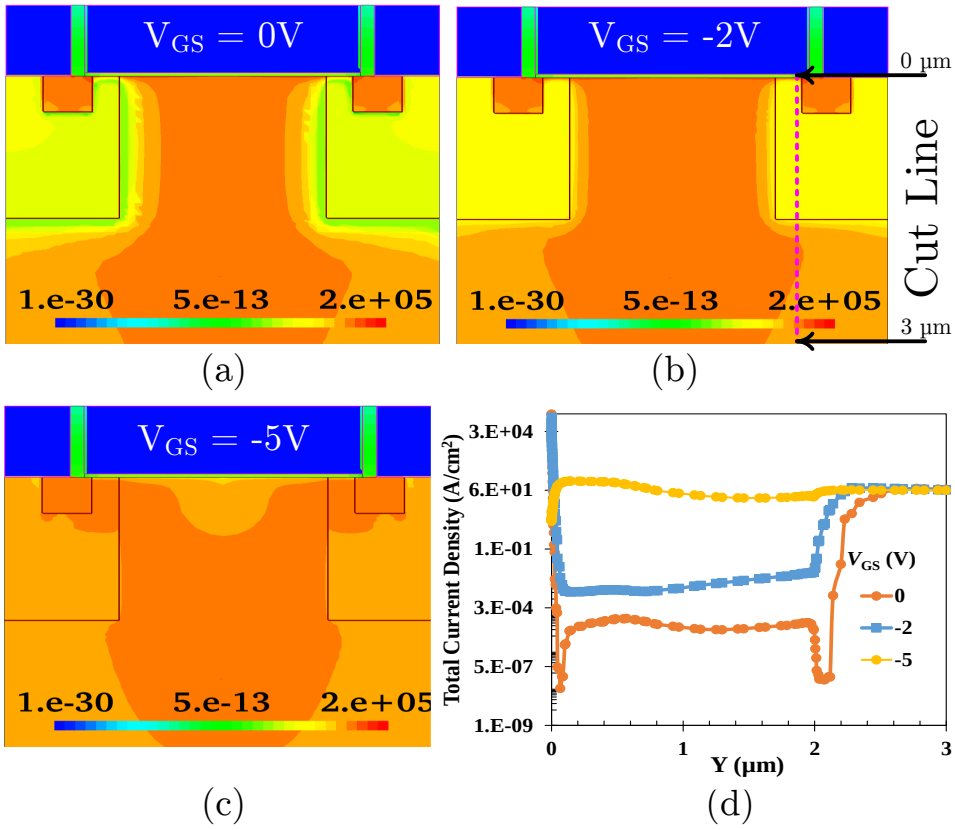


Figure 6.18. (a-c) Total current distribution at high current density (I_{SD}=5A) for different V_{GS} values. (d) Total current profile along the Y-axis cutline at middle of the channel (as shown in (b)).

Next, the total current density distribution is simulated at high current density (I_{SD}=5A) for three different V_{GS} values, i.e., 0V, -2V, and -5V. Two-dimensional T-CAD simulation of total current density distribution is illustrated in Fig. 6.18 (a)-(c) for three different V_{GS}

values and total current profile along the Y-axis cutline at the middle of the channel is shown in Fig. 6.18 (d). Similarly to the low current density simulations, at V_{GS} values of 0V and -2V, the channel is still on and conduction most of the current. The very high peak current density close to Y=0μm along the Y-axis cutline also verifies the channel conduction. When V_{GS}=-5V, the channel is completely blocked, and the current density spreads across the P-N junction and has more uniform distribution along the Y-axis cutline except for the channel region.

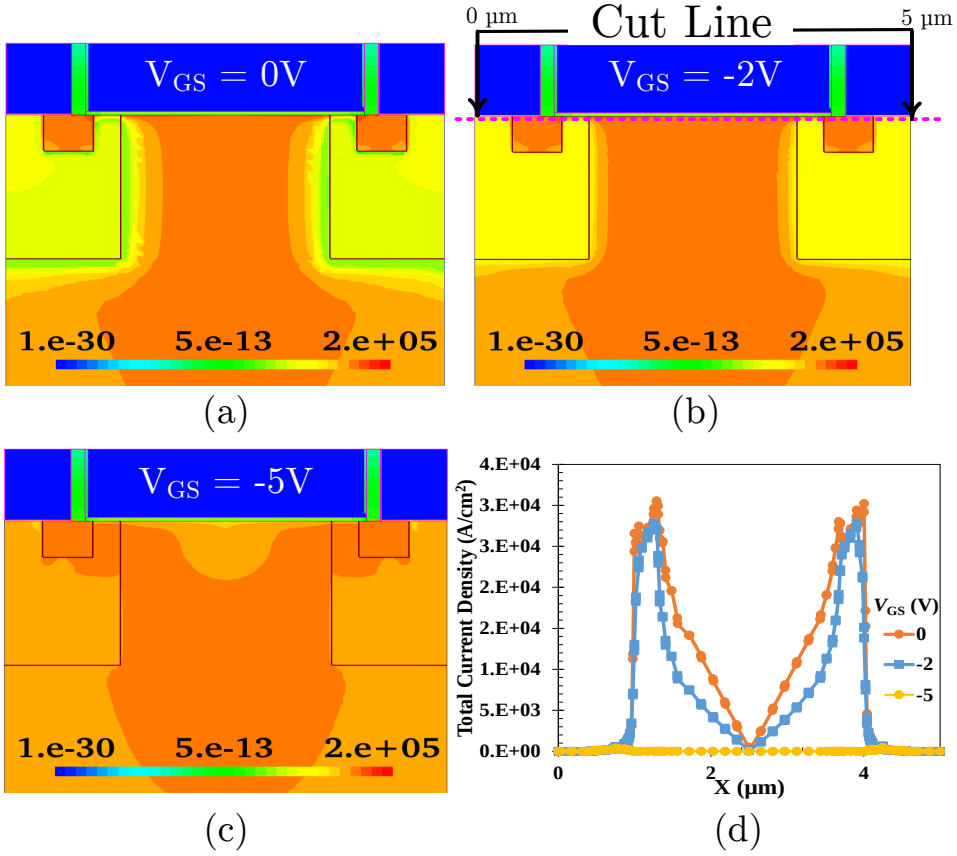
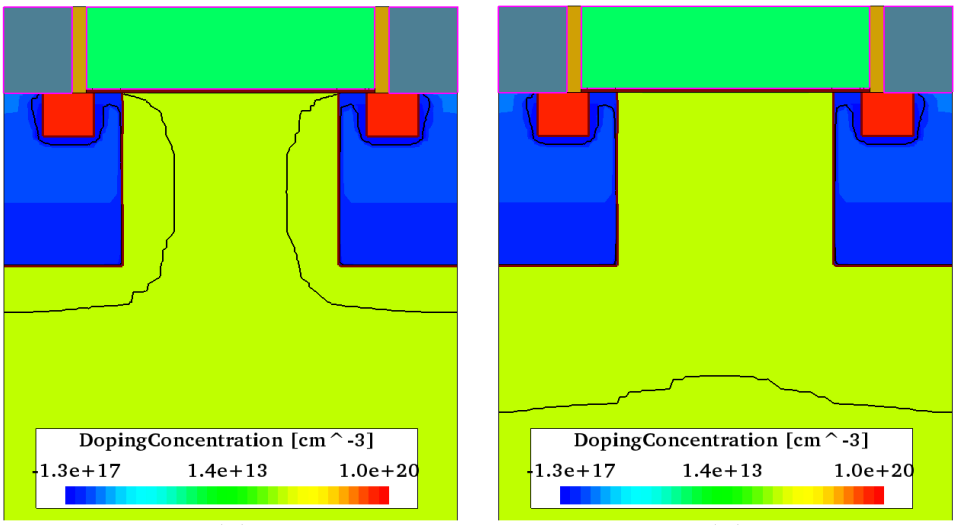


Figure 6.19. (a-c) Total current distribution at high current density (I_{SD}=5A) for different V_{GS} values. (d) Total current profile along the X-axis cutline at the channel surface (as shown in (b)).

For further verification of the channel conduction, the total current density distribution profile at high current density is also analyzed along the X-axis cutline at the channel surface.

Illustration of the X-axis cutline and the total current profile along the X-axis cutline at the channel surface is shown in Fig. 6.19. The total current profile along the X-axis cutline clearly illustrates the current conduction at the channel region for V_{GS} values of 0V and -2V. Moreover, it also discloses zero current density for V_{GS}=-5V.



(a) (b)

Figure 6.20. Doping concentration and depletion layer boundaries (a) at negative @V_{DS} (b) at positive @V_{DS} .

As explained in Section 6.1, one factor causing more pronounced the body effect in SiC MOSFETs is the short-channel design utilized in modern SiC MOSFETs [58]. In this case, one can wonder how the SiC MOSFETs can have channel conduction with negative V_{DS} while it has very low leakages when V_{DS} is positive. In order to investigate this phenomenon, the doping concentration in SiC MOSFET is simulated under negative and positive V_{DS} while V_{GS}=0V, as shown in Fig. 6.20. When the V_{DS} is negative, the depletion region shrinks and exposes the channel region, which allows current conduction in reverse direction. When the depletion region shrinks as shown in Fig. 6.20(a), electrons will only have the short channel as a barrier, which further reduces with the body effect. However, when the V_{DS} is positive, the depletion region quickly extends and shields the channel region, as can be seen

in Fig. 6.20(b). Therefore, SiC MOSFET can have a very low leakage current in blocking mode.

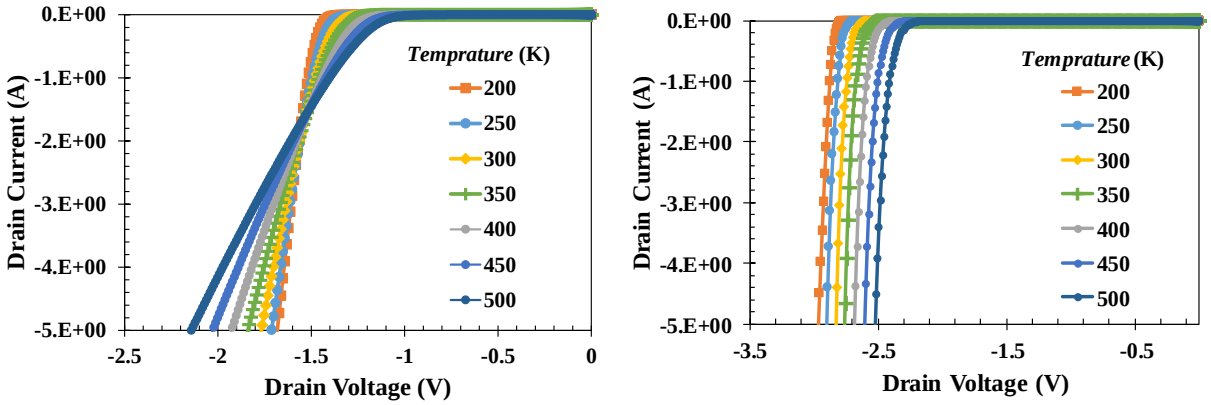


Figure 6.21. Body diode characteristics as a function of temperature (a) @V_{GS}=0V (b) @V_{GS}=-5V.

Finally, the effect of the junction temperature (T_J) on the third quadrant characteristic is investigated. The body diode characteristics are simulated at V_{GS}=0V and V_{GS}=-5V and the I_D-V_{DS} curves are shown in Fig. 6.21. The I_D-V_{DS} curves at different gate biases reveal different temperature responses at different conduction modes. When V_{GS}=0V, the knee voltage decreases due to decreasing threshold voltage, but the channel resistance increase reduces the I_D-V_{DS} slope, as seen in Fig. 6.21(a) [55]. When V_{GS}=-5V, the knee voltage decreases with increasing temperature due to decreasing P-N junction voltage drop, as seen in Fig. 6.21(b).

These T-CAD simulation results clearly verify the existence of two different conduction paths due to the body effect. In summary, when V_{GS}=0V, the channel is still conducting, and V_{SD} knee voltage is much smaller than the built-in P-N junction voltage drop. With negative V_{GS} values, the knee voltage increases. When V_{GS}=-5V or more negative, the channel is completely blocked, and the knee voltage is not changing anymore.

6.3 Reverse Recovery of SiC MOSFET Body Diode

The evidence of SiC MOSFETs conducting through the MOS channel at V_{GS}=0V raises another question for the third quadrant operation of SiC MOSFETs: How the channel conduction would possibly influence the reverse recovery characteristic of the SiC MOSFET body diode. Fig. 6.22 shows the body diode switching characteristics of three different MOSFET technologies, i.e., CoolMOS, Si MOSFET, and SiC MOSFET at -75°C and 175°C [59]. The reverse recovery current comparison shows a much lower reverse recovery charge in SiC MOSFET body diodes.

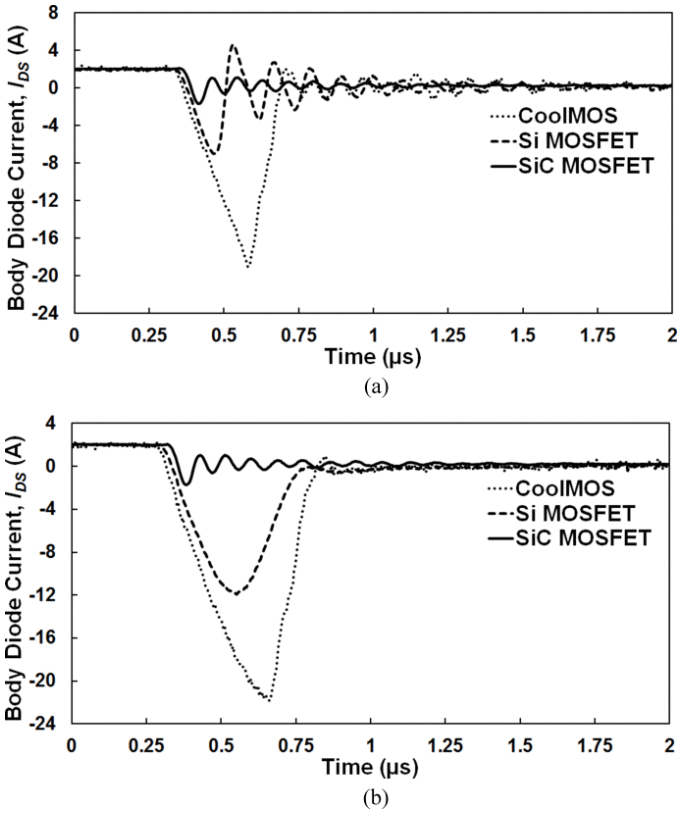


Figure 6.22. Comparison of the reverse recovery current of SiC MOSFET, silicon power MOSFET, and CoolMOS body diode with a forward current of 2 A, at (a) -75°C (b) 175°C (Reproduced with permission from IEEE [59]).

Although the SiC MOSFETs have significantly low reverse recovery current, the reverse recovery can still be an issue -especially at high switching frequency applications. Therefore,

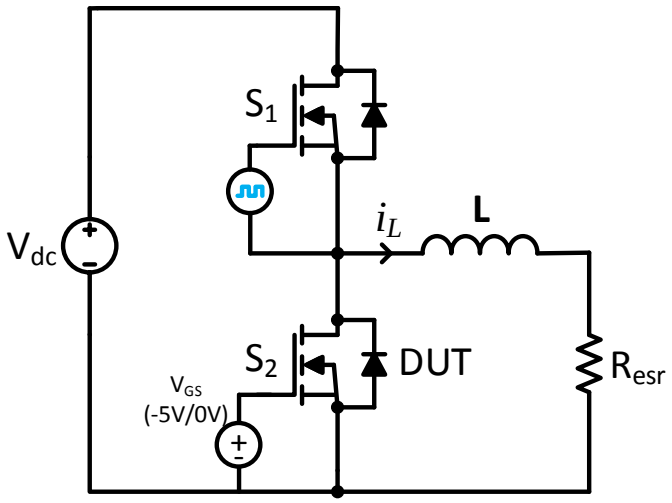


Figure 6.23. The circuit diagram of the reverse recovery test setup.

the impact of the negative gate bias voltage on the reverse recovery characteristics of the SiC MOSFET body diodes is investigated in this section.

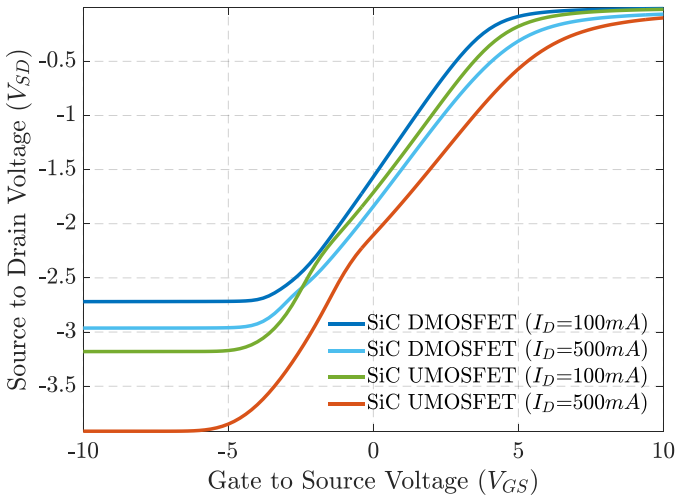


Figure 6.24. Body diode transfer characteristics of tested SiC MOSFETs.

For this test, the reverse recovery of one planar and one trench SiC MOSFETs, with a 1200V blocking voltage and 75$m\Omega$ typical on-resistance, are tested experimentally. The circuit diagram of the experimental test setup utilized for the reverse recovery test is shown in Fig. 6.23. The device under test (DUT) is biased with 0V and -5V gate voltage, and

the switching speed is controlled by the high side switch which uses $R_G = 2\Omega$ as the gate resistor.

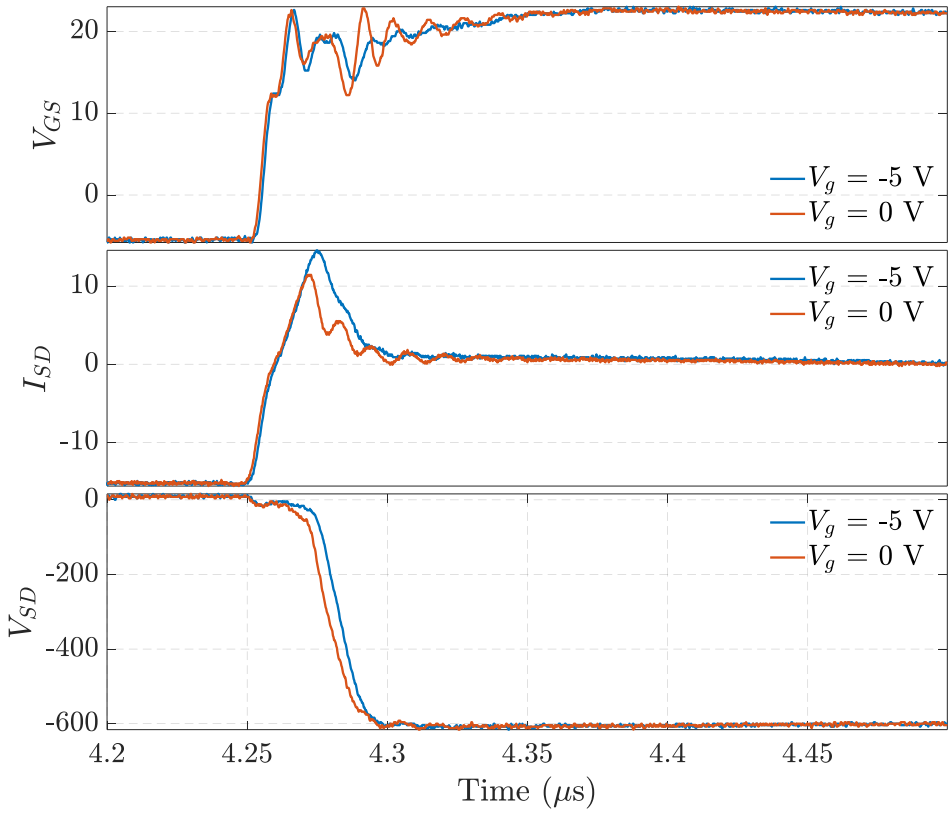


Figure 6.25. Experimental body diode reverse recovery test waveforms for the planar SiC MOSFET body at diode at V_{GS}=-5V and V_{GS}=0V.

In order to define the gate voltage which completely blocks the MOS channel conduction in these devices, the body diode transfer characteristics of both the planar and the trench SiC MOSFETs at I_{DS}=-100mA and I_{DS}=-500mA are presented in Fig. 6.24. As it can be seen, the planar SiC MOSFET settles to a constant V_{SD} value around V_{GS}=-4V. Therefore the channel should be blocked at V_{GS}=-5V. On the other hand, the V_{SD} transition period of the trench MOSFET goes beyond V_{GS}=-5V, even at a relatively low drain current density of $500mA$. Consequently, even with V_{GS}=-5V, the trench MOSFET is expected to conduct current through the channel.

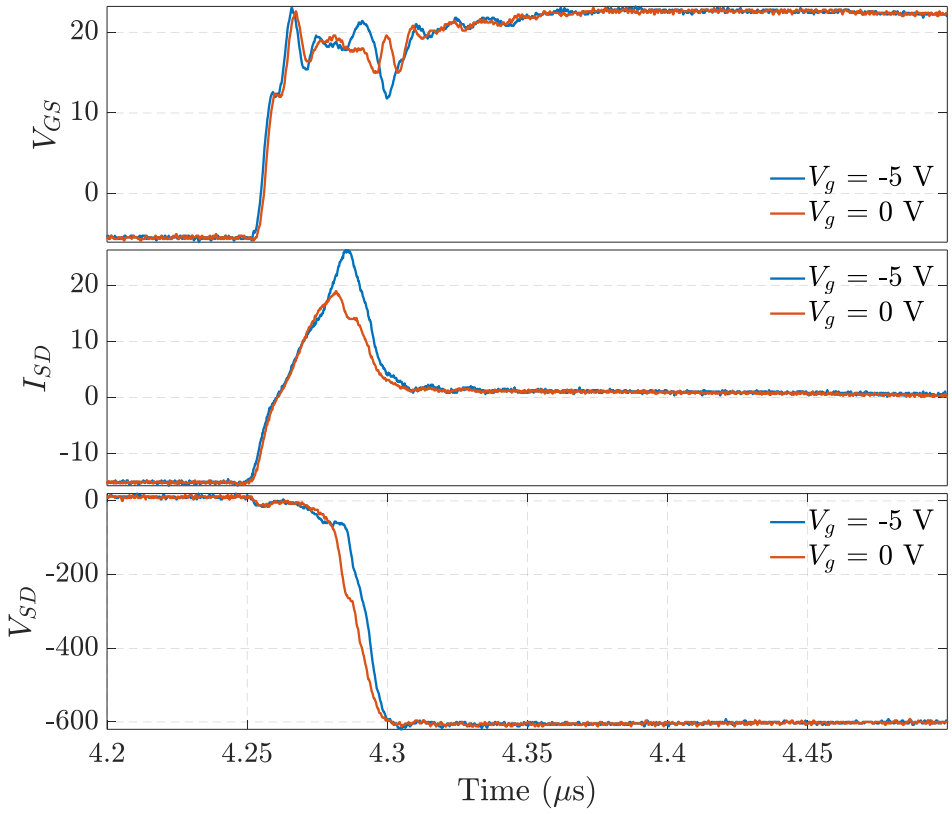


Figure 6.26. Experimental body diode reverse recovery test waveforms for the trench SiC MOSFET body at diode at V_{GS}=-5V and V_{GS}=0V.

The reverse recovery tests are carried out at 600V DC bus voltage (V_{DC}) and 15A diode forward current (I_F). When the body diode conducts in the forward direction, a large concentration of electron and hole carriers are injected into the drift layer. In order to switch the diode from the forward conduction to reverse high voltage blocking, the injected free carriers need to be swept out of the drift layer to enable the formation of a depletion layer. This process is referred to as reverse recovery, and during this process, a large recovery current flows through the diode in the reverse direction, causing a large reverse recovery loss.

In order to measure the reverse recovery characteristics, the body diode should first conduct current in the forward direction and then switch to high voltage blocking. For this, first, the top side switch is turned on to increase the inductor current. When the inductor

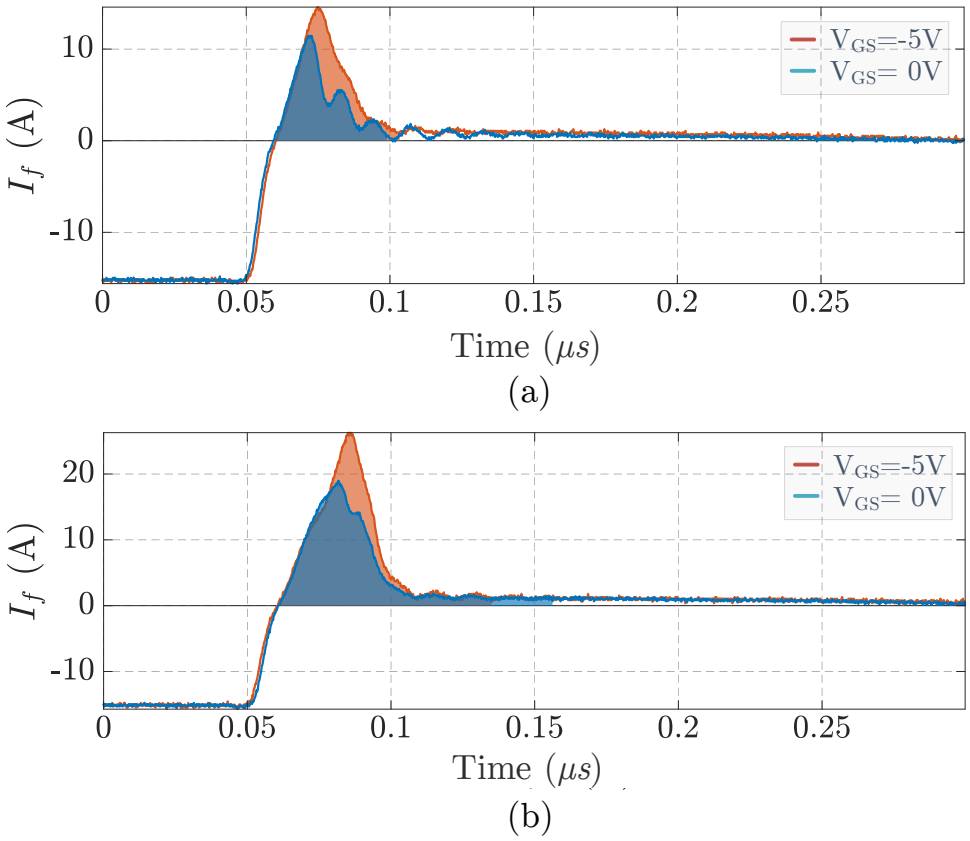


Figure 6.27. Calculation of reverse recovery charge based on JEDEC24-10 (a) for the planar SiC MOSFET (b) for the trench SiC MOSFET.

current reaches the desired value, the top side switch is turned off, and the freewheeling current conducts through the DUT body diode. When the high side switch turns on again, a large recovery current flows through the body diode in the reverse direction.

Table 6.1. Calculated body diode reverse recovery values for the planar SiC MOSFET

V_{GS} (V)	Q_{rr} (nC)	t_{rr} (ns)	I_{rr_max} (A)	di/dt (A/ns)	dv/dt (V/ns)	%
0	182.4	31.3	11.4	1.1	29.4	35.69%
-5	283.7	34.8	14.6	1.2	31.2	

The reverse recovery test waveforms for the planar and trench SiC MOSFET are shown in Fig. 6.25 and in Fig. 6.26, respectively. As it can be seen from the waveforms, both DUTs

Table 6.2. Calculated body diode reverse recovery values for the trench SiC MOSFET

V_{GS} (V)	Q_{rr} (nC)	t_{rr} (ns)	I_{rr_max} (A)	di/dt (A/ns)	dv/dt (V/ns)	%
0	493.8	41.4	18.9	1.2	30.8	17.17%
-5	596.2	41.1	26.3	1.1	37.7	

has a higher peak reverse recovery current (I_{rrm}) at V_{GS}=-5V compared to V_{GS}=0V. This is due to MOS channel conduction when V_{GS}=0V, which decreases the current conduction through the PiN diode.

The reverse recovery values can be calculated based on JEDEC24-10 [60] standard. The reverse recovery charge Q_{rr} is calculated as the area under I_{DS} which is shown in Fig. 6.27 for both devices. As it can be seen, Q_{rr} is higher at V_{GS}=-5V compared to V_{GS}=0V. The calculated reverse recovery values are given in Table 6.1 for the planar SiC MOSFET and in Table 6.2 for the trench SiC MOSFET. For both devices, reverse recovery charge (Q_{rr}), the peak reverse recovery current (I_{rrm}), and reverse recovery time (t_{rr}) has decreased at V_{GS}=0V compared to the values at V_{GS}=-5V.

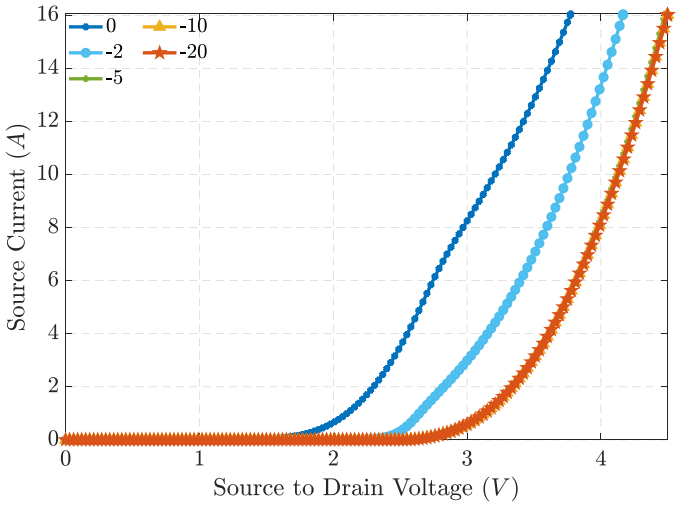


Figure 6.28. Measured body diode characteristics of the planar SiC MOSFET as a function of gate bias.

The Q_{rr} value has decreased by 35.69% percent for the planar MOSFET, while it only changed 17.17% for the trench MOSFET. This difference is probably due to MOS channel current conduction through the channel in the trench MOSFET at V_{GS}=-5V while the channel is off in the planar MOSFET. In order to verify this, the current sharing proportion between the MOS channel and the PiN diode should be calculated for V_{GS}=0 for both MOSFETs. The following method is proposed for this calculation.

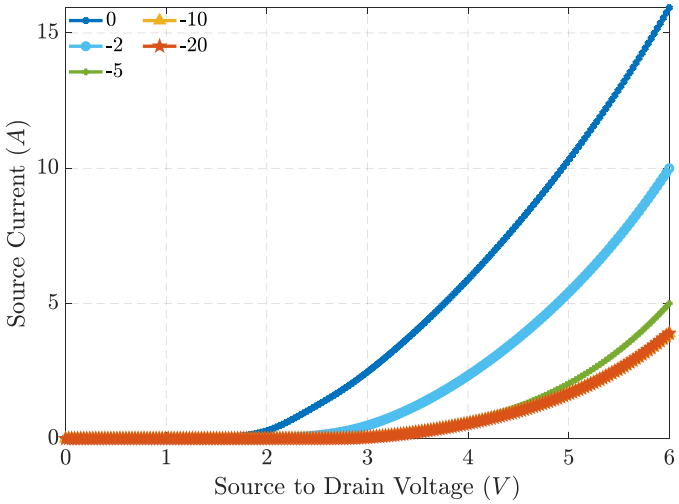


Figure 6.29. Measured body diode characteristics of the trench SiC MOSFET as a function of gate bias.

First, the body diode characteristics (I_{SD}-V_{SD}) of both MOSFETs are measured with Keysight B1506A curve tracer at different negative gate bias voltages by ensuring to have at least one measurement at V_{GS}=0 and another measurement at the lowest maximum gate voltage level. The reason behind the requirement of I_{SD}-V_{SD} measurement at the lowest maximum gate voltage level is ensuring the channel blockage. In this study, V_{GS}=-20V is used as the lowest maximum gate voltage, although it does not provide any additional channel blockage compared to V_{GS}=-10V. The I_{SD}-V_{SD} measurements at various gate bias values is given in Fig. 6.28 for the planar SiC MOSFET and Fig. 6.29 for the trench SiC MOSFET.

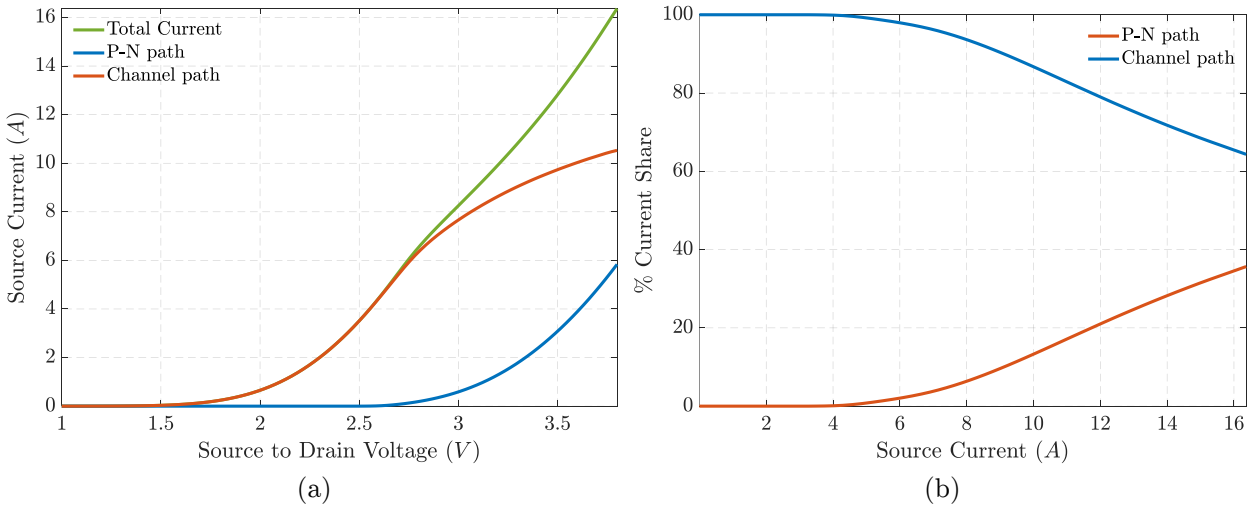


Figure 6.30. Calculated current sharing values between the MOS channel path and the PIN path at V_{GS}=0 for the planar SiC MOSFET (a) absolute values (b) percent.

From the I_{SD}-V_{SD} curve at V_{GS}=0V, the V_{SD} voltage drop for I_F=15A can be found. Then the PiN diode current (I_{PiN}) conduction at that V_{SD} voltage drop can be calculated from the I_{SD}-V_{SD} curve at V_{GS}=-20V. Then when we subtract I_{PiN} from the total current of I_F=15A, we can find the MOS channel current (I_{MOS}) portion of the total current. The calculated current sharing values between the MOS channel path and the PIN path at V_{GS}=0V and I_F= 15A is given in Table 6.3.

Table 6.3. Calculated current sharing values between the MOS channel path and the PIN path at V_{GS}=0V and I_F= 15A

Type (V)	I_{MOS} (A)	I_{PiN} (A)	I_{MOS} %	I_{PiN} %
Planar SiC MOSFET	10.27	4.73	68.5%	31.5%
Trench SiC MOSFET	11.54	3.46	76.9%	23.1%

If this calculation method is applied across the drain current range, current sharing values between the MOS channel path and the PIN path can be calculated, as shown in Fig. 6.30 for the planar SiC MOSFET and Fig. 6.31 for the trench SiC MOSFET.

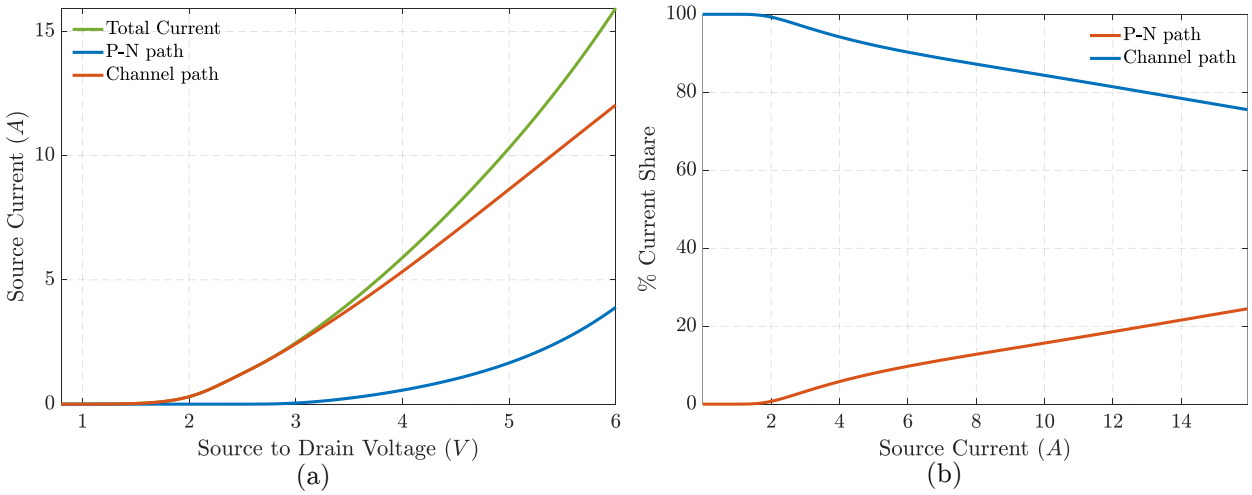


Figure 6.31. Calculated current sharing values between the MOS channel path and the PIN path at V_{GS}=0 for the trench SiC MOSFET (a) absolute values (b) percent.

CHAPTER 7

AN INVESTIGATION ON DIAGNOSIS BASED POWER SWITCH LIFETIME EXTENSION STRATEGIES FOR THREE-PHASE INVERTERS

In this chapter a hybrid secondary lifetime extension control scheme is proposed for three-phase inverters based on the identified failure precursors which dynamically changes the modulation scheme and adjusts the switching frequency. The tradeoff between the THD and achievable lifetime extension is addressed, and a control algorithm is proposed which maximizes the lifetime with feasible lowest THD. Although a Si IGBT module -not SiC MOSFET- is used as a medium to demonstrate the lifetime extension strategy, this chapter aims to provide a framework which could easily be applied on SiC power MOSFETs as well [61].

7.1 Introduction

Due to the increasing trends in high power density designs and high temperature operations, reliability of power electronics systems is becoming more critical in various applications such as automotive, oil and gas, solar energy applications [62]. It is well studied in the industry surveys that in power electronic systems, the electrolytic bus capacitors and the power semiconductor devices are the components most susceptible to failures, and hence, key limiting factor for overall system lifetime and reliability [63]. Power devices deployed in power electronics converters can undergo both mechanical and environmental stresses which cause wear out over time and induce failure [40]. Among these, high junction temperature and large thermal fluctuations caused by power cycling are the major contributors to package related failures [64, 65, 66]. For instance, the temperature swing amplitude can go up to 80°C in traction drives and wind power applications, which significantly reduces the reliability of power devices [63, 67]. Due to the number of failures reported by industry, exhaustive

research has been devoted to identifying the thermal stress related failure mechanisms [66, 67, 68].

Thermal cycles related failures occur due to the mismatch of thermal expansion coefficients (CTE) between different layers of the semiconductor. In case of frequent recurrence of thermal cycles, thermomechanical fatigue occurs between the adjacent layers, which further leads to degradation of solder joints and bond wire lift-offs [8]. These aging effects caused by the thermal stress have been replicated and assessed on custom built accelerated aging test-beds [67, 68, 69, 70, 71, 34]. In power modules with direct-bond-copper (DBC) layer, power cycling related high frequency temperature fluctuations are found to be leading to bond-wire failures, while low frequency thermal cycles induce solder joint related issues [72]. For discrete power devices, thermomechanical stress is mainly observed at the die solder attachment as cracks or delamination [70, 34].

The packaging related degradation typically causes variations in the physical parameters of the devices. The die attach solder degradation gradually increases the thermal impedance as well as electrical resistance of the device, which can be observed through the variation of on-state resistance in power MOSFETs and collector-emitter voltage (V_{ce}) in IGBTs. Similarly, when a bond-wire lifts off in a power module, a remarkable jump is observed in the collector-emitter voltage of an IGBT module [66, 73, 74, 75]. By tracking the changes in the physical parameters, the degradation of a power device can be detected during operation and a failure criterion can be defined for end of lifetime (EOL) condition. For IGBT power modules, a 5% increase in V_{ce} or a 20% increase in thermal resistance (R_{th}) is accepted as a common failure criterion [76]. Thermal impedance, gate threshold voltage, and switching transition times are other parameters broadly used as indicators for die and package degradation [40, 41]. When the failure mechanism is die attach solder degradation, the on-state resistance of a discrete power MOSFET increases following a specific pattern [33]. An experimental data of the on-state resistance variation with respect to thermal aging presented

in the literature is given as an example in Fig. 7.1 [34]. It has been found that the on-state resistances of the switches initially increase exponentially to a certain value, and then suddenly jump to higher unstable levels [70, 33]. Once the tracked parameter reaches to and exceeds predefined threshold, an early warning signal can be flagged for further actions to extend the useful lifetime.

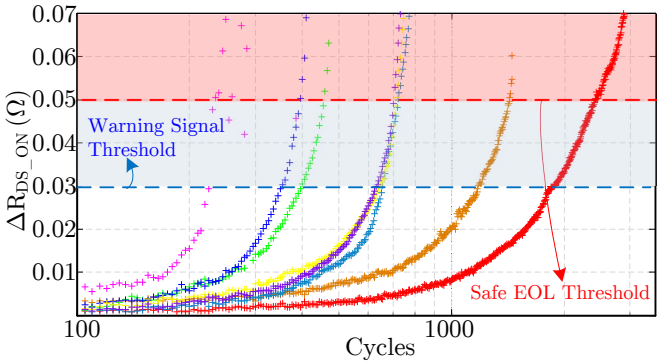


Figure 7.1. ΔR_{ds_on} variation of thermally aged power MOSFETs in the exponential region.

In the literature, there are several studies focusing on developing more reliable or fault tolerant systems [77]. The simplest way to increase the reliability is hardware redundancy which includes switch-level, leg-level or module-level redundancy, yet additional hardware increases the system size and cost [78, 79]. A more effective approach to increase the lifetime of power devices is through reducing the average junction temperature and/or the temperature fluctuation on the devices, which are the main reasons for thermo-mechanical aging related failures [79, 80, 81]. Majority of the work done on life extension strategies rely on controlling the junction temperature that prevents the maximum junction temperature to exceed maximum continuous temperature limit defined by the manufacturer, which can cause a sudden failure [82, 83, 84, 85, 86]. The junction temperature of semiconductor devices can be controlled by adding an advanced cooling system or by active control of cooling system [87, 88]. However, the extra cooling components increase the system cost and volume and also bring additional complexity to the system. Another method for limiting the maximum

junction temperature relies on modifying the control variable with a fuzzy controller and derating of the output power [89]. However, in this strategy, the power converter may not be operated at its full scale power which jeopardizes the system performance. In [89, 90, 91], the switching frequency reduction technique is employed to keep the junction temperature at safe level during the start-up process of an AC machine till synchronization is achieved.

Other lifetime extension strategies mainly focus on reducing the junction temperature fluctuation. In [92], the switching frequency is increased at low load conditions in order to increase the power losses and prevent the devices to cool down. The major drawback of this solution is elevated average junction temperature, which will aggravate the lifetime, and significantly reduce the efficiency. In [93], the switching frequency is decreased at high wind speeds for extending the lifetime of the wind power converter, while in [94], the switching frequency is altered in both directions using hysteresis control.

Most of these studies aim either to keep the junction temperature under control or to reduce only the large temperature fluctuation during short-term load variations or during the low frequency operation. Although the large temperature fluctuations cause the most damage, preventing large fluctuations does not save the switch from deformations. According to [95], any thermal cycle with amplitudes higher than 3°C will affect the lifetime of the switch due to frequent recurrence. Moreover, even though decreasing the switching frequency technique offers high potential for lifetime extension, it cannot be employed without incurring power quality degradation (i.e., output current harmonics). Therefore, utilizing these strategies throughout the lifetime of the converter may not be the optimal solution for critical applications. However, in order to prevent a costly shutdown or possibly a catastrophic failure, the state of device health can be monitored by tracking the variations in the failure precursors. Since the critical level of monitored failure precursor depends on the device technology, packaging and application, a specific critical limit should be determined by the user in order to trigger a warning signal. Once the warning signal showing device deterioration is issued, a secondary control algorithm can be initiated and lifetime of the converter

can be extended by changing the modulation scheme/switching frequency at the expense of higher THD. By doing this, the thermal stress on the degraded switches can be reduced and the power converter can survive until the next scheduled maintenance. However, there are not enough studies focusing on incipient fault detection and diagnosis based power switch lifetime extension. Also, the effects of lifetime extension strategies on the power quality have not been explored thoroughly in the literature.

In this chapter, a diagnosis based active lifetime extension strategy which combines switching frequency adjustment and PWM modulation scheme selection is proposed for three-phase inverters. When the measured failure precursor reaches to the predetermined threshold value, the thermal stress or, in other words, power dissipation on the degraded switches are reduced by either 1) decreasing the switching frequency, 2) changing the zero-vector placement. The effects of modulation and switching frequency adjustment on the harmonic distortion factor as well as on the lifetime of converter are investigated.

This chapter is organized as follows: Section 7.2 explains the principles of modulation techniques and their effects on switching losses and harmonic distortion. Section 7.3 provides the details of lifetime extension strategy together with accurate junction temperature estimation and remaining useful lifetime (RUL) calculations. Simulation results are presented in Section 7.4. The experimental validation of the proposed strategy is given in Section 7.5. The conclusions are summarized in Section 7.6.

7.2 Analysis of Modulation Techniques

In advanced adjustable speed drive inverters, the PWM modulation controller applies more than one type of modulation scheme according to the modulation index to achieve optimal efficiency, THD and accurate current measurement through shunt resistors. On the other hand, switching frequency is usually optimized considering the harmonic distortion, switching losses, device switching characteristics, EMI filters, etc. at the design stage and remains

constant throughout the operation. In this section, the principles of modulation techniques, corresponding switching losses and harmonic distortion are explained.

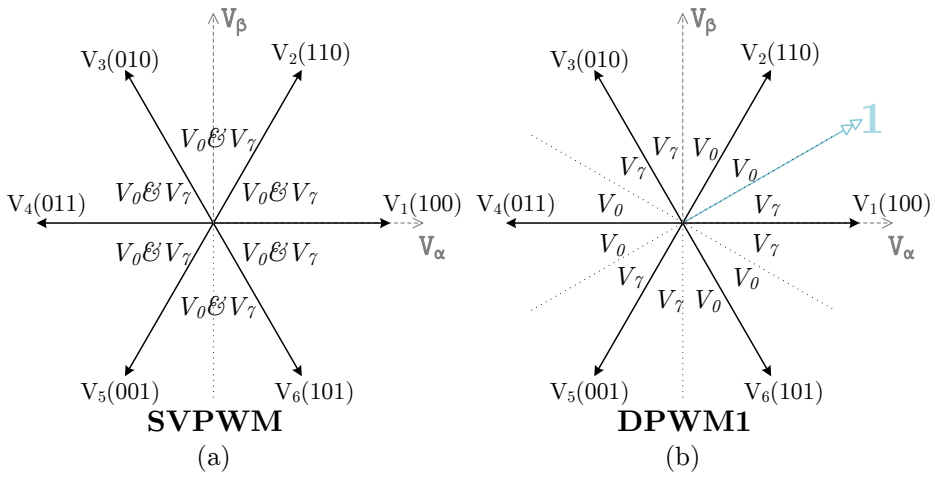


Figure 7.2. Zero-vector placement in SVPWM, DPWM0 and DPWM1 modulation schemes.

7.2.1 Continuous and Discontinuous Modulation Techniques

In SVPWM, two active vectors and two zero vectors are used to synthesize the reference voltage vector in each sector. The time durations of zero vectors $V_0(000)$ and $V_7(111)$ are equally distributed in each switching period as shown in Fig. 7.2(a). This distribution provides a better current waveform under low modulation indexes; however, exhibits higher switching losses. To reduce the switching losses and improve the current waveform quality, the modulation scheme is typically switched to DPWM at higher modulation indexes. In DPWM schemes, only one zero vector is used in every 60° sectors. The placement of zero vectors leads to various different DPWMs. For instance, DPWM0 uses V_0 vector at the first defined sector. 30° shift in the defined sectors results in DPWM1 strategy (Fig. 7.2(b)), where the upper leg switches are clamped to 1 when the leg voltages are highest, and clamped to 0 when they are lowest. By using one zero vector, the voltage reference of one phase is clamped to positive or negative dc-link potential for certain interval and the corresponding

power device keeps its status without switching. This eliminates the switching losses for the device in this period and therefore the average power loss of the device decreases.

7.2.2 Switching Loss Comparison

Switching loss is the major loss component that rise the junction temperature of a power devices. It is proportional to the dc bus voltage and instantaneous load current, and it can be calculated by taking the average over a line cycle. In SVPWM, the switching loss of a switch over one half of a fundamental cycle is expressed as [96]

$$P_{SVPWM}\left(V_{dc}, I_M\right) = \frac{2V_{dc}I_M}{\pi} \tag{7.1}$$

For comparison with switching losses that in DPWM, a switching loss factor (SLF) is defined.

$$SLF = \frac{P_{DPWM}\left(V_{dc}, I_M, \varphi\right)}{P_{SVPWM}\left(V_{dc}, I_M\right)} \tag{7.2}$$

where φ denotes the load angle. For DPWM techniques, the switching loss is a function of load angle as the switches are clamped to "0" or "1" during a 60° interval, in which switching losses become zero. This suggests that DPWM1 provides minimum switching loss when load angle is 0°. Likewise, DPWM0 and DPWM2 provide optimum loss reduction when load angle is -30° and +30°, respectively. Eliminating switching losses for 60° interval introduces a boundary to the integral of loss calculation. The generalized formula for calculating the SLF is expressed as [97, 96].

$$SLF_{DPWM} = \begin{cases} \dfrac{\sqrt{3}}{2}\cos\left(\dfrac{4\pi}{3} + \psi - \varphi\right), & -\dfrac{\pi}{2} \le \varphi \le -\dfrac{\pi}{2} + \psi \\ 1 - \dfrac{1}{2}\sin\left(\dfrac{\pi}{3} + \psi - \varphi\right), & -\dfrac{\pi}{2} + \psi \le \varphi \le \dfrac{\pi}{6} + \psi \\ \dfrac{\sqrt{3}}{2}\cos\left(\dfrac{\pi}{3} + \psi - \varphi\right), & \dfrac{\pi}{6} + \psi \le \varphi \le \dfrac{\pi}{2} \end{cases} \tag{7.3}$$

The SLF function is plotted in Fig. 7.3. As proposed in [98], the 60° clamping interval can be shifted with respect to load angle within -30° and +30° to achieve minimum switching losses.

This method is called as generalized DPWM and denoted as GPWM in Fig. 7.3. Thus, it is assumed that DPWM switching losses are half of that in SVPWM for the same switching frequency operation for a wide load angle operation range. This figure of merit suggests that theoretically the switching frequency in DPWM can be increased to twice of that in SVPWM for the same overall switching losses. However, it should be noted that the instantaneous power loss increases the device junction temperature, which in turn impacts the turn-on and turn-off characteristics and changes the switching energy losses. The junction temperature effect on the switching losses is neglected in (7.1) and (7.2).

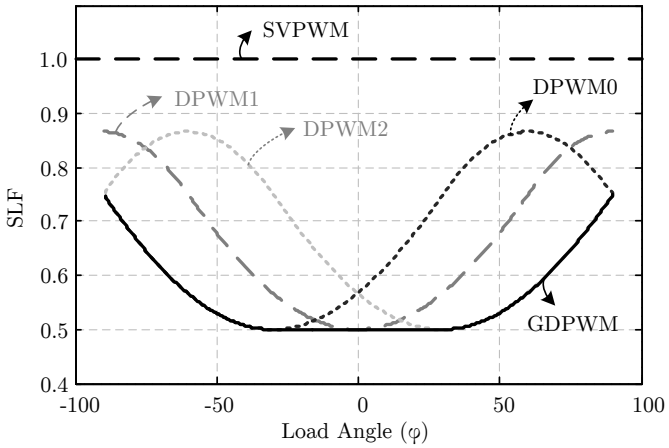


Figure 7.3. SLF plot for SVPWM and DPWM at different load angles.

7.2.3 Harmonic Distortion Comparison

The major harmonics in a balanced three-phase inverter are typically observed around the switching frequency. The harmonic distortion can be found by analyzing the ripple current within a switching cycle as in [96]. The switching harmonics are a function of applied dc bus voltage, load impedance, frequency and modulation index. Considering that the load is inductive, and inverter operates under the same dc bus voltage, a harmonic distortion factor (HDF) that can be used to compare the harmonic distortions of SVPWM and DPWM can

be defined. In SVPWM technique, the integration over the positive cycle results in [97, 96]

$$HDF_{SVPWM}(f_s,M)=\frac{1}{{f_s}^2}\left(\begin{array}{l}\frac{3}{2}\left(\frac{\pi M}{4}\right)^2-\frac{4\sqrt{3}}{\pi}\left(\frac{\pi M}{4}\right)^3\\+\frac{9}{8}\left(\frac{3}{2}-\frac{9\sqrt{3}}{8\pi}\right)\left(\frac{\pi M}{4}\right)^4\end{array}\right) \tag{7.4}$$

Likewise, the HDF for DPWM techniques are found as [97, 96]

$$HDF_{DPWM1}\left(f_s,M\right)=\frac{1}{{f_s}^2}\left(\begin{array}{l}6\left(\frac{\pi M}{4}\right)^2-\left(\frac{45}{2\pi}+\frac{4\sqrt{3}}{\pi}\right)\left(\frac{\pi M}{4}\right)^3\\+\left(\frac{27}{8}+\frac{27\sqrt{3}}{32\pi}\right)\left(\frac{\pi M}{4}\right)^4\end{array}\right) \tag{7.5}$$

$$HDF_{DPWM0,2}\left(f_s,M\right)=\frac{1}{{f_s}^2}\left(\begin{array}{l}6\left(\frac{\pi M}{4}\right)^2-\left(\frac{35\sqrt{3}}{2\pi}\right)\left(\frac{\pi M}{4}\right)^3\\+\left(\frac{27}{8}+\frac{81\sqrt{3}}{64\pi}\right)\left(\frac{\pi M}{4}\right)^4\end{array}\right) \tag{7.6}$$

HDF is plotted in Fig. 7.4 according to the modulation index for SVPWM and DPWM. As it can be observed from the plots, there is no significant difference in terms of harmonic distortion in between DPWM methods, particularly when $0 \leq M \leq 0.4$. In case generalized DPWM method is used, HDF plot would stand in between the curves of DPWM1 and DPWM0,2; thus, the comparison will be made according to DPWM1 herein after.

With respect to above discussion on the switching losses, the HDF of DPWM when switching frequency is increased to twice of that in SVPWM is also plotted in Fig. 7.4 for a fair comparison. As it can be seen in Fig. 7.4, SVPWM performs superior in terms of harmonic distortion for the same switching frequency. When the switching frequency in DPWM is increased to twice in the SVPWM, the HDF of DPWM becomes better in whole modulation range, while the switching losses remain the same as of SVPWM. The HDF

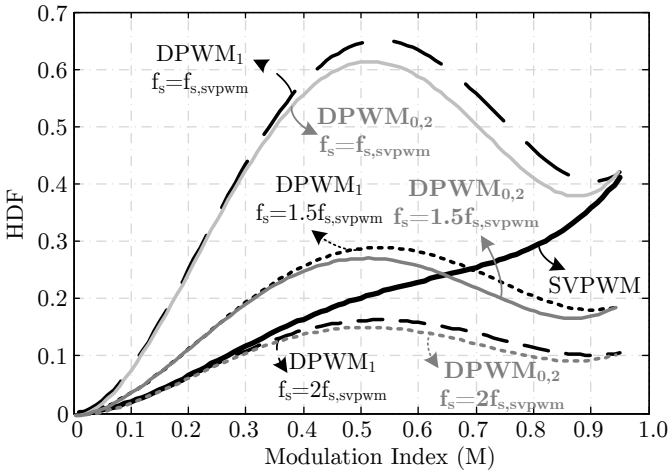


Figure 7.4. HDF plot for SVPWM and DPWM modulation schemes at different modulation indexes.

surfaces with respect to modulation index and switching frequencies have been plotted in Fig. 7.5(a) and Fig. 7.5(b) for SVPWM and DPWM1, respectively.

The optimal HDF surface can be defined when switching frequency of SVPWM is kept at 1pu and DPWM1 is swept from 1pu to 2pu, as shown in Fig. 7.6. It should be noted that there is no switching frequency limitation in this surface within the defined limits. However, in typical power converters both the lower and upper limits of switching frequency are set considering the power losses, EMI filters, audible noise level and switching capability of the device and so on. Thus, it is not always viable to increase the switching frequency to 2pu. As seen from Fig. 7.4 and Fig. 7.6, SVPWM provides better current waveform quality and is preferable at modulation indexes less than 0.65 when the upper switching frequency is limited to 1.5pu.

7.3 Thermal Stress and Lifetime Calculations

It is a challenging task to calculate the exact lifetime of a power semiconductor device due to variation of load profile and distinctness of each semiconductor device. Nevertheless, earlier studies [82, 83, 84] have shown a reasonable correlation between device lifetime and junction

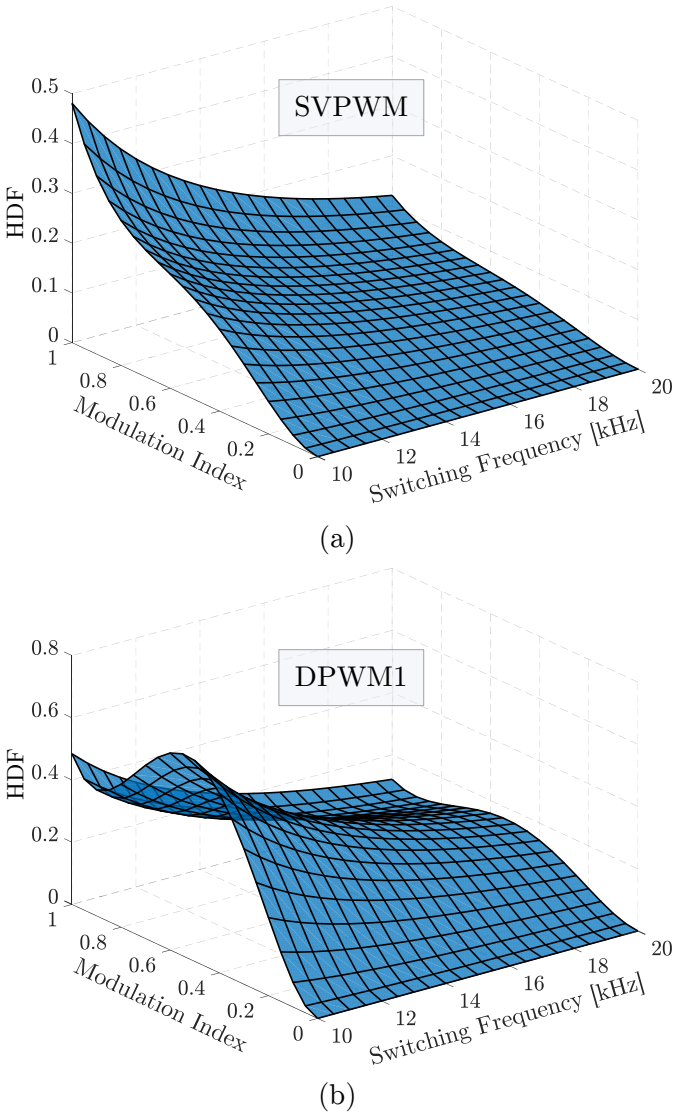


Figure 7.5. HDF surfaces at different modulation indexes and switching frequencies; (a) SVPWM and (b) DPWM.

temperature variation, which is determined by power losses and thermal dissipation capability the device. Therefore, in order to find the relation between the junction temperature and power loss distribution, the instantaneous power loss and their impact on the junction temperature need to be analyzed.

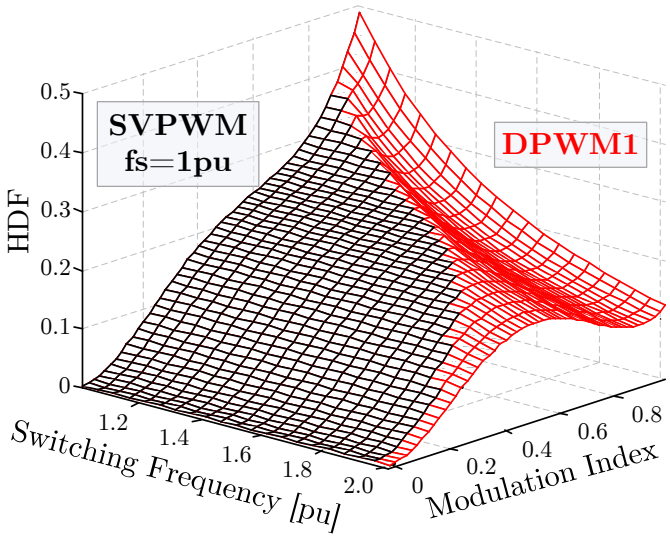


Figure 7.6. Optimal HDF surface when $fs_{SVPWM} = 1pu$ and $1pu \leq fs_{DPWM1} \leq 2pu$.

7.3.1 Power Loss and Junction Temperature Calculations

An accurate real-time calculation of the junction temperature is vital for quantifying the lifetime of the devices correctly. In the literature, datasheet based loss calculation methods are widely used for calculating the power losses on the power semiconductor [99]. However, this method uses static thermal calculation and assumes the junction temperature remains constant within one sinusoidal period. Moreover, the switches are assumed to have an ideal cooling with a constant heat sink temperature, which does not reflect the real application conditions. In reality, the heat dissipation depends on design and thermal impedance, and hence the heat sink does not necessarily have a constant temperature. In this study, dynamic variation of junction temperature is calculated with updated heat sink temperature values. To do this, thermal equivalent circuit diagrams are utilized and three-dimensional structures are mapped into one-dimensional models . In order to simplify the calculations, the thermal impedances are commonly represented with a Foster thermal network [100]. However, the elements of Foster networks cannot be assigned to physical components or combined with different heat sink models to represent the thermal impedance of the entire system. In order

Table 7.1. Cauer Network Parametes

Segment	1	2	3	4
R ($^{\circ}C/W$)	1.053608	1.259346	0.509136	0.132584
C ($J/^{\circ}C$)	0.008819	0.043133	0.305389	9.904288

to calculate the dynamic temperatures correctly, Cauer network equivalent circuit is used which is shown in Fig. 7.7.

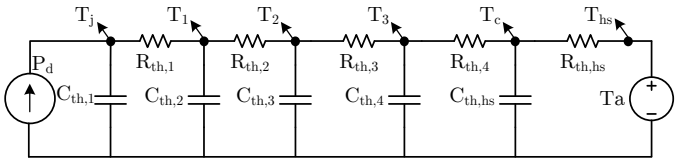


Figure 7.7. Cauer thermal model of power switch.

In this study, an IPM power module with 600V blocking voltage and 20A nominal current is used [101]. Since the thermal network parameters are not provided by the manufacturer, first, the Foster thermal network coefficients of the switch are found by curve fitting method from provided thermal response of the module. Then, a circuit transformation method given in [99] is utilized to obtain the equivalent Cauer network. The calculated parameters of the Cauer network thermal equivalent circuit are given in Table 7.1.

Once the thermal equivalent circuit is obtained, the junction temperature can be estimated by the following equation.

$$T_J = P_{loss} Z_{th} + T_c \tag{7.7}$$

where, Z_{th} is the thermal impedance, and T_c is the case temperature. The power losses include IGBT and diode losses; however, in order to decrease the computational burden, the diode power losses are neglected. Considering only the IGBT losses, the total power loss of each switch (P_{loss}) is calculated by adding conduction losses and switching losses as follows,

$$P_{loss} = P_{cond\_avg} + \frac{(E_{on} + E_{off}) . f_{sw}}{\pi} \tag{7.8}$$

where, P_{cond_avg} and f_s represent the average conduction loss and switching frequency respectively; E_{on} and E_{off} denote the switching energies during turning on and off instants. The average conduction losses under SVPWM modulation technique can be calculated as [102]

$$P_{cond\_avg} = \frac{1}{\sqrt{3}}\left(U_{ce0}(T_j)\frac{I_m}{\pi} + r(T_j)\frac{I_m^2}{4}\right) + M\cos(\varphi)\left(U_{ce0}(T_j)\frac{I_m}{8} + r(T_j)\frac{I_m^2}{3\pi}\right) \quad (7.9)$$

where, $U_{ce0}(Tj)$, $r(Tj)$ denote temperature dependent threshold voltage and bulk resistance, respectively. These parameters can be obtained by curve fitting the saturation voltage characteristic which is given in Fig. 7.8. The switching energies can be found for each turn-on and turn-off switching events as follows [100]

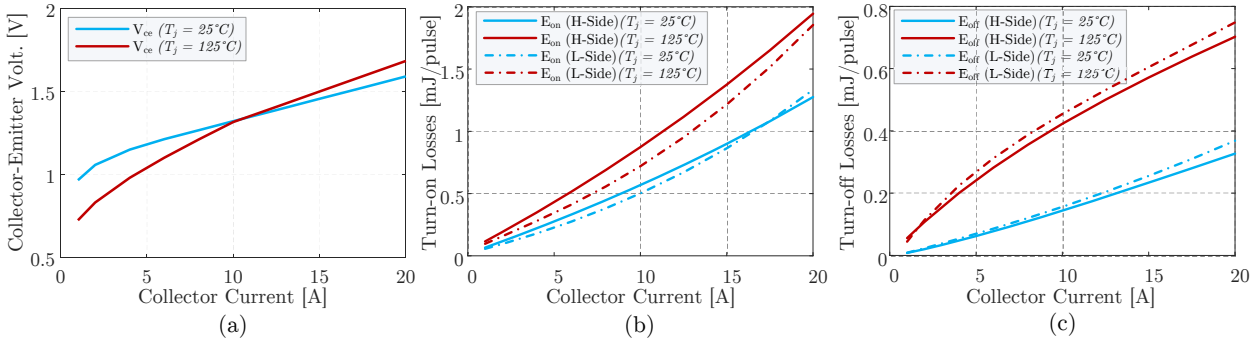


Figure 7.8. Power loss graphs depending on collector current (a) Conduction loss (b) Turn-on loss (c) Turn-off loss.

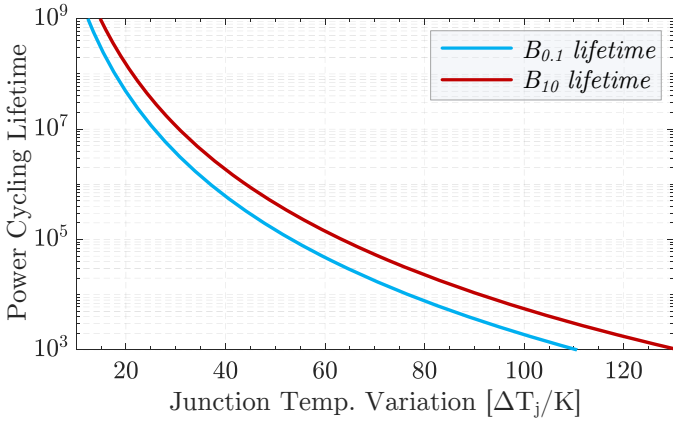


Figure 7.9. Power cycling lifetime curves of the utilized IPM.

$$E_{sw} = E_{sw(T_j=25)} \left(\frac{I_m}{I_{ref}} \right)^{Ki} \left(\frac{V_{dc}}{V_{ref}} \right)^{Kv} \times (1 + TC_{sw}(T_j - 25)) \tag{7.10}$$

where, V_{ref} and I_{ref} are the voltage and current at the given test points, for which switching energies are provided. K_i and K_v are the exponents for the current and the voltage dependency of switching losses, respectively. TC_{sw} is temperature coefficient of switching losses and can be found as

$$TC_{sw} = \frac{E_{sw(T_j=125)} - E_{sw(T_j=25)}}{E_{sw(T_j=25)}.\,(125 - 25)} \tag{7.11}$$

As it can be seen from (7.8)-(7.11), all power losses are a function of T_j. Thus, the average junction temperature needs to be calculated by iteratively solving (7.7) to (7.10) until T_j and T_c are stable and thermal stability is achieved. In order to solve the equations, T_j and T_c are considered the same as room temperature during the first iteration. The conduction and switching losses are computed utilizing the conduction and switching energy loss graphs that are provided in datasheet. Fig. 7.8 shows all the power loss graphs for IGBT module used in analysis for this study. While thermal resistance, R_{th}, can be used for average junction temperature calculation, dynamic junction temperature variation calculation requires thermal impedance (Z_{th}) information. Dynamic temperature variation can be obtained by solving equations derived from the Cauer model. The state-space model of the Cauer network is obtained as in (7.12).

$$\frac{d}{dt}\begin{bmatrix} T_j \\ T_1 \\ T_2 \\ T_3 \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_1C_1} & \frac{1}{R_1C_1} & 0 & 0 \\ \frac{1}{R_1C_2} & -\frac{R_1+R_2}{R_1R_2C_2} & \frac{1}{R_2C_2} & 0 \\ 0 & \frac{1}{R_2C_3} & -\frac{R_2+R_3}{R_2R_3C_3} & \frac{1}{R_3C_3} \\ 0 & 0 & \frac{1}{R_3C_4} & -\frac{R_3+R_4}{R_3R_4C_4} \end{bmatrix} . \begin{bmatrix} T_j \\ T_1 \\ T_2 \\ T_3 \end{bmatrix} + \begin{bmatrix} \frac{1}{C_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} .P_{loss} \tag{7.12}$$

For simplification, the model includes the thermal impedance from junction to case, where T_c is equal to the value from the latest iterative update. The dynamic switching and conduction power losses are calculated by averaging the instantaneous power losses over a switching cycle and then transforming it into an equivalent sinusoidal half wave. Then, the junction temperature fluctuation is obtained by finding the time response of (7.12) to the calculated of power dissipation.

7.3.2 Remaining Lifetime Calculation

As a common practice, semiconductor manufacturers provide a lifetime expectancy in terms of B_{10} or B_{01} lifetime graphs, which shows the number of cycles at which 10% and 0.1% of modules fails, respectively [10]. In this study, B_{10} lifetime provided by the manufacturer of the utilized IPM, given in Fig. 7.9, is used [103]. This power life cycle curve is obtained through power cycling the module and evaluating the number of cycles to failure (N_f) under different temperature swings (ΔT_j). The end of life (EOL) of a power device can be approximated by the well-known CoffinManson model, even though it has some shortcomings as it only considers ΔT_j and the mean temperature (T_m). Number of cycles to failure can be modeled as

$$N_f = \Delta T_j{}^{\delta} A e^{\frac{E_a}{kT_m}} \tag{7.13}$$

where k_B is the Boltzmann constant ($= 8.6173310^{-5} eV/K$), E_a is the activation energy and A and δ are the experimental coefficients. By curve approximation to B_{10} lifetime E_a, δ and A are found as $0.5eV$, -6.342 and 9.41810^7, respectively. The remaining useful lifetime (RUL) of the switches can be expressed as

$$RL = 1 - \sum_{1}^{n} \frac{N_n}{N_{EOL,n}}\bigg|_{\Delta Tj_n} \tag{7.14}$$

where N_n is the number of thermal cycles experienced by the switch and N_{EOL} is the expected number of cycles to failure at a given ΔT_j and T_m.

7.4 Lifetime Extension Strategy

Due to variations during production process, some of the switches may have higher power losses and thereby experience a larger stress. This fact suggests that some of the switches age slightly faster than others. With the recent findings on the failure precursors indicating package related wear-out, it is possible to monitor the health of the switches, which further enables new methods to enhance the reliability. Once one of the tracked failure precursors reaches to the critical threshold value, the device lifetime can be enhanced by engaging a secondary lifetime extension control strategy and reducing the power losses on that switch.

In order to increase the lifetime of the converter, modulation scheme manipulations and switching frequency variations are employed systematically. Unlike the conventional control algorithms, hybrid modulation controller proposed in this chapter determines the zero-vector placement and switching frequency according to the device degradation level. Both of these adjustments aim to reduce the power loss of the devices. Nevertheless, they are not preferable under normal operating conditions when the devices are classified as "healthy", as these adjustments deteriorate the current waveform and increases the harmonic distortion.

The selection between SVPWM and DPWM considering a feasible switching frequency range is essentially dependent on the harmonic distortion or harmonic losses limitation and the desired power loss reduction which has an exponential relation with the end-of-life (EOL) of the switches. In Fig. 7.10, the SLF of DPWM and HDF_{DPWM}/HDF_{SVPWM} are plotted with given frequency and HDF limitation planes. The figure illustrates an application with the following limitations; $HDF_{DPWM1} \leq 2 \cdot HDF_{SVPWM}$ and $1pu \leq fs_{DPWM1} \leq 1.5pu$. The SLF plot resembles the power loss that can be achieved and HDF_{DPWM}/HDF_{SVPWM} shows the increased HDF ratio compared to that of SVPWM. It is clear that higher switching frequency leads to lower HDF, while power losses decrease through the reduced switching frequency. Once the limitations are defined, the selection criterion is mostly dependent on the tradeoff between the desired level of reliability and increased THD. Depending on the

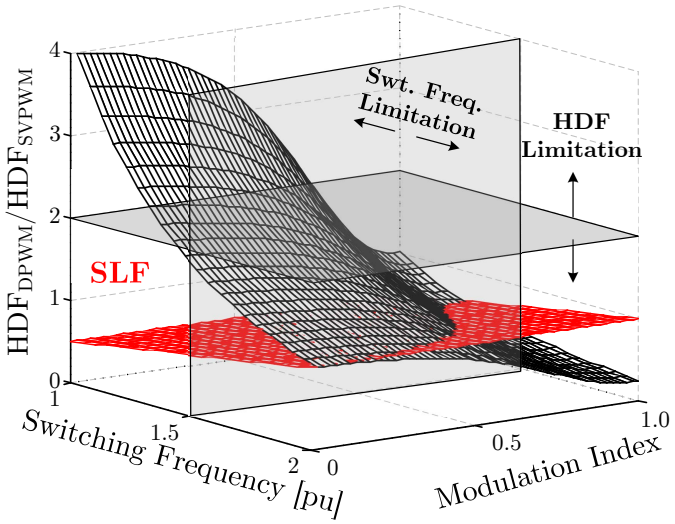


Figure 7.10. HDF and SLF surfaces of DWPM1 with respect to SVPWM under switching frequency and HDF limitations *i.e.* $HDF_{DPWM1} \leq 2 \cdot HDF_{SVPWM}$ and $1pu \leq fs_{DPWM1} \leq 1.5pu$.

power loss variation in time, the maximum value of the junction temperature is calculated by solving the thermal impedance equations. In case the losses follow a sinusoidal envelope, the junction temperature is estimated by solving (7.7)-(7.10) as a function of time. The maximum value of this function can then be found by taking the time derivative. In Fig. 7.11(a), average junction temperature graph is given with respect to the power level and switching frequency, while Fig. 7.11(b) presents the maximum temperature variation. Once the maximum junction temperature is calculated, the RUL of the switch can be calculated by (7.14). The calculated values of RUL are depicted in Fig. 7.11(c).

7.5 Simulation Results

The simulations are conducted in PLECS software which can combine electrical and thermal quantities. The parameters of the used three-phase converter is as follows; $L = 2mH$, $Po = 4500W$, $Vdc = 400V$, IGBT rating: $600V/20A$, Rth of the heat sink:$3.4W/K$, $T_{amb} =$ 25°C. The output power is intentionally selected high for the chosen switch type in order to highlight the junction temperature reduction with the proposed approaches.

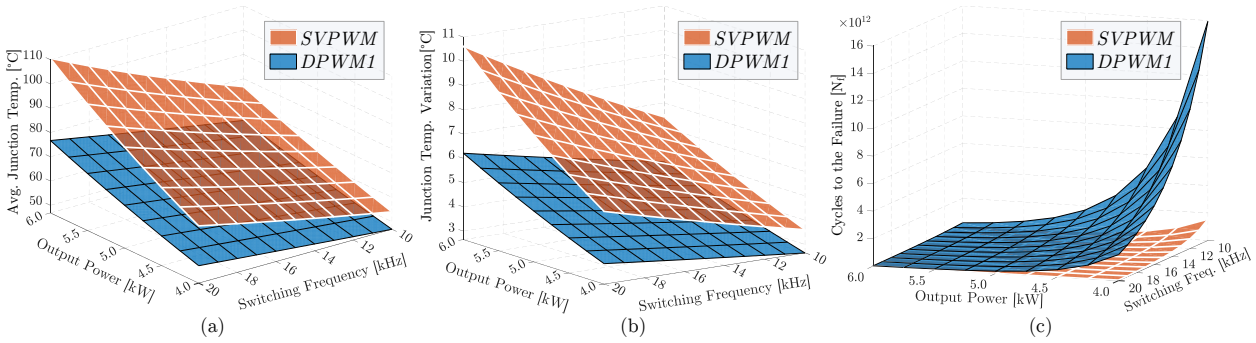


Figure 7.11. Calculations with respect to the power level and switching frequency (a) average junction temperature (b) maximum temperature variation (c) remaining useful lifetime.

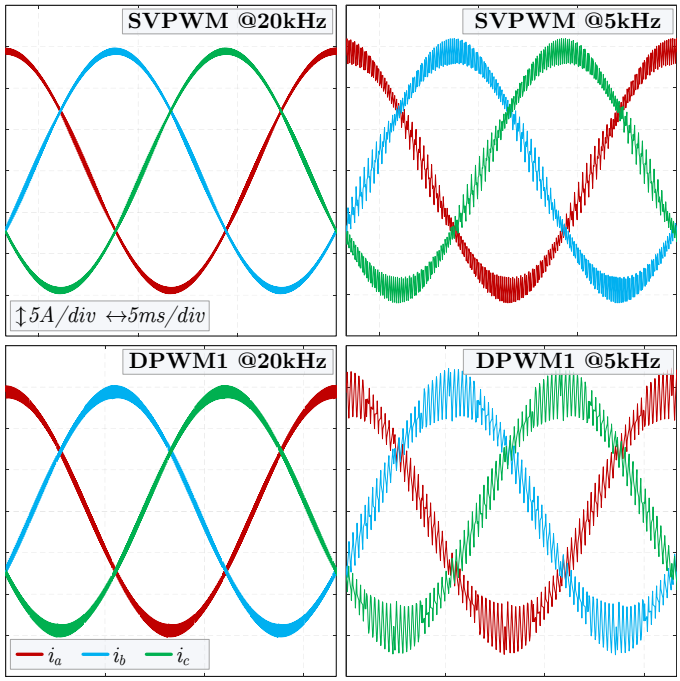


Figure 7.12. Current waveform at different switching frequencies under SVPWM and DPWM1 techniques.

In the first simulation, the switching frequency is reduced in each modulation technique to illustrate the current waveform distortion. As shown in Fig. 7.12, the worst current waveform is achieved when the converter is switched at 5 kHz under DWPM1 technique. In Fig. 7.13, the simulation results of modulation, phase currents, power losses, and junction temperatures are shown for SVPWM and DPWM1 at the same switching frequency. Basically, the power losses are continuous for the half period and proportional to load current in continuous

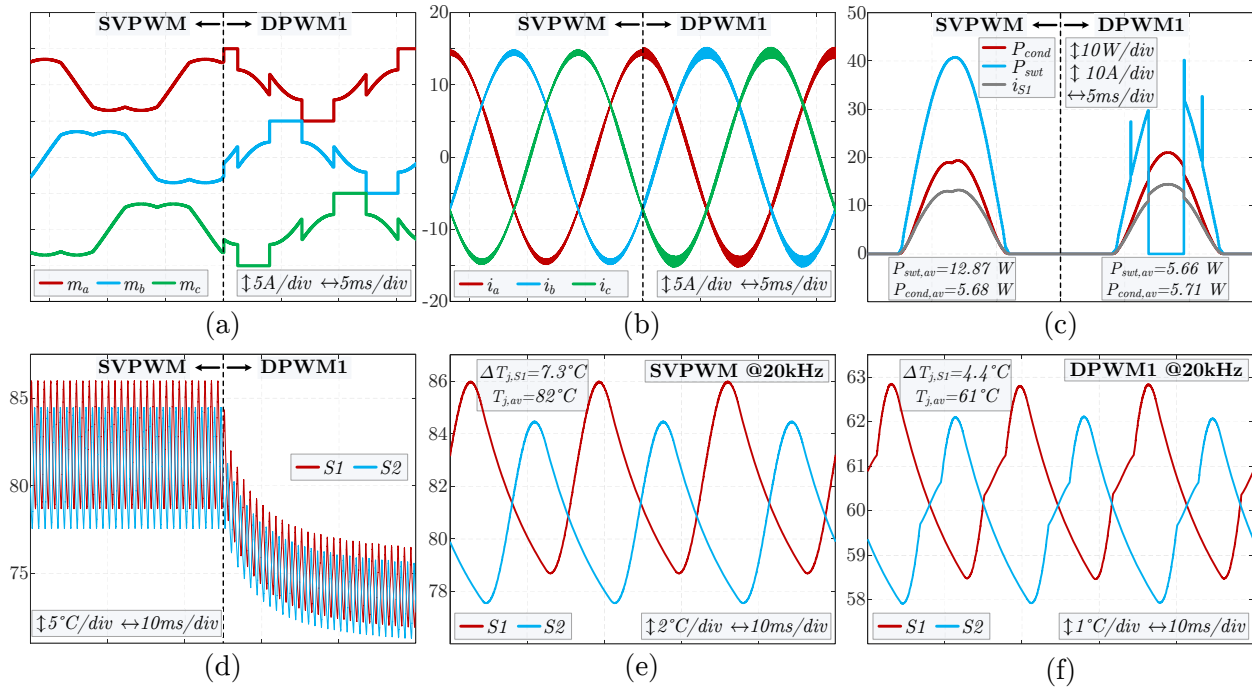


Figure 7.13. Simulation results of three-phase converter when modulation technique is switched from SVPWM to DPWM1; (a) modulation, (b) phase currents, (c) power losses, (d) junction temperatures, (e) zoom-in profile of junction temperatures in SVPWM at steady-state, (f) zoom-in profile of junction temperatures in DPWM1 at steady-state.

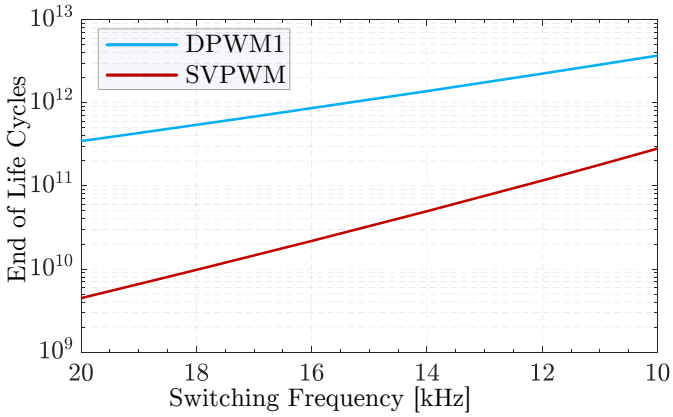


Figure 7.14. EOL results for SVPWM and DPWM1 under variable switching frequency.

PWM strategies, whereas switching losses are chopped when the phase current is maximum in DPWM. As a result of this, the switching losses decrease from 12.87W to 5.66W. The junction temperatures corresponding to each modulation strategies are shown at steady state

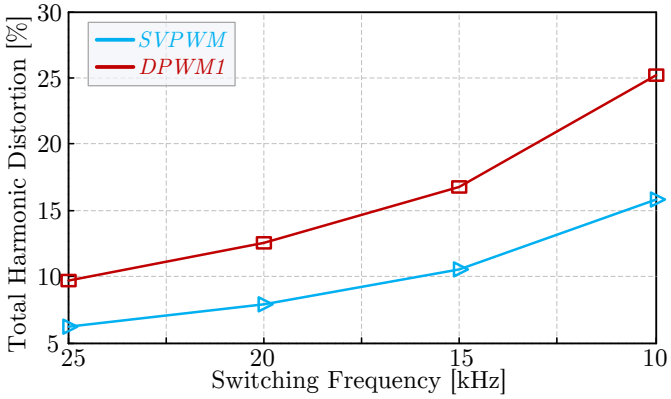


Figure 7.15. THD results for SVPWM and DPWM1 under variable switching frequency.

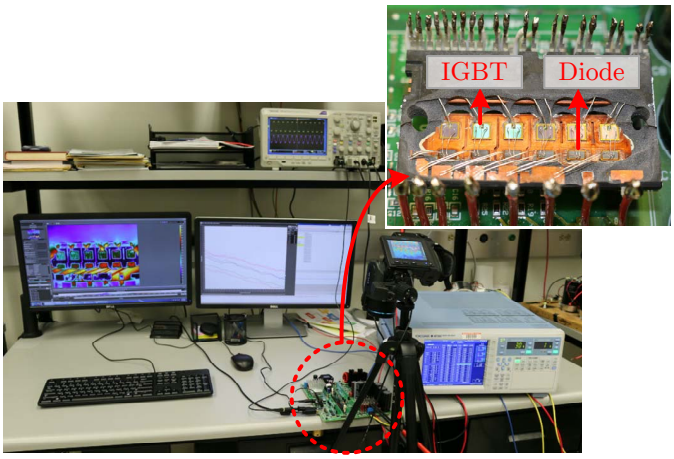


Figure 7.16. Experimental test setup.

in Fig. 7.13(e)-(f). The ΔT_j and T_m are equal to 7.3°C and 82°C, respectively, when SVPWM is used. On the other hand, the ΔT_j and T_m for DPWM1 are 4.4°C and 61°C, respectively. As it can be seen, the losses per switch and junction temperature significantly decrease at the expense of distorted current waveform as soon as DPWM1 is engaged.

Fig. 7.14 shows the end-of-life (EOL) of the switches and Fig. 7.15 presents the THD results with respect to the switching frequency for both modulation schemes. EOL curves are calculated offline from the junction temperature of the switches using Coffin-Manson model. These two curves are for the output power and modulation index used in the simulation.

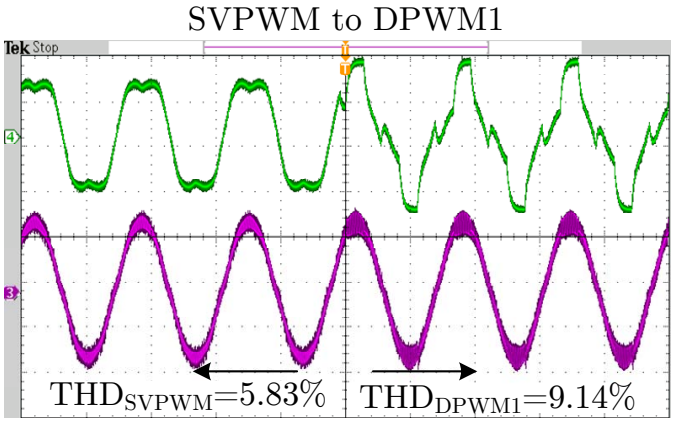
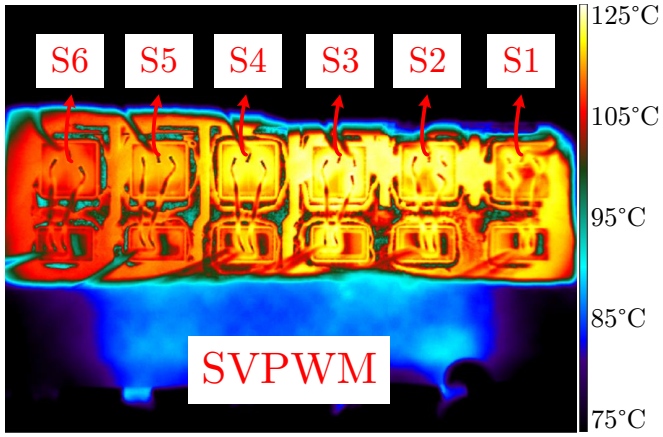


Figure 7.17. Experimental results of generated modulation signal and phase current when modulation scheme.

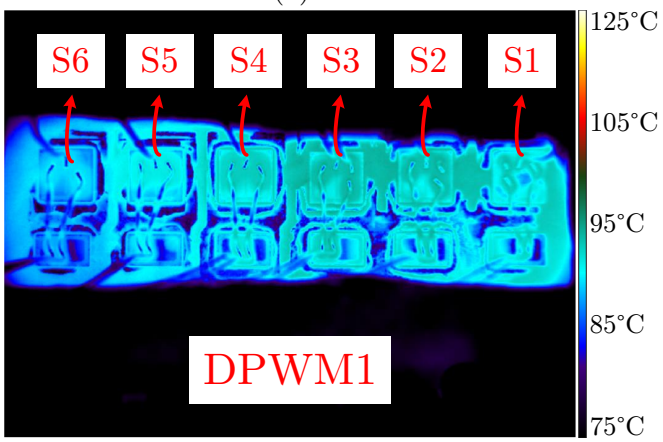
7.6 Experimental Verification

The proposed power lifetime extension strategies are implemented and verified experimentally on a two level inverter shown in Fig. 7.16. A three phase resistor bank is used in series with inductors as the load for the inverter. In order to measure temperature of each switch precisely, the power module of the kit is decapsulated and mounted as flipped. An IR thermal camera is utilized for capturing thermal variations of all switches during experimental tests. The control algorithm is implemented on a fixed point signal processing unit (*TMS320F28035*) by utilizing *IQ Math* library. The generated modulation signals are obtained from low pass filtered PWM signals and captured on a scope together with load current waveform. The harmonic measurements are realized with a power analyzer.

In order to verify the effectiveness of the proposed method first, the system is run with SVPWM at 10 kHz switching frequency, until the switch temperatures reaches to a steady level. Afterwards, it is assumed that one of the switches in a power module reaches to the critical threshold value and the modulation technique is switched from SVPWM to DPWM1 to decrease the thermal stresses over the switch. In Fig. 7.17, the experimental results of the generated modulation signals and phase current are given when the modulation technique is



(a)



(b)

Figure 7.18. IR thermal image of IGBT dies during (a) SVPWM modulation (b) DPWM1 modulation.

switched from SVPWM to DPWM1. As it can be seen from the figure, harmonic distortion increases from 5.83% to 9.14% with the same effective output current. The total drawn power from the inverter is 225 W and the modulation index is 0.68 throughout the experiments. It should be noted that, although it would be better verification to load the system at the same level as simulation, due to decapped module without a heat sink, experimental tests had to be carried out at low power level. Fig. 7.18 shows the IR thermal image of IGBT dies during SVPWM and DPWM1 modulations respectively. The proposed strategy introduces a significant reduction in the switching power losses of the IGBT switches, which are assumed to be aged.

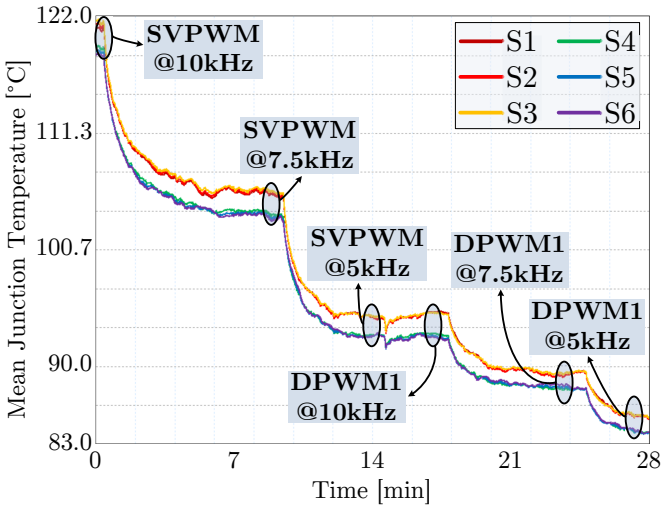


Figure 7.19. Mean junction temperature deviation of IGBT switches under switching power loss reduction case scenario.

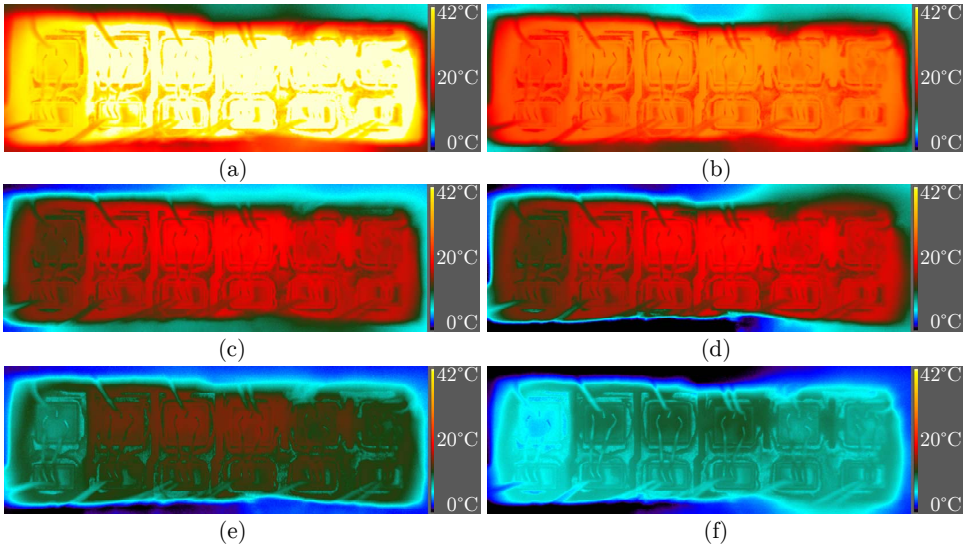


Figure 7.20. IR thermal image of IGBT dies for each cases throughout the switching power loss reduction case scenario when (a) SVPWM @10 kHz, (b) SVPWM @7.5 kHz, (c) SVPWM @5 kHz, (d) DPWM1 @10 kHz, (e) DPWM1 @7.5 kHz, and (f) DPWM1 @5 kHz.

As a second set of experimental verification, a switching power loss reduction scenario is created which demonstrates and also summarizes all approaches discussed above. In this scenario, as the failure precursor reaches to the pre-defined threshold value while inverter is running through SVPWM at 10 kHz switching frequency, initially the switching frequency

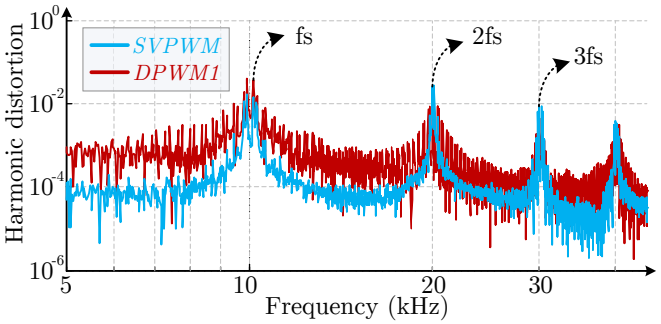


Figure 7.21. Total harmonic distortion comparison for the switching power loss reduction case scenario.

is decreased from 10 kHz to 7.5 kHz in order to decrease the switching losses and extend the lifetime of power switch. After that, with the assumption of further aging, the switching frequency is decreased from 7.5 kHz to 5 kHz. To provide further thermal relief, first, the modulation scheme is switched to DPWM1 while setting switching frequency back to 10 kHz -which has the same switching power losses with the last condition- and then, the switching frequency is decreased to 7.5 kHz and 5 kHz respectively, as final loss reduction options.

The deviation of mean junction temperature in IGBT switches under switching power loss reduction case is depicted in Fig. 7.19. The mean junction temperatures of all switches are reduced from 121.8°C to 105.5°C by reducing the switching frequency from 10 kHz to 7.5 kHz. The junction temperature is decreased to 92.6°C by lowering the switching frequency from 7.5 kHz to 5 kHz. As expected, the mean junction temperature of all IGBT switches remain the same when the switching modulation is switched to DPWM1 and the switching frequency increased back to 10 kHz. Decreasing the switching frequency from 10 kHz to 7.5 kHz within DPWM1 modulation scheme leads to additional 3.3°C decrease to the mean junction temperatures. Finally, the junction temperature of all IGBT switches decreased from 89.3°C to 85.6°C as we decrease the switching frequency of DPWM1 modulation to 5 kHz. Fig.18 7.20 shows IR thermal images of IGBT dies when the temperature is settled for all cases in the switching power loss reduction scenarios. These images are obtained by

taking the coolest condition (83°C) as baseline and providing the differential temperature change compared to this temperature.

Total harmonic distortion comparison results are given in Fig. 7.21. As it is typical for a balanced three-phase inverter, the major harmonics are observed around the switching frequency. The total harmonic distortion measurement increases from 5.83% to 9.14% when the modulation scheme is switched from SVPWM and DPWM1. THD ratio in the experimental results is $THD_{ratio} = 5.83/9.14 = 0.6379$ where this is calculated as 0.66 in Fig. 7.4. This shows good correlation between theoretical calculations and experimental results.

It is clear from Fig. 7.19 that the switching power loss reduction scenario provides 36.2°C reduction in the mean junction temperatures for all IGBT switches. This can be interpreted as a direct benefit of the proposed strategy to reduce the switching power losses effectively for aged power devices. As the lifetime of the power semiconductor devices is mainly affected by their average junction temperatures and junction temperature fluctuation; lifetime extension of thermally-aged device is efficiently performed using the proposed strategy. On the other hand, since there is an increase in THD of the output currents due to the proposed strategy, the tradeoff between EOL and THD needs to be well analyzed for the specific application. In practice, the selection between the switching frequency and modulation technique should be made according to these figures of merits for the given application.

7.7 Conclusion

In this chapter, two approaches are presented to increase the lifetime of the three-phase converters. Recent studies on the failure precursors indicate that it is possible to monitor the health of the switches on the fly which in turn necessitates new control or modulation based solutions regarding the lifetime of the inverter. For this purpose, systematic manipulations of both the modulation techniques and switching frequency are analyzed in detail and proposed as secondary control strategy engaged with predefined precursor threshold values. The

proposed modulation controller adjusts the zero-vector placement as well as the switching frequency in order to reduce the power losses on the switches. The proposed approach affects current waveform quality but increases the remaining lifetime of the faulty device. This tradeoff needs to be well analyzed for given applications. In this chapter, a framework has been given to address this tradeoff. The selection of the switching frequency and modulation technique is strictly dependent on the desired level of reliability and application limitations.

CHAPTER 8

SUMMARY AND CONCLUSIONS

The rapid and widespread deployment of SiC devices raises long term reliability concerns, particularly for mission and safety critical systems due to limited field data and potential uncertainties. Therefore, in this dissertation, a comprehensive reliability and aging evaluation of SiC MOSFETs is presented for high temperature applications. The SiC MOSFETs used in this study are aged through accelerated high temperature power cycling and key parameters are measured using an automated curve tracer at certain intervals. The variation of electrical parameters with respect to aging cycles is evaluated. The correlation between electrical parameter variations and state of the device health is investigated with a particular focus on the effect of each degradation mechanism.

It has been shown that on-state resistance, and gate threshold voltage are the electrical parameters that remarkably increase with aging for all devices. After a detailed analysis, the threshold voltage drift and continuous increase in on-state resistance are found to be related to the gate oxide degradation. Gate threshold voltage increases logarithmically throughout the aging due to the gate oxide interface charge trapping. The on-state resistance shows a very similar trend to the gate threshold voltage except two devices showing sudden increases after 7000 cycles. These jumps in on-state resistance values for two devices are also observed at body diode voltage drop at -5V gate voltage bias. It is concluded that sudden increases in body diode voltage drop and on-state resistance are due to packaging-related degradation. This assumption is verified with a detailed failure analysis and the root cause of the packing related degradation is found to be the wedge bond heel cracking.

Since all parameters are closely related to operating conditions, in-situ monitoring with the ability to control electrical and thermal conditions is proposed. First, simultaneously monitoring the threshold voltage and body diode voltage drop is proposed in order to distinguish different failure mechanism; any of which could be the major aging mechanism for

the specific application. Furthermore, after detailed analysis, it has been discovered that SiC MOSFETs has a unique secondary conduction mode in the third quadrant operation. This unique operation mode is clearly illustrated with a proposed body diode transfer characterization curve. This unique two different conduction modes of SiC is found to be the MOSFET path conduction and the PiN diode path conduction.

Body diode voltage drop variations captured throughout aging at 0V and -5V gate voltage bias and it found that contact resistance variations can be monitored with PiN diode path conduction while the gate oxide degradation can be detected during MOSFET path conduction. Therefore, it is concluded that just by capturing body diode voltage drop at different gate biases, a complete state of health of SiC devices can be obtained. Armed with this finding, a new condition monitoring method is invented for SiC power MOSFETs. This method monitors the reverse body diode voltage drop at 0V and -5V gate bias in order to have detailed condition information of the device with a simple circuit. An experimental implementation circuit of the new condition monitoring method is provided as an example. Experimental results are presented for two artificially degraded devices to demonstrate the designed condition monitoring circuit can accurately detect both gate oxide degradation and the package related degradation. The experimental results verified that the proposed method can accurately monitor both the gate oxide and packaging degradation with the ability of distinguishing the contribution of each just by monitoring a single precursor parameter. Furthermore, possible ways of integrating the monitoring method into a gate driver are presented.

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BIOGRAPHICAL SKETCH

Enes Ugur received the BSc degree in electrical engineering from Istanbul Technical University, Istanbul, Turkey, in 2008 and the MSc degree from Yildiz Technical University, Istanbul, in 2011. He is currently working toward the PhD degree at The University of Texas at Dallas, Richardson, TX, USA. His research interests include dcdc converters, electric vehicles, real-time fault diagnosis of wide-bandgap devices, and energy management strategies for renewable energy systems.

CURRICULUM VITAE

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EDUCATION

The University of Texas at Dallas, Richardson, TX *December 2019*
PhD in Electrical Engineering

Yildiz Technical University, Istanbul, Turkey *August 2011*
MS in Electrical Engineering

Istanbul Technical University, Istanbul, Turkey *June 2008*
BA in Electrical Engineering

RESEARCH AND TECHNICAL EXPERIENCE

Texas Instruments May. 2019 - Aug. 2019
Design Engineering Intern *Dallas, TX*

- Partnered with marketing teams and system engineering to develop SiC gate driver design specifications.
- Developed test specifications and designed prototypes for gate driver performance verification.
- Provided high-level analysis on chip architecture trade-offs to ensure spec compliance and superior performance at a competitive cost.

Power Electronics and Drives Laboratory, UT Dallas Sep. 2015 - May. 2019
Research Assistant *Richardson, TX*

- Investigated reliability of SiC semiconductor devices to establish real-time degradation monitoring for power electronics systems and defined most viable precursor parameters.
- Invented a condition monitoring method for SiC based power converters which can independently monitor die and package health (patent pending).
- Proposed hybrid modulation controller for reducing the power losses on the switches and implemented on a two-level inverter.
- Conducted a research project in collaboration with Texas Instruments Inc. on fault characterization and degradation monitoring of SiC devices.

Yildiz Technical University Sep. 2011 - Sep. 2015
Research Associate *Istanbul, Turkey*

- Designed a 5 kW cascaded bi-directional buck-boost converter for electric vehicles.
- Implemented an energy management system on a battery powered 3-wheel vehicle for battery life extension by drawing peak load demands from ultra-capacitor.
- Conducted a government supported research project 10 KW multi input bi-directional power conditioning unit for battery powered systems.

United Nations Industrial Development Organization (UNIDO) Nov. 2009 - Sep. 2011
Electrical Engineer *Istanbul, Turkey*

- Participated in several multi-disciplinary hydrogen energy projects supported by European Union.
- Designed and implemented a 10 kW hydrogen fuel cell and solar powered hybrid boat.
- Implemented a 5kW fuel cell and battery powered hybrid power train passenger cart.
- Supervised a 30kW wind turbine and 20 kW PV panels installation as a part of $1.9M budgeted small hydrogen island project.

TECHNICAL STRENGTHS

Software	Code Composer Studio, Altium, ReserchIR, Visio
Modeling	PSIM, PLECS, LTspice, MATLAB/Simulink
Programming	C, MATLAB, LabVIEW (Certified LabVIEW Associate Developer)
Tools	Curve Tracer, NI DAQ, Scanning Acoustic Microscopy (SAM)

LEADERSHIP EXPERIENCE

Yildiz Technical University Sep. 2011 - Sep. 2015
Research/Teaching Associate *Istanbul, Turkey*

- Coordinated $500K budgeted smart home project which accomplished autonomous energy supply and management.
- Lectured *Electrical Circuit Laboratory, Electronics Laboratory, and Electric Energy Systems Laboratory* courses for 300+ undergraduate students each semester.
- Prepared exams and graded students for Electrical Circuit Laboratory courses for 4 semesters.

Joint Research Centre - European Commission July 2010 & July 2011
Organizing Committee *Istanbul, Turkey*

- Organized venue, lecture schedule and social activities at *International Summer School on: PEM Fuel Cells Applications and Integration* for 40+ researchers.

Istanbul Technical University Sep. 2006 - Jun. 2008
Chairman, Electrical Engineering Student Club *Istanbul, Turkey*

- Elected as chairman of the board for two consecutive years in Electrical Engineering Student Club with 100+ students.
- Organized several trainings and technical meetings for graduate and undergraduate students.

Chamber of Electrical Engineers Sep. 2006 - Jul. 2007
Project Coordinator, Fuel Cell Vehicle Team *Istanbul, Turkey*

- Found a team of 20 undergraduate students to attend the competition of fuel cell powered vehicles.
- Directed the research team and coordinated interdisciplinary team work.

PUBLICATIONS

Patents

- **E. Ugur**, S. Pu, B. Akin, F. Yang, and C. Xu, "Condition Monitoring System and Method for SiC Power MOSFETs," *(patent pending)*.

Selected Journal Papers

- **E. Ugur**, F. Yang, S. Pu, S. Zhao and B. Akin, "Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling," in *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2858-2867, May-June 2019.
- **E. Ugur**, S. Dusmez and B. Akin, "An Investigation on Diagnosis-Based Power Switch Lifetime Extension Strategies for Three-Phase Inverters," in *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 2064-2075, March-April 2019.
- F. Erturk, **E. Ugur**, J. Olson and B. Akin, "Real-Time Aging Detection of SiC MOSFETs," in *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 600-609, Jan.-Feb. 2019.
- F. Yang, **E. Ugur**, B. Akin and G. Wang, "Design Methodology of DC Power Cycling Test Setup for SiC MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.
- F. Yang, **E. Ugur** and B. Akin, "Evaluation of Aging's Effect on Temperature Sensitive Electrical Parameters in SiC MOSFETs," in *IEEE Transactions on Power Electronics*.
- S. Pu, **E. Ugur**, F. Yang, G. Wang and B. Akin, "In-situ Degradation Monitoring of SiC MOSFET Based on Switching Transient Measurement," in *IEEE Transactions on Industrial Electronics*.
- S. H. Ali, **E. Ugur** and B. Akin, "Analysis of Vth Variations in IGBTs Under Thermal Stress for Improved Condition Monitoring in Automotive Power Conversion Systems," in *IEEE Transactions on Vehicular Technology*, vol. 68, no. 1, pp. 193-202, Jan. 2019.
- C. Xu, F. Yang, **E. Ugur**, S. Pu and B. Akin, "Performance degradation of GaN HEMTs under accelerated power cycling tests," in *CPSS Transactions on Power Electronics and Applications*, vol. 3, no. 4, pp. 269-277, Dec. 2018.

Selected Conference Papers

- S. Dusmez, **E. Ugur** and B. Akin, "Power switch lifetime extension strategies for three-phase converters," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1176-1182.
- **E. Ugur** and B. Akin, "Aging assessment of discrete SiC MOSFETs under high temperature cycling tests," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 3496-3501.
- C. Xu, **E. Ugur** and B. Akin, "Investigation of performance degradation in thermally aged cascode GaN power devices," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices*

and Applications (WiPDA), Albuquerque, NM, 2017, pp. 55-59.

- S. Pu, **E. Ugur** and B. Akin, "Real-time degradation monitoring of SiC-MOSFETs through readily available system microcontroller," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 378-382.
- S. Pu, **E. Ugur**, B. Akin and H. Akca, "Investigation of EM radiation changes in SiC based converters throughout device aging," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 190-194.
- F. Yang, C. Xu, **E. Ugur**, S. Pu and B. Akin, "Design of a Fast Dynamic On-Resistance Measurement Circuit for GaN Power HEMTs," *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, Long Beach, CA, 2018, pp. 359-365.
- C. Xu, **E. Ugur**, F. Yang, S. Pu and B. Akin, "Investigation of Performance Degradation in Enhancement-Mode GaN HEMTs under Accelerated Aging," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, 2018, pp. 98-102.
- S. Pu, **E. Ugur**, F. Yang, C. Xu and B. Akin, "Thermally Triggered SiC MOSFET Aging Effect on Conducted EMI," *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, 2018, pp. 51-55.
- F. Yang, **E. Ugur**, S. Pu and B. Akin, "Design of a High-Performance DC Power Cycling Test Setup for SiC MOSFETs," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 1390-1396.
- S. Pu, F. Yang, **E. Ugur**, B. T. Vankayalapati, C. Xu and B. Akin, "On-Board SiC MOSFET Degradation Monitoring Through Readily Available Inverter Current/Voltage Sensors," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, Detroit, MI, USA, 2019, pp. 1-5.
- S. Pu, F. Yang, **E. Ugur**, C. Xu and B. Akin, "SiC MOSFET Aging Detection Based on Miller Plateau Voltage Sensing," *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, Detroit, MI, USA, 2019, pp. 1-6.