DESIGN APPROACHES FOR ENHANCING PHOTOVOLTAIC PERFORMANCE OF SILICON SOLAR CELLS SENSITIZED BY PROXIMAL NANOCRYSTALLINE QUANTUM DOTS

by

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Dedicated to my mom and dad

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Energy transfer (ET) based sensitization of silicon (Si) using proximal nanocrystal quantum dots (NQDs) has been studied extensively in recent years as a means to develop thin and flexible Si based solar cells. The driving force for this research activity is a reduction in materials cost. To date, the main method for determining the role of ET in sensitizing Si has been optical spectroscopic studies. The quantitative contribution from two modes of ET (namely, nonradiative and radiative) has been reported using time-resolved photoluminescence (TRPL) spectroscopy coupled with extensive theoretical modelling. Thus, optical techniques have established the potential for utilizing ET based sensitization of Si as a feasible way to develop novel NQD-Si hybrid solar cells. However, the ultimate measure of the efficiency of ET-based mechanisms is the generation of electron-hole pairs by the impinging photons. It is therefore important to perform electrical measurements. However, only a couple of studies have attempted electrical quantification of ET modes. A few studies have focused on photocurrent measurements, without considering industrially relevant photovoltaic (PV) systems. Therefore, there is a need to develop a systematic approach for the electrical quantification of ET-generated

charges and to help engineer new PV architectures optimized for harnessing the full advantages of ET mechanisms. Within this context, the work presented in this dissertation aims to develop an experimental testing protocol that can be applied to different PV structures for quantifying ET contributions from electrical measurements. We fabricated bulk Si solar cells (SCs) as a test structure and utilized CdSe/ZnS NQDs for ET based sensitization. The NQD-bulk Si hybrid devices showed ~30% PV enhancement after NQD deposition. We measured external quantum efficiency (EQE) of these devices to quantify ET-generated charges. Reflectance measurements were also performed to decouple contributions of intrinsic optical effects (i.e., anti-reflection) from NQD mediated ET processes. Our analysis indicates that the contribution of ET-generated charges cannot be detected by EQE measurements. Instead, changes in the optical properties (i.e., anti-reflection property) due to the NQD layer are found to be the primary source of the photocurrent enhancement. Based on this finding, we propose to minimize bulk Si absorption by using an ultrathin (~300 nm) Si PV architecture which should enable measurements of ET-generated charges. We describe an optimized process flow for fabricating such ultrathin Si devices. The devices fabricated by this method behave like photo-detectors and show enhanced sensitivity under 1 Sun AM1.5G illumination. The geometry and process flow of these devices make it possible to incorporate NQDs for sensitization. Overall, this dissertation provides a protocol for the quantification of ET-generated charges and documents an optimized process flow for the development of an ultrathin Si solar cells.

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CHAPTER 1

INTRODUCTION

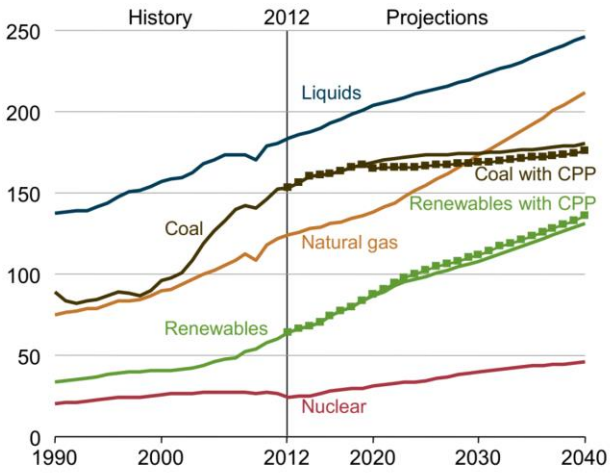
1.1 Motivation

Energy demand in the world is rapidly increasing. In recent times, the global demand of energy has increased several folds due to rapid technological advances. The U.S. Energy Information Administration (EIA) projects a 48% increase in global energy consumption by 2040 [1]. This increase in energy demand will be strongly driven by developing countries where economic growth and improvement in infrastructure will rapidly increase the consumption of energy. In fact, the EIA estimates a 71% rise in energy demand from 2012-2040 in developing countries compared to an 18% increase in developed countries for the same period [1]. In developed countries, technological advancement is a dominating force in our daily life and the energy cost associated with such upward progression cannot be overlooked. Modern society will need constant connectivity to electronic products and their associated services which will require abundant access to cheap energy. Within this context, renewable energy sources such as solar energy has the enormous potential to produce cheap energy.

Renewable energy sources are abundant, whereas fossil fuels are limited, expensive and not eco-friendly. This environmental factor is one of the chief reasons to utilize renewable energy sources such as wind, solar, hydro and geothermal energy. In fact, continues and heavy use of fossil fuel is causing climate change and increasing the occurrence and strength of natural disasters [2]. Substantial global capacity addition for the renewable energy sources has been observed in the 2015-16 period due to these reasons and the projection for the future is also very strong.

Solar energy is particularly important among all the renewable energy sources. It is the most abundant in nature. Solar energy is freely available for all the inhabitants of Earth and has zero greenhouse gas emissions, which is a major concern for the continued use of fossil fuels. The total radiant power of the sun is 3.8×10^{23} kW and the Earth receives about 1.8×10^{14} kW (i.e. solar irradiance is 1000 W/m^2 at the middle of a clear day) [2, 3]. The EIA estimates that US residential customers use on an average 30 kWh/day [2]. This personal daily energy consumption can be harnessed from an area of only 5 m^2 (or ~54 square foot) considering 6 hours of daily sunlight. Studies indicate that solar energy can sustainably satisfy the global demand for energy as the sun, an inexhaustible source of energy, will provide sustainable output over a very long period [2, 4].

The growth of renewable energy capacity has steadily increased (see the green curve labeled as renewables in Figure 1.1 (a)) as the global commitment to reducing the use of fossil fuels increased [5]. In 2015, the installed capacity of global solar photovoltaic (PV) increased by 28% from 2014 levels (see Figure 1.1 (b)) and this increase is highest among all the other sources of renewable energy as seen from Figure 1.1 (b) [5]. At the same time, there is a drive to increase PV efficiency. Researchers are actively evaluating different concepts and approaches to increase PV module efficiency in addition to cost reduction. In the foreseeable future, the PV industry will continue to see development in all sub-sectors such as photovoltaics (PVs), concentrating solar panels (CSP) and solar heaters [2]. It is an exciting time to explore innovative ideas with the aim to increase the uptake of PV.



Note: Dotted lines for coal and renewables show projected effects of the U.S. Clean Power Plan.

(a)

	Hydropower	PV[1]	CSP[2]	Wind	Geothermal	Biomass	All Renewables
2005	2%	38%	0%	23%	4%	13%	4%
2006	2%	32%	0%	25%	3%	7%	4%
2007	3%	5%	5%	27%	0%	6%	5%
2008	3%	71%	14%	29%	4%	4%	6%
2009	3%	62%	22%	31%	7%	15%	7%
2010	3%	90%	83%	25%	3%	13%	8%
2011	3%	78%	43%	20%	1%	9%	8%
2012	3%	41%	57%	19%	5%	12%	8%
2013	3%	38%	36%	13%	3%	6%	7%
2014	4%	28%	29%	16%	6%	6%	8.5%
2015	1%	28%	9%	17%	3%	14%	7.9%

- annual decrease annual increase +

(b)

Figure 1.1 (a) Energy consumption (unit of quadrillion Btu) in world by energy source from 1990-2040.[1] (b) Annual percentage change of cumulative global electricity capacity by source.[5]

Overall success for PV uptake depends on the cost ($/kWh) to the consumer, which is not currently cheaper than conventional energy sources. However, over the last decade, the market has observed a significant reduction in PV prices [6, 7]. The cost is estimated by '*cost per peak watt ($/W$_p$)*' which encompasses both the module cost and costs related to installation [8].

Currently, $\$/W_p$ is ~1 or ~0.10 \$/kWh, which is close to the average grid electricity cost in the US [8]. In fact, 20 states in US have achieved grid parity (i.e., comparable cost to grid electricity using conventional energy sources) [9]. However, achieving grid parity alone is not sufficient to replace the fossil fuels conventionally used for electricity production. Therefore, development of strong infrastructure is necessary to encourage widespread uptake of PV in addition to cost reduction.

In fact, PV related costs need to be reduced to at least half or one-third of the current rate (i.e., down to ~ 0.05 to 0.03 \$/kWh, Figure 1.2) for significant uptake of PV modules in the current energy production landscape [8]. Figure 1.2 effectively shows the relationship between module cost (\$/m^2), power conversion efficiency (PCE, %) and production cost (\$/kWh). Within this context, current technologies suffer due to low efficiency and high cost of modules. A significant reduction in module cost can offset the efficiency demand and vice versa.

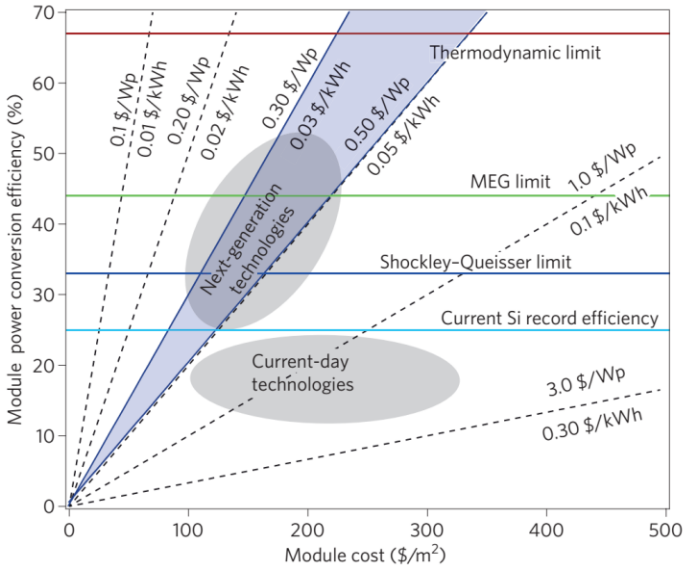


Figure 1.2. Relationship between power conversion efficiency, module costs per area and cost per peak watt (\$/W$_p$). Decreasing the module cost can facilitate use of lower efficiency cells but higher module cost can be tolerated if the module efficiency can be substantially increased.[8]

Hence, the PV community is actively developing and implementing 'third generation' approaches [10, 11] targeted towards achieving PV modules that cost 0.03-0.05 $/kWh. Historically, the 'first generation' of PV technology is based on single crystal Silicon (Si) wafers and this technology eventually matured and achieved a record efficiency of 25.6 % in a laboratory set-up [11]. Continued research and development is occurring to push the PCE towards the Shockley-Queisser limit for Si (33.5%) [2, 8, 10, 12]. It is well known that when any technology matures the overall cost is limited by the inherent materials cost [10]. A study on Si PVs for high volume production (500 MW/year) showed that 70% of the overall manufacturing cost is due to the material cost of Si [10]. Thus, the 'second generation' PVs based on thin film deposition techniques was developed.

Currently substantial activity is occurring for the design of 'third generation' approaches which rely on advanced thin film deposition techniques in combination with different innovative approaches [11, 13]. The aim of 'third generation' techniques is to reduce the overall PV cost and facilitate a widespread addition of PV capacity [8, 10, 11]. The 'third generation' approaches seek to achieve two main goals : (a) reduction of total cost by substantially decreasing materials cost and (b) increasing the efficiency of the PV modules beyond the Shockley-Quiesser limit in case of single junction devices [8, 11].

It is worth mentioning that PV modules based on single crystal Si still has ~90% of the total PV market share [14]. However, one of the major disadvantages of using Si PVs is the cost of manufacturing Si wafers with superior electronic properties [14]. Additionally, Si is an indirect band gap material (Band gap, E_g= 1.12 eV corresponding to an absorption cut-off at 1160 nm) which results in poor light absorption, specifically in the longer wavelength region.

Therefore, Si wafers with thickness of ~200 μm are necessary for complete light absorption, setting a severe lower limit for cost reduction [15]. It has been reported that the calculated inherent PCE of a Si PV module can reach 29.4% for an optimum Si thickness of 110 μm [14]. Therefore, materials cost will play a significant role even after achieving a PCE close to the Shockley-Quiesser limit. This constitutes a substantial roadblock for continued use of Si PV devices despite more than 40 years of strong manufacturing development. The implementation of a 'third generation' approach is therefore mandatory. The next section describes an approach that takes advantage of the electronic properties of Si and its mature manufacturing processes and adds a photonic element to address the photon absorption component of the devices, thus circumventing the issue associated with inherent material cost.

1.2 Concept of nanocrystal quantum dot (NQD)-Si hybrid photovoltaics

A widely applied alternative approach to reduce cost ($/kWh) has been the utilization of advancements in thin film deposition techniques. Amorphous Si (a-Si) has been widely studied within this context. However, thin films of a-Si have been limited to a PCE of 10% despite cheap and low energy deposition techniques [11]. Band gap engineering has been widely investigated as a 'third generation' approach to increase the band gap of crystalline Si by embedding quantum wells (QWs) or quantum dots (QDs) of Si inside a Si-based dielectric such as oxides, nitrides or carbides [11]. This approach has resulted in the fabrication tandem cell with the QWs or QDs as the top cell and a thin film of crystalline Si as the bottom cell [11]. These reported techniques capitalize on the advances in thin film Si processing.

However, another equally innovative 'third generation' approach is based on separating PV functionalities into two different components (1) a photonic element for light absorption and

(2) a crystalline, semiconductor element for charge generation and collection. Nanocrystal quantum dots (NQDs) are used as the photonic element (i.e., absorber material) and Si thin films are used as the charge generation-collection material. The generation of charges in the Si thin film is achieved through excitonic energy transfer (ET) mechanisms. This is in contrast with conventional PV devices which are based on charge transfer (CT) mechanism. ET is inherently different from CT which uses the same material for both absorption and carrier transportation. In ET based devices, effective sensitization results in carrier generation due to the efficient electromagnetic interaction between the NQDs and Si. This unique approach harnesses the tunable absorption property of NQDs (particularly in the near-infrared region) and maintains the superior carrier generation-transportation property of the Si [16, 17]. Overall, the approach provides a pathway to overcome the severe lower limit of thickness that results from weak absorption in Si at longer wavelengths. Therefore, ET based sensitization of thin film crystalline Si can significantly reduce materials cost.

This dissertation is focused on this concept of ET based sensitization of Si by NQD for solar cell applications. In 2009, Lu and Madhukar [17] proposed the idea of separating optical and electrical functionalities for the application in a solar cell. The basic design principle of an ET based NQD-Si hybrid system is shown in Figure 1.3. Here, ‘coupling’ of the NQDs and Si via Near-field electromagnetic interaction is key to combine the clearly separated functionalities inside a PV device. NQDs absorb incident solar light and an excited electron-hole pair (exciton) is created, which is bound inside NQD by Coulombic attraction. This bound electron-hole pair (exciton) can transfer energy to the underlying high-mobility Si channel where carriers are generated and collected. The absorbed energy is transferred to Si by near-field electromagnetic

interaction between NQD and Si. There are two modes of energy transfer, namely non-radiative energy transfer (NRET) and radiative energy transfer (RET) [18]. So, optimization of these two modes is crucial for energy management from NQD towards Si. The ET modes are discussed in chapter 2. However, ET based NQD- Si hybrid PV devices relax the strict demands needed for producing efficient charge separation in the conventional devices such as homojunction and heterojunction PVs as well as organic PVs.

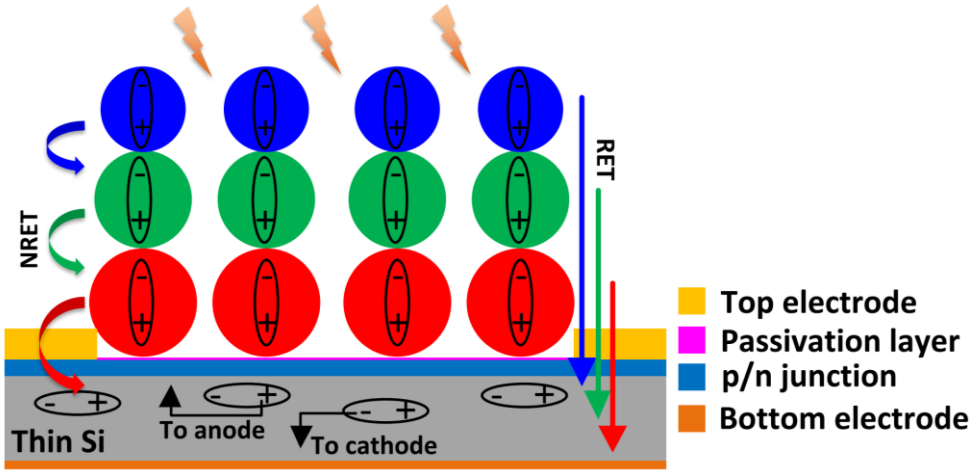


Figure 1.3. Schematic drawing showing the concept of ET based NQD-Si hybrid solar cell in a planar configuration. Size gradient NQD layers cover the solar spectrum. Absorbed energy is cascaded towards Si through different ET modes such as non-radiative energy transfer (NRET) and radiative energy transfer (RET).

ET based NQD-Si hybrid PVs has the potential to significantly reduced Si thickness requirements from ~ 200 µm. In fact, optimization of ET from different sizes of NQDs can potentially reduce Si thickness to <1 µm. Thereby materials cost can be reduced substantially. Also, the PV modules can be flexible with the development of ultrathin devices. Within this context, it is essential to fully understand the effectiveness of ET mechanisms inside an industrially relevant PV device architecture. Systematic study and correct quantification of ET-generated carriers will help to rationally design different PV structures. Then, the devices can be

optimally engineered for maximum carrier generation in Si. Furthermore, understating the hybrid system from charge generation perspective can help to incorporate new absorber materials and innovative nanostructured geometries. This dissertation addresses the core issue of finding the electrical viability of ET-generated carrier contribution inside a working PV system. Overall, the studies test different PV architectures to provide a systematic route for electrical characterization.

1.3 Dissertation organization

This dissertation has six chapters and is organized in the following way to provide a coherent flow facilitating logical progression of the study.

- Chapter 1 describes the importance and relevance of renewable energy, particularly solar energy, in the context of the recent energy landscape. This introduction lays the foundation and motivation behind the undertaken study. The scope of solar energy in terms of economic impact is also discussed. Later, the concept of energy transfer (ET) based nanocrystal quantum dot (NQD) sensitization of Si is briefly explained.
- Chapter 2 provides theoretical background with comprehensive literature review. This chapter provides important references relevant to this study which is essential for a detailed understanding of the project. Also, the working principle of a solar cell and the extraction of basic parameters from the I-V graph is briefly discussed.
- Chapter 3 outlines the experimental methods used in this work. Different deposition techniques such as low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) and electron-beam evaporation are discussed.

Plasma processing for etching, and characterization methods (scanning electron microscope, atomic force microscopy, spectroscopic ellipsometry, reflectance measurements, profilometery, four-point probe measurements) are briefly discussed. Additionally, the electrical characterization of solar cells via current-voltage (I-V) and external quantum efficiency (EQE) measurements are described.

- Chapter 4 presents the results for the NQD sensitization of bulk Si solar cells via ET. This chapter is central to the development of chapter 5. The method for quantifying ET-generated carriers is described in this chapter. Bulk Si solar cells sensitized by CdSe/ZnS NQDs are used as test PV system to understand the origin of PV enhancement after NQD deposition.
- Chapter 5 discusses the design approach for fabricating ultrathin (300 nm) Si solar cells. Mechanical and structural roadblocks for fabricating such a fragile structure are identified and subsequently optimized to improve yield. Once fabricated, the solar cells are characterized electrically. Overall, the chapter provides detailed steps for the fabrication of ultrathin Si PV devices with the possibility of incorporating NQDs in the finished structure.
- Chapter 6 summarizes the outcomes and provides future direction to circumvent problems faced during this dissertation. This chapter proposes different approaches that can be investigated to improve the processing of ultrathin Si solar cells and provides guidelines for incorporating NQDs into the structures.

CHAPTER 2

THEORETICAL BACKGROUND AND LITERATURE REVIEW

Contents related to energy transfer mechanisms to Si of this chapter have been adapted with permission from Weina Peng, Sara M. Rupich, Natis Shafiq, Yuri N. Gartstein, Anton V. Malko and Yves J. Chabal, *Silicon surface modification for emergent photovoltaic applications based on energy transfer*, Chemical Reviews, 115 (23), Copyright 2015 American Chemical Society [19]. I acknowledge the major contribution from all the other authors and re-use some of the paragraphs as a co-author. Sections and sub-sections 2.1, 2.1.1, 2.1.2 were taken fully from the paper with minor modifications such as correcting the figure numbers as per the organization of the dissertation. Readers are encouraged to study the theoretical consideration from this review article which is relevant for understanding the theoretical framework of the energy transfer mechanism to Si substrates. The paper also discusses photocurrent measurements and different deposition techniques for NQDs. Readers are suggested to consult the paper for detailed information.

After providing the background on ET, section 2.2 briefly introduces the working principle of a solar cell (SC) and the important parameters. This work uses SCs as a test structure for NQD sensitization. Thus, a brief overview is provided in this section and introduces (with appropriate references) the working principles of SCs. Readers are encouraged to consider references provided therein to study further.

2.1 Energy transfer (ET) mechanism

The main focus of this section is on the mechanisms of ET into Si from neighboring photoexcited quantum emitters such as colloidal NQDs. We distinguish non-radiative ET (NRET) and radiative ET (RET) [20] as qualitatively different contributions to the overall ET enabled by near-field electromagnetic interactions [18, 21-23]. Dexter [24] was probably the first to explicitly suggest the idea of external NRET sensitization of inorganic semiconductors for PV applications. The NRET mechanism is akin to the familiar Förster ET (with the usual acronym FRET) enabled by dipole-dipole interaction between neighboring molecular species and depending on the spectral overlap of the energy donor emission and energy acceptor absorption spectra [25-27]. The NRET process can be thought of as direct excitation [28] of the electron-hole pairs in a semiconductor by the electric field of the decaying emitter excitons. While the NRET mechanism is more frequently discussed in the literature for ET-hybrids [16, 17, 29-33], the potential significance of RET should not be overlooked as its relative contributions can vary depending on both the distance between the emitter and acceptor and on the spectral range considered [18, 23]. In the RET process, the emitter's exciton preferentially decays into photonic modes that can propagate only within the energy-accepting semiconductor, that is waveguide modes in spatially-confined semiconductor layers and wires [34]. These propagating modes would eventually be absorbed to produce electron-hole pairs contributing to the electric current. The effective conversion of the incoming solar plane-wave photons, via re-emission from a relaxed localized exciton, into waveguide modes may be compared to the effect from scattering processes achievable with metallic and dielectric structures judiciously patterned to increase the incident light absorption in thin semiconductor layers [35, 36].

2.1.1 Determination of NRET efficiencies from nanocrystal quantum dots to semiconductor Substrates

The field of ET between molecular absorbers or semiconductor NQDs and various semiconductor surfaces for the purpose of photovoltaic light harvesting has seen something of resurgence in the past few years. Particularly, GaAs and silicon surfaces have been employed in order to improve efficiencies of the existing technologically important solar cells, where GaAs-based structures pertain to very high-efficiency (and possibly multi-junction) cells while Si structures are thought to become more efficient in the thin film geometries. Clear illustrations of the viability of the energy transfer-based concepts first started to emerge in experimental studies of NQDs on GaAs substrates, in which the NRET efficiency was predicted to be substantial thanks to the large absorption coefficient of GaAs arising from its direct band gap transitions.

The efficiencies of ET can be measured via time- and spectrally- resolved PL spectroscopy. This technique is a valuable tool that can be used to monitor the presence and dynamical behavior of correlated electrons and holes in semiconductor media and is extensively described in a number of books [37, 38]. During the ET process, the emission of the donor molecule or NQD is quenched while the emission of the acceptor molecule is enhanced. The degree of the quenching/enhancement provides a quantitative measure of the ET efficiency. However, this ratiometric appoach is not always reliable. A more precise approach is to monitor changes in the PL dynamics of a donor in the presence of an acceptor.

NRET from near-infrared active PbS NQDs emitting at ~ 965 nm to buried InGaAs quantum wells was shown by Lu *et al*. [16]. Quantum wells made from short-period superlattices were buried about 3 nm below the sulfur-passivated GaAs surface. A drop-cast layer of NQDs

was deposited on the top of the structure, with (approximately 8 nm separating the monolayer and quantum wells. To eliminate charge carrier feeding by electron-hole pairs generated in the substrate, the excitation wavelength was set to 910 nm. The authors observed about a 35% reduction in the NQD PL intensity as compared to the reference substrate without buried quantum wells. Additionally, the average PL decay time decreased from 298 ns on GaAs to 208 ns on the buried well structure as seen in Figure 2.1. Based on these measurements, the authors estimated a non-radiative transfer decay time of ~690 ns compared with the radiative decay time of 960 ns for the PbS NQDs. That corresponds to ~30% non-radiative transfer efficiency to the quantum wells from these NQDs. Another important achievement was a demonstration of NRET-induced photocurrent in GaAs patterned quantum wells sensitized with CdSe/ZnS NQDs [33].

By comparison of the PL decay times, the authors estimated the efficiency of NRET from NQDs to the proximal semiconductor surface to be 79%. Additionally, photocurrent measurements revealed a six-fold enhancement for the patterned hybrid devices when compared to the reference *p-i-n* structure. From the data, the authors concluded that approximately 89% of the exciton energy was transferred into the quantum wells via NRET from the proximal NQDs. They also noted that such hybrid configurations are not limited to using NQDs as energy donors, but should also be applicable to other strongly absorbing, solution-based materials.

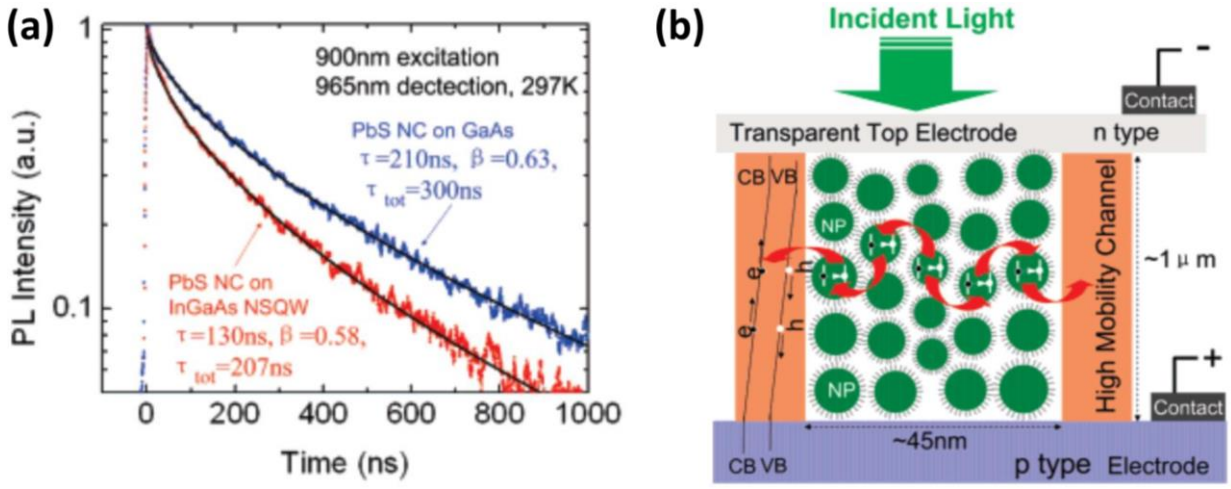


Figure 2.1. (a) Time-resolved PL of PbS NQDs on passviated GaAs (blue) and on passivated near surface quantum wells (red), excited at 900 nm (below GaAs bandgap) and detected at 965 nm (PbS PL peak). The decay of the TRPL curves are fitted using a stretched exponential function. (b) Schematic showing an architecture comprising NQD absorbers embedded in a vertical array of high-mobility channels that allow nonradiative transfer of excitons from the adjacent NQDs and simultaneously provide high-mobility transport.[16]

The studies mentioned above were based on NQDs that were drop-cast onto semiconductor surfaces. In such situations, unprepared interfaces might have a substantial number of surface trapping sites that will facilitate exciton dissociation and subsequent charge trapping. This is especially important when time-resolved photoluminescence (TRPL) dynamics are recorded as a method of choice to register NRET signatures – faster dynamics of the emitting donor (NQD or molecule) species indicate an energy transfer channel. However, any other non-radiative channels such as interface charge trapping would similarly affect dynamics, thus hindering NRET effects. Further, drop casting does not allow for uniform layer deposition, thus providing for a multitude of the donor-acceptor distances, complicating interpretation of the PL lifetimes. Recently, several publications have achieved controllable positioning of monolayers of NQDs on Si surfaces, thus allowing for a quantitative determination of the elemental transfer rates. Nguyen *et al.* [21] discussed NRET from a monolayer of CdSe/ZnS NQDs controllably

grafted on a SAM-passivated Si surface. TRPL measurements revealed a progressive shortening of the PL lifetime of the donor NQDs as the separation from the acceptor Si surface decreased with ~$1/d^3$ dependence, confirming its dipole-dipole origin. The calculated NRET efficiency at 565 nm reached 65% with an interaction distance of about 4.4 nm. Extension of NRET to the near-infrared wavelength range was accomplished in Nimmo *et al.* [23], where a monolayer of CdSe or CdTeSe NQDs emitting between 545-800 nm was similarly grafted on thw Si surface. There, efficiency of NRET was found to decrease from ~70% to <50%, mostly owning to lower absorption of Si at longer wavelengths, as seen in Figure 2.2.

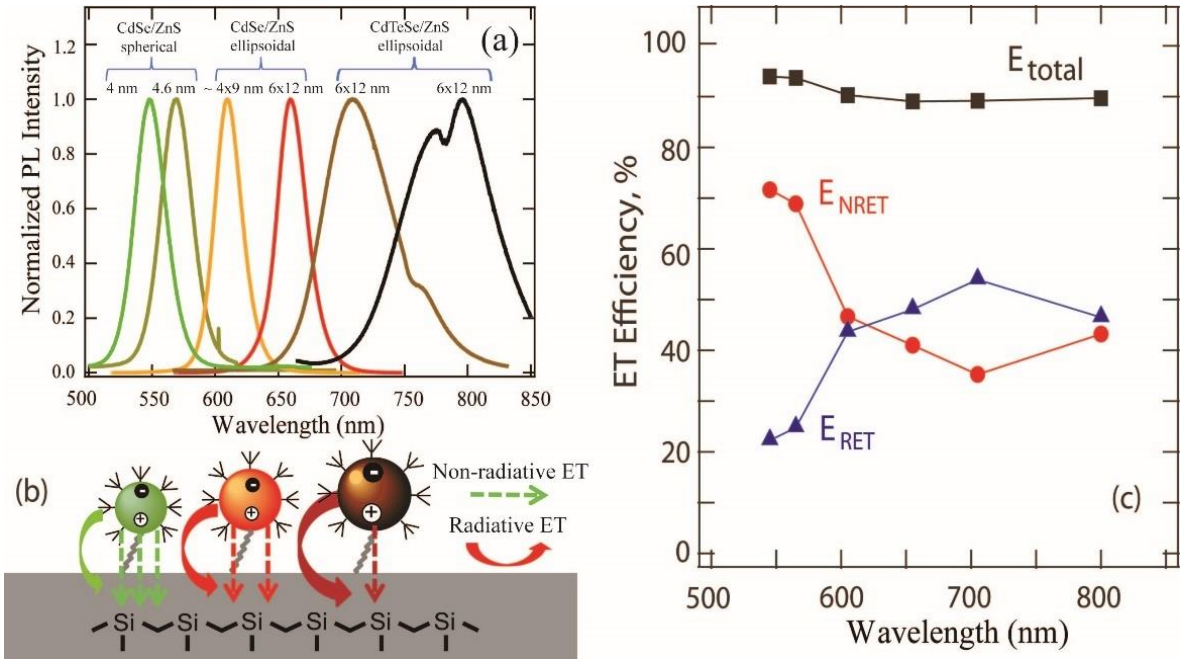


Figure 2.2. (a) PL emission spectra of different NQDs emitting from 545 to 800 nm as grafted on SiO_2. NQDs on Si exhibit the same PL profile. (b) Schematics of energy transfer from NQDs emitting at different wavelength to Si substrate. (c) Total ET efficiency (E_{total}) shown by black squares along with separate contributions E_{NRET} from NRET (red circles) and E_{RET} from RET (blue triangles).[23]

We would like to note that precise measurements of NRET rates were possible due to the fact that NQDs were grafted within a monolayer on the substrate, thus avoiding complications in the PL lifetime signatures that arise from a distribution of distances and associated NRET rates. Later on, another study of NRET was performed by Andreakou *et al*. [31] who drop casted PbS NQDs emitting at ~ 900 nm and obtained transfer efficiency estimated at 44%.

2.1.2 Radiative energy transfer to Si substrates

In addition to purely electrostatic dipole-dipole interaction that constitutes the NRET process, RET was experimentally demonstrated to be operative and very efficient across a wide wavelength range. This process involves the coupling of the donors' emission into the waveguide modes of the high-refractive-index semiconductor substrate. Nguyen *et al*. [18] used a monolayer of CdSe/ZnS NQDs grafted on thin Si nanomembranes (SiNM) of different thickness t =25-300 nm and varied the distance to Si as shown in Figure 2.3 (c). The PL lifetimes were observed to exhibit oscillating behavior as a function of the SiNM thickness as a result of the PL coupling to various waveguide modes (Figure 2.3 (a), (b)). The maximum RET coupling efficiency was observed for a SiNM thickness of *75* nm that corresponds to the half wavelength of the donor emission (vacuum emission wavelength λ_0*=565* nm) within the Si material. Overall, the ET efficiency to the SiNM was found to be around 90%, for the minimum NQD-to-Si separation (*d=4.4* nm), whereas the NRET efficiency was 58% and the RET 29%. The relative effects of these contributions were reversed at larger separation distances, due to the much larger effective length of the RET interaction ($d \sim 0.1\lambda_0$). At *d=12.6* m, the RET and NRET efficiencies were 52% and 21%, respectively, while at *d=18.6* nm, the RET efficiency was 57.5% and the NRET efficiency was only 5.5%. These results clearly indicate that 1) RET coupling is a major, long-

distance mechanism contributing to the overall ET and 2) the total ET to very thin SiNMs can be as effective as into bulk Si, but not at the expense of the latter.

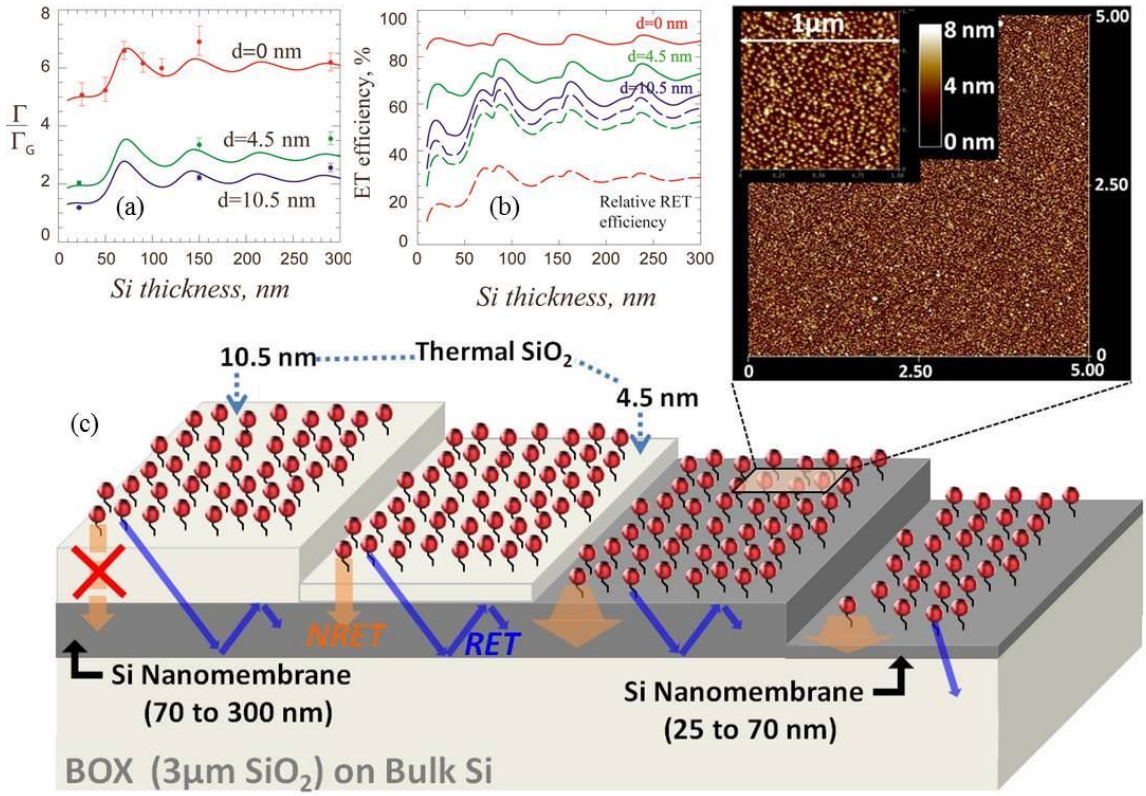


Figure 2.3. (**a**) Relative acceleration of the NQD exciton decay with respect to the reference glass sample as a function of the thickness, *t*, of the SiNM. The data points and theoretical curves are grouped by different values of the silicon oxide spacer thickness (*d*). The distance of the dipole emitter from the top surface is taken as z = 4 nm for the red theoretical curve and z = 3.7 nmfor the green and blue ones. The dielectric parameters of Si used for calculations are ε' =16.5 and ε'' = 0.32. Here the data points are shown with the reference τ_G = 22.8 ns. (**b**) Efficiency of ET into Si as extracted from the color-coordinated theoretical curves in panel (a). The solid lines correspond to the total ET efficiency [$(\Gamma_{RET}+ \Gamma_{NRET})/\Gamma$] and the dashed lines show the relative efficiency of ET just via waveguide modes in the SiNM (Γ_{RET}/Γ). (**c**) Schematics of different NQD/SiNM structures used to extract the relative participation of various decay channels: schematically displayed are NRET and RET processes from NQDs into the underlying Si slab as well as into SiO_2 substrate (on the rightmost structure). The role of NRET is strongly diminished with a thicker spacer (the leftmost structure), while the waveguide modes in Si are excited quite efficiently. (Top right) AFM images of NQDs attached via carboxy-terminated alkyl chains on an oxide-free SiNM surface. The 5x5 μm image emphasizes the homogeneity of the NQDs' monolayer attachment, while the 1x1 μm confirms the individuality of the NQDs to minimize interdot ET effects.[18]

Further detailed evidence of the emission coupling into the Si substrate was presented by Nguyen *et al*. [22], who studied the PL emission from CdSe/ZnS NQD monolayers on Si for separation distances of up to 500 nm. The authors observed clear oscillatory behavior of the PL lifetimes as a function of the separation distance due to the field interference effects. Strong directionality of the PL emission and its preferential coupling into the Si substrate was also demonstrated, confirming the effectiveness of the waveguide coupling mechanism.

2.2 Fundamentals of solar cells

Solar cells convert energy from light to electrical energy by photovoltaic energy conversion. Photons are absorbed by a semiconductor material which produces electron-hole pairs and eventually carrier separation and transportation. Typically, p-n junctions are used for carrier separation as an asymmetric semiconductor structure is needed. The electron density is higher in n-type region, whereas the hole density is higher in the p-type region., In a p-n junction under illumination, the number of electron-hole pairs produced by light absorption is proportional to the light intensity. Under illumination, the photo-generated excess electron-hole pairs use the electric field in depletion region for the drift of electrons towards the n-region and holes towards the p-region. Thus, the separation of carriers results in current flow when this illuminated p-n junction is electrically shorted. A schematic of photovoltaic energy conversion is shown in Figure 2.4 (a). The energy band diagram for the short-circuited and open circuited voltage is shown in Figure 2.4 (c) and (d), respectively. Current-voltage characteristic of a p-n junction in the dark and under illumination is shown in Figure 2.4 (b).

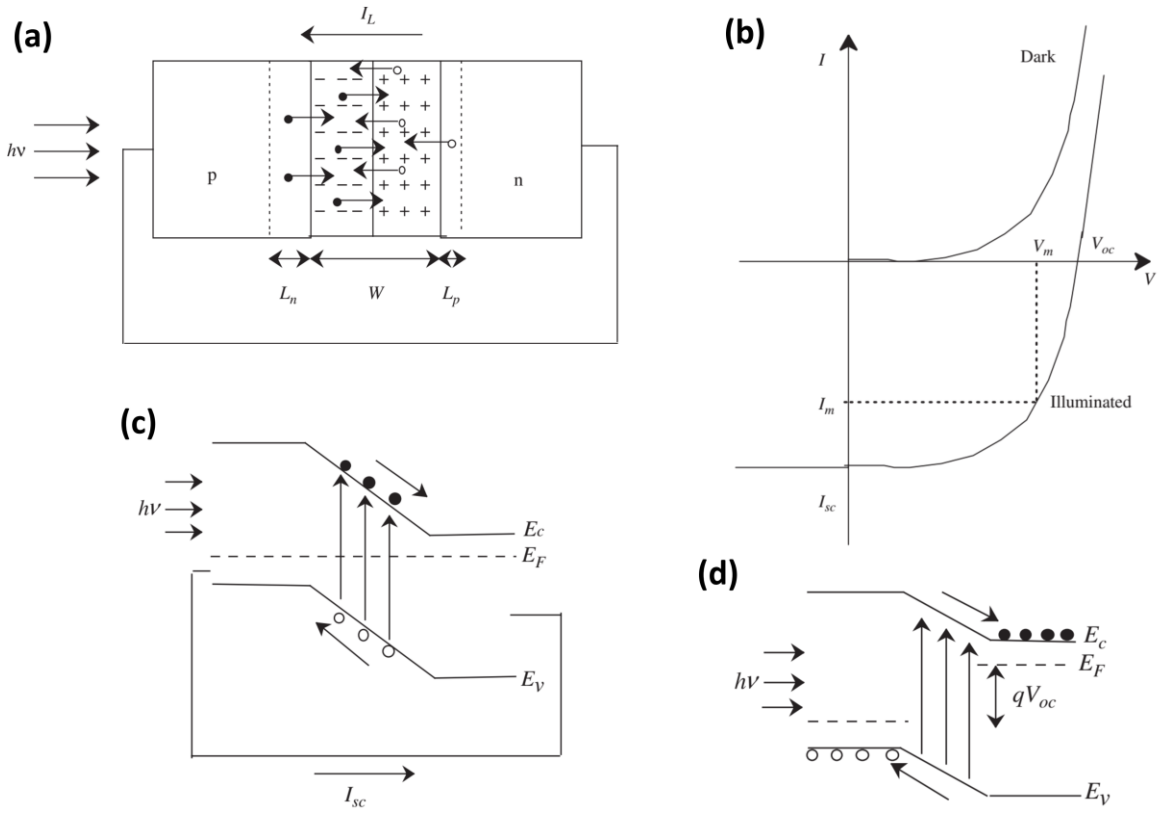


Figure 2.4. Schematic diagram (a) of a p-n junction under illumination, (b) the current-voltage characteristic of a p-n junction in the dark and under illumination, (c) a short-circuited current under illumination, and (d) open-circuited voltage.[39]

Four main parameters are extracted from the I-V graph of a solar cell under illumination. These are (i) the short circuit current density (J_{sc}), (ii) the open circuit voltage (V_{oc}), (iii) the fill factor (FF), and (iv) the efficiency (η). In general, the current density (mA/cm^2) is used to make the current independent of the illuminated area. Thus, comparison between devices with different areas is possible. When, the p- and n- region is short circuited under illumination, the current is called the short circuit current (I_{sc}) or short circuit current density (J_{sc}). J_{sc} is equal to the photo-generated current at zero series resistance. In the case of the open-circuit condition, the electron moves to the n-region and the holes move to the p-region. This condition generates a potential which is called the open circuit voltage (V_{oc}). The J_{sc} and V_{oc} are the maximum current density

and voltage from a solar cell, respectively. At these two-operating points, the power from a solar cell is zero. In this case, a parameter named the fill factor (FF) is used to determine the maximum power from a solar cell. The FF is defined as the following (equation 2.1),

$$FF = \frac{V_m I_m}{V_{oc} I_{sc}} \qquad (2.1)$$

and can be observed as a rectangle fitted inside the 4th quadrant of the I-V curve measured under illumination (Figure 2.4 (b)). The last parameter extracted from the I-V curve of a solar cell under illumination is the efficiency (η). η is defined as the ratio of output power to input power. The maximum power that can be achieved from a solar cell is given by equation 2.2

$$P_{max} = V_{oc} I_{sc} FF \qquad (2.2)$$

Then the efficiency can be calculated by the following relationship (equation 2.3),

$$\eta = \frac{V_{oc} I_{sc} FF}{P_{in}} \qquad (2.3)$$

Most solar cells are measured under AM1.5 condition at 25 ^{o}C temperature. In this case, the input power (P_{in}) is 1 kW/m^2 or 100 mW/cm^2. The other three parameters (V_{oc}, I_{sc} and FF) need be increased to increase efficiency of a solar cell.

The maximum theoretical efficiency for a single junction solar is given by the Schokley-Queisser limit [12]. This was calculated by finding the exact electrical energy that can be extracted for each incident photon. The Schokley-Queisser limit for a single junction solar cell with a bang gap (E_g) of 1.4 eV (for AM1.5 solar spectrum) is 33.7%. The calculation was done for $E_g = 1.4\ eV$ because the solar radiation modeled as a 6000 K blackbody radiation peaks at 1.4 eV. The Schokley-Queisser efficiency calculation is dependent on the band gap. While silicon is close to this band gap ($E_{g_{Si}} = 1.12\ eV$), there are several mechanisms that are

responsible for the low efficiency limit for an ideal solar cell. A schematic of these losses associated with an ideal solar cell is shown in Figure 2.5.

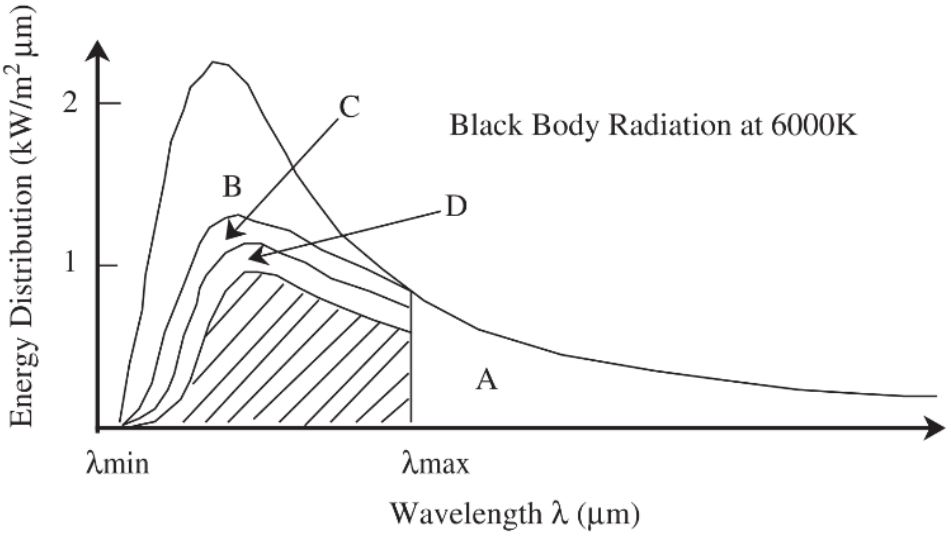


Figure 2.5. Schematic of energy losses in an ideal solar cell. 'A' is related to energy that is not absorbed by the semiconductor. 'B' deals with thermalization loss to the band edge, (i.e. loss of excess energy after absorption). 'C' is loss associated with voltage and 'D' is loss associated with the fill factor.[39]

The open circuit voltage is always smaller than E_g as the Fermi level resides inside the band gap. Thus, p-n junctions cannot fully utilize the maximum voltage and hence some efficiency is lost (marked as 'C' in Figure 2.5). The FF is always less than unity, and thus some efficiency is also lost (marked as 'D' in Figure 2.5). Also, light can pass through the solar cell if the cell does not have enough thickness to absorb the whole solar spectrum (marked as 'A' in Figure 2.5). In the case of a real solar cell, in addition to these losses there are other losses such as reflection loss, recombination loss, series and shunt resistance loss etc. Combination of all these losses result in the lower efficiency (η) of real solar cell than the ideal cell.

The effect of series and shunt resistance on the solar cell is shown in Figure 2.6 (a) using a simple equivalent circuit based on single diode model. In general, the effect of series and shunt

resistance can easily be observed from decreased FF values. Series resistance is associated with the resistance of the bulk, interfaces, interconnects and contacts etc. Shunt resistance is associated with lattice defects and leakage current at the edges of the solar cell. To increase efficiency, the shunt resistance should be high (low defects) and series resistance should be low (high quality interfaces, low doping etc.).

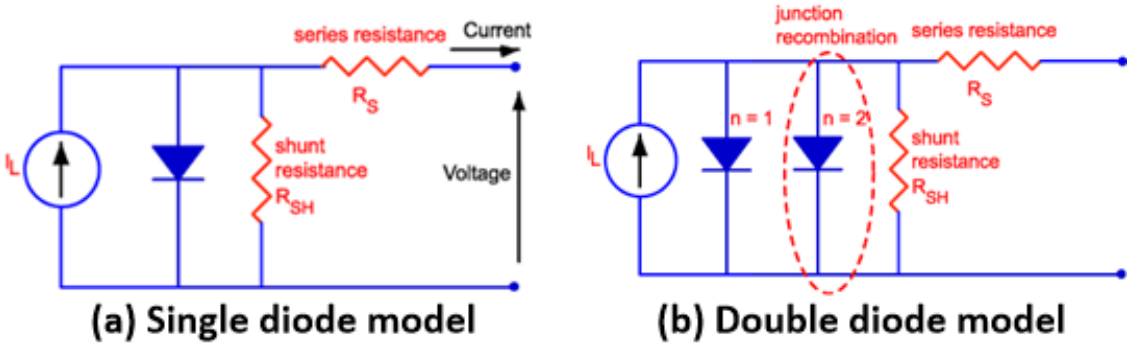


Figure 2.6. Equivalent circuit of the solar cell showing both series and shun resistant for (a) one and (b) two diode model.[40]

In the ideal case, the p-n junction is modeled as a single diode and the ideality factor (n) is 1.0. However, in real cases, the diodes behave non-ideally and the ideality factor is >1. 0.. The ideality factor is 2.0 if the diode characteristic is dominated by trap states inside the depletion region. The schematic diagram of a two-diode mode is shown in Figure 2.6 (b). However, modeling can become particularly difficult if the devices are not well made. In that case, high ideality factors (n>2) can be observed. The reason behind such deviation can be rationalized by considering presence of multiple rectifying junction at the interfaces.

CHAPTER 3

EXPERIMENTAL METHODS

The primary experimental techniques and associated tools that were used in this work are described briefly in the following section. It is encouraged to look in the references provided herein for detailed descriptions of the techniques.

3.1 Deposition techniques

3.1.1 Low pressure chemical vapor deposition (LPCVD)

LPCVD is a type of chemical vapor deposition (CVD) process. In general, in the CVD process gases react on a solid surface to produce solid phase of material. The source materials are gases and the byproducts after deposition are pumped away. The deposition rate is around 0.1-10 nm/s. In a typical CVD process (see Figure 3.1 (a)), (i) the reacting source material in gaseous form transports or diffuses to the surface, (ii) then adsorption or chemisorption occurs on the surface, (iii) afterwards heterogeneous surface reaction is initiated, (iv) then desorption of reaction byproducts occurs and (v) finally, byproducts of the reaction are transported away from the surface. CVD processes depend on both the chemical reaction on surface and the flow of the reaction gases. LPCVD is mainly used for depositing polysilicon, silicon oxide, and silicon nitride films. The thickness of the film can be varied from 2 nm to 5 μm. Figure 3.1 (b) shows a schematic of a typical LPCVD chamber. Low pressure (~250 mTorr) and high temperatures (600 °C to 900 °C) are used for deposition. Thermal decomposition of the precursor gases leads to solid film formation on the wafer surface. Quartz is used as furnace tube to withstand the high temperatures. Wafers are usually loaded horizontally on the boat which allows the gas to come in

direct contact with the surface. Multiple wafers can be loaded on a single boat. The typical reaction that occurs in the LPCVD of poly Si is the following:

$$SiH_4(g) \rightarrow Si(s) + 2\,H_2 \quad [Deposition\ temperature\ is\ 625\ ℃$$

An example of a deposition is described. First, Si are cleaned according to standard Si cleaning procedures to remove any impurities and to limit chamber contamination Si wafers. The furnace temperature is gradually increased from the standby temperature (400 ^{o}C) to the set point. Then gases are flown over the wafers at high temperature and low pressure to from thin films of poly Si. For n-doped poly Si deposition, 15% phosphene (PH_3) at a flow of 80 sccm is flown into the chamber in addition to 150 sccm SiH_4 at 250 mTorr. After deposition, by product gases are pumped out and the chamber is gradually cooled to 100 °C before unloading. A major disadvantage of LPCVD is that the furnace needs to be maintained at high temperature thus limiting the range of materials that can be used in the furnace (for example: Aluminium (Al) cannot be used due to its low melting point ~ 650 ºC).

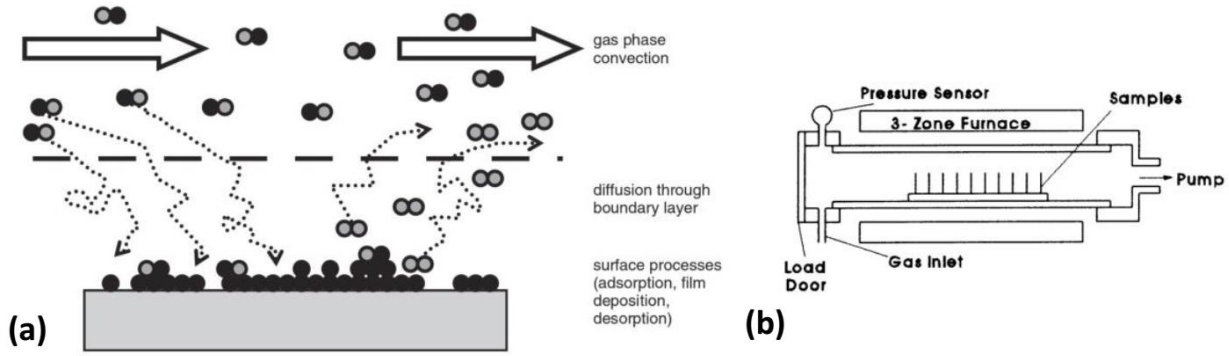


Figure 3.1. (a) Typical steps in a CVD process for film deposition of film.[41]. (b) schematic of a LPCVD chamber.[42]

3.1.2 Plasma enhanced chemical vapor deposition (PECVD)

PECVD is a type of chemical vapor deposition technique that is useful for depositing thin films of oxide, nitride, and carbide etc. at lower temperatures (typically < 300 ºC) which are suitable for materials with low melting points. In PECVD, source gas decomposition and deposition is enhanced by a plasma which enables lower temperature deposition. Additionally, the pressure, temperature, flow rate, flow rate ratio and radio frequency (RF) power can be varied. The results in reposition rates that range from 0.1-10 nm/s [43].

In PECVD, the sample is placed on the heated bottom electrode of a parallel-plate diode reactor (see Figure 3.2 (a)). The source gases are introduced from the top and pumped out from the bottom. The operating frequency can be varied from 400 KHz to 13.56 MHz. The RF power can be applied to both the top and bottom electrodes. Thus, the frequency, duty cycle and power can be different for the two electrodes. When low frequencies (i.e. 400 KHz) are applied, ions can follow the field electric and ion bombardment occurs. At 13.56 MHz, the frequency is high enough that only electrons can follow the field and thus ion bombardment is reduced. It important to note that the ratio of 13.56 MHz power to KHz power is tailored to reduce the stress in the deposited film.

The PECVD (Plasma-Therm 790) tool in the UTD cleanroom (Figure 3.2 (b)) is configured with 2% silane in helium and can deposit film at temperatures from 100 ºC to 300 ºC. This tool is predominantly used to deposit PECVD silicon oxide and silicon nitride films. The basic reactions are the following:

$$PECVD\ SiO_x\colon\ SiH_x + N_2O\ \rightarrow\ SiO_x\ (+H_2 + N_2)$$

$$PECVD\ Si_xN_y\colon SiH_x + NH_3\ \rightarrow\ Si_xN_y(+H_2)$$

PECVD SiO_2 recipe: Temperature-250 ºC, Pressure-900 mTorr, Power-50 W, 2% SiH_4-400 sccm, N_2O-900 sccm, N_2-0 sccm, He-0 sccm, deposition rate-39.6 nm/min.

PECVD low stress Si_xN_y recipe: Temperature-250 ºC, Pressure-900 mTorr, Power-100W, 2% SiH_4-200 sccm, NH_3-4 sccm, N_2-200 sccm, He-600 sccm, deposition rate-11.3 nm/min.

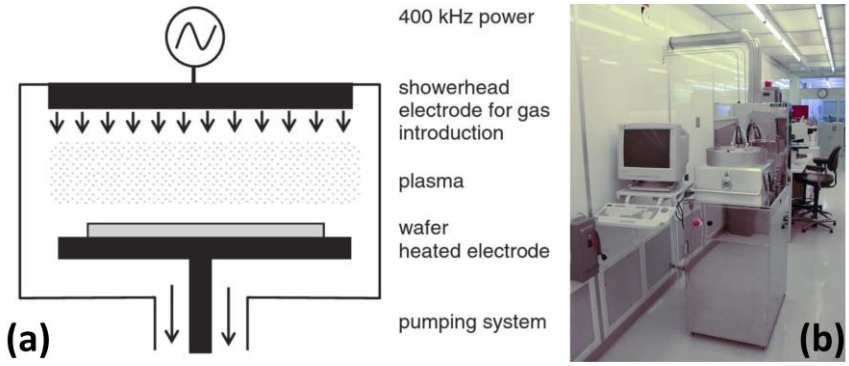


Figure 3.2. (a) Schematic of a simple parallel-plate diode PECVD reactor.[43]. (b) Image of the Plasma-Therm 790 PECVD in the UTD clean room.

3.1.3 E-beam evaporation

Electron beam evaporation is a type of physical vapor deposition (PVD) technique. In general, the evaporation of metal is a straightforward process where a filament generates an beam of electrons which is guided through electric and magnetic field to a target where the metal is vaporized. The evaporated atoms are then transported to the substrate under vacuum (Figure 3.3 (a)). The deposition rate is usually 0.1-1 nm/s [43]. The deposition is done either in high vacuum (HV) or ultrahigh vacuum (UHV). Typically, the best UHV processes have 10^{-11} Torr base pressure (but the deposition herein was done typically at a base pressure of $5x10^{-6}$ Torr). In the case of UHV, collisions between the evaporated atoms do not occur due to the large mean free path (MFP) of the evaporated atoms and thus the transportation path of the atoms is line-of sight route. In this case, planar surfaces are well covered while the sidewalls of nanostructures

are poorly coated. The evaporated atoms arrive at thermal speeds and thus contribute to the deposition temperature. Unlike the evaporation of metals, alloy and compound deposition is a complicated process as the component with higher vapor pressure evaporates more readily and thus the film composition can be very different than desired. Additionally, compounds can decompose at high temperatures. Therefore, there are limitations and restrictions to the conditions which certains metals, alloys, and compounds can be evaporated. For instance, refractory metals such as Mo, Ta, W, graphite can be deposited but care must be taken to prevent decomposition.

However, for elemental metals such as Au, Al and Ti, e-beam evaporation is the easiest processes to form thin films. The quality of thin metal films prepared by e-beam evaporation is good. However, only a few parameters are available to tailor the properties of the deposited film. For instance, substrate heating can facilitate desorption of impurity atoms and subsequent diffusion of evaporated atoms to favorable lattice sites. Stage rotation can assist is depositing metals on the sidewalls of nanostructures.

In the UTD cleanroom, there are three different e-beam evaporation tools and each serves a different purpose. The CHA e-beam evaporation tool (Figure 3.3 (b)) is used for side wall coverage by using a planetary accessory. The chamber is big and thus it takes a long time to reach the deposition pressure (i.e., 5×10^{-6} Torr). The Cryo e-beam deposition tool (Figure 3.3 (c) and the Temescal (Figure 3.3 (d) are used regularly for deposition of metals on planar surfaces. The substrate holder (i.e., the stage) is usually stationary, however, the stage in the Temescal can rotate. Temescal reaches desired vacuum level quickly due to small chamber size but can't be used for refractory metal such Mo, W etc. deposition as the chamber gets extremely

hot during deposition and leads to complications. Instead, these are deposited in the Cryo e-beam where the overall temperature is less effected during the depositions process.

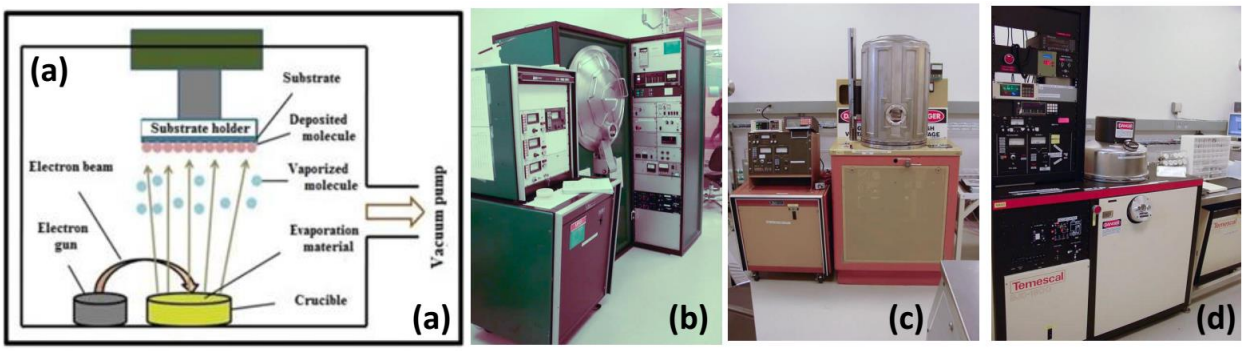


Figure 3.3. (a) Schematic of electron beam evaporation.[41]. Images of the (b) CHA-50 evaporator (planetary accessory for sidewall deposition), (c) Cryo e-beam evaporator (stage is stationary) and (d) Temescal e-beam evaporator (stage rotation available) in the UTD cleanroom.

3.2 Etching by plasma processes

Plasma etching is one of the most widely used methods in the semiconductor industry. In principle, plasma is an ionized gas which consists of free electrons, ions, radicals and neutral species. Energy needs to be supplied to create and sustain plasma. External electromagnetic is used for such energy transfer to the plasma constituents. In the case of an inductively coupled plasma (ICP), a radio-frequency (RF) source delivers energy to the plasma. The time varying magnetic field introduces an electric field that circulates the plasma. This results in collisions between fast moving electrons and slow moving ions which cause further ionization of the plasma. The electrons are lost through the chamber walls creating a static voltage termed plasma voltage which is different from a bias voltage. In an inductively coupled system, the ion density and other plasma parameters can be changed without drastically changing the incident ion energy on the sample.

Plasma processing was used extensively while developing processes described in chapter 5. Particularly, inductively coupled plasma reactive ion etching (ICP-RIE) using both fluorine and chlorine based chemistry was utilized for Si etching. A benefit of plasma processes is that they achieve high fidelity in terms of pattern transfer. However, to achieve such high precision careful control of the etch rate, uniformity, selectivity, anisotropy and sample quality need to be taken into consideration. Also, the processing environment can induce detrimental effects such as heating (or cooling) of the sample which can effectively lead to delamination of thin films (due to thermal expansion coefficient mismatch between layers). Minimizing thermal fluctuation is a big concern in the semiconductor industry. Figure 3.4 shows a schematic of an ICP-RIE system.

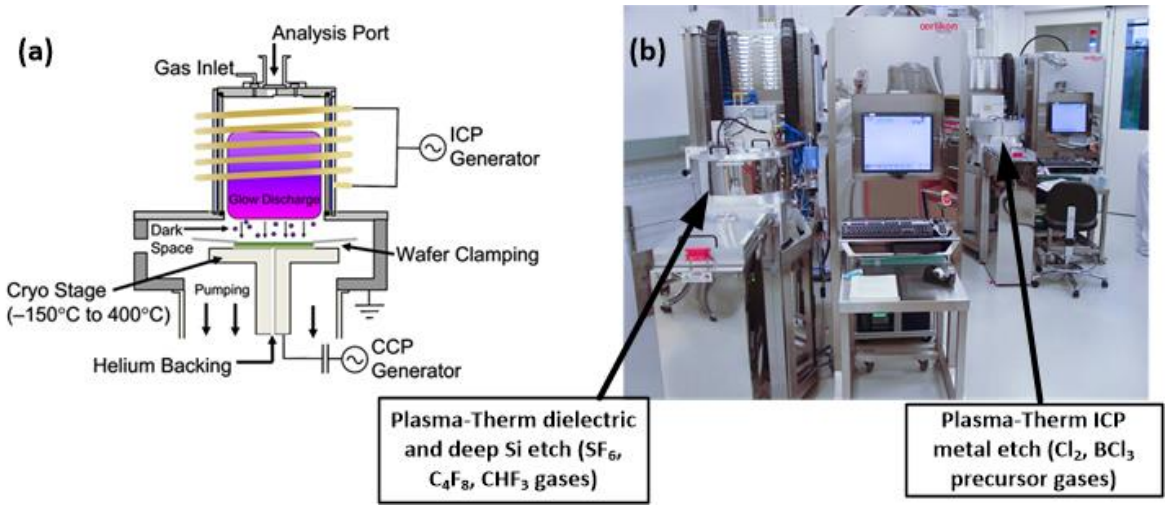


Figure 3.4. (a) Schematic of an ICP-RIE tool.[44]. (b) Image of the plasma processing tools used in the UTD cleanroom.

An added benefit of ICP-RIE is that in contrast to wet etching which results in isotropic etching it can be modified for anisotropic etching. This is particularly attractive for pattern transfer. By depositing a passivating or inhibitor layer on the sidewalls during the plasma

processes enables an anisotropic etching profile. The Bosch silicon etch process uses such an approach and has been used extensively in this work to removal the Si handle of the silicon-on-insulator (SOI) wafer. The Bosch Si etch process is a time-multiplexed processing technique where the Si is etched in one cycle followed by an immediate passivation cycle to protect the sidewalls. This is achieved by using alternating plasma steps. In this process, the samples is exposed to SH_6 (sulfur hexafluoride) gas for a very short period to etch the Si and then the gas and plasma valves are rapidly closed. Then next step exposes the sample to another plasma and C_4F_8 (octafluorocyclobutane) which serves as the passivation gas for sidewalls. This alternating sequence is continued for the entire processing time. The fast alternating cycles create "scallops" or "notches" on the sidewalls which can be controlled (but not fully avoided) by changing the duty cycle between the steps as well the total duration of the two steps. Selection of mask and i thickness also plays important role as the mask interacts with the gases and plasma during the etching processes. This results in the mask gradually eroding and thus the fidelity of the transferred pattern can gradually decrease.

In an ICP system, the main controllable parameters include: ICP power, forward power, temperature, chamber pressure and gas flow rate. The etch rate, selectivity, sidewall profile and edge roughness are controlled by optimizing these parameters. Regular cleaning of the chamber (i.e. conditioning of chamber) by O_2 plasma is important to maintain a constant etch rate and profile. Micro-masking can happen due to re-deposition of residual etched molecules on the sidewalls and thus can affect the overall etch behavior. If possible, O_2 cleaning should be done between processing steps. The effects of the different parameters are described below:

(i) ICP power: This controls the ionization energy of the gas and depends on both the gas flow and chamber pressure. The number of ions are increased with increasing ICP power which increases the etch rate in both the vertical and lateral direction. Increased ICP power can lower mask selectivity in addition to reduced sidewall passivation.

(ii) Forward power: Increasing the forward power increases the electric field between the plasma and substrate electrodes. This results in the higher momentum ions and thus the silicon milling rate increases. However, there is also a slight increase of etching in the lateral direction. Increasing the forward power reduces mask selectivity and results in rapid erosion of the mask.

(iii) Chamber pressure: The amount of gas is controlled by the changing chamber pressure. This controls the amount of ionization which influences the etch rate and mask selectivity.

(iv) Gas flow rate: Optimization is necessary to control the etch rate and selectivity for a certain process.

In the case of nanoscale etching of Si, the Bosch process is unsuitable due to poor sidewall structuring. For the ICP-RIE etching of nanostructures such as Si nanopillars, nanowires etc. a low etch rate is often necessary to achieve smooth and controllable sidewalls with limited undercutting. Mixed mode gas chemistries are used to achieve this. Unlike the actual Bosch process C_4F_8 is simultaneously used with SF_6 during Si etching to achieve an overall slow etch rate. Therefore, an ICP system provides enormous versatility to achieving different etching goals.

3.3 Characterization techniques

Several materials characterization techniques are employed in this study. The most relevant ones are briefly introduced in the following section. Scanning electron microscopy (SEM) is used to look at the surface morphology as well as the cross-section of sample to estimate the film thickness. Atomic force microscopy (AFM) is used to measure the surface roughness and film thickness. SEM cross-section images are difficult for very thin films (i.e., 1-2 monolayers of NQDs) and therefore AFM is appropriate for those situations. Spectroscopic ellipsometer (SE) is used to determine the thicknesses of deposited poly Si, oxide and nitride films. SE is also used to determine the refractive index (n) and extinction coefficient (k) of deposited layers. Profilometry is a AFM type of tool used to find step heights after etching. A four-point probe is used to extract the doping concentration of the poly Si layers.

3.3.1 Scanning electron microscope (SEM)

SEM is one of the most widely used electron microscopes. It provides an image of the microscopic structure of a surface containing topological and compositional information by scanning a focused electron beam across the surface. In an SEM, electrons ranging in energy 1-40 KeV are emitted from an electron gun and then guided and focused onto a spot size of ~1 nm using a combination of electromagnetic lenses. The focused beam is rastered across a sample and the electrons emitted from the surface, either secondary or back-scattered, are collected by a special detector, which is then amplified and reconstructed into an image. A schematic of an SEM is shown in Figure 3.5 (a).

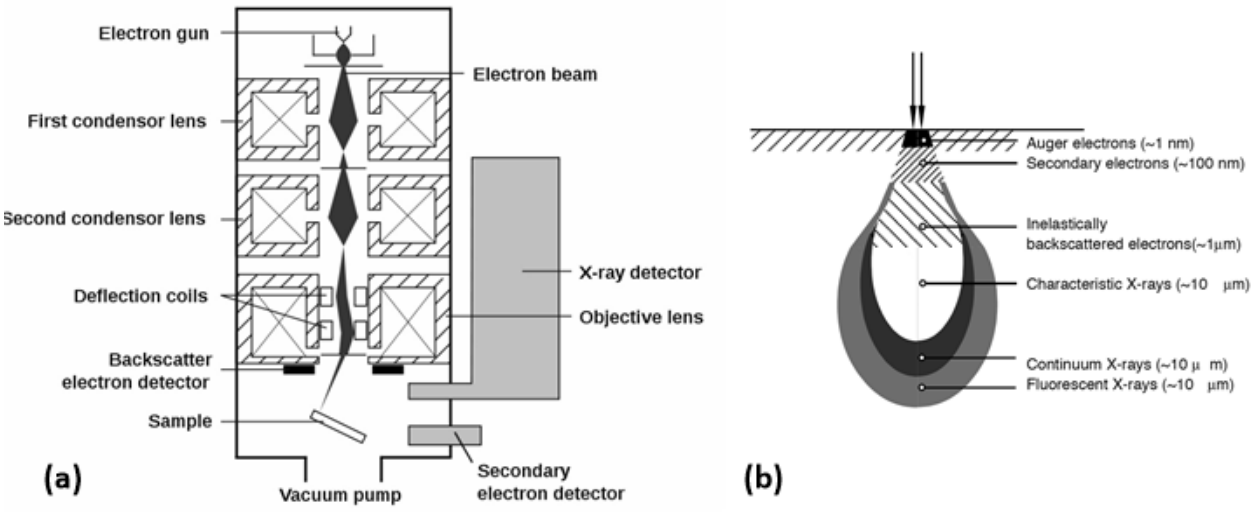


Figure 3.5. Schematics of (a) a scanning electron microscope.[43] and (b) interaction volume of electron and specimen atoms.[45]

SEM is operated to detect either secondary electrons (SE) which provide topographical information of the sample or back-scattered electrons (BSE) which also provide elemental compositional information. In electron microscopy, knowledge of the interaction volume of the electron with the samples atoms is important to understand spatial and depth resolution. The interaction volume of electrons shown in Figure 3.5 (b) clearly indicates that SEs have better spatial resolution compared to BSEs.

Sample preparation for the SEM is easy and samples simply need to be conductive. However, insulting samples can be imaged by depositing a thin layer of conductive film (i.e. Au) on top of the insulating sample. In all cases, one major source of contamination in SEM is the existence of hydrocarbon molecules in the samples which often leave dark spots on the SEM images due to decomposition of the hydrocarbon under the focused electron beam.

The Zeiss Supra 40 SEM in the UTD cleanroom facility can reach a spot size of 1-2 nm. Additionally, this SEM is equipped with energy dispersive X-ray spectrometer (EDAX) for mapping the elemental composition on the sample.

3.3.2 Atomic force microscope (AFM)

Atomic force microscopy is a type of scanning probe microscopy (SPM) that obtains a true image of the surface and provides angstrom (Å) scale resolution in the vertical direction (~ 0.1 nm). However, lateral resolution is poor in comparison as it is limited by the shape of the probe tip. A sharp tip (probe) is mounted on a cantilever and used to generate a surface topographical image. AFM can be operating in several modes including tapping and contact. Tapping mode is the most common.

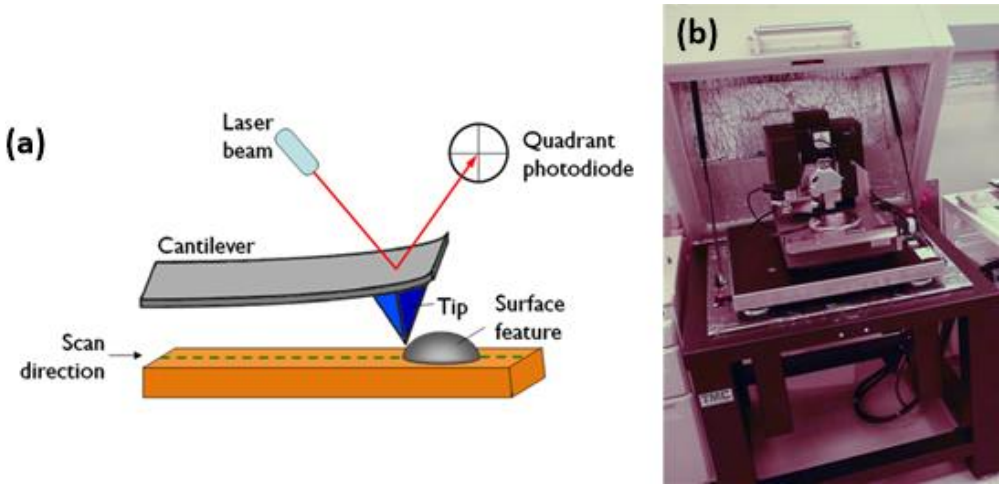


Figure 3.6. (a) Schematic of the working principle of atomic force microscope (AFM).[46] (b) Image of the Veeco Model 3100 AFM.

A schematic of the working principle of AFM is illustrated in Figure 3.6 (a). In tapping mode, the tip does not touch the sample's surface, rather the cantilever is positioned very close to the sample surface and the cantilever oscillates near it's resonance frequency. A laser beam is

focused on top of the cantilever. A s the tip is rastered across the surface, the cantilever is deflected due to near-field forces between the tip and the surface atoms. Any deflection of the cantilever causes a change in the reflection of the focused laser beam. A position sensitive photo-diode sensor tracks the change in the reflected laser beam and produces a topographical image of the scanned surface. A feedback loop is keep the distance between the tip and sample constant. In addition to topographical information, phase data is simultaneously collected. The phase lag present in the cantilever with respect the initial signal can reveal important information about composition, adhesion, friction and viscoelasticity of the surface.

In this work a Veeco, Model 3100 Dimension AFM was utilized for the measurements (Figure 3.6 (b)).

3.3.3 Spectroscopic ellipsometry (SE)

Ellipsometry is a non-destructive optical technique that is widely used to characterize the optical properties of thin films. It is an effective technique to characterize thin films both *in-situ* and *ex-situ*. In ellipsometry, the change in polarized light after reflection (absorption, scattering, transmission) from the surface is measured. Figure 3.7 shows a schematic of major components of a SE. In brief, unpolarized light (either a single wavelength or range from UV-infrared) is passed through a polarizer to linearly polarize the light before shining on the sample. The reflected light is then passed through an analyzer to determine its polarization before passing through a detector. In ellipsometry, the amplitude ratio (ψ) and phase difference (Δ) between the p-and s-polarized light are measured. Using this, an optical model is created to calculate the properties of interest (i.e., complex refractive index, complex dielectric function, absorption coefficient, band structure etc.).

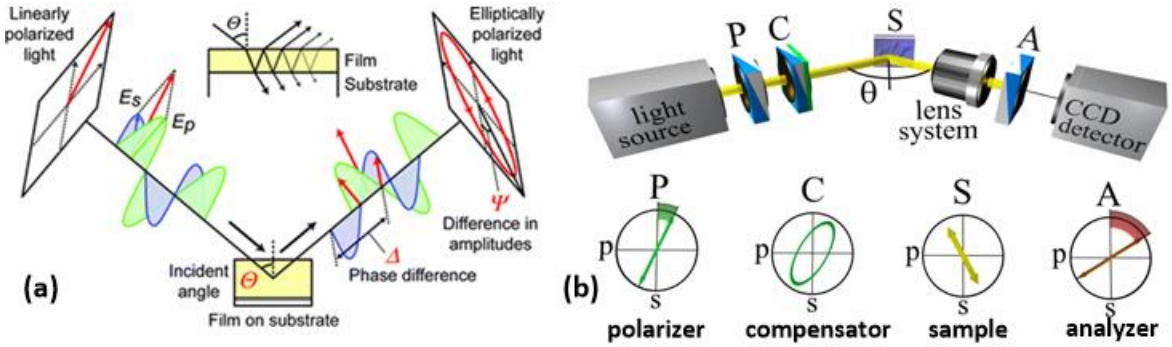


Figure 3.7. (a) Working principle of spectroscopic ellipsometry.[47] and (b) schematic of major parts of the ellipsometry tool.[48]

The advantages and disadvantages of SE are described in Table 3.1. Overall SE is a beneficial tool and can achieve very high resolution (~ 0.1 Å) in terms of measuring thickness.

Table 3.1. The advantages and disadvantages of using spectroscopic ellipsometry.[49]

Advantages:	High precision (thickness sensitivity: ~0.1 Å)
	Nondestructive measurement
	Fast measurement
	Wide application area
	Various characterizations including optical constants and film thicknesses are possible
	Real-time monitoring (feedback control) is possible
Disadvantages:	Necessity of an optical model in data analysis (indirect characterization)
	Data analysis tends to be complicated
	Low spatial resolution (spot size: several mm)
	Difficulty in the characterization of low absorption coefficients ($\alpha < 100\,cm^{-1}$)

During the measurement, it very important to choose proper incident angle (typically 70° for semiconductors) as the sensitivity of the measurement depends on incident angle. However, normal incidence is not possible as the s-and p-polarized light become indistinguishable. Additionally, the surface roughness cannot be too large (within ~30% of the incident light's wavelength), otherwise scattering hinders the sensitivity of the reflected light. In contrast to SEM and AFM which measure areas on the order of microns, SE has low spatial resolution as the spot size is 1-2 mm and elliptical in shape. In this project, the UVISEL spectroscopic ellipsometer by

Horiba Scientific was used. The wavelength range for this instrument is 190-2100 nm. The spot size can be varied from 0.1-1.2 mm. The film thicknesses which can be measured range from 1 Å - 30 µm.

3.3.4 Reflectance measurement

It is important to measure the surface reflectance for solar cells in addition to transmittance and absorbance. Reflectance measurements are performed from 250 - 2500 nm. There are two types of reflection: (i) specular and (ii) diffuse (see Figure 3.8 (a)).

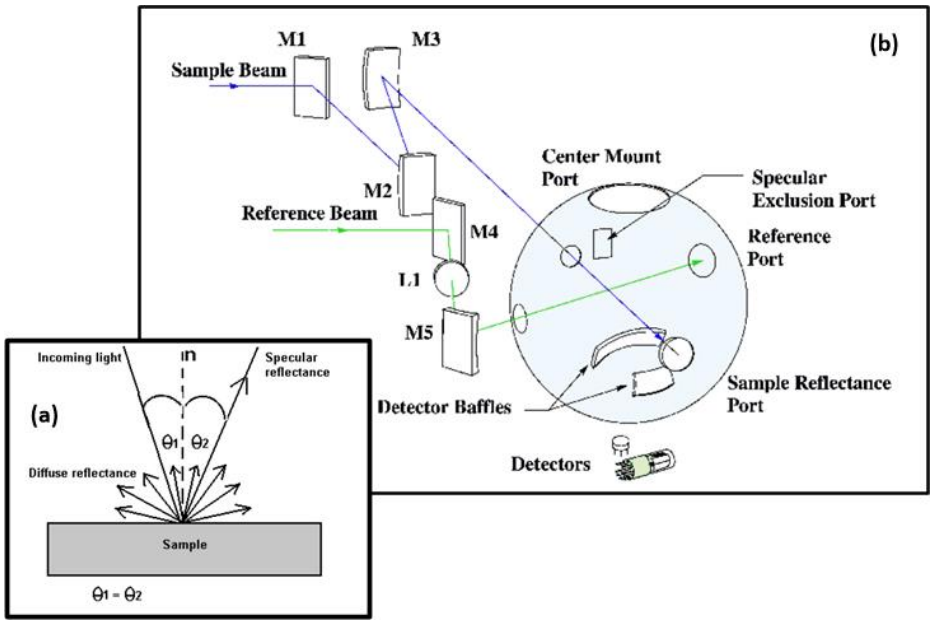


Figure 3.8. (a) Schematic showing specular and diffuse reflectance. (b) Schematic of an integrating sphere (diffuse reflectance accessory (DRA)) used for Cary 5000 UV/VIS/NIR spectrometer.[50]

Diffuse reflection occurs when the light is reflected in many different directions which happens on rough surfaces. In contrast, specular reflection occurs on smooth (mirror like) surfaces and the angle of reflection is equal to the angle of incidence. Most materials (films) exhibit a combination of diffuse and specular reflection which can be measured using an

integrating sphere. A diffuse reflectance accessory (DRA) for a Cary 5000 UV-VIS-NIR spectrometer was used in this work and can perform reflectance measurements on diffuse, specular or mixed samples. The reflectance of a sample is measured relative to a polytetrafluoroethylene (PTFE disk). A schematic of the integrating sphere for Cary 5000 spectrometer is shown in Figure 3.8 (b).

3.3.5 Profilometer

A profilometer is used to measure the surface profile of a sample and can determine step height as well as surface curvature or flatness. The UTD cleanroom has a Veeco Dektak VIII Prolifometer. It is stylus type profilometer, where a probe moves along the surface to measure surface height using force feedback. The tip of the probe physically touches the surface and thus precaution is needed for measuring soft and sensitive samples. The tip size and shape is an important parameter as it influences the of lateral resolution as well as vertical sensitivity. The instrument in cleanroom uses a stylus of 12.5 µm radius and shown in Figure 3.9.

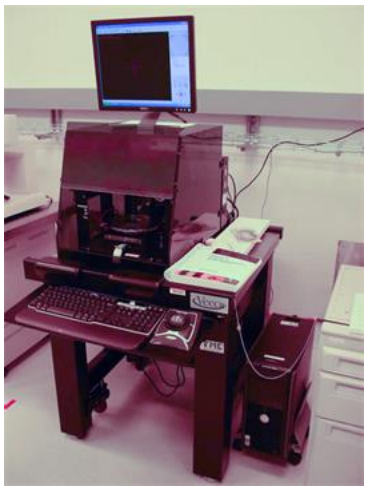


Figure 3.9. Veeco Dektak VIII Prolifometer at UTD cleanroom.

3.3.6 Four-point probe

A four-point probe used to measure sheet resistance of thin films deposited by different techniques. Resistivity, ρ, is an important measurement as it relates directly to dopant concentration. In this method, four probes are collinearly placed to make contact with the sample as shown in Figure 3.10. Current (I) is passed through the outer two probes and the corresponding voltage (V) is measured in between the inner probes. If the probes are uniformly spaced, the distance between the probes is denoted by s and the resistivity is given by eqs 3.1 and 3.2

$$\rho = \frac{2\pi s V}{I}\ \mu\Omega - cm\ for\ t \gg s \qquad (3.1)$$

$$\rho = \left(\frac{\pi t}{ln2}\right) * \frac{V}{I}\ \mu\Omega - cm\ for\ s \gg t \qquad (3.2)$$

In the above equations, t = thickness of thin layer. The sheet resistant, R_s, for shallow layers of semiconductors is thus given by equation 3.3,

$$R_s = \frac{\rho}{t} = \left(\frac{\pi}{ln2}\right) * \frac{V}{I} = 4.53 * \frac{V}{I}\ \mu\Omega - cm\ for\ s \gg t \quad (3.3)$$

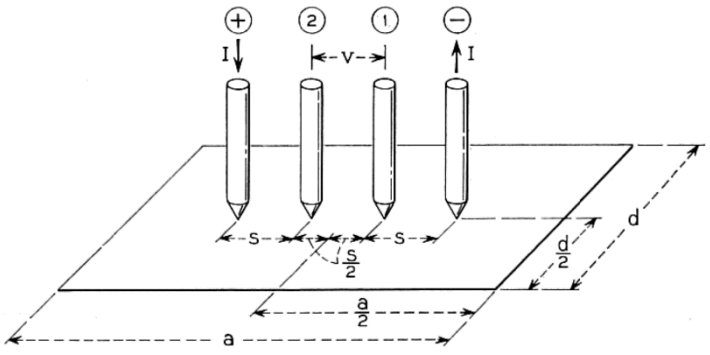


Figure 3.10. Schematic diagram of a four-point probe measurement.[51]

The probes must make ohmic contact with the sample and thus only thin films (10 nm -1 μm) can be measured. For this work, an Alessi manual 4-point probe with tungsten carbide probes placed 1 mm apart was used in the UTD cleanroom.

3.4 Electrical measurements of the fabricated devices

The photovoltaic measurements (both the dark and 1 Sun AM 1.5G illumination) were done inside a N_2 glove box in Dr. Jason Slinker's lab. Figure 3.11 (a) shows a schematic of the measurement setup and Figure 3.11 (b) shows the schematic of the Newport 9600 solar simulator. A Newport 96000 150 W solar simulator was used for illumination. The system has a 150 W Xenon Arc lamp with a power supply that delivers constant power to the lamp. In principle, the simulator produces a collimated beam that is ~3.3 cm in diameter, but only a 15 mm spot in the middle of the beam has less than 5% variation in intensity. Devices were carefully positioned to minimize intensity variations. I-V measurements were carried out using a HP 4155A semiconductor parameter analyzer that was controlled by LabView. This is a versatile instrument that that measures current from 1 fA to 100 mA and voltage from 1 μV to 100 V. The I-V sweep measurements were done in DC mode. A Si reference cell was used every time for calibration. The output of the reference cell is 22 mA/cm^2 under 1 Sun AM 1.5G illumination. Therefore, the power of the light source was adjusted to get the desired output from the reference cell before proceeding with sample measurements.

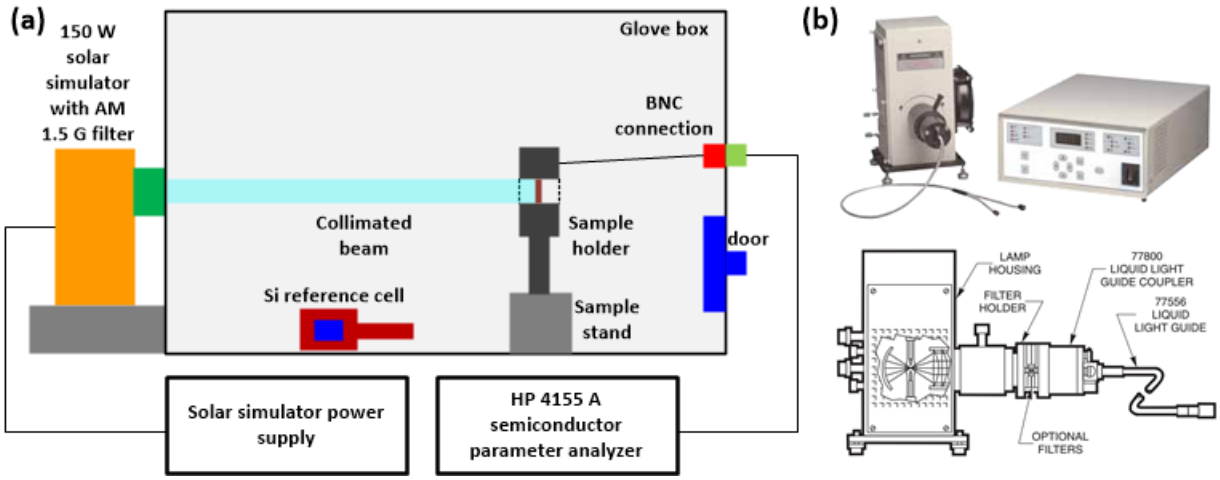


Figure 3.11. (a): Schematic of the solar cell measurement setup inside a glove box. (b) Newport 9600 solar simulator with power source.[52]

External quantum efficiency (EQE) measurements were done in collaboration with Dr. Liang Xu in Dr. Julia P. Hsu's laboratory. A schematic of a generic EQE measurement system is given in Figure 3.12.

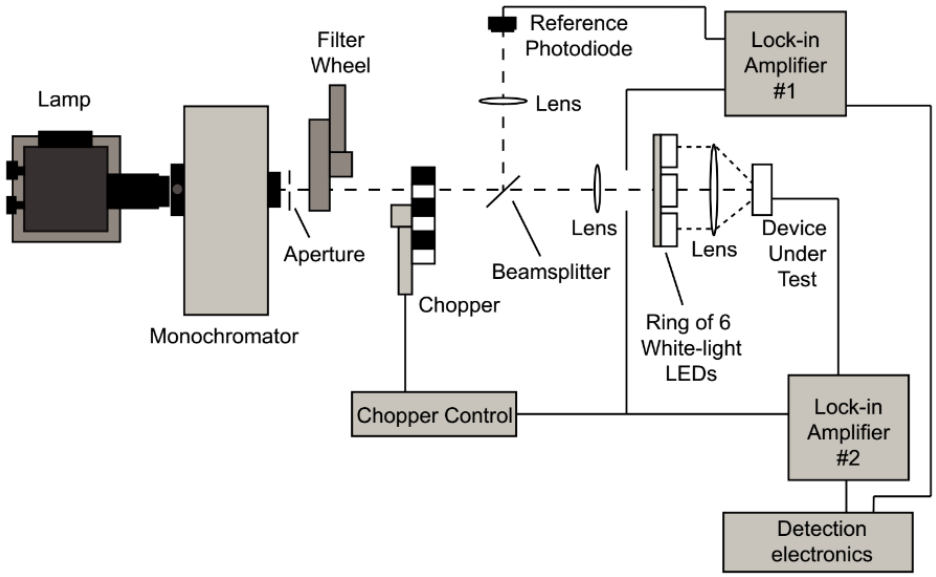


Figure 3.12. Schematic of a white light biased EQE system.[53]

In brief, EQE measurements are acquired from 400 to 900 nm in 10 nm steps using chopped monochromatic light (Horiba TRIAX-180, grating 600 grove/mm). To modulate the monochromatic light, a chopper (Terahertz, C-995) was used at a frequency of 1971 Hz in combination with a lock-in amplifier (Stanford Research System, SR830). The EQE was quantified against a NREL calibrated Si photodiode. The sample was positioned to focus the light in the active area, with a spot size of 1 mm, the active area was always slightly larger than this.

CHAPTER 4

PERFORMANCE EHANCEMENT OF BULK SILICON SOLAR CELL USING PROXIMAL NANOCRYSTALLINE QUANTUM DOTS

4.1 Preface

The literature provides ample spectroscopic evidence of efficient excitonic ET from NQDs to semiconductor substrates using optical techniques [16, 18, 21, 23, 54, 55]. However, only a few studies have reported a systematic approach for quantifying the contribution of different ET modes in the electrical characterization of PV devices. Thus, it is important to develop a protocol that can be utilized for a systematic quantification of the different ET modes during conventional PV measurements. The ET based sensitization of PV or other optoelectronic devices by NQDs should result in an enhanced electrical response or gain. A detailed understanding of a test structure will help to rationally implement ET based enhancement mechanisms inside a conventional PV architecture. Within this context, we utilized a simple test structure based on bulk p-type Si and proposed a simple experimental protocol to decouple the contribution of intrinsic optical effects from those due to ET. Our study of a bulk-Si PV structure sensitized by proximal CdSe/ZnS NQDs provides a simple experimental approach for developing a systematic test protocol that is relevant to the broader PV community. In our study, we found that a ~30% enhancement in the short circuit current density (J_{sc}) and external quantum efficiency (EQE) can be achieved using a ~70 nm thick NQD film. Furthermore, the open circuit voltage (V_{oc}) and fill factor (FF) values remain unchanged which indicate that our devices did not degrade upon NQD deposition. Overall, our study lays the foundation for the rational design

of a PV architecture that can utilize ET processes for charge generation and thus provides a positive outlook for ET based hybrid PV devices.

4.2 Introduction

PV devices that harvest solar energy to generate electricity are set to help mitigate the next generation energy problems. Presently, crystalline Si dominates the solar cell (SC) market and enjoys more than 80% of the market share [56]. The thickness of crystalline Si SCs varies from 150 - 300 μm and this incorporates a significant materials cost into the overall manufacturing cost of PV modules [35]. The manufacturing cost can be reduced substantially if thin film SCs (thickness of 1-2 μm) with comparable power conversion efficiencies can be produced [35]. However, thin film SCs using Si as the sole absorber material suffer due to the indirect nature of the bandgap and therefore thick films are necessary to overcome its weak absorption especially for near-bandgap and longer wavelength light [35, 57].

In addition to third generation approaches [58] for enhancing SC performance, there is a desire to fabricate hybrid Si SCs that utilize the existing Si manufacturing technology. In this regards, substantial effort exists to develop and incorporate advanced nanoscale materials which serve as absorbers in an effort to overcome weak absorption problems [59]. One such method is to create energy transfer (ET) based hybrid PVs and optoelectronic devices [18, 23, 60-67] where ET sensitizes the Si. ET mechanisms, specially Förster resonance energy transfer (FRET) are well studied and understood for molecular systems [68, 69] and have been utilized in chemical and biological applications [22, 25]. In fact, ET sensitization has been demonstrated for dye-sensitized solar cells (DSSCs) [64, 65, 68, 70] and organic photovoltaics (OPVs) [71].

Dexter [24], first reported the possibility of using Förster type non-radiative energy transfer (NRET) for sensitization of inorganic semiconductors for PV applications. In recent years, ET based sensitization of semiconductors for the development of hybrid SCs has gained renewed interest due to the emergence of nanocrystal quantum dots (NQDs) [17-19, 21-23, 55, 57, 60-62, 72, 73]. NQDs have large absorption cross-sections and can act as efficient photon absorbers. They are also photo-stable and possess a size and composition dependent wavelength tunability [74-76]. Recently, our group reported several studies where NQDs serve as energy donors to sensitize thick Si substrates [22, 23, 61] as well as ultrathin (~ 50-300 nm) SiNMs [18]. Thus, sensitization of Si, or other semiconductor materials, by utilizing ET from NQDs provides a potential method to develop ultrathin and flexible ET based hybrid SCs.

Similar to photosynthesis, ET allows for the separation of the two major functionalities in a SC, i.e. light absorption (optical) and carrier transportation (electrical) [19]. This approach is inherently different from traditional SCs which employ the same material for light absorption as well as carrier separation and transportation [77]. In a hybrid NQD/Si architecture, NQDs are used as the light absorbing component. By creating multilayers of different NQDs, a wide range of the solar spectrum can be covered and thus the weak absorption in Si can be overcome [23, 73]. The absorbed solar energy in the NQD layers is transferred to the Si via NRET and RET, where carriers are created and subsequently separated and transported [22]. NRET is responsible for the direct creation of electron-hole pairs in Si due to the fast decay of the dipolar field of NQD excitons [28]. Whereas, RET involves radiative decay of the donor excitons into photonic modes that propagate along the substrate (waveguiding modes) before eventual reabsorption [34]. NRET exhibits strong distance dependence decay characteristics and becomes ineffective at

donor-acceptor (NQD-Si) separation distances greater than a few nanometers of [78]. In contrast, RET is active for separation distances of tens of nanometers [18, 22] and thus facilitates the use of thicker NQD films for efficient light absorption [54, 60]. The overall ET from both NRET and RET thus contributes towards the enhancement of the power conversion efficiency in hybrid NQD/Si SCs [18, 22, 23].

Currently, most reports on excitonic ET in NQD based systems relied on spectroscopic evidence using time-resolved photoluminescence (TRPL) [23, 32, 61, 63, 79]. A limited number of studies used electrical measurements to understand the ET processes in such systems [17, 33, 55, 60, 80]. However, most of these studies used either direct [33] or time-resolved photocurrent measurements [17]. They reported improvements in the electrical response due to NQD sensitization for different systems including Si nanowire SCs [16] [73], GaAs multiple quantum well heterostructures in a p-i-n configuration [55], bulk GaAs p-i-n structures [33], ultrathin SiNM based field effect transistors [19], and ultrathin Si Schottky SCs [60]. Additionally, there are reports of enhanced PV efficiency due to the deposition of NQDs in systems such as multi-crystalline Si [81], Si nanopillars [80, 82], GaAs nanopillars [83] and textured crystalline Si [84]. These reports attribute the enhancement in PV efficiency to the increased responsivity in the ultra-violate (UV) range of the solar spectrum and to reduced reflection. However, reports on the electrical effects of ET within the existing framework of PV systems are lacking. A few reports [60, 73, 85, 86] link the enhancement in PV efficiency to ET processes although contributions from other effects such as reduced reflection [80] and charge transport in the NQD layer [87] need to be considered. Inclusion of these effects complicates attempts to accurately quantify the contribution from ET in these measurements

In this work, we report the fabrication of a bulk Si based SC as a test structure to quantify the contribution of ET in PV measurements. A bulk Si based test structure was used because (a) the conventional PV architecture is relevant to industry and (b) the simplicity of the device fabrication steps provides the foundation for future design approaches. We report an overall PV enhancement of ~ 30% after deposition of a ~70 nm thick CdSe/ZnS core-shell NQD layer on a p-i-n Si SC. We developed an approach to quantify the contribution of ET modes to the overall PV performance enhancement using reflectance measurements to distinguish ET from optical effects (i.e. anti-reflection). From these results, new design approaches can be proposed for quantifying ET-generated charges.

4.3 Experimental methods

Device Fabrication: A simplified fabrication process flow diagram is provided in Figure 4.1. In brief, devices were fabricated on 500 µm Boron doped p-type Si <100> wafers with a resistivity of 0.01- 0.02 **Ω**-cm^{-1} (doping density > 10^{18} cm^{-3}). The wafers were cleaned according to the RCA procedure [88] by immersing in a solution of first 4:1:1 H_2O:H_2O_2:NH_4OH then 4:1:1 H_2O:H_2O_2:HCl at 80 ^oC for 10 min. This was followed by immersion in a piranha solution (3:1 H_2SO_4:H_2O_2:) at 80 ^oC for 10 min before thoroughly rinsing under DI water and subsequent drying under N_2 flow. Next, a 500 nm thermal oxide was grown on top of the wafer by LPCVD. Then, 100 nm of intrinsic (i-) and 140 nm of n-doped poly Si layers were deposited by LPCVD. The p-i-n Si wafer was annealed first at 900 ^oC for 30 min under N_2 to activate and diffuse the dopants and then at 400 ^oC for 30 min in forming gas (5% H_2, 95% N_2) to passivate the surface and reduce surface defect states. The poly Si was then etched in the ICP-RIE to define the active area. The devices were then encapsulated with 100 nm SiO_2 by PECVD. Then the SiO_2 over the

active areas were opened by wet chemical etching in buffered oxide etch (7:1 NH_4F:HF) for 1 min. Finally, a 150 - 200 nm thick layer of Aluminum (Al) was deposited at a rate of 1-2 Å/sec to create top and the back contacts using the cryo e-beam evaporator. The final product consisted of a 2 cm x 2cm chip with 8 devices, each with a 1.5 x 1.5 mm active area.

Deposition of NQDs: A solution of CdSe/ZnS (absorbance ~ 560 nm) NQDs in toluene (80 µL solution at 25 mg-mL^{-1}) was spun cast on the chips. The spin coater was a CEE system from Brewer Scientific which spun at 1000 rpm for 18 s followed by 1500 rpm for 1 min. This resulted in uniform coverage of NQDs over the devices. The devices were stored under N_2 when not in use. PbS NQDs were deposited as purchased by spin casting.

Device Characterization: Photovoltaic measurements were done inside a N_2 glove box to ensure a controlled environment. A detailed description of the set-up for both PV and EQE measurements was provided in Chapter 3.4.

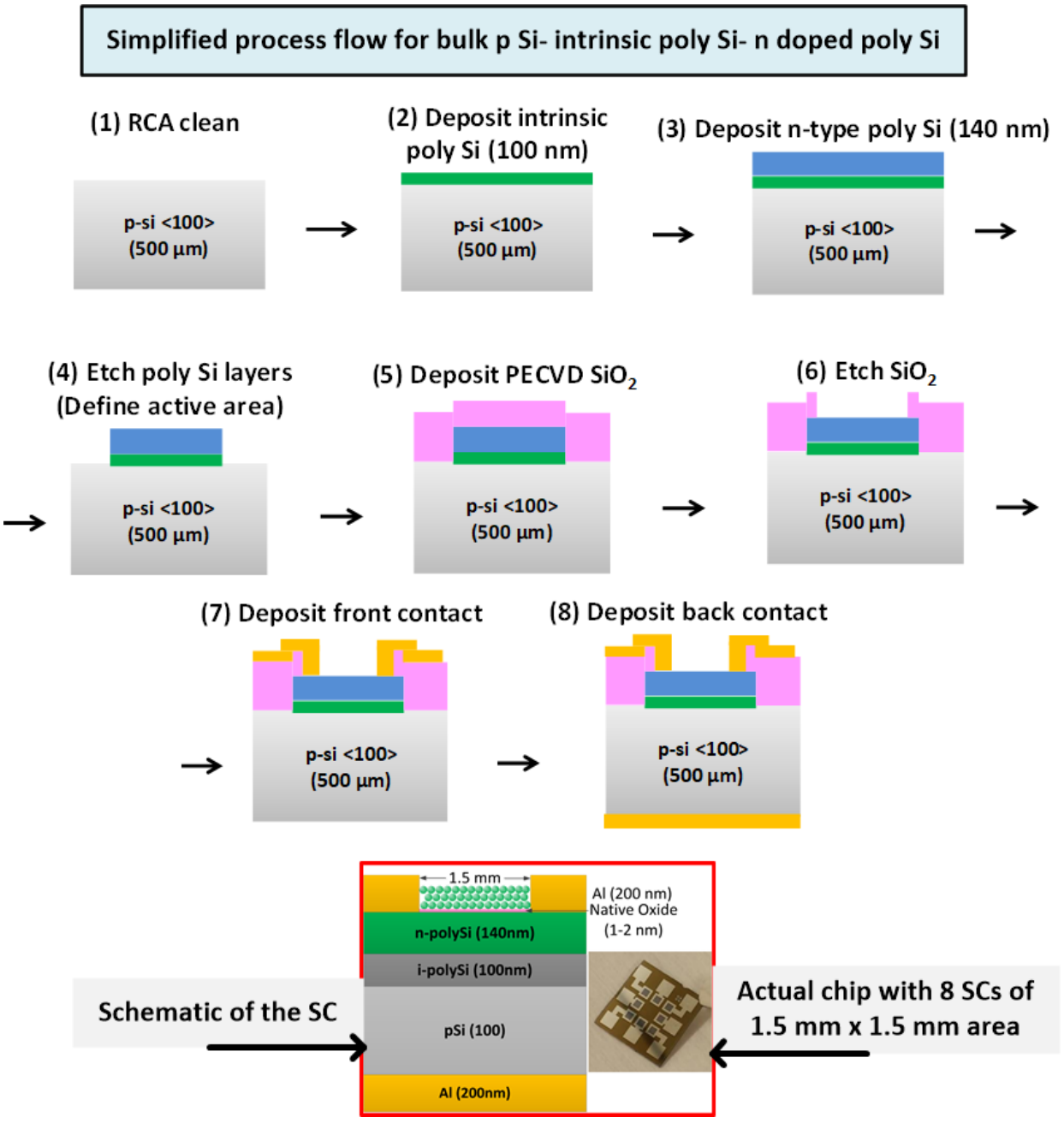


Figure 4.1. Simplified fabrication process flow of bulk Si p-i-n PV devices.

4.4 Results and Discussion

4.4.1 Establishing the stable PV characteristic of the fabricated devices

Once fabricated, the stability of the PV devices needs to be measured. Stable PV behavior is necessary so that the effect from NQD deposition can be confidently identified over day to day variations. A previous report [89] on ultrathin (~75 nm) back gated Si FET type photodetectors showed considerable fluctuations (~ 15-20%) in device characteristics and thus they were measured under vacuum (~ 10^{-6}-10^{-7} Torr). Here, an inert atmosphere N_2 glove box was used during the PV measurements to avoid these fluctuations and in fact, stable and reproducible results (<1% variation) were observed. EQE measurements were performed under ambient conditions, however, the samples showed stable behavior.

Figure 4.2 shows the PV characteristics (dark and illuminated) of the devices with and without NQDs measured over three days to establish long term temporal variation. From the J_{sc}-V curves, a < 1% variation in signal under illumination was observed. An ~5% enhancement in PV behavior was observed from 1-2 monolayers (~6 – 15 nm thick film, Figure 4.2 inset) of NQDs on the device. Overall, the fabricated bulk Si PV devices with and without NQDs were stable and an observable PV enhancement was recorded. The temporal stability study with 1-2 monolayers of NQDs showed that this measurement setup was suitable to use in developing a measurement protocol to quantify the contribution of ET modes towards NQD sensitized PV enhancement.

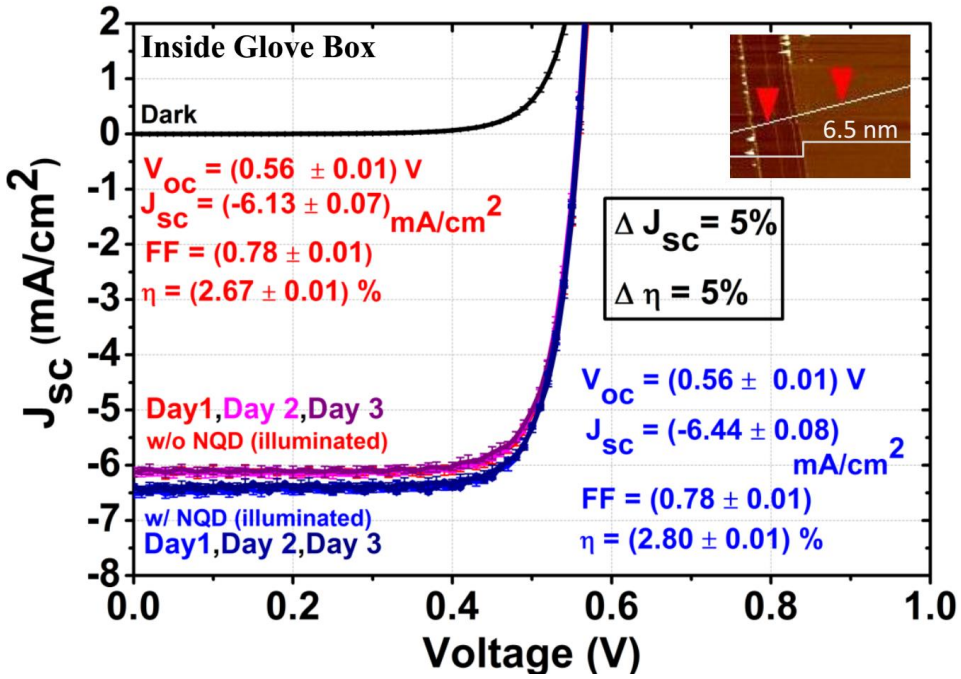


Figure 4.2. Temporal stability of the fabricated bulk p-type Si SC measured inside the glove box. J-V curves of the device under dark and illuminated conditions for consecutive 3 days. Inset: AFM image showing a ~6.5 nm thick NQD layer (~1 monolayer) deposited on the device. Black curves: dark measurement, Red and blue curves show the illuminated measurement without and with NQDs, respectively.

In our measurement protocol, performing the I-V measurements in a glove box ensures the optical quality of NQD layer remains intact. Environmental degradation of the NQD layers would be detrimental as the quantum yield (QY) would deteriorate. Although core-shell NQDs are photostable [90], photo-oxidation and photobleaching [90, 91] can occur due to the diffusion of oxygen. In fact, the presence of oxygen and water plays an active role in the degradation of NQDs (i.e. spectra diffusion: blue shifting and PL quenching [90-95]). While some studies [91, 96] add an additional capping layer to protect the NQDs, carrying out the measurement in an inert atmosphere serves the same purpose. Thus, developing a measurement protocol that minimizes exposure of the NQD films to ambient conditions protects the integrity of the NQDs.

The developed measurement protocol consists of several steps: (1) initial J-V measurements are conducted in the glove box, (2) EQE measurements are done in air, (3) a NQD film is spun cast on the device in air, (4) this is transferred into a N_2 filled centrifuge tube and then into the glove box, (5) I-V measurements are conducted in the glove box, (6) EQE measurements are done immediately in air and then (7) the hybrid NQD/Si SCs are stored under N_2 in a glove box. During this process, all attempts were made to minimize air exposure and thus EQE measurements were done at the very end before storing the measured device. Using this procedure, repeatable results were obtained for the J-V and EQE measurements for the bulk Si SCs with and without NQDs. This confirms that short exposures to environmental conditions do not degrade the NQD films. Thus, the observed PV enhancement from 1-2 monolayers of NQDs is backed by repeatable and stable device characteristics.

4.4.2 Enhancement of PV characteristics of the SCs

This section reports the results and observations for SCs after NQD deposition using three different systems. The main device consists of bulk p-type Si with 100 nm of intrinsic poly Si and 140 nm n-doped poly Si with ~70 nm of CdSe/ZnS NQDs. The results are described in section 4.4.2.1. Then, the effect of thinner poly Si layers on the overall PV enhancement was studied. The devices in section 4.4.2.2 have a 50 nm intrinsic layer and a 70 nm n-doped layer on which ~70 nm of CdSe/ZnS NQD were deposited. Lastly, section 4.4.2.3 explores the effect of near-infrared NQD on the main device. In this case, we spun cast PbS NQD (peak emission at 1000 nm) on the devices.

In these studies, a thicker NQD film was used as this is desirable for many optoelectronic applications [97-100]. Additionally, a 70 nm thick film has more light absorption compared to a

1-2 monolayer film. A balance between NQD film thickness is necessary as ET from NQDs to Si becomes inefficient for very thick layers (>100 nm) [60]. In fact, 90 % efficient exciton energy transfer (NRET and RET) can be achieved from a single monolayer of NQD [23], whereas the ET efficiency drops to 60% (NRET + RET) for an ~100 nm thick NQD film [54]. Thus, 70 nm thick films ensure sufficient light absorption without drastically decreasing ET efficiency. Additionally, previous work by Peng *et al.* [89] reported a 300 times gain in photocurrent from an ~70 nm thick NQD film on ultrathin Si FET devices. Thus, taking these factors into consideration, we conducted all subsequent PV measurements using a ~70 nm thick NQD film.

4.4.2.1 Effects of CdSe/ZnS NQD on bulk p Si-i (100 nm) poly Si- n-doped (140 nm) poly Si

Intrinsic and n-doped poly Si were deposited on top of a bulk p-type Si substrate to achieve a p-i-n type SC architecture on which ~70 nm of CdSe/ZnS NQDs were deposited. Figure 4.3 shows the J_{sc}-V characteristics of 4 devices on the same chip before and after NQD deposition. The PV parameters extracted from these J_{sc}-V curves are summarized in Table 4.1. A ~30% (on average) enhancement in the PV performance was observed after NQD deposition. The V_{oc} and FF did not change or deteriorate upon NQD deposition indicating SC stability. The PV enhancement mainly occurred due to the increase of the J_{sc} and thus, η increased by a similar amount.

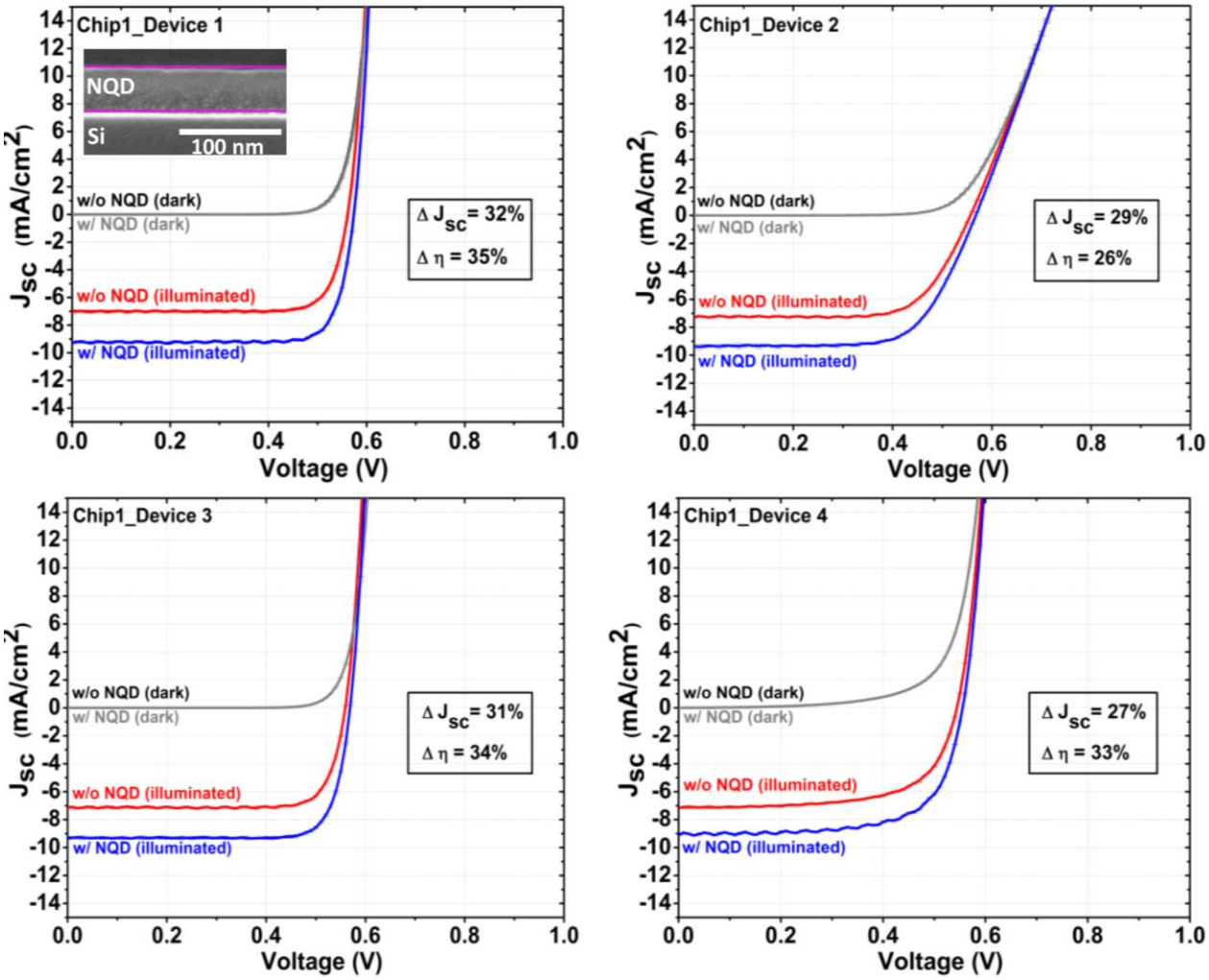


Figure 4.3. J_{sc}-V curves for 4 devices on 1 chip measured in the dark and under 1 Sun AM1.5G illumination. The black and grey curves represent the dark behavior with and without NQDs. Red curves represent J_{sc}-V characteristics for SCs without NQDs under illumination. Blue curves represent J_{sc}-V characteristics for SCs with NQDs. Inset: Shows SEM image of ~70 nm CdSe/ZnS NQD layer deposited by spin coating.

Table 4.1. Summary of PV performance parameters for 4 devices on chip-1 measured under 1 sun AM1.5G illumination without (w/o) and with (w/) NQDs.

Chip label		Open circuit voltage V_{oc} (V)	Short circuit current density J_{sc} (mA/cm^2)	Fill Factor FF	Efficiency η (%)	Change in J_{sc} (ΔJ_{sc})	Change in η ($\Delta \eta$)
Chip-1 Bulk p-Si- 100 nm intrinsic poly-140 nm n-doped poly							
Device 1	w/o NQD	0.56 ± 0.01	-7.01 ± 0.14	0.81 ± 0.02	3.19 ± 0.03	↑ 32%	↑ 35%
	w/NQD	0.57 ± 0.01	-9.29 ± 0.06	0.82 ± 0.01	4.31 ± 0.02		
Device 2	w/o NQD	0.56 ± 0.01	-7.27 ± 0.08	0.69 ± 0.01	2.83 ± 0.02	↑ 29%	↑ 26%
	w/NQD	0.57 ± 0.01	-9.36 ± 0.04	0.67 ± 0.01	3.57 ± 0.04		
Device 3	w/o NQD	0.54 ± 0.01	-7.10 ± 0.06	0.81 ± 0.01	3.21 ± 0.02	↑ 31%	↑ 34%
	w/NQD	0.57 ± 0.01	-9.29 ± 0.07	0.82 ± 0.01	4.31 ± 0.02		
Device 4	w/o NQD	0.54 ± 0.01	-7.14 ± 0.08	0.67 ± 0.01	2.57 ± 0.02	↑ 27%	↑ 33%
	w/NQD	0.56 ± 0.01	-9.08 ± 0.08	0.68 ± 0.01	3.42 ± 0.04		

Chip is sensitized by visible NQD

While all devices showed an enhancement, the performance of the individual SCs showed some variation. This may originate from thickness variations in the deposited poly Si as seen optically in Figure 4.4.

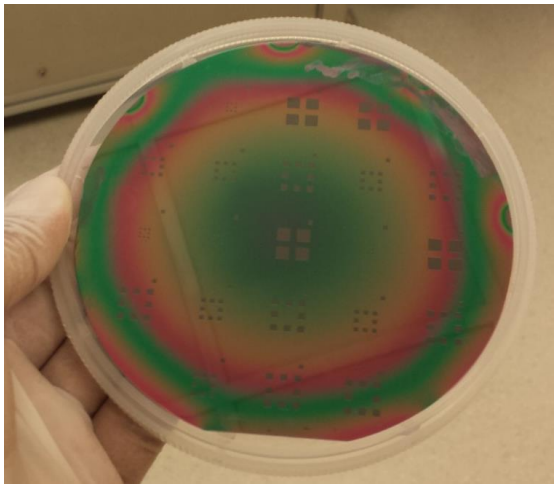


Figure 4.4. Thickness variation of poly Si deposited by LPCVD on a bulk p-type Si wafer. The thickness of the deposited intrinsic and n-doped poly Si is 100 nm and 140 nm, respectively.

The poly Si thickness variation mostly effects the J_{sc} values (Table 4.1). In this regard, comparison of PV parameters (J_{sc}, V_{oc}, FF and η) to determine the enhancement from NQD deposition were carried out on the same device. Then the observed enhancements due to NQD effects were compared between devices as well as chips to establish a baseline. The J_{sc}-V curves from 5 different devices for a second chip are shown in Figure 4.5 with the extracted PV parameters given in Table 4.2.

Table 4.2. Summary of PV performance parameters for 5 devices from **chip2** measured under 1 sun AM1.5G illumination without (w/o) and with (w/) NQDs.

Chip label		Open circuit voltage V_{oc} (V)	Short circuit current density J_{sc} (mA/cm^2)	Fill Factor FF	Efficiency η (%)	Change in J_{sc} (ΔJ_{sc})	Change in η (Δ η)
Chip-2 Bulk p-Si- 100 nm intrinsic poly-140 nm n-doped poly							
Device 1	w/o NQD	0.54 ± 0.01	-7.40 ± 0.06	0.72 ± 0.01	2.87 ± 0.01	↑ 32%	↑ 36%
	w/NQD	0.56 ± 0.01	-9.78 ± 0.11	0.71 ± 0.01	3.90 ± 0.01		
Device 2	w/o NQD	0.54 ± 0.01	-4.81 ± 0.05	0.80 ± 0.01	2.10 ± 0.01	↑ 16%	↑ 15%
	w/NQD	0.54 ± 0.01	-5.60 ± 0.04	0.80 ± 0.01	2.41 ± 0.01		
Device 3	w/o NQD	0.56 ± 0.01	-7.56 ± 0.07	0.81 ± 0.01	3.43 ± 0.01	↑ 34%	↑ 37%
	w/NQD	0.57 ± 0.01	-10.15 ± 0.09	0.81 ± 0.01	4.71 ± 0.03		
Device 4	w/o NQD	0.55 ± 0.01	-5.71 ± 0.06	0.81 ± 0.01	2.53 ± 0.01	↑ 11%	↑ 14%
	w/NQD	0.56 ± 0.01	-6.35 ± 0.03	0.81 ± 0.01	2.88 ± 0.01		
Device 5	w/o NQD	0.32 ± 0.01	-6.85 ± 0.12	0.55 ± 0.01	1.21 ± 0.01	↑ 33%	↑ 46%
	w/NQD	0.35 ± 0.01	-9.14 ± 0.08	0.56 ± 0.01	1.77 ± 0.01		

Chip is sensitized with visible NQD

Overall, the PV enhancement for devices on the two chips were similar with both showing a ~30% PV enhancement in J_{sc} and η. However, on the second chip, 2 devices showed only a ~15% enhancement. For these two devices (device 2 and 4 in Table 4.2), the initial J_{sc} values without NQDs were lower than the more efficient devices (~5 mA/cm^2 vs. 7 mA/cm^2). This shows that the degree of PV enhancement is affected by the quality of the initial devices with higher enhancements for devices with higher starting J_{sc} values.

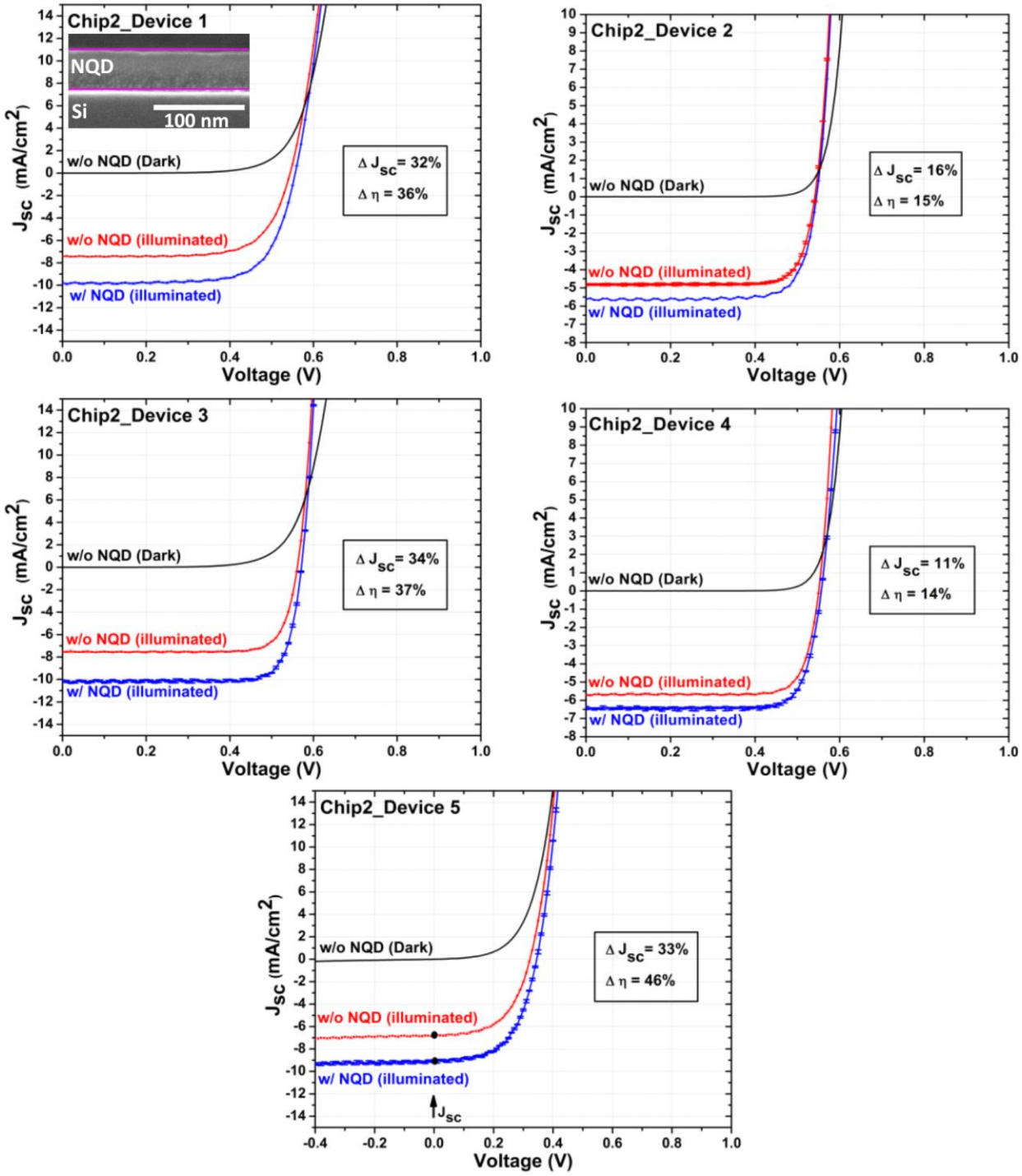


Figure 4.5. J_{sc}-V curves for 5 devices on of **Chip2** measured in the dark and under 1 Sun AM1.5G illumination. The black curves represent dark J_{sc}-V behavior of the SCs with and without NQDs. Red and blue curves are for SCs without and with NQDs under illumination. respectively Inset: SEM image of ~70 nm NQD (CdSe/ZnS) layer deposited by spin coating.

As the chips were made from the same bulk p-Si wafer and experienced the exact same fabrication processing steps, it is believed the differences result from the thickness variation of the deposited intrinsic and n-doped poly Si layers. This suggests optimization of the poly Si deposition is needed. The recipe used for poly Si deposition was optimized for transistors where the n-doped poly Si layer is highly doped (~ 10^{19} cm^{-3}). Thus, it is necessary to optimize the poly Si recipe for specific applications with greater control over thickness and doping.

In addition to I-V measurements, the EQE was measured for each chip by averaging measurements from the individual devices on a chip. Figure 4.6 shows the average EQE behavior for each chip before and after NQD deposition. Overall, the shape of the EQE curve is similar for both the chips, although some differences are observed. One notable difference is that chip 1 shows slightly better performance between 450 - 650 nm. The EQE in both the shorter and longer wavelength regions is almost identical for both chips.

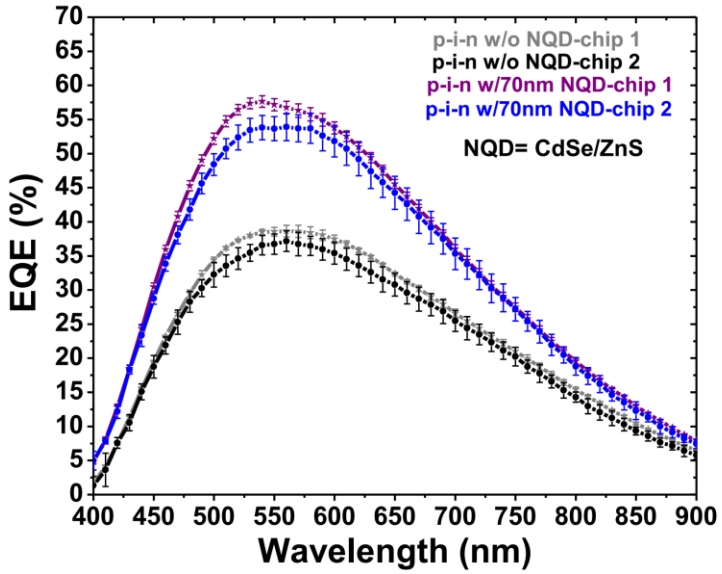


Figure 4.6. Comparison of the average EQE curves for **chip1** and **chip2**. Grey and black curves are before NQD deposition. Purple and blue curves are after SCs after NQD deposition.

The shape of the EQE curves are similar to those measured for amorphous hydrogenated Si (a-H:Si) thin film SCs [101-104]. The absorption coefficient of a-H:Si rapidly decreases around 650 nm and thus, the response of the SC is poor in the red (longer) wavelength region. A number of studies have been done to understand the behavior a:H-Si layers for thin film SC applications [15, 101-103, 105-108]. Additionally, a-H:Si and poly Si have higher blue absorption than crystalline Si and thus thinner layers can be utilized. In general, the EQE the hybrid NQD/Si devices indicates that the deposited poly Si plays an important role in the SC behavior and the devices act like non-optimized amorphous Si SCs.

In this section, the overall behavior of hybrid NQD/Si SCs was discussed. This works provides the premise to build a testing protocol for quantifying the contribution of NRET and RET as well as optical effects.

4.4.2.2 Effects of CdSe/ZnS NQD on bulk p Si-i (50 nm) poly Si- n-doped (70 nm) poly Si

We studied the effect of poly Si thickness on hybrid NQD/Si SCs by fabricating a device where the intrinsic and n-doped layer thickness was halved compared to that discussed in Section 4.4.2.1. Figure 4.7 shows the J_{sc}-V curves for 3 devices with the thinner poly Si layers and the extracted PV parameters are given in Table 4.3. Here, 2 devices showed ~40% PV enhancement in J_{sc} and η compared to the observed ~30% enhancement for SCs with thicker poly Si layers. However, one device showed a smaller enhancement. For this device, a change in the shape of the J_{sc}-V curve (Figure 4.7, device 2) occurred upon NQD deposition which resulted in a lower FF value. This led to a decrease in the magnitude of the enhancement. However, the overall enhancement was still significant. It should be noted that the V_{oc} and FF values are similar for the two poly Si thickness, however, the J_{sc} values for thinner poly Si exhibited a larger increase after

NQD composition than for the thicker poly Si SCs (Table 4.2 and 4.3). The larger increase in J_{sc} results in a higher PV enhancement for the thinner poly Si SCs.

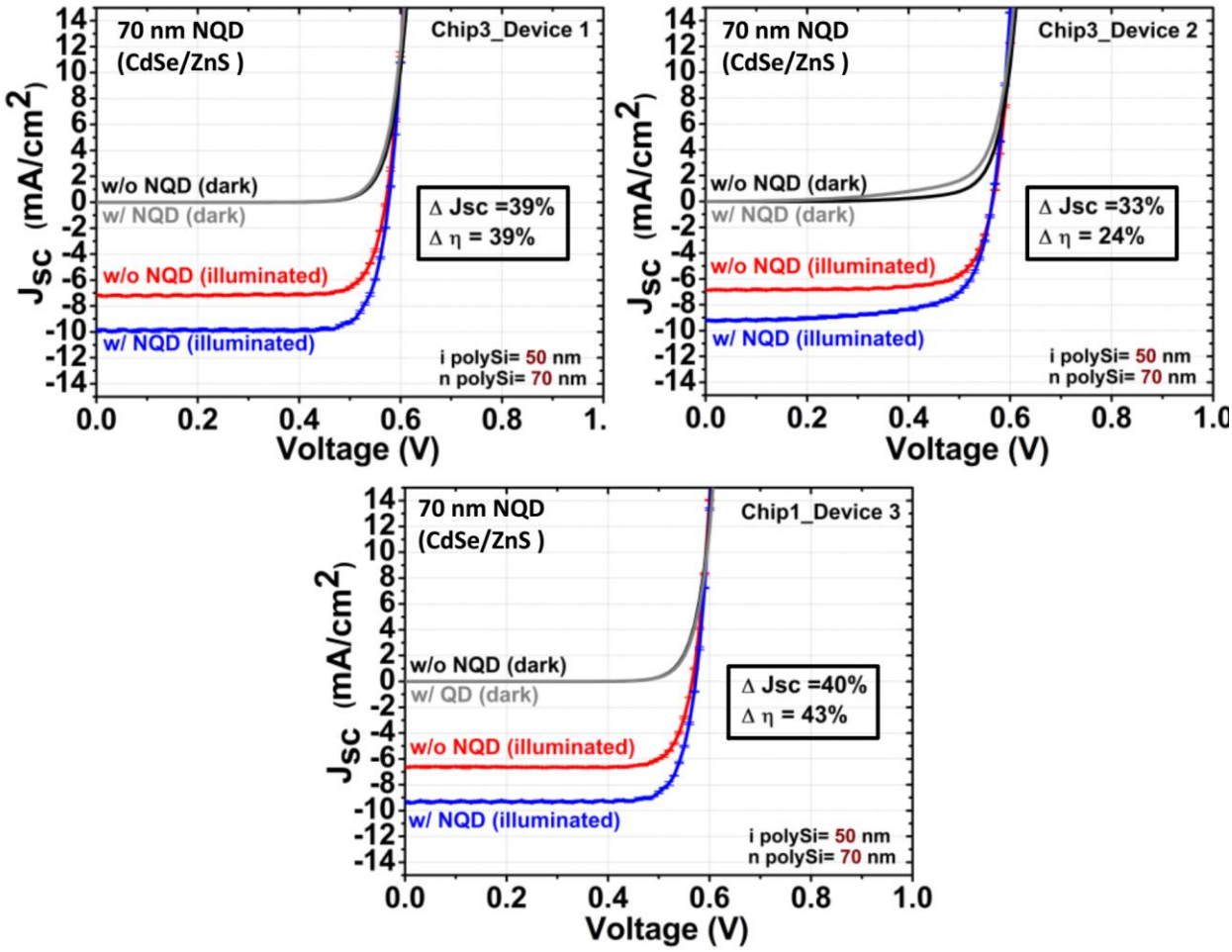


Figure 4.7. J_{sc}-V curves for SCs with thinner poly Si layers (i(50nm)-n(70nm)) measured in the dark and under 1 Sun AM1.5G illumination. The black and grey curves represent the dark J_{sc}-V behavior without and with NQDs, respectively. Red and blue curves represent J_{sc}-V characteristics under illumination without and with NQDs, respective.

Table 4.3. Summary of PV performance parameters for 3 devices from **chip3** with thinner i-poly Si (50nm) and n-doped (70nm) poly Si layers as measured under 1 sun AM1.5G illumination without (w/o) and with (w/) NQD (CdSe/ZnS) NQD deposition.

NQD= CdSe/ZnS

Chip label Chip-3 Bulk p-Si- 50 nm intrinsic poly-70 nm n-doped poly		Open circuit voltage V_{oc} (V)	Short circuit current density J_{sc} (mA/cm²)	Fill Factor FF	Efficiency η (%)	Change in J_{sc} (ΔJ_{sc})	Change in η ($\Delta \eta$)
Device 1	w/o NQD	0.57 ± 0.01	-7.15 ± 0.07	0.81 ± 0.01	3.33 ± 0.01	⬆ 39%	⬆ 39%
	w/NQD	0.57 ± 0.01	-9.98 ± 0.07	0.81 ± 0.01	4.62 ± 0.01		
Device 2	w/o NQD	0.57 ± 0.01	-6.87 ± 0.02	0.76 ± 0.01	2.95 ± 0.02	⬆ 33%	⬆ 24%
	w/NQD	0.56 ± 0.01	-9.17 ± 0.09	0.72 ± 0.01	3.65 ± 0.01		
Device 3	w/o NQD	0.57 ± 0.01	-6.63 ± 0.10	0.82 ± 0.01	3.06 ± 0.01	⬆ 40%	⬆ 43%
	w/NQD	0.57 ± 0.01	-9.28 ± 0.07	0.82 ± 0.01	4.37 ± 0.01		

i poly Si = 50 nm, n poly Si = 70 nm

The origin of the PV enhancement can be found by comparing EQE curves for chips with different poly Si thicknesses (Figure 4.8). Thinner poly Si SCs show improved blue response compared to thicker poly Si SCs and this is further enhanced after NQD deposition. The increased blue response may be due to improved carrier collection efficiency in thinner layers. The highly n-doped poly Si layer is electrically inactive due to short minority carrier diffusion lengths and this becomes prominent when the thickness is increased. In this case, thicker poly Si layers require photo-generated carriers to travel longer distances thus increasing the probability of annihilation during transportation. The increase is largest in the blue region as these highly energetic photons are absorbed near the surface. By reducing the poly Si thickness, the carriers generated from blue photons have a higher probability of being collected after transportation through the layer.

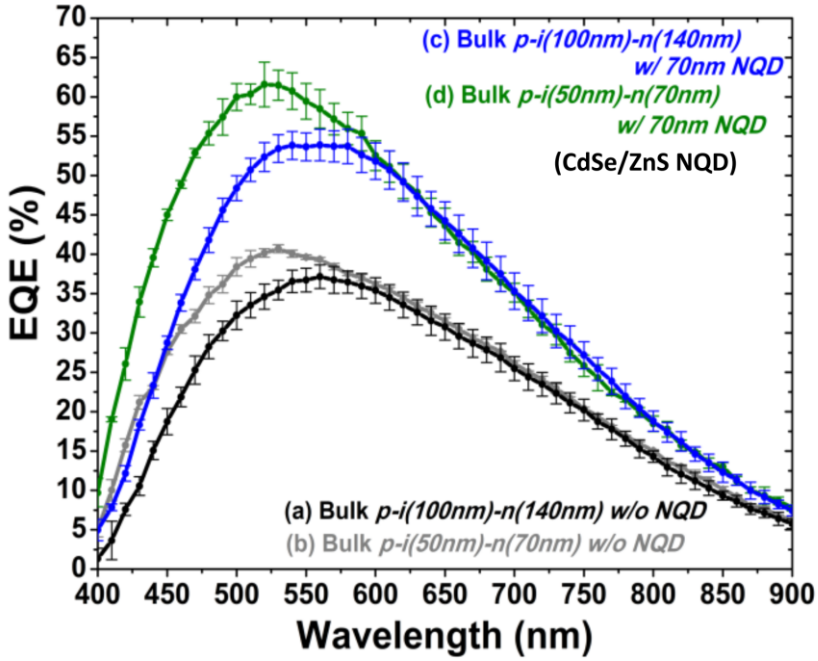


Figure 4.8. Comparison of EQE curves for **chip2 (i(100nm) n(140nm))** and **chip3 (i(50nm) n(70nm))**. Black and grey curves: EQE of the SCs before NQD deposition for chip2 and chip3, respectively. Blue and green curves: EQE of the SCs after NQD deposition (~70 nm of CdSe/ZnS) for chip2 and chip3, respectively.

This confirms the enhancement in PV behavior and reveals the importance of optimizing the thickness of poly Si layers. However, a balance needs to be achieved due to the presence of grain boundaries which can adversely affect the overall response of the SCs.

4.4.2.3 Effects of PbS NQD on bulk p Si-i (100 nm) poly Si- n-doped (140 nm) poly Si

CdSe/ZnS NQDs and Si absorb well in the ultra-violate and visible regions of the solar spectrum. Thus, the SC behavior is dominated by absorption in bulk Si. As Si has poor (or very low) absorption in the infrared region of the solar spectrum, another method to increase the enhancement is to use NQDs that emit in the NIR. Using PbS NQDs with emission at ~1000 nm, the contribution of Si absorption can be minimized thus providing another pathway to study ET mechanisms in a bulk Si SC system.

Figure 4.9 shows the J_{sc}-V curves for SCs sensitized with PbS NQDs. The extracted PV parameters are given in Table 4.4. As prepared, the devices showed similar behavior to those measured in Section 4.4.2.1, although relatively lower initial values of J_{sc} were observed. After PbS deposition a ~ 15% PV enhancement was measured. The relatively smaller enhancement may be due to the reduced J_{sc} of the starting device. Additionally, little information outside of the PbS NQDs emission is known. Therefore, the deposited films may be thinner which could result in a lower increase in efficiency.

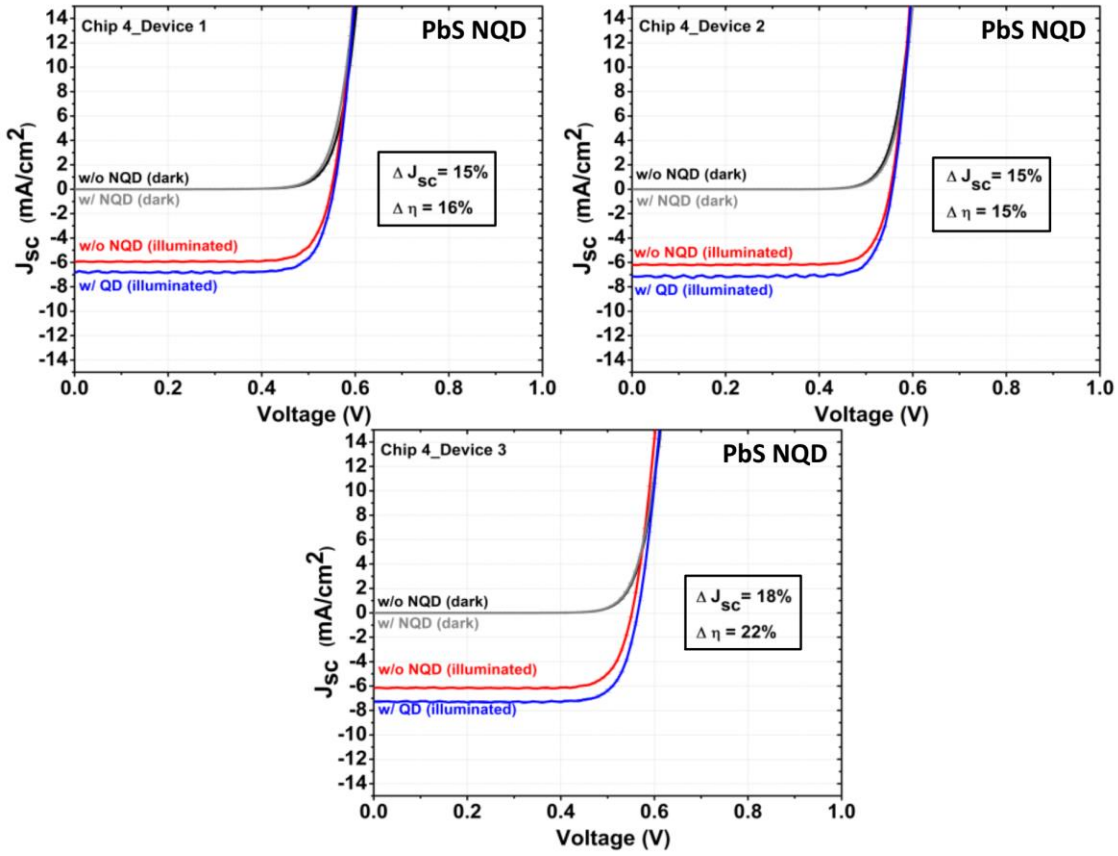


Figure 4.9. J_{sc}-V curves for hybrid NQD/Si p-i-n SCs with NIR emitting PbS NQDs. The black and grey curves represent dark behavior without and with PbS NQDs, respectively. Red and curves represent behavior under 1 Sun AM1.5G illumination without and with PbS NQDs, respectively. The SC had poly Si layer o with 100 nm of i- and 140 nm n-type Si.

Table 4.4. Summary of PV performance parameters for SCs with i-poly Si (100nm) and n-doped (140nm) poly Si layers as measured under 1 sun AM1.5G illumination without (w/o) and with (w/) NQD (PbS) deposition.

Chip label Chip-4 w/PbS Bulk p-Si- 100 nm intrinsic poly-140 nm n-doped poly		Open circuit voltage V_{oc} (V)	Short circuit current density J_{sc} (mA/cm^2)	Fill Factor FF	Efficiency η (%)	Change in J_{sc} (ΔJ_{sc})	Change in η ($\Delta \eta$)
Device 1	w/o NQD	0.55 ± 0.01	-5.95 ± 0.04	0.80 ± 0.01	2.60 ± 0.01	↑ 15%	↑ 16%
	w/NQD	0.55 ± 0.01	-6.84 ± 0.05	0.80 ± 0.01	3.02 ± 0.01		
Device 2	w/o NQD	0.55 ± 0.01	-6.19 ± 0.06	0.81 ± 0.01	2.77 ± 0.02	↑ 15%	↑ 15%
	w/NQD	0.56 ± 0.01	-7.13 ± 0.06	0.80 ± 0.01	3.18 ± 0.01		
Device 3	w/o NQD	0.55 ± 0.01	-6.15 ± 0.08	0.81 ± 0.01	2.72 ± 0.01	↑ 18%	↑ 22%
	w/NQD	0.56 ± 0.01	-7.27 ± 0.02	0.82 ± 0.01	3.32 ± 0.02		

Average EQE curves for the PbS sensitized SCs are shown in Figure 4.10. The enhancement in EQE is similar to that for the CdSe/ZnS sensitized devices. No significant increase in the NIR region was observed upon PbS NQD deposition. Thus, it is difficult to determine if there was any significant contribution due to ET from PbS NQDs.

The aim of the study was to develop a robust test structure and associated protocol to quantify the contribution of ET modes. This study revealed no significant advantage for using PbS NQDs over CdSe/ZnS NQDs, and in fact, CdSe/ZnS NQDs showed a larger impact on the PV enhancement.

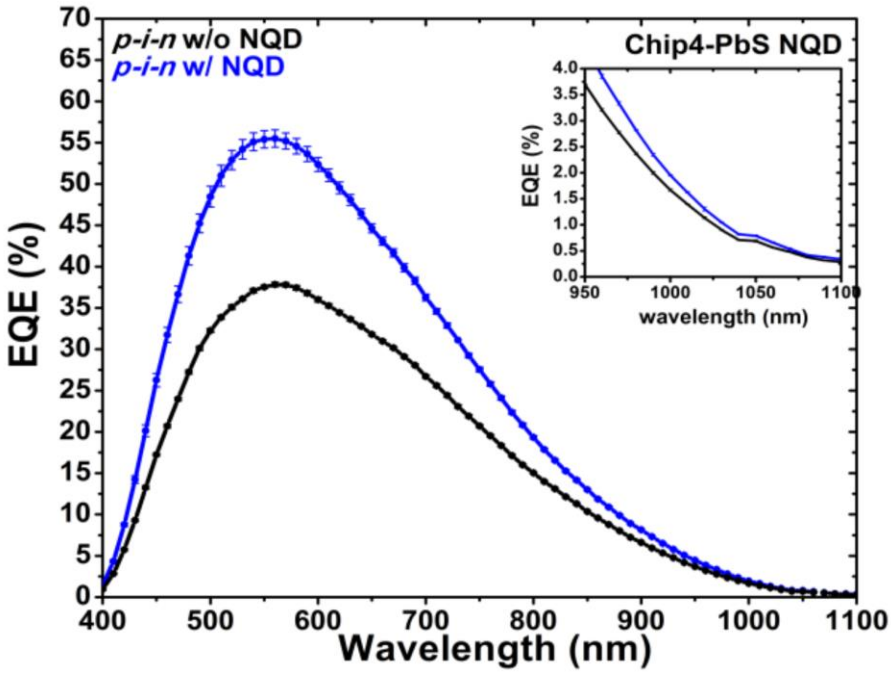


Figure 4.10. Average EQE curves for p-i-n devices with PbS NQDs. Black curve: EQE of SCs without NQD. Blue curve: EQE of the SCs after deposition of PbS NQD using same spin coating condition. Inset: Zoomed EQE curves from 950-1100 nm. Thickness of i poly Si and n-doped poly Si is 100 nm and 140 nm, respectively.

4.4.3 Development of a simple framework for quantification of ET contribution

There is a need to quantify the contribution from ET processes (NRET+RET) and separate out the contribution from optical effects (i.e. reduced reflection due the presence of the NQD layer). Both NRET and RET processes rely on light absorption in the NQD layer and subsequent ET to the Si. Optical effects, such as anti-reflection, work by reducing reflection at the surface and thereby enhancing absorption. Anti-reflection coatings (such as Si_3N_4 in conventional SCs) have a different index of reflection than Si and this facilitates multiple internal reflections at the Si and coating interface. Inherently, anti-reflection materials are transparent. Thus, any PV enhancement originating from ET due to NQD sensitization will have a different effect compared to a simple anti-reflection coating.

A test protocol based on reflectivity measurements was developed to separate ET and optical effects. SiO_2 was chosen a purely as an anti-reflection coating as it has a different index of refraction (n_{SiO_2}= 1.5) compared to Si (n_{Si} = 3.4). Additionally, its index of refraction is a similar to the NQD solids (n_{NQD} = 1.6 - 1.65) [54]. First, the effect of an anti-reflection coating (70 nm of SiO_2) on a bulk pSi-i(100nm)-n(140nm) sample was measured by comparing two cases, with and without the SiO_2 layer, as shown in Figure 4.11. The deposition of 70 nm of SiO_2 reduced reflection (Figure 4.13 inset) and therefore enhanced absorption in the SC. The increase absorption is seen by the increased in EQE for the sample with a SiO_2 layer (Figure 4.11).

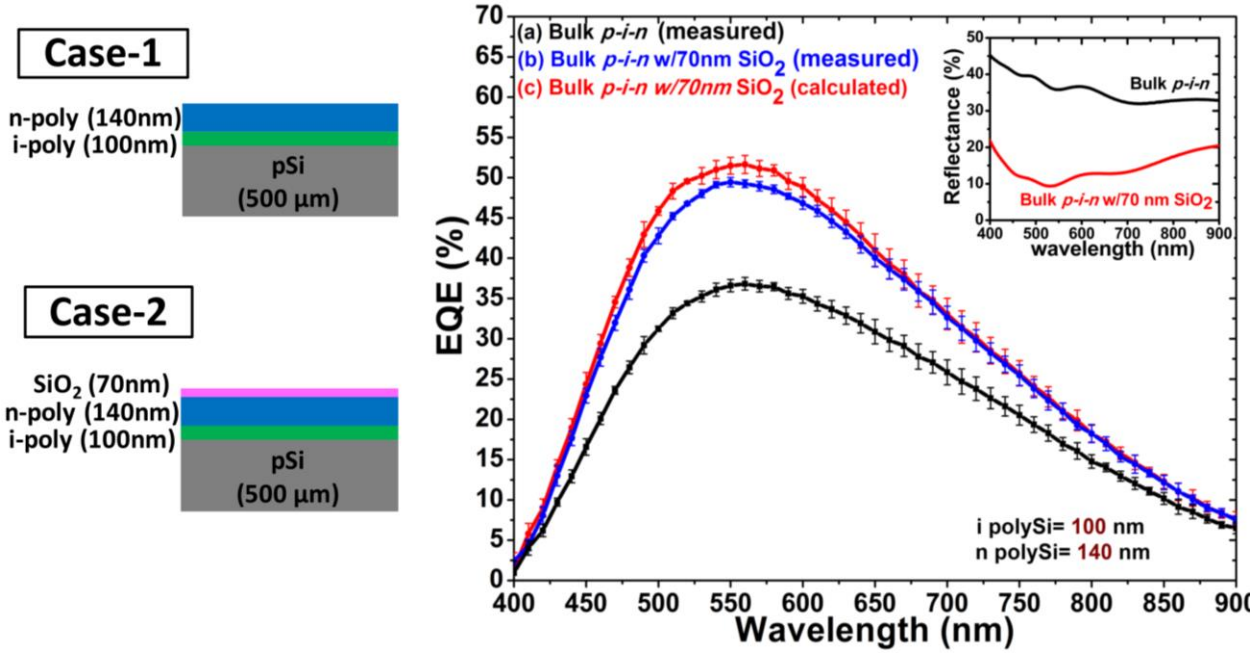


Figure 4.11. Schematics of the two cases studied: SC without (Case 1) and with Case 2) 70 nm of SiO_2. EQE curves of (a) bare bulk pSi-i(100nm)-n(140nm) poly Si SC, (b) with 70 nm of SiO_2 and (c) calculated by considering enhanced absorption as found from reflectivity measurements. Inset: reflectivity measurements case 1 and case 2.

The change in EQE due to SiO_2 can also be calculated by assuming all of the enhancement originates from the increased absorption due to reduced reflection. Eq. 4.1 calculates the increase in EQE due to decreased reflection and the result is plotted in Figure 4.11.

$$EQE_{calculated\ for\ optical\ effects} = \frac{(1-R_{SiO2\ on\ p-i-n})}{(1-R_{only\ p-i-n})} \times EQE_{measured\ without\ SiO2} \quad (4.1)$$

The calculated EQE curve agrees well with the measured EQE data. This provides a framework to construct EQE graphs from the reflectivity measurements.

4.4.4 Understanding the contribution of ET and optical effects towards PV enhancement

Using the protocol developed in section 4.4.3, calculated EQE curves can be created to show only optical effects (i.e. anti-reflection) and then compared with measured data that has contributions from both optical and ET effects. First, the reflectance of all devices discussed in section 4.4.2 was measured for structures that were bare and coated with either a 70 nm thick layer of NQDs or SiO_2. The results are shown in Figure 4.12.

Then, using the reflectivity data, the EQE due to optical effects can be calculated according to eq. 4.2.

$$EQE_{calculated\ for\ optical\ effects} = \frac{(1-R_{QD\ on\ p-i-n})}{(1-R_{only\ p-i-n})} \times EQE_{measured\ without\ QD} \quad (4.2)$$

The calculated EQE is plotted along with the measured EQE for two different devices in Figure 4.13 and differences are observed. As above equation considers EQE enhancement only due to reduced reflection, any contribution from ET processes in the hybrid NQD/Si system will result in an increase in the measured EQE compared to the calculated EQE. If there is ET from the NQDs to Si, the increase in the measured EQE is to follow the absorption profile of the NQDs.

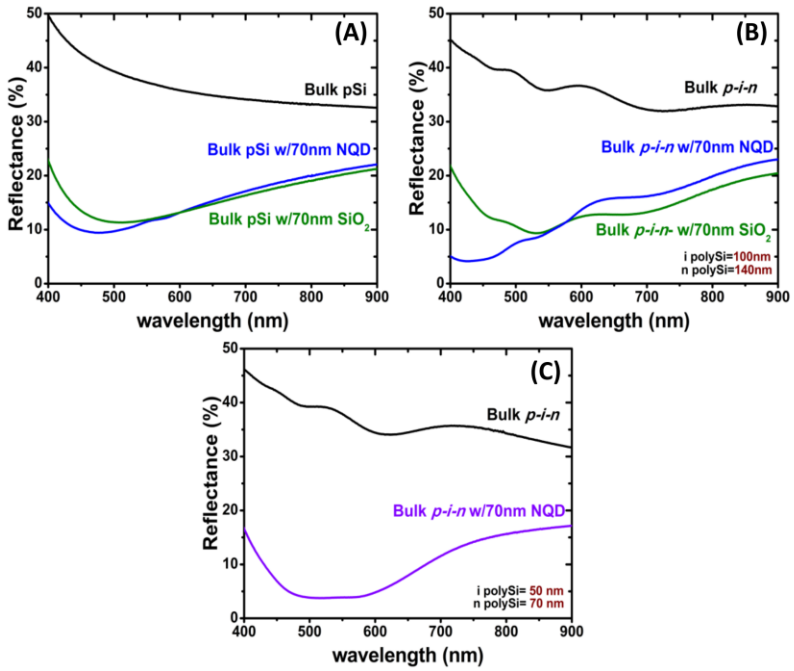


Figure 4.12. Reflectance measurements (a) of bulk p-Si bare, with 70 nm NQDs and 70 nm oxide (b) of bulk p-i (100nm)-n (140nm) Si bare, with 70 nm NQDs and with 70 nm oxide and (c) bulk p-i (50nm)-n (70nm) Si bare and with 70 nm NQDs.

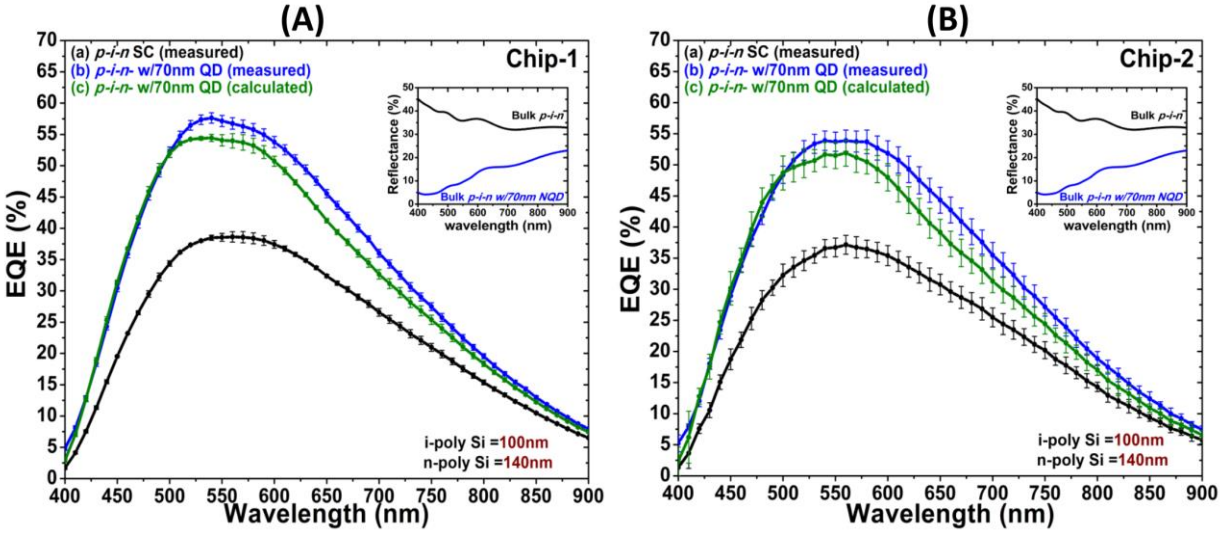


Figure 4.13. Measured and calculated EQE curves for (A) Chip 1 and (B) chip 2 bulk pSi-i(100nm)-n(140nm) poly Si SCs. The black curve is for the bare device, while the blue and green are the measure and calculated curves respectively. Inset: (A) and (B) are reflectivity measurements for the devices with (blue) and without (black) NQDs.

A wavelength dependent enhancement was previously seen in the work of Peng *et al*. [89] who studied NQD sensitized ultrathin (~75 nm) back gated FET devices. Figure 4.14 shows the wavelength dependence of the photocurrent enhancement upon NQD deposition for two different sized NQDs (absorption maximum at 585 nm and 605 nm). Here, the enhancement in photocurrent follows the absorbance of the NQDs indicating a contribution due to the NQDs. A similar wavelength dependent increase is expected in the EQE measurements if the origin of the enhancement is due ET processes (NRET+RET).

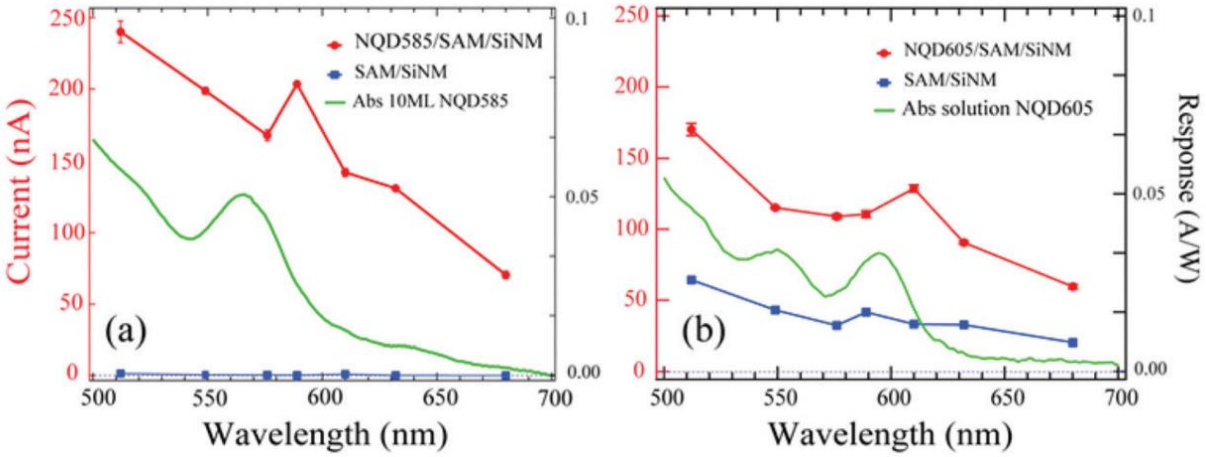


Figure 4.14. Photocurrent as a function of excitation wavelength for SAM passivated ultrathin (~75 nm) SiNMs. The blue and red traces show the photocurrent before and after NQD deposition respectively. The green curve shows the solution absorbance of the NQDs. The graph on the left shows NQDs that peak at 585 nm while that on the right peaks at 605 nm.[89]

The approach of using the reflectivity data to construct EQE graphs considering only optical effects is simple method for probing and quantifying the contribution from ET processes. In fact, a difference between the measured and calculated EQE is observed in the longer wavelength region (Figure 4.13). To determine if there is a wavelength dependence, the EQE enhancement due to NQDs is calculated using eq. 4.3:

$$EQE\ enhancement = \frac{EQE_{w/NQD} - EQE_{w/o\ NQD}}{EQE_{w/o\ NQD}} \quad (4.3)$$

The EQE enhancement ratios are shown in Figure 4.15 and 4.16 for the two chips discussed in section 4.2.2.1 with a bulk p-i(100nm)-n(140nm) structure.

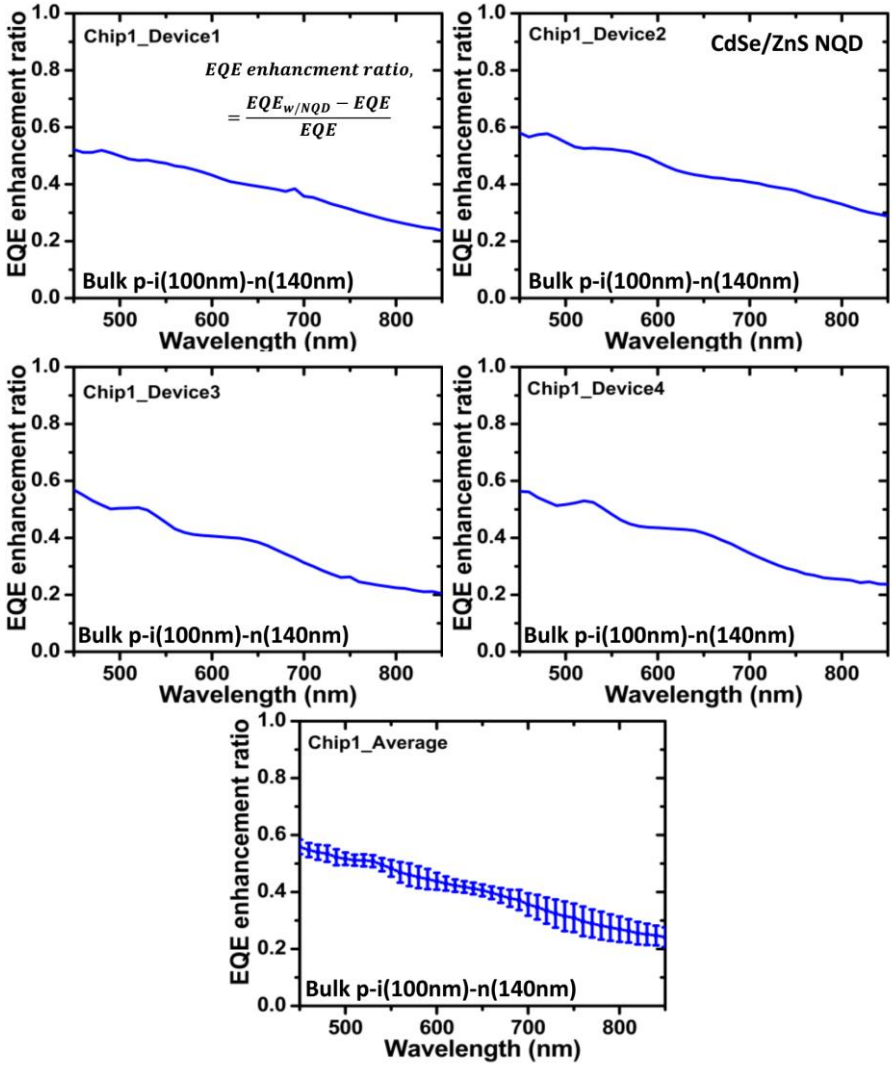


Figure 4.15. Top four graphs show EQE enhancement for individual devices from Chip-1 (bulk pSi-i(100nm)-n(140nm) poly Si SC) after ~70 nm NQD deposition. Bottom graph shows the average behavior for all the devices.

Here, no clear wavelength dependence is observed. Rather, both chips show an almost monotonic increase in EQE over the wavelength range (i.e., EQE increases with increasing energy). However, some variation in the EQE enhancement was observed for different devices

across the two chips and the average EQE for each device is shown in Figures 4.15 and 4.16. The slope of the increase in Figure 4.15 is greater than that in Figure 4.16 which showed nearly constant enhancement over the wavelength range. These differences may relate back to variations in the poly Si thickness. In both cases, no distinguishable increase related to the NQD absorption was observed. This indicates that the origin of the PV enhancement is related to intrinsic optical effects (i.e. reduced reflection and enhanced absorption).

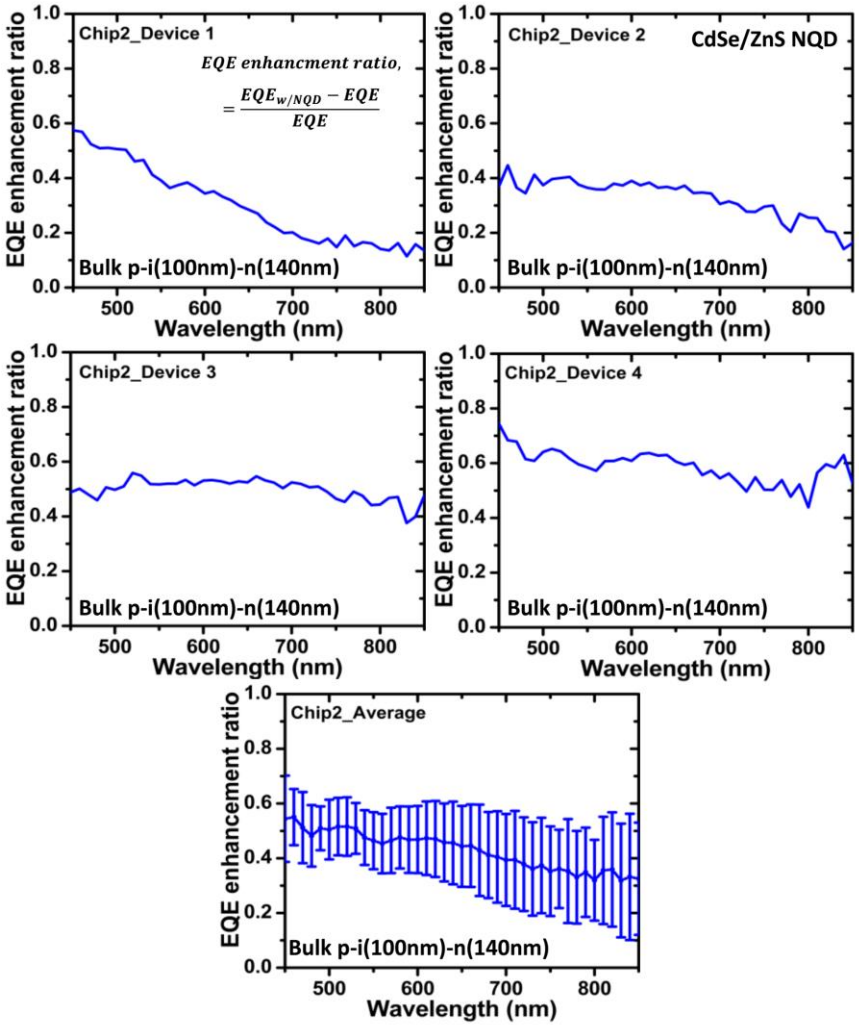


Figure 4.16. Top four graphs show EQE enhancement for individual devices from Chip-2 (bulk pSi-i(100nm)-n(140nm) poly Si SC) after ~70 nm NQD deposition. Bottom graph shows the average EQE enhancement for all the devices.

The same test was carried out for the devices comprised of thinner poly Si films. The measured and calculated EQE are shown in Figure 4.17. Here, the EQE curves are nearly identical. The EQE enhancement ratio is given in Figure 4.18 where a monotonic increase is observed, similar that seen with the thicker poly Si layers. Combined, this confirms that the PV enhancement is due to optical effects. One notable difference in the measured and calculated EQE between the thinner (Figure 4.17) and thicker (Figure 4.13) poly Si SCs is observed in the longer wavelength region. In this region, the measured EQE for the thicker poly Si SCs is larger than the calculated EQE, whereas they are the same for the thinner poly Si SCs.

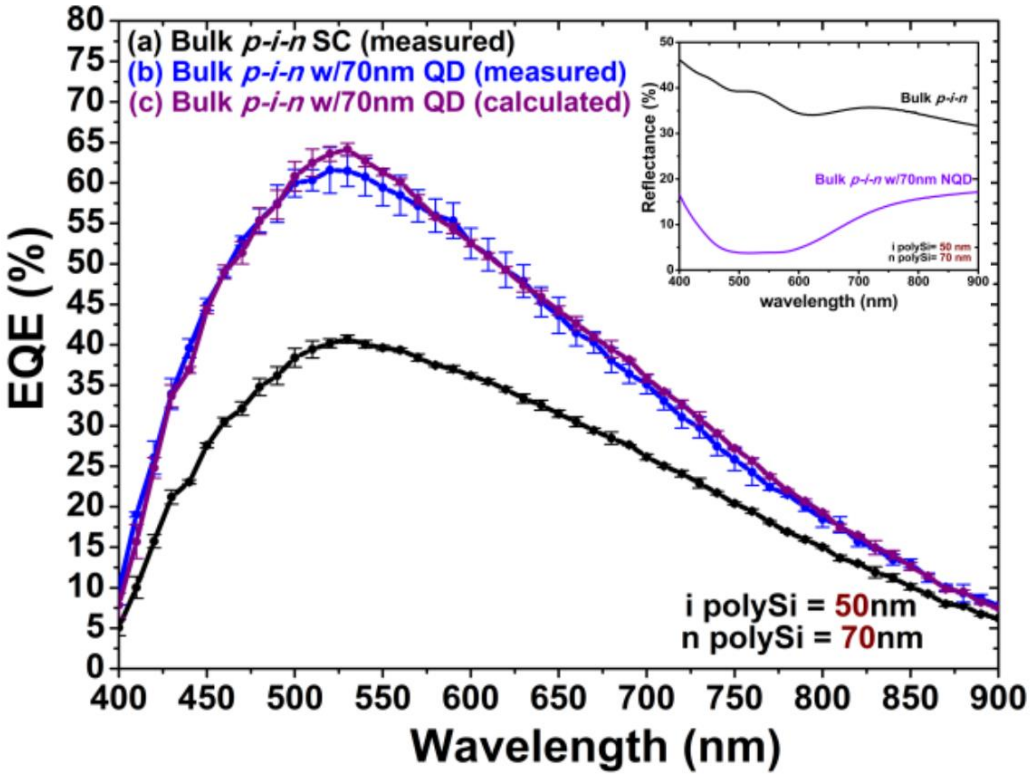


Figure 4.17. Measured and calculated EQE curves for bulk pSi-i(50nm)-n(70nm) poly Si SCs (a) bare, (b) with 70 nm of CdSe/ZnS NQDs and (c) calculated from the reflectivity measurements. Inset: reflectivity measurement for pSi-i(50nm)-n(70nm) poly Si without (black) and with 70 nm of NQDs.

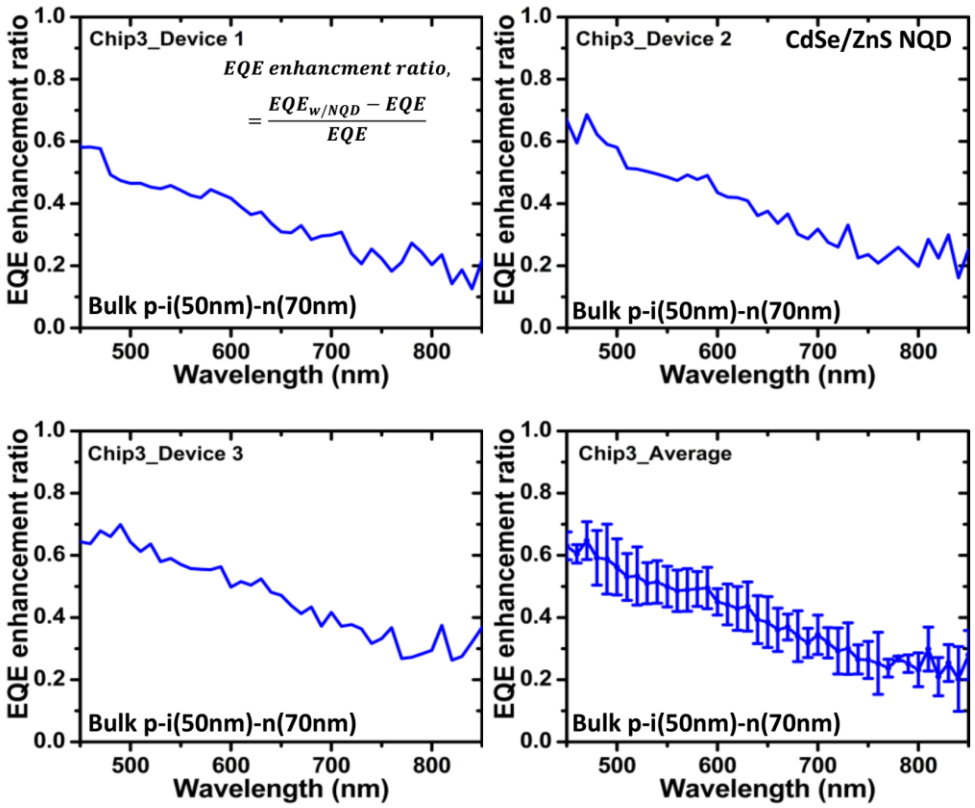


Figure 4.18. First three graphs show individual EQE enhancement for 3 devices from Chip-3 (bulk pSi-i(50nm)-n(70nm) poly Si SC) after 70 nm CdSe/ZnS NQD deposition. Last graph shows the average EQE enhancement for all the devices.

The EQE enhancement ratio vs. wavelength is also shown for NIR sensitized SCs in Figure 4.19. Again, a monotonic increase in EQE is observed with no peaks corresponding to the absorption maximum (~1000 nm) of PbS NQDs.

All systems showed a monotonic increase in EQE enhancement upon Si sensitization by proximal NQDs without maximums corresponding to the NQD absorption spectra. This highlights that optical effects (i.e. anti-reflection) are the primary origin of the observed PV enhancement in the bulk Si SC architecture. Any enhancement due to ET from NQD sensitization is very small.

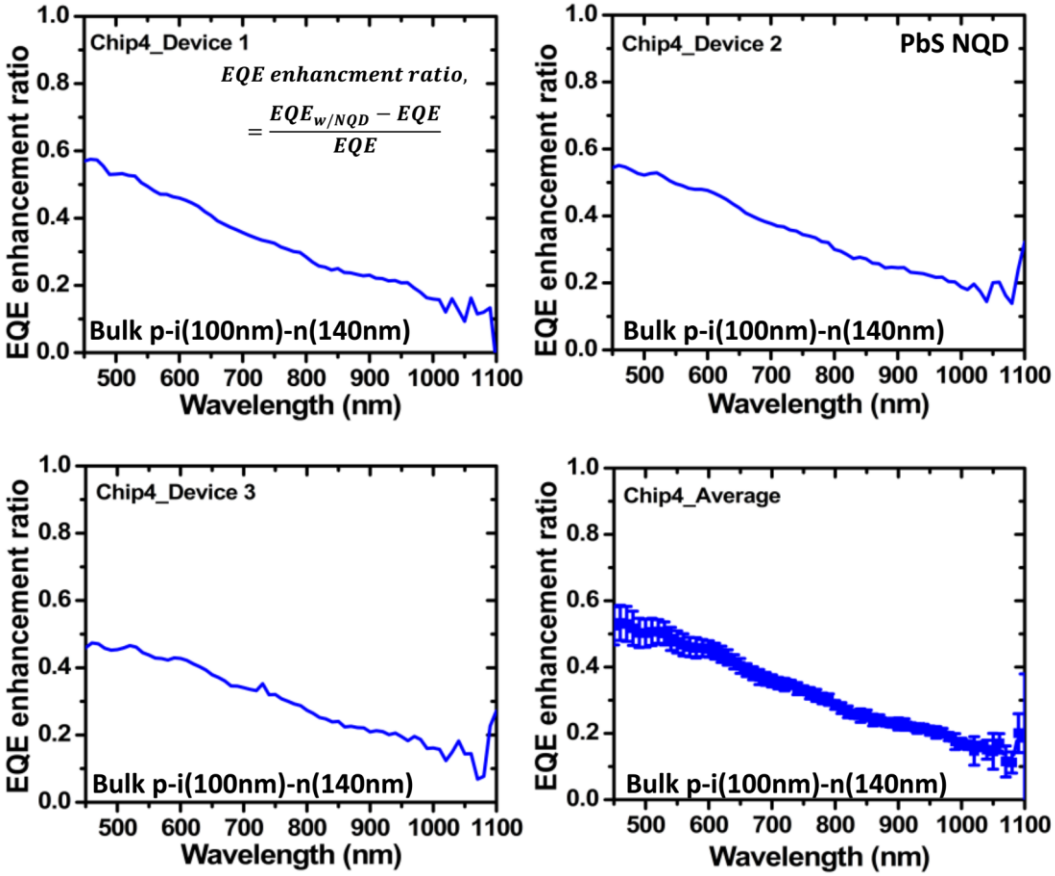


Figure 4.19. First three graphs show individual EQE enhancement for 3 devices from Chip-4 (bulk pSi-i(100nm)-n(140nm) poly Si SC) after ~ PbS NQD deposition. Last graph shows the average EQE enhancement for all the devices.

In the case of bulk Si SCs, the quantification of the contribution from ET processes is difficult due to the strong absorption of Si itself. Bulk Si (500 µm) absorbs all of the incoming solar energy at the peak absorption (~550 nm) of CdSe/ZnS NQDs. In fact, 70 nm of CdSe/ZnS NQDs only absorbs ~7% $\alpha_{CdSe} = 1.0 \times 10^4\ cm^{-1}\ @\lambda_{abs.} = 550nm$ [109] of the incoming photons at ~550 nm calculated using Beer-Lambert's law ($I = I_0 e^{-\alpha_{CdSe} l}$). Similar calculation with Si (absorption coefficient, $\alpha_{Si} = 9.3 \times 10^3\ cm^{-1}\ @\lambda_{abs.} = 550nm$) [110] having the path length of the bulk thickness ($l = 500\ \mu m$) indicates that the remaining 93% of the photons will be completely absorbed by Si. So, only 7% of the carriers will be generated due to absorption in

~70 nm of NQD layer and the remaining 93% will be generated due to complete absorption of 550 nm photons in Si. Assuming 100% carrier generation and collection efficiency, only a 7% contribution from ET processes due to ~70 nm CdSe/ZnS NQD is expected. In reality, this contribution decreases with any reductions in collection efficiency due to the fabrication steps. Thus, it is difficult to quantify ET processes in a bulk Si. However, it is likely that ET processes exists, but the carriers generated from ET will have very small contribution and are buried by carrier generation due to optical effects and absorption in bulk Si.

4.5 Conclusions

. In summary, an experimental protocol to quantify and distinguish the contribution of ET processes from intrinsic optical effects (i.e. anti-reflection) was developed. The test protocol was applied to an industrially relevant SC architecture based on bulk Si using CdSe/ZnS or PbS NQDs as absorbers. In short, a CdSe/ZnS – bulk Si hybrid SC was used as a test candidate for ET based hybrid PVs with a goal to develop an easily applicable and experimentally rooted measurement protocol for quantifying ET contributions from electrical measurements. Reflectivity measurements of samples with and without NQDs were performed and this data was used to construct EQE curves considering enhancement from purely optical effects. If the enhancement is due to ET processes, a wavelength dependent increase corresponding to the NQD absorption profile would be observed. Comparison of the measured and calculated EQE curves indicated that the ~30% PV enhancement after CdSe/ZnS NQD deposition predominately originates from optical effects. Additionally, as the absorption of bulk Si is dominant, any ET based enhancement would be very small. Thus, it is not possible to separate ET processes from optical effects in the PV enhancement of bulk Si based hybrid devices. This experimental model

to monitor and quantify ET processes from SC data is general and can be applied to other engineered PV architectures. Overall, the study of this model system and associated measurement protocol is important for future studies on SCs based on ultrathin (~100-300nm) Si.

CHAPTER 5

DESIGN APPROACHES FOR ULTRATHIN SILICON SOLAR CELLS

5.1 Introduction

In the previous chapter, the quantification of ET-generated charges using a hybrid NQD-bulk Si SC was discussed. The observed PV enhancement revealed that absorption in bulk Si dominates carrier generation and masks any contribution from ET-generated charges. Additionally, the observed enhancement was attributed to intrinsic optical effects, i.e. anti-reflection, due to the NQD layer. A simple calculation based on Beer-Lambert's law indicates that the thickness of Si needs to be significantly reduced in order to distinguish the contribution from ET-generated charges. Table 5.1 shows the percent of incoming photons at λ=550 nm absorbed for different thicknesses of the Si layer and the CdSe NQD film. The extinction coefficients for Si and CdSe NQDs are $\alpha_{Si} = 9.3 \times 10^3\ cm^{-1}$ [110] and $\alpha_{CdSe} = 1 \times 10^4\ cm^{-1}$ at λ=550 nm, respectively [109]. Assuming the thickness (l) of Si and NQD are $l_{Si} = 300\ nm$ and $l_{NQD} = 70\ nm$ and there is 100% conversion of the absorbed photons to electron-hole pairs (EHPs), then the contribution of ET-generated charges is ~ 30% (7 out of 24 total). This is significantly more than for bulk Si, where the ET generated charges are only 7% of the total. The contribution of ET-generated charges can reach ~50% if the thickness of Si is reduced below 100 nm.

Table 5.1. Percent of absorbed incoming photons at λ=550 nm for different thicknesses of Si and CdSe NQD.

Thickness (nm)	Si	CdSe NQD
	Absorbed incoming photon for λ=550 nm (%)	Absorbed incoming photon for λ=550 nm (%)
50	3	5
70	4	7
100	6	10
300	17	26
500	27	40
1000	47	63

In our study, 300 nm silicon on insulator (SOI) wafer are utilized as the starting thickness of Si for the fabrication of an ultrathin vertical p-i-n SC. While previous efforts to quantify ET generated charges were carried out with a Schottky type thin (500 nm) and lateral SC architecture, this is not relevant to the PV community as Schottky SCs are not used widely used. Therefore, designing an industrially used vertical p-i-n structure that is sensitized with NQDs is relevant to the entire PV community.

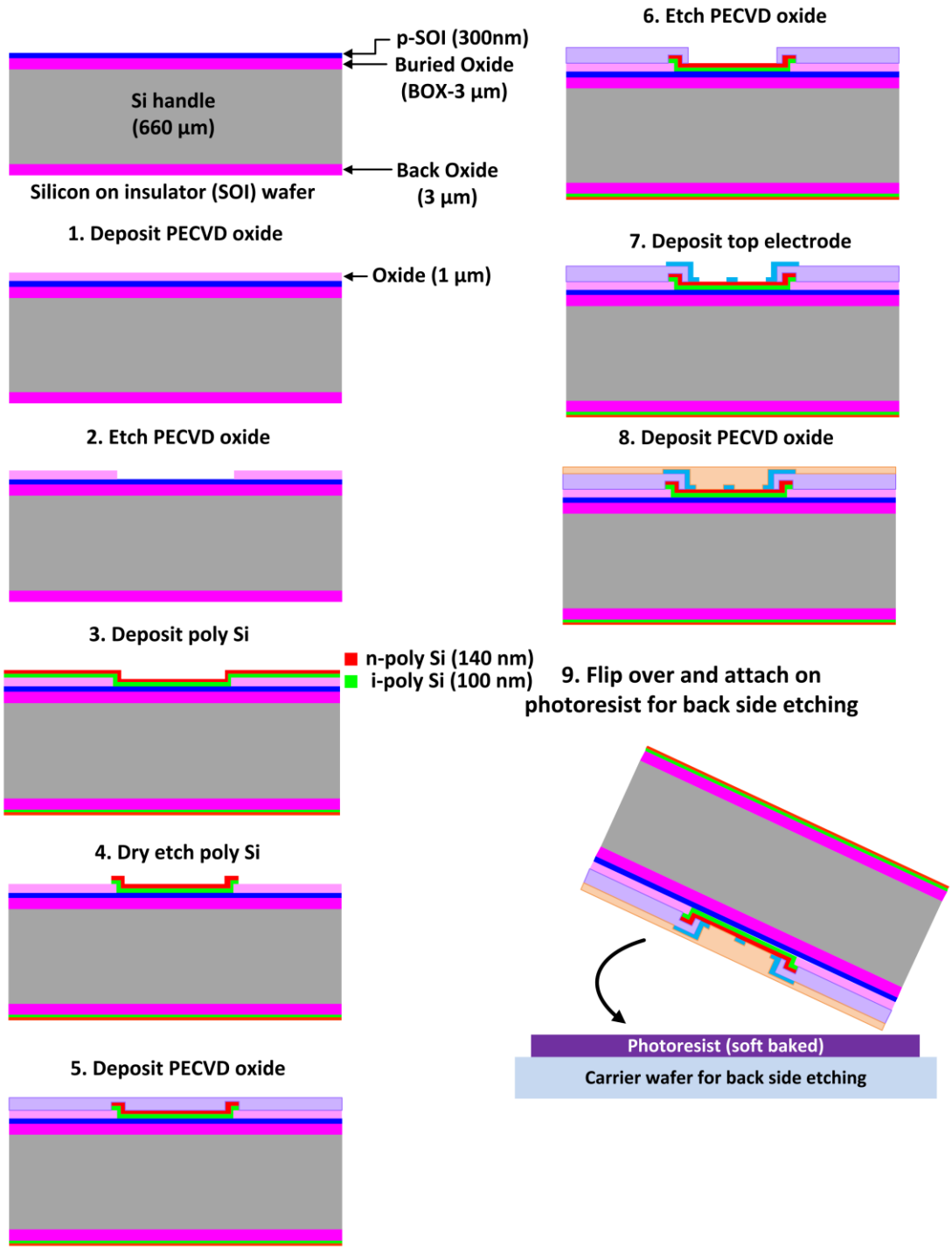
In this chapter, we discuss the approaches that have been taken to fabricate an ultrathin Si SC based on 300 nm p-type (~10^{15} cm^{-3}) SOI wafers. First, the general approach to fabricate these devices is discussed. As a note, the process flow was created with the eventual goal to incorporate NQDs into the devices in mind. Then, major challenges are identified and the process is modified to overcome these roadblocks. For instance, one major challenge is related to mechanical and thermal stresses on the free standing (suspended) ultrathin SOI films. Careful design optimization helped reduce stress and thereby increase the mechanical and structural yield of the suspended SOI devices. The as-fabricated devices were characterized electrically revealing

I-V characteristics of a highly resistive diode with an enhanced photo-response under 1 Sun AM1.5 G illumination.

Overall, an integrated design approach to fabricate ultrathin Si SCs for the quantification of ET-generated carriers from NQDs is proposed. The resulting devices are suspended over an etch hole (500-600 μm in diameter) and constitute a vertical p-i-n type structure. The devices act as ultrathin Si photodetectors which can be improved to impart photovoltaic behavior. Overall, this work provides guidelines for design parameters to fabricate stress-minimized defect-free ultrathin Si devices.

5.2 Fabrication steps of ultrathin SOI devices

This section introduces the general processing steps to fabricate ultrathin devices from a 300 nm SOI wafer. Subsequent sections discuss the roadblocks faced in the development of the fabrications and solutions to these challenges. Figure 5.1 shows the simplified process flow. The starting SOI wafers are Boron doped and p-type with (100) crystal orientation and 300 nm thickness. The resistivity is 500 Ω-cm corresponding to a doping density of ~ 10^{15} cm^{-3}. The thickness of the buried oxide (BOX) is 3 μm. The thickness of the Si handle is 660 μm. Wafers are 150 mm in diameter. A schematic diagram of the completed SOI device suspended over an etch hole of ~1000 μm is shown in Figure 5.2. The completed device has a top electrode (~ 130 nm), passivation layer (~ 500 nm) and bottom electrode (~80 nm) suspended over the entire etch hole. After fabrication, the total thickness of the active device is ~540 nm.


p-SOI (300nm)
Buried Oxide
(BOX-3 µm)
Si handle
(660 µm)
Back Oxide
(3 µm)
Silicon on insulator (SOI) wafer
1. Deposit PECVD oxide
Oxide (1 µm)
2. Etch PECVD oxide
3. Deposit poly Si
n-poly Si (140 nm)
i-poly Si (100 nm)
4. Dry etch poly Si
5. Deposit PECVD oxide
6. Etch PECVD oxide
7. Deposit top electrode
8. Deposit PECVD oxide
9. Flip over and attach on
photoresist for back side etching
Photoresist (soft baked)
Carrier wafer for back side etching

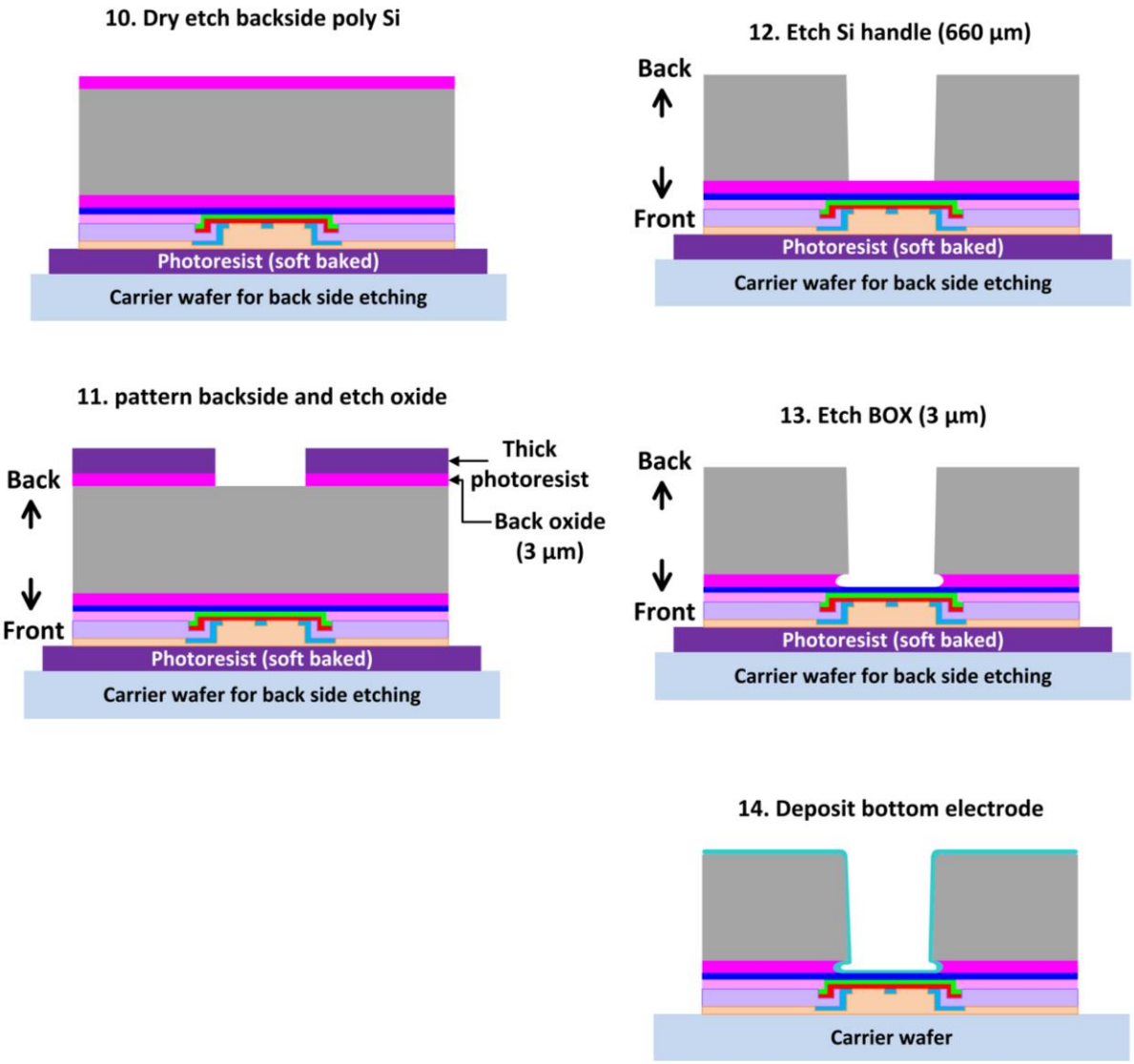


Figure 5.1. Simplified processing steps for the fabrication of a n ultrathin p-i-n Si SC based on 300 nm SOI.

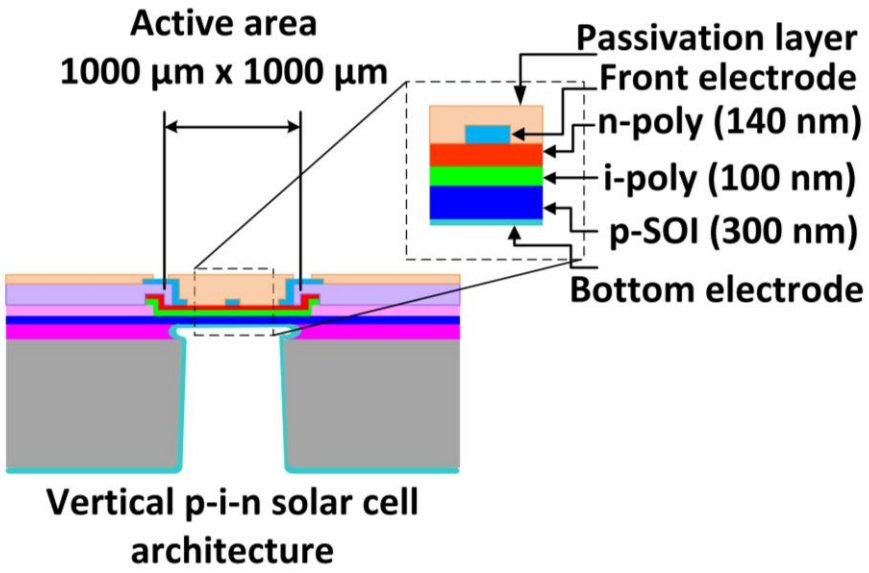


Figure 5.2. Schematic of the free standing SOI based Si p-i-n SC after all fabrication steps are complete.

Detailed fabrication steps:

1. A 65 mm x 35 mm piece is cut from the SOI wafer. This piece contains 8 chips. Each chip has an area of 15 mm x 15 mm and 8 devices with an active area 1000 µm x 1000 µm. From each piece, 64 devices are fabricated.

Mask layer 1: Wet etch oxide to deposit poly Si

2. The SOI piece is cleaned with isopropanol (IPA), acetone and de-ionized (DI) water for 1 minute by ultrasonication.
3. PECVD oxide (~ 1 µm) is deposited using the standard PECVD oxide recipe at 250 ^{o}C.
4. The sample is cleaned with IPA, acetone and DI water for 1 minute by ultrasonication.
5. A positive photoresist (S1813) is spun cast on the sample by spinning at 2000 rpm (acceleration 1000 rpm) for 60 s.
6. The wafer undergoes a soft-bake at 115 ^{o}C for 2 min.

7. M***ask 1*** is used to pattern the active area on the deposited oxide. The wafer is exposed to the g-line of the UV lamp at 130 mJ/cm^2.
8. The sample is developed with MF 319 developer for 55 s and then cleaned with DI water and dried under N_2.
9. The wafer is ashed using O_2 plasma (200 mTorr, 200 W) for 15 s to remove unwanted photoresist from the active area.
10. The sample undergoes a hard bake at 115 ^oC for 8-10 min.
11. The PECVD oxide is etched using BOE 7:1 (NH_4F: HF) for 1 min 30 s to open the active area.
12. The sample is rinsed with DI water and dried under N_2, before rinsing with acetone for 1 min. by ultrasonication.
13. Subsequently, O_2 plasma (200 mTorr, 200 W) for 5 min. is used to completely remove the photoresist.
14. The wafer is cleaned in IPA, acetone and DI wafer for 1 min. by ultrasonication.
15. Intrinsic poly Si (100 nm) and phosphorus doped n-type poly Si (140 nm) are deposited by LPCVD at 625 ^oC.

Mask layer 2: Etch poly Si to isolate devices

16. The sample is cleaned with IPA, acetone and DI water for 1 min. by ultrasonication.
17. Steps 5 and 6 are repeated.
18. M***ask 2*** is used to etch the poly Si and isolate the devices by exposing the wafer to g-line of the UV lamp (130 mJ/cm^2).
19. Steps 8-10 are repeated.

20. Cl_2 based dry plasma etching is used to etch the poly Si. Here, the PECVD oxide acts as an etch stop layer. *Process parameters*: chamber pressure (5 mTorr), Cl_2 flow (20 sccm), electrode temperature (60 ^oC), bias forward power (50 W) and ICP forward power (150 W). The etch rate is 98 nm/min.
21. Rinse with acetone for 1 minute under ultrasonication. Subsequently use O_2 plasma (200 mTorr, 200 W) for 5 min. to completely remove photoresist.
22. The wafer is cleaned in IPA, acetone and DI wafer for 1 min. by ultrasonication.

Mask layer 3: Deposit oxide to electrically isolate deposited poly Si layers and etch oxide to open active area for subsequent top electrode deposition

23. Deposit PECVD oxide (~1 μm).
24. Steps 5 and 6 are repeated.
25. M***ask 3*** is used to open the active area on the deposited oxide by exposing the wafer to g-line of the UV lamp (130 mJ/cm^2).
26. Steps 8-14 are repeated.

Mask layer 4: Deposit top electrode

27. Steps 5 and 6 are repeated
28. ***Mask 4*** is used to pattern the photoresist for top electrode deposition by exposing the wafer to g-line of the UV lamp (130 mJ/cm^2).
29. Steps 8-10 are repeated.
30. Al (130-150 nm) is deposition in a cryo e-beam evaporator (without rotation) at a deposition rate of 1-2 Å/s.

31. Lift-off the deposited metal in ethanol at 60 ^{o}C on a hot plate. Provide ethanol during the process to avoid drying of the solution. Short periods of ultrasonication speed up the process. Alternatively, lift off can be done by leaving the sample in acetone overnight at room temperature and finishing the lift-off process in the morning in ethanol.
32. After lift-off, the sample is rinsed with acetone for 1 min. by ultrasonication. Then, O_2 plasma (200 mTorr, 200 W) for 5 min is used to completely remove photoresist.
33. The wafer is thoroughly rinsed with DI wafer and dried with N_2.

Mask layer 5: Open via in the oxide to contact the top electrode

34. PECVD oxide or nitride (~2 μm) is deposited as the front passivation (or protection) layer.
35. Steps 5 and 6 are repeated
36. M***ask 5*** is used to open the via in the oxide (or nitride) layer by exposing the wafer to g-line of the UV lamp (130 mJ/cm^2).
37. Steps 8-13 are repeated. However, here, the BOE etch is carried out for 3 min.
38. Then, the wafer is rinsed thoroughly with DI wafer and dried with N_2.

Mask layer 6: Pattern backside of the wafer to etch Si handle, BOX and deposit bottom electrode

39. The poly Si on the back is etch according to step 20.
40. A positive photoresist (SIPR 7126M) is spun cast on the sample by spinning at 3000 rpm (acceleration 1000 rpm) for 60 s.
41. The wafer undergoes a soft-bake at 115 ^{o}C for 2 min.
42. ***Mask 6*** is used for backside alignment by exposing the wafer to g-line of the UV lamp (700 mJ/cm^2).

43. The sample is developed with MF 26A for ~ 8-10 mins.
44. Then, the sample undergoes a hard bake at 115 ^{o}C for 10 min.
45. A positive photoresist (SPR 220 7.0) is spun cast at 4500 rpm (acceleration 1000 rpm) for 60 s on a clean 4-inch carrier wafer to coat the wafer with 2 µm thermal oxide. The device is place top side down on the carried wafer this undergoes a soft bake at 115 ^{o}C for 2 min.
46. The photoresist at the edge (>2mm) of the carrier wafer is removed with acetone using cleanroom swabs. Then, a hard bake at 115 ^{o}C for 5 min is carried out.
47. The backside oxide (3 µm) is etched using the PE04 dry plasma system. *Process parameters:* time (800 s), chamber pressure (10 mTorr), gas flow (CHF_3@40 sccm, Ar@10 sccm), RF forward bias power (100 W), ICP forward bias power (800 W) and electrode temperature (20 ^{o}C). The etch rate is 3.75 nm/s.
48. The Si handle (660 µm) is etched using the Bosch process recipe (DSE 100) in the PE04 dry plasma system until only ~100 µm of Si handle is remaining.
49. The device wafer is detached from the carrier wafer using photoresist stripper (AZ400T).
50. The device wafer is placed on a clean carrier wafer with 2 µm thermal oxide and placed back in the PE04 plama system. Using the DSE 100 recipe, the wafer is etched until only ~50 µm of the handle remain.
51. The remaining handle is removed as described in Section 5.4 (2).
52. The BOX (3 µm) is etched using the PE04 dry plasma system to release the suspended SOI device. *Process parameters:* time (2737 s), chamber pressure (10 mTorr), gas flow (CHF_3@40 sccm, Ar@10 sccm), RF forward bias power (50 W), ICP forward bias power (500 W) and electrode temperature (20 ^{o}C). Etch rate: 1.09 nm/s.

53. The released device is mounted on a clean carrier wafer for bottom electrode deposition. Cr/Au (3/70 nm) or Cr/Cu (3/70 nm) is deposited using the CHA e-beam evaporator. The *'Planetary'* accessory is used for sidewall coverage. The deposition rate is ~0.5 Å/s for Cr and ~ 1 Å/s for Au and Cu deposition.

5.3 Defects in the suspended SOI films

From the fabrication process, the resulting ultrathin devices are very fragile and any stress can cause cracks or fractures which is detrimental to the device performance. For instance, shorting between the top and bottom electrodes can occurs due to defects in suspended SOI films. Most defects are related to mechanical stress. In this regards, the process flow must be designed so that a reasonable number of devices show diode behavior. In fact, without proper optimization of the process flow the chance of achieving a suspended SOI diode is low.

To understand the defect formation, the suspended SOI film is imaged with SEM and optical microscopy before the deposition of the top and bottom electrodes. An early device is shown in Figure 5.3 where most of the suspended SOI films were destroyed. The thin SOI can be suspended over large distances up to ~5 mm (see Figure 5.3 inset (b)). However, the mechanical and structural integrity is very low.

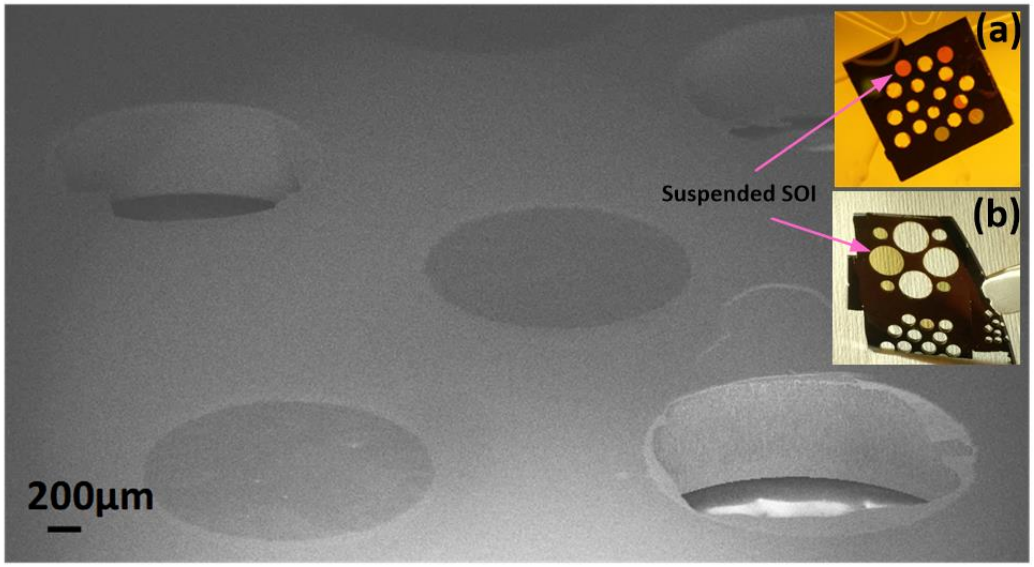


Figure 5.3. SEM image showing a free-standing SOI (without top and bottom metal electrodes) suspended over a 1.5 mm diameter etch hole. The inset (a and b) show chips with several etch holes with a diameter of 1.5 and 5 mm, respectively. Most of the suspended SOI films are destroyed after the full processing cycle due to induced mechanical and structural stress.

In addition to breaking as seen in Figure 5.3, different defects can occur during the etching of the Si handle. Defects include partial fracture, large or small pinholes, fracture at the edges of the etch hole. Optical images of these defects are shown in Figure 5.4 (a) for SOI suspended over a ~1.5 mm etch hole. Additionally, wrinkles can form due to stress in the SOI film as seen in Figure 5.4 (b). While these films are continuous, wrinkles increase the probability of stress induced cracks. Even if a film appear continuous, closer examination often reveals small pinholes (~3 µm) which can result in electrical shorting upon electrode deposition (Figure 5.4 (c)). To minimize these defects, the design process needs to be optimized to achieve a flat, free-standing SOI film.

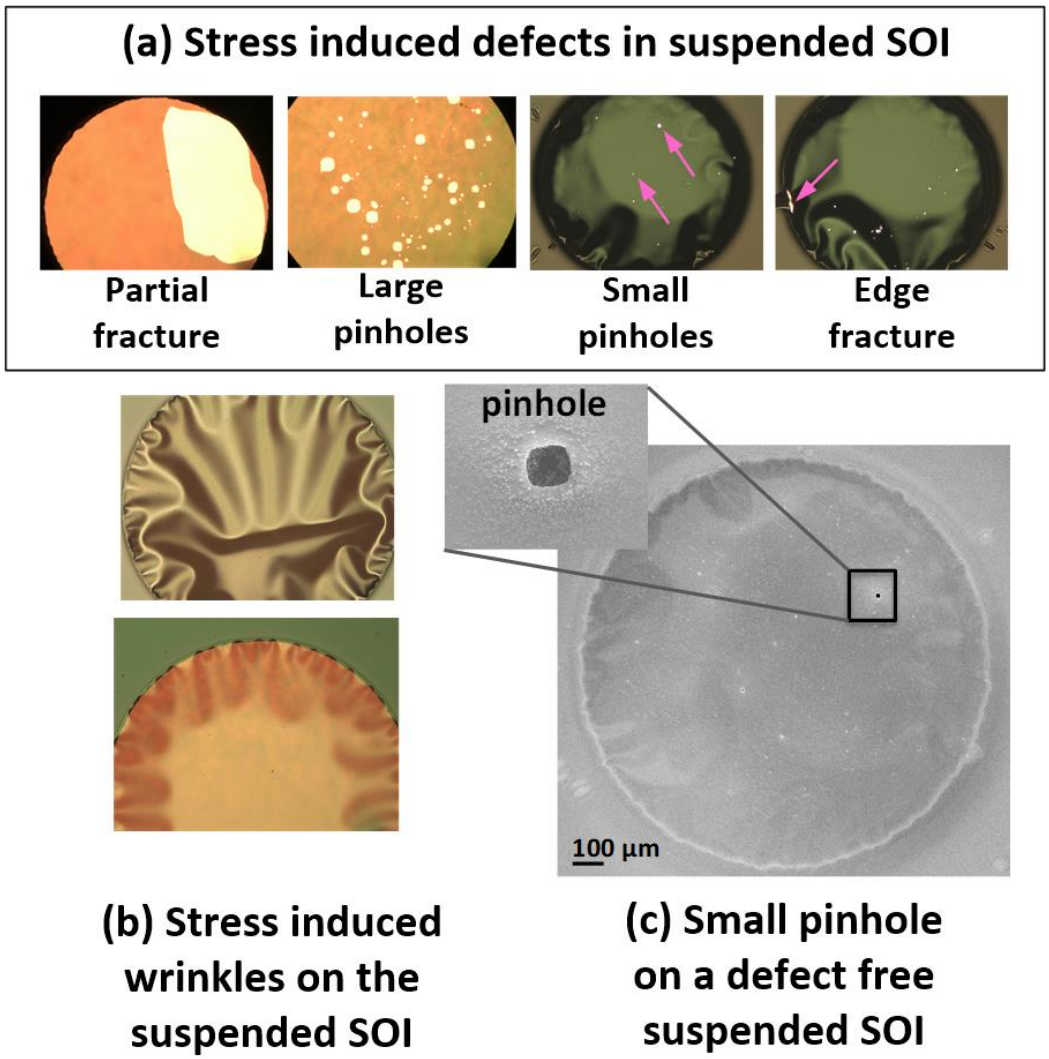


Figure 5.4. Stress induced defects in free standing SOI films suspended over a 1.5 mm diameter etch hole. (a) Optical images showing different defects observed after the process completion. (b) Optical images of wrinkled SOI films due to stress either over the entire film or at the edges (c) SEM image showing small pinholes in an otherwise defect free suspended SOI. The size of the pinhole is ~ 3 µm.

5.4 Design considerations

This section introduces five key manufacturing roadblocks (Figure 5.4) encountered during the design process and methods around them. Through process optimization, these challenges were overcome and resulted in improve yield of suspended SOI devices.

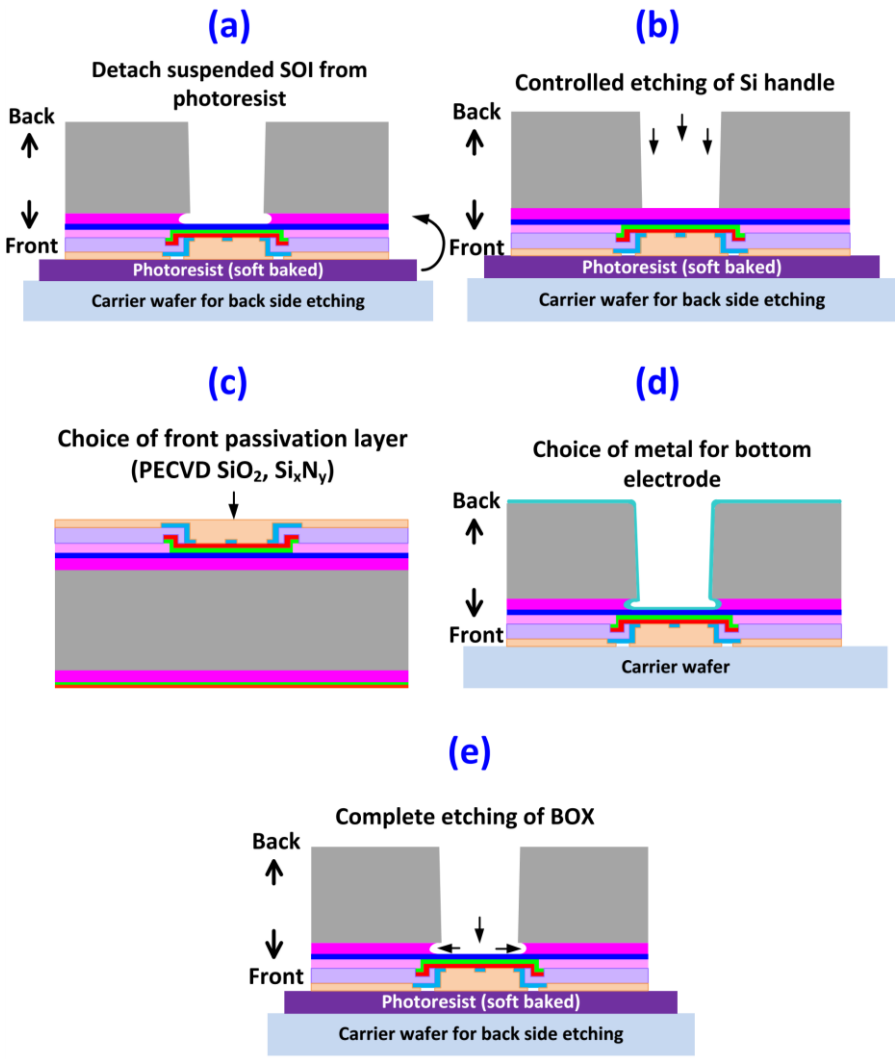


Figure 5.5. Schematic showing five major roadblocks encountered during the design of suspended SOI based Si SC. These include (a) stress reduction during detachment of the suspended SOI films from the photoresist, b) controlled etching of the Si handle (660 µm) to reduce stress, (c) selection of front passivation layer to prevent etching the front of the SOI film, (d) bottom electrode metal selection to reduce thermally induced stress, and (e) removal of BOX (3 µm) layer for electrical contact at the back.

(1) Detaching the suspended SOI film from the photoresist:

In order to etch the Si handle, the front side of the chip containing the suspended SOI devices needs attached to a carrier wafer. Samples are usually attached using a heat sink compound (Dow corning 340) which helps conduct heat and protect the photoresist during

prolonged etching at elevated temperature. However, this leaves a residue on the wafer surface even after cleaning. A clean alternative is to use photoresist which can prevent travel of etchant atoms from the back of device wafer. However, heat conduction is poor. Additionally, the photoresist hardens at elevated temperature and then stripping becomes problematic and can cause unwanted stress (Figure 5.6 (a)). This results in the destruction of most of the suspended SOI films.

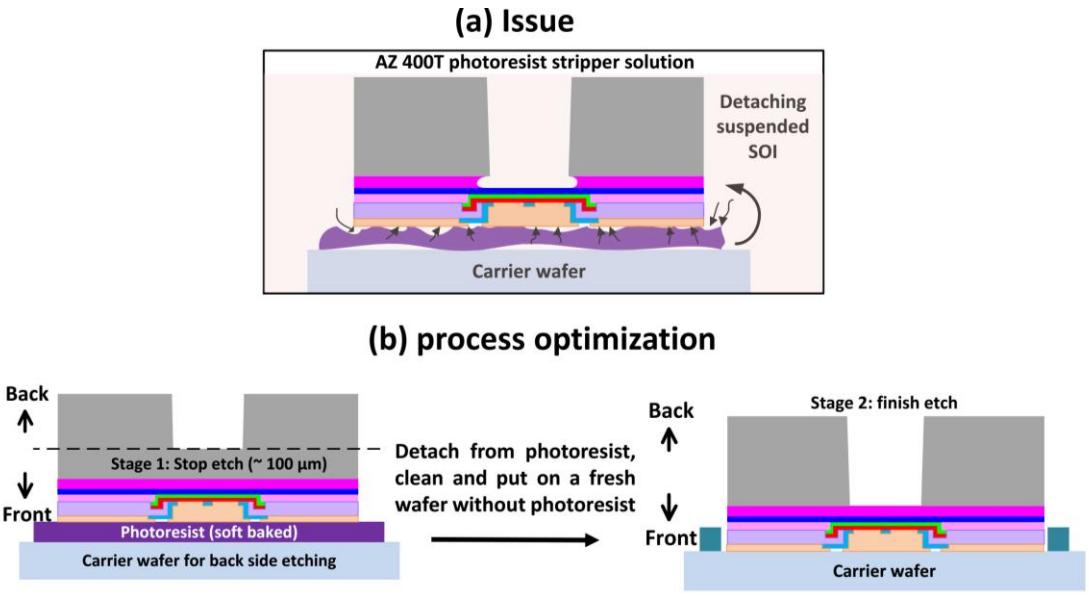


Figure 5.6. (a) Schematic showing the stress induced during photoresist stripping in AZ400T stripper solution. (b) Schematic showing a 2- step process that that overcomes this problem.

To overcome this issue, a two-step process was developed as shown in Figure 5.4 (b) which results in improved device yield. Here, the etching of the Si handle is stopped when ~ 100 µm remains. Then, the device wafer is detached from the photoresist. The 100 µm Si handle provides enough mechanical stability to prevent damage to the SOI. The newly detached wafer is place on a clean carrier wafer coated with 2 µm thermal oxide. To prevent slippage, Si pieces at

attached with thermal past to the carrier wafer around the device wafer. The remainder of the Si handle is etched at this configuration.

(2) Controlled etching of Si handle:

If was found that if the Si handle is fully etched according to the Bosch process, the yield of suspended SOI devices is low (Figure 5.7 (a)). The Bosch process [44, 111] is a fast and highly anisotropic Si etching process. It is widely used for fabricating Si nanostructures, such as nanotrenches [112], nanopillars [113, 114] and hollow nanopillars [115] . The process involves two steps. First, SF_6 is used to etch Si. Then, octaflurocyclobutane (C_4F_8) is introduced to passivate the side walls. During the SF_6 pulse, Si is etched in all direction. However, deposition of C_4F_8 significantly reduces lateral etching. Etching is continued until the desired etch depth is achieved. The recipe has a high etch rate which can results in stress that leads to SOI fracture. Additionally, it results in 'scalloped' sidewall structures [44, 116-119], but in our case, this 'scalloping' is not important. Table 5.2 provides the process parameters used here.

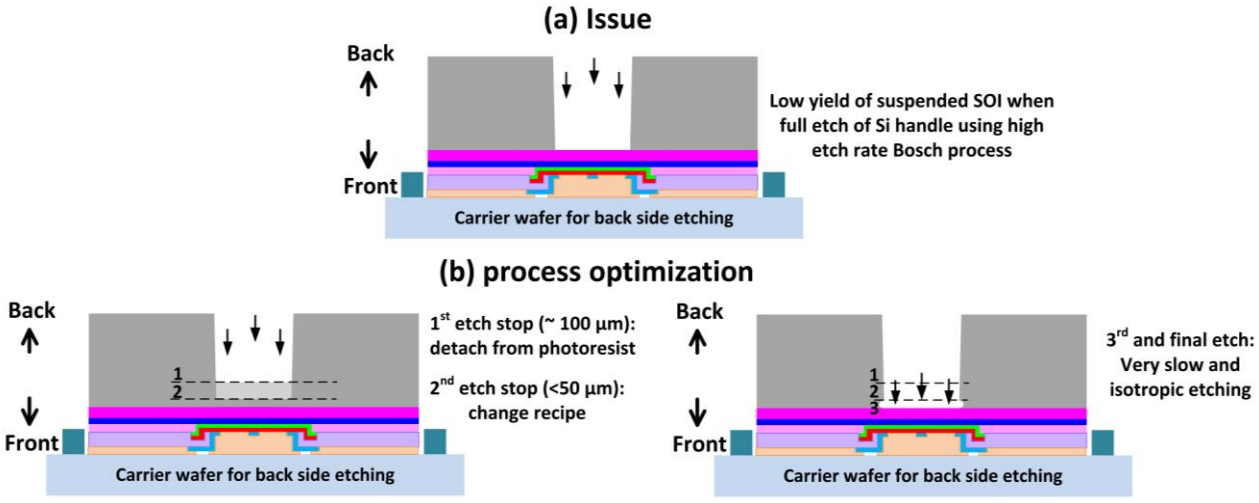


Figure 5.7. (a) Schematic showing the low yield of suspended SOI film when the Si handle is completely etched by the Bosch process. (b) Schematic showing the optimized multiple step etching process.

Table 5.2. Process parameters for the Bosch process (labeled ‘DSE 100’).

Process parameter (Alternating etch A and B constitute 1 cycle)	Etch A	Etch B
	C_4F_8	SF_6
Time (s)	2	4
Pressure (mTorr)	20	30
Gas flow (sccm)	30	100
Bias Power (W)	11	250
ICP forward power (W)	1200	1200
Temperature (^oC)	180	180

To fully etch the Si handle while retaining intact SOI films, the process was optimized as shown Figure 5.7 (b). Instead of a single Bosch process, the etching of the Si handle was divided into 3 steps and this significantly improved the suspended SOI device yield.

Etch stage 1: The Bosch process is used to achieve an etch depth target of ~ 560 µm. At this point, ~100 µm of the Si handle remains. The device wafer is detached from photoresist and cleaned for the next stage.

Etch stage 2: The SOI device wafer is placed on a carrier wafer without photoresist. The Bosch process is carried out to achieve an etch depth target ~ 610-620 µm. At this point, ~ 50 µm of the Si handle remains.

Etch stage 3: The remaining 50 µm are etched using a low etch rate at room temperature which reduces stress on the suspended SOI devices. Here, SF_6 is the only gas and thus the etching profile is isotropic. The process parameters for this etch are: chamber pressure (5 mTorr), gas flow (SF_6@20 sccm), RF forward bias power (10 W), ICP forward bias power (600 W) and electrode temperature (30 ^oC).

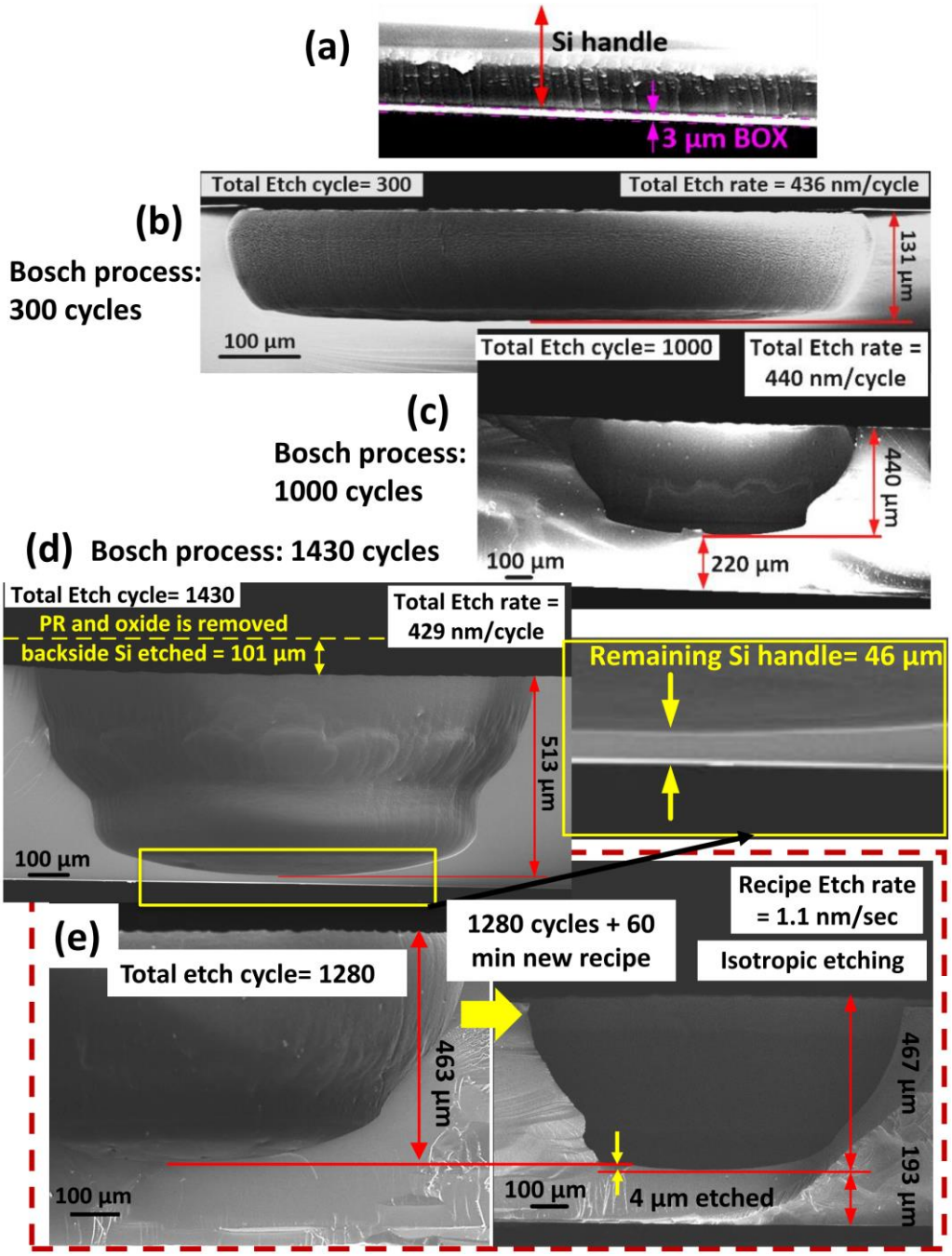


Figure 5.8. SEM images showing the etch depth and etch rate during different cycles of the Bosch process. SEM image of the SOI wafer with 3 µm BOX (a) before etching, (b) after 300 cycles when 131 µm Si has been etched, (c) after 1000 cycles when 440 µm has been etched, (d) and after 1430 cycles when 614 µm of Si has been etched and 46 µm of the Si handle remains, (e) etch rate of new oxide recipe determined as 1.1 nm/sec from the 4 µm Si etched after 60 mins of new recipe.

Figure 5.8 shows the progression of the different etching steps as described above. Before the start of etching, the Si handle rests on 3 µm BOX (Figure 5.8 (a)). The etch rate of the 'DSE 100' recipe was determined from SEM analysis of the wafer after a certain number of cycles and found to be ~435 ± 5 nm/cycle for a patterned etch hole diameter of 800 µm. For instance, after 300 cycles, 131 µm of the handle was etched resulted in a rate of ~ 436 nm/cycle (Figure 5.8 (b)). According to the estimated etch rates, '**etch stage 1**' is stopped after ~ 1250 cycles and '**etch stage 2**' is after ~ 1430 cycles. At the end of "etch stage 2" ~ 46 µm of the Si handle remains (Figure 5.8 (d)). Additionally, the photoresist, backside oxide and ~100 µm Si was etched during '**etch stage 2**' (Figure 5.8 (d)).

At this point, '**etch stage 3**' is carried out. The etch rate is again estimated from SEM images taken after different etching times and found to be ~ 1.1 nm/s (Figure 5.8 (e)). 'The slow Si etch is frequently paused to allow the device wafer to be checked optically to make sure the sample is not over etched. The etching is stopped when a ~ 500-600 µm etch hole is created.

(3) Choice of front passivation (etch protection) layer:

Passivation of the front of the SOI device is necessary to protect from etching. The SF_6 gas used to etch Si can enter from side of the wafer. This results in etching of the active area from the side in. Initially, PECVD Si_xN_y was used as the front passivation layer. However, thick (~2-3 µm) Si_xN_y films produce excessive tensile stress [120, 121] on the suspended SOI films which can cause fractures (Figure 5.9 (a)).

To reduced stress, ~2 µm PECVD SiO_2 is used as the front passivation layer. After '**etch stage 1**' and detachment from the carrier wafer, the SiO_2 layer is removed by wet etching. Then a thin (~300-500 nm) layer of SiO_2 is deposited on the top surface of the devices. A via is opened

for electrical connection to the front electrode is opened by wet etching in BOE solution for 30-45 s. The SOI device wafer is place top side down on a clean carrier wafer '**etch stage 2 and 3.**' It is important to note that PECVD SiO_2 produces film with compressive stress [122, 123]. Thus, optimization of thickness will be necessary for further stress reduction.

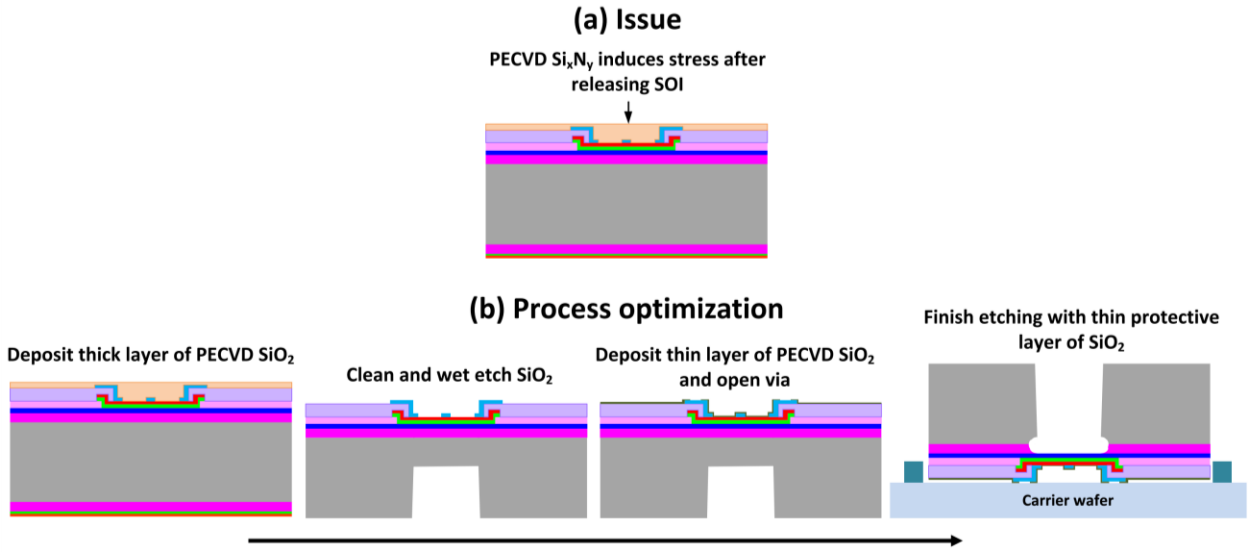
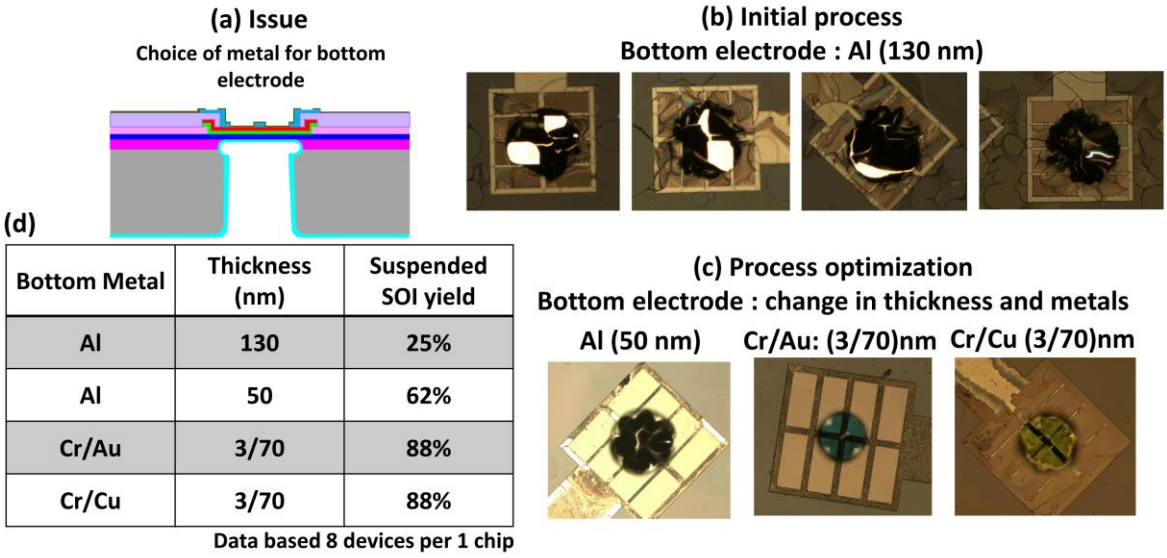


Figure 5.9. (a) Schematic showing ~2 µm PECVD Si_xN_y deposited over the suspended SOI film. (b) Schematic of the process optimization to overcome this problem. Here, ~2 µm PECVD SiO_2 is used as a protective layer in the 1st step. Then a thin (~300-500 nm) SiO_2 layer is deposited on top as protective layer for the final etching stages.

(4) Choice of metal for bottom electrode:

The choice of metal for the bottom electrode is important due to stress originating from a mismatch in the linear thermal expansion coefficient (α) (Figure 5.10). Initially, Al was used to form ohmic contact to p-type SOI. However, Al has a ~ 5 times higher thermal expansion ($\alpha_{Al} = 24 \times 10^{-6}/℃$) [124] coefficient than Si ($\alpha_{Si} = 5 \times 10^{-6}/℃$) [124] which led to fractures in the SOI devices (Figure 5.10 (b)). With 130 nm Al election, the defect free device yield was ~ 25% (Figure 5.10 (d)).



Bottom Metal	Thickness (nm)	Suspended SOI yield
Al	130	25%
Al	50	62%
Cr/Au	3/70	88%
Cr/Cu	3/70	88%

Data based 8 devices per 1 chip

Figure 5.10. (a) Schematic showing the stress induced due to bottom electrode. (b) Optical images showing fractures in suspended SOI film after depositing thick (~ 130 nm) Al films. (c) Optical images showing suspended SOI devices electrodes comprised of thinner Al (50 nm), Cr/Au and Cr/Cu. (d) Table of the mechanical and structural yield of the suspended SOI devices with different metals and thicknesses.

It is found that thickness of the deposited metal plays an important role in the device yield. Decreasing the thickness of Al from 130 nm to 50 nm improved the defect free suspended SOI yield to 62% (Figure 5.10 (c) and (d)). The yield of defect free suspended SOI can be increased to 88 % choosing metals with low thermal expansion coefficient that are comparable to Si. In this case, Cr ($\alpha_{Cr} = 6.2 \times 10^{-6}/°C$), Au ($\alpha_{Au} = 14.2 \times 10^{-6}/°C$) and Cu ($\alpha_{Cu} = 16.5 \times 10^{-6}/°C$) [124] were used. Here, the yield of defect free suspended SOI is substantially improved using Cr/Au (3/70 nm) and Cr/Cu (3/70 nm) (Figure 5.10 (d)). Figure 5.10 (c) shows optical images of the devices with Cr/Au and Cr/Cu as the bottom electrode.

(5) Complete removal of BOX:

Before depositing metal to from the bottom electrode, the BOX (3 µm) needs to be completely etched. Incomplete removal of BOX layer acts as an insulator towards electrical

connection between the top and bottom electrode. The schematic in Figure 5.11 show the issue and approach to process optimization for overcoming this problem.

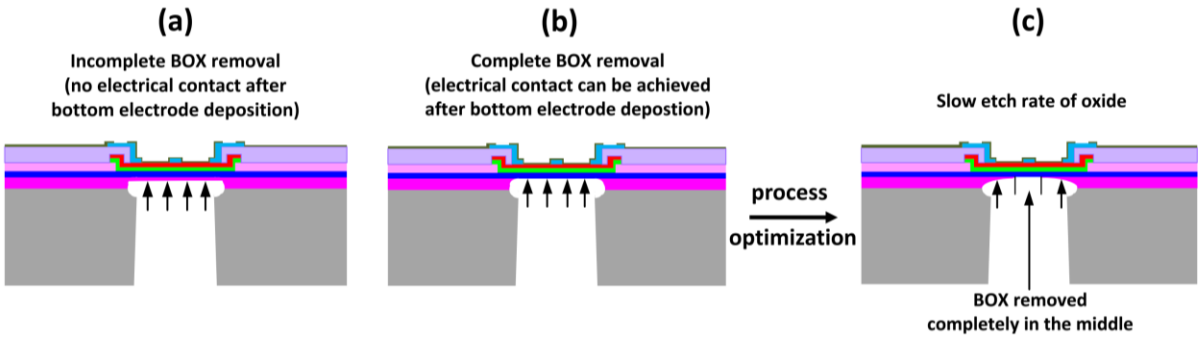


Figure 5.11. (a) Schematic showing how incomplete removal of the BOX (3 µm) layer prevents an electrical connection after bottom electrode deposition. (b) Complete removal of the BOX is necessary to achieve an electrical connection. (c) Using a slow and isotropic etch recipe allows complete removal of the BOX layer from the middle of the device.

Initially, the time to etch the BOX was based on the etching speed of blank water. The etch rate for a standard oxide plasma etch recipe (*process parameters*: pressure - 10 mTorr, gas flow - CHF3 @ 40 sccm, Ar @ 10 sccm, RF forward power -1 00 W, ICP forward power - 800 W, temperature - 20 ^{o}C) is 3.8 nm/s. Etching a blank Si wafer with 2 µm thermal oxide took 790 s. Based on the determined etch rate of oxide, it was estimated that a total etching time of 800 s (790 s +10 s) was necessary for complete BOX removal. Figure 5.12 (a) shows a series of optical images of a suspended SOI device at different stages of etching. The suspended SOI remains defect free at all stages. However, the corresponding I-V curve (Figure 5.12 (b)) show pA current indicting no electrical connection between the top and bottom electrodes due to incomplete BOX removal. From this, it is clear that the etching rate inside the etch hole (depending on the size of the pattern) is very different than on a blank wafer. Increasing the etch time to >900 s decreased the yield of defect free SOI, however, the BOX is not completely removed at this time.

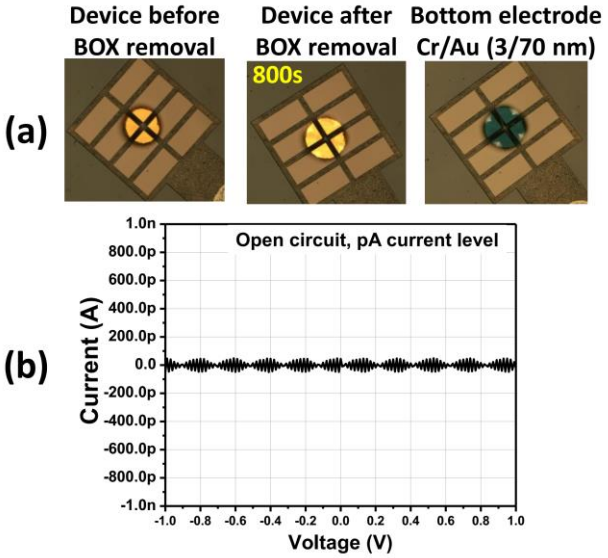


Figure 5.12. (a) Optical images (illuminated from back) showing suspended SOI devices before BOX removal, after 800 s etching and after deposition of theCr/Au back electrode. (b) I-V curve of the above device. The open circuit device behavior indicates presence of an insulating layer in between SOI and bottom electrode.

Complete removal of the BOX is necessary for electrical contact; however, the process must be modified as simply increasing the etch time is not sufficient. An optimized process based on a very slow and isotropic etching recipe is proposed in Figure 5.11 (c) to overcome this problem. The slow etch will facilitate finding the exact time required for complete BOX removal. Figure 5.13 shows a series of optical images taken at different times during the BOX etch. Due to the isotropic nature of the etch recipe, the BOX is complete etched only in the center of the etch hole. A clean outline can be seen corresponding to complete removal of the BOX after 2737 s (shown as the dark blue arrows in Figure 5.13 (c)). The suspended SOI device remains defect free during the full oxide etching process as well as after Cr/Cu deposition (Figure 5.13 (d)). The I-V characteristics of this device are presented in the next section.

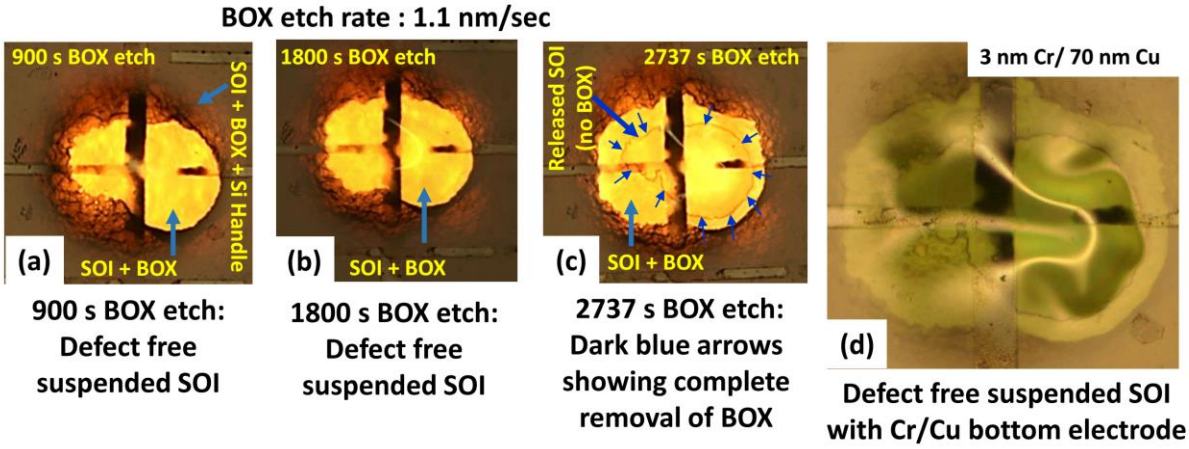


Figure 5.13. Series of optical images (illuminated from back) showing the evolution of BOX etching after (a) 900 s, (b) 1800s, (c) 2737 s and (d) after Cr/Cu deposition. The etch rate is ~1.1 nm/s. The image in (c) shows that BOX is completely removed from the middle (indicated by dark blue arrows).

5.5 Electrical characterization

I-V measurements were performed on the completed devices (8 devices on 1 chip). The mechanical and structural yield of this chip is 88%, i.e. 7 out of 8 SOI devices are defect free. The electrical yield of the suspended devices is 50%, i.e. 4 out of 8 devices show diode behavior in the dark and photo-response under illumination. Results for the best device are discussed in this section.

The I-V characteristic of the suspended p-i-n SOI device are shown in Figure 5.14. The device shows diode behavior under dark conditions and enhanced photo-response. The device acts like a photo-detector as it has an enhanced response under illumination in the reverse bias condition (Figure 5.14 inset). The device does not deliver any power to an external load like photovoltaic devices. The power in a photovoltaic device can be extracted if a 'negative' current (i.e. short circuit current at 0 V) is present in the 3rd quadrant of the I-V curve under illumination.

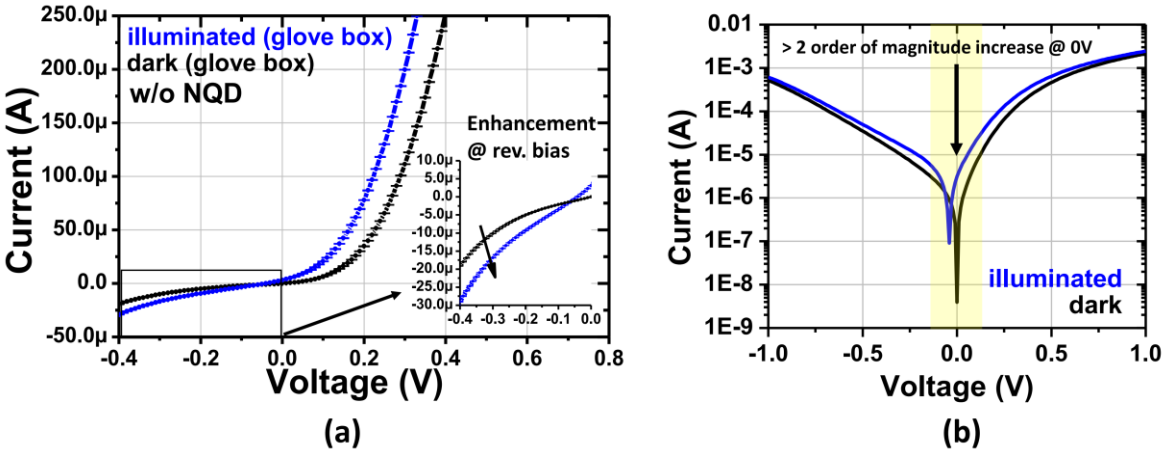


Figure 5.14. Electrical measurements of the suspended SOI device after removal of BOX and deposition of a bottom Cr/Cu electrode as shown in Figure 5.13. (a) I-V characteristic of the device in dark (black curve) and under 1 Sun AM1.5G illumination (blue curve). The inset shows an enhanced photo-response in the reverse bias condition. (b) I-V characteristic of the device plotted in a semi-log graph. The blue curve (under illumination) shows >2 order of magnitude enhancement at 0 V compared to black curve (dark).

However, >2 orders of magnitude enhancement at 0 V is observed from the device as shown in the semi-log plot of Figure 5.14 (b). This is similar to self-powered photo-detectors [125-127] which can work without an external power source. A built-in electric field at any of the interfaces provides the driving force for the enhanced photo-response. Detailed study is needed to understand the role of the different interfaces in driving efficient separation of photo-generated carriers at 0 V. The interface between the n-doped poly Si and p-SOI should drive the separation of carriers. However, there are several interfaces (Al and n-doped poly Si, n-doped poly Si and intrinsic poly Si, intrinsic poly Si and p-SOI, p-SOI and Cr/Cu) that can play important role.

The ideality factor (n) [128] provides information about the behavior of the fabricated diodes compared to a diode governed by the ideal diode equation . An ideal p-n junction diode is dominated by the recombination of minority carriers and has an ideality factor of 1.0 as per Sah-

Noyce-Shockley [129] theory. However, the diode ideality factor is higher than 1.0 for most diodes, but ≤ 2 for a good quality diode. High ideality factors can be explained by additional p-n junctions present at the interfaces [125]. Different heterojunctions at can act as additional rectifying junction and increase the overall ideality factor.

The suspended SOI photo-detectors show significant deviation from ideal diode behavior with an overall high ideality factors. In fact, the ideality factors vary over different regions (Figure 5.15). Here, regions dominated by leakage current (V< 0.3 V) [130] and series resistance (V > 0.3 V) [131] are observed. Poor passivation on the sidewalls and front surface cause low shunt resistance (R_{sh}) which results in increased leakage current in the reverse bias. The ideality factor is > 2.0 in this region. Additionally, the device has high series resistance (R_s) due to poor interface quality. The ideality factor is > 9.0 in the region where the I-V behavior is dominated by R_s. Processing steps needs to be optimized to reduce leakage current and R_s.

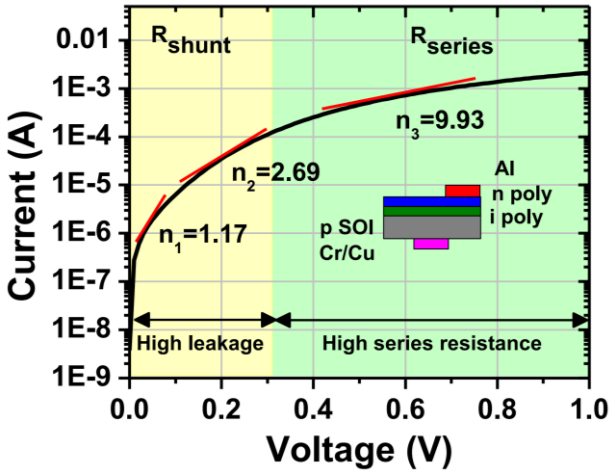


Figure 5.15. I-V graph showing ideality factors for one of the fabricated SOI devices. The device shows significant deviation from high performing diodes (n<2). The low voltage region (V< 0.3 V) is dominated by high leakage current. The high voltage region (V> 0.3 V) is dominated by high series resistance.

The effect of the environment on the I-V characteristic of the device was also studied. As the suspended SOI devices are ultrathin changes in the environment can introduce instability in the device performance. The dark I-V characteristic of the device is compared in ambient and under inert conditions (Figure 5.16 (a)). The device shows different behavior inside the glove box as compared to under ambient conditions.

A different device was measured over 2 days under inert conditions to determine the device stability inside a controlled atmosphere (Figure 5.16 (b)). The device shows stable and repeatable I-V behavior both in the dark and under illumination.

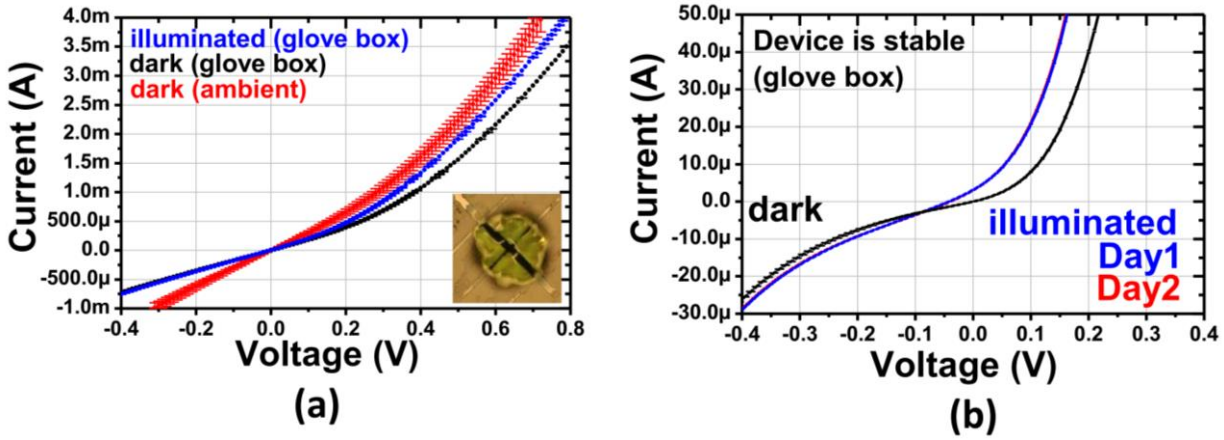


Figure 5.16. Effect of the environment on the stability and repeatability of the suspended SOI device characteristics. (a) I-V graph of the device measured in the dark in ambient conditions (red) and in the glove box (black) as well as under illumination in the glove box blue). Inset: optical image of the measured device. (b) I-V graph of the device measured for two days in the glove box. Black curve shows the dark behavior. Blue (day1) and red (day2) curves show device behavior under illumination. The red curve is hard to see as it falls under the blue curve.

5.6 Conclusions

A detailed process flow was presented to fabricate suspended ultrathin (300 nm) SOI devices. Stress induced defects in the suspended SOI device were identified. The fabrication process was modified and optimized systematically to improve the yield of defect free suspended

SOI devices. A structural process yield of 88% (7 out of 8 devices) was achieved after all the optimization. The electrical response device yield was 50% (4 out of 8 devices). The devices act as self-powered photo-detectors. The devices show > 2 orders of magnitude enhancement in photo-response at 0 V. Effective separation of charge occurs due to a built-in electric field at the interface which drives the device without the need for any external power sources. The device showed improved photo-response under reverse bias. Overall, the device behavior is dominated by high leakage current and high series resistance. Further optimization is needed to improve the electrical quality of the devices. However, the developed process flow enables the integration NQDs into the final structure. Thus, the process flow provides an efficient way to facilitate the goal of quantifying ET-generated charges within the framework of an ultrathin Si SC.

CHAPTER 6

OUTLOOK AND FUTURE DIRECTIONS

Our study showed that for bulk Si SCs, the absorption due to Si dominates and thus prevents quantification of ET-generated charges after NQD sensitization. Additionally, we found that the observed PV enhancement originates from optical effects (i.e. anti-reflection). We proposed a PV structure based on ultrathin (~300 nm) Si as way to reduce the effect from Si absorption. A process flow for fabricating these ultrathin devices was developed and tested in the dark and under 1 Sun AM 1.5G illumination. The devices showed photo-detector type behavior. We observed > 2 orders of magnitude increase in photocurrent at 0V. Additionally, an enhancement in detection under reverse bias was observed. More experiments need to be conducted to understand these results. However, the ultrathin SCs were designed so that NQDs can be incorporated to the device. We expect to observe ET-generated charges after NQD deposition due to a significant reduction in Si absorption. Based on the current outcomes, we propose the following directions for future work.

(1) Controlled shallow/ultra-shallow doping in ultrathin Si: Thin layers of highly doped poly Si were used to form n^+ - i^- structures. Highly doped Si as a top layer is not desirable for PV applications because high energy photons are absorbed at the surface. High doping levels in poly Si can drastically reduce photo-generated charge collection. One way around this is to controlled diffusion doping using spin-on-dopant sources. Spin-on-dopant is an easy and cost effective way to make shallow (~ 100 nm) junctions. Rapid thermal annealing can be used to control the junction depth. Another method to over this issue is to deposit a doped epitaxial Si layer. In both

cases, secondary ion mass spectroscopy can be used to determine the junction depth. Thus, by controlling the doping depth in the poly Si layer, a working SC can be developed.

(2) Si surface passivation and extensive electrical characterization: Ultrathin Si devices are sensitive to surface conditions. Therefore, Si surface passivation is extremely important. However, the distance dependence of the ET mechanisms need to be considered when passivating the surface. For instance, surface passivation by a thick oxide will drastically reduce ET efficiency. On the other hand, self-assembled monolayers can effectively passivate Si surfaces while retaining high ET rate. The process flow needs to be optimized to integrate self-assembled monolayer passivation.

(3) NQD deposition techniques on ultrathin Si SCs: This dissertation focused on the fabrication of ultrathin Si SCs. In order to determine the effect of ET on the ultrathin SCs, the next step is to incorporate NQDs into the structures. The controlled deposition of NQDs is necessary, such as through the deposition band gap graded layers. One simple approach for incorporating NQDs can occur during near the beginning of the fabrication process. Here, NQDs will be deposited on top of the devices by spin coating before etching the backside of the Si and subsequent metal deposition. To protect the NQDs during the later processing step, the NQDs needs to be passivated with metals oxides or other materials to retain the optical integrity of NQDs. A compatible method needs to be developed to protect the NQDs and enable device fabrication steps. Additionally, the optical integrity of the NQDs upon different passivation methods (i.e., atomic layer deposition, PECVD, sputtering etc.) needs to be studied. Once the NQDs are incorporated, the devices can be characterized to monitor changes in electrical charges imparted by NQD deposition.

(4) Nano-structures on ultrathin Si solar cells: One technique to increase light absorption in SCs is to nano-structure the surface. Additionally, nanostructures, such as nanopillars or nanowires, increase the surface area. This enables higher NQD loading densities. Another direction to explore is the fabrication of nanostructured (nanowires, nanopillars, etc) thin/ultrathin Si SCs that are compatible with the fabrication process and can be sensitized with NQDs.

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Natis Shafiq was born in Dhaka, Bangladesh. He received his B.S. in Mechanical Engineering from Bangladesh University of Engineering and Technology (BUET) in 2007. He received his M.S. in Mechanical and Aerospace Engineering from Oklahoma State University in 2011. He gained extensive experience in surface enhanced Raman spectroscopy during his M.S. under the supervision of Dr. A. K. Kalkan. He started his Ph.D. in Materials Science and Engineering under the supervision of Dr. Yves Chabal in August 2011. His research has focused on photovoltaic performance enhancement of Si solar cells using proximal nanocrystal quantum dots. He has extensively worked in semiconductor fabrication and process development during his Ph.D. His research was to propose a design approach based on ultrathin (300 nm) Si for energy transfer from nanocrystal quantum dots to Si.

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List of Publications

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