LOW NOISE INTEGRATED CIRCUITS AND SYSTEMS USING NANO-SCALE MOSFETS AND INTELLIGENT POST-FABRICATION SELECTION

by

Venkata Pavan Kumar Yelleswarapu

APPROVED BY SUPERVISORY COMMITTEE:

_____

Dr. Kenneth K. O, Chair

_____

Dr. Rashaunda M. Henderson

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Dr. Dongsheng Brian Ma

_____

Dr. Yiorgos Makris

This dissertation is dedicated to my family for their endless support, encouragement and love.

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VENKATA PAVAN KUMAR YELLESWARAPU, MSEE

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LOW NOISE INTEGRATED CIRCUITS AND SYSTEMS USING NANO-SCALE MOSFETS AND INTELLIGENT POST-FABRICATION SELECTION

Venkata Pavan Kumar Yelleswarapu
The University of Texas at Dallas, 2021

Supervising Professor: Kenneth K. O

Recent advances in integrated radio design have enabled many applications such as wearable healthcare, 5G communication, and beyond 5G or 6G applications for ultra-high data rate communications, high-resolution imaging, sensing, and spectroscopy. All these applications require low noise radio transceivers for achieving high performance. For example, applications requiring high data rate and higher order modulation schemes need to achieve high signal to noise ratio (SNR) and therefore a low noise figure to maintain a low bit-error rate (BER). In addition, noise phenomena like jitter and phase noise can impact the critical parameters like maximum achievable data rate and energy efficiency. This research aims to improve the noise performance of integrated circuits and systems through intelligent post-fabrication selection of an array of nano-scale transistors sized near the minimum in CMOS processes.

A phase noise reduction technique in LC Voltage Controlled Oscillators (VCO's) is demonstrated by post-fabrication selection of a subset of an array of near minimum-size cross-coupled transistor pairs with reduced low frequency noise and thermal noise. The technique reduces the phase noise by taking advantage of the fact that when transistor dimensions are reduced, the low frequency

noise and thermal noise vary significantly. Applying an intelligent post-fabrication selection process using a genetic algorithm, the lowest phase noise of -122 dBc/Hz, -127 dBc/Hz, -137.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively from a 3.8-GHz carrier has been measured. The VCO prototype was fabricated in a 65-nm CMOS process and dissipates 7 mW of DC power. The maximum figure of merit (FoM) including phase noise, carrier frequency and power consumption is 191 dBc/Hz and the figure of merit including the VCO core area, FoM_A is 207 dBc/Hz.

A technique is demonstrated to reduce both the in-band and out-of-band phase noise of a 4-GHz Integer-N PLL by employing an array of individually selectable cross-coupled pairs formed using near minimum-size transistors in an LC VCO and intelligent post-fabrication selection. By reducing both the in-band and out-of-band phase noise, the overall integrated phase jitter in a frequency synthesizer can be minimized. Applying an intelligent post-fabrication selection process, the lowest phase noise of -72 dBc/Hz at 30-kHz offset, -106 dBc/Hz at 300-kHz offset, -121.8 dBc/Hz at 1-MHz offset, and -132.5 dBc/Hz at 3-MHz offset, respectively from a 4.01-GHz locked carrier has been measured. The integrated rms jitter from 100-kHz to 100-MHz offsets is 440 fs.

A mixer-first downconverter employing an array of passive mixers formed using near minimum-size transistors and intelligent post-fabrication selection achieves a double sideband noise figure of 4.2 dB at RF of 6 GHz, which is the lowest at 6 GHz for CMOS mixer-first downconverters. The downconverter is fabricated in 65-nm CMOS and demonstrates out-of-band IIP3 and IIP2 of 25 dBm and 65 dBm, respectively at 80-MHz IF, while dissipating 11.5 mW. Post-fabrication

selection is performed by a genetic algorithm which takes ~17 generations to converge to the combinations exhibiting the lowest noise.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Recent advances in integrated radio design have enabled many applications like wearable healthcare, 5G communication, and beyond 5G or 6G applications for ultra-high data rate communications, high-resolution imaging and sensing, spectroscopy, and others. In addition, a new class of ICs and systems are being developed which have many promising and new features realized through on-die machine learning techniques. Some of these features include self-optimization to maintain high performance; self-healing to increase longevity; self-identification and verification for improved trust and security. These high-performance autonomous systems can be widely used in a wide variety of applications like mission critical DoD communication and navigation systems, communication systems, autonomous vehicles, intelligent highways, and others.

For all the mentioned applications, implementation of transceiver (transmitter & receiver) relies on efficient design of the RF, baseband, and mixed-signal integrated circuits (ICs) achieving multiple design targets. Especially, realizing low noise radio systems is a critical need and challenge. For example, applications requiring high data rate and higher order modulation schemes need to achieve a high signal to noise ratio (SNR) and thereby a low noise figure to maintain a low bit-error rate (BER). In addition, jitter and phase noise can impact maximum achievable data rate and energy efficiency. Due to all these reasons, the transceivers and the integrated circuit components of these radio transceivers such as low noise amplifiers, mixers, frequency

synthesizers, etc., must be designed for reduced noise performance. Depending on the type of applications, sometimes they must also be designed for ultra-low noise performance.

1.2 Radio Receiver

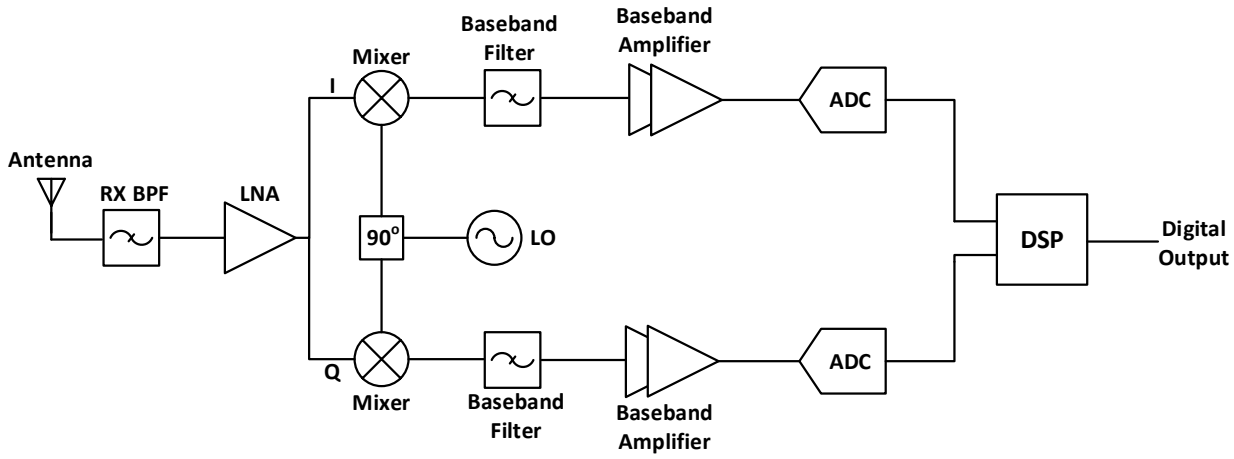


Figure 1.1. Block diagram of a radio receiver.

Figure 1.1 shows a block diagram of a typical IQ receiver for a single communication band [1]. The antenna picks up the input RF signal. The receiver (RX) band-pass filter (BPF) serves as a tuned RF stage to attenuate the unwanted out-of-band signals. It may also serve to prevent strong out-of-band signals from saturating the receiver. The signal is then fed into a IQ mixer for demodulation, where it is mixed with a sine wave from a local oscillator (LO), which needs to be stable and spectrally clean.

Mixers use non-linear components such as transistors to produce both the sum and difference of the frequencies of input and LO signals. In the receiver configuration, the difference of input frequencies, called the baseband frequency is the signal of interest since we need to eventually down-convert the RF signal to an audio frequency range. A baseband filter, typically a

low-pass filter rejects the unwanted harmonics and passes only the baseband signal. The signal is then finally amplified by baseband amplifiers before passing to the ADC and DSP for processing the signals in digital domain.

1.3 Sensitivity and Dynamic Range

Sensitivity of a radio receiver is a key parameter that determines the performance of any radio communication system. It determines the minimum input signal level that a receiver can successfully detect in the presence of noise [1]. If the noise is excessive, the detection becomes difficult and the wanted signal or data become corrupted. Whether it is for the reception of radio signals carrying audio for which the quality of audio deteriorates, or for a data signal where the bit error rate (BER) increases and the throughput falls, the signal to noise ratio is critical in any receiver design. Sensitivity is given by:

$$P_{sen} = -174 + NF + 10*\log(B) + SNR_{min}\,, \tag{1.1}$$

where P_{sen} is the sensitivity in dBm, NF is noise figure in dB, B is signal bandwidth in dB/Hz, and SNR_{min} (dB) is the minimum signal to noise ratio required by the receiver at its output.

Noise figure determines the amount of noise an element adds to the overall system. The amount of noise may be from an LNA, mixer, or a complete receiver. Often, the noise figure is used as a metric to define the performance of a receiver and can be used instead of the signal to noise ratio. Therefore, having a low noise figure for a receiver is critical in any application.

Dynamic Range of a receiver is defined as the maximum input signal level that a receiver can tolerate divided by the minimum input signal level that it can detect [1]. The minimum input level detected being the sensitivity. It is limited by the compression of the signal at the upper end and noise at the lower end. The dynamic range is essentially the range of signal levels over which it can properly process the input signal. Therefore, having a high linear dynamic range for a receiver is highly desirable along with low noise figure.

1.4 Noise in MOSFETs

There are mainly six sources of noise in MOSFET transistors, they are:

1) Thermal noise in the channel.

2) Flicker Noise.

3) Gate Induced Thermal Noise.

4) Noise due to the substrate resistance.

5) Noise due to resistive poly silicon gate.

6) Shot Noise.

Of the above six noise sources, the first two are dominant and important in most of the applications. We first review some of these noise sources in brief before introducing the phenomenon of low frequency noise and how it is different from the flicker noise in the next section.

Channel Thermal Noise

Thermal noise is generated by thermally induced motion of electrons in the conductive regions of a MOSFET. For MOSFETs operating in saturation region, the channel noise can be modeled by a current source connected between the drain and source terminals and expressed as,

$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{do} \,, \tag{1.2}$$

where γ is 2/3 for a long channel device and 2 or even higher for short channel devices, and g_{do} is zero bias drain conductance. Thermal noise of the channel when referred to input, can be represented by a voltage source in series with the gate. The voltage power spectral density is

$$\frac{\overline{v_{n,d}^2}}{\Delta f} = \frac{8}{3}\frac{kTg_{do}}{g_m^2} \,, \tag{1.3}$$

where g_m is the transconductance of transistor in saturation.

Flicker Noise

Flicker noise is caused by the gate dielectric traps due to defects that randomly capture and release carriers. This noise is associated with DC current flow in both conductive and depletion regions. It is modelled by a current source across the drain and source and expressed as,

$$\frac{\overline{i_{nf}^2}}{\Delta f} = \frac{K_f}{f}\frac{g_m^2}{C_{ox}WL} \,, \tag{1.4}$$

where K_f is a device specific constant, f is the frequency, C_{ox} is the oxide capacitance, and W and L are the effective width and length of MOS transistor. When referred to input, the noise is represented by a voltage source between the gate and source. The voltage spectral density is

$$\frac{\overline{v_{nf}^2}}{\Delta f} = \frac{K_f}{f}\frac{1}{C_{ox}WL} \ , \tag{1.5}$$

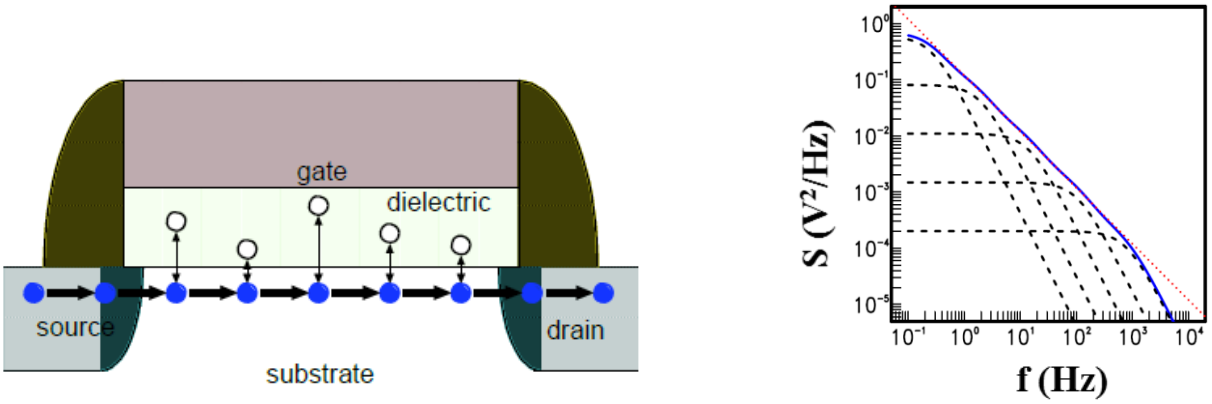
Flicker noise reduces with increasing frequency. The frequency at which flicker noise is equal to thermal noise is called the corner frequency of flicker noise.

In addition, gate induced thermal noise is caused due to fluctuations in the channel charge in the inversion region, which thereby will induce a noisy current in the gate due to capacitive coupling. Shot noise is generated due to the leakage current of the reverse biased diodes in the drain to source junction as well as that through the gate dielectric layer. Many techniques and methods have been developed until now to mitigate the effects of thermal noise in CMOS circuits. But very few techniques have been introduced to counter the effects of flicker noise and low frequency noise in CMOS circuits, which is a major focus of this thesis.

1.5 Low Frequency Noise

A widely accepted theory is that traps in a gate dielectric layer near the dielectric/Si interface are largely responsible for 1/f noise or flicker noise [85]. The McWhorter model [2] attributes the trapping and de-trapping process of the channel electrons or holes of MOSFETs as the generation mechanism for flicker noise, as illustrated in Figure 1.2(a). The behavior of each

single trap is described as Random Telegraph Signal (RTS). The power spectral density of RTS which is termed as Lorentzian spectrum and shown in Figure 1.2(b).



(a) (b)

Figure 1.2. (a) Trapping-detrapping process in MOSFETs [3], (b) Distribution of Lorentizians leading to 1/f noise [3].

The properties of each trap determine the corner frequency and if these traps do not interact with each other, the power spectral density (PSD) of each trap can be added [85]. McWhorter [2] showed that all the traps with an equal RTS amplitude will generate a 1/f noise spectrum with corner frequencies of their PSDs exponentially distributed. However, in nano-scale transistors, the number of the traps decreases to a few or maybe even less than one per transistor. Such devices do not exhibit the 1/f spectrum as a large number of traps are required to generate the 1/f dependence [85]. Hence, it is much more accurate to refer this as low frequency noise rather than 1/f noise or flicker noise.

1.6 Low Frequency Noise Variability

Scaling of the MOSFETs in advanced nano-scale CMOS technologies comes at a cost of increased process variation and noise variability. In this perspective, the low frequency noise (LFN) is considered as one of the key limiting factors in integrated circuit design. The LFN, which scales as reciprocal to the device area, is becoming a major concern not only for RF, analog and mixed-signal circuits, but also for digital circuits operation. In particular, it can limit the performance of a wide variety of circuits including VCOs, PLLs, Mixers, Operational Amplifiers, DRAM cells, SRAM cells, and inverters.

The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling. One missing dopant or having an additional defect can have dramatic impact on device characteristics including threshold voltage, current and noise [29]. The defect density related to low frequency noise in nano-scale CMOS is ~$1x10^9$ cm^{-2} (kTN_{ot}/α_t of Eq. (1) in [4]), which translates to on the average, one trap in ~300 x 300 nm^2 or ~90,000 nm^2. In modern nano-scale MOSFETs, the number of traps is not a fixed process constant, but rather a random variable with increasing uncertainty with a shrinking device size [85]. This leads to a large variation of low frequency noise for otherwise similar devices of near minimum sizes, and a large device-to-device variation in MOSFET low frequency noise is reported in [4]-[10].

Considering both the carrier number fluctuation and correlated mobility fluctuation, a unified model for the 1/f drain current noise spectral density is [9]-[12]

$$S_{Id} = \frac{q^2 kT}{WLC_{oxf}^2}\left(g_m + \alpha\mu_{eff}C_{ox}I_d\right)^2 \lambda N_t \,, \tag{1.6}$$

where α is the Coulomb scattering coefficient, N_t stands the area and energy density of oxide traps,

and λ is the tunneling attenuation distance. $\lambda = kT/\Delta E_a$, where ΔE_a is the amplitude of the activation energy dissipation. Process induced variations in W, L, C_{ox}, μ_{eff}, I_d, and g_m covered in PDK for advanced technologies are relatively too small to explain the large standard deviations in the measurement results of low frequency noise variations. Instead, they come directly from the large fluctuations in the effective area trap density $N_{teff} = \lambda N_t$ [9]. Figure 1.3 shows the measured low frequency noise of 32 NMOS transistors of width and length of 150 nm and 60 nm, respectively or a gate area of 9000 nm^2.

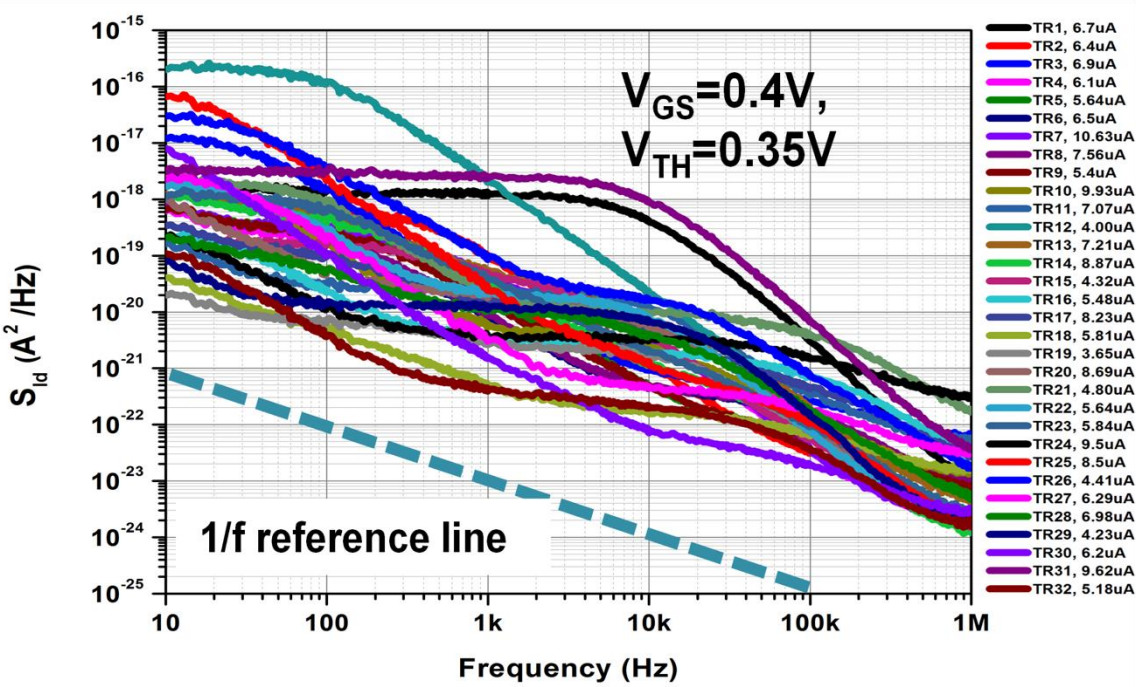


Figure 1.3. Measured low frequency noise variability of 32 NMOS transistors with dimensions near the minimum for a 65-nm CMOS process.

The transistors are biased at V_{GS}=0.4V, V_{DS}= 0.6V and V_{TH}=~0.35V. From the plot, it can be observed that the drain current noise spectral density varies by 4 orders of magnitude at 10-kHz, and by 3 orders of magnitude at 1-MHz. This large variation is attributed to the fact that

the number of traps in the transistors is not the same. The average low frequency noise in the PDK is dominated by a few devices with the highest noise. This implies that some transistors can have significantly lower noise than the mean noise predicted by the PDK model.

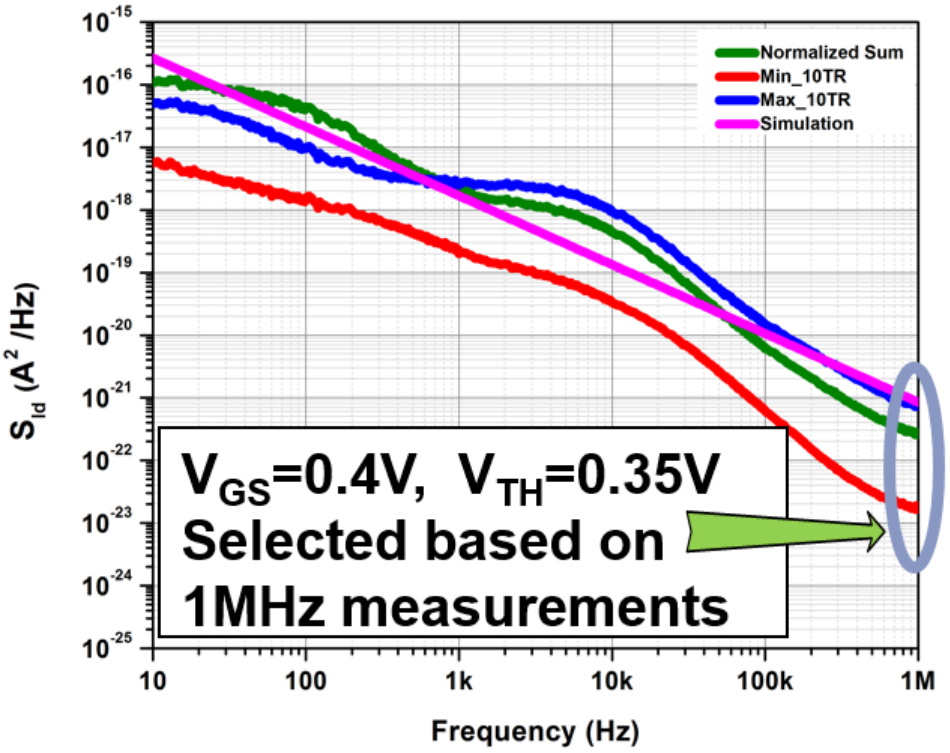


Figure 1.4. Current noise power spectral density of combinations formed by randomly selecting 10 transistors out of 32.

Figure 1.4 shows the maximum and minimum current noise spectral densities of a set of 10 transistors randomly selected from the array of 32 transistors. The minimum current noise spectral density is an order of magnitude lower than the normalized sum predicted by the PDK. This indicates that, if only the transistors with low noise can be used by post-fabrication selection, then it should be possible to significantly reduce the low frequency noise impact. Using minimum size transistors to reduce low frequency noise is opposite to the conventional approach for reducing

the impact of low frequency noise by using larger transistors, which relies on averaging to the value determined by the PDK model. Because of this, the approach using the post-fabrication selection [13] should result in circuits with significantly reduced noise.

1.7 Thermal Noise Variability

The channel thermal noise of a MOS transistor operating in the saturation region can be modelled by a current source [1]. The noise current spectral density is

$$\overline{i_{n,d}^2} = 4kT\gamma g_{d0} \ , \tag{1.7}$$

where g_{d0} is the zero-bias drain conductance of the device, and γ is a bias-dependent coefficient of thermal noise, which can be much greater than one for short channel MOS devices. The relation between g_{d0} and the transconductance, g_m can be given by the factor α [69], as shown below

$$\alpha \triangleq \frac{g_m}{g_{d0}} \ , \tag{1.8}$$

For short channel MOS devices, α can be much less than one. It is well known that g_m in terms of bias voltages (V_{GS}, V_{DS}), threshold voltage (V_{TH}), width (W), length (L), mobility (μ_n), and oxide capacitance (C_{ox}) of a long channel MOS transistor can be given below

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})(1 + \lambda_n V_{DS}). \tag{1.9}$$

After substituting the equations for α and g_m in (1.8), noise current spectral density can be re-written as below,

$$\overline{i_{n,d}^2} = \frac{4kT\gamma}{\alpha} . [\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})(1 + \lambda_n V_{DS})] \quad (1.10)$$

It can be observed from (1.10) that the thermal noise current spectral density of a MOS transistor mainly depends on its mobility, physical dimensions, bias voltages, threshold voltage, oxide capacitance and bias dependent coefficients α, γ, λ. For a given V_{GS} and V_{DS}, all other parameters in (1.10) such as mobility, effective channel length, threshold voltage and gate dielectric layer thickness can significantly vary [31]-[33], which leads to a significant variation of the thermal noise. In addition, the correlation of low frequency noise to thermal noise due to a correlated increased mobility due to lower trap density [61] can also be a factor. This implies that if only the transistors with lower thermal noise can be used by post-fabrication selection, then it should also be possible to reduce the thermal noise impact.

1.8 Scope and Organization of the Dissertation

This research in particular aims to improve the noise performance of integrated circuits and systems by applying intelligent post-fabrication selection to an array of nano-scale transistors sized near the minimum in CMOS processes. The rest of the thesis is organized as follows.

Chapter 2 demonstrates a phase noise reduction technique for LC Voltage Controlled Oscillators. More specifically, the design and measurement results of a low phase noise 3.8-GHz LC Voltage Controlled Oscillator (VCO) in 65-nm CMOS using an array of cross-coupled nano-scale MOSFETs and intelligent post-fabrication selection are discussed. Chapter 3 demonstrates a jitter reduction technique in frequency synthesizers. The design and measurement results of a

4.01-GHz phase locked loop (PLL) in 65-nm CMOS employing an array of cross-coupled nano-scale MOSFETs in the VCO and intelligent post-fabrication selection are presented. The jitter reduction technique seeks to optimally reduce both the in-band phase noise and out-of-band phase noise of the 4.01-GHz PLL. Finally, chapter 4 demonstrates a noise figure reduction technique in Mixer-First Downconverters by discussing the design and measurement results of a 6-GHz Mixer-First Downconverter in 65-nm CMOS which achieves low noise figure by using an array of passive mixers formed with nano-scale MOSFETs and intelligent post-fabrication selection.

CHAPTER 2

PHASE NOISE REDUCTION IN LC VCO's USING AN ARRAY OF CROSS-COUPLED NANO-SCALE MOSFETS and INTELLIGENT POST-FABRICATION SELECTION

2.1 Introduction

Oscillators are key blocks used in both the transmit and receive paths of integrated transceivers of high-performance wireless communication systems. The spectral purity of oscillators highly affects the performance of a transceiver. The phase noise of oscillator can mix with a blocker and thereby appear on top of the desired signal, thus degrading the sensitivity of a receiver [1]. Adjacent channel rejection and jitter of demodulated signals which are dependent on the VCO phase noise, are key factors determining the order of modulation that can be deployed for a communication system to increase the data rate and energy efficiency. In the transmit path, the phase noise of the oscillator is amplified and can desensitize a nearby receiver [53].

An oscillator is a feedback system satisfying the Barkhausen criteria [54]. It generates a periodic output. Figure 2.1 shows a feedback system. The Barkhausen criteria for the oscillation condition for the system is,

$$|H(s = j\omega)| = 1, \tag{2.1}$$

$$\angle H(s = j\omega) = 180^{\circ}. \tag{2.2}$$

A feedback system for an oscillator usually consists of an amplifier and a resonant circuit. For a negative feedback system shown in Figure 2.1, the phase delay through the amplifier and the resonant circuit should be odd integer multiples of 180^0.

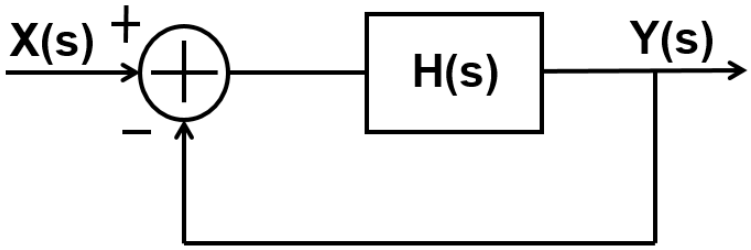
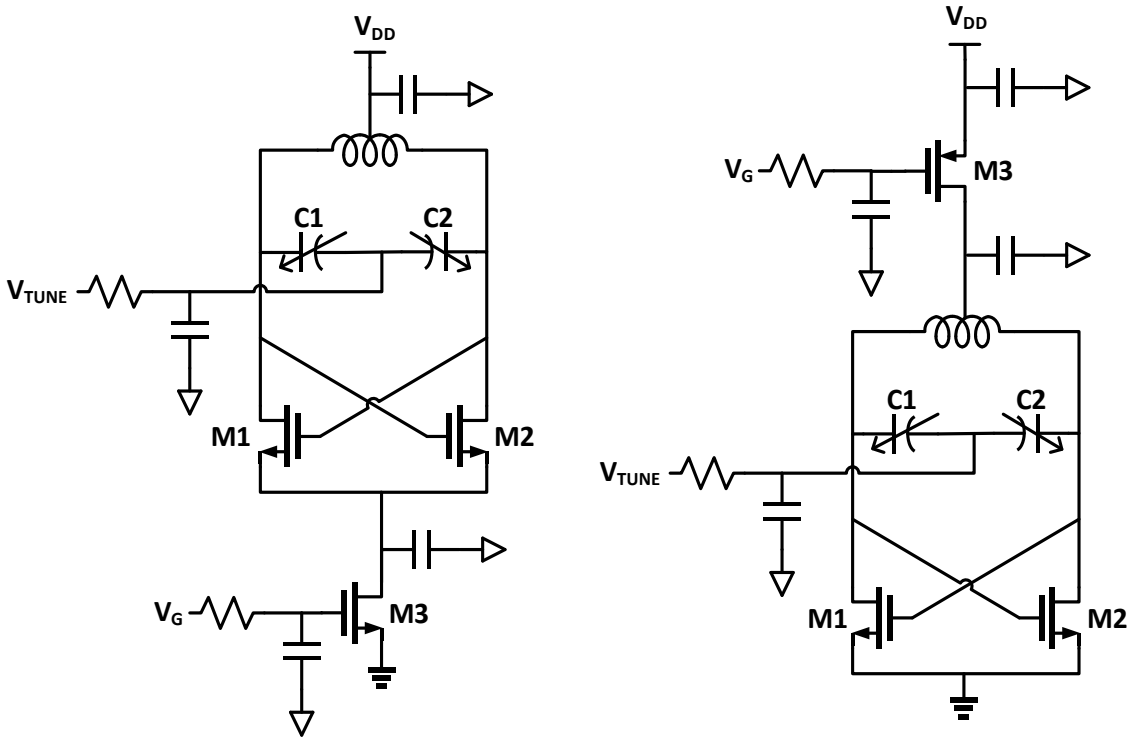


Figure 2.1. Negative feedback system.

2.2 Review of Low Frequency Noise Reduction Techniques in VCO's



(a) (b)

Figure 2.2. NMOS Voltage Controlled Oscillator with (a) an NMOS tail-current source and (b) a PMOS top-current source.

Figures 2.2(a) and (b) show topologies of a conventional NMOS VCO with a current source both in the bottom and the top of the cross-coupled pair formed by M1 and M2 which generates the negative resistance for cancelling the losses in the tank. The varactor pair formed by C1 and

C2 is used to tune the oscillation frequency with V_{TUNE}. One of the key mechanisms for generation of oscillator phase noise is up-conversion of white and low frequency noise of the cross-coupling transistors. Low frequency noise from the current source transistor M3 can be minimized by using a wide and long channel length transistor. But the same method cannot be applied to the core cross-coupling transistors since increasing their size increases the associated parasitics and limits the oscillation frequency and tuning range. According to Leeson's model [14], phase noise is

$$L(\Delta\omega) = 10\log\left[\frac{2KTF}{P_{\text{sig}}}\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right\}\left\{1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right\}\right], \tag{2.3}$$

where F is an empirical factor which considers the device excess noise, K is the Boltzmann's constant, T is temperature in degree Kelvin, ω_0 is the oscillation frequency, $\Delta\omega$ is the offset frequency, $\Delta\omega_{1/f^3}$ is the up-converted low frequency noise corner and Q is the quality factor of the tank.

Low frequency noise of the cross-coupling transistors is up-converted to the close-in phase noise in VCOs mainly via four mechanisms:

1) Noise folding phenomenon i.e., the low-frequency noise can be mixed up to frequencies close to the carrier due to the pumping/mixing action of the oscillator.

2) Amplitude to phase noise (AM-PM) conversion due to the non-linearity of varactors in a VCO tank [15]-[17].

3) AM-PM conversion due to the non-linear parasitic capacitances of the cross-coupling transistors in a VCO [19].

4) Modulation of the harmonic content of the output voltage waveform in a VCO, i.e., "Groszkowski effect" [20].

Among the above four phenomena, the first phenomenon is always present and mostly unavoidable. Of the remaining three, the main contributor is the Groszkowski effect since discrete tuning with a switched capacitor bank or switched LC tank can suppress the AM-PM effect by reducing the VCO gain, K_{vco} [34]. Circuit techniques for reduction of low frequency noise impact in oscillators are briefly reviewed in order to make a clear distinction between these techniques and the proposed post-fabrication selection technique applied to a VCO to lower its phase noise.

A. Phase-Locked Loop (PLL)

In a typical PLL, both the phase and the frequency of a VCO is locked to the phase and frequency of an input reference signal through a feedback loop. If the input reference spectrum is clean or low noise, the PLL suppresses the phase noise of the VCO by an amount determined by the loop gain. For this noise mechanism, the PLL loop bandwidth must be larger than the offset frequency at which the phase noise of the VCO should be suppressed. Although this is a commonly used technique, this has limitations. Within the loop bandwidth, the noise contributions of the blocks like phase frequency detector (PFD), charge pump, and the frequency divider are not attenuated by the loop, which means the noise of these blocks must be reduced. In addition to this, for applications requiring a small loop bandwidth, low frequency noise can be a significant problem [21].

B. Resistors in series with drains of cross-coupling transistors

Low frequency noise up-conversion in voltage-biased oscillators can be suppressed by

inserting resistances in series to the drain of the cross-coupling core MOSFETs [22]. This technique is simple and effective in suppressing the $1/f^3$ phase noise. But the series resistors degrade the quality factor of the tank, and also add thermal noise. As a result, though the $1/f^3$ phase noise are suppressed, the phase noise in the $1/f^2$ or thermal noise limited region is not reduced. In addition to this, careful sizing of the components is needed in order to avoid degradation of the start-up gain margin.

C. 2nd Harmonic Filtering

To minimize the up-conversion of low frequency noise from the tail current source, all even harmonics must be suppressed, with the 2nd harmonic ($2f_o$) being the dominant. The noise filtering of $2f_o$ at the tail current source is implemented by a second-harmonic short circuit formed by an LC resonant filter [23].

This technique can also be used to effectively suppress the up-conversion of the low frequency noise of cross-coupling transistors because the low frequency noise from the cross-coupled differential pair modulates the second harmonic voltage waveform (i.e., Groszkowski effect) at the common source node, which in turn induces noisy current at the source of each cross-coupled transistor. This current is then mixed down to the fundamental frequency by the switching action of the cross-coupled pair, thereby inducing the close-in phase noise [24]. The drawback of this technique is mainly the additional area penalty caused by the inductor in the resonant filter.

D. Switched Biasing

Switched biasing is proposed as a technique for reducing the intrinsic low frequency noise of the device itself [25]. This technique reduces the low frequency noise by exploiting a physical

effect: cycling MOS transistors between strong inversion and accumulation reduces its low frequency noise observed in strong inversion. Instead of applying a constant gate-source bias to a MOS transistor, the transistor is periodically switched between two states: 1) “active state” in strong inversion region, in which it contributes to the functional operation of a circuit e.g., delivering a bias current; and 2) “inactive state” in accumulation region. In the accumulation region, the MOS transistor is not operational.

The main difficulty arises in ensuring that the regions of operation for the transistors include the accumulation region. Use of this technique in the current source requires an additional signal source with a sufficient voltage range to switch the current source transistors between inversion and accumulation. This technique has been demonstrated only until few MHz of switching frequencies. In addition, the spurs resulting from the source for switched biasing must be properly managed.

E. Reduce up-conversion by maintaining symmetry

Hajimiri proposed a theory to quantify the effects of up-conversion of low frequency noise in oscillators [26]. The oscillator is modeled as a linear time-variant system, and an impulse sensitivity function is used to characterizes the sensitivity to up-conversion. Based on this theory, symmetry of oscillator waveforms helps to reduce the up-conversion [27]. However, the achievable symmetry is limited in cases where complementary devices are used.

In summary, numerous techniques have been proposed for reducing the effect of low frequency noise in oscillators. Each has benefits and drawbacks. We will now describe an alternate approach of reducing noise impact in oscillators by taking advantage of the phenomenon of noise

variability discussed in Chapter 1. Scaling of the MOSFETs in advanced CMOS technologies accompanies increased process variation and noise variability. The number of intended dopants and un-intended defects in a minimum sized device is reduced with technology scaling [29]. One missing dopant or having an additional defect can have dramatic impact on device characteristics including threshold voltage, current and low frequency noise [4]-[10]. In addition, the thermal noise among the nano-scale transistors of similar size can also vary considerably due to variations of the DC parameters such as mobility, effective channel length, threshold voltage and gate dielectric layer thickness [31]-[33].

This work presents a phase noise reduction technique in LC VCO's by using an array of individually selectable cross-coupled pairs of transistors [29] with dimensions near the minimum and post-fabrication of pairs with reduced low frequency and thermal noise. Applying an intelligent post-fabrication selection process [13] in a VCO using the array to select cross-coupled pairs with reduced low frequency noise and thermal noise, the phase noise is lowered from the average by 2 dB at 600-kHz and 1-MHz offsets, and by 1.5 dB at 3-MHz offset, respectively from a 3.8-GHz carrier, and it is lowered by 3.5 dB from the maximum phase noise at the offset frequencies.

The average and maximum phase noise should be close to those for a conventional VCO using a cross-coupled pair formed with two transistors but with the same total width as that of the selected cross-coupled pairs in the array. The lowest phase noise of -122 dBc/Hz, -127 dBc/Hz, -137.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively from a 3.8-GHz carrier has been measured using the PLL method with 50 averaging and without the correlation feature in a Keysight E5052B Signal Source Analyzer.

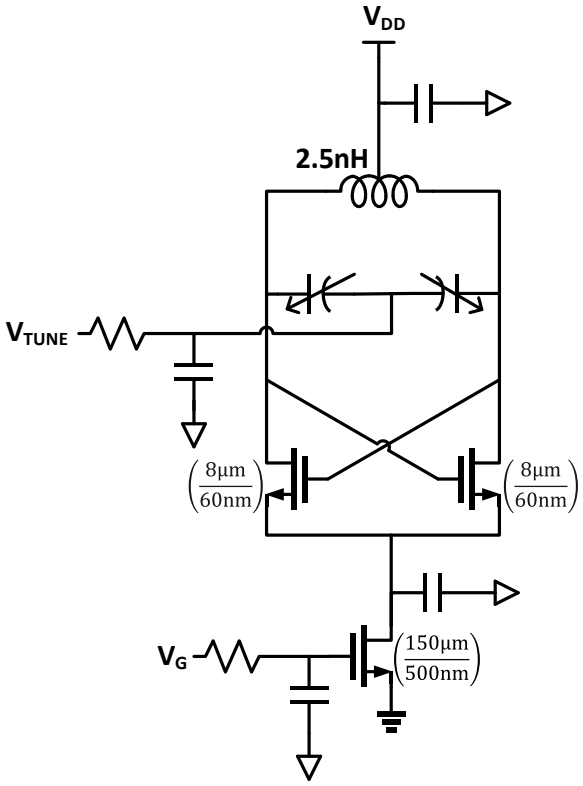


Figure 2.3. Conventional NMOS VCO.

2.3 VCO Using an Array of Near Minimum Sized Transistors

2.3.1 VCO Design

To demonstrate the technique of reducing the impact of low frequency noise and thermal noise in an LC VCO by using an array of transistors sized near the minimum and post-fabrication selection, a VCO operating around 4 GHz using an array of cross coupled pairs of near minimum-size transistors is implemented. To start, a conventional VCO using a cross-coupled NMOS pair of 8-µm width and 60-nm length with an NMOS tail current source as shown in Figure 2.3 is first designed. By using a long and wide NMOS tail current transistor of 150-µm width and 500-nm length, the low frequency noise of the cross-coupled devices is made the dominant source. The top

plate of varactors is connected to V_{DD} through an inductor. The 2.5-nH inductor is formed with a 5-turn circular symmetric center-tapped structure shown in Figure 2.4. It has a simulated Q-factor of 12 at 4 GHz. The varactors are of an accumulation mode type implemented as an NMOS structure in an n-well [28].

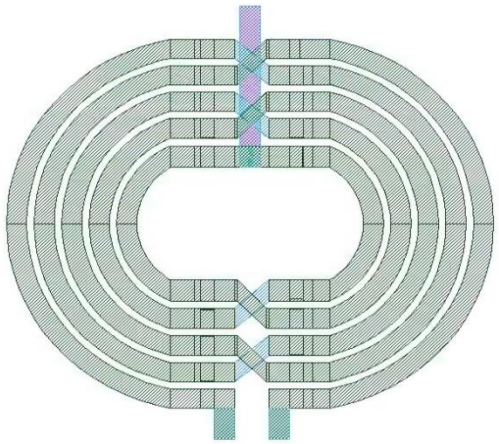


Figure 2.4. 5-turn circular symmetric center-tapped inductor.

Figure 2.5 shows the proposed VCO that uses an addressable array of 16x4 (64) NMOS cross-coupled transistor pairs for post-fabrication selection of pairs for reducing low frequency and thermal noise. Each transistor forming the cross-coupled pair in Figure 2.3 is divided into 32 transistors of width and length of 250 nm and 60 nm, respectively or an area of 15,000 nm^2. To provide redundancy, 32 additional pairs are added. Each unit also includes 2.5-μm wide switches at the drain of the cross-coupling transistors for selection. The switches of the 64-pair cross-coupled transistor pairs are controlled by a 64-bit Serial-In Parallel-Out (SIPO) D flip-flop chain. The D flip-flop is falling edge-triggered. The layout of the cross-coupling transistor array with the SIPO is shown in Figure 2.6. A block diagram of the 64-bit SIPO chain of D flipflops is shown in Figure 2.7.

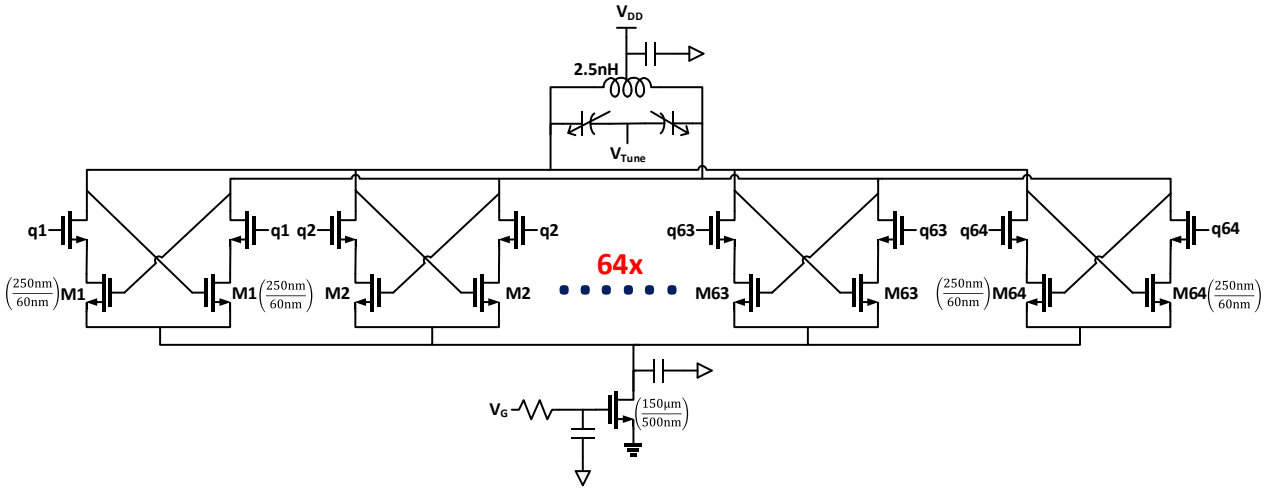


Figure 2.5. Proposed VCO using an array of cross-coupled near minimum size NMOS transistor pairs.

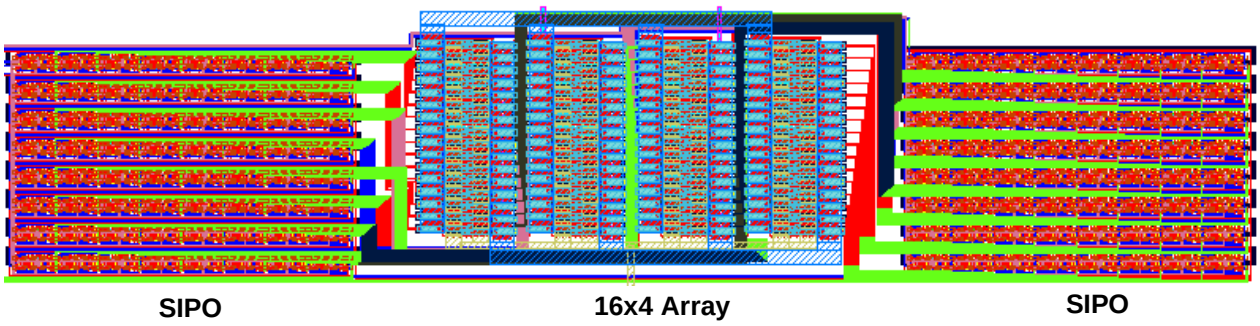


Figure 2.6. Layout of the Cross-Coupling Transistor Array with the Serial-In Parallel-Out (SIPO) chain of D flipflops.

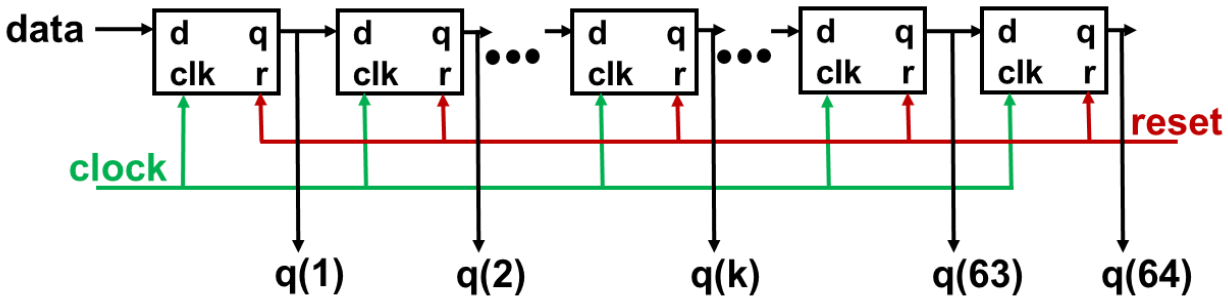
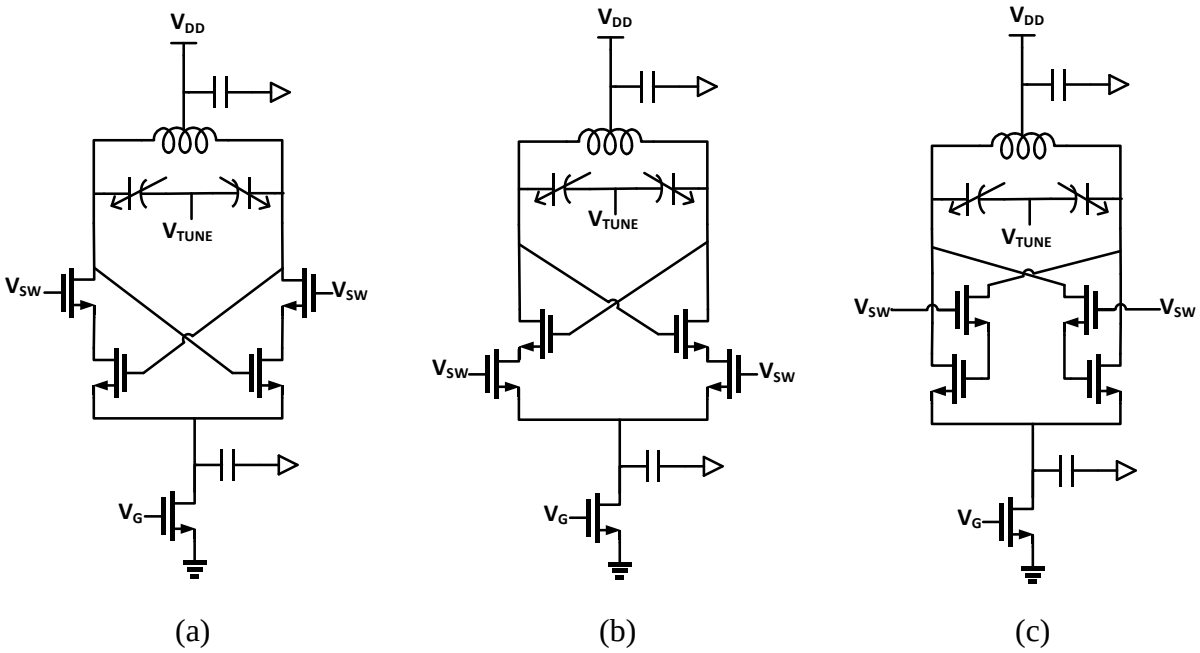


Figure 2.7. Block diagram of the 64-bit SIPO chain of D flipflops.

2.3.2 Switching Core Options and Simulations

The selection switch for a pair can be placed at the gate, drain or source of the transistor as shown in Figure 2.8. The phase noise with the switch at the gate of the transistor is worse than that for the VCO with the switch at the drain of the transistor for the same switch size. This is due to the switch resistance being in series with the gate impedance of the cross coupled transistors. The switch at the gate can be sized larger to reduce the gate resistance, but this however increases the the parasitic capacitances of the switch as well as cell area.



(a) (b) (c)

Figure 2.8. (a) Drain-switched core, (b) Source-switched core, (c) Gate-switched core.

The switch at the source side of transistor degenerates the core transistors and also degrades the phase noise. Figure 2.9 shows the simulated phase noise of a VCO using the array for different switching cores at the tuning voltage of 0V and with 32 cross-coupled transistor pairs switched ON. A switch size of 2.5-μm width and 60-nm length is chosen for all the switching cores. The

phase noise of the VCO using the array with drain switched core at 1-MHz offset is -119 dBc/Hz from a 3.83-GHz carrier, whereas the phase noise with gate switched core is -116 dBc/Hz at 1-MHz offset, which is 3 dB higher than that of the drain switched core. The phase noise with the source switched core is -118 dBc/Hz at 1-MHz offset, which is 1 dB higher than that of the drain switched core.

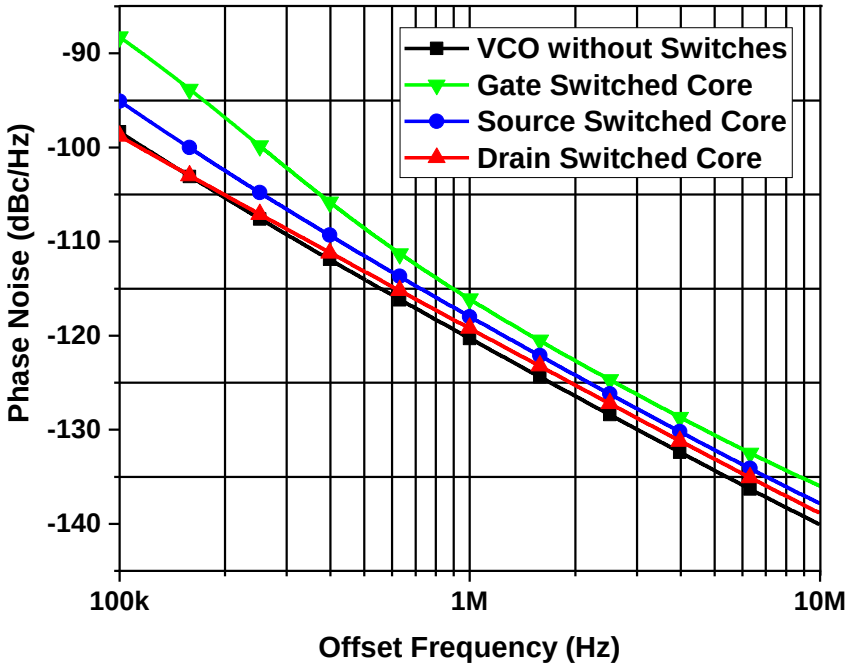


Figure 2.9. Simulated phase noise of VCO with and without switches for post fabrication selection.

The switch size mentioned earlier is chosen to ensure the additional parasitics of the switches do not significantly degrade both the phase noise performance and tuning range of the VCO array compared to that of a conventional VCO. Figure 2.9 also shows the simulated phase noise of the conventional VCO and that of a VCO using the array with drain side switching at a tuning voltage of 0V. Compared to the VCO without switches, there is ~1 dB phase noise

degradation for the VCO using the array with drain-side switching. The phase noise of the conventional VCO is -120 dBc/Hz at 1-MHz offset from a 3.98-GHz carrier.

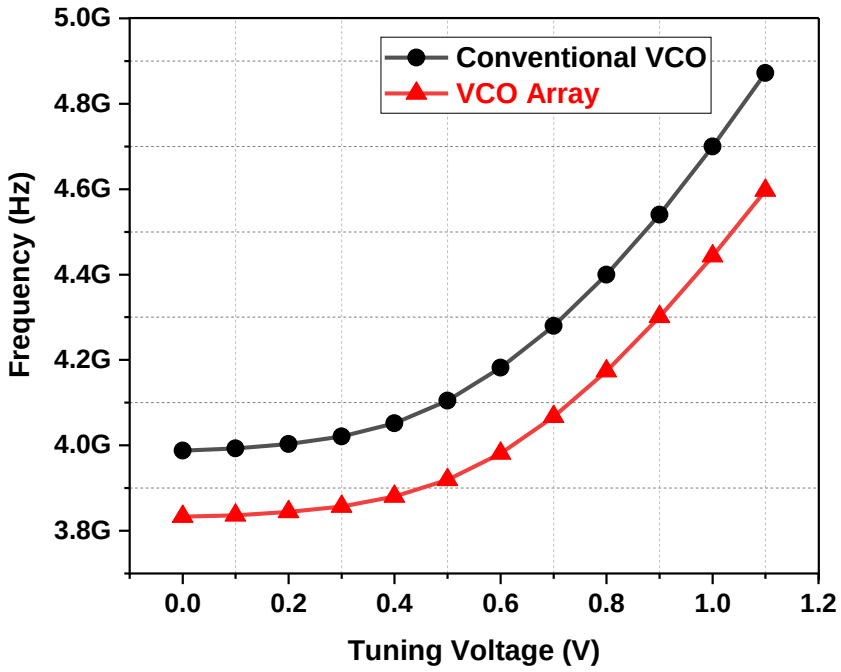


Figure 2.10. Tuning Range comparison between the Conventional VCO without switches and VCO array with drain side switching.

Figure 2.10 shows the tuning range comparison between the conventional VCO without switches and the VCO using the array with drain side switching and 32 cross-coupled pairs switched ON. The conventional VCO without switches oscillates from 3.98-GHz to 4.87-GHz which corresponds to a simulated tuning range of 20%. The VCO using the array with drain side achieves a simulated tuning range of 18% from 3.83-GHz to 4.59-GHz which is only 2% smaller compared to that of the conventional VCO. Figure 2.11 shows the simulated single-ended transient voltage of VCO array. The peak-to-peak voltage swing is ~1.3V.

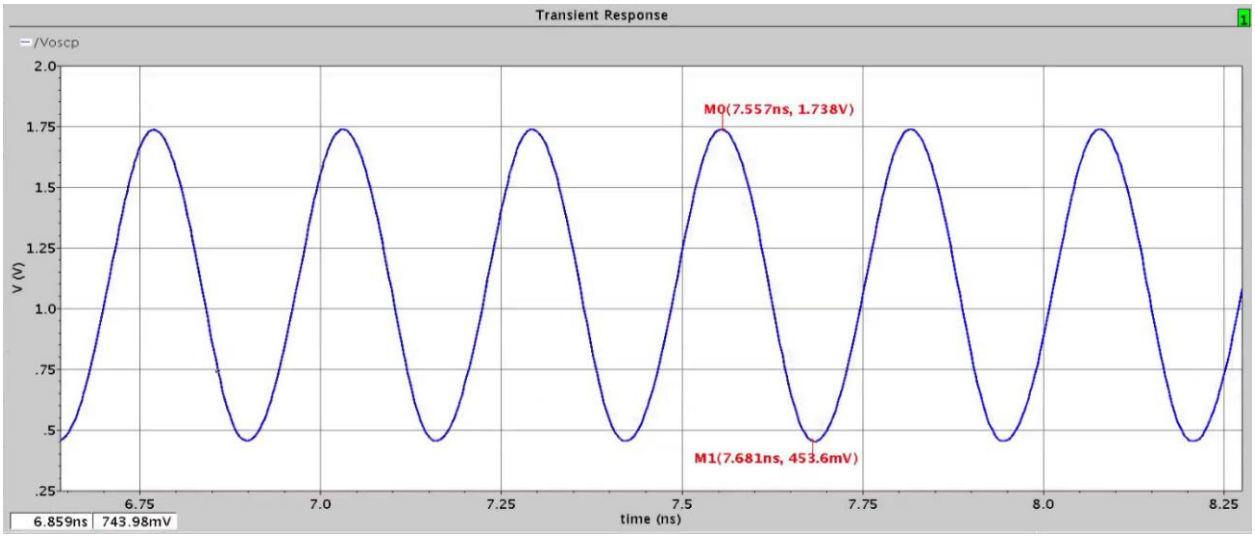


Figure 2.11. Single-ended peak to peak voltage of the VCO using array.

2.4 Intelligent Search Via Genetic Algorithm

Searching among the vast space of 2^{64} possible combinations of switched-on cross-coupled transistor pairs to identify the ones having the lowest phase noise requires an intelligent algorithm. Hamming distance-driven search [29] explores a predetermined number of options in the hamming distance vicinity of initial seed and may converge to a local minimum. Instead, a classic genetic algorithm, which introduces more entropy in the search and is particularly efficient in exploring high-dimensional unstructured spaces is employed. In addition, the genetic algorithm makes no assumptions about the search space and is driven by randomness, which makes it superior in searching for the combinations having low phase noise in a large space.

A flowchart of the genetic algorithm is shown in Figure 2.12. It defines the phase noise at a particular offset-frequency as a “fitness function” to be optimized. Each cross-coupled transistor pair is represented by a bit, with a value of “1” indicating the pair is switched ON. The algorithm

starts by generating a random population of chromosomes (i.e. binary strings with a varying length) with a user-defined range of number of "1"s for which the fitness function is measured.

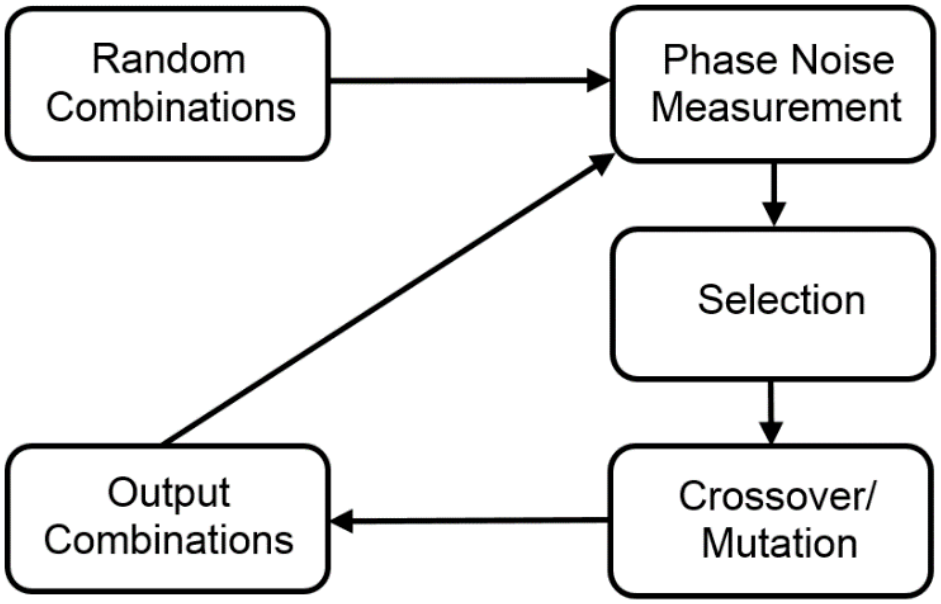


Figure 2.12. Flowchart of the Genetic Algorithm for Phase Noise Reduction.

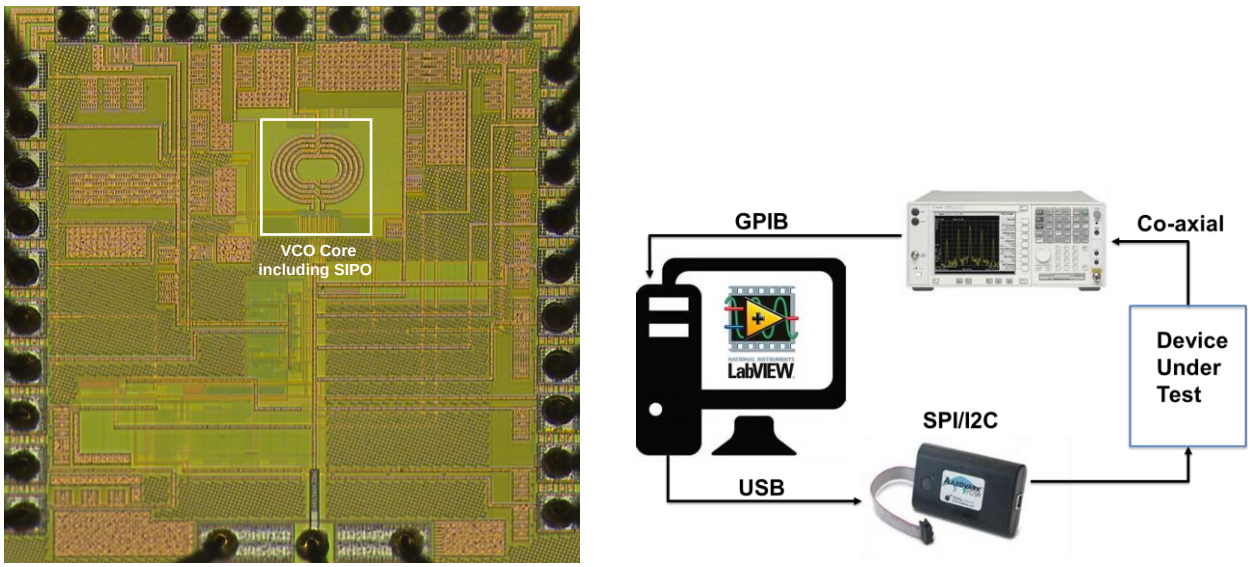
The top 50% of the initial population with the lowest phase noise is retained and the rest of population is discarded. The binary strings in the top 50% of the population are named as "parent strings". The population is then replenished with new chromosomes by mutating the pairs of parent strings at a randomly chosen bit-location, called the "crossover point.

All the bits to the right of the crossover point are swapped between pairs of parent strings to generate new offspring strings. The rationale of this operation is that, after multiple generations, mutation will allow a sufficiently diverse space to be explored while the crossover will discard the bits having high phase noise in the parent strings and, thereby generating new offspring strings

with lower phase noise. The algorithm continues until a user-selected fitness limit is achieved, or until a sufficient number of combinations with adequately low phase noise are found.

2.5 Measurement Results and Performance Benchmark

A prototype of the VCO array was fabricated in a 65-nm CMOS process with 10 Copper metal layers and wire-bonded onto a printed circuit board (PCB) for measurements. The die micrograph is shown in Figure 2.13(a). The core area of the VCO array including SIPO is 0.025 mm^2. A setup for measuring the phase noise with different combinations of cross-coupled pair units is shown in Figure 2.13(b). 32 of the 64 cross-coupling transistor pairs are switched ON in the VCO by sending a random set of 32 "1" bits using LabVIEW to the DUT using an SPI/I2C interface. The phase noise is measured using the phase locked loop (PLL) method of the Keysight E5052B Signal Source Analyzer and is collected using LabVIEW.



(a) (b)

Figure 2.13. (a) Die Micrograph of the proposed VCO, (b) Measurement setup for phase noise.

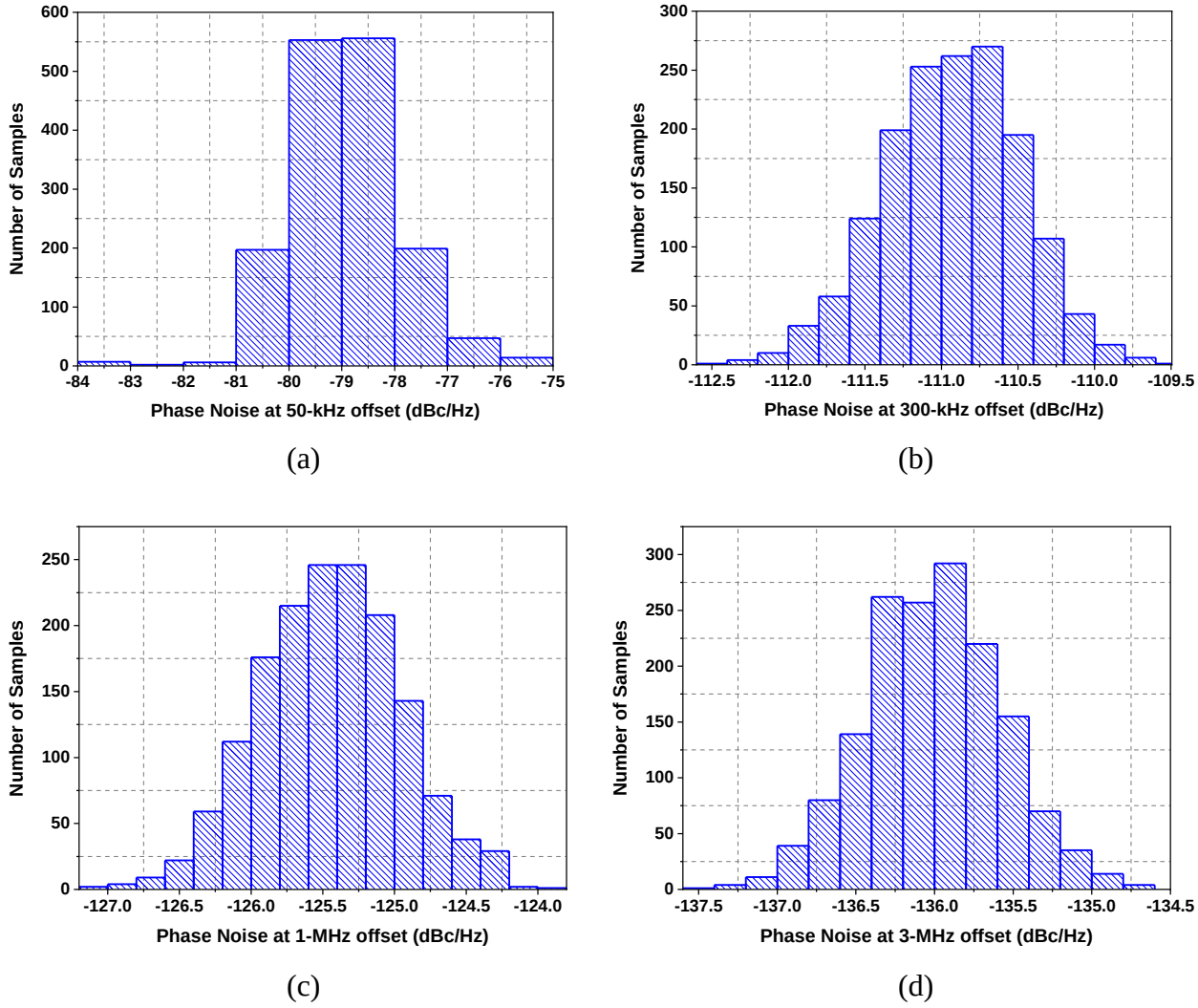


Figure 2.14. Histograms of phase at (a) 50-kHz offset, (b) 300-kHz offset, (c) 1-MHz offset, and (d) 3-MHz offset from a 3.8-GHz carrier, when 32 cross-coupled transistor pairs are switched ON.

Figure 2.14 shows the histograms of measured phase noise variations of ~1500 random combinations at 50-kHz, 300-kHz, 1-MHz and 3-MHz offsets from a 3.8-GHz carrier, respectively when 32 cross-coupled transistor pairs out of the 64 pairs are switched ON. Figure 2.15 shows the phase noise plots of these 1500 combinations. Two main observations can be made from these figures: (i) From 10-kHz offset to 60-kHz offset, the phase noise variation is around 9 dB, which mainly is due to the low frequency noise variation of the core devices being the dominant

determining factor, and (ii) variation of phase noise is ~3.5 dB at the higher offsets of 1-MHz and 3-MHz, respectively.

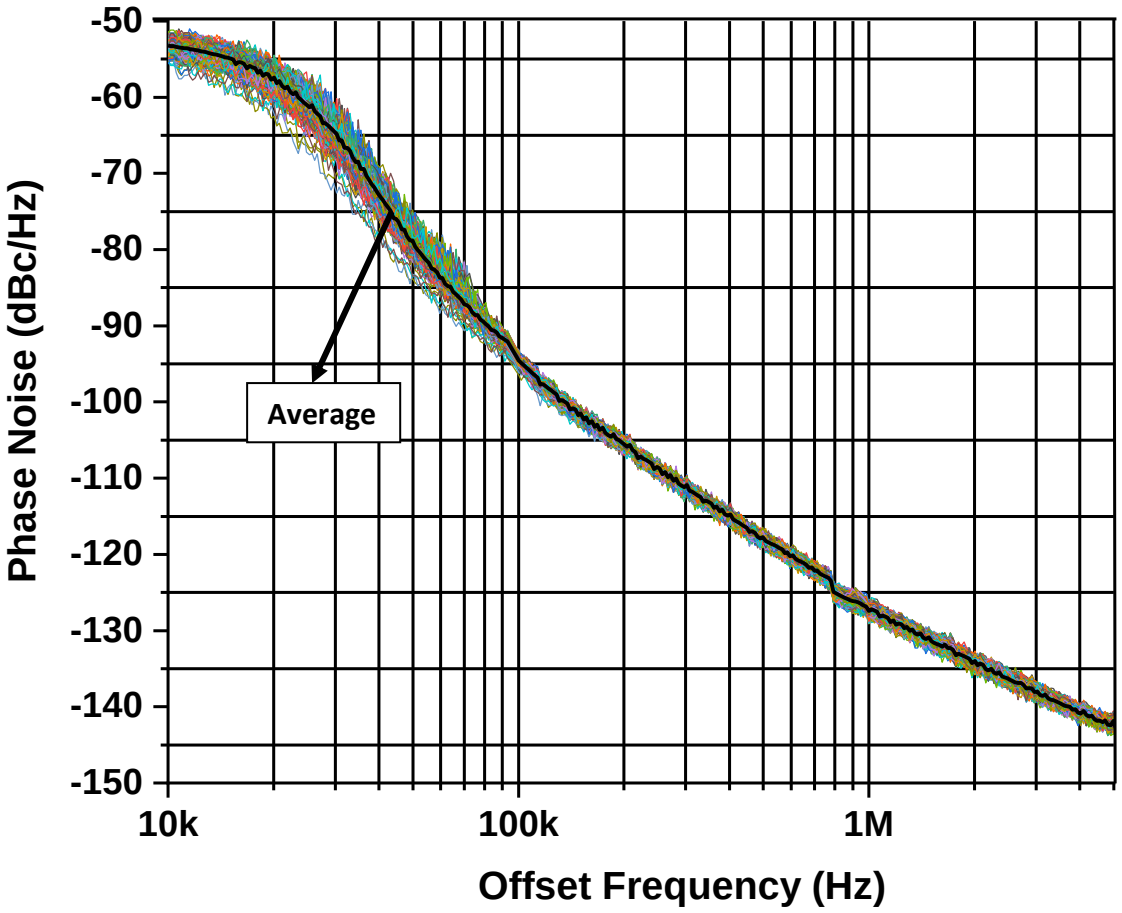
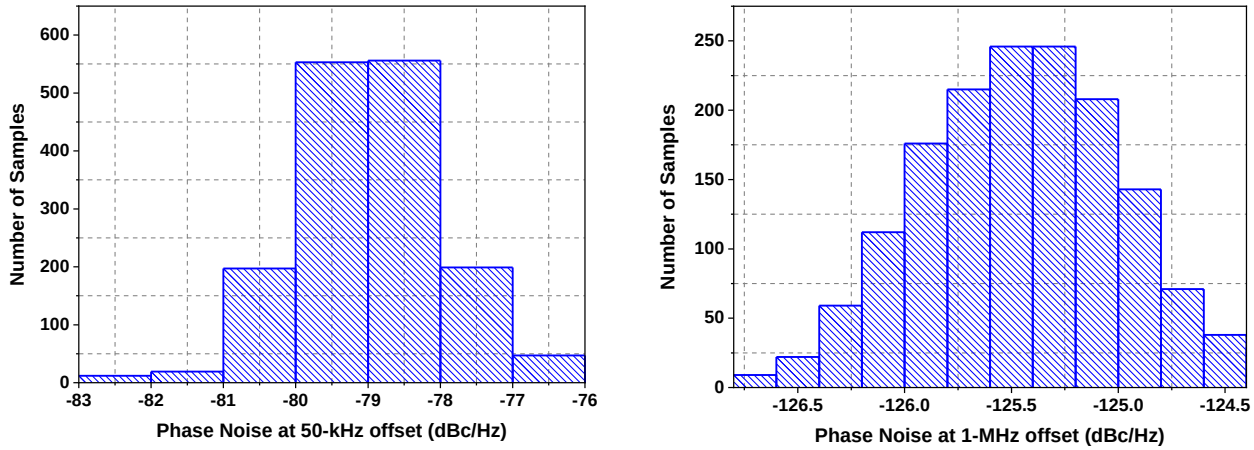


Figure 2.15. Measured phase noise plots when 32 cross-coupled transistor pairs are switched on. The average phase noise is also shown in the figure.

The phase noise variation decreases with an increasing offset because the contributions of thermal noise increase at higher frequency offsets. It can also be noted from Figure 2.15 that the lowest phase noise is 9 dB lower than the maximum phase noise at 50-kHz offset, whereas it is ~3-3.5 dB lower than the maximum phase noise at 1-MHz and 3-MHz offsets. Figure 2.16 shows the histograms of phase noise variations of ~1500 random combinations at 50-kHz and 1-MHz

offsets from a 3.78-GHz carrier when 48 cross-coupling transistor pairs out of the 64 pairs are switched ON. The phase noise variations are ~7 dB at 50-kHz offset and ~2.5 dB at 1-MHz offset. These variations are 2 dB and 1 dB lower than that when 32 pairs are selected out of 64, respectively.



(a) (b)

Figure 2.16. Histograms of phase noise at (a) 50-kHz offset and (b) 1-MHz offset from a 3.78-GHz carrier, when 48 cross-coupled pairs are switched ON.

The reduction of phase noise variation with an increasing number of switched-on cross-coupling pairs can be attributed mainly to the law of large numbers. In addition to the variations in low frequency noise and thermal noise, variations of the carrier power of cross-coupling transistor pairs can also contribute to the phase noise variation. The variation of the output power for the combinations with an equal number of cross-coupled pairs switched ON should be mainly due to the variations in the VCO bias current and parallel resistance R_p of the tank due to the variations of the output resistance of the cross-coupling transistor pairs.

The output power (P_o) in an LC VCO is directly proportional to the square of product of current flowing through the cross-coupled pairs (I_{cp}) and the total parallel resistance (R_p) in the tank [1], as shown in (2.4).

$$P_o \propto (I_{cp} R_p)^2 \tag{2.4}$$

Since I_{cp} is set by the current source, the power variation should be due to the variation of R_p. Neglecting the losses due to the gate resistance, substrate resistance and varactor, R_p as shown in (2.5) can be given by the parallel combination of the equivalent resistance (R_{pL}) of inductor and output resistance (R_{ds}) of the cross-coupled transistor pairs [62].

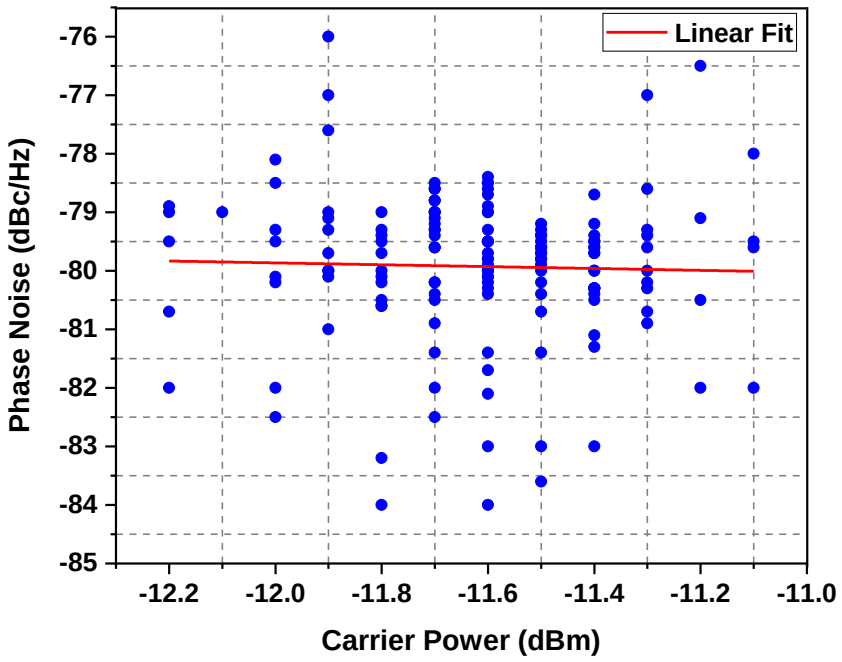
$$R_p = R_{pL} \,||\, R_{ds} \tag{2.5}$$

The total R_{ds} in the VCO array is given by (2.6)

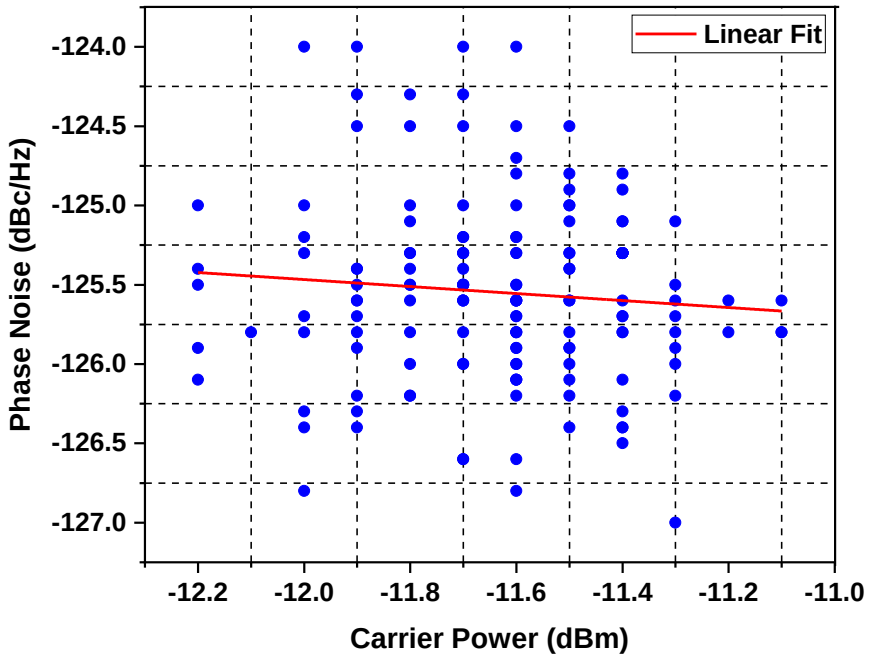
$$R_{ds} = R_{ds,1} || \, R_{ds,2} \,||\, R_{ds,3} \;\ldots\ldots R_{ds,n}. \tag{2.6}$$

where $R_{ds,1}$ to $R_{ds,n}$ are the output resistances of a single transistor from each selected cross-coupling transistor pair, and n is the total number of pairs switched ON out of 64.

Figures. 2.17(a) and (b) show the correlation between carrier power and phase noise at 50-kHz offset and 1-MHz offsets, respectively when 32 cross-coupled transistor pairs are switched ON. Randomly chosen subsets of combinations from phase noise bins in Figure 2.14 are selected for carrier power measurements. The variation in carrier power is only ~1 dB for 32 selected pairs. A maximum phase noise variation of ~6 dB is observed at a carrier power of -11.6 dBm at 50-kHz offset and the correlation coefficient using the linear fit shown in Figure 2.17(a) is only 3%. Whereas at 1-MHz offset, a maximum phase noise variation of ~3 dB is observed at multiple



(a)



(b)

Figure 2.17. Phase Noise versus Carrier Power at (a) 50-kHz offset and (b) 1-MHz offset from the 3.8-GHz carrier when 32 cross-coupled pairs are switched ON.

carrier power levels (-11.6 dBm, -11.7 dBm and -12 dBm), and the correlation coefficient using the linear fit shown in Figure 2.17(b) is only 9%. These results indicate that the variation of phase noise is not due to the carrier power variation.

The genetic algorithm for post-fabrication selection is coded in Python and integrated with LabVIEW. Offset frequencies of 50 kHz, 600 kHz, 1 MHz and 3 MHz were used in the genetic algorithm to lower the phase noise. Around 100 combinations were generated by the algorithm in each generation. The user-defined range for the number of selected cross-coupling pairs is from 20 to 60. Figure 2.18 shows the measured lowest phase noise at 50-kHz, 600-kHz, 1-MHz and 3-MHz offsets, respectively at varying generations. The genetic algorithm converges to the combinations having the lowest phase noise of -84 dBc/Hz at 50-kHz offset, -122 dBc/Hz at 600-kHz offset, -127 dBc/Hz at 1-MHz offset and -137.5 dBc/Hz at 3-MHz offset, respectively from a 3.8-GHz carrier.

Figure 2.19 shows the phase noise plot of the best combination having the lowest phase noise of -127 dBc/Hz at 1-MHz offset from a 3.8-GHz carrier when 32 cross-coupling pairs are selected. The slope of -2 is also shown in the figure, which is between 900-kHz and 9-MHz offsets. The lowest phase noise when 32 pairs are switched ON is 0.5 dB lower at 1-MHz offset than that for the best combination when 48 pairs are selected, whereas the phase noise when all the 64 pairs are switched ON is -124.5 dBc/Hz at 1-MHz offset, which is 2.5 dB higher than that for the best combination having 32 selected pairs. Increasing the number of selected cells increases the overall transistor width while keeping the VCO DC current constant due to the tail current source. This increases the transconductance while keeping R_{ds} thus R_p approximately constant, thereby

increasing the VCO loop gain ($g_m R_p$). This shows that the phase noise of VCO using the array is not reduced by an increase of the VCO loop gain.

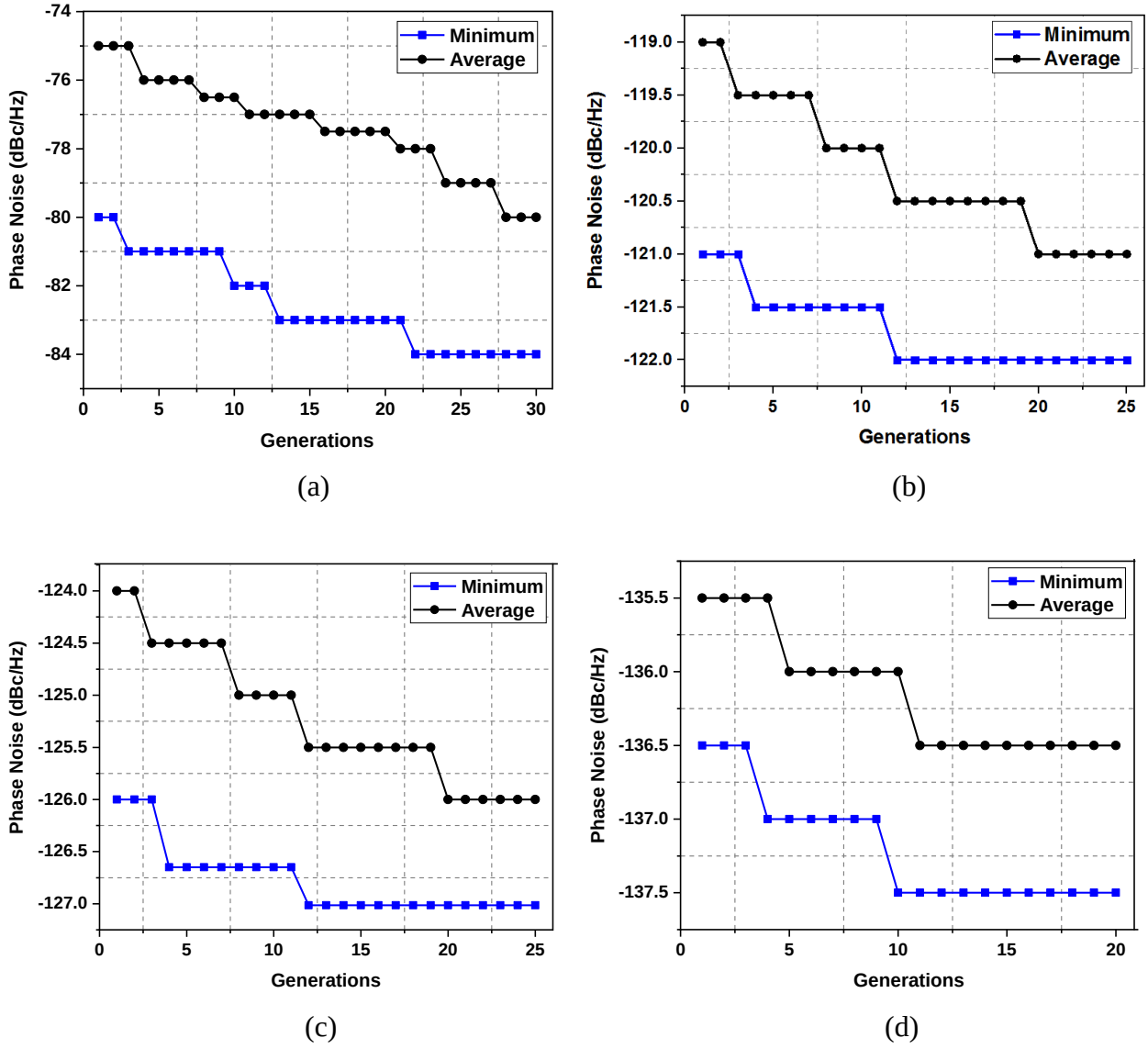


Figure 2.18. Phase noise reduction using the Genetic algorithm at (a) 50-kHz offset, (b) 600-kHz offset, (c) 1-MHz offset and (c) 3-MHz offsets from a 3.8-GHz carrier.

Variations of the VCO gain (K_{vco}) with the number of selected cross-coupled pairs can also contribute to the phase noise variation, since a higher VCO gain increases the phase noise due to

increased AM-PM conversion and vice-versa [17]-[18]. Figure 2.20 shows the phase noise at 1-MHz offset versus measured VCO gain for the samples used for the histograms in Figure 2.14. 32 cross-coupled transistor pairs were switched ON. The VCO gain shown in the figure is measured for a tuning voltage from 0 to 0.1V. The minimum phase noise is measured at a tuning voltage of 0V for all the combinations of cross-coupling transistor pairs. As observed in the figure, the maximum phase noise variation of ~3 dB is observed at the VCO gains of 30 MHz/V and 40 MHz/V. The correlation coefficient using a linear fit shown in Figure 2.21 is only 10%. This shows that the phase noise variations of the VCO using the array are not due to variations of the VCO gain.

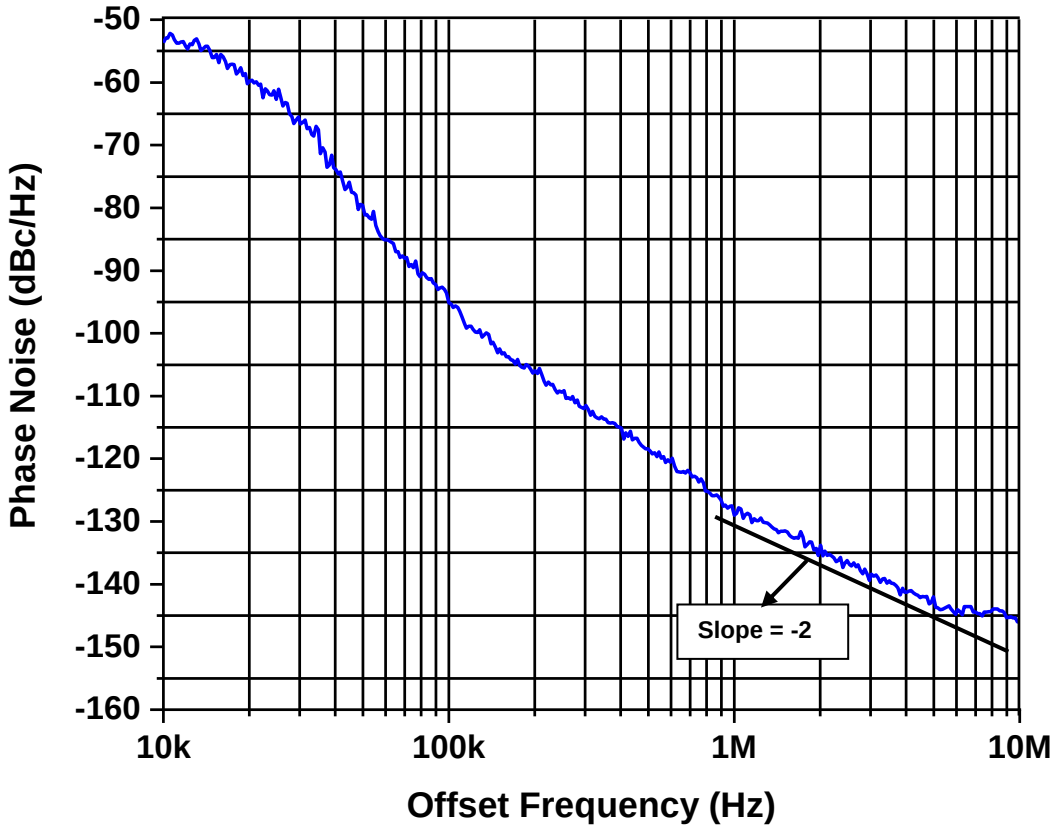


Figure 2.19. Phase noise of the best combination having lowest phase noise at 1-MHz offset from a 3.8-GHz carrier.

This process of elimination and the fact that phase noise can vary by many dBs at a given VCO output power and gain suggest that the likely cause for the phase noise variation is the variations of the low frequency noise and thermal noise. The increase of phase noise by 2.5 dB when all the 64 pairs are switched ON compared to the case when 32 pairs are selected shows that there exist some pairs of transistors having high thermal noise and low frequency noise, and these pairs should be discarded to reduce the phase noise of VCO.

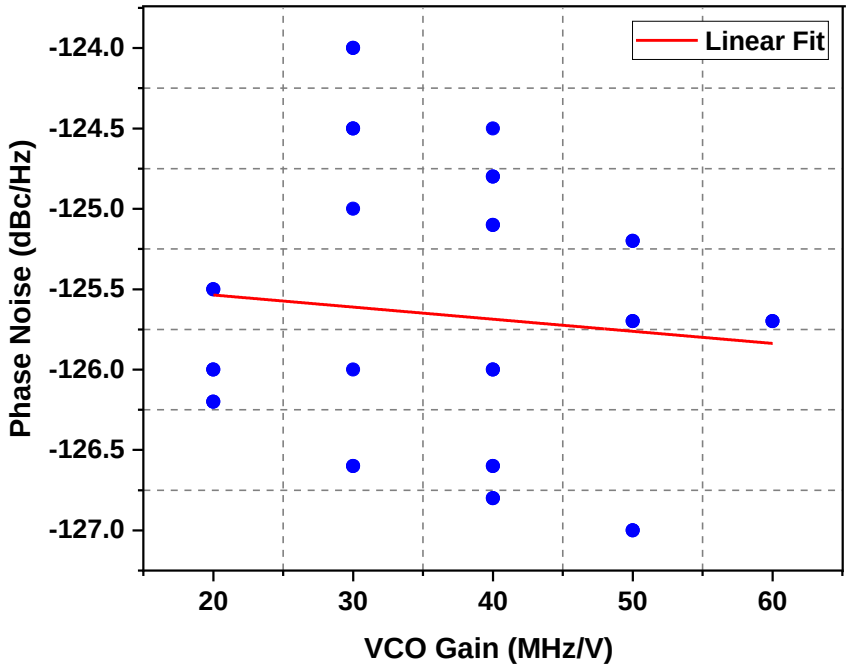


Figure 2.20. Phase noise at 1-MHz offset versus VCO gain when 32 cross-coupled pairs are switched ON.

The VCO was characterized using the PLL method in E5052B because multiple works reporting low phase noise VCO have used the PLL method of E5052B for their measurements [43], [46]. The proposed VCO in this work was also characterized using the phase noise utility in Keysight E4440A PSA. The lowest phase noise measured using the E4440A PSA is 9 dB higher than that in E5052B. Improvements are expected from using the PLL method in E5052B because

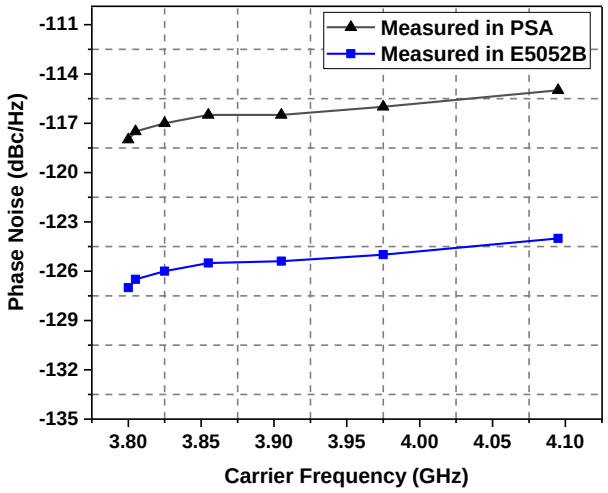
it locks the free-running VCO to measure its phase noise, although the 9-dB difference seems large. Measurements were checked and repeated multiple times to ensure proper operation of the instruments. Because of this, the figure of merit (FoM) in (2.7) normalizing the oscillation frequency (f_o), power dissipation (P_{DC}), and phase noise (L_{offset}) at a particular offset frequency (f_{offset}) have been estimated from the measurements from both E4440A PSA and E5052B.

$$FoM = 20log\left(\frac{f_0}{f_{offset}}\right) - L_{offset} - 10log\left(\frac{P_{DC}}{1mW}\right) \tag{2.7}$$

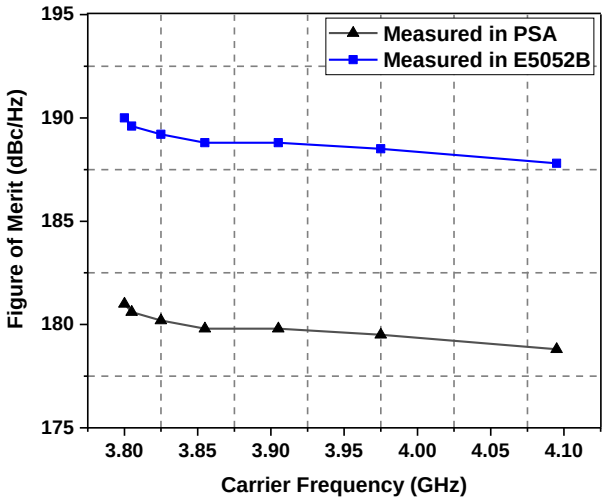
Figures. 2.21(a) and (b) show the phase noise and FoM at 1-MHz offset across the frequency tuning range for the best combination, respectively. There is ~3 dB variation of phase noise at 1-MHz offset across the tuning range. The peak FoM of 190 dBc/Hz at 1-MHz offset is achieved at the minimum frequency of 3.8 GHz where the tuning voltage is 0 V. The FoM measured in the PSA is 9 dB lower than that in E5052B. There is ~2 dB variation of FoM across the tuning range. This is due to the phase noise degradation at higher tuning voltages, which in turn is caused by the higher AM-PM conversion due to higher VCO gains [17]-[18]. This problem can be resolved by linearizing the VCO tuning curve with a programmable capacitor bank, and thereby maintaining a lower Kvco over the entire tuning range [34].

Nevertheless, the VCO still achieves an FoM of greater than 187.5 dBc/Hz (measured in E5052B) over the tuning range. Table 2.1 summarizes the improvements of phase noise (PN) from the average and maximum phase noise at various offsets from the 3.8-GHz carrier. The phase noise at 50-kHz offset is lowered by 5-6 dB from the average phase noise in the measurements done in both PSA and E5052B, and by 9 dB from the maximum in E5052B and by 12 dB in PSA. Whereas

at 600-kHz, 1-MHz and 3-MHz offsets, it is lowered by 1.5-2 dB from the average and by ~3.5 dB from the maximum. Both the measurements using the PSA and E5052B show that phase noise can be lowered by applying an intelligent post-fabrication selection process to a VCO employing an array of individually selectable cross-coupled pairs of transistors with dimensions near the minimum for a given process.



(a)



(b)

Figure 2.21. (a) Phase Noise at 1-MHz offset and (b) FoM at 1-MHz offset for the best combination across the tuning range.

Table 2.1. Phase noise improvement from average and maximum at various offset frequencies.

Offset	Improvement from Average (in E5052B)	Improvement from Max (in E5052B)	Improvement from Average (in PSA)	Improvement from Max (in PSA)
50 kHz	5 dB	9 dB	6 dB	12 dB
600 kHz	2 dB	3.5 dB	2 dB	3.5 dB
1 MHz	2 dB	3.5 dB	2 dB	3.5 dB
3 MHz	1.5 dB	3 dB	1.5 dB	3.5 dB

Table 2.2. Performance Benchmark with the State-of-the-Art CMOS LC VCO's.

	Frequency (GHz)	PN at 1-MHz offset (dBc/Hz)	Power Dissipation (mW)	Tuning Range (%)	PN at 1-MHz offset (dBc/Hz) Normalized to 5 GHz	Peak FoM (dBc/Hz)	Core area (mm^2)	[1] Peak FoM_A (dBc/Hz)	CMOS Technology
This Work (PLL Method in E5052B)	3.8	-127	7	7.8	-126.6	191	0.025	207	65nm
This Work (E4440A PSA)	3.8	-118	7	7.8	-115.6	182	0.025	198	
[35] ISSCC'21	5	-130	6.1	23.9	-130	196.2	0.24	202.4	65nm
[36] ISSCC'21	3.09	-138.9	20.9	26.6	-134.7	195.1	0.36	199.5	40nm
[37] JSSC'18	4	-124.3	1.2	25.5	-122.3	195.5	0.14	204	65nm
[38] VLSI'17	4.55	-123.4	1.35	5.5	-122.6	195.3	N/A	N/A	180nm
[39] JSSC'16	5.4	-126.7	12	25	-127.3	190.5	0.13	199.3	40nm
[40] ISSCC'16	4.83	-119	0.5	13.8	-118.7	195.7	0.18	203.1	28nm
[41] JSSC'15	4.35	-135	41.6	19	-133.8	191.6	0.2	198.6	65nm
[42] ISSCC'15	2.4	-128.4	4.2	1.7	-122	189.8	0.09	200.2	130nm
[43] ISSCC'14	3.72	-129.3	20	88.7	-126.7	187.7	0.432	191.3	40nm
[44] JSSC'13	3.7	-131	15	25	-128.4	190.6	0.12	199.8	65nm
[45] JSSC'13	3.42	-127	6.6	28	-123.7	189.5	0.08	200.5	90nm
[46] JSSC'12	3.69	-128.3	10.4	76.5	-125.6	189.5	0.294	194.8	65nm

Table 2.2 summarizes the performance and benchmarks of the proposed VCO array in this paper with that of the other low phase noise CMOS LC VCO's in the literature. The main aim of

this paper is to verify the proposed technique. The peak FoM of VCO array is 191 dBc/Hz at 3-MHz offset from a 3.8-GHz carrier. Another figure of merit, FoM_A which also takes the core area of VCO into account is calculated for all the works and included in the table. The VCO array in this paper exhibits an excellent FoM_A of 207 dBc/Hz when the phase noise is measured using the PLL method in E5052B. Even from the PSA measurements, FoM_A of 198 dBc/Hz is on par with the recently published low phase noise CMOS LC VCO's.

An important point to note is that the proposed technique for reducing phase noise using post-fabrication selection of transistor pairs sized near the minimum is orthogonal to the other phase noise reduction techniques since the proposed method reduces the device noise itself. This technique can be applied in combination with any other phase noise reduction techniques [35]-[46]. For instance, it can be used along with the harmonic shaping technique in a Class-F VCO and achieve an ultra-low phase noise. In this way, the benefits of noise reduction of both the techniques can be exploited. Lastly, it should be possible to integrate an on-chip phase noise measurement circuit in order to make this technique more practical [63]-[68].

2.6 Conclusion

A technique is demonstrated to reduce the phase noise of LC VCO's by employing an array of individually selectable cross-coupled pairs formed using transistors with dimensions near the minimum and by employing an intelligent post-fabrication selection. The technique reduces the phase noise by taking advantage of the fact that when transistor dimensions are reduced, the low frequency noise and thermal noise can vary significantly. Using minimum size transistors to reduce the impact of low frequency noise is opposite to the conventional approach of using larger

transistors, which relies on averaging to the value determined by the PDK model. Applying an intelligent post-fabrication selection process using a genetic algorithm to an LC VCO employing the array, the phase noise at 600-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier is lowered by 1.5-2 dB from the average phase noise and by ~3.5 dB from the maximum phase noise. The proposed technique can be applied with other phase noise reduction techniques to realize the ultra-low phase noise oscillators.

CHAPTER 3

REDUCTION OF PHASE NOISE AND JITTER IN FREQUENCY SYNTHESIZER'S BY INCORPORATING A VCO EMPLOYING AN ARRAY OF CROSS-COUPLED TRANSISTOR PAIRS AND INTELLIGENT POST-FABRICATION SELECTION

3.1 Introduction

A frequency synthesizer generates an output signal whose frequency is a fixed or programmable multiple of input reference frequency. It has wide applications in modern RF/analog systems. In RF systems, the output of such a frequency synthesizer can be used as the local oscillator signal in transceivers. It may also be used to perform frequency modulation and demodulation, as well as to regenerate the carrier from a received modulated signal.

Most frequency synthesizers in wireless systems employ phase locked loops (PLL's) to generate a clean and stable LO signal in both the transmitters and receivers. Phase-locking is built around a VCO that is free-running and drifts continuously over time, causing instability in the output carrier frequency and so is essential to achieve accuracy and stability for the signal generation.

The goal of this work is to demonstrate the concept of reducing both the in-band and out-of-band phase noise and thereby the overall jitter in a frequency synthesizer operating around 4-GHz. A 4-GHz Integer-N PLL fabricated in 65-nm CMOS incorporates a VCO employing an array of cross-coupled transistor pairs discussed in Chapter 2 and utilizes the intelligent post-fabrication selection.

3.2 Overview and AC Model of the 4-GHz Integer-N PLL

A block diagram of the 4-GHz Integer-N PLL is shown in Figure 3.1. PLL Output of 4-GHz is locked to an integer multiple (x 32) of the input reference signal of 125-MHz in a negative feedback configuration. Both the phase and frequency of the PLL output is locked to that of the input reference signal.

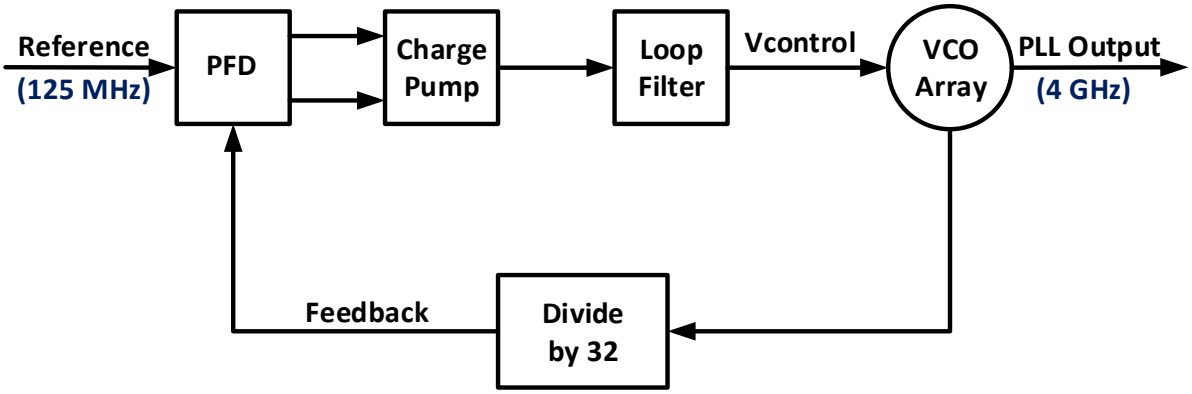


Figure 3.1. Block diagram of the 4-GHz PLL fabricated in 65-nm CMOS.

A phase Detector (PFD+Charge Pump) compares the phase & frequency difference between the two inputs and generates an error signal proportional to the difference. Loop filter suppresses the high-frequency components in the error signal and allows the DC value to pass to control the frequency of VCO. The loop is considered “locked” if the phase difference between the reference and divided signals is constant with time, and the frequencies of input reference and divided output are equal. Figure 3.2 shows a block diagram of the PFD with a charge pump. The PFD comprises of two D flip-flops with a reset control. The input reference signal, Ref and the divider output, Div are the two inputs to PFD.

Figure 3.3 shows the input and output waveforms of the PFD. If the frequency of Ref is higher than that of Div, then the PFD generates positive pulses for UP. If the frequency of Ref is lower than that of Div, then the PFD generates positive pulses for DN. If the frequencies are equal, then the PFD generates pulses at either UP or DN with a pulse width equal to the phase difference between Ref and Div [70]. The pulses at UP and DN control the charge pump switches, so the average current delivered to the loop filter is proportional to the phase difference.

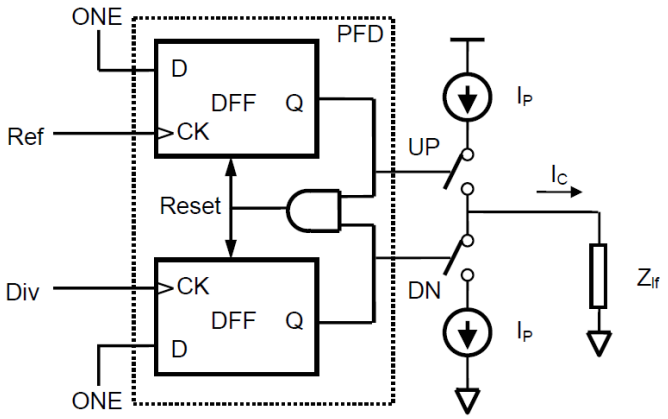


Figure 3.2. Phase frequency detector driving a charge pump [1].

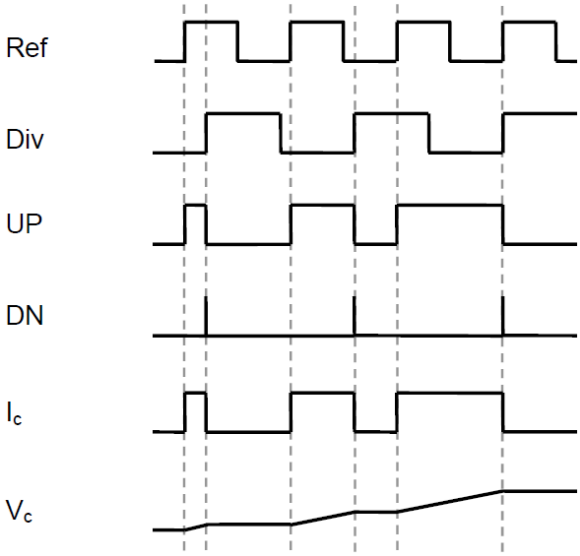


Figure 3.3. Input and output waveforms of a PFD [1].

Figure 3.4 shows a block diagram of the PLL with an s-domain transfer function for each block. Using the continuous-time approximation, the average error current of the charge pump over a reference cycle is [70]

$$\bar{i_c} = I_p \cdot t_p/T = I_p \cdot \phi_e/2\pi \,, \tag{3.1}$$

where I_p is the charge pump current, t_p is the charge pump current pulse width due to a phase error ϕ_e between the input reference and divider output signals. The charge pump gain is

$$\bar{i_c}/\phi_e = I_p/2\pi \,. \tag{3.2}$$

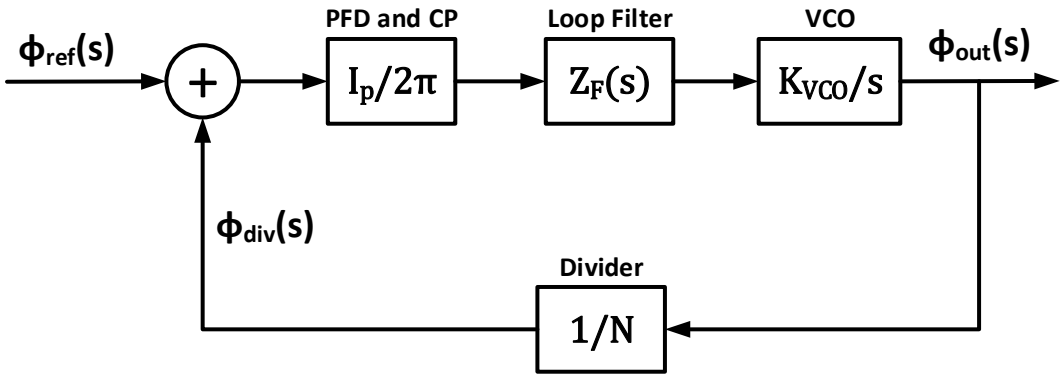


Figure 3.4. AC model of Integer-N PLL.

For an ideal VCO, the output frequency (ω_{out}) is a linear function of control voltage (V_{ctrl}), as given below [70]

$$\omega_{\text{out}} = \omega_{FR} + K_{VCO} V_{ctrl} \,, \tag{3.3}$$

where ω_{FR} is the free-running output frequency, and K_{VCO} is the VCO gain.

The VCO is a linear time-invariant system, with the V_{ctrl} as input and the phase $\phi_{\text{out}}(t) = K_{VCO} \int V_{ctrl} dt$ as the output. The transfer function of VCO is

$$\frac{\Phi_{\text{out}}}{V_{ctrl}}(s) = \frac{K_{VCO}}{s} \tag{3.4}$$

The frequency divider divides the phase by the factor ‘N’, so its transfer function is 1/N.

From the AC model in Figure 3.4, the open-loop transfer function, $H_{oL}(s)$ and close-loop transfer function of PLL, $H(s)$ is

$$H_{oL}(s) = \frac{I_p}{2\pi} \cdot Z_F(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} . \tag{3.5}$$

$$H(s) = \frac{\frac{I_p}{2\pi} \cdot Z_F(s) \cdot \frac{K_{VCO}}{s}}{1 + \frac{I_p}{2\pi} \cdot Z_F(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N}} , \tag{3.6}$$

$$= \frac{H_{OL}(s) \cdot N}{1 + H_{oL}(s)} . \tag{3.7}$$

3.3 PLL Transfer Function

A third-order passive loop filter for an Integer-N PLL is shown in Figure 3.5. The charge pump current (I_p) is the input, and control voltage (V_{ctrl}) is the output.

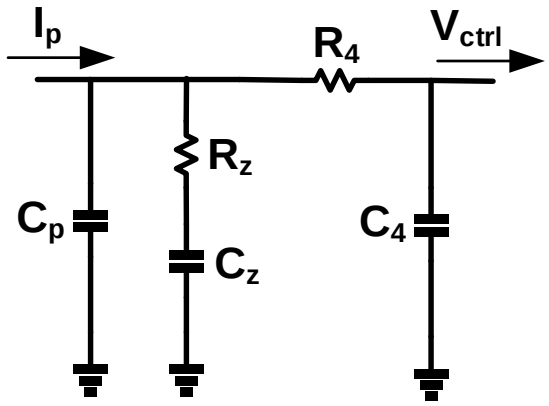


Figure 3.5. Third-Order passive loop filter.

Since the VCO transfer function includes a pole at the origin, the third-order loop filter makes the whole PLL a fourth-order loop.

For the third order loop filter, the transfer function is

$$Z_F(s) = \frac{V_{ctrl}(s)}{I_p(s)} \tag{3.8}$$

$$= \{\left(\frac{1}{sC_p}\right) // \left(R_z + \frac{1}{sC_z}\right)\}. \frac{1}{1+sC_4R_4} \tag{3.9}$$

$$= \frac{1+sR_zC_z}{s(sR_zC_zC_p+C_z+C_p)} \cdot \frac{1}{1+sC_4R_4}. \tag{3.10}$$

Therefore, the open loop and close loop transfer functions are

$$H_{OL}(s) = \frac{I_p}{2\pi} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \cdot \frac{1+sR_zC_z}{s(sR_zC_zC_p+C_z+C_p)} \frac{1}{1+sC_4R_4}, \tag{3.11}$$

$$H(s) = \frac{H_{OL}(s) \cdot N}{1+H_{oL}(s)}, \tag{3.12}$$

$$H(s) = \frac{K_{VCO}I_p(1+sR_zC_z)}{2\pi \cdot s^2(sR_zC_zC_p+C_z+C_p)(1+sC_4R_4)+\frac{K_{VCO}I_p}{N}(1+sR_zC_z)}. \tag{3.13}$$

From (3.11), the open loop transfer function has one zero and four poles. Two poles are located at the origin. The third and fourth poles (ω_{p3}, ω_{p4}) and the zero (ω_z) are located at frequencies

$$\omega_z = \frac{1}{R_zC_z}, \tag{3.14}$$

$$\omega_{p3} = \frac{C_z+C_p}{R_zC_zC_p}, \tag{3.15}$$

$$\omega_{p4} = \frac{1}{R_4C_4}. \tag{3.16}$$

The phase margin (PM) of a fourth order PLL is

$$PM = \tan^{-1}(\omega_t/\omega_z) - \tan^{-1}(\omega_t/\omega_{p3}) - \tan^{-1}(\omega_t/\omega_{p4}) \quad (3.17)$$

3.4 Phase Noise of Integer-N PLL

All the PLL blocks including VCO, PFD & charge pump, frequency divider and loop filter contribute to the phase noise at the PLL output. Figure 3.6 shows the block diagram of Integer-N PLL with noise sources from every block. All these noise sources and the noise from the input reference source will be modified by noise transfer functions and show up at the PLL output.

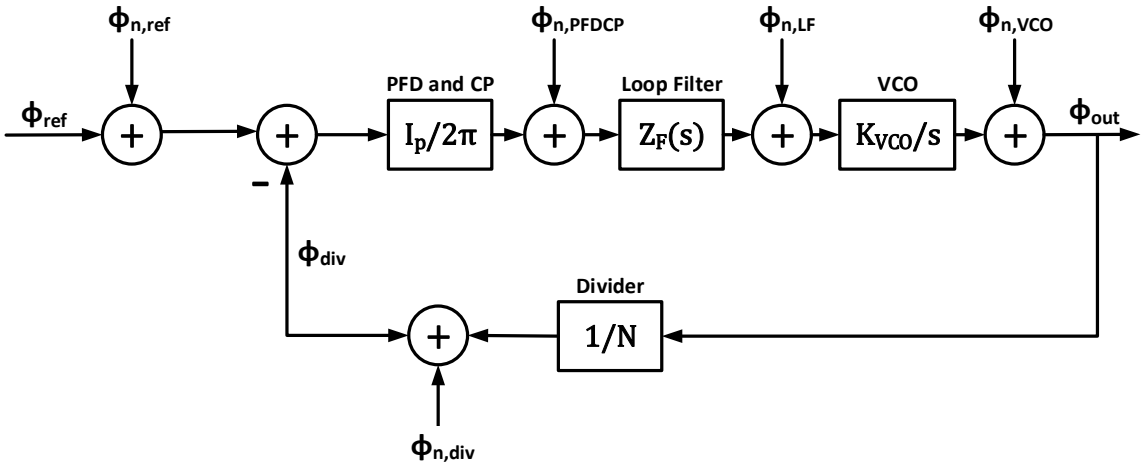


Figure 3.6. Integer-N PLL with noise sources.

3.4.1 Phase Noise from VCO

A VCO can be modeled as a noiseless VCO with an additive noise source $\phi_{n,VCO}$, as shown in Figure 3.7. In order to derive the transfer function between VCO phase noise and PLL phase noise at the output, the reference signal and all other noise sources is set to zero [70]. The simplified system is shown in Figure 3.8. Using a fourth order PLL open loop transfer function in equation (3.11), the noise transfer function from the VCO to PLL output (N_{VCO}) is

$$N_{VCO} = \frac{\Phi_{out}(s)}{\Phi_{n,VCO}(s)} = \frac{1}{1+H_{OL}(s)} \tag{3.18}$$

$$= \frac{2\pi \cdot s^2 N\left(sR_zC_zC_p+C_z+C_p\right)(1+sC_4R_4)}{2\pi \cdot s^2 N\left(sR_zC_zC_p+C_z+C_p\right)(1+sC_4R_4)+K_{VCO}I_p(1+sR_zC_z)} \ . \tag{3.19}$$

From equation (3.19), the noise transfer function has four zeros, and the PLL system works as a high pass filter.

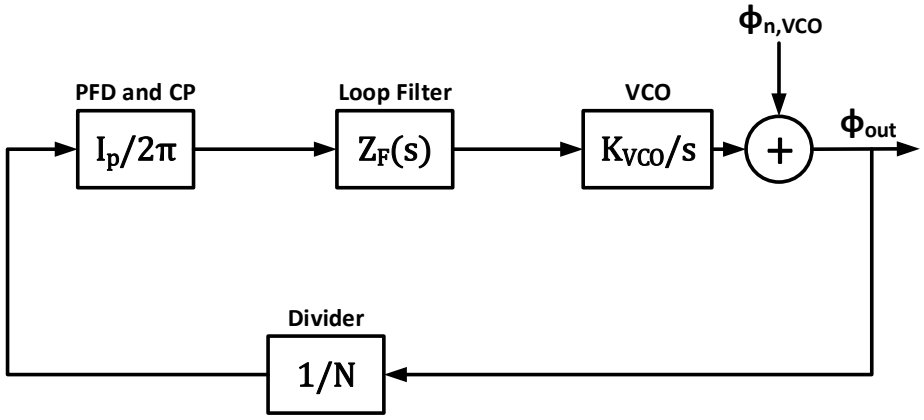


Figure 3.7. Simplified system for computing VCO noise transfer to the PLL output.

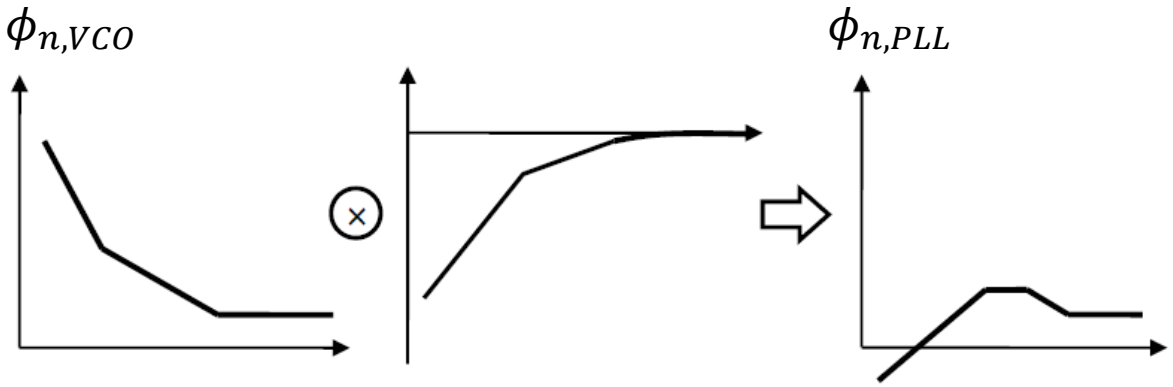


Figure 3.8. VCO noise transfer to the PLL output [70].

For low frequency phase noise components, the slow phase variations of the VCO are detected by the PFD and converted to voltage by the charge pump and loop filter. This voltage is

applied to the VCO control line so that the VCO frequency is changed in the opposite direction. Therefore, the phase variations can be suppressed by the feedback loop. For high frequency phase noise components, the feedback loop cannot follow the phase variations of VCO, and the control voltage does not change with the phase variations [70].

So, the feedback loop is open for the high frequency phase variations, which allows all the phase variations of VCO to be transferred to the PLL output. Figure 3.8 shows the high-pass filtering of phase noise of the VCO by the loop. For example, the low frequency $1/f^3$ noise of the VCO output spectrum can be suppressed by the high pass noise transfer characteristics if the PLL loop bandwidth is chosen to be larger than the VCO $1/f^3$ noise corner frequency.

3.4.2 Phase Noise from Input Reference

In order to derive the noise transfer function from the input reference to the PLL output, once again all other noise sources are set to zero. Figure 3.9 shows the simplified system for computing the noise transfer function.

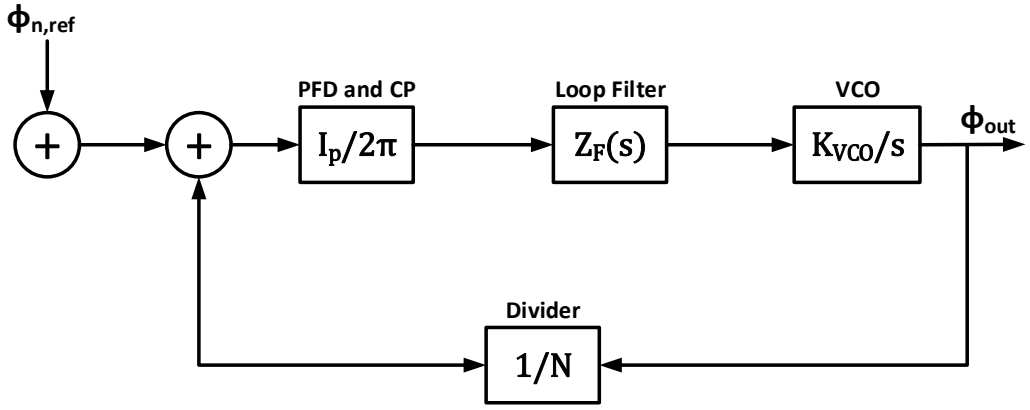


Figure 3.9. Simplified system for computing the reference noise transfer to the PLL output.

Using a fourth order PLL open loop transfer function in equation (3.11), the noise transfer function from input reference to PLL output (N_{Ref}) is

$$N_{Ref} = \frac{\Phi_{\text{out}}(s)}{\Phi_{n,Ref}(s)} = \frac{H_{OL}(s).N}{1+H_{OL}(s)} \tag{3.20}$$

$$= \frac{N.K_{VCO}I_p(1+sR_zC_z)}{2\pi \cdot s^2 N\left(sR_zC_zC_p+C_z+C_p\right)(1+sC_4R_4)+K_{VCO}I_p(1+sR_zC_z)}. \tag{3.21}$$

From equation (3.21), the PLL works as a low pass filter. For slow phase variations at the reference, PLL output can track the phase change and maintain the relation between the input and output. For fast phase variations, PLL fails to track the input phase change, so the high frequency phase variations are suppressed by the loop [70]. In addition, the reference phase noise is amplified by the PLL DC gain N within the loop bandwidth.

3.4.3 Phase Noise from Frequency Divider

The noise transfer function for the frequency divider (N_{Div}), as shown in equation (3.22), is the same as the transfer function for the input reference, except for a minus sign due to the negative feedback.

$$N_{Div} = \frac{\Phi_{\text{out}}(s)}{\Phi_{n,Div}(s)} = \frac{-H_{OL}(s).N}{1+H_{OL}(s)} \tag{3.22}$$

$$= \frac{-N.K_{VCO}I_p(1+sR_zC_z)}{2\pi \cdot s^2 N\left(sR_zC_zC_p+C_z+C_p\right)(1+sC_4R_4)+K_{VCO}I_p(1+sR_zC_z)}. \tag{3.23}$$

The PLL acts as a low pass filter for the phase noise of frequency divider.

3.4.4 Phase Noise from Other Blocks of the PLL

For the phase noise generated by PFD and CP, the loop also operates as a low-pass filter. As shown in Figure 3.6, there is only a gain stage between the reference noise and PFD/CP noise injection points, so the transfer function for the PFD & CP noise to PLL output should have the

same shape as the noise transfer function of reference noise, but with a different magnitude. As for the loop filter noise, which is injected before the integration performed by the VCO, the noise transfer function should be VCO noise transfer function multiplied by the factor (K_{VCO}/s). The loop filter noise is band-pass filtered by the PLL [70].

Usually, in a cascaded chain of PFD, CP and Loop Filter, the noise of Loop Filter is dominant. In the 3rd order loop filter, the noise of resistors, R_z and R_4 is the main source as shown in Figure 3.5. The noise transfer function for the chain of PFD, CP and Loop Filter (N_{LF}) is

$$N_{LF} = \frac{\Phi_{out}(s)}{\Phi_{n,LF}(s)} = \frac{(\frac{K_{VCO}}{s})}{1+H_{OL}(s)} \tag{3.24}$$

$$= \frac{2\pi \cdot \mathrm{s}.N.K_{VCO}.(sR_zC_zC_p+C_z+C_p)(1+sC_4R_4)}{2\pi \cdot s^2 N(sR_zC_zC_p+C_z+C_p)(1+sC_4R_4)+K_{VCO}I_p(1+sR_zC_z)} . \tag{3.25}$$

3.4.5 Phase Noise at the PLL Output due to noise contributions from all the PLL blocks

From the above discussions, the noise from a VCO is high-pass filtered by the loop and the noise from input reference frequency divider, PFD & charge pump is low-pass filtered. Whereas the noise from loop filter is band-pass filtered by the loop.

The overall phase noise of the Integer-N PLL (Φ_{PLL}) due to all the above-mentioned noise contributions from the PLL blocks is

$$\Phi_{PLL} = \Phi_{Vco}|N_{Vco}|^2 + \Phi_{Ref}|N_{ref}|^2 + \Phi_{Div}|N_{Div}|^2 + \Phi_{LF}|N_{LF}|^2 \tag{3.26}$$

The phase noise spectrum of the PLL will have a shape similar to that in Figure 3.10 [70]. The phase noise within the loop bandwidth (ω_t) is referred as the in-band phase noise. In this frequency

range, the phase noise from input reference, frequency divider, PFD & charge pump is dominant since the VCO phase noise is suppressed by the high-pass noise transfer function.

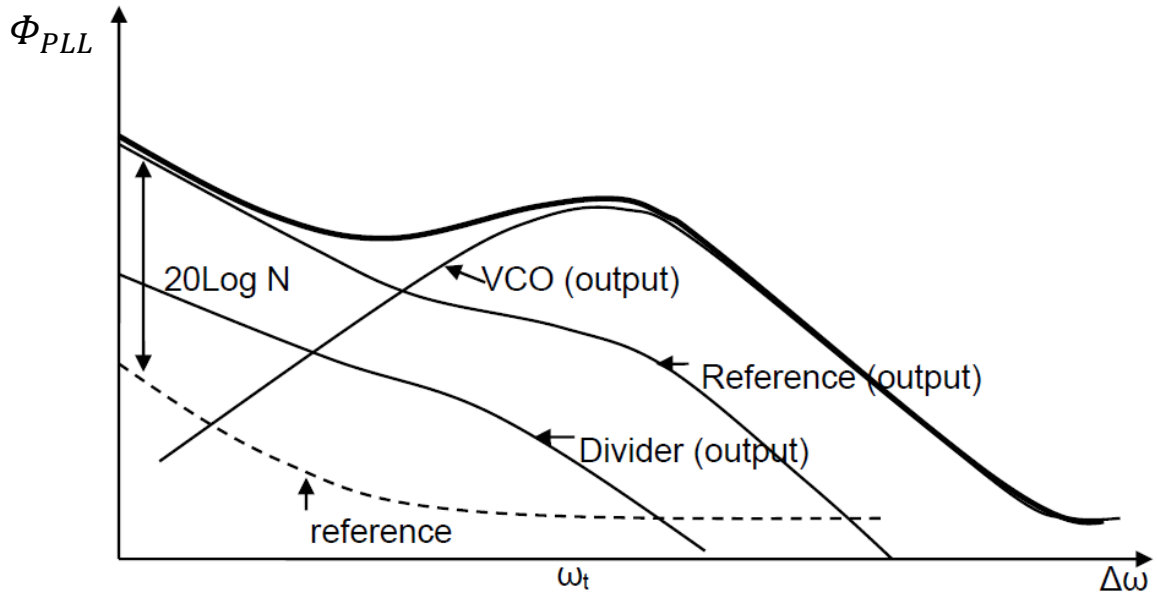


Figure 3.10. Output phase noise of an Integer-N PLL [70].

The in-band phase noise is dominated by the phase noise from the input reference. Figure 3.10 shows the phase noise of the PLL when the phase noise of frequency divider is much lower than the phase noise of input reference. Beyond the loop bandwidth, the phase noise is called out-of-band phase noise. In this frequency range, the phase noise of VCO is dominant because of the high pass noise transfer function from a VCO to PLL output, and the phase noise from other circuit blocks are suppressed by the loop beyond the loop bandwidth. The loop bandwidth of the PLL can be defined as the frequency at which the open loop gain, H_{oL} reduces to 0 dB.

3.5 4-GHz Integer-N PLL design in 65-nm CMOS

3.5.1 Dead-Zone Free Phase Frequency Detector

A Phase Frequency Detector (PFD) detects both the phase and frequency differences of the inputs. The latter is used to aid acquisition when the loop is out of lock. For an Integer-N PLL using a phase-frequency detector, the frequency locking range is limited only by the VCO and frequency divider [70]. Figure 3.11 shows the schematic of the dead-zone free PFD used in the 4-GHz PLL design. Figure 3.12(a) shows the transistor implementations of the two-input NAND gate using NMOS and PMOS transistors in the PFD design.

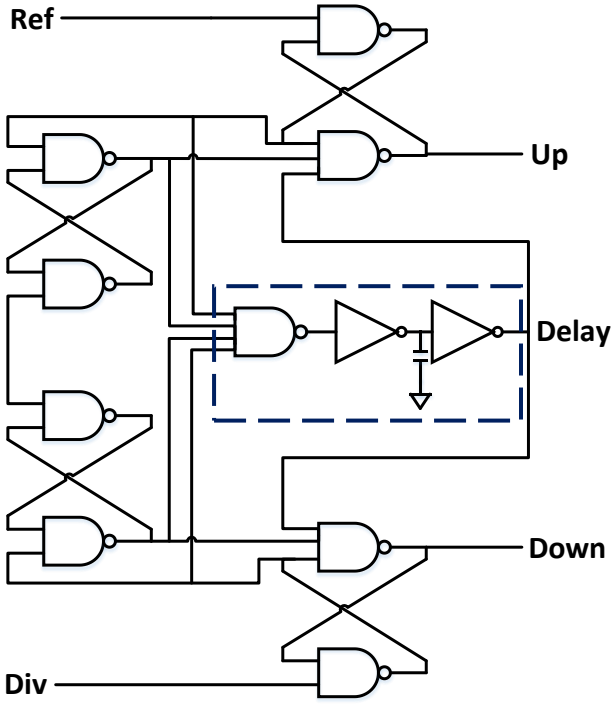
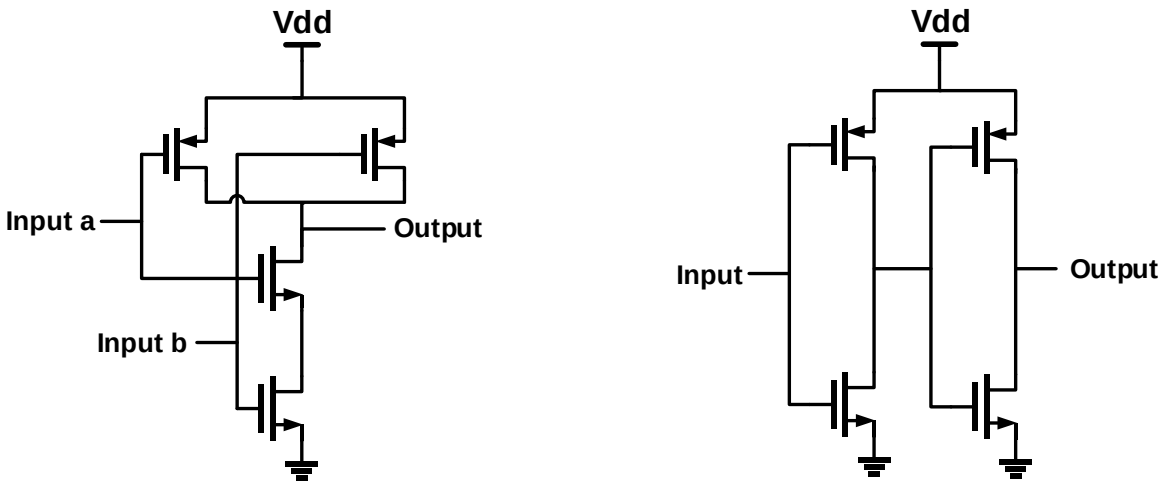


Figure 3.11. Schematic of the dead-zone free phase frequency detector.

The buffer is implemented using a two-stage inverter, as shown in Figure 3.12(b). All the PMOS transistors used in the NAND gates and Buffers have a width and length of 1.3 μm and

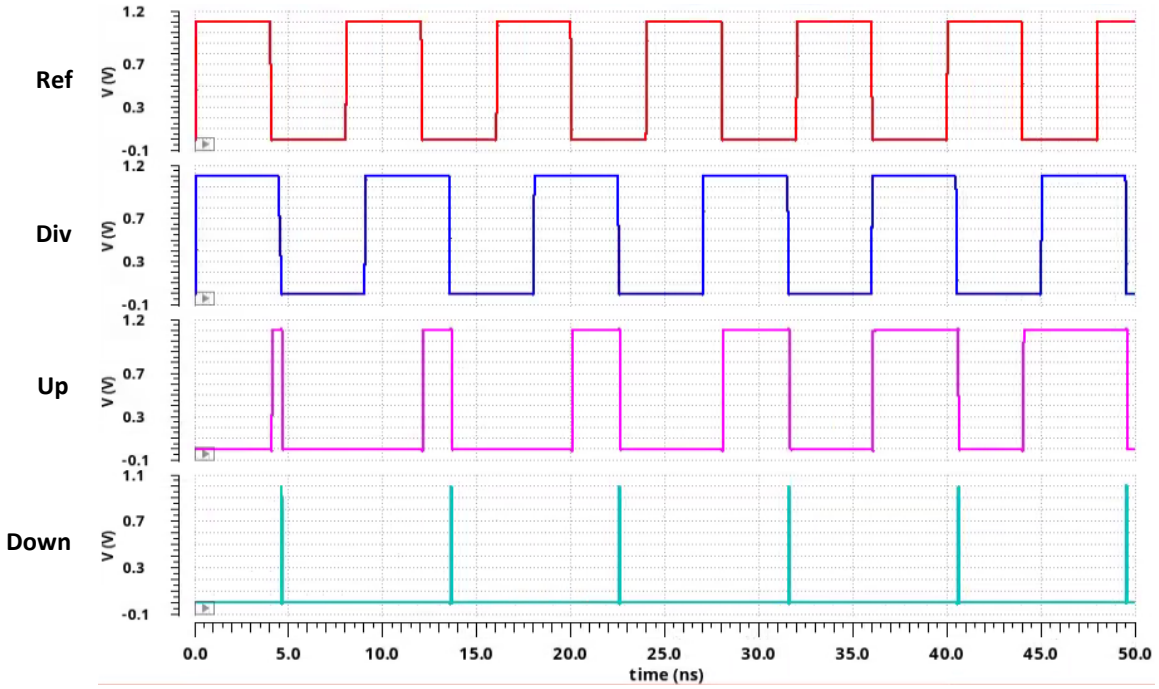
60 nm, respectively, whereas all the NMOS transistors in the PFD have a width and length of 650 nm and 60 nm, respectively.



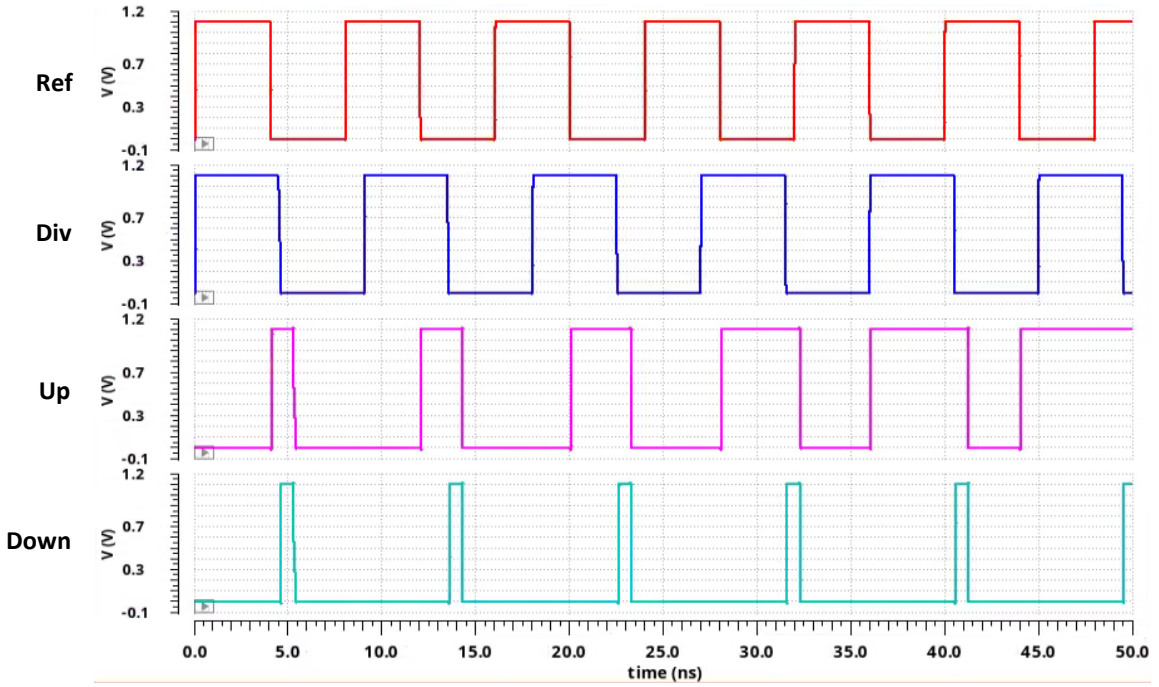
(a) (b)

Figure 3.12. Transistor implementation of (a) two-input NAND gate and (b) Buffer.

A problem of the PFD is the existence of a dead zone around zero-degree phase difference. Since the charge pump needs finite time to change the UP and DN current, it has difficulty responding to small phase differences. A dead zone reduces the loop gain to zero and because of this, the loop can be unlocked for a small period of time, or it can also be falsely locked to a wrong frequency. In order to avoid the dead zone, a delay block implemented by a buffer and a MOS capacitor is added to the PFD reset line. It gives a fixed minimum width to the PFD output pulses so that the dead zone can be avoided. Figures 3.13(a) and (b) show the transient voltage simulations of the PFD without and with the delay cell, respectively.



(a)



(b)

Figure 3.13. Transient waveforms of PFD (a) without a delay cell, and (b) with a delay cell.

From the Figure 3.13(a), it can be observed that if ‘Div’ signal is leading ‘Ref’ signal, then the phase difference between these two signals is detected by the ‘Up’ signal, so the outputs ‘Up’ = 1 and ‘Down’ = 0 during this time period. Figure 3.13(b) shows the voltages during the same conditions when a fixed minimum width is given to the PFD output pulses for avoiding the dead zone. It can be observed from the pulse width of ‘Down’ signal that the simulated pulse width for avoiding the dead zone is 0.78 ns which is ~10% of the reference period of 8 ns.

3.5.2 Charge Pump with Dual Op-amps

The charge pump (CP) for the PLL needs to provide matched up (UP) and down (DN) currents for most of the CP output voltage range. The matching of UP and DN currents is important for the charge pump design. The mismatch in the UP and DN currents generates ripples on VCO control line, which results in frequency spurs in the PLL output spectrum. The charge pump architecture shown in Figure 3.14 employs dual operation amplifiers (Op-amps) where both amplifiers utilize a high-swing folded cascode topology [71, 72]. The first amplifier, OA1 forms the feedback loop where the gate voltage of PMOS in the up current path is tracked to keep the current the same as that of NMOS, whereas the second amplifier, OA2 acts as a unity gain amplifier to track the change of VCO control node (CP Out) to the dummy node.

In addition, to reduce the charge pump current mismatch caused by the threshold voltage variations of transistors, the switch transistors (Mn1, Mn2, Mp1, Mp2) and the current source transistors (M1, P1) in the charge pump have large transistor sizes and are also designed to operate at relatively large overdrive voltage to reduce the current mismatch caused by the threshold voltage variations [70]. The charge pump current is externally controlled to change the loop bandwidth of

the PLL. Figure 3.15 shows the simulated mismatch between UP and DN currents over the charge pump output voltage range of (0.2V – 1.1V). The highest mismatch is 4.75% when the charge pump output voltage is 1.1V, whereas good matching of less than 1% is obtained for the output voltage range of (0.4V – 1V). Figure 3.16 shows the layout of the PFD and Charge Pump chain used in the 4-GHz PLL design in 65-nm CMOS.

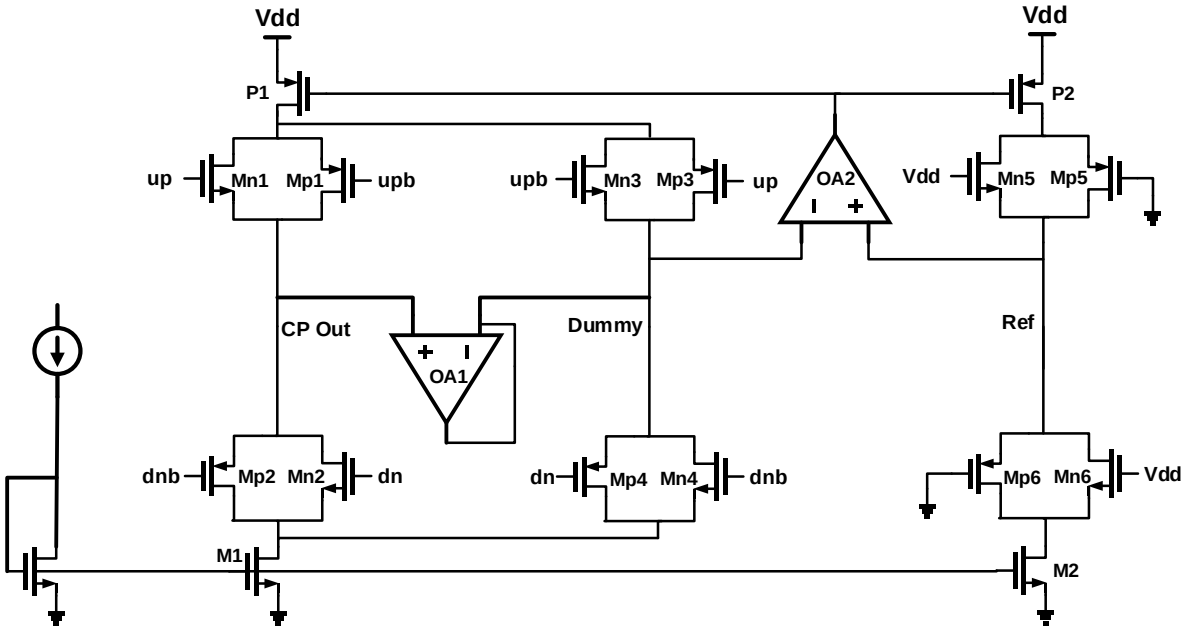


Figure 3.14. Schematic of the charge pump design with dual Op-amps [82].

3.5.3 Third Order Loop Filter

Figure 3.17 shows a schematic of the third order passive loop filter used in the 4-GHz PLL design. The component values are also shown in the schematic. The loop filter integrates, and low-pass filters the error current (I_p) generated by the charge pump, thereby generating a control voltage (V_{ctrl}) for the VCO as shown in Figure 3.18. The capacitors in the loop filter are implemented with a thick-gate 2.5-V MOS capacitors to reduce the leakage current.

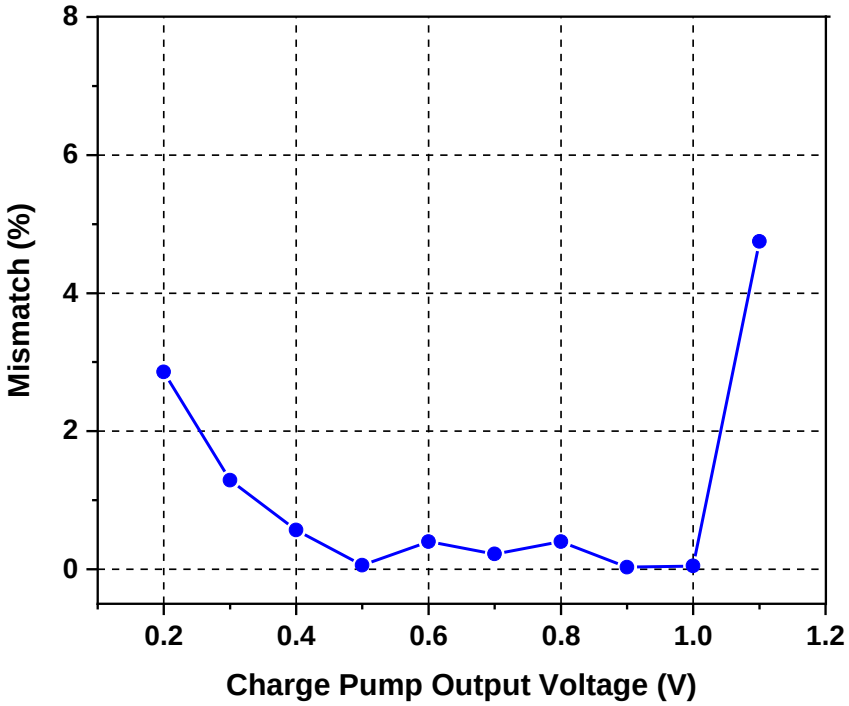


Figure 3.15. Simulation of mismatch between UP and DN currents over the charge pump output voltage range.

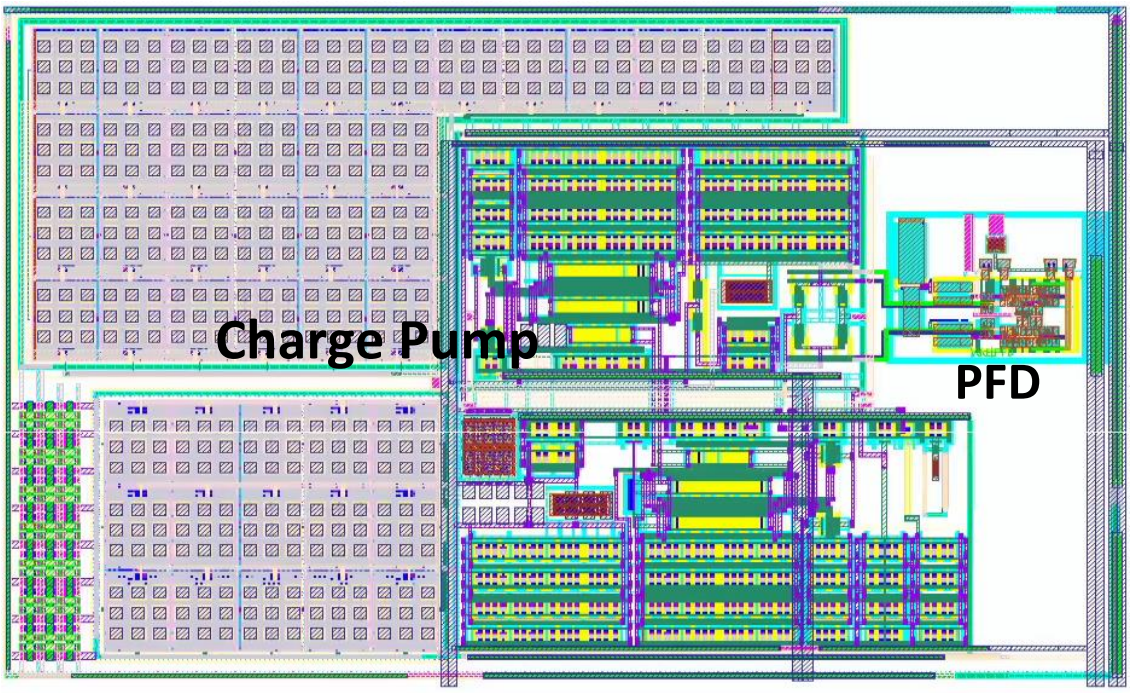


Figure 3.16. Layout of PFD and Charge Pump chain used in the design of 4-GHz PLL.

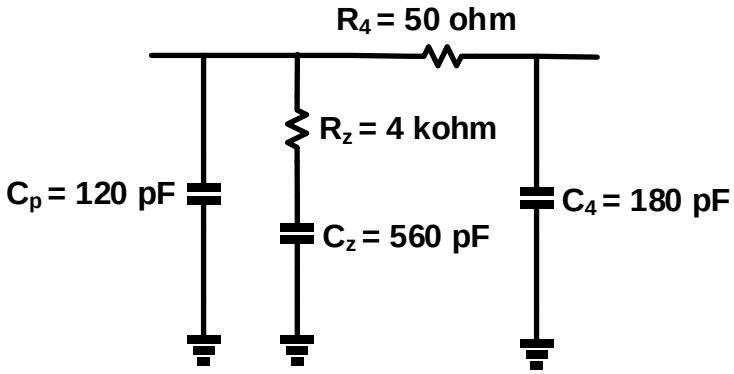


Figure 3.17. Schematic of loop filter used in the 4-GHz PLL design.

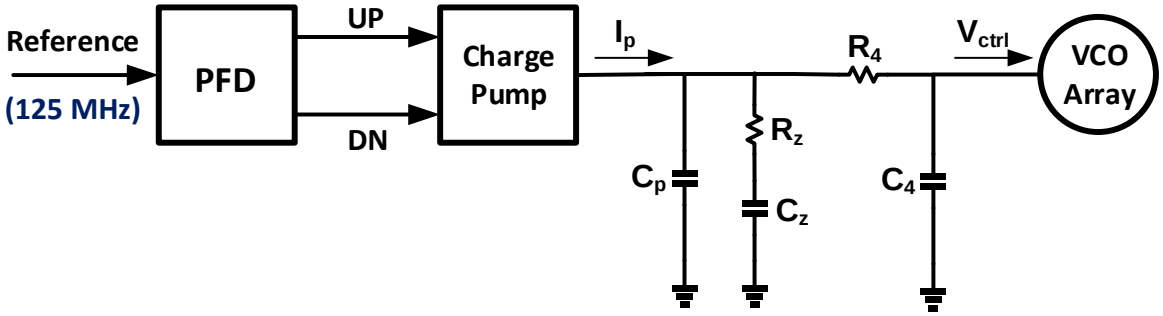


Figure 3.18. Block diagram of a chain of PFD, Charge Pump, loop filter and VCO.

A capacitor, C_z integrates the error current and generates the error voltage or control voltage proportional to the error current. Having only C_z in the loop filter makes the loop unstable since the phase margin of the loop in this case is zero degree. Therefore, resistor, R_z is added in the loop filter which adds a zero to the transfer function for providing a sufficient phase margin and stability for the loop. To maintain the loop stability, a phase margin of 45º or more is preferred. A Capacitor, C_p provides a low impedance path to the ground for the ripples in the control voltage which is caused due to the switching action in the PFD and charge pump, and also due to the non-idealities such as skew in PFD and charge pump current mismatch. C_p adds an additional pole to the transfer function which degrades the phase margin.

An additional RC filter formed by R_4 and C_4 is also included in the loop filter to further attenuate the ripples and spurs on the control voltage node. The fourth pole formed by R_4 and C_4 can be placed at a desired frequency higher than the third pole, without affecting the other three poles and zero. The frequency of the fourth pole must be lower than the reference frequency so to properly attenuate the spurs [70]. The drawback of the higher order loop is the degradation of stability. The fourth pole must be typically 4 to 5 times higher than the loop bandwidth to make the phase margin degradation small [75].

The phase margin (PM) of a fourth order PLL is

$$PM = \tan^{-1}(\omega_t/\omega_z) - \tan^{-1}(\omega_t/\omega_{p3}) - \tan^{-1}(\omega_t/\omega_{p4}), \quad (3.27)$$

where,

$$\omega_z = \frac{1}{R_z C_z}, \quad (3.28)$$

$$\omega_{p3} = \frac{C_z + C_p}{R_z C_z C_p}, \quad (3.29)$$

$$\omega_{p4} = \frac{1}{R_4 C_4}. \quad (3.30)$$

3.5.4 Frequency Divide-by-32

A frequency divider is one of the critical blocks in a synthesizer because it is one of the two fblocks which determine the maximum operating frequency of a Type-II PLL, the other factor being the maximum output frequency. A key factor which needs to be considered in the design of the frequency divider is its proper operation at the maximum VCO output frequency.

For the design of frequency divide-by-32 in the 4-GHz PLL, mainly two topologies were considered, and their performance was compared. They are (i) Current mode logic (CML) divider, and (ii) CMOS Dynamic divider.

(i) Current Mode Logic Divider

Figure 3.19 shows the block diagram of an asynchronous divide-by-32, which is formed by a 5-stage cascaded chain of CML frequency divide by two. The divider is based on the master–slave D flip-flop in which the inverted slave outputs are connected to the master inputs [73]. Figure 3.20 shows the transistor implementation of a CML frequency divide-by-two circuit, implemented in a master-slave configuration. Both the master and slave stages consist of an evaluate stage implemented by a differential pair of a width and a length of 400 nm and 60 nm, respectively, and a latch stage or regenerative stage implemented by a cross-coupling transistor pair of a width and a length of 320 nm and 60 nm, respectively.

The loads of the master and slave stages are implemented by PMOS load transistors acting as resistors. The current sources in conventional CML latches are omitted [74] for low-voltage operation. The cross-coupled pair transistors are often made smaller than the input differential pair to increase the maximum operating frequency [70]. In this design, the optimum cross-coupled pair transistor to differential pair transistor size ratio is chosen to be 4/5.

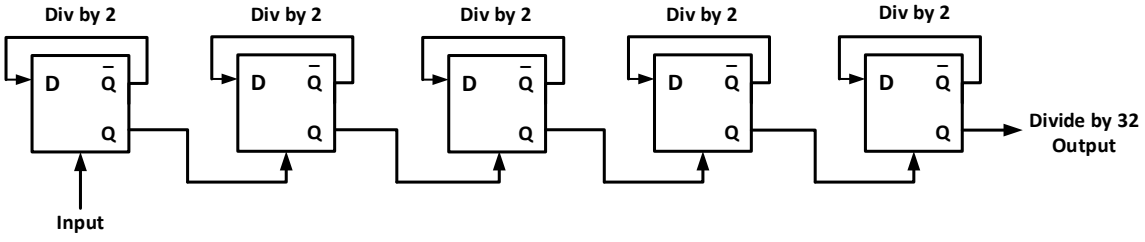


Figure 3.19. Block diagram of the asynchronous CML divide-by-32.

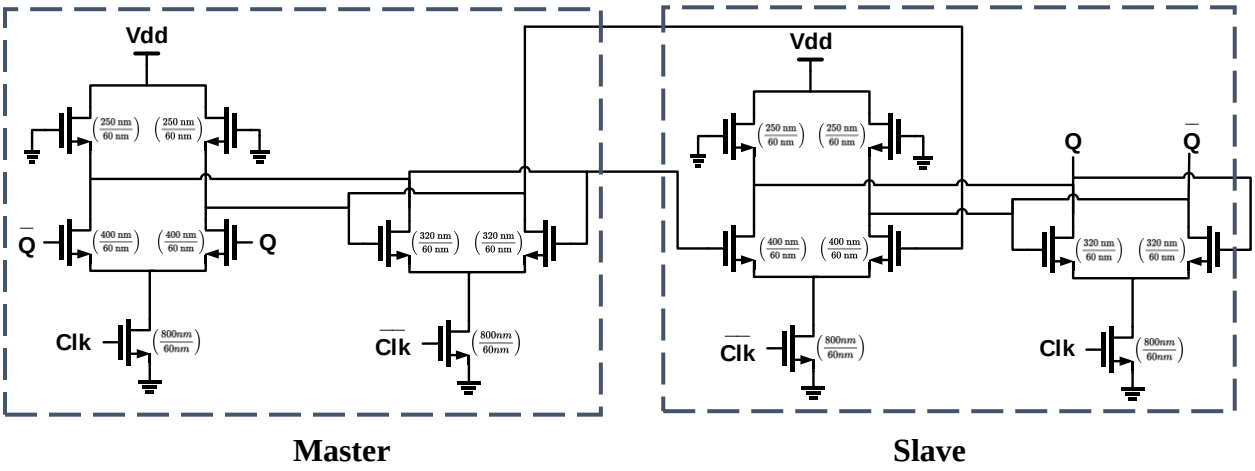


Figure 3.20. Schematic of the CML divide-by-2.

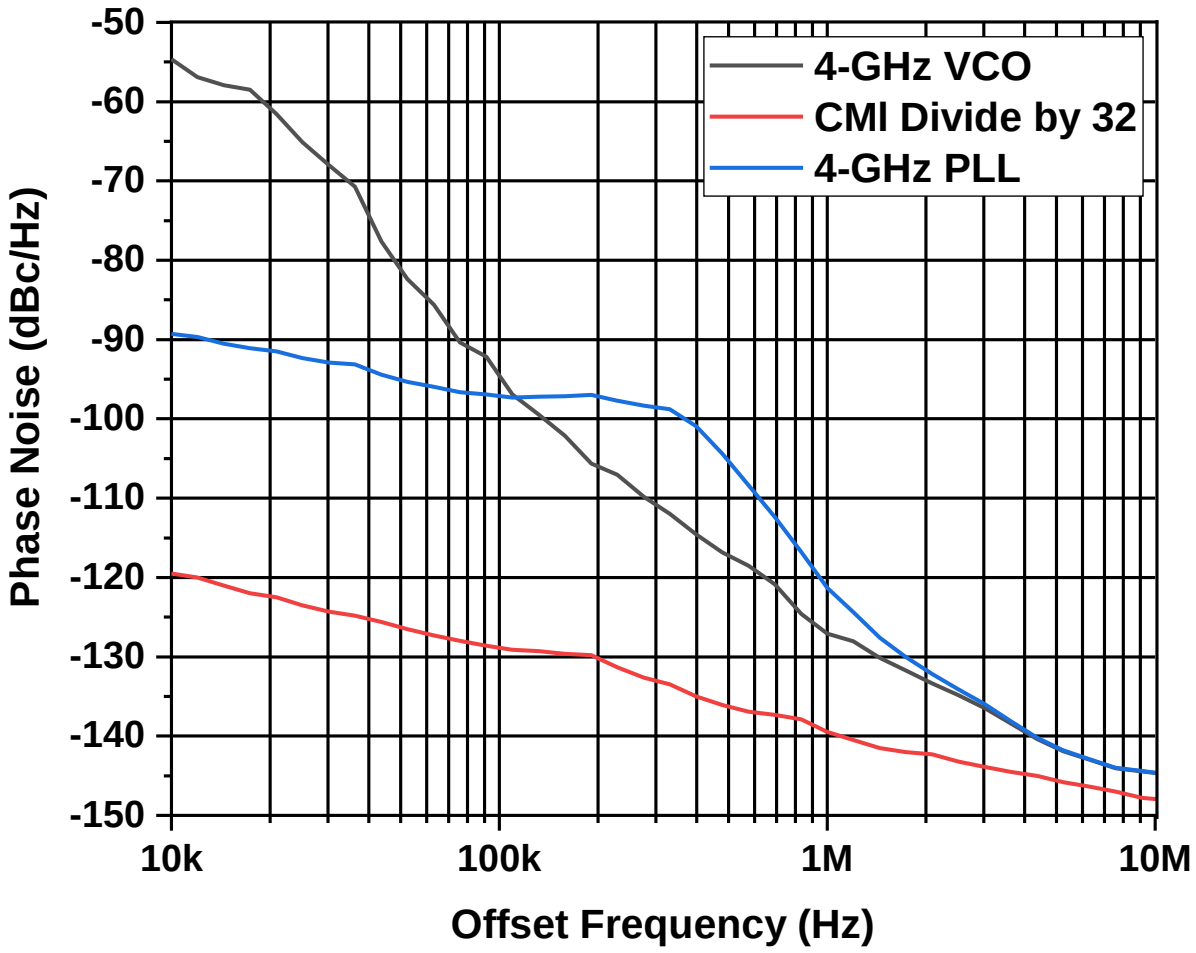


Figure 3.21. 4-GHz PLL phase noise with noise contributions from VCO and CML divide-by-32.

Figure 3.21 shows the simulated phase noise of CML divide-by-32 and the PLL phase noise when the contributions of measured VCO phase noise and simulated phase noise of CML divide-by-32 are included. It can be observed from the figure that for a measured phase noise of 4-GHz VCO array which is -127 dBc/Hz at 1-MHz offset, the PLL phase noise is -121 dBc/Hz at 1-MHz offset from 4-GHz, which is 6 dB higher. This is due to the out-of-band noise contribution of CML divide by 32. The phase noise of the CML divider is -140 dBc/Hz at 1-MHz offset from the 125-MHz divided output.

Since the divider phase noise is low-pass filtered by the loop as discussed in Section 3.4, the in-band phase noise of the PLL is dominated by the noise of divider and the out-of-band phase noise is dominated by the noise of VCO. The in-band phase noise gets higher by the factor $20\log(32) = 30$ dB compared to the phase noise of divider, which is due to the frequency multiplication. For example, if the phase noise of divider is -120 dBc/Hz at 10-kHz offset from 125 MHz, then the PLL phase noise is -90 dBc/Hz at 10-kHz offset from a 4-GHz carrier.

The out-of-band phase noise is also affected due to the phase noise of the divider, since the loop filter cannot completely filter out the noise of divider. Due to this, the phase noise from 200-kHz to 2-MHz offsets is limited by the phase noise of CML divide-by-32. In addition, the in-band phase noise of the PLL is significantly affected by the phase noise of divider when its phase noise is higher than the phase noise of input reference, which limits the overall jitter performance of the Integer-N PLL.

(ii) CMOS Dynamic Divider

Though the CML divider topology is popular and quite preferred for low power and high frequency operations, its high phase noise is a limitation for use in low phase noise and low jitter

synthesizers as discussed in the previous section. The reasons for the high phase noise of CML dividers are mainly due to a small internal signal amplitude, a long transistor turn-on time that increases the conversion gain for both AM and PM noise present in the divider [76]. On the other hand, a dynamic divider with square-wave internal signals can achieve much lower phase noise.

Figure 3.22 shows the design of updated frequency divide-by-32. The first divide-by-2 stage is still kept a CML divider mainly for handling the high frequency input from VCO, but the transistor sizes are increased compared to the previous design in Figure 3.20, so as to lower its phase noise. Figure 3.23 shows the updated design of the first stage CML divide-by-2. In addition, the PMOS load transistors in Figure 3.20 are replaced with resistors to lower the phase noise.

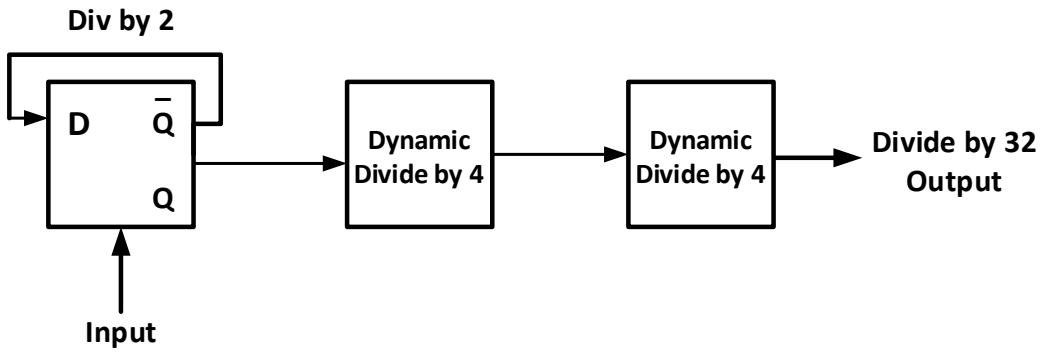


Figure 3.22. Block diagram of the updated divide-by-32 design.

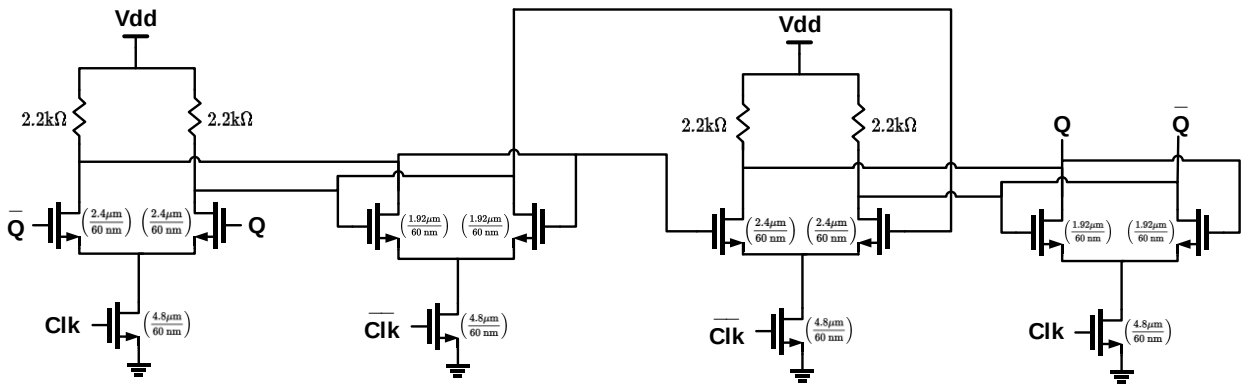


Figure 3.23. Updated design of the CML divide-by-2 circuit.

The divide-by-16 stage after CML divide-by-2 is formed by cascading two stages of dynamic divide-by-4 stages. The dynamic divide-by-4 is formed by cascading two dynamic D flip-flops with inverted D_2 output feeding back to D_1 input [76] as shown in Figure 3.24.

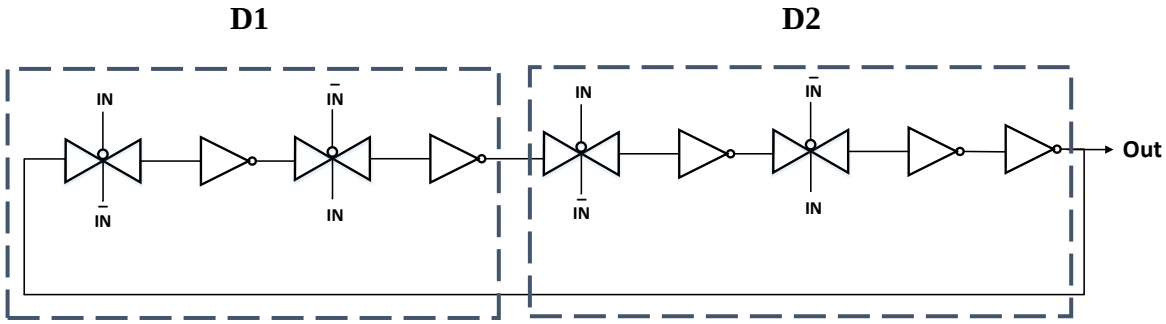


Figure 3.24. Simplified circuit schematic of the dynamic divide-by-4.

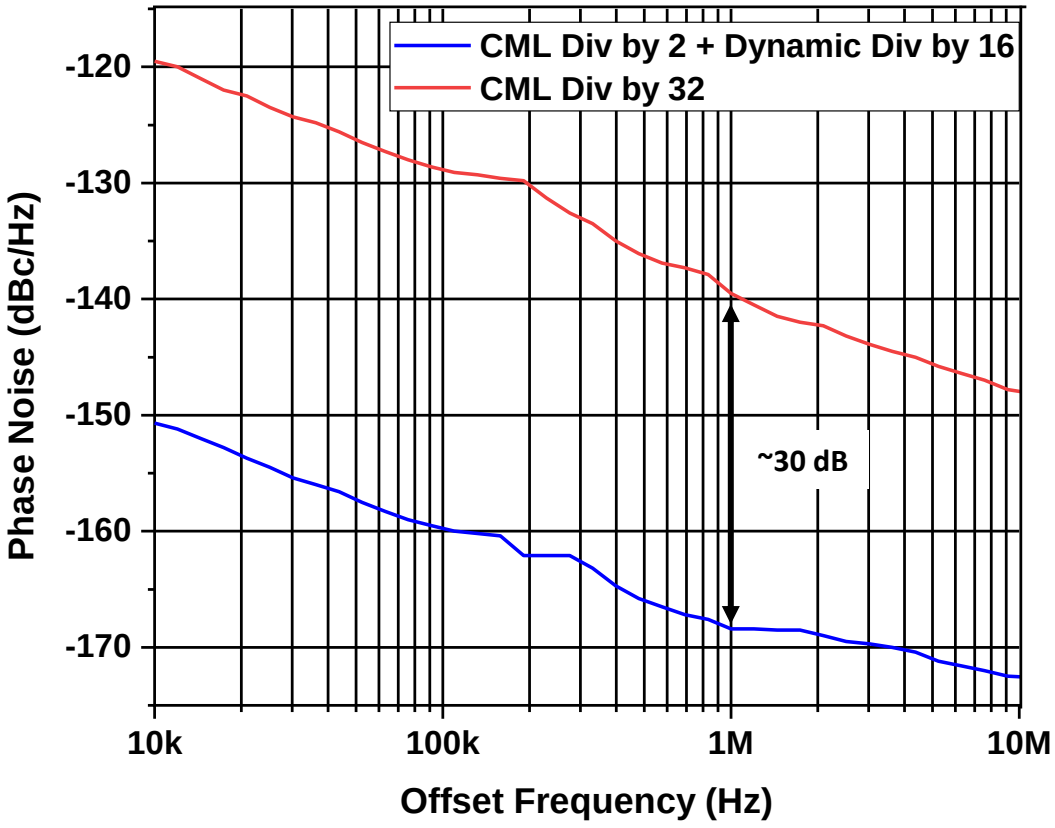


Figure 3.25. Simulated phase noise of divide-by-32 with CML div-by-2 as the first stage, followed by a dynamic div-by-16 circuit.

The dynamic flip-flops are formed with pass-gates and inverters. Since the internal waveforms are square and have a short rise and fall time in the dynamic dividers, so they contribute less noise and are less sensitive to AM and PM noise. Figure 3.25 shows the simulated phase noise of the updated divide-by-32 with CML divide-by-2 as the first stage, followed by the dynamic divide-by-16 circuit. From the figure, it can be observed that compared to the design using a CML divide-by-32 circuit, the updated design has a phase noise which is ~30 dB lower at 10-kHz to 10-MHz offsets from the 125-MHz output frequency.

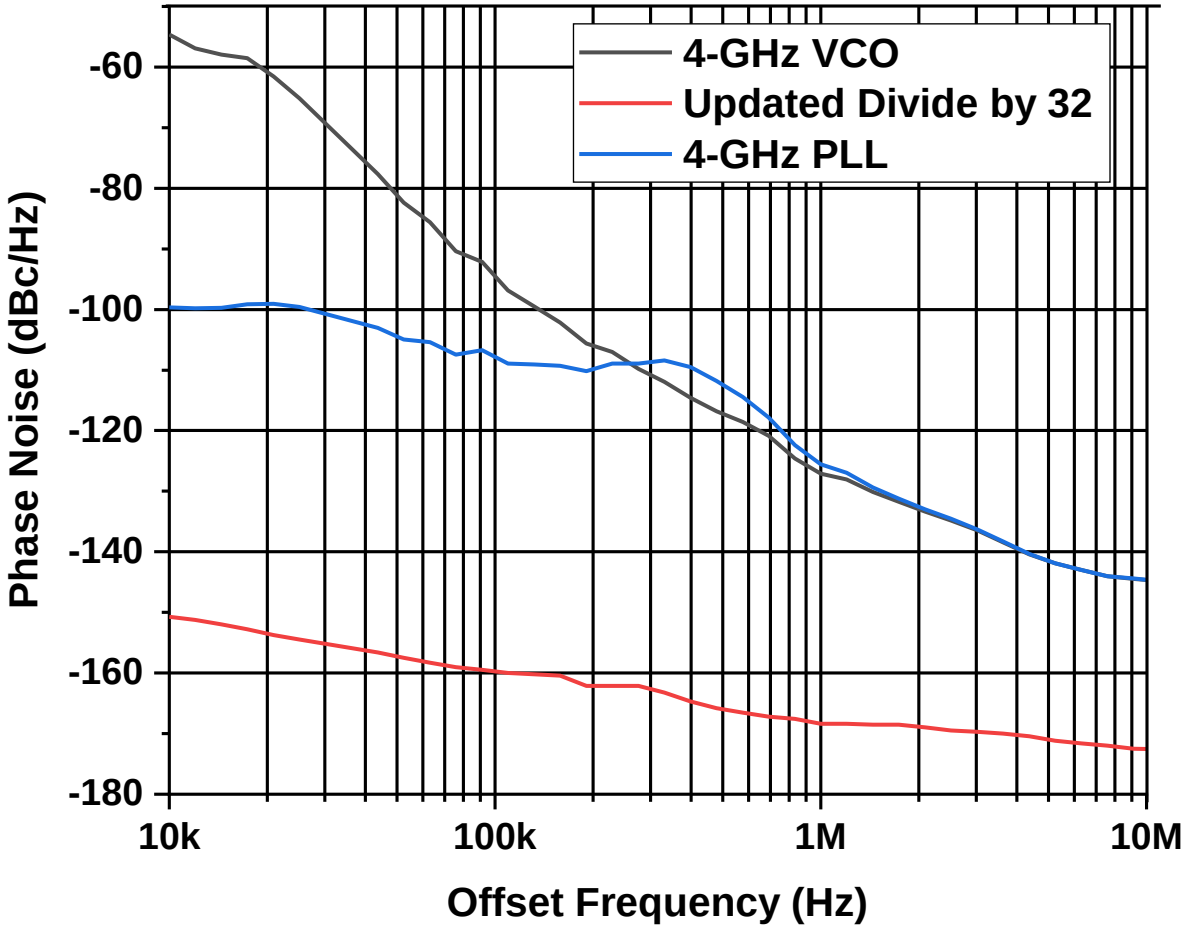


Figure 3.26. 4-GHz PLL phase noise with noise contributions from the VCO and updated divide-by-32 circuit.

Figure 3.26 shows the PLL phase noise when the contributions of measured VCO phase noise and simulated phase noise of updated divide-by-32 are included. It can be observed from the figure that for the measured phase noise of 4-GHz VCO which is -127 dBc/Hz at 1-MHz offset, the PLL phase noise is -125.5 dBc/Hz at 1-MHz offset from 4-GHz, which is only 1.5 dB higher. In addition, the in-band phase noise of PLL is also lowered compared to that in Figure 3.21 when the CML divide-by-32 circuit was used. For example, the PLL phase noise at 10-kHz offset from a 4-GHz carrier is -100 dBc/Hz, which is 10 dB lower than that in Figure 3.21. Figure 3.27 shows the layout of the updated divide-by-32 circuit design.

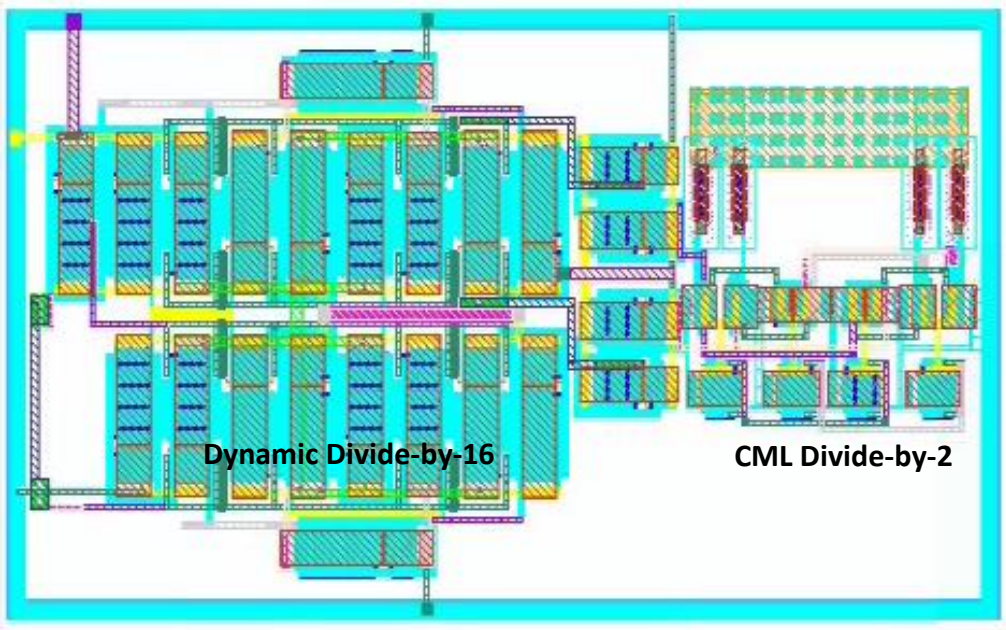


Figure 3.27. Layout of the divide-by-32 with CML divide-by-2 circuit as the first stage and followed by a dynamic divide-by-16 circuit.

3.5.5 4-GHz PLL Schematic

A schematic of 4-GHz PLL incorporating a VCO employing an array of cross-coupled pairs and intelligent post-fabrication selection in 65-nm CMOS is shown in Figure 3.28. Buffers

are included in the design for the 4-GHz VCO/PLL output to drive a 50-ohm load, for divide-by-32 output, and between the 125-MHz input reference and PFD. A level shifter between the VCO and the divide-by-2 provides right bias voltages for the ‘clk+’ and ‘clk-’ transistors by shifting down the 1.1V output common-mode voltage of VCO to 0.6V.

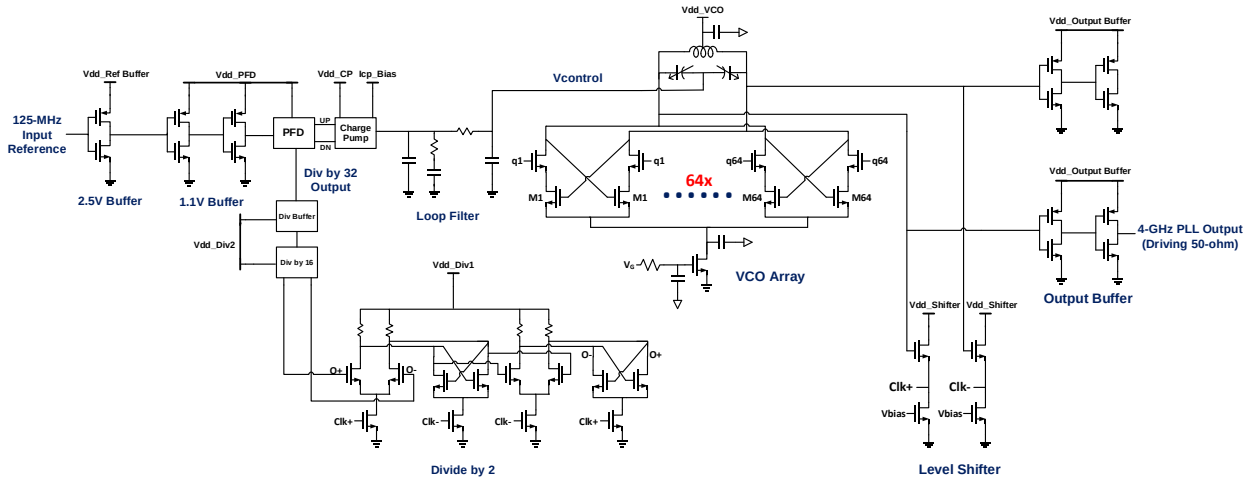


Figure 3.28. Schematic of 4-GHz PLL incorporating a VCO employing an array of cross-coupled pairs and intelligent post-fabrication selection in 65-nm CMOS.

3.6 4-GHz PLL Simulations

3.6.1 Phase Margin and Stability

The phase margin and stability of the 4-GHz PLL is analyzed using a bode plot in Figure 3.29. The open loop transfer function (H_{oL}) of the fourth order 4-GHz PLL (equation 3.31) is used for calculating the phase margin. The phase margin (PM) from the plot is 45^o. Higher phase margin of 60^o can be obtained by modifying the loop filter, but at the cost of higher phase noise, higher spur levels and lower phase tracking during locking. For example, decreasing the size of C_p and C_4 in the loop filter leads to a higher phase margin, but at the same time increases the noise

contribution from the loop filter and increases the spur levels caused due to non-idealities in the PFD and Charge Pump.

$$H_{OL}(s) = \frac{I_p}{2\pi} \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \cdot \frac{1+sR_zC_z}{s\left(sR_zC_zC_p+C_z+C_p\right)} \frac{1}{1+sC_4R_4}. \tag{3.31}$$

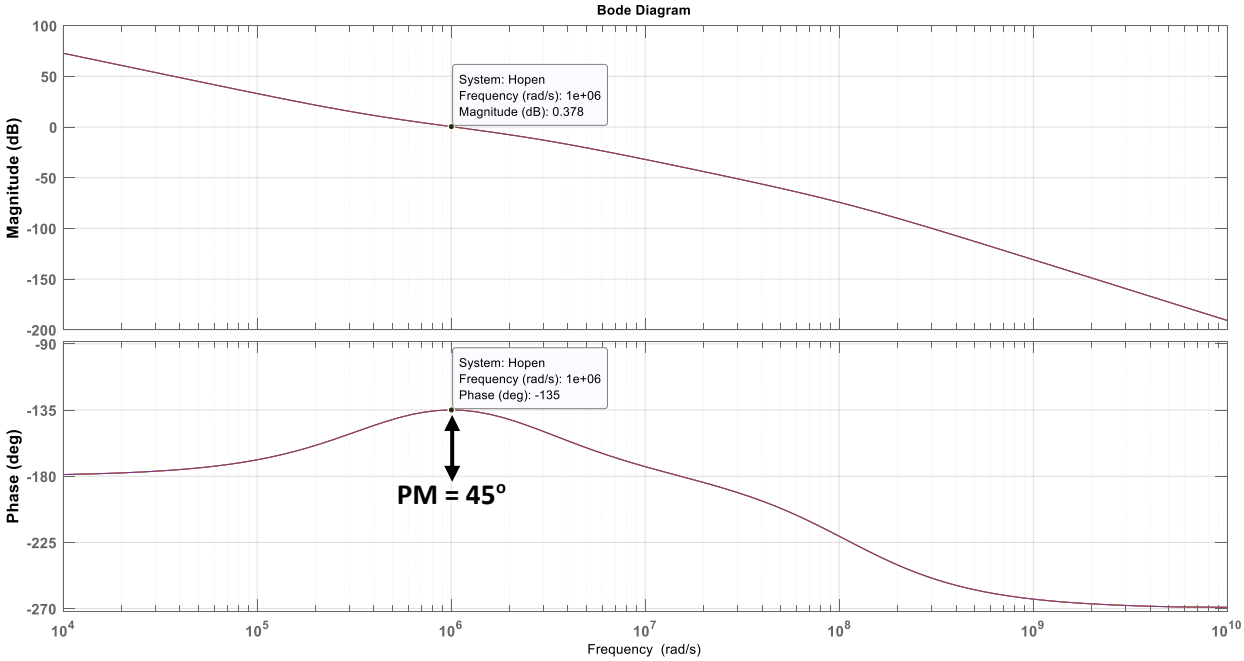


Figure 3.29. Bode plot of the 4-GHz PLL for calculating phase margin.

3.6.2 VCO phase noise transfer to PLL output

Since the measured VCO phase noise is low, for example -127 dBc/Hz at 1-MHz offset, the PLL design needs to ensure the loop does not increase the out-of-band phase noise of PLL which is dominated by the VCO. For this reason, the loop bandwidth must be low enough such that most of the low phase noise of VCO transfers to the output of PLL. Due to this, the loop bandwidth is set around 100-kHz for the 4-GHz PLL design. Figure 3.30 shows the phase noise transfer of 4-GHz VCO array to the output of 4-GHz PLL. It can be seen there is a ~3 dB

degradation in the PLL phase noise compared to the VCO phase noise at offset frequencies from 100-kHz to 200-kHz which are around the loop bandwidth, and there is less than 1 dB degradation from 300-kHz offset up to a far offset at 10-MHz.

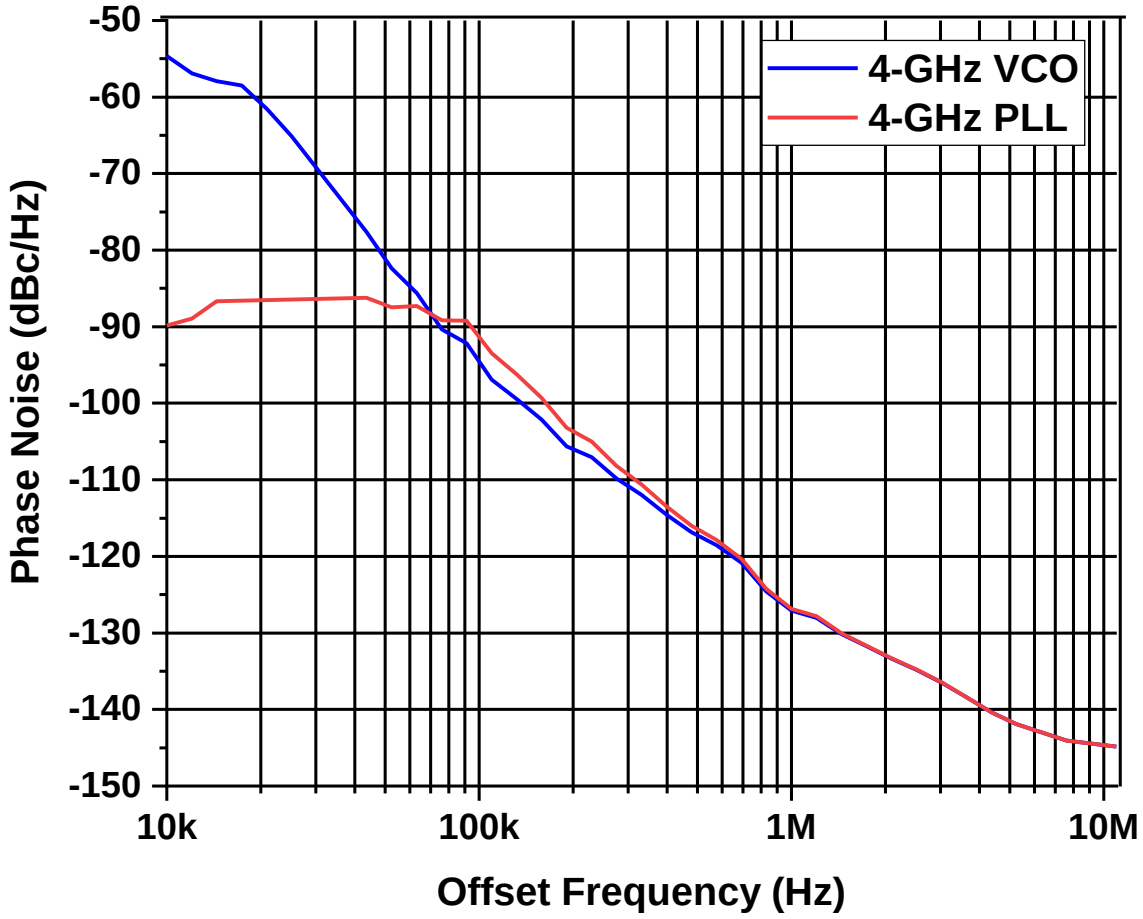


Figure 3.30. Phase noise transfer of 4-GHz VCO to the output of 4-GHz PLL.

3.6.3 PLL phase noise with noise contributions from VCO and Input reference

Figure 3.31 shows the simulated phase noise of 4-GHz PLL when the noise contributions from both the 4-GHz VCO and 125-MHz input reference are included in the system transfer function for phase noise transfer to the output. The 125-MHz input reference is generated by a Rohde & Schwarz SMB100A Signal Generator. From the figure, there is ~2-dB degradation of the

PLL phase noise compared to the VCO phase noise at offset frequencies from 100 kHz to 200 kHz which are around the loop bandwidth, and there is less than 1-dB degradation from 300-kHz offset up to a far offset at 10 MHz.

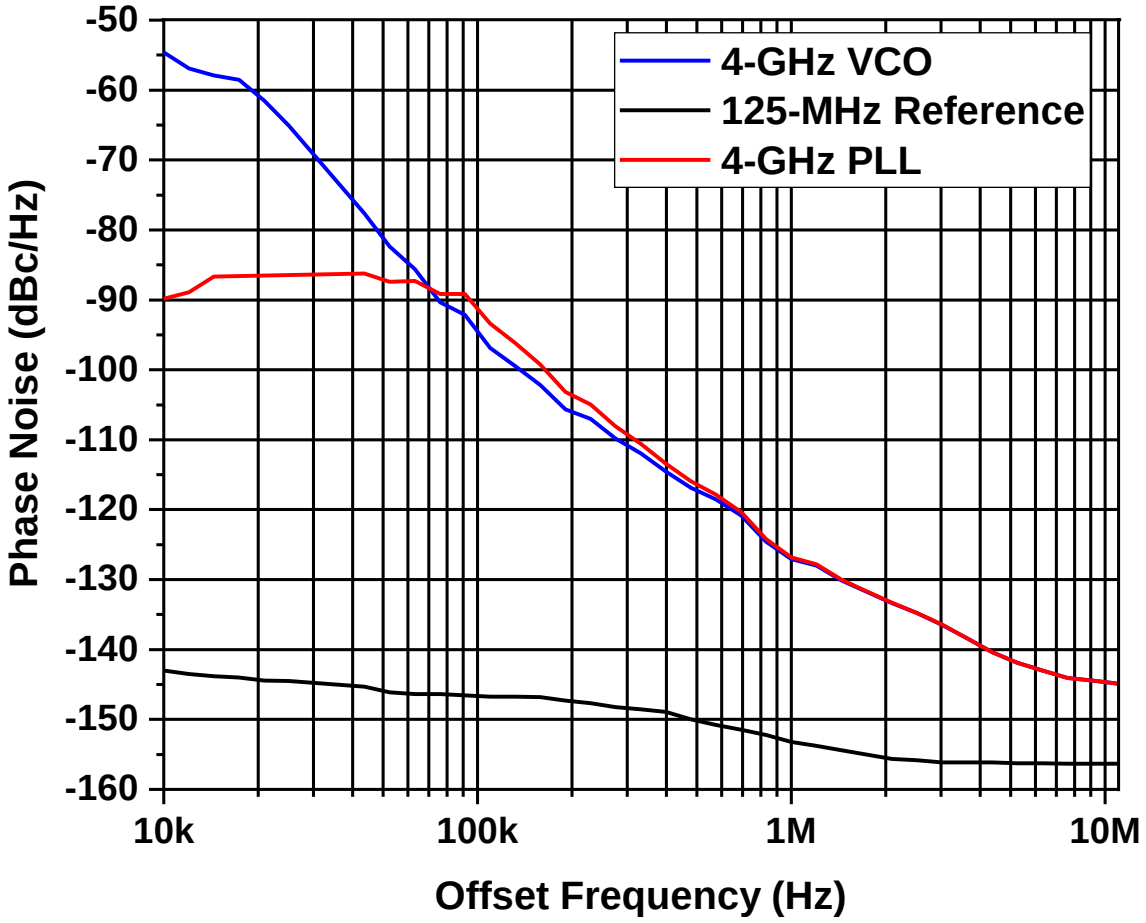


Figure 3.31. Simulated phase noise of 4-GHz PLL with the noise contributions from the 4-GHz VCO and 125-MHz Input Reference.

3.6.4 Total simulated phase noise of the 4-GHz PLL

Figure 3.32 shows the simulated phase noise of 4-GHz PLL when the noise contributions from VCO, input reference, divide-by-32, PFD, charge pump, and loop filter are included in the system transfer function for computing the phase noise at the PLL output. From the figure, it can

be seen there is a ~2-dB degradation in the PLL phase noise compared to the VCO phase noise at offset frequencies from 100 kHz to 300 kHz which are around the loop bandwidth, and there is less than 1-dB degradation from 400-kHz offset up to a far offset at 10-MHz. The simulated phase noise of the 4-GHz PLL is -93 dBc/Hz at 100-kHz offset, -118 dBc/Hz at 600-kHz offset, -126.7 dBc/Hz at 1-MHz offset, and -145 dBc/Hz at 10-MHz offset.

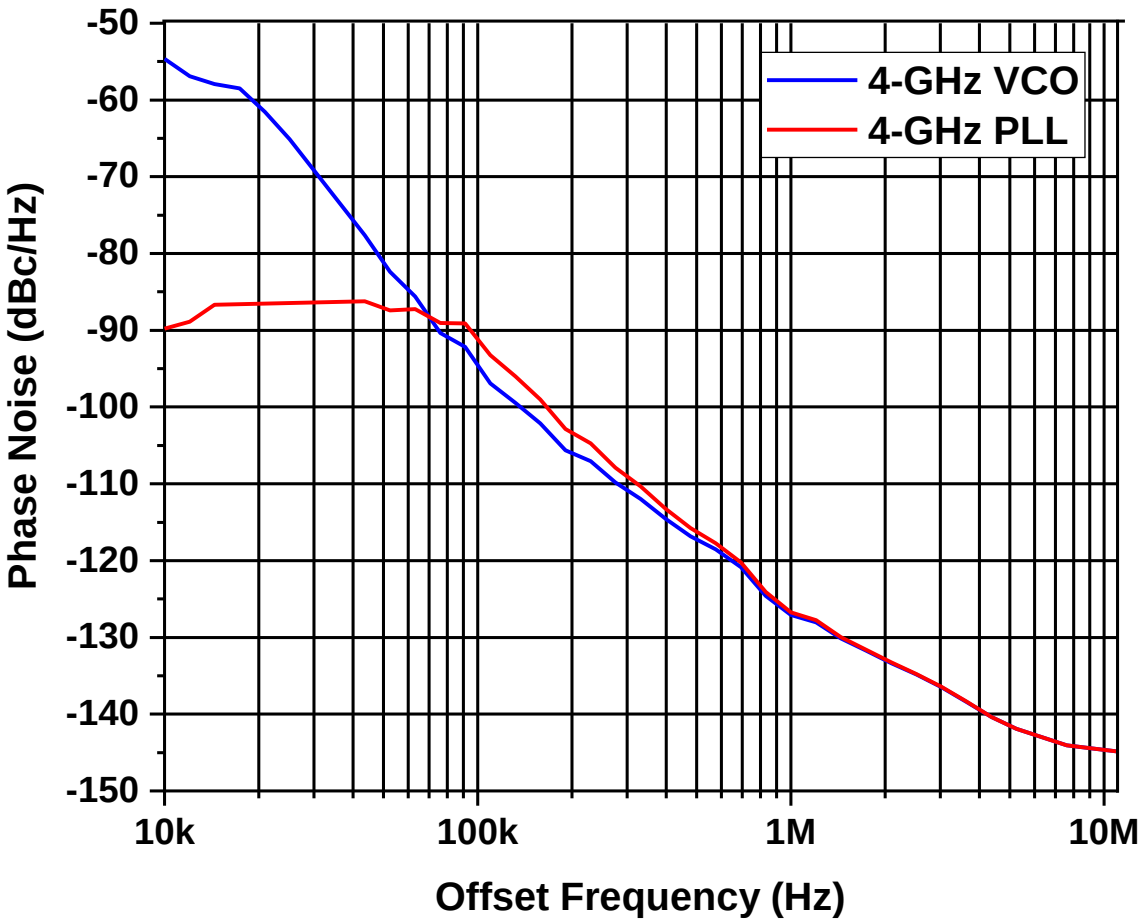
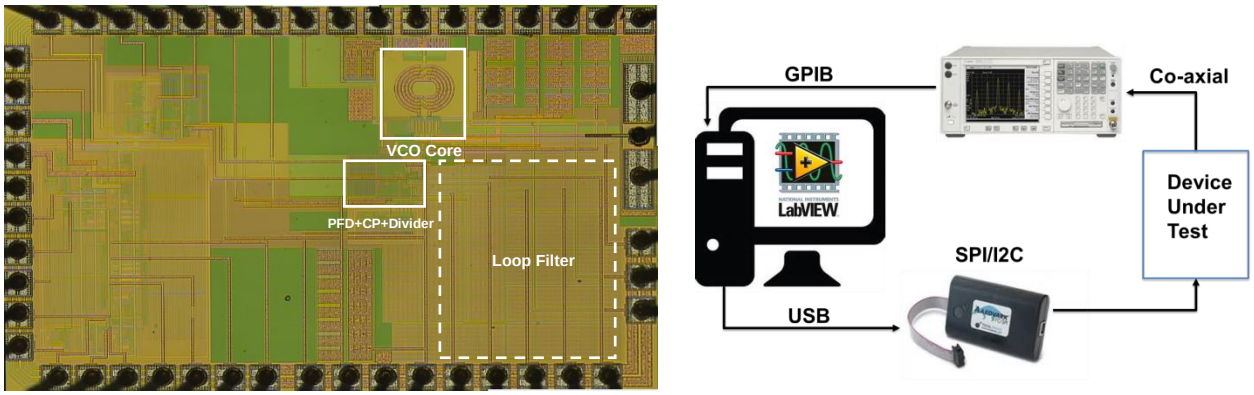


Figure 3.32. Simulated phase noise of 4-GHz PLL when the contributions from all the components in the loop are included.

3.7 Measurement Results

A prototype of PLL was fabricated in a 65-nm CMOS process with 10 Copper metal layers and wire-bonded onto a printed circuit board (PCB) for measurements. The die micrograph is shown in Figure 3.33(a). A setup for measuring the PLL phase noise with different combinations of cross-coupled pairs in the VCO is shown in Figure 3.33(b). 32 of the 64 cross-coupling transistor pairs are switched ON in the VCO by sending a random set of 32 "1" bits using LabVIEW to the DUT using an SPI/I2C interface.



(a) (b)

Figure 3.33. (a) Die photograph and (b) Measurement setup of the PLL in 65-nm CMOS incorporating a VCO employing an array of cross-coupled pairs and intelligent post-fabrication selection, respectively.

The locking range of the PLL is 4.01 - 4.7 GHz. The phase noise of PLL is measured using the PLL method in a Keysight E5052B Signal Source Analyzer and is collected using LabVIEW. Figure 3.34 shows the histograms of measured PLL phase noise variations of ~1700 combinations at 30-kHz, 300-kHz, 1-MHz, and 10-MHz offsets from a 4.01-GHz locked carrier, respectively when 32 cross-coupled transistor pairs out of the 64 pairs in the VCO are switched ON. Figure 3.35 shows the phase noise plots of these 1700 combinations.

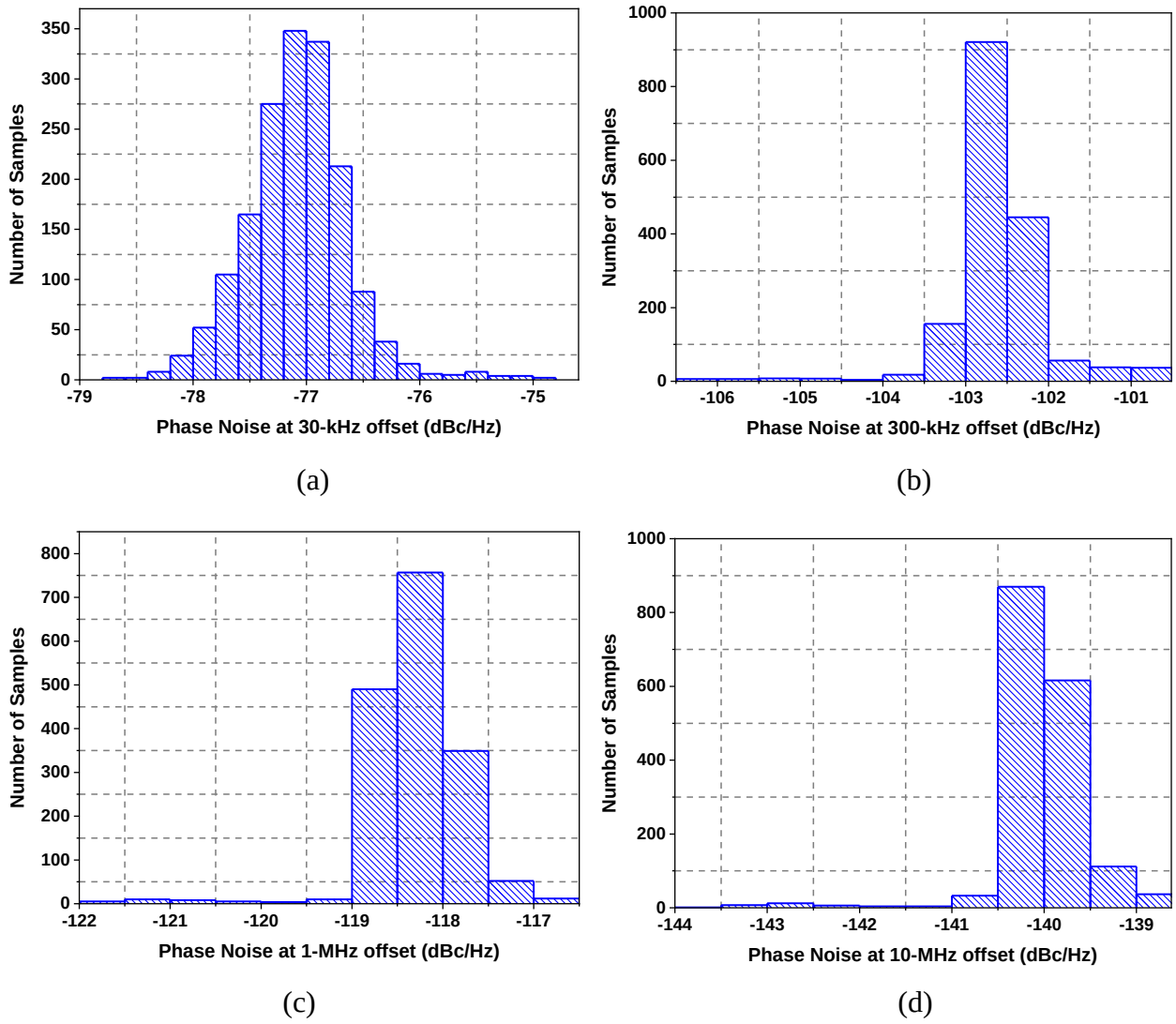


Figure 3.34. Histograms of PLL phase noise variations at (a) 30-kHz offset, (b) 300-kHz offset, (c) 1-MHz offset, and (d) 10-MHz offset from a 4.01-GHz carrier, respectively when 32 cross-coupled pairs are switched ON in the VCO.

From Figure 3.35, it can be observed that the loop bandwidth of the combinations varies from around 60 kHz to 90 kHz. The variation in the PLL loop bandwidth for equal number of switched-ON cross-coupled pairs is mainly due to the variation in VCO gain, K_{vco}. As discussed in section 3.4.5, the loop bandwidth is the frequency at which the open loop gain of the PLL, H_{oL} is reduced to 0 dB. The open loop gain of the PLL is given by equation 3.31. From the equation,

it can be observed that all the parameters are constant for the combinations of cross-coupling pairs, except for the factor "K_{vco}/s", which is one of the main factors in determining the loop bandwidth. This implies that when the VCO gains vary among the combinations having an equal number of switched-ON cross-coupling pairs, the open-loop gain and therefore the loop bandwidth also varies among these combinations.

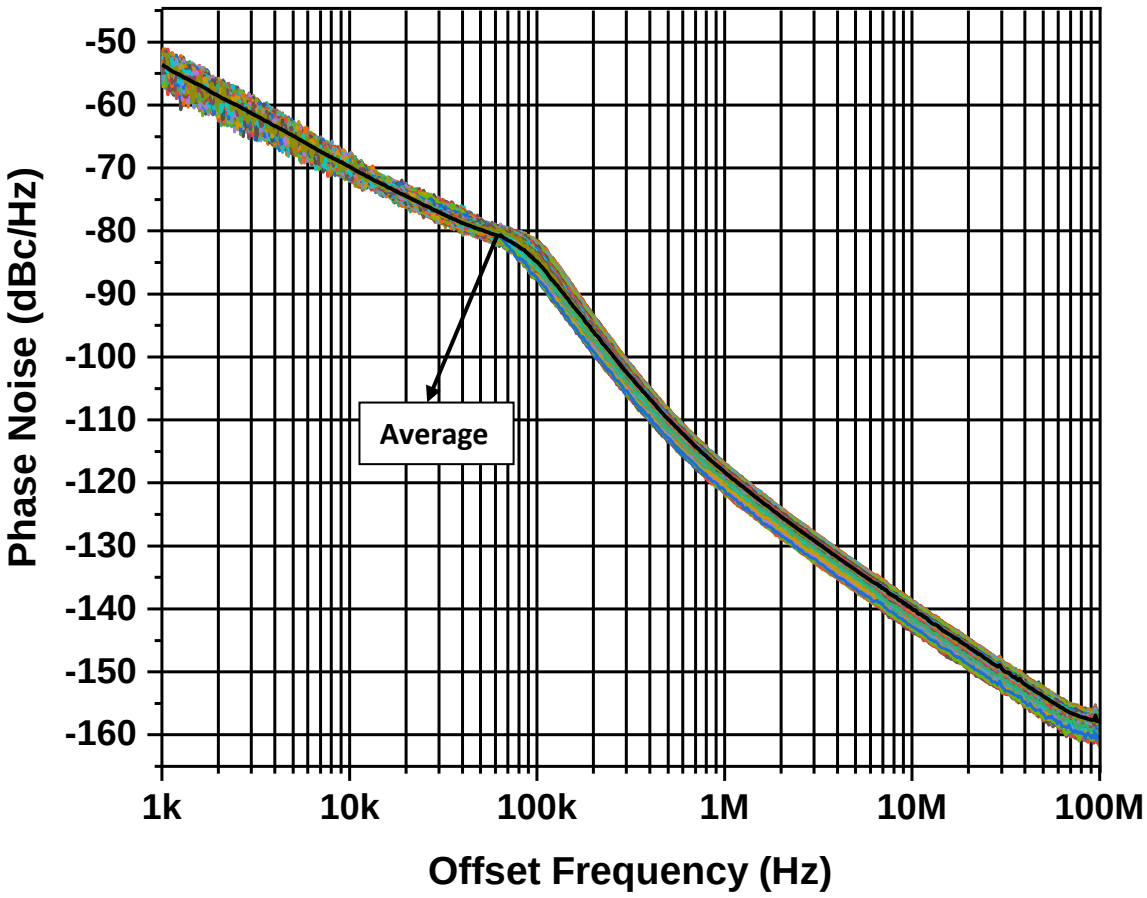


Figure 3.35. Measured phase noise plots of PLL when 32 cross-coupled transistor pairs are switched ON in the VCO. The average phase noise is also shown in the figure.

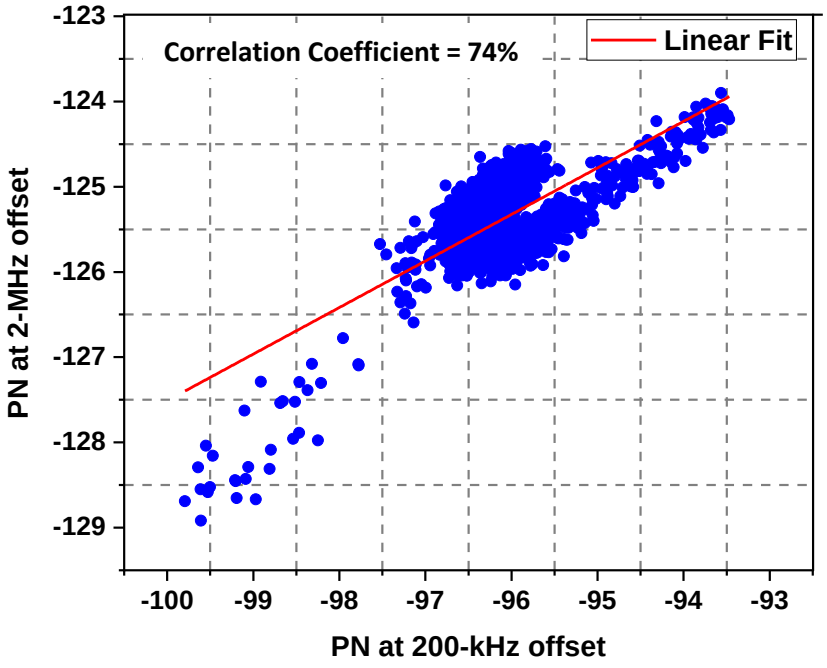
Two main observations can be made with respect to the PLL phase noise variations at 4.01GHz. The first observation is the in-band phase noise variation from 10-kHz offset to 60-kHz

offset is ~4-4.5 dB. In general, it is expected to have no variation in the in-band phase noise since it is dominated by the phase noise of input reference, but there are variations because of two reasons. The first reason is that since the loop gain and so bandwidth is relatively low, so the loop filter does not completely filter out the VCO phase noise below the loop bandwidth. There are some residual phase noise of VCO which show up in-band when the loop bandwidth is not high enough. Second reason is that there could be some variations in the reference phase noise transferred to the PLL output due to the variations of the VCO gain, K_{vco}. From section 3.4.4, the noise transfer function of input reference to the PLL output, N_{Ref} is

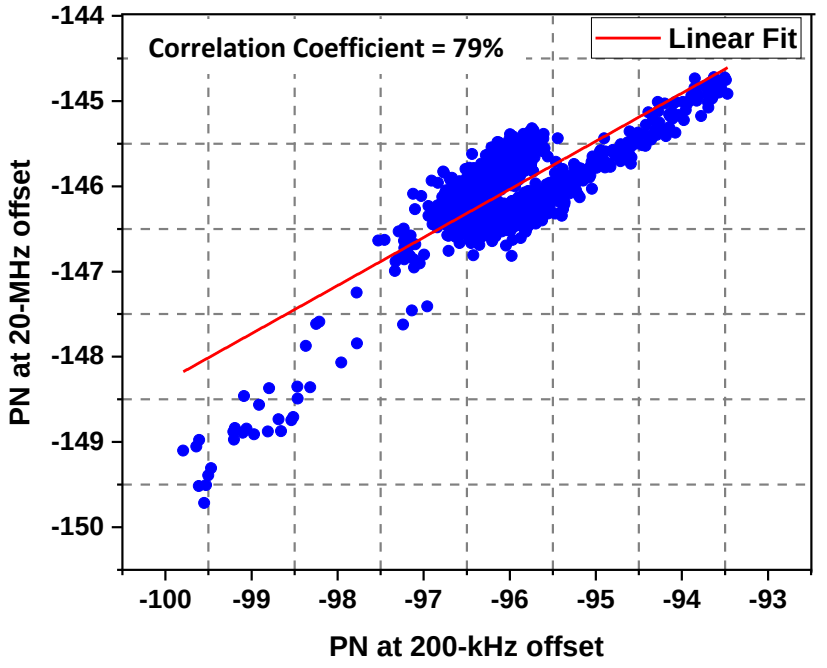
$$N_{Ref} = \frac{\Phi_{\text{out}}(s)}{\Phi_{n,Ref}(s)} = \frac{N.K_{VCO}I_p(1+sR_zC_z)}{2\pi \cdot s^2 N\left(sR_zC_zC_p+C_z+C_p\right)(1+sC_4R_4)+K_{VCO}I_p(1+sR_zC_z)} \qquad (3.32)$$

From the above equation, it can be observed that all the parameters in the equation are constant for the combinations of cross-coupling pairs, except the K_{vco} factor. Therefore, due to the variations of VCO gain, there can be a variation in the noise transfer of input reference to PLL output, which leads to the in-band phase noise variation.

The second observation is the out-of-band phase noise variation from 100-kHz offset to 100-MHz offset is ~5-5.5 dB. This is mainly due to the variation in both low frequency noise and thermal noise of the core cross-coupling transistor pairs in the VCO array, as discussed in Chapter 2. The low frequency noise variation of core devices in the VCO causes variation mainly of the PLL phase noise at offset frequencies from 100 kHz to 1 MHz, whereas the thermal noise variation causes variation mainly of the PLL phase noise at offset frequencies higher than 1 MHz.

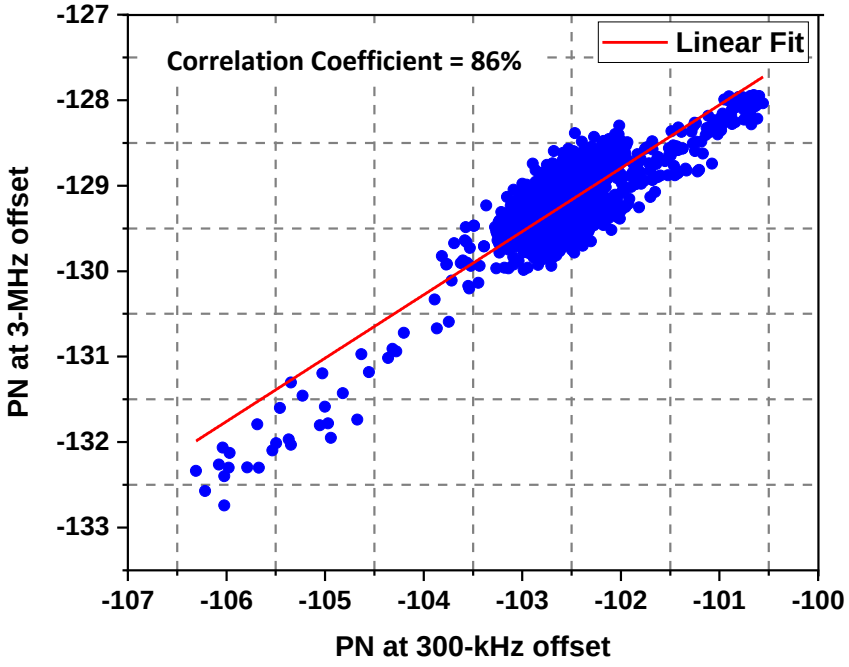


(a)

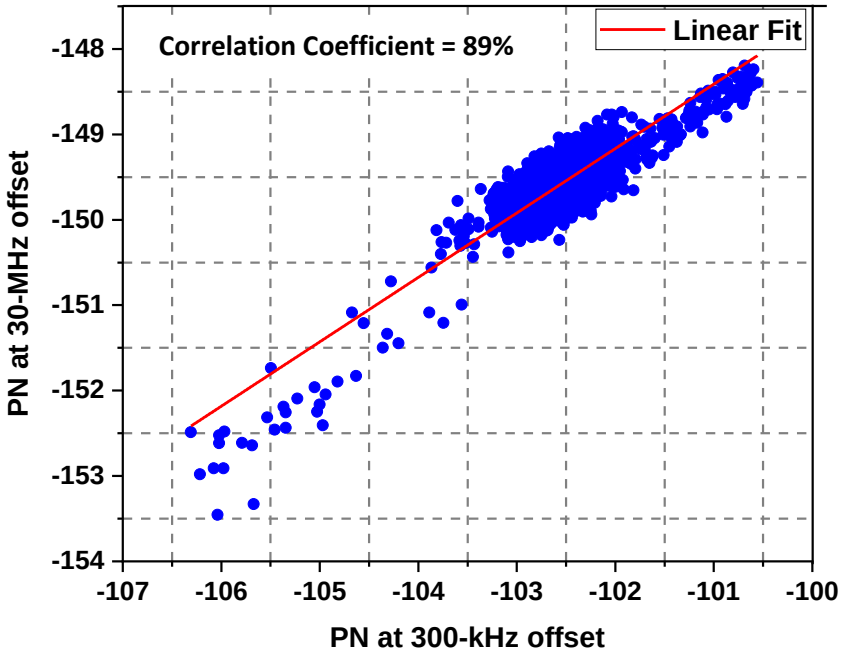


(b)

Figure 3.36. Phase noise of 4.01-GHz PLL at (a) 2-MHz offset versus 200-kHz offset, and (b) 20-MHz offset versus 200-kHz offset, when 32 cross-coupled transistor pairs are switched ON.



(a)



(b)

Figure 3.37. Phase noise of 4.01-GHz PLL at (a) 3-MHz offset versus 300-kHz offset, and (b) 30-MHz offset versus 300-kHz offset, when 32 cross-coupled transistor pairs are switched ON.

It can also be noted from Figure 3.35 that the lowest phase noise of PLL at 10-kHz offset and 30-kHz offsets are 2.5 dB and 2 dB lower than the average phase noise, respectively, whereas it is ~3.5-4 dB lower than the average phase noise at 300-kHz, 1-MHz and 3-MHz offsets, respectively from the 4.01-GHz locked carrier. Figures 3.36(a) and (b) show the PLL phase noise at 2-MHz offset versus 200-kHz offset, and 20-MHz offset versus 200-kHz offset, respectively for the combinations used in Figure 3.35 when 32 cross-coupled pairs are switched ON in the VCO. Similarly, Figures 3.37(a) and (b) show the phase noise at 3-MHz offset versus 300-kHz offset, and 30-MHz offset versus 300-kHz offset, respectively for the combinations used in Figure 3.35.

The calculated correlation coefficient between the phase noise at 2-MHz and 200-kHz offsets is 74% and between 20-MHz and 200-kHz offsets is 79%. Whereas, between 3-MHz and 300-kHz offsets, it is 86% and between 30-MHz and 300-kHz offsets, it is 89%. These high correlation coefficients indicate that there is correlation between low frequency noise and thermal noise, which is mainly due to the fluctuations in power spectral density, S_{id} of both the low frequency noise and thermal noise. The fluctuations of the power spectral density are again due to the variations of the number of traps and DC characteristics among the near minimum-size transistors that results in variations of low frequency noise and thermal noise, respectively as discussed in Chapter 1. Another reason for this phenomenon can be due to a correlated increased mobility due to lower trap density [61].

The genetic algorithm for post-fabrication selection is coded in Python and integrated with LabVIEW. Offset frequencies of 30-kHz, 300-kHz, 1-MHz and 3-MHz were used in the genetic algorithm to lower the phase noise. Around 100 combinations with 32 switched ON cross-coupling transistor pairs were generated by the algorithm in each generation.

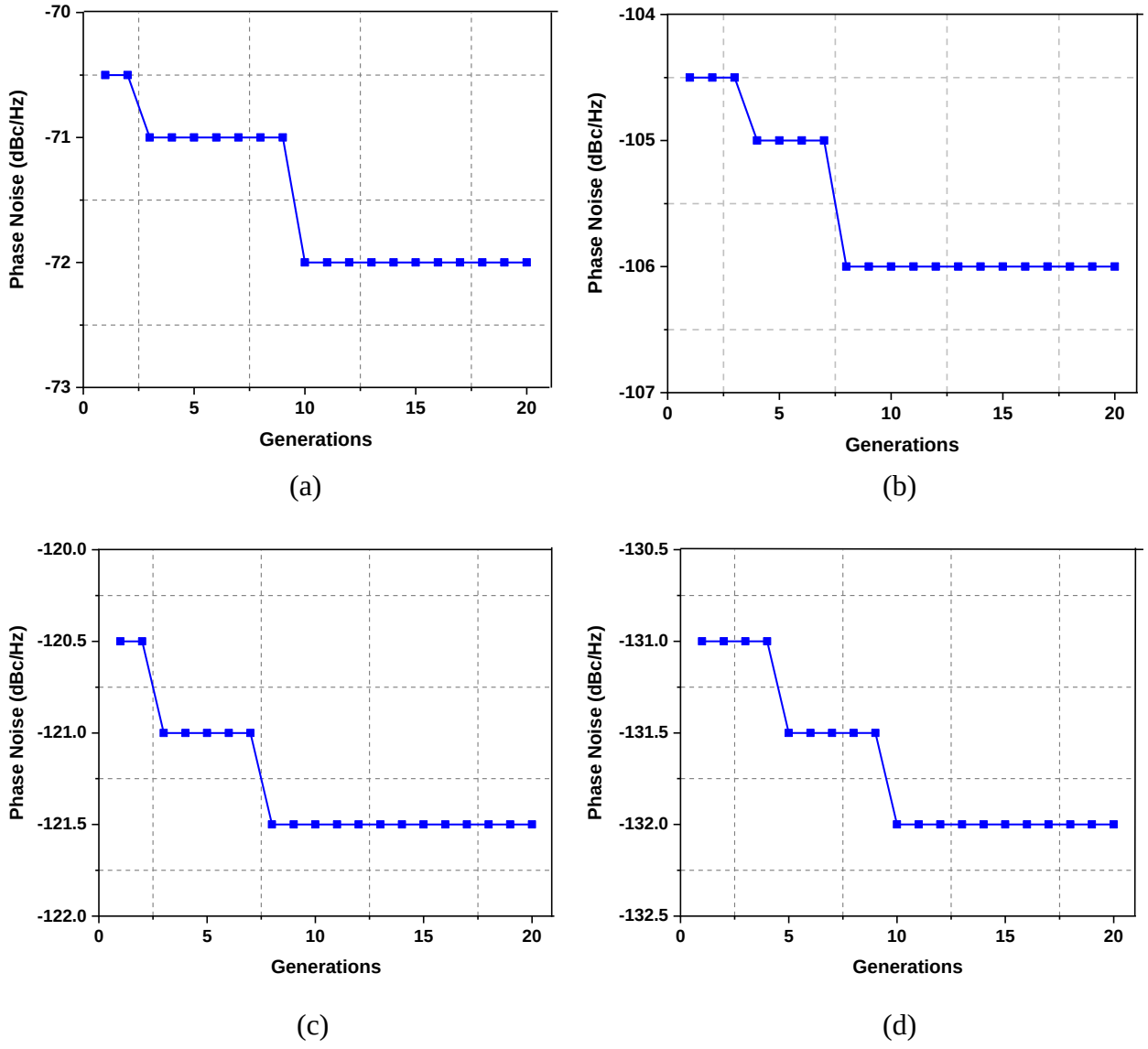


Figure 3.38. Phase noise reduction of PLL using a genetic algorithm at (a) 30-kHz offset, (b) 300-kHz offset, (c) 1-MHz offset and (d) 3-MHz offset from a 4.01-GHz carrier, respectively.

Figure 3.38 shows the measured lowest phase noise at 30-kHz, 300-kHz, 1-MHz and 3-MHz offsets, respectively at varying generations. The genetic algorithm converges to the combinations having the lowest phase noise of -72 dBc/Hz at 30-kHz offset, -106 dBc/Hz at 300-kHz offset, -121.5 dBc/Hz at 1-MHz offset, and -132 dBc/Hz at 3-MHz offset, respectively

from a 4.01-GHz locked carrier. By reducing phase noise at multiple offset frequencies, the overall integrated phase jitter of an Integer-N PLL can be reduced.

Figure 3.39 shows the PLL phase noise for the combination having the lowest phase noise of -121.8 dBc/Hz at 1-MHz offset from a 4.01-GHz carrier when 32 cross-coupled pairs in the VCO are selected. The slope of -2 is also shown in the figure, which is between 2-MHz and 20-MHz offsets. The loop bandwidth of the PLL is ~50 kHz. The phase noise at other offset frequencies is -69.4 dBc/Hz at 10-kHz offset, -74.8 dBc/Hz at 30-kHz offset, -106 dBc/Hz at 300-kHz offset, and -132.2 dBc/Hz at 3-MHz offset. The integrated rms jitter from 10-kHz to 100-MHz offsets is 2.4 ps, whereas it is 0.44 ps when integrated from 100-kHz to 100-MHz offsets.

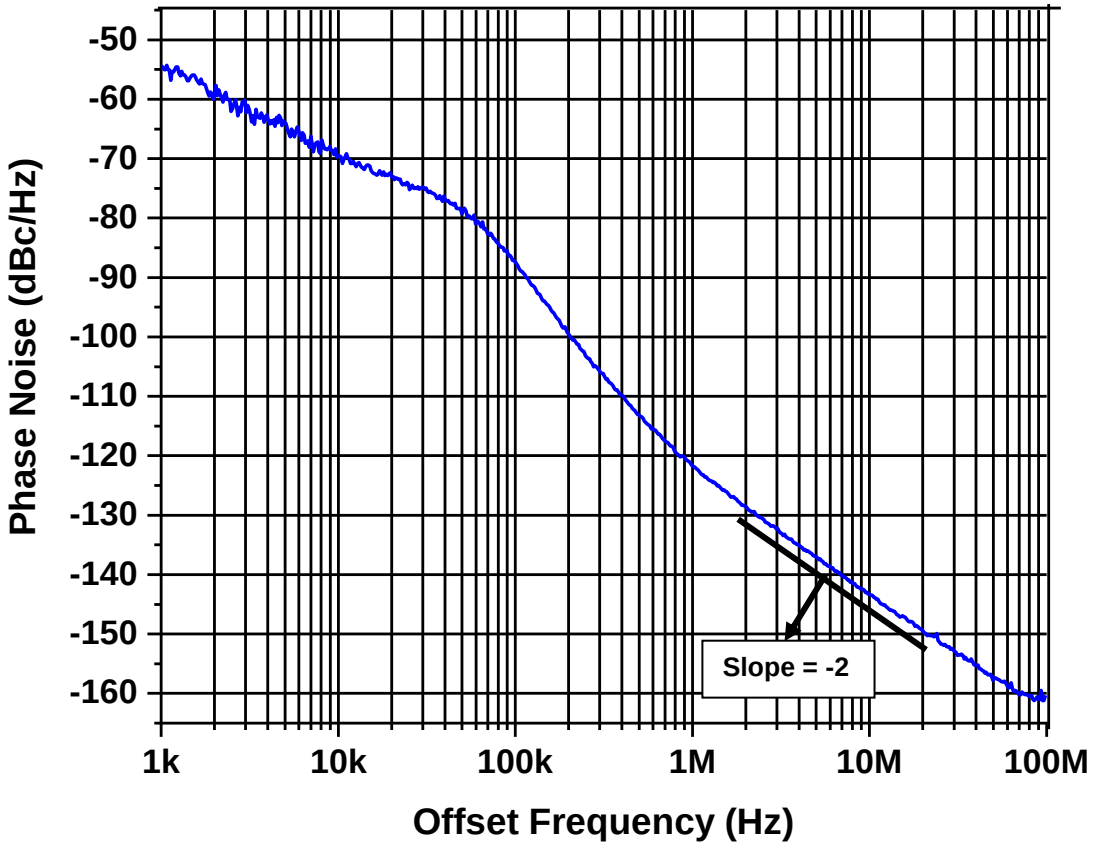


Figure 3.39. Phase noise of the PLL having the lowest phase noise of -121.8 dBc/Hz at 1-MHz offset from the 4.01-GHz carrier, when 32 cross-coupled pairs are switched ON in the VCO.

3.8 Conclusion

A technique to reduce both the in-band and out-of-band phase noise of a 4-GHz Integer-N PLL is demonstrated by employing an array of individually selectable cross-coupled pairs formed using near minimum-size transistors in an LC VCO and intelligent post-fabrication selection. The technique reduces the phase noise by taking advantage of the fact that when the transistor dimensions are reduced, the low frequency noise and thermal noise significantly varies. By reducing both the in-band and out-of-band phase noise, the overall integrated phase jitter in a frequency synthesizer can be minimized. Applying an intelligent post-fabrication selection process using a genetic algorithm, the phase noise at 30-kHz offset from 4.01-GHz is lowered by 2 dB from the average phase noise and by 4.5 dB from the maximum phase noise. Whereas at 300-kHz, 1-MHz, and 3-MHz offsets, it is lowered by 3.5-4 dB from the average phase noise and by ~5-5.5 dB from the maximum phase noise. The lowest phase noise of PLL at 1-MHz offset is -121.8 dBc/Hz from the 4.01 GHz carrier, whereas the integrated rms jitter from 10-kHz to 100-MHz offsets is 2.4 ps, and it is 440 fs when integrated from 100-kHz to 100-MHz offsets. The proposed technique is orthogonal to other jitter reduction techniques like sampling and sub-sampling PLL topologies [77]-[80] and can be applied in combination with these techniques to realize ultra-low jitter frequency synthesizers.

3.9 A Low Jitter 5-GHz PLL incorporating a VCO employing an array of nano-scale cross-coupled MOSFETs in 12-nm FinFET CMOS for an Autonomous System-On-Chip

Autonomous System-on-Chip (A-SoC) is a high-performance secure and trusted signal source in a 12-nm FinFET CMOS technology with a longer lifetime needed for applications that cannot tolerate unexpected failures. These high-performance autonomous systems can be used in a wide variety of applications like mission critical DoD communication and navigation systems, communication systems, autonomous vehicles, intelligent highways, and others. The goal of this work is to demonstrate a low jitter 5-GHz Integer-N phase locked loop (PLL) in 12-nm FinFET CMOS for A-SoC which self-optimizes for performance, self-heals to increase longevity, and self-identifies and verifies for improved trust and security by exploiting the variability of nano-scale MOS transistors through on-die machine learning.

3.9.1 Design and Simulations of the 5-GHz Integer-N PLL in 12-nm FinFET CMOS

A block diagram of the 5-GHz Integer-N PLL in 12-nm FinFET CMOS is shown in Figure 3.40. It is the same as that fabricated in 65-nm CMOS. A goal of this work is to investigate the applicability of the jitter reduction technique using an array of cross-coupled MOSFETs and intelligent post-fabrication selection discussed in section 3.7 to an advanced CMOS node. The 5-GHz output of VCO is locked to an integer multiple (x32) of the input reference signal of 156.25-MHz in a negative feedback configuration. Both the phase and frequency of the PLL output is locked to that of the input reference signal. The PLL incorporates a VCO using an array of near minimum size cross-coupled transistor pairs for post-fabrication selection of pairs with lower noise

which leads to lower phase noise in the VCO, and thereby a low jitter in the PLL. The schematic of VCO is shown in Figure 3.41.

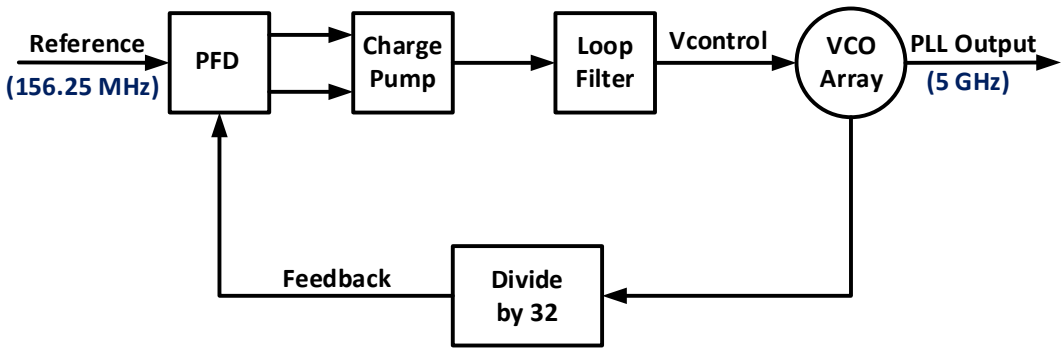


Figure 3.40. Block diagram of the 5-GHz PLL in 12-nm FinFET CMOS.

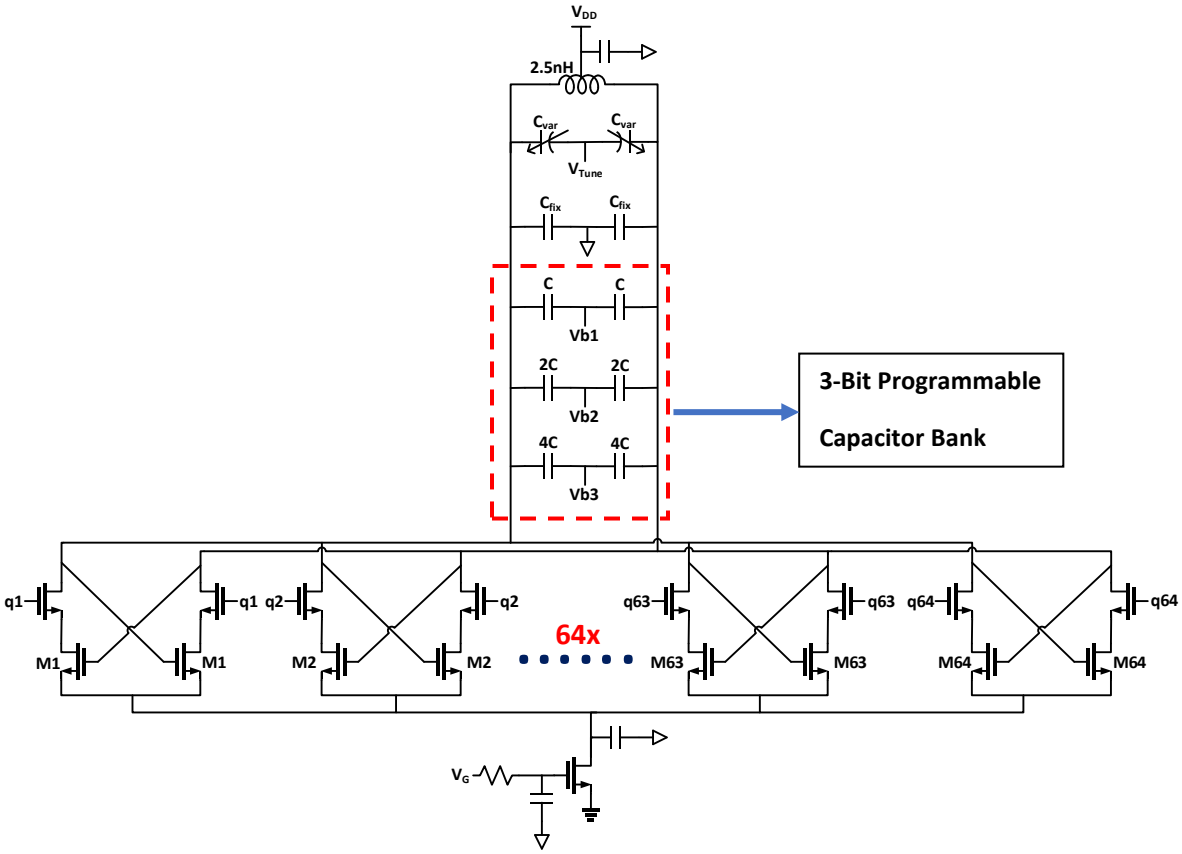


Figure 3.41. Schematic of the VCO using near minimum size cross-coupled transistor pairs in 12-nm FinFET CMOS.

The transistors (M1 to M64) forming the cross-coupled pairs have a width of 192 nm and a length of 14 nm. A 3-bit programmable capacitor bank is included in the design to maintain a constant and low VCO gain, K_{vco} throughout the entire tuning range of the VCO such that the AM-to-PM conversion is minimized [34] and a low phase noise is achieved throughout the entire tuning range.

The schematic of the complete 5-GHz Integer-N PLL in 12-nm FinFET CMOS is shown in Figure 3.42. The PLL uses a 3rd order passive loop filter which makes the whole PLL a 4th order system. Buffers are included in the design for the 5-GHz VCO/PLL output to drive a 50-ohm load, for divide-by-32 output, and between the 156.25-MHz input reference and PFD. A level shifter between the VCO and divide-by-2 provides proper bias voltages for the 'clk+' and clk-' transistors by shifting down the output common-mode voltage of VCO from 0.9V to 0.5V.

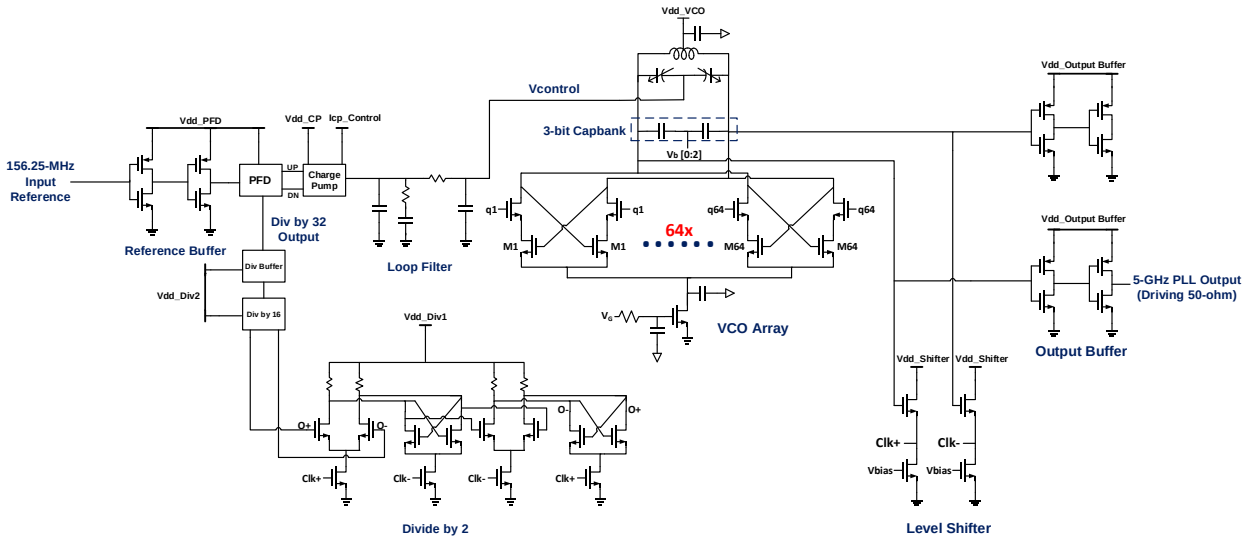


Figure 3.42. Schematic of the 5-GHz Integer-N PLL incorporating a VCO employing an array of cross-coupled transistor pairs in 12-nm FinFET CMOS and intelligent post-fabrication selection.

The transient simulations of the PLL are shown in Figure 3.43. The simulations show that mainly after the PLL reaches a steady state, (i) input reference frequency and the divided output frequency are equal, and (ii) Control Voltage (Vcontrol) is constant. These two observations show that the PLL is locked. The layout of 5-GHz PLL in 12-nm FinFET CMOS is shown in Figure 3.44. The core area of the PLL is 325 μm x 350 μm.

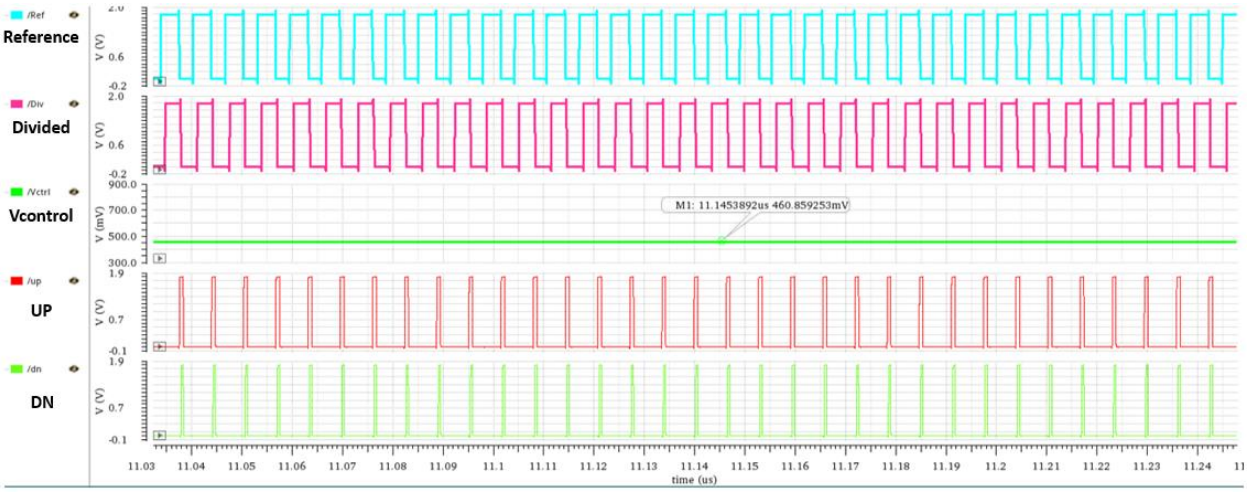


Figure 3.43. Transient simulations of the 5-GHz PLL.

3.9.2 Measurement Results

The prototype of 5-GHz PLL was fabricated and wire-bonded onto a printed circuit board (PCB) for measurements. The die micrograph is shown in Figure 3.45(a). A setup for measuring the PLL phase noise with different combinations of cross-coupled pair units in the VCO is shown in Figure 3.45(b). A particular number of cross-coupling transistor pairs can be switched ON in the VCO by sending a random set of "1" bits using LabVIEW to the DUT using an SPI/I2C interface.

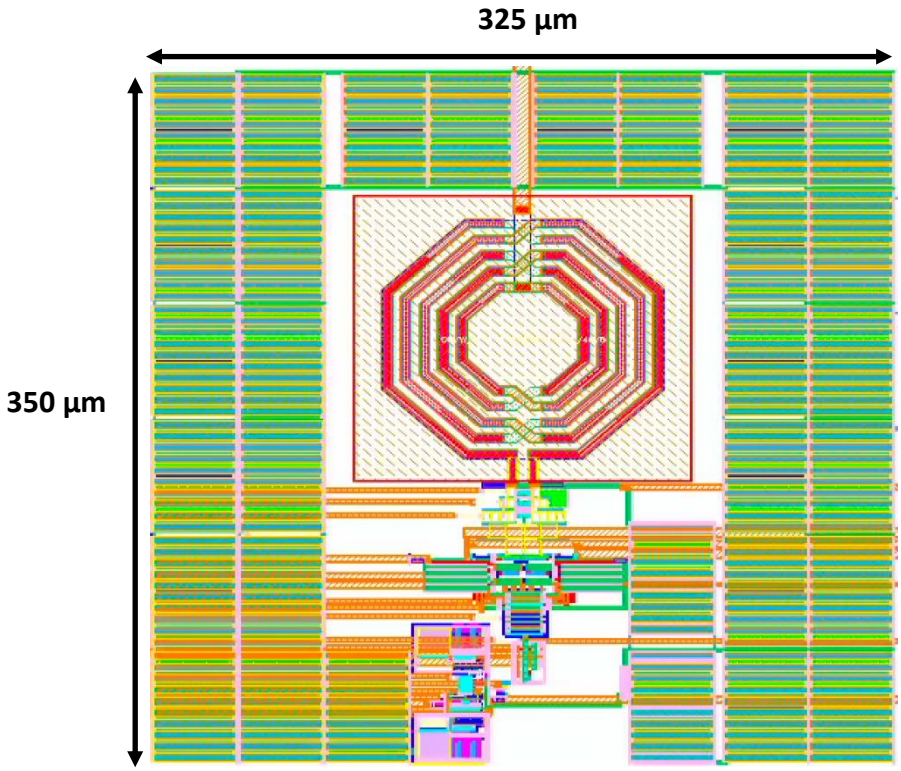
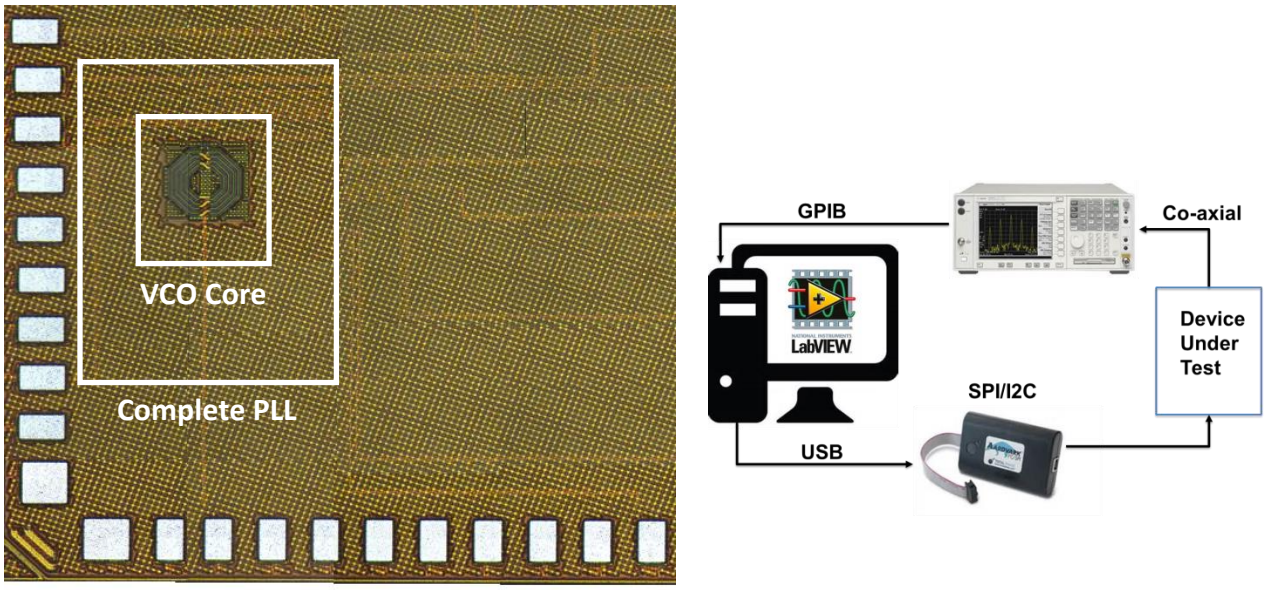


Figure 3.44. Layout of the core 5-GHz PLL in 12-nm FinFET CMOS.



(a) (b)

Figure 3.45. (a) Die photograph of the 5-GHz PLL in 12-nm FinFET CMOS, (b) Measurement setup for phase noise.

Initial measurements were made by checking the spectrum and phase noise performance of the free-running VCO. Figure 3.46 shows the measured phase noise of VCO in E5052B Signal Source Analyzer when all the 64 cross-coupled transistor pairs are switched ON in the VCO. From the figure, it can be observed that the phase noise at 100-kHz, 1-MHz and 10-MHz offsets are -76.5 dBc/Hz, -115 dBc/Hz and -136.5 dBc/Hz, respectively from a 4.7-GHz carrier.

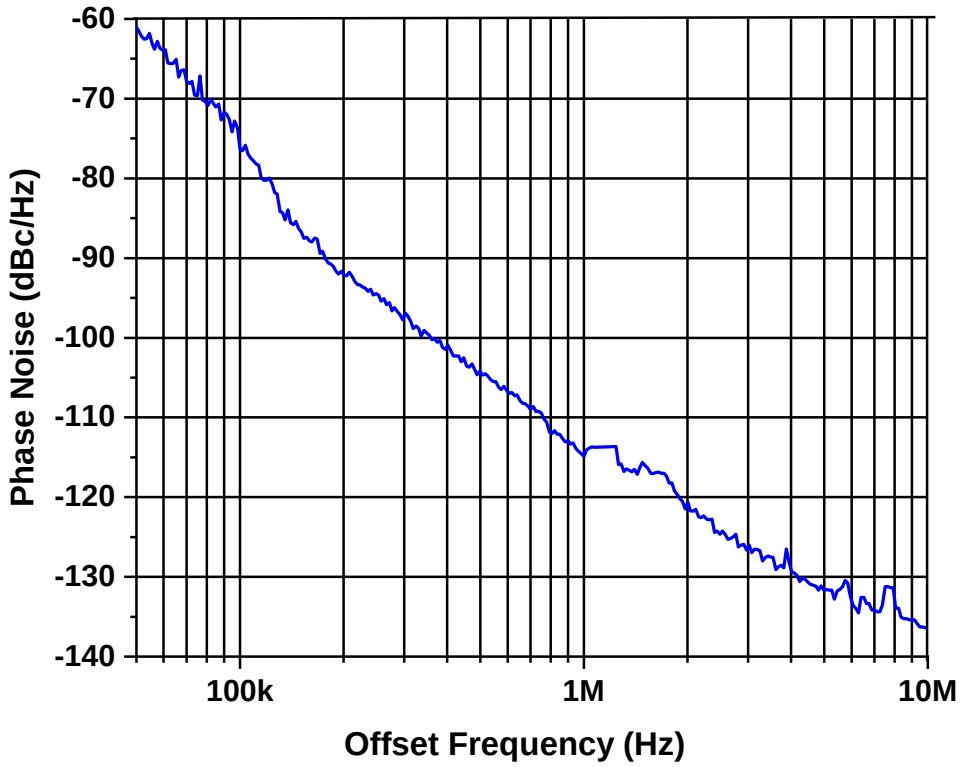


Figure 3.46. Measured phase noise of the 4.7-GHz VCO in 12-nm FinFET CMOS when all the 64 cross-coupled pairs are switched ON.

Figure 3.47 shows the histograms of measured phase noise variations of ~600 random combinations at 600-kHz, 1-MHz, 3-MHz and 10-MHz offsets from a 4.8-GHz carrier, respectively when 48 cross-coupled transistor pairs out of the 64 pairs are switched ON. Two main observations can be made from these histograms: (i) At 600-kHz offset, the phase noise variation

is around 12 dB, which mainly is due to the low frequency noise variation of the core devices being the dominant factor, and (ii) variation of phase noise is ~8 dB at the higher offsets of 1 MHz, 3 MHz and 10 MHz, respectively. The phase noise variation decreases with an increasing offset because the contributions of thermal noise increase at higher offset frequencies. Improvement in the VCO performance is expected after optimizing the bias current and selecting the best combinations of the cross-coupling pairs using intelligent post-fabrication selection.

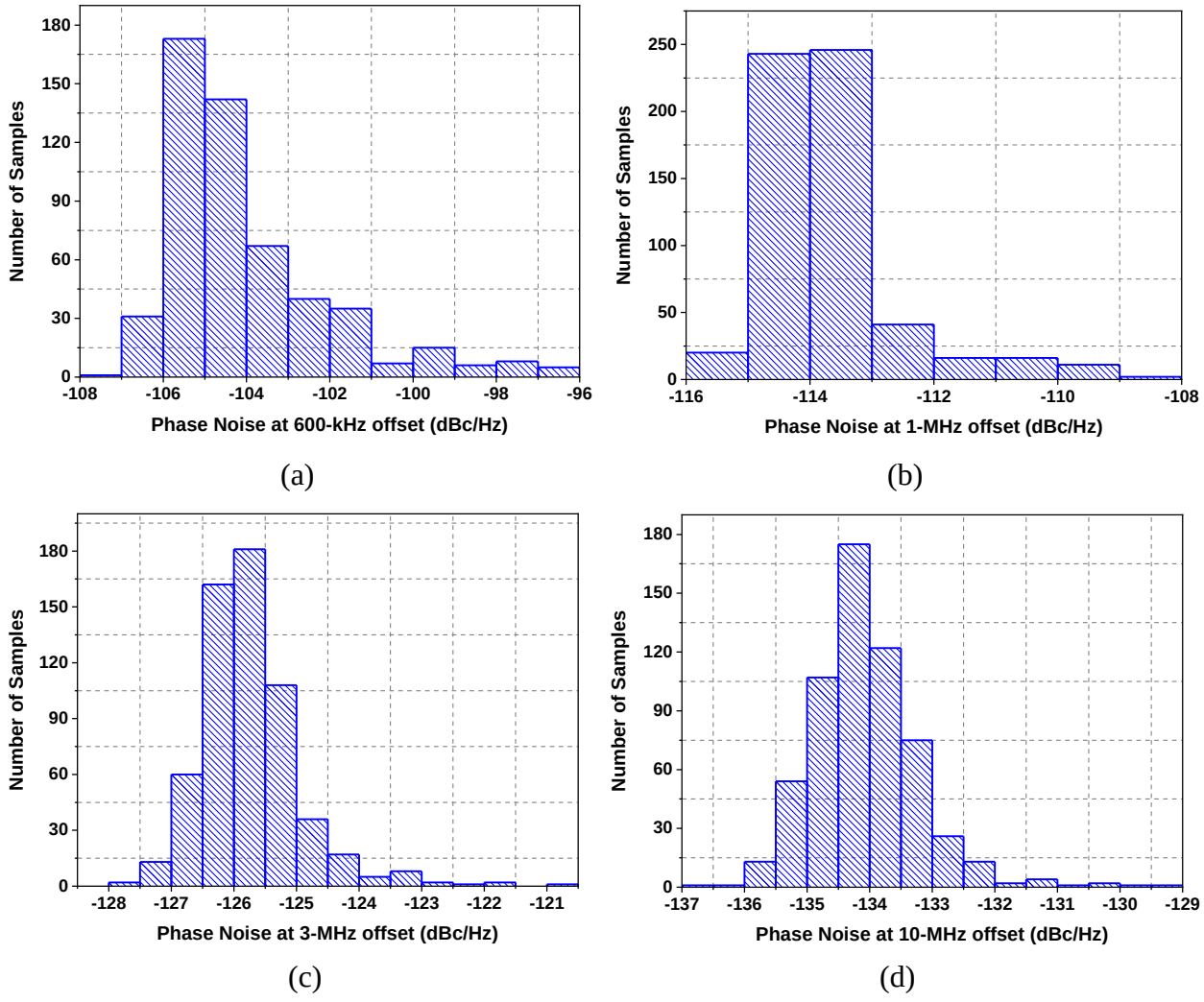


Figure 3.47. Histograms of phase noise at (a) 600-kHz, (b) 1-MHz, (c) 3-MHz and (d) 10-MHz offsets, respectively from a 4.8-GHz VCO, when 48 cross-coupled pairs are switched ON.

CHAPTER 4

NOISE FIGURE REDUCTION OF 6-GHZ CMOS MIXER-FIRST DOWN-CONVERTERS USING AN ARRAY OF PASSIVE MIXERS AND INTELLIGENT POST-FABRICATION SELECTION

4.1 Introduction

Ideally, an antenna interface of an RF receiver should perform three functions [86]: (i) match the impedance of the antenna for extracting the maximum signal power from the antenna and prevent the reflections, (ii) amplify the in-band signal while minimizing the signal to noise ratio, and (iii) reject the out-of-band interferers. The architecture of typical narrowband direct-conversion receivers includes an off-chip RF band-pass filter (BPF), a matching network, LNA, mixer, and finally the baseband circuitry. The band-pass filter rejects out-of-band interferers and is typically implemented with high quality-factor (Q) off-chip components such as SAW or BAW filters. The matching network, typically implemented with a resonant LC network, transfers as much power as possible to the LNA [86].

However, achieving above goals over a wide RF tuning range has proven quite challenging [55, 56]. Typically, the solutions for receivers capable of capturing several widely spaced bands either involve multiple, parallel narrowband front-ends, used one at a time [57, 58], or wideband receivers with only moderate rejection of interference (out-of-band IIP3 of <0 dBm) at many bands [55, 56]. The former solution comes at a significant cost in area both on chip and off because SAW and BAW filters occupy a large area [86], and the latter cannot achieve the necessary performance for many applications.

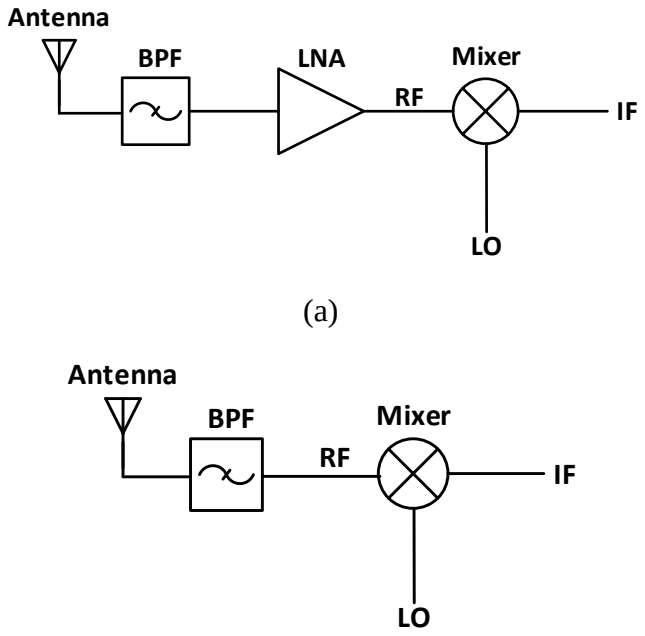


Figure 4.1. Block diagram of (a) LNA-first front end and (b) Mixer-first front end.

In principle, a direct conversion receiver does not require any RF components but a mixer and a local oscillator for its functioning [86], and indeed early receivers included only these components [59]. This simple approach has recently attracted more attention, as recent works suggests that connecting the antenna directly to a CMOS passive mixer without an RF LNA can provide significant benefits such as low power consumption [47] or wide RF tuning range and higher linearity [60]. It has been showed in [49] that a passive mixer-first receiver can achieve (i) S_{11} on par with that of the high-Q resonant matching networks and (ii) provide front-end filtering which results in out-of-band linearity competitive with the implementations using off-chip high-Q SAW and BAW filters.

In a conventional LNA-first receiver front end, as shown in Figure 4.1(a), the bandpass-filtered antenna input is first amplified by the LNA, so the mixer noise has a small contribution to the system noise performance. But in a mixer-first receiver, as shown in Figure 4.1(b), the problem is maintaining a low noise figure due to high conversion loss and high noise figure of the mixer. In this chapter, the main focus is to reduce the noise figure of CMOS passive mixer-first receivers by reducing the impact of low frequency noise through using an array of passive mixers.

4.2 Low Frequency Noise in Passive Mixers

Passive mixers are usually attractive because of having no sources of low frequency noise especially in AC coupled configurations, in contrast to the active mixers formed with Gilbert cells. Most circuit simulators adopt the approach of taking the mean of the fluctuating channel current bias as the value to be used for calculating the 1/f or low frequency noise. Hence, if a MOS transistor has a capacitor in series with the drain, there can be zero DC mean, and hence no noise should result. However, a more rigorous analysis in [48] showed that even with a zero DC mean, a non-zero time varying drain current noise can appear around the zero frequency as well as around the harmonics.

In a passive mixer, the magnitude of RF current in the drain is usually small. However, the LO drive is usually large to achieve a high linearity and therefore the overlap capacitances can significantly couple the currents into the drain at high frequencies, particularly if the impedances at each end of the mixer are unequal. Measurements in [48] showed that the low frequency noise was indeed present, and its impact was seen to increase linearly with the level of the RF drain current.

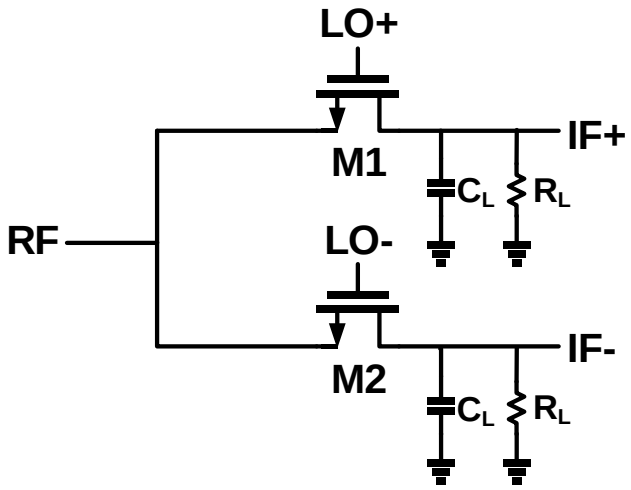


Figure 4.2. Schematic of a single-balanced passive mixer.

Figure 4.2 shows a schematic of a passive mixer formed with MOS transistors M1 and M2 and R-C loading. In general, larger MOS transistors are used in passive mixers for various reasons including better linearity, and for minimizing the series resistance of the switch which minimizes the RF to IF conversion loss and lowers the noise figure. However, simulations in [48] show that these larger MOS transistors in a passive mixer result in large overlap capacitances and large RF drain currents, thereby implicating that having larger MOS transistors for a passive mixer leads to more low frequency noise in the simulations.

Another work [30] showed that even without requiring any current flow, low frequency noise appears around the signal frequency. In a passive mixer, the bias voltages force the terminal voltages into one of three regions of operation. They are: “OFF overlap”, “zero overlap”, and “ON overlap”. Overlap refers to a time window around the LO zero crossing where both the MOSFETs with a common output terminal are in the same state; they are either both ON or both OFF. Over the rest of the LO cycle, one MOSFET is ON and the other MOSFET is OFF. Low frequency noise

at the gate modulates the moments of turn on/turn off of the MOSFET switches when they are driven by a gate voltage waveform of finite slope [30]. In turn, this modulates the duty cycle of the output and therefore the noise appears at the output.

Both the simulations and measurements in [30] showed that the mechanism for low frequency noise in passive mixers does not require any current flow in the MOSFETs. In summary, the low frequency noise at the output of a passive mixer depends on the amplitude of the RF input. In the region of "ON overlap", the low frequency noise lies at frequencies away from the signal. However, a large unwanted input signal at certain frequencies can add low frequency noise on to the wanted signal at the output of mixer. In "OFF overlap", the low frequency noise coincides in frequency with the wanted signal at the mixer output. As the noise is proportional to the signal, the signal to noise ratio (SNR) at the output due to low frequency noise is constant, improving only with sharper LO transitions [30].

This chapter presents a mixer-first downconverter employing an array of passive mixers formed using near minimum-size transistors and intelligent post-fabrication selection to reduce the low frequency noise impact in passive mixers and reduce the noise figure.

4.3 Mixer-First Downconverter Design Using an Array of Passive Mixers

4.3.1 Downconverter Design

Figure 4.3 shows a block diagram of the mixer-first downconverter employing a single-balanced passive-mixer formed using an addressable array of 8x16 (128) unit-cell pairs (M1 to M128). Figure 4.4(a) shows the schematic of a unit-cell. Each unit-cell pair consists of two mixing transistors with a width of 250 nm and a length of 60 nm, and a pair of CMOS inverter LO drivers

with two switches (S#) of a width of 1.2 µm and a length of 60 nm for selection. The widths of 60-nm length PMOS (Mp1) and NMOS (Mn1) transistors in the LO driver are 300 nm and 250 nm, respectively. The digital inputs for controlling the 128 switches are provided through a 128-bit Serial-In Parallel-Out (SIPO) flip-flop chain. When all the unit cells are selected, the total width of each mixing transistor is 32 µm, while the total width of the PMOS and NMOS transistors of each driver are 38.4 µm and 32 µm, respectively. An LC matching network is included between the RF input and the mixer-array for matching the mixer input impedance to 50 Ω at 6-GHz

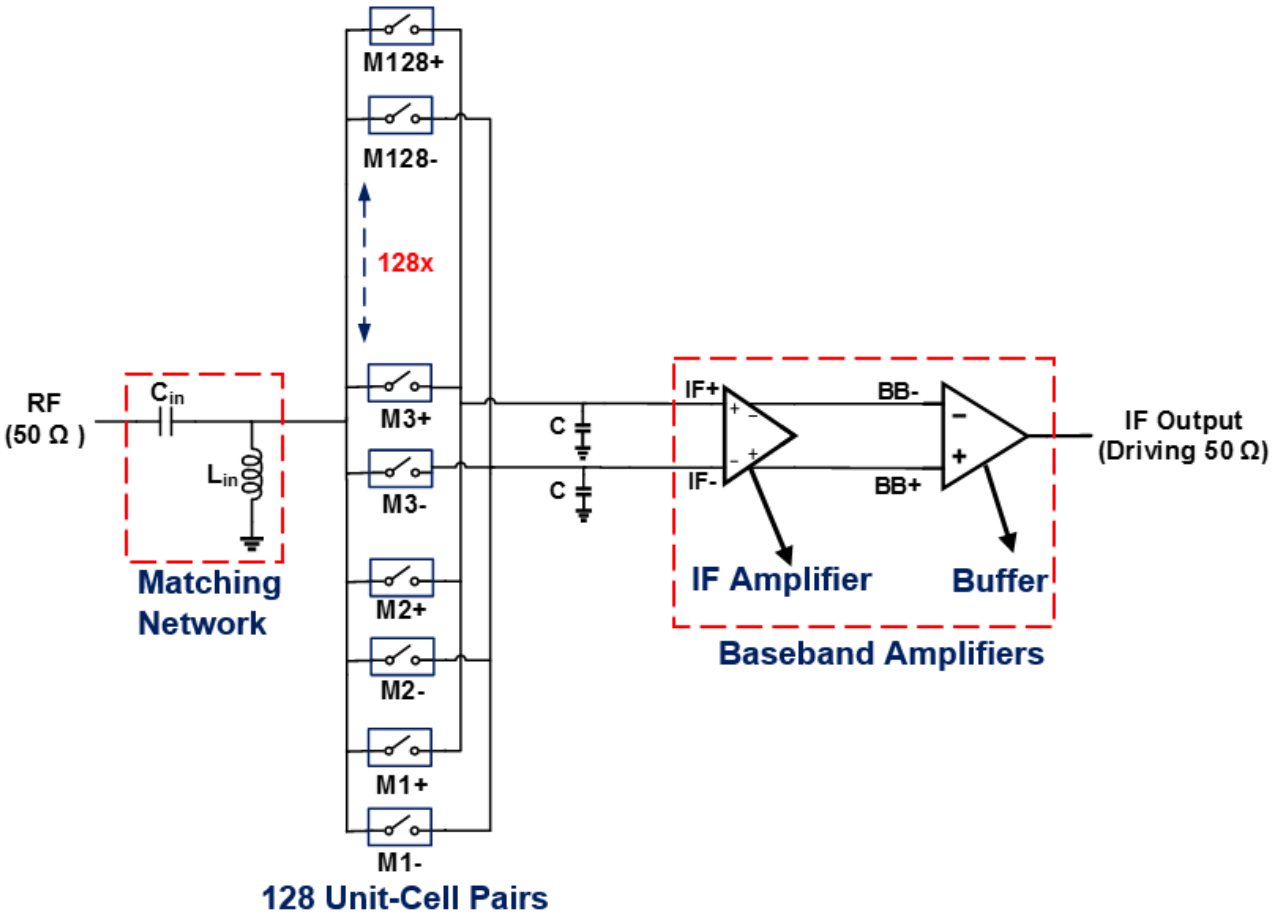
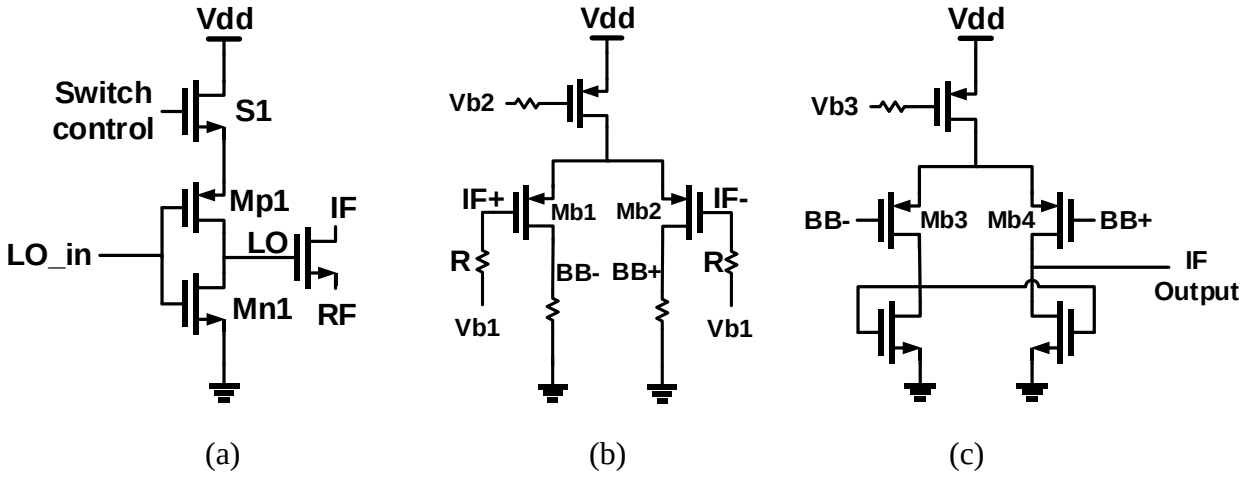


Figure 4.3. Block Diagram of the mixer-first downconverter using a passive-mixer array and baseband amplifiers.



(a) (b) (c)

Figure 4.4. Schematics of (a) Unit-Cell of LO Buffer+Mixer, (b) IF Amplifier, and (c) Buffer.

The matching network formed by a series capacitor (C_{in}) and a shunt inductor (L_{in}), lowers the noise figure by increasing the source impedance seen by the mixing transistors [47], which lowers the impact of their noise due to the series resistance. The load for the mixer-array consists of a parallel combination of sampling capacitors, bias resistors and the input capacitances of IF amplifier. A two-stage amplifier chain comprising a PMOS input IF amplifier and a buffer is used for signal amplification at baseband. The schematics of IF amplifier and buffer are shown in Figure. 4.4(b) and (c), respectively. Both amplification stages use wide and long channel length transistors (W=1 mm/L=500 nm for IF amplifier and W=1 mm/L=1 μm for buffer) to reduce their thermal noise and low frequency noise contributions at the IF output. The layout of the mixer-array with the SIPO is also shown in Figure 4.5.

4.3.2 Intelligent Search Via Genetic Algorithm

Searching among the vast space of 2^{128} possible unit-cell pair combinations to identify the ones having the lowest noise requires an intelligent algorithm. Hamming distance-driven search

[29] explores a predetermined number of options in the hamming distance vicinity of the initial seed and may converge to a local minimum. Instead, a classic genetic algorithm, which introduces more entropy in the search and is particularly efficient in exploring high-dimensional unstructured spaces is employed. In addition, the genetic algorithm makes no assumptions about the search space and is driven by randomness, which makes it superior in searching for the combinations having low phase noise in a larger space.

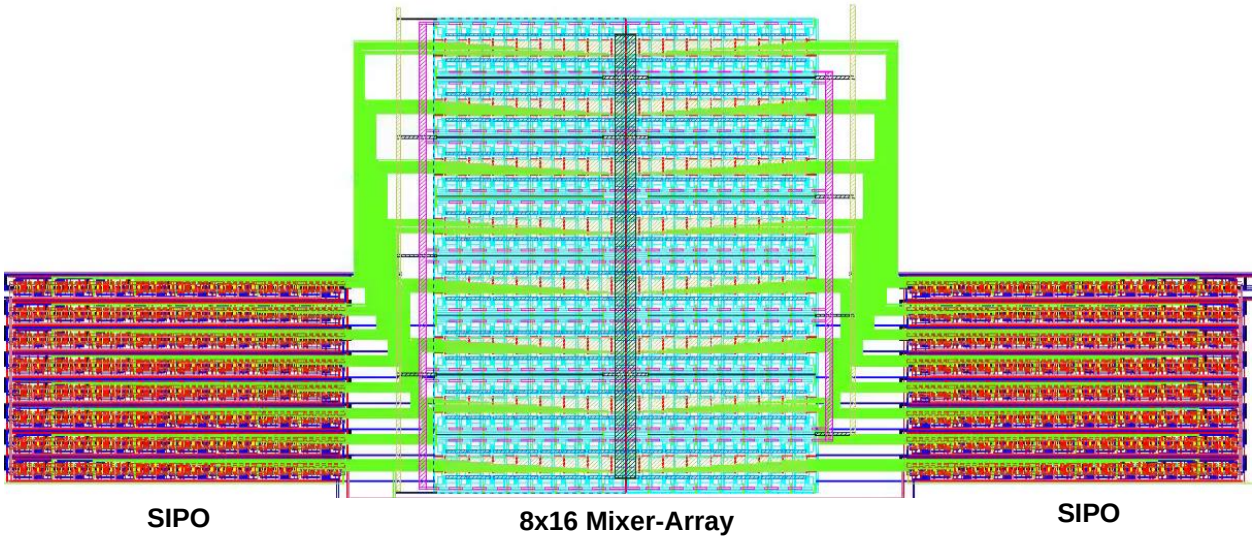


Figure 4.5. Layout of the Mixer-Array with SIPO.

The flowchart of the genetic algorithm is shown in Figure 4.6. Each unit-cell pair is represented by a bit, with a value of "1" indicating the pair is switched ON. The genetic algorithm starts by generating a random population of chromosomes (i.e. binary strings with a varying length) with a user-defined range of numbers of "1's", for which the fitness function (i.e. output noise) is measured. The top 50% of the population with the lowest output noise is retained, and the binary strings in this population are named as "parent strings".

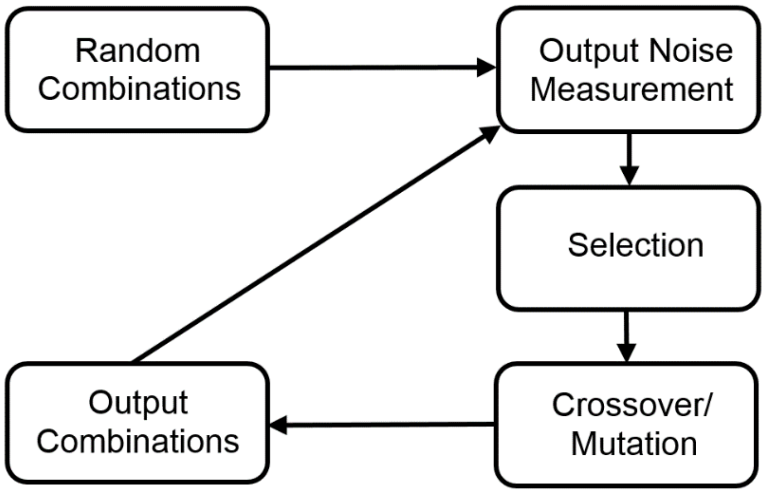
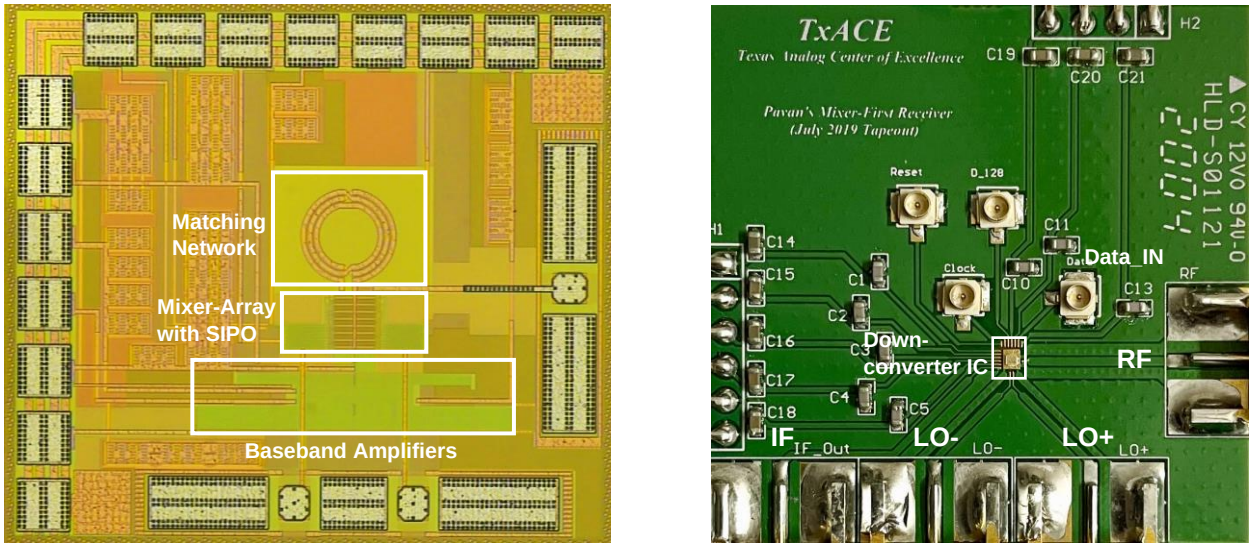


Figure 4.6. Flowchart of the Genetic Algorithm for Output Noise Reduction.

The population is then replenished with new chromosomes by mutating the pairs of parent strings at a randomly chosen bit-location, called the "crossover point". All the bits to the right of the crossover point are swapped between the pairs of parent strings to generate new offspring strings. The rationale of this operation is that, after multiple generations, mutation will allow a sufficiently diverse space to be explored while the crossover will discard the bits having high noise in the parent strings and, thereby generating new offspring strings with lower noise. The algorithm continues until a user-selected fitness limit is achieved, or until combinations with sufficiently low output noise are found.

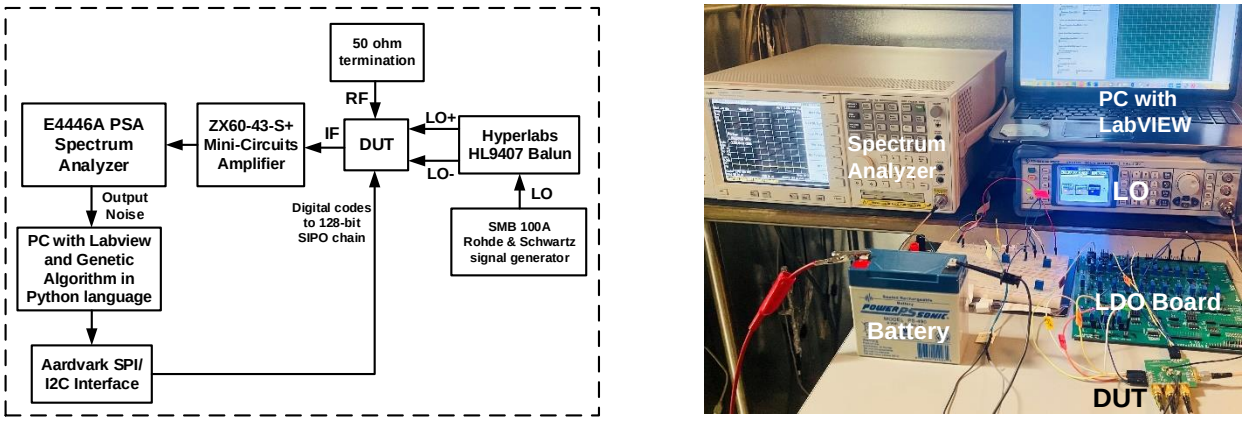
4.4 Measurement Results

The mixer-first downconverter is fabricated using a 65-nm CMOS process with 10 Copper metal layers and 1 Aluminum bond pad layer, and wire-bonded onto a printed circuit board (PCB). The die photo is shown in the Figure 4.7(a), and photograph of the PCB is shown in Figure 4.7(b).



(a) (b)

Figure 4.7. (a) Die photograph and (b) PCB photograph of the mixer-first downconverter, respectively.



(c) (d)

Figure 4.8. (a) Block Diagram and (b) Photograph of the measurement setup, respectively for output noise measurement.

The die size is 0.7×0.65mm^2. The total power consumption of the downconverter is ~11.5 mW, including the LO buffer power consumption of 1.5 mW. Figures. 4.8(a) and 4.8(b) show the block diagram of the measurement setup for output noise and the photograph of the measurement setup, respectively.

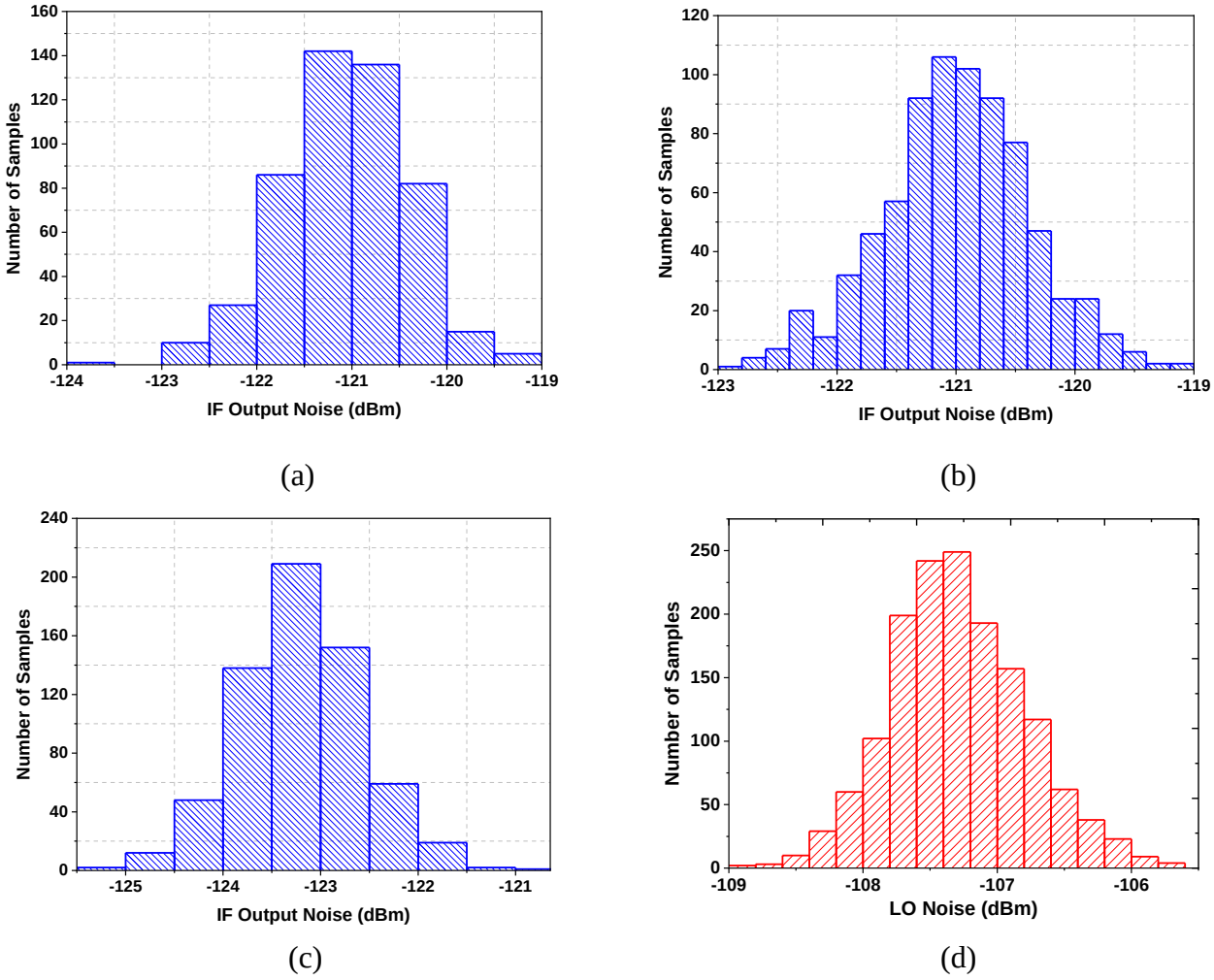


Figure 4.9. Histograms of Noise Variations at (a) 500-kHz IF, (b) 1-MHz IF, (c) 5-MHz IF, and (d) 1-MHz offset from the 6 GHz LO.

Figure 4.9 shows the histograms of the measured output noise of 800 random combinations in which 108 of the 128 unit-cell pairs are switched on. The output noise variation is measured at IF of 500-kHz, 1-MHz and 5-MHz with a fixed LO frequency of 6 GHz. There is a variation of ~4-5 dB, mainly due to the low frequency noise of the LO buffer which is first up-converted to LO frequency, and then down-converted to IF by the mixer. In addition, the mismatch between LO+ and LO- signals and that between the mixer switch transistors causes differential to common-

mode conversion at the input of the mixer, which is down-converted to DC [48]. The noise variation at the 1-MHz offset from the 6-GHz LO is measured using the leakage at the IF output and is shown in Figure 4.9(d). The variation is ~3.5 dB, demonstrating the up-conversion of low frequency noise to LO frequency by the LO driver.

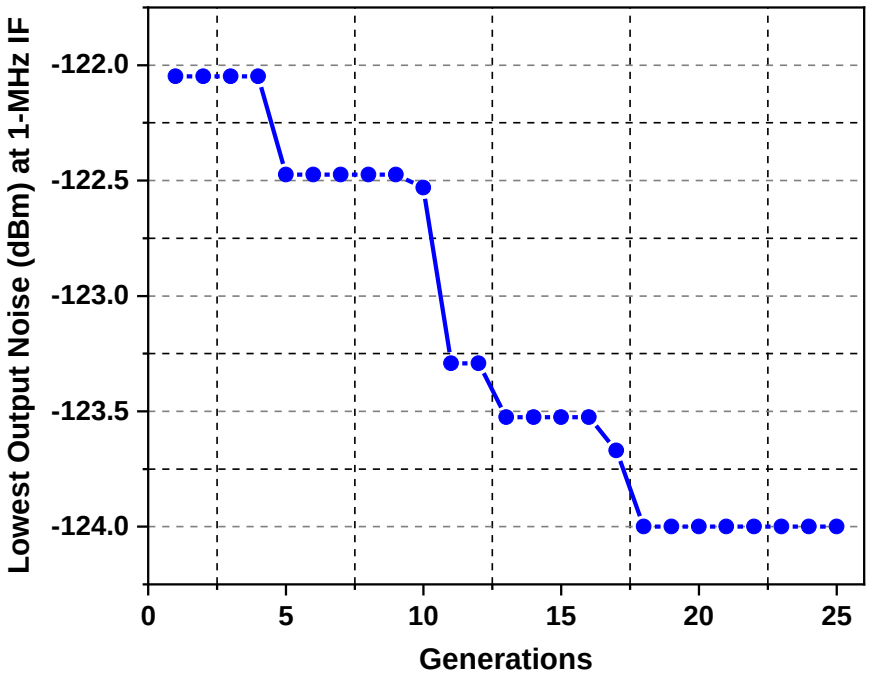


Figure 4.10. Output Noise Reduction using the Genetic Algorithm.

The genetic algorithm is written in Python and integrated with LabVIEW. Figure 4.10 shows the lowest output noise measured at 1-MHz IF versus generation number. In each generation, 80 combinations are measured. The algorithm converges to combinations having the lowest noise in the 17th generation. Figure 4.11 shows the measured conversion gain and double sideband noise figure (DSB NF) versus IF, respectively for the six best combinations identified by the algorithm. Noise Figure is measured using the gain method and includes the impact of the connector and PCB transmission line losses. The combination "f", which has 110 pairs out of 128

unit-cell pairs switched ON has the lowest DSB NF of 4.2 dB at 1-MHz IF and 5.1 dB at 10-MHz IF. All the six lowest noise combinations identified by the genetic algorithm have a lower noise figure than that when all the 128 pairs are switched on, demonstrating the effectiveness of this technique. The largest reduction is ~2 dB.

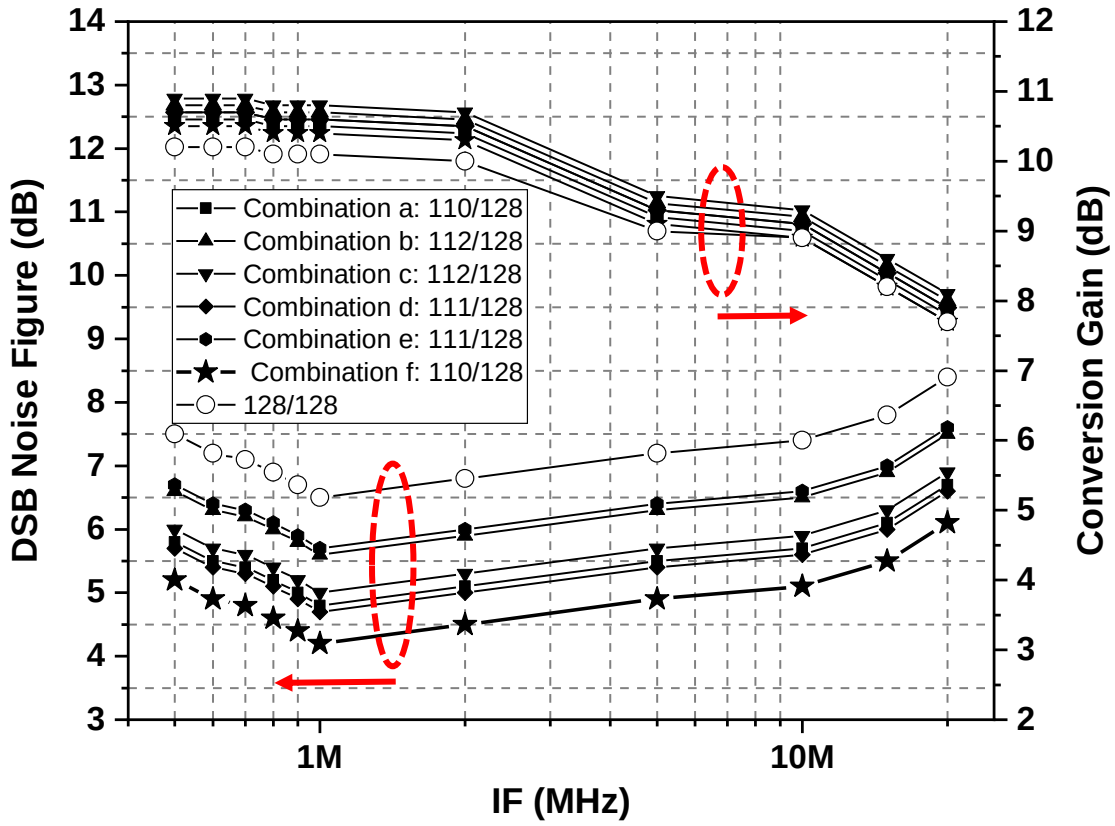


Figure 4.11. Measured conversion gain and DSB NF versus IF of the six combinations with lowest noise.

Figures 4.12 and 4.13 show the measured out-of-band (OOB) IIP3 and IIP2 for the combination "f", respectively. IIP3 is measured with a two-tone test at RF frequencies f_1 and f_2 of 5.96 GHz and 5.84 GHz respectively, and f_{LO} at 6 GHz, such that the 3rd order intermodulation ($2f_1 - f_2 - f_{LO}$) is 80-MHz.

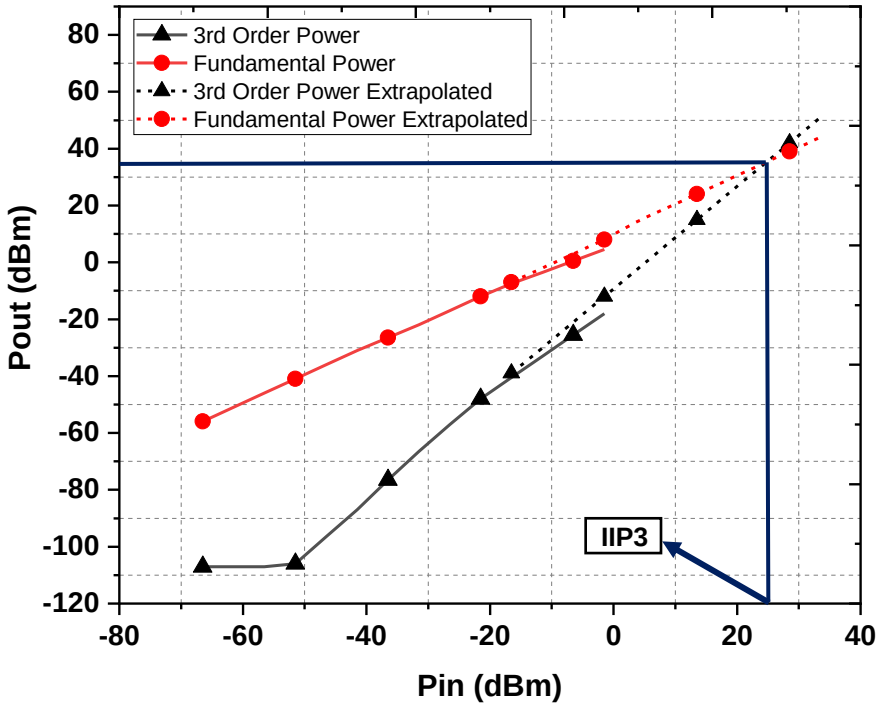


Figure 4.12. Measured Out-of-Band IIP3 for the Combination "f".

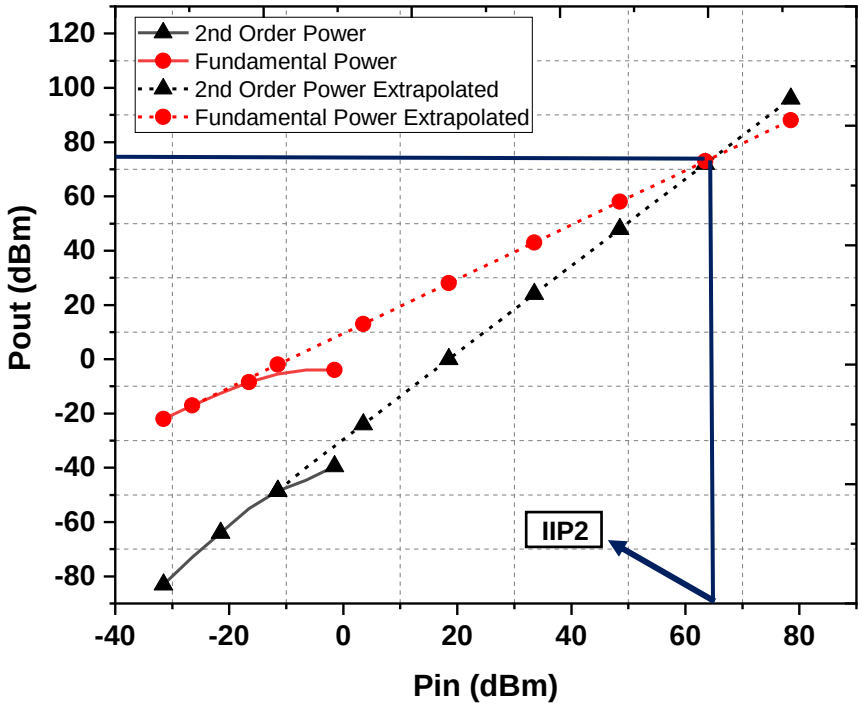


Figure 4.13. Measured Out-of-Band IIP2 for the Combination "f".

The IIP3 at which the extrapolated fundamental power is equal to the extrapolated third order power is 25 dBm. Similarly, IIP2 is measured with RF frequencies f_1 and f_2 of 5.9 GHz and 5.82 GHz respectively, and f_{LO} at 6 GHz, such that the 2nd order intermodulation ($f_1 - f_2$) is 80-MHz. The IIP2 at which the extrapolated fundamental power is equal to the extrapolated second order power is 65 dBm.

4.5 Performance Benchmark

Table 4.1. Performance summary and Comparison with other published downconverters.

	This work	**[47] JSSC '06**	**[49] JSSC '10**	**[50] JSSC '18**	**[51] ISSCC '12**	**[52] ISSCC '11**
Topology	**Mixer-First Array with Matching Network**	Mixer-First with Matching Network	N-Path Filter	Mixer-First	Mixer-First with Noise Cancelling	Dual-path (Mixer-First plus LNA-First)
RF (GHz)	**6**	2.4	0.1-2.4	0.2-8	0.08-2.7	0.4-6
IF (MHz)	**20**	N/A	20	10	N/A	20
Gain (dB)	**10.5 (Power Gain)**	N/A	40-70	21	70	70
DSB NF (dB)	**4.2 (at 1-MHz IF)**	5.1	3-5 (at 1-MHz IF)	2.3-5.4 (0.5-6 GHz f_{LO})	1.9	3-6.5 (at 1-MHz IF)
DSB NF (dB) @6-GHz RF	**4.2 (at 1-MHz IF)**			5.4 (IF N/A)		6.5 (at 1-MHz IF)
OOB IIP3 (dBm)	**+25 (at 80-MHz)**	N/A	+27	+39	+13.5	+10
OOB IIP2 (dBm)	**+65 (at 80-MHz)**	N/A	+56	+88	+55	+70
Power Dissipation (mW)	**11.5**	0.33	37-70	50-240	27-60	30-55
Technology (CMOS)	**65-nm**	130-nm	65-nm	45-nm	40-nm	40-nm

Table 4.1 compares the performance from this work to those of other published mixer-first downconverters. The proposed downconverter employing the mixer-array achieves the lowest noise figure at 6-GHz RF among the CMOS passive mixer-first downconverters.

4.6 Conclusion

A technique to reduce the noise figure of mixer-first downconverters is demonstrated by employing an array of passive mixers and LO buffers formed using transistors with near the minimum dimensions allowed in a CMOS technology and by employing an intelligent post fabrication selection. The technique reduces low frequency noise and thereby noise figure by taking advantage of the fact that when transistor dimensions are reduced, the number of defects responsible for low frequency noise can vary significantly. A genetic algorithm was used for post-fabrication selection to identify the combinations of transistor pairs having lower low frequency noise. Fabricated in 65-nm CMOS, the mixer-first downconverter achieves the lowest noise figure at 6-GHz RF among the CMOS passive mixer-first downconverters. It should be possible to extend this technique to receivers incorporating an N-path Filter. Lastly, an on-chip noise measurement circuit which can select combinations with low output noise at IF is needed to make this technique more practical.

CHAPTER 5

SUMMARY AND FUTURE WORKS

5.1 Summary

The low frequency noise, thermal noise and DC characteristics of nano-scale MOS transistors with dimensions close to the process minimum are highly variable. This work improves the noise performance of various integrated circuits and systems such as a 3.8-GHz voltage controlled oscillator (VCO), a 4-GHz synthesizer, and a 6-GHz mixer-first downconverter by exploiting the variability of nano-scale MOSFETs through an intelligent post-fabrication selection process.

First, phase noise of LC VCO's is reduced by employing an array of individually selectable cross-coupled pairs formed using transistors with dimensions near the minimum and through intelligent post-fabrication selection. The technique reduces the phase noise by taking advantage of the fact that when transistor dimensions are reduced, the low frequency noise and thermal noise can vary significantly. Applying an intelligent post-fabrication selection process using a genetic algorithm to the LC VCO employing an array of near minimum size cross-coupled transistors in a 65-nm CMOS process, the phase noise at 600-kHz, 1-MHz, and 3-MHz offsets from a 3.8-GHz carrier is lowered by 1.5-2 dB from the average phase noise and by ~3.5 dB from the maximum phase noise. The lowest phase noise of -122 dBc/Hz, -127 dBc/Hz, -137.5 dBc/Hz at 600-kHz, 1-MHz, and 3-MHz offsets, respectively from a 3.8-GHz carrier has been measured, while dissipating 7 mW of DC power. The VCO exhibits a state-of-the-art peak FoM of 191 dBc/Hz and an excellent FoM_A (FoM including the core area) of 207 dBc/Hz.

Next, a technique is demonstrated to reduce both the in-band and out-of-band phase noise of a 4-GHz Integer-N PLL by once again employing an array of individually selectable cross-coupled pairs formed using near minimum-size transistors in an LC VCO and through intelligent post-fabrication selection. By reducing both the in-band and out-of-band phase noise, the overall integrated phase jitter in a frequency synthesizer is minimized. Applying an intelligent post-fabrication selection process using a genetic algorithm, the phase noise at 30-kHz offset from 4.01-GHz is lowered by 2 dB from the average phase noise and by 4.5 dB from the maximum phase noise. Whereas at 300-kHz, 1-MHz, and 3-MHz offsets, it is lowered by 3.5-4 dB from the average phase noise and by ~5-5.5 dB from the maximum phase noise. The lowest phase noise of PLL at 1-MHz offset is -121.8 dBc/Hz from the 4.01 GHz carrier, whereas the integrated rms jitter from 10-kHz to 100-MHz offsets is 2.4 ps, and it is 440 fs when integrated from 100-kHz to 100-MHz offsets.

Finally, a technique to reduce the noise figure of mixer-first downconverters is demonstrated by employing an array of passive mixers and LO buffers formed using near minimum-size transistors and by employing an intelligent post-fabrication selection process. A genetic algorithm was used for post-fabrication selection to identify the combinations of transistor pairs having lower noise. Fabricated in a 65-nm CMOS process, the mixer-first downconverter dissipates 11.5 mW and achieves a double sideband noise figure of 4.2 dB at RF of 6 GHz, which is the lowest among CMOS passive mixer-first downconverters at 6-GHz RF. The out-of-band IIP3 and IIP2 of the downconverter are 25 dBm and 65 dBm, respectively at 80-MHz IF.

Using minimum size transistors to reduce the impact of low frequency noise is opposite to the conventional approach of using larger transistors, which relies on averaging to the value determined by the PDK model. An important point to note is that the proposed technique in this work for improving the noise performance is orthogonal to the other techniques since the proposed method reduces the device noise itself. For an LC VCO, the proposed technique can be applied in combination with other phase noise reduction techniques [35]-[46] to realize ultra-low phase noise oscillators. For instance, it can be used along with the harmonic shaping technique in a Class-F VCO and achieve an ultra-low phase noise. Similarly, for a PLL, the technique can be applied in combination with other jitter reduction techniques like sampling and sub-sampling PLL topologies [77]-[80] to realize ultra-low jitter frequency synthesizers. Finally, for a mixer-first downconverter, it should be possible to extend the proposed technique to the receivers incorporating an N-path filter, where a passive mixer-first downconverter is employed in each parallel chain of the N-path filter [49].

5.2 Future Works

5.2.1 Updated Mixer-First Downconverter

The 6-GHz passive mixer-first downconverter discussed in Chapter 4 (block diagram shown again in Figure 5.1) has a low measured conversion gain of 10.5 dB. This is mainly due to the reduced voltage gain of IF amplifier, which in turn is caused by the gate bias of PMOS transistors in IF amplifier (Mb1 and Mb2) being shorted to ground by the shunt inductor (L_{in}) in the RF matching network, when the passive mixers are switched ON in the array. The nominal

gate bias of transistors Mb1 and Mb2 is 0.2V. This problem can be resolved by re-designing the matching network with a series inductor and a shunt capacitor.

A block diagram of the design updates needed for the mixer-first downconverter in 65-nm CMOS is shown in Figure 5.2, where the matching network comprises of a series inductor (L_{in}) and shunt capacitor (C_{in}). The NMOS switch transistors (S_i) in the unit-cell pairs of "LO Buffer+Mixer" in the array should be changed to PMOS transistors, since the PMOS transistor is a better choice than NMOS transistor for pulling up voltages to V_{DD}. These modification in the switch design should provide a sharper LO signal with a higher amplitude to the passive mixer, and therefore a higher conversion gain and lower noise figure for the updated mixer-first downconverter is expected. Finally, the number of unit-cell pairs in the mixer array should be increased from 128 to 256 to provide more redundancy during the post-fabrication selection.

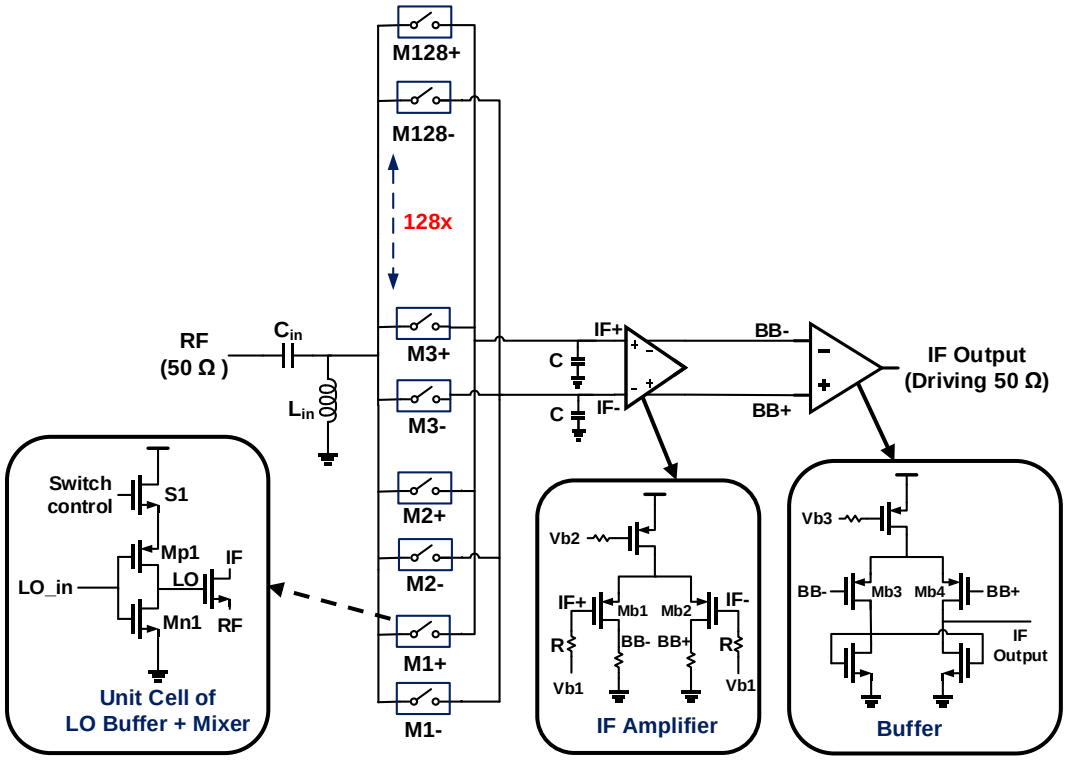


Figure 5.1. Block diagram of the passive mixer-first downconverter discussed in Chapter 4.

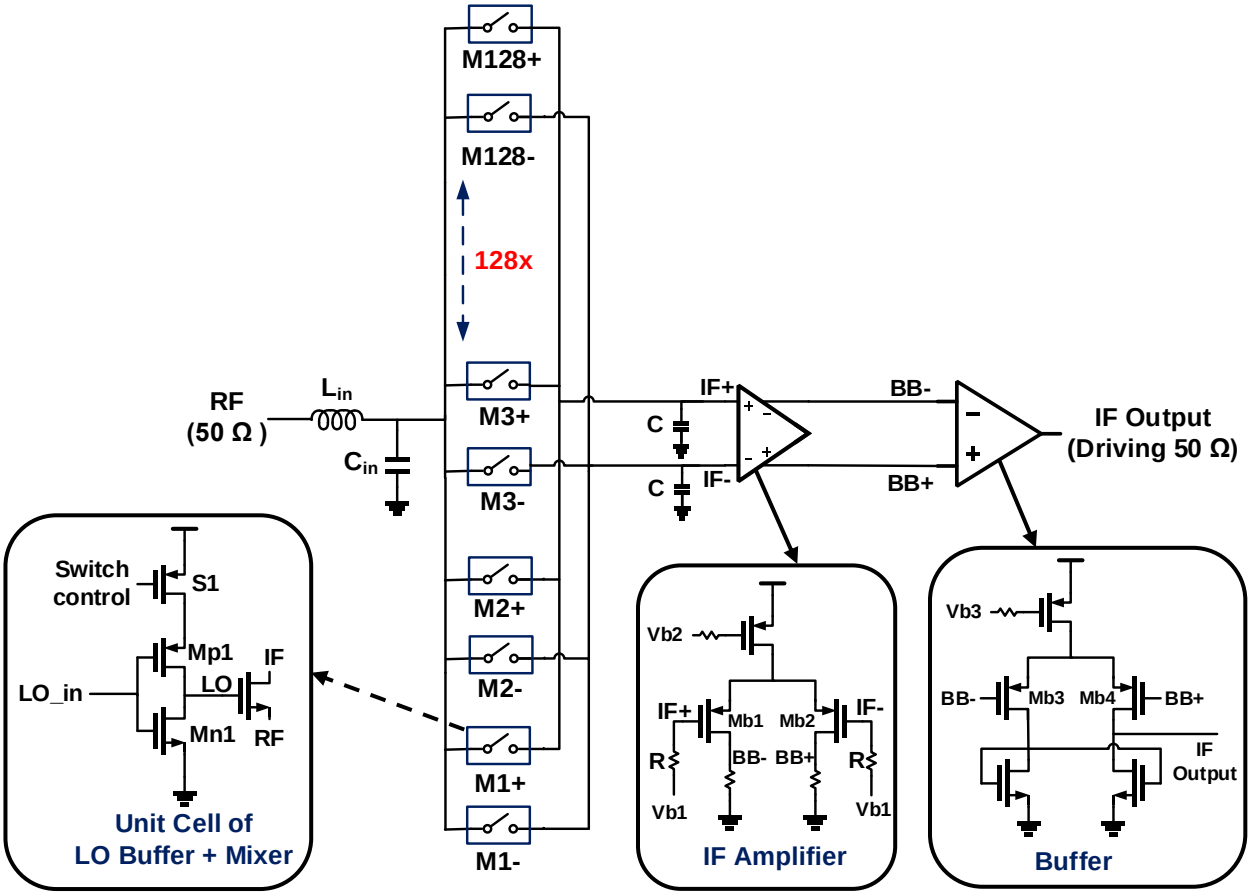


Figure 5.2. Block diagram of the updated mixer-first downconverter using a passive-mixer array and baseband amplifiers in 65-nm CMOS.

5.2.2 5-GHz Integer-N PLL in 12-nm FinFET CMOS

As mentioned in Chapter 3, initial measurements of the chip were made by checking the spectrum and phase noise performance of the free-running VCO. The measured phase noise of 5-GHz VCO in E5052B Signal Source Analyzer when all the 64 cross-coupled transistor pairs are switched ON at 100-kHz, 1-MHz and 10-MHz offsets are -76.5 dBc/Hz, -115 dBc/Hz and -136.5 dBc/Hz, respectively from the carrier. Variation in the phase noise is 12 dB at 600-kHz offset and 8 dB at 1-MHz, 3-MHz and 10-MHz offsets, respectively from a 4.8-GHz carrier, when

48 cross-coupled pairs are switched ON. Improvement in the VCO phase noise performance is expected after optimizing the bias current and selecting the best combinations of the cross-coupling pairs using intelligent post-fabrication selection.

5.2.3 Increasing Lifetime of Nano-Scale CMOS Circuits

It has been observed that noise is a highly sensitive parameter to device aging [83] and the degradation of small transistors is stochastic [84]. Because of these, it should be possible to use the circuits using arrays of transistors with dimensions close to the process minimum to monitor the degradation of noise performance due to aging of devices and identify alternate combinations using intelligent post-stress selection to maintain the noise performance over a longer operation time or increase the lifetime. The results from this work can also allow operation of circuits closer to the reliability limit to improve performance. The degradation of noise performance can be monitored using on-chip noise measurements circuits.

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BIOGRAPHICAL SKETCH

Venkata Pavan Kumar Yelleswarapu was born in Visakhapatnam, India in September 1990. He received his Bachelor of Technology degree in electronics and communications engineering from GITAM University, Visakhapatnam, India, in 2013 and his Master of Science degree in electrical engineering from The University of Texas at Dallas, Richardson, TX, USA, in 2015. In 2016, he joined TxACE at The University of Texas at Dallas to work towards his doctorate degree in electrical engineering. During summer 2020, he was a design intern at Qualcomm, Richardson, TX, where he worked on voltage-controlled oscillator (VCO) design for 5G millimeter wave applications. His research interests include integrated circuits and systems design for RF, millimeter wave and sub-millimeter wave applications.

CURRICULUM VITAE

Dec 1st, 2021

Pavan Yelleswarapu, Ph. D.
Department of Electrical Engineering,
The University of Texas at Dallas
Email: pavankumar.utd@gmail.com
Website: https://www.linkedin.com/in/pavankumaryv/

Summary:

- Interests mainly include integrated circuits and systems design for RF, millimeter wave and sub-millimeter wave applications.

- Successful tape-out experiences with VCO's, PLL, Mixer & Mixer-First Receiver so far in advanced CMOS technology nodes.

- Strong background in transistor level design of LNA, Mixer, VCO, PLL, Amplifier, Frequency Divider, etc.

- Good understanding of CMOS device physics and various RF architectures & their tradeoffs.

- Proficient with Cadence Virtuoso, Spectre RF, HFSS, Altium PCB. Strong background in layout, DRC, LVS, parasitic extraction, EM modelling of passives, and post-layout optimization.

- Proficient with lab measurements and equipment like probing, spectrum analyzer, network analyzer, oscilloscope, etc.

Educational History:

Ph.D, Electrical Engineering - University of Texas at Dallas, TX, USA	Dec. 2021
M.S, Electrical Engineering - University of Texas at Dallas, TX, USA	Dec. 2015
B.Tech, Electronics and Communications Engineering - GITAM University, India	May 2013

Employment History:

Research Assistant, **TxACE, UT Dallas,** USA Jan. 2016 - Dec. 2021

- New architectures for improving the noise performance of various circuits and systems like VCO, PLL, Mixer & Mixer-First Receiver in advanced CMOS technology nodes.
- Design of a 160-GHz LO chain for 315-GHz CMOS Receiver.
- Design of an Area-Efficient 17-20 GHz VCO+Divide-by-4 chain in 65-nm CMOS.

RF/mmWave IC Design Intern, **Qualcomm Incorporated,** USA May 2020 - Aug. 2020

Worked on design of high-performance, wide-band CMOS VCO's for 5G mmWave applications.

RF Hardware Design Intern, **Blackberry Limited,** USA June 2015 - Aug. 2015

Conducted the Radiated Sensitivity tests in anechoic chambers to verify for the 3GPP specifications for GSM, LTE, and WCDMA. Made changes on the printed circuit boards which resulted in better sensitivity of the radio receivers.

Publications:

- **Pavan Yelleswarapu**, A. Jha, A. Ahmadi, F. Jalalibidgoli, R. Willis, Y. Makris and Kenneth K.O, "Low Phase Noise Signal Generation Circuits in CMOS for Autonomous Sensors and Communication Systems", *SRC TECHCON 2019*, [P096888].
- Amit Jha, **Pavan Yelleswarapu**, Ken Liao, Geoffrey Yeap, and Kenneth K.O, "Approaches to Area Efficient High-Performance Voltage-Controlled Oscillators in Nanoscale CMOS", *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 1, pp. 147-156, Jan. 2021.
- Ibukunoluwa Momson, Shenggang Dong, **Pavan Yelleswarapu**, Wooyeol Choi, and Kenneth K.O, "315-GHz Self-Synchronizing Minimum Shift Keying Receiver in 65-nm CMOS", *IEEE Symposium on VLSI Circuits*, June 2020.
- Shenggang Dong, Ibukunoluwa Momson, Sandeep Kshattry, **Pavan Yelleswarapu**, Wooyeol Choi, and Kenneth K.O, "10-Gbps 180-GHz Phase-Locked-Loop Minimum Shift Keying Receiver", *IEEE Journal of Solid State Circuits*, vol. 56, no. 3, pp. 681-693, Nov. 2020.

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Honors:

Awarded Teaching Assistant for Master's level RF Integrated Circuit Design Course (EERF6330) at The University of Texas at Dallas in Spring 2018 semester.