COMPREHENSIVE CAPACITANCE-VOLTAGE ANALYSIS INCLUDING QUANTUM EFFECTS FOR HIGH-K INTERFACES ON GERMANIUM AND OTHER ALTERNATIVE CHANNEL MATERIALS

by

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My mother, father and sisters.

Whose love, encouragement and prayers of day and night make me able to achieve such success and honor.

My beloved wife and son.

Whose endless love, understanding, sacrifice and support made it possible to complete this work.

And all of my teachers.

Who made me the person I am today. I will be eternally grateful to you.

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by

SARKAR R. M. ANWAR, BSc, MSEE

DISSERTATION

Presented to the Faculty of

The University of Texas at Dallas

in Partial Fulfillment

of the Requirements

for the Degree of

DOCTOR OF PHILOSOPHY IN

ELECTRICAL ENGINEERING

THE UNIVERSITY OF TEXAS AT DALLAS

December 2016

ACKNOWLEDGMENTS

This may be the shortest but the most important section of my dissertation. After spending five years with these wonderful people, now I have a chance to express my gratitude to them.

First and foremost, I would like to thank my advisor, Professor Chris Hinkle, for his mentorship and guidance throughout my time at The University of Texas at Dallas. I appreciate the freedom and encouragement he provided which gave me the positive energy I needed for my research. I have been, and continue to be, inspired by his scientific intellect, integrity, tenacity, professionalism, and work ethic. His understanding and patience, especially through difficult times, was vital and I'm grateful to him for this. His rigorous review process has been an immensely valuable learning experience. His personality always impressed me and made me feel extremely fortunate to work with the finest advisor that one could possibly hope for.

I would also like to thank Professors Lawrence Overzet, Duncan MacFarlane, and Robert Helms for agreeing to be on my committee.

I am very grateful to have Shakil Mohammed as a colleague and a mentor. I have learned a lot from Shakil about work and family.

I would like to thank the cleanroom staff at UTD. Gordon Pollack for answering my questions about tools and processes, Scott Riekena for help with the PECVD system, Wallace Martin for trying to honor my every request, John Maynard for his flexibility and help with the sputter tools, and John Goodnight and Roger Robbins for keeping me safe inside the clean room. Thank you all for your dedication.

I would like to acknowledge Professor William Vandenberghe for his critical help in writing and benchmarking the CV ACE code and Professor Robert Wallace for the use of his XPS system.

During my time in NSERL, I have been fortunate to meet new friends and colleagues, including Adam Barton and Ruoyu Yue who have always been enjoyable to work with. Lee Walsh has put in a great effort to help me finish this dissertation, and it would not have been possible without him.

Thanks to Ashley Willess for efficient administrative support.

Also special thanks to Samsuddin Faisal Mahmood, who has been a great roommate and guide in university life in a foreign country.

There are no words in the dictionary to express my deepest gratitude to my parents and my sisters. Their continued love, sacrifice, support and encouragement have allowed me to pursue my ambitions.

Tasfia Khan, my better half, thank you for coming into my life and bringing joy. Your continued sacrifices have made the stress much more bearable. And thanks to Zaeem Anwar for delaying my PhD for unknown years. You are the best son one can ask for.

October 2016

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Publication No. _____

Sarkar R. M. Anwar, PhD
The University of Texas at Dallas, 2016

Supervising Professor: Christopher L. Hinkle

High mobility alternative channel materials to silicon are critical to the continued scaling of metal oxide semiconductor (MOS) devices. However, before they can be incorporated into advanced devices, some major issues need to be solved. The high mobility materials suffer from lower allowable thermal budgets compared to Si (before desorption and defect formation becomes an issue) and the absence of a good quality native oxide has further increased the interest in the use of high-k dielectrics. However, the high interface state density and high electric fields at these semiconductor/high-k interfaces can significantly impact the capacitance-voltage (C-V) profile, and current C-V modeling software cannot account for these effects. This in turn affects the parameters extracted from the C-V data of the high mobility semiconductor/high-k interface, which are crucial to fully understand the interface properties and expedite process development.

To address this issue, we developed a model which takes into account quantum corrections which can be applied to a number of these alternative channel materials including Si_xGe_{1-x},

Ge, InGaAs, and GaAs. The C-V simulation using this QM correction model is orders of magnitude faster compared to a full band Schrodinger-Poisson solver. The simulated C-V is directly benchmarked to a self consistent Schrodinger-Poisson solution for each bulk semiconductor material, and from the benchmarking process the QM correction parameters are extracted. The full program, C-V Alternative Channel Extraction (CV ACE), incorporates a quantum mechanical correction model, along with the interface state density model, and can extract device parameters such as equivalent oxide thickness (EOT), doping density and flat band voltage (V_{fb}) as well as the interface state density profile using multiple measurements performed at different frequencies and temperatures, simultaneously. The program was used to analyze experimentally measured C-V profiles and the extracted device parameters show excellent agreement with the known device structure and previously published results.

CV ACE has been applied in the development of a process flow for germanium interface passivation in Ge based MOS devices using a GeO_x interlayer. A post atomic layer deposition (ALD) plasma oxidation (PPO) process was developed using radio frequency (RF) plasma in a plasma enhanced chemical vapor deposition (PECVD) chamber and demonstrated significant surface passivation. Various gases were investigated and 1% O_2/Ar was found to reduce the growth rate and provide excellent control over the degradation of EOT. A 100 W plasma with 1% O_2/Ar was found to provide the best combination of EOT and low D_{it} and is concluded to be the optimum process for PPO of germanium surfaces.

CV ACE and PPO were also utilized to investigate other process development challenges. A study of the impact of low temperature anneals on Ge-based MOS devices was found to result in a degradation of the electrical thickness and a change in fixed charge, indicating that the process window is very narrow and at much lower temperatures than for Si.

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CHAPTER 1

INTRODUCTION

1.1 Transistor

The transistor is the fundamental building block of modern electronics, in which there are millions of transistors working together to perform numerous operations every second. The transistor was first invented in 1947 at Bell Laboratories by W. Shockley and his colleagues [1]. The transistor demonstrated was a bipolar point contact transistor and was made from germanium. Despite being the first of its kind, the point contact transistor suffered from a delicate structural configuration and was unsuitable for high volume manufacturing. Shockley and Pearson subsequently designed a Bipolar Junction Transistor (BJT) which was superior than the point contact transistor in many aspects. This transistor was made in a single crystal of germanium and doped to a n-p-n structure. In this new design, Shockley and Pearson demonstrated a significant modulation of conductance at the top surface of the semiconductor by applying an electric field. This type of transistor was the dominant type of transistor before the widespread use of Field Effect Transistors (FET).

The concept of a field effect transistor (FET) was first introduced and patented by Julius Edgar Lilienfeld in 1926. However, at the time there was a lack of availability of necessary technology to produce a FET. Shortly after the invention of the BJT, it became possible to make a FET and soon different types of FETs were fabricated. The advancement in transistor research was accelerated by the invention of new and better methods of forming solid single crystal semiconductor materials, mostly silicon and germanium. The Czochralski method, zone refining and the float zone technique are the most notable in this regard and are still being used today.

Many types of FETs were theorized and eventually fabricated. The most common among them was the Junction FET (JFET), which was made from a reverse biased p-n junction and acts as a voltage controlled resistor. Even though the JFET was very good in many aspects, it was superseded by the Metal Oxide Semiconductor (MOS) FET in 1959, which has lower power consumption and is smaller in size.

1.2 MOSFET

A silicon based MOSFET was first demonstrated by Atalla and Kahng in 1959 at Bell Labs. The reason for using silicon in the MOSFET is to have a much higher quality gate oxide layer, which is thermally grown. This high quality silicon dioxide layer has much lower interface state density compared to other insulator-semiconductor interfaces. The interface states block the electric field penetrating into the semiconductor and degrade the performance of the device. A MOSFET is superior to the BJT in many aspects – including very low power consumption, ease of manufacturing, smaller size, and convenient scaling laws. As a result, the MOSFET is the dominant transistor structure in microchips that are used today.

In Fig. 1.1, a simplified structure of a nMOSFET is shown, where the substrate is p-type and the drain and source are made from n-type silicon. Drain and source regions may be heavily doped. The oxide layer has been historically comprised of only SiO_2. However, for recent advanced devices, the oxide layer has multiple layers of different oxides, SiO_2 and HfO_2. The metal layer historically was formed from highly-doped polycrystalline silicon. However, the gate metal in this case was still a semiconductor and thus could be depleted of carriers which then acted as a dielectric layer, reducing the inversion capacitance. As a result, drive current was degraded and so poly-silicon was replaced by metals or metal like materials, e.g., TaN, TiN. The metal, oxide, and semiconductor forms the critical stack for MOSFET operation.

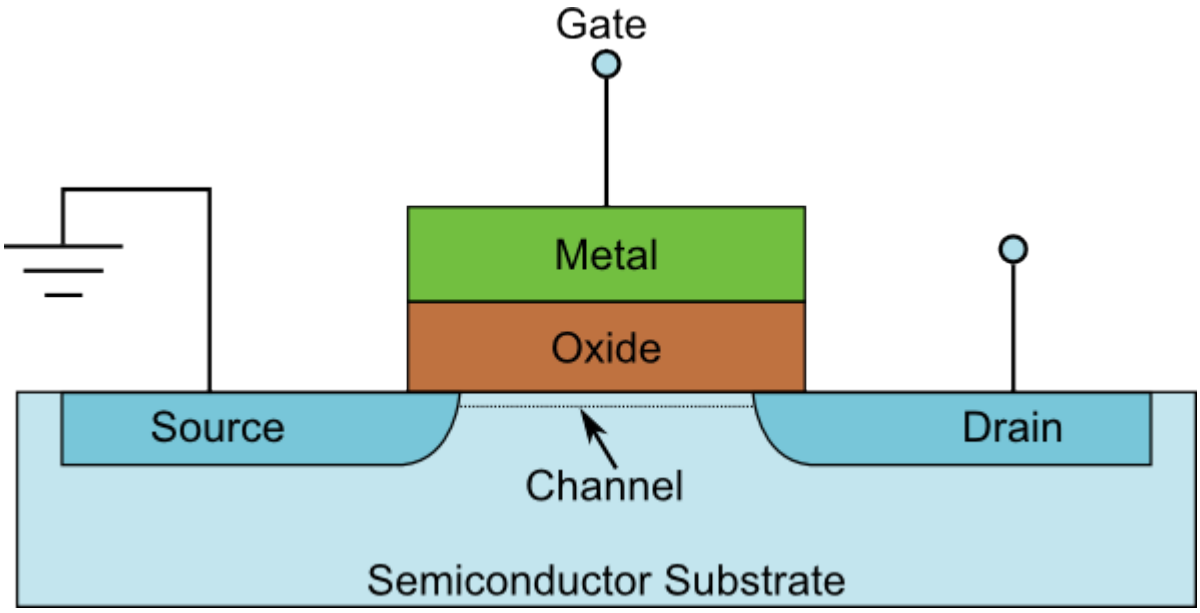


Figure 1.1. Basic structure of MOSFET

MOSFETs are generally four terminal devices – gate, body/bulk, drain, and source. Usually, the bulk/body of a MOSFET is directly connected to the source during fabrication, making it a three terminal device. In the body of the FET, the region connecting the source and drain terminal is called the channel region. By changing the bias on the gate, the electric field in the channel is varied, and this induced electric field controls the density of charge carriers in the channel, thereby controlling the current through the channel or through the MOSFET. So a MOSFET can be thought as a voltage controlled current source.

1.3 MOSFET Operating Principle

In a MOSFET, the voltage applied at the gate terminal controls the formation of the channel and hence the current flow through the device. Without a channel, no current flows through the device and the device can be said to be "OFF" and can be represented in binary as "0". With the presence of a channel, current can flow through the device and in that case, the device is considered "ON" or in binary "1". In this regard, a MOSFET can be thought of as a switch.

For a MOSFET, as shown in Fig. 1.1, the source terminal is connected to ground and a positive voltage is applied to the gate terminal with respect to the ground. For an nMOSFET, the substrate is p-type, which means that holes are the majority carrier type. By applying a positive voltage at the gate (V_g), an electric field is created from the gate to the substrate through the oxide layer. This field forces the holes to move away from the top surface. As a result, the top surface of the substrate becomes depleted of free carriers and is called the depletion layer. For a sufficiently high gate voltage, the electric field is so high that the top surface of the p-type semiconductor "pushes away" all the holes into the substrate and creates a thin layer dominated by electrons, the minority carrier, which are attracted to the top surface due to the electric field. As a result, the top surface of the p-type semiconductor becomes electron rich and acts as a n-type semiconductor and the device is "inverted". This thin layer of electrons (for a nMOSFET) is the channel, a two dimensional electron gas (2DEG) that carries electrons from source to drain if another positive voltage is applied to the drain terminal (V_D) with respect to the source terminal. As a result of the channel formation, the electrical current can flow from the drain terminal to the source terminal. This current is called the drive or drain current (I_D). If the device is not inverted, the source, substrate and drain form a n-p-n (for pMOSFETs p-n-p) junction, prohibiting any current flow through the device, even if a drain voltage is applied.

Initially, for a given gate voltage, the drain current increases linearly with an increase in the drain voltage. This region of operation of a MOSFET is called the linear region. Analytically, using the gradual channel approximation, the drive current in the linear region can be written as,

$$I_{\mathrm{D,lin}} = \frac{W}{L}\mu C_{\mathrm{ox}}[(V_g - V_t) - \frac{V_D}{2}]V_D \tag{1.1}$$

where, W and L are the physical gate width and length of the MOSFET respectively. μ is the carrier mobility of the semiconductor, C_{ox} is the capacitance of the gate dielectric and

V_t is the threshold voltage of the MOSFET, which indicates the minimum voltage necessary to turn on the device.

If the drain voltage is increased beyond the linear region, the drain current no longer increases linearly, eventually saturating at a maximum amount of current. The device is then in the saturation region and the drive current is given by,

$$I_{\mathrm{D,sat}} = \frac{W}{L}\mu C_{\mathrm{ox}}\frac{(V_g - V_t)^2}{2} \tag{1.2}$$

However, in practical devices, the drain current changes slightly with drain voltage i.e. it has a non-zero slope. The drain current in saturation is then calculated by,

$$I_{\mathrm{D,sat}} = \frac{W}{L}\mu C_{\mathrm{ox}}\frac{(V_g - V_t)^2}{2}(1 + \lambda V_D) \tag{1.3}$$

From these simple equations, it is obvious that, if everything else is fixed, by decreasing only the gate length (L), a higher drive current may be achieved. An important point to note here is that the actual gate length to be considered here is the physical distance between source and drain, rather than the length of the gate metal. An overlap between the gate metal and the source and drain regions is necessary for a continuous conducting path for the drive current. This overlap is usually designed to be very small to minimize the effect of parasitic capacitances.

An increase in oxide capacitance (C_{ox}) also increases the drive current. Physically, this oxide capacitance is increased by using a thinner dielectric layer (t_{ox}) and is calculated from the following:

$$C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}}\frac{WL}{t_{\mathrm{ox}}} \tag{1.4}$$

Decreasing the dielectric thickness has one major shortcoming. Gate leakage current increases with thinner dielectrics. One way to prevent that is to use a thin layer of SiO_2 and on top of it, another dielectric with a higher value dielectric constant (k). As a result, the

physical thickness of the dielectric stack is higher and so leakage current is lower for similar oxide capacitance. High-k dielectrics will be discussed later in section 1.5.

Another way of increasing the drive current is to increase the mobility of the carriers. However, as mobility is an inherent property of a semiconductor, it is difficult to increase electron or hole mobility for a given semiconductor. Strain engineering has been used to increase hole mobility and increase device performance. However, in modern MOSFETs, the channel length is much smaller ($\sim$10 nm) than the mean free path of carrier scattering ($\sim$65 nm). This indicates that the measured mobility from the so called long channel devices, with channel lengths in the μms, is overestimated in the modern day short channel devices. Even then, as shown by Lundstrom [2, 3], carrier mobility is an important factor in determining on current for short channel devices. However, as the device dimensions are further reduced and the carriers approach the ballistic limit, the significance of the mobility reduces.

1.4 Scaling

Compared to other types of transistors, MOSFETS are small in size, require very low power and are easy to mass manufacture. As a result, microchips were very cheap to manufacture and started the revolution of digital electronics. To continue progress in this technology, scaling is important to further reduce the size of the MOSFETs so that more devices can be put in a given area, thereby increasing performance and decreasing price. There are many advantages and a few disadvantages of scaling. Two of the important properties of transistors that are associated with scaling are the switching delay and energy consumption,

$$\text{switching delay} = \frac{CV_{\text{DD}}}{I_{\text{D,sat}}} \tag{1.5}$$

and,

$$\text{energy consumption} = CV_{\text{DD}}^2 \tag{1.6}$$

where, C is the total capacitive load of the MOSFET and V_{DD} is the supply voltage.

For better understanding, the "energy-delay product" is used, which is an important figure of merit associated with scaling,

$$\text{Energy delay product} = \frac{C^2 V_{\text{DD}}^3}{I_{\text{D,sat}}} \tag{1.7}$$

In an ideal case, the energy-delay product should decrease with a decrease in the device dimensions. In his famous paper, Dennard [4] showed that the device parameters for a MOSFET should scale approximately proportionally to keep the power density constant.

1.5 High-k Dielectrics

Scaling involves a reduction in the gate dielectric thickness. One downside of decreasing the gate dielectric thickness is an increase in tunneling current through the dielectric. A semi-empirical model for tunneling current density through the dielectric is given in [5],

$$J_{\text{tunneling}} = \frac{q^2}{8\pi h \epsilon \Phi_{b,i}} C(V_G, V, t_{\text{phys}}, \Phi_{b,i}) exp\left\{ \frac{8\pi\sqrt{2m_{\text{eff,i}}}(q\Phi_{b,i})^{3/2}}{2hq \mid E \mid} [1 - (1 - \frac{\mid V \mid}{\Phi_{b,i}})^{3/2}] \right\} \tag{1.8}$$

where, q is the electron charge, h is the Planck's constant, ϵ is the dielectric permittivity, t_{phys} is the physical thickness of the gate dielectric, $\Phi_{b,i}$ is the tunneling barrier height in eV, $m_{\text{eff,i}}$ is the carrier effective mass in the dielectric, V is the voltage across the dielectric, and E is the electric field in the dielectric. From (1.8), it can be seen that with everything else constant, the tunneling current density would be dependent on the physical thickness of the dielectric. For example, at a SiO_2 thickness of 1.2 nm, the leakage current density would be around $10^3 A/cm^2$. This very large leakage current would increase the idle power consumption of the MOSFET tremendously. So increasing the dielectric thickness would decrease gate capacitance and decreasing the dielectric thickness would increase leakage current, both of which are detrimental to the device.

To solve this issue, the use of dielectrics with higher dielectric constant were proposed [6] to use in conjunction with SiO_2. In this way, the physical thickness of the dielectric layer

will be higher and the leakage current will be lower. At the same time, because of the higher dielectric constant, the gate capacitance may be higher. For convenience, the thickness of the high-k dielectric used is converted to an equivalent thickness of SiO_2 by,

$$EOT = t_{\mathrm{high-k}}\Big(\frac{k_{\mathrm{SiO_2}}}{k_{\mathrm{high-k}}}\Big) \tag{1.9}$$

If the high-k dielectric is used on top of SiO_2, the EOT of the high-k dielectric can be added to the physical thickness of the SiO_2 layer and be approximated as a single SiO_2 layer. However, in practice, there may be fixed charges and defects in the dielectric due to deposition techniques used. At the same time, the dielectric material needs to be thermodynamically stable, so as to not react with silicon. If the dielectric material reacts with silicon and forms more SiO_2, the total EOT of the device will be degraded and if it forms a silicide, the gate terminal may be shorted to the substrate, both of which are undesirable for device performance.

One advantage of SiO_2 is that it is usually grown by high temperature thermal oxidation of the silicon substrate itself. This process is well studied and well understood. High-k dielectrics, on the other hand, must be deposited. Many deposition methods have been researched. Sputtering is a physical deposition process that it is widely available and is able to produce stoichiometric oxides. However, as this process involves plasma and the material is an insulator, deposited dielectrics often have plasma induced damage. Additionally, as this is a "line of sight" process, conformality is a major issue for advanced devices with complex structures such as the FinFET.

Another method is to deposit a thin layer of a metal using electron beam evaporation and use ozone or other oxidizers to form metal oxides. Chemical vapor deposition (CVD) may also be employed for deposition of the high-k dielectric, where a volatile metal compound is used as a precursor. This precursor is introduced into the CVD chamber, where the substrate resides, and oxidized using oxygen balanced in a neutral gas or water vapor. The

Table 1.1. Material properties of different important semiconductors

Parameter	Si	Ge	SiGe			GaAs	InGaAs	
x	-	-	0.5	0.6	0.75	-	0.2	0.53
ϵ_s	11.7	16.2	13.95	13.5	12.83	12.90	13.23	13.9
χ_s	4.05	4.00	4.05	4.05	4.05	4.07	4.24	4.51
E_g	1.12	0.66	0.92	0.96	1.02	1.42	1.14	0.75
m_e	1.08	0.56	1.06	1.06	1.06	0.063	0.055	0.041
m_h	0.81	0.34	0.58	0.62	0.63	0.51	0.49	0.46
μ_e	1400	3900	-	-	-	9200	6900	13000
μ_h	450	1900	-	-	-	400	300	450

advantage of this method is that CVD is widely used in the semiconductor industry, the deposition of the dielectric is conformal, and the deposition rate is highly controllable. The most preferred and widely used method is atomic layer deposition(ALD), which is a cyclic, self-limiting deposition method. This technique is described in more detail in chapter 2, as it is used extensively in this dissertation.

1.6 Alternative Channel Materials

For advanced MOSFETs, higher drive current may be achieved with a semiconductor material which has a higher bulk carrier mobility compared to silicon. In table 1.1, the electron and hole mobilities, among other properties for various semiconductors are shown.

From the previous discussion, it can be noted that for highly scaled devices, mobility is not as significant as in long channel devices. However, from table 1.1, it can be seen that the bulk electron mobility of other materials can be around 10 times higher compared to silicon and the hole mobility can be around four times higher. As a result, a significant increase in drive current and subsequent device performance can still be expected from these short channel devices made of alternative channel materials. The electron and hole mobilities in germanium, for example, are about two and four times higher, respectively,

compared to silicon which makes germanium a very promising potential channel replacement. In fact, germanium is already being used in the industry for strain engineering in silicon based devices. This makes it easier for the semiconductor industry to move from silicon to germanium instead of silicon to III-V materials.

To implement these high mobility alternative channel materials into advanced and highly scaled devices, some major issues need to be solved. The high mobility materials suffer from lower allowable thermal budgets compared to Si (before desorption and defect formation becomes an issue) and the absence of a good quality native oxide. For example, germanium has a native oxide (GeO_2) similar to silicon. However, the GeO_2 is well known to be hygroscopic, highly soluble in water, and thermally instable. Similar to silicon oxide, germanium oxide has very good passivating characteristics [7]. But because of GeO_2's solubility in water, integrating germanium oxide with high-k dielectrics is challenging. The ALD processes, necessary for scaled high-k dielectric deposition in FinFETs, utilize de-ionized water (DIW) as an oxidizing agent, which damages and partially etches the germanium oxide layer. Many attempts have been made to solve the issues with the Ge:GeO_2 interface [8, 9, 10, 11, 12]. The most promising of these is the post ALD plasma oxidation. In this method, a high-k dielectric layer, typically Al_2O_3, is deposited on top of cleaned germanium surface using ALD. The germanium surface is then oxidized, through the high-k, by exposing the sample to an oxygen based plasma ambient. The oxygen permeability of Al_2O_3 is just high enough so that the oxygen ions can pass through the dielectric layer and oxidize the germanium surface. The advantage of this method is that the germanium oxide needed to electrically passivate the germanium surface is not damaged as it is formed after the high-k dielectric deposition. In this way, both GeO_2 and high-k dielectrics may be integrated into the device process flow. This method has shown excellent interface state properties and high mobility in long channel devices.

III-V compound semiconductors are, of course, comprised of materials from group III and group V of the periodic table which individually are metals. However, when they are

made into a solid solution, they form a semiconductor. As a result, the structure of III-V materials is more complex compared to Si, Ge, or even SiGe. As a result of its inherent nature, it is hard to define a native oxide for III-V semiconductors. It has been reported that Ga_2O_3 in GaAs has very good electrical characteristics [13, 14] while later reports correlated Ga_2O_3 to poor device performance [15]. There have been similar discrepancies regarding the role of As-oxides on device performance [16]. The lack of a good quality native oxide means that the high-k dielectrics are needed to be put directly of top of the III-V semiconductor. Many high-k dielectrics have been demonstrated on III-V semiconductors, for example ALD Al_2O_3 [17], HfO_2 [18], HfAlO [19], and ZrO_2 [20]. However, the interface of those dielectrics with the III-V semiconductors are not atomically abrupt, resulting in a thin disordered region at the interface [21, 22]. This disordered region causes carriers to tunnel through the region into III-V related defects and oxide related border traps, resulting in anomalous C-V characteristics. The wide range of available high-k dielectrics and III-V semiconductors result in a wide variety of semiconductor-dielectric interface combinations, which are difficult to analyze using a singular methodology.

III-V semiconductors are also different than Si, Ge, and SiGe in band structure. III-V semiconductors are direct band-gap materials and they have higher electron mobility. But this comes at a cost of having a lower electron effective mass (which will be discussed later) as shown in Table 1.1 and consequently have about an order of magnitude lower conduction and valence band density of states compared to group IV materials. In addition, the conduction band of III-V materials is highly non-parabolic, resulting in a different carrier density profile with respect to potential than if the conduction band is assumed to be parabolic.

1.7 Semiconductor/Dielectric Interface Analysis

The semiconductor/dielectric interface is of utmost importance for proper device operation. The high electrical quality of the $Si:SiO_2$ interface was one of the major advantages of using

silicon as a semiconductor. The interface is one of the best that nature has produced in terms of defect density. The interface is atomically abrupt with few defect sites and there are almost no dangling bonds, especially after hydrogen passivation. Electrically active defects give rise to states the resides energetically inside the band-gap of the semiconductor which can trap free carriers. Typically, they are sites of either impurities or oxygen deficit or excess oxygen. These defects can either be at the interface or in the dielectric layer and degrade device performance. There are four main disadvantages of these electrically active defects:

1. Scattering of carriers in the channel reduces the carrier mobility
2. Carriers trapped in the defects change the threshold voltage
3. Certain defects allow tunnelling of carriers through the dielectric
4. The defects degrade device reliability as they are the point of origin for dielectric breakdown

Therefore, it is obviously necessary to have a high quality semiconductor/dielectric interface with minimal defects. However, significant challenges are needed to be overcome before alternative channel materials are widely used in the industry. One of the biggest challenges is a detailed understanding of these interfaces and their impact on device performance. Because Si has been the industry standard for decades most of the analytical methods developed to understand interfaces were based on silicon. But many of those analysis techniques are not applicable to III-V devices. Consequently, there is no singular methodology available to analyze all semiconductor-dielectric interfaces possible for advanced device fabrication, and the community is divided on what technique to use for analysis of the alternative channel interfaces.

1.8 MOSCAP

The MOSFET is quite complex to make, often requiring hundreds of steps to fully fabricate. As a result, when MOSFET characteristics deviate from ideal behavior, it is hard to determine precisely where in the process flow the problem lies; is it a poor semiconductor/dielectric interface or some other issue elsewhere in the processing? As a result, using MOSFETs to develop process flows to obtain semiconductor/dielectric interfaces with excellent electrical characteristics would be highly time consuming, inefficient, and very expensive. MOS capacitors (MOSCAPs) are essentially the gate structure of a MOSFET and can therefore be used to understand the properties of the MOSFET gate including the semiconductor/high-k interface.

MOS capacitors do not require long and complex fabrication steps and the electrical characteristics of a MOSCAP are primarily dependent on the semiconductor/dielectric interface. As a result, using the MOS capacitor structure to investigate the interface and develop processes to achieve high quality dielectrics and interfaces is highly efficient, with very short turn-around time, making MOSCAP analysis relatively inexpensive compared to a full MOSFET flow in terms of man hours and materials.

In Fig. 1.2, a simple MOSCAP structure is shown, which is part of a fully fabricated MOSFET structure shown in Fig. 1.1. This MOSCAP can be easily fabricated using the simple process flow shown in Fig. 1.3. The process steps are:

1. A wafer or a piece of wafer is selected and cleaned.

2. Dielectric is deposited on top of the cleaned wafer. The deposition process might be ALD, CVD, or any other deposition process.

3. Metal is deposited on top of the dielectric. The metal may be deposited by sputtering, thermal evaporation, e-beam evaporation, or ALD.

4. Photoresist is spin coated on top of the metal. Then using an appropriate lithography mask, the sample is exposed to UV light. The resist is developed to form the MOSCAP.

5. Metal and dielectric layers are removed from the exposed areas using wet or dry etch techniques, leaving the metal and dielectric under the resist in the MOSCAP structure.

6. Residual resist is removed by a solvent and/or oxygen plasma.

7. A metal back contact is deposited to reduce series resistance (not shown in Fig. 1.2.)

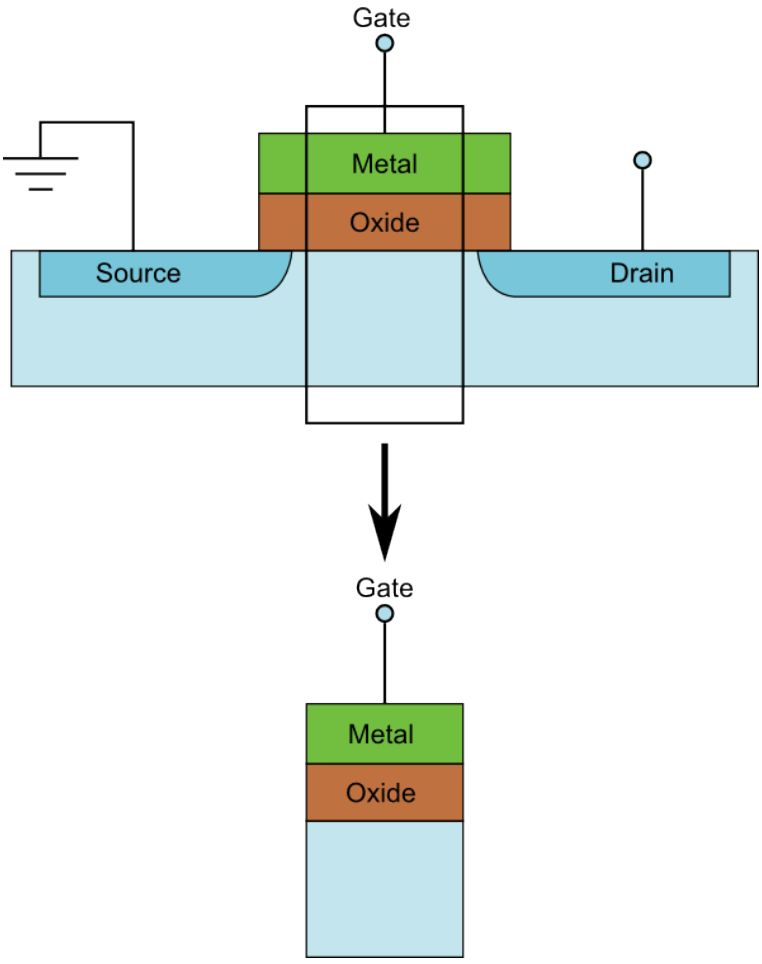


Figure 1.2. Basic structure of MOSCAP

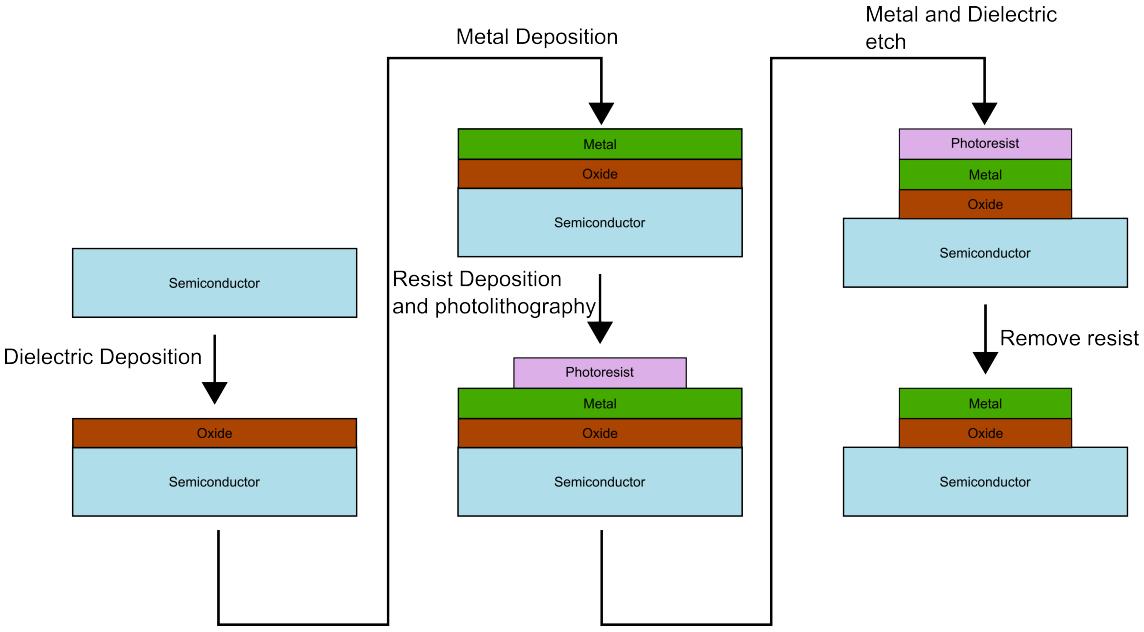


Figure 1.3. MOSCAP fabrication process flow

Another advantage of using the MOSCAP for research and development is that MOSCAPs can be characterized by a combination of electrical and physical characterization techniques much more easily than a complex MOSFET.

1.9 Problem Statement

There is a lack of proper models and software tools available to analyze the semiconductor/dielectric interface and to accurately extract parameters of advanced devices fabricated from alternative channel materials and high-k dielectrics. This dissertation addresses this deficiency by developing the models and a software tool that takes into account all the effects that are present in alternative channel materials and high-k dielectrics.

We then utilize this new tool to assess one of these alternative channel materials, germanium, that shows tremendous potential to be used in future MOS devices but lacks a good interface. A process flow is developed to properly passivate the germanium surface to make it suitable for device fabrication and the devices are analyzed using the program developed.

In addition, for total control over germanium based MOS devices, effective work function (EWF) tuning is needed. To achieve this, low temperature anneals in different ambients have been performed to show the effect on the work function of these germanium based devices.

1.10 Dissertation Overview

The dissertation is divided into following chapters-

1. Chapter 2: For proper process flow development, a deep understanding behind the operating principles of various semiconductor processing tools are needed. Additionally, surface characterization is paramount for semiconductor-dielectric interface analysis. For fabricated device characterization, a wide knowledge and understanding of the parameters that control the characteristics of the semiconductor-dielectric interface are needed. In this chapter, the operating principles of semiconductor processing tools that are used in this dissertation are explained. Surface characterization using XPS and the theory behind it is described. And finally, the theory behind C-V analysis from a fabricated MOSCAP is presented along with the tools used to measure the C-V profile from fabricated devices.

2. Chapter 3: Various alternative channel materials are being considered to replace silicon in advanced MOS devices. As a result, new semiconductor/dielectric interfaces are needed to be analyzed. However, the tools developed for silicon based devices are not accurate for other semiconductor materials. Also for advanced devices, quantum mechanical effects and, especially for III-V materials, nonparabolicity of the conduction band makes it difficult to properly analyze the interface and extract device parameters from measured C-V data. In this chapter, a quantum mechanically corrected C-V model is proposed and validated for various alternative channel materials with high-k

gate dielectrics. The model is implemented in a computer program called CV Alternative Channel Extraction (CV ACE), developed in C++ programming language, which can be used to simulate and extract device parameters from measured C-V data for a variety of semiconductors and dielectrics. Analysis of the measured experimental C-V data for various semiconductors will be presented and compared with existing models.

3. Chapter 4: In order to passivate the germanium channel for high performance advanced MOS devices, many different methods have been reported. Post ALD plasma oxidation is one of the most promising methods. In this chapter, a process is developed to passivate the germanium interface using a plasma enhanced CVD based oxygen plasma after ALD of high-k dielectrics. The effect of plasma composition, power, chamber pressure, oxidation time, and forming gas anneal at different temperatures will be discussed, and the resultant devices analyzed with the proper models and tools developed in chapter 2 (CV ACE).

4. Chapter 5: Effective work function (EWF) tuning in Ge devices is essential to enable high-performance CMOS devices. A simple anneal in different environments has been shown to affect the EWF of HfO_2/TiN on silicon based devices. In this chapter, a similar process is implemented on germanium based devices. This process is shown to have a different thermal budget on Ge compared to silicon and as a result, requires careful and fine control over the temperatures and background environment. CV ACE is again used to analyze the process development for degradation in EOT and D_{it} as well as changes to the EWF.

5. Chapter 6: In this chapter, a summary of this dissertation along with future work suggestions are presented.

CHAPTER 2

EXPERIMENTAL METHODS AND TECHNIQUES

2.1 Introduction

The primary objective of this research is to accelerate the process development of next generation high-k/high mobility substrate interfaces. To achieve this objective, a C-V simulation and analysis tool is required, which can extract important device parameters taking quantum mechanical effects and others into account. To develop this tool, a solid understanding of C-V analysis and semiconductor dielectric interfaces is necessary. At the same time, process development requires a good knowledge of how the thin film deposition process and the tools themselves work. Combining the fundamental knowledge and understanding of semiconductor physics, process tools and materials characterization is critical to the development of fabrication processes for next generation MOS devices. In this section the theory and applications of the various fabrication and characterization methods will be outlined. The specific experimental details of the tools used will also be described.

2.2 Atomic Layer Deposition

Atomic layer deposition (ALD) [23, 24, 25] is a thin film deposition method based on chemical vapor deposition (CVD). CVD is a process where thin films are deposited from a gaseous state (vapor) to a solid state on the substrate. In this process, one or more volatile gaseous precursors are used, which react or decompose on the substrate surface, depositing the solid material. As this reaction/decomposition typically occurs at high temperatures and in a sealed chamber free from contaminants, the films deposited are very high quality. Obviously, the parameters of the deposition process, e.g., chamber pressure, temperature, or time need

to be tuned to deposit the highest quality films. Due to the purity, controllability, and versatility of this process it is widely employed in the semiconductor industry, primarily for dielectric deposition.

The reaction in a CVD process can be described using the following equation,

$$A(g) + B(g) = AB(s) \tag{2.1}$$

The major difference between ALD and other CVD methods is that in ALD, the precursors are not present in the reaction chamber simultaneously, they are injected sequentially one after another, with a pumping step in between each to remove any remaining precursor which has not reacted with the target substrate. In this way, the reactions of the precursors are divided into two parts. Each part is self-limiting and they react only on the surface of the target substrate. After these two half-reactions are complete a monolayer of stable material is deposited on the substrate. This is shown in Fig. 2.1.

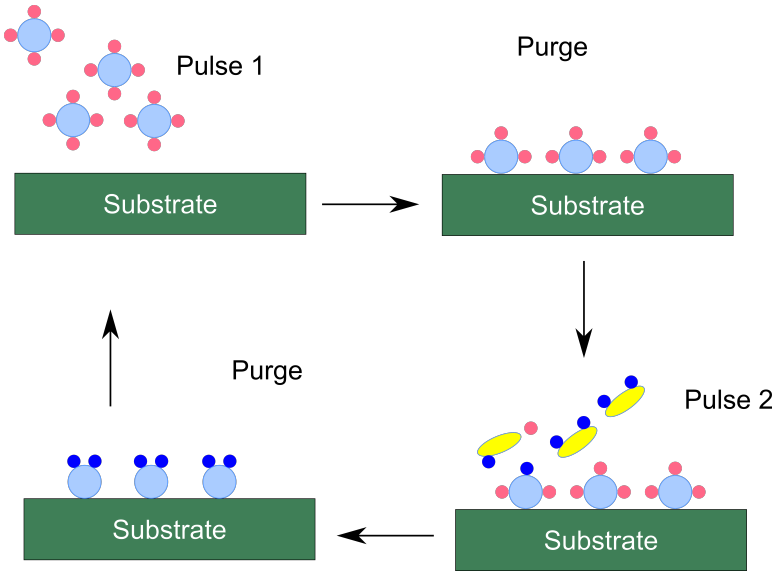


Figure 2.1. Atomic layer deposition process

The chemical reaction can be expressed using the following equation

First half-reaction:

$$AX(g) + Z(s) = AZ(s) + X(g) \tag{2.2}$$

Second half-reaction:

$$AZ(s) + BY(g) = AB(s) + Y(g) \tag{2.3}$$

where, AX and BY are the chemical precursors and Z is the substrate.

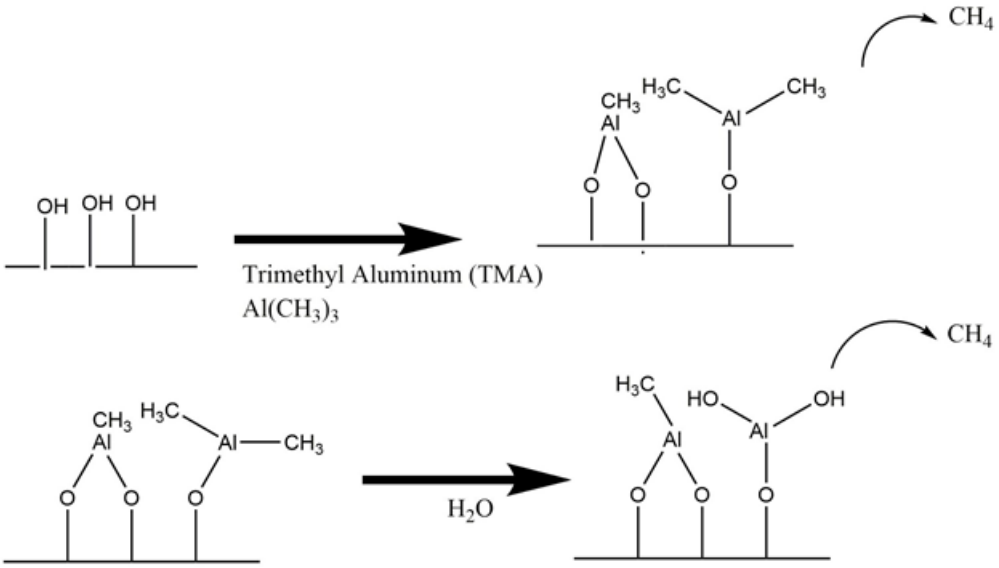


Figure 2.2. Atomic layer deposition process [26]

For HfO_2 deposition, TDMA-Hf heated to 75°C is used as a precursor and DIW is used as the oxidizer. The TDMA-Hf reacts with water and forms HfO_2 on the substrate and hydrogen is produced as a by-product which is pumped out during the purge cycle. A basic setup of an ALD tool is shown in Fig. 2.3. In a typical ALD tool, there may be a number of precursors connected to the manifold, through which the choice of precursor, and consequently the material deposited can be selected. The manifold is connected to the deposition chamber, where a target substrate is placed. The precursor is supplied to the chamber through the manifold in a brief pulse, where a valve is opened for a very small amount of time, usually on the order of milliseconds. The purge line of the chamber is connected to a pump which keeps the chamber under vacuum to minimize contaminants. Due to the vacuum inside the ALD chamber, when the valve of precursor opens, a vapor of the precursor escapes through the manifold into the deposition chamber coating the substrate. The excess precursor is

pumped out through the purge line by the vacuum pump. Next, the valve of the oxidizer is opened, again for a short period of time so that the water vapor can be pulled through the manifold and into the chamber, oxidizing the precursor absorbed on the substrate and forming a monolayer of the desired material.

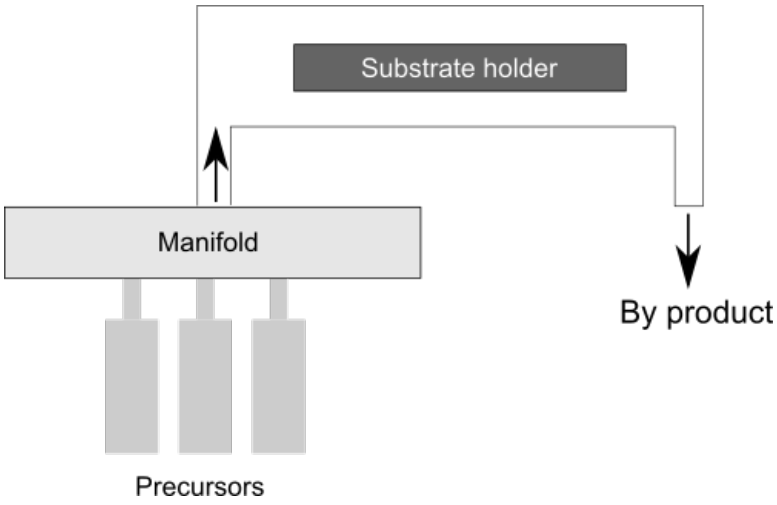


Figure 2.3. Basic structure of a ALD tool

There are many advantages of ALD:

1. Excellent adhesion – can be deposited on almost any substrate
2. Self-saturating reactions with surface
3. Low temperature and low stress
4. Excellent control of the film thickness
5. Excellent conformality, excellent coverage of 3D structures
6. Large area thickness uniformity and scalability
7. Gentle deposition process for sensitive substrates
8. Simple operating procedure

9. Chemistry and mechanism is well understood
10. Low temperature, low energy process

However, there are some limitations of ALD:

1. Not every material can be achieved
2. Precursors may react with the substrate
3. Precursors may be expensive
4. Precursor is wasted during the purge step
5. Conformal coating may require significant cycle time

2.3 Plasma Enhanced Chemical Vapor Deposition

Plasma Enhanced CVD is another variant of the typical CVD process where the decomposition rate of the precursor or the reaction rate between multiple precursors are increased by inducing a plasma inside the deposition chamber. A plasma is a gas or a mixture of gases, where a significant portion of the gas is ionized. In a plasma, the energy exchange between the neutral atoms of the gas and the electrons is very inefficient. The reason for this inefficiency is the orders of magnitude difference in mass between atoms and electrons. As a result of this highly inefficient energy transfer, electrons can have very high energy or very high equivalent temperatures, compared to the neutral atoms which remain at room temperature. Consequently, these high energy electrons drive the processes and reactions necessary for the deposition of thin films, which would otherwise be improbable at lower temperatures. The reactions or the dissociation of precursors is also helped by the increased number of free radicals in the plasma. The result of the addition of plasma into the CVD

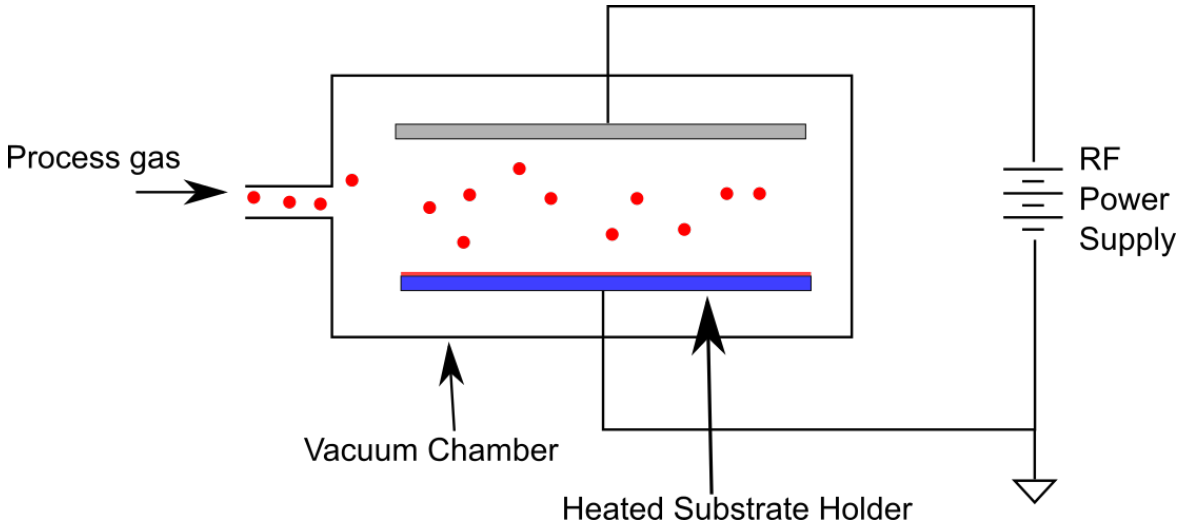


Figure 2.4. PECVD basic diagram

process is an increased deposition rate and low temperature deposition, while maintaining the electrical and mechanical properties of the deposited material.

There are many different types of PECVD. The most common and widely used is with a capacitive plasma, which is shown in Fig. 2.4, where two parallel plates are placed inside the PECVD chamber. By applying a RF voltage between two electrodes the plasma is generated. Usually, there are pin holes in the top electrode through which the process gas flows into the chamber. The bottom electrode serves as a wafer holder and can be heated through a heater. Typically, after the sample substrate is put onto the bottom plate, the chamber is evacuated using a vacuum pump and then flushed with an ultra high purity neutral gas – N2 or Ar. After making sure that all of the contaminants are removed, the process gas is used to flush the chamber to remove the neutral gas. After that the process gas flow is stabilized, a RF voltage is applied between the conductors to ignite the plasma and start the deposition process. After the deposition is complete, the chamber is again flushed with the neutral gas to remove the potentially toxic process gas. The chamber is then vented and the sample is removed from the PECVD. In this work, a PECVD tool, Unaxis 790, shown in Fig. 2.5, is used to passivate the germanium surface for advanced MOS device applications.

Instead of deposition, in the PPO method, the PECVD tool is used to generate oxygen ions that diffuse through the pre-deposited dielectric layers, to oxidize the high-k/Ge interface in a very controlled fashion. In the tool, the plasma is generated through a 13.56 MHz radio frequency (RF) plasma generator. In this work, the process time and pressure along with three different gases (N_2O , 25% O_2/Ar and 1% O_2/Ar) were investigated to passivate the germanium surface.

Figure 2.5. PECVD tool used in this work

Advantages of PECVD include,

1. Conformal coverage
2. Can be used with temperature sensitive substrates
3. Fast deposition rates

4. Good film quality

5. A low density plasma reduces substrate damage.

The disadvantages of PECVD are,

1. A high density plasma can damage substrates

2. Some materials may be sensitive to plasma

3. Silicon oxide and silicon nitride films deposited in this method contains a significant amount of contaminants

4. Not all materials can be deposited

2.4 Sputter Deposition

Sputter deposition is a physical vapor deposition (PVD) process for thin film depositions widely used in the semiconductor industry. This process involves the sputtering of a target material, which means bombarding the target with a heavy molecules to physically eject material from the target which then deposits on the substrate. Target materials ejected by this process have a wide kinetic energy distribution range. The ejected atoms may have enough kinetic energy to ballistically damage the substrate during the deposition. However, at higher sputtering gas pressures, the ejected atoms may collide with these gas atoms and lose kinetic energy. For pure metal deposition an inert gas such as Ar, Xe etc. can be used. Compound materials can be deposited using a sputter process, where along with the neutral gas, a reactive gas is simultaneously inserted into the chamber. In this way, reaction between the ejected material and reactive gas occurs in the chamber before reaching the substrate surface. With many parameters available to control the process, sputtering is a complex process. At the same time, it allows a large degree of freedom and control over the deposition

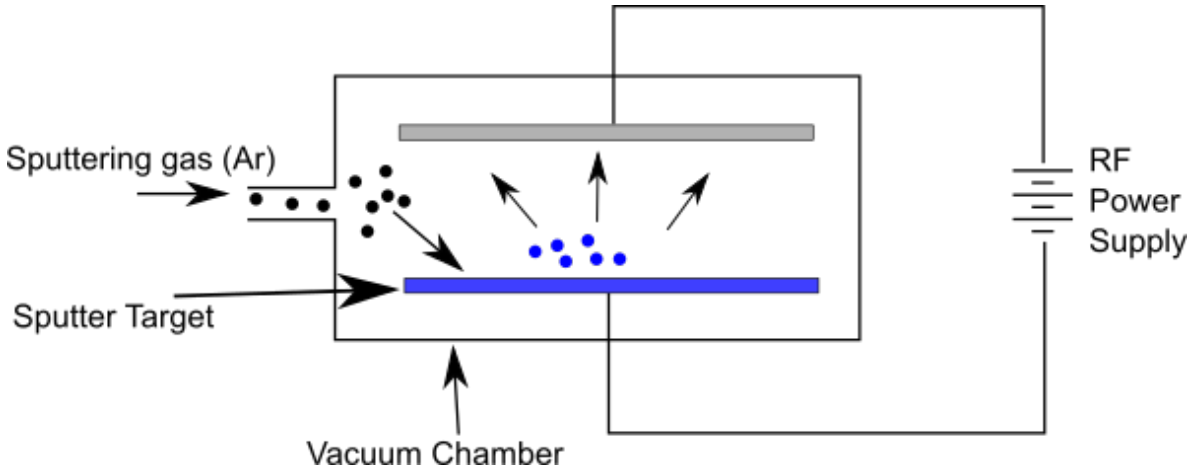


Figure 2.6. The sputtering process

of thin films. In Fig. 2.6, a basic diagram of a sputtering chamber is shown. The bottom plate, is the target material that is to be deposited on the substrate, put on the top plate facing down. The target material is usually a high purity (greater than 99.9999%) metal, which is put into a special enclosure to limit and focus the plasma onto the target. Sputtering is typically performed in vacuum to reduce contaminants. After the substrate is loaded into the chamber, a neutral sputtering gas, typically Ar, is introduced into the chamber. A plasma is then generated and directed onto the sputtering target in the enclosure, where the neutral Ar atoms are ionized and hit the target metal, ejecting metal atoms. The plasma can either be a DC or RF plasma. This is a line of sight method of deposition. However, by changing the deposition angle, good sidewall coverage may be achieved. In this work, a sputter deposition tool manufactured by the AJA international model 1500-V, shown in Fig. 2.7, is used to deposit TiN using reactive sputtering. W cladding and Ti+Al back contacts are also deposited with this tool.

Advantages of sputtering include,

1. Highly controllable

2. Good uniformity and high quality films

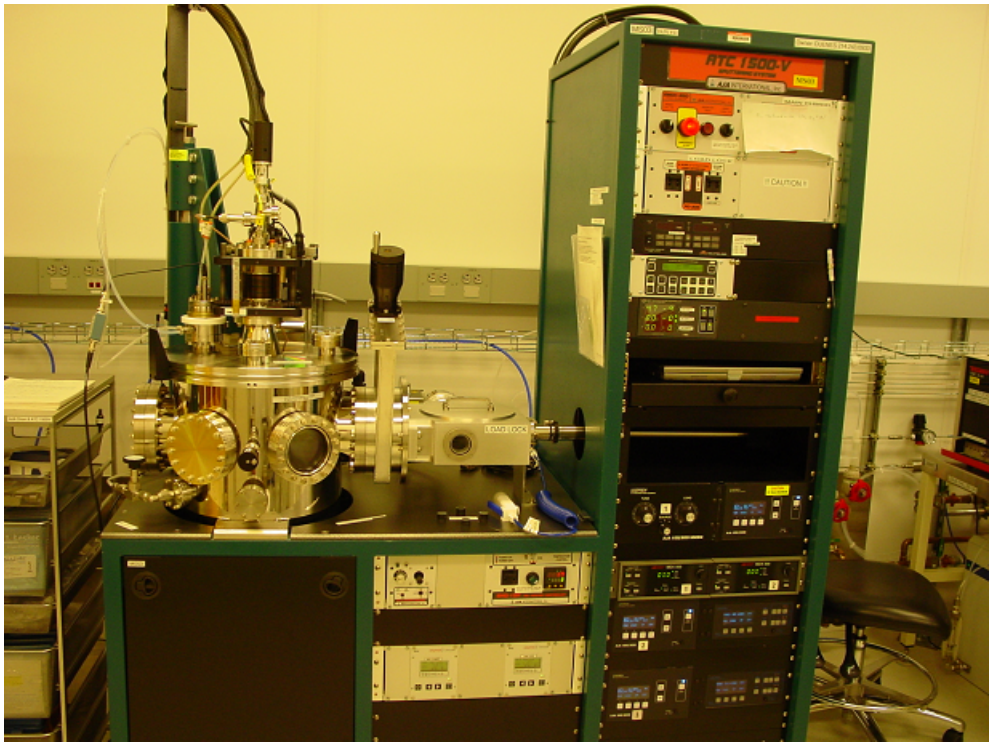


Figure 2.7. The sputter tool in the UTD cleanroom

3. Highly repeatable

4. Reactive sputtering can produce some unique materials unattainable through other methods

5. Wide range of materials can be deposited

6. Wide range of control over many different aspects of the deposition process

The disadvantages of sputtering are,

1. Line of sight is required

2. Non-conformal coverage

3. High energy target atoms can damage the substrate

2.5 X-ray Photoelectron Spectroscopy

X-ray Photoelectron Spectroscopy (XPS) is a material characterization technique [27, 28, 29, 30] based on the photoelectric effect [31, 32]. In this effect, when light is incident upon a material, electrons are excited from their core levels and ejected from the material. Electrons generated or emitted in this manner are called photoelectrons. However, incident light upon a material does not always emit electrons. In the photoelectric effect, one of the three following events occurs:

1. The photons do not interact with the material and pass straight through. In this case, the material is said to be transparent to the incident light.

2. The photons in the light may interact with an electron in the material and pass all of their energy to that electron causing it to be emitted from its core level.

3. The light scatters away after interaction with the material.

The basis of the XPS lies in the second phenomena, where the emitted electrons are measured as a function of their kinetic energy. However, no electron will be emitted unless the energy of the photons in the incident light is greater than a characteristic threshold energy known as the binding energy (BE), which is specific to the core level in which the electron resides. If the incident photons have kinetic energy which exceeds this threshold energy the electron is emitted and the kinetic energy (KE) of the electron is related to the energy of the photons. This relationship is described by Einstein in his famous work [32] as,

$$BE = E_{\text{incident}} - KE \tag{2.4}$$

where,

$E_{\text{incident}} = h\nu$

h is Planck's constant $= 6.63 \times 10^{-34} m^2 kg/s$

and ν is the frequency of the incident light.

The binding energy of a certain core level is determined by the atomic structure of the element. In an atom, an electron, which is negatively charged, is attracted to the nucleus, which consists of a proton (positively charged) and neutron (charge neutral). The smaller the atom, the closer the electrons are to the nucleus, and the higher this attraction and thus the BE is. As a result, every element has a different set of characteristic binding energies at which the electrons are ejected. For example, in this report we are focusing on germanium, which has an atomic number of 32 and has an electronic configuration of $1s^2 2s^2 2p^6 3s^2 3p^6 3d^1 04s^2 4p^2$. Consequently, it might be expected that from the electronic configuration that electrons are emitted in wide range of binding energies. In practice, however, the photon source does not have enough energy to excite and emit electrons from every core level. As a result, in conventional XPS (with a photon energy of 1486.7 eV from the x-rays generated by an Al anode), peaks up to and including the Ge $2p$ can be excited, but the BE of the $2s$ and $2p$ peaks are too high.

From the energy range of the electrons detected and measured in an XPS system, the material under inspection can easily be interrogated. In this way, the binding energy associated with a material can be thought of as a finger print by which the material can be identified. The binding energy is calculated from the kinetic energy of the electrons detected, using (2.4). However, in a practical XPS system, the detector has a work function which must be included into calculation of the binding energy. So (2.4) is modified to the following,

$$BE = E_{\text{incident}} - KE + \phi_{\text{spect}} \tag{2.5}$$

where, ϕ_{spect} is the work function of the material in the spectrometer.

The photons used in XPS penetrate deeply into the sample (on the order of microns). However, the depth from which the photoelectrons can escape is much lower. Unlike photons, electrons interact with the other atoms in the sample as they are emitted, and this interaction can lead to scattering and a loss of kinetic energy. This interaction limits the escape depth

of the photoelectrons to 5-7 nm into the sample, depending on the specific material. As a result, XPS is usually used for the investigation of the surface rather than the bulk of a material.

XPS is primarily used to analyze the chemical composition of a sample. When a sample is inspected using XPS, the number of electrons detected are plotted against the BE. Using specialist peak fitting software the area of the core level peak can be extracted, which is proportional to the concentration of that element present in the sample being measured. This fitted area of each core level is weighted by their respective sensitivity factors and then used to obtain the surface composition.

For XPS analysis in this report, a monochromatic x-ray source (line width = 0.25 eV) and a 125 mm hemispherical analyzer equipped with 7 channel detectors were used. The setup is shown in Fig. 2.8. A pass energy of 15 eV is used in combination with a photon energy of 1486.7 eV generated by Al Kα x-rays. Binding energy calibration is performed using the adventitious C 1s peak at 284.8 eV.

2.6 Capacitance Voltage

MOSCAPs are similar to parallel plate capacitors [33, 34, 35] where the top plate is the metal gate and bottom plate is the semiconductor. Even though in practice there is a metal contact at the back of the semiconductor, because of the wide area and very low thickness of the semiconductor in actual devices, the bulk of the semiconductor material can act as the bottom plate when charge builds up at the semiconductor/dielectric interface. The capacitance measured is the small signal capacitance calculated from the change in charge with respect to the change in gate voltage:

$$C = \frac{dQ_g}{dV_{gb}} = -\frac{dQ_s}{dV_{gb}} \tag{2.6}$$

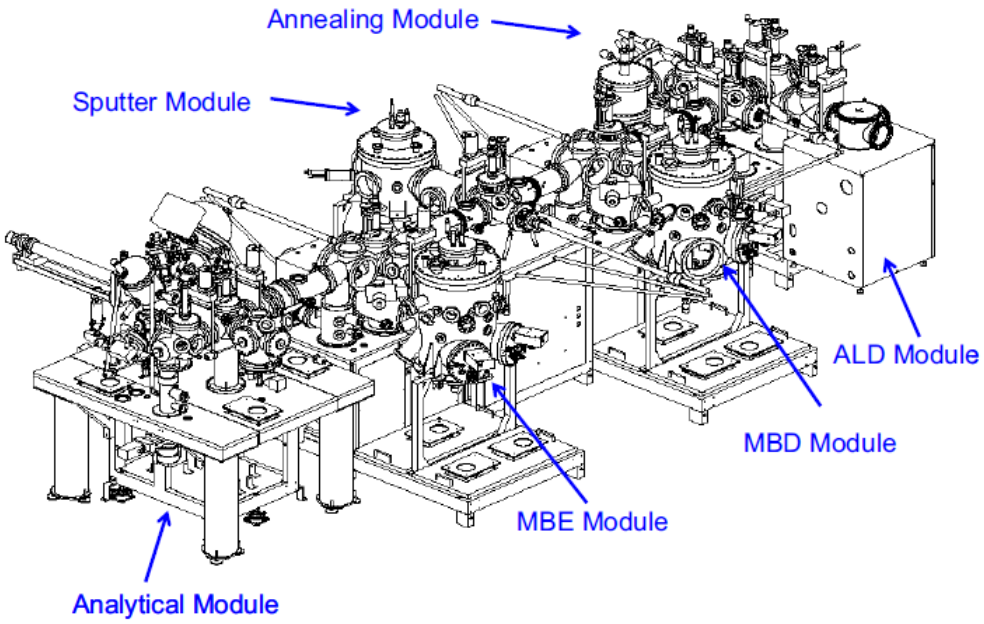


Figure 2.8. Professor Robert Wallace's XPS tool is used in this work

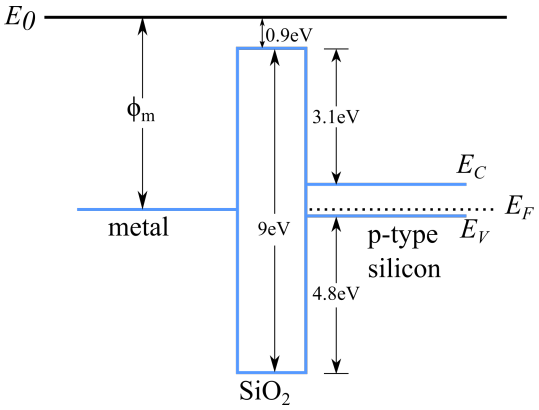
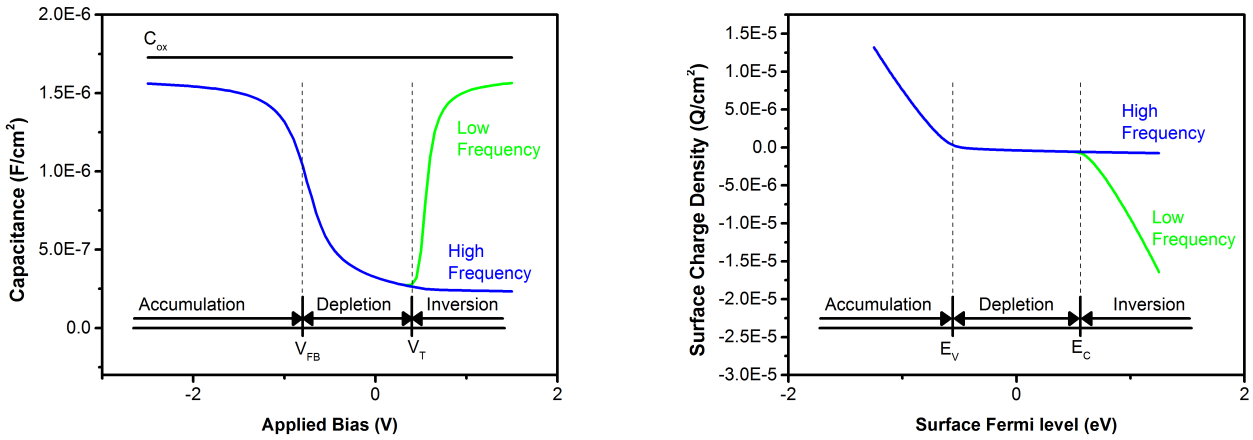


Figure 2.9. Flat band condition in a MOSCAP.



(a) Capacitance vs. voltage

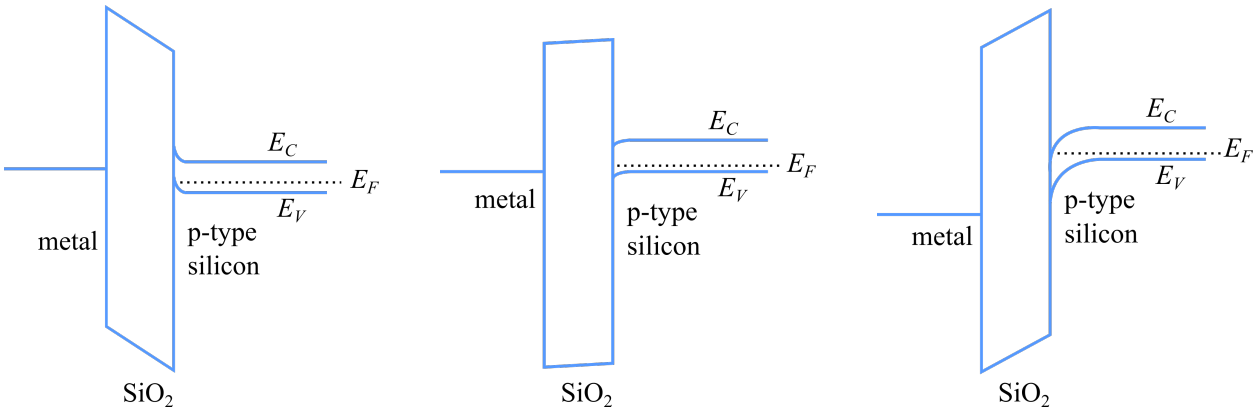
(b) Surface charge vs. Fermi level

Figure 2.10. Capacitance voltage and surface charge density for different regions of the MOS structure

It is highly convenient to start the analysis of a MOSCAP at the flat band condition, which is shown in Fig. 2.9. At flat band condition, the gate bias is called the flat band voltage (V_{FB}), which is shown in Fig. 2.10a. At the flat band condition, there is no band bending at the semiconductor meaning that the surface electric field in the semiconductor is zero and there is also no electric field in the dielectric.

For a p-type semiconductor, increasing the gate bias from V_{fb} causes the semiconductor band edges to bend at the surface as shown in Fig. 2.11b, resulting in more electrons (the minority carrier) attracted to the semiconductor surface and more holes (the majority carrier) pushed away from the surface. If the voltage is smaller than the threshold voltage (V_T), the semiconductor is in depletion, a condition where the charge carrier density is very low resulting in a small measured capacitance.

As the gate bias is increased, more electrons move toward the semiconductor surface and eventually the density of electrons becomes larger than the density of holes at the surface, resulting in the formation of an inversion layer. The gate bias when the semiconductor surface becomes inverted is called the threshold voltage, V_T . The Fermi level at the surface of the semiconductor moves near or into the conduction band (Fig. 2.11c) and the substrate



(a) Accumulation (b) Depletion (c) Inversion

Figure 2.11. Band structure of MOSCAP in different bias conditions.

capacitance is high. Conversely, decreasing the gate bias from V_{FB} would result in moving the surface Fermi level towards the valence band edge accumulating a large density of holes (the majority carrier) because of the negative bias voltage. Similar to the inversion region, increasing or decreasing the voltage in this region would change the surface hole density drastically, resulting in a high value of capacitance.

The resultant C-V profile depends on the frequency of the AC signal. If the frequency of the AC signal is very low, the minority carriers can follow the AC signal and there would be enough minority carrier generation to result in a high capacitance. However, if the frequency is high, minority carriers cannot follow the AC signal and the measured capacitance will be as low as depletion capacitance. Usually in a MOS capacitor structure, without external stimulation, the quasi-static or low frequency response is not observed as it would take minutes to thermally generate enough minority carriers to show the inversion response. In a MOSFET conversely, the source and drain regions act as an infinite supply of both majority and minority carriers and can readily supply electrons to the inversion layer and form the channel.

A MOSCAP can be expressed in terms of circuit elements. The most simple equivalent circuit of a MOSCAP consists of a capacitor as shown in Fig. 2.12, where the voltage applied

across gate and bulk is V_{gb}. In a parallel plate capacitor, the voltage on one side is measured with respect to the opposite side of the dielectric. So the voltage at the back contact can be considered zero or grounded whereas the top side shows the voltage applied. However, in a MOSCAP, the bottom side of the dielectric is not at 0 V. As a result there is a potential at the top surface of the semiconductor which is called surface potential and the voltage across the dielectric V_{ox}.

$$V_{gb} = V_{ox} + \psi_s \tag{2.7}$$

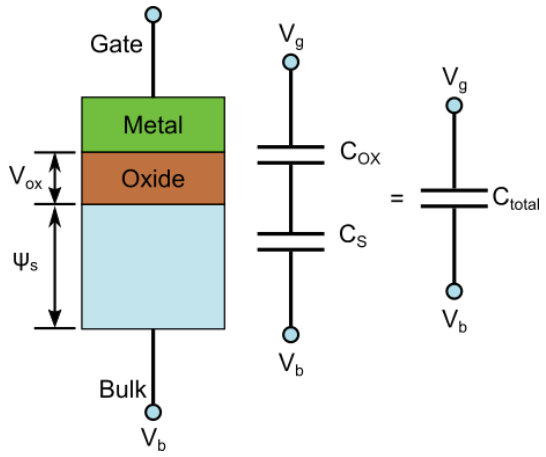


Figure 2.12. Equivalent circuit of MOSCAP.

As discussed before, the impedance of the total device can be measured from the difference in the applied DC bias and the measured current. From the real part of the impedance, conductance data can also be gathered from a MOSCAP. Admittedly conductance data may provide a good indication of the series resistance issue in the gate stack and it is also considered more sensitive to interface state density in depletion and weak inversion. However, this method is dependent upon accurate extraction of the gate oxide capacitance (C_{ox}) from C-V. Even though they can give unique insight into the characteristics of the interface and the gate stack, conductance is difficult to model properly and typically does not provide as detailed information as the C-V method does. Additionally, the leakage current can

give an indication on the quality of the dielectric deposited and its interface state density. Conductance and leakage current measurements are typically used as a supplementary or confirmatory data to C-V analysis.

In summary, the C-V method is highly useful for MOS device and the interface analysis. It is a very quick method, requiring only minutes of measuring time and a simple setup of a probe station and LCR meter. Along with the simplicity and rapidity of analysis, many device parameters including doping density of the semiconductor, thickness of the dielectric and gate oxide capacitance, flat band voltage, threshold voltage, etc. can easily be determined from the C-V measurement. Along with device parameters, the C-V profile can also be used to determine the quality of the dielectric as the presence of defects at the interface or in the dielectric layer would modify the C-V profile significantly from dielectric with good electrical characteristics.

2.7 Electrical Probe Station

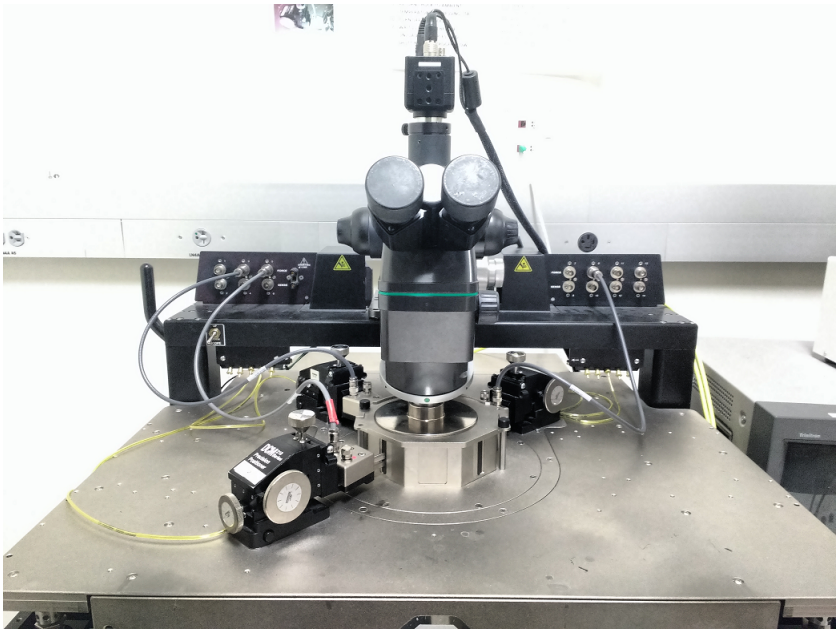


Figure 2.13. Probe station used in this work

As the devices fabricated are very small by design and necessity, a specialized setup is necessary to perform measurements on the fabricated samples. For example, in this report, all the samples have a active area of $7.74 \times 10^{-5} cm^{-2}$. To connect the LCR meter for C-V measurement to the connecting pads, a probe station is used as shown in 2.13. This probe station consists of a table with a microscope built in to the top. The sample holder is metal disk with vacuum holes placed strategically throughout the plate to hold samples steady. The sample holder can be moved vertically by a lever. The probes used in this setup are needle like structures with very fine tips with tip diameter of about 0.5μm. Each of the probes are connected to a manipulator, which can be moved in three dimensions using three sets of micrometer screws. Using the screws the tip of the probes can be easily manipulated around and placed on the pad. Electrically, the probes are connected to the manipulator via a triaxial wire to reduce noise, which in turn can be connected to the LCR meter using another triaxial cable. In this way, the LCR meter can have uninterrupted and noise free electrical connection to the pad. The sample holder is also connected to the other terminal of the LCR meter. In this work, a LCR meter made by Agilent Technologies model 4284 is used. The equivalent circuit of the model measured is given in Fig. 2.14.

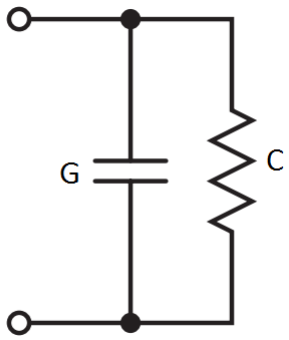


Figure 2.14. Equivalent circuit for C-V measurement used in the LCR meter

The capacitance, C shown in Fig. 2.14 is equal to the total gate capacitance in the equivalent circuit of a MOSCAP as shown in Fig. 2.12. The measured capacitance measured

is then divided by the area of the active area of the MOSCAP to obtain capacitance per area of a MOSCAP. This data is then analyzed using C-V ACE (described in chapter 3).

CHAPTER 3

ALTERNATE CHANNEL EXTRACTOR

Contributors in this chapter consists of SEMATECH staff, Dr. Rohit Galatage and Professor William Vandenberghe.

3.1 Model Development

3.1.1 Introduction

For current and future metal oxide semiconductor field-effect transistor (MOSFET) technology, various alternative semiconductor channel materials are used or being considered to improve device performance, including SiGe [36, 37, 38], germanium [39, 40, 41, 42, 43, 44, 10], and III-V compound semiconductors [45, 46, 47, 48, 49, 50, 51, 52, 53]. These high-mobility channel materials, used in conjunction with high-k dielectrics [54, 55] and metal gates may provide important advantages, leading to increased device density and performance while driving down the cost of manufacturing and energy consumption. However, characterizing experimentally fabricated gate stacks on these new channel materials is challenging.

The analysis of MOS capacitance-voltage (C-V) measurements has been a critical technique to determine many important gate stack parameters, such as the Equivalent Oxide Thickness (EOT), substrate doping density, flat band voltage, and the distribution and density of interface traps (D_{it}). C-V measurements are especially instrumental for new gate stacks since results can be obtained on MOS Capacitors (MOSCAPs) which are much simpler and quicker to fabricate compared to the full MOSFET. While there are very useful C-V analysis tools available to the community, most notably the ubiquitous North Carolina State University (NCSU) CVC code by Hauser and Ahmed [56], these tools all have certain

characteristics that limit their applicability to alternative semiconductor channel MOS gate stack analysis since they were developed for silicon where quantum effects are less prevalent compared to higher performance materials.

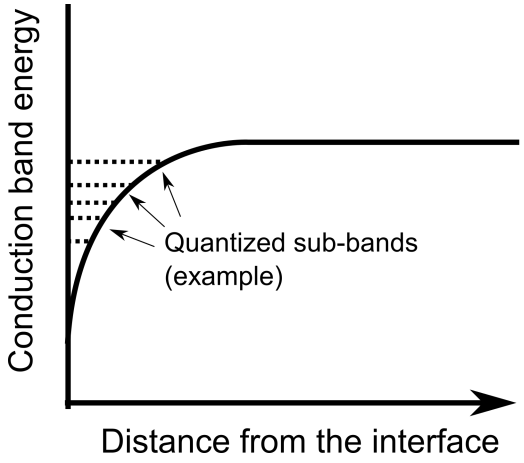


Figure 3.1. Quantized sub-band formation at the semiconductor-dielectric interface due to quantum confinement.

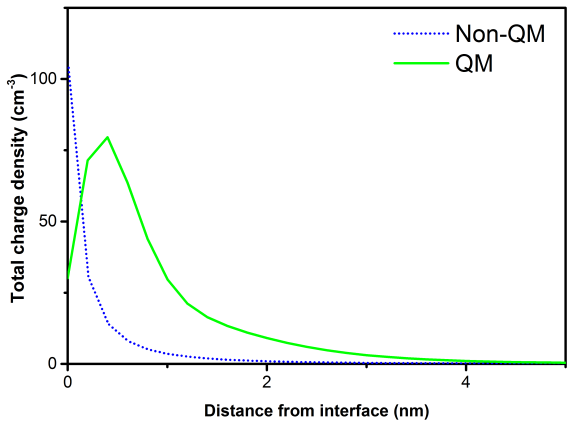
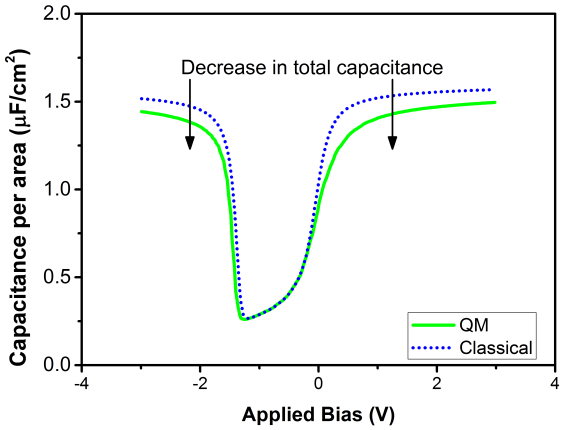
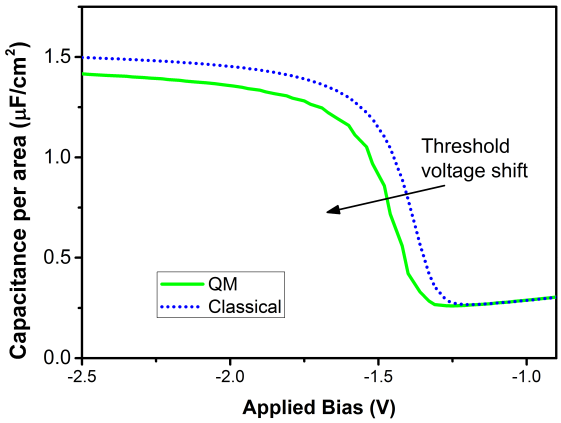


Figure 3.2. Carrier distribution calculation using QM and non QM method shows carrier confinement away from the interface. Non QM simulation was performed using MOSCap [57].

It is well established that the potential well at the semiconductor-oxide interface confines the free carriers normal to the interface and creates a two dimensional (2D) electron or hole gas [58]. Carrier confinement in strong inversion and accumulation splits the classically



(a) Change in total capacitance



(b) Shift in threshold voltage

Figure 3.3. Quantum mechanical effects on MOS C-V

continuous energy bands into discrete sub-bands where the energy level of the first sub-band does not coincide with the conduction or valence band edges as shown in Fig. 3.1. Additionally, and importantly when considering capacitance, the carrier centroid is shifted away from the semiconductor-dielectric interface compared to the classical carrier density depth profile as shown in Fig. 3.2 [59]. This leads to an additional quantum capacitance in series with the oxide capacitance. The total effect of the quantization is a reduction in the carrier density in the semiconductor and a shift in threshold voltage as shown in Fig. 3.3.

Quantum effects are generally much more important in advanced devices based on alternative materials compared to historical silicon devices for two reasons. First, scaling has reduced EOT and increased channel doping density. As a result, the electric field at the oxide-semiconductor interface has significantly increased, increasing the depth of the well and the quantum mechanical repelling of the charge carriers away from the interface. Secondly, the improved performance of alternative materials is often linked to the lower effective mass. While lighter effective mass particles usually travel faster, they inevitably also suffer more from quantum confinement effects, becoming important at lower electric fields.

3.1.2 Previous Quantum Mechanical Correction Models

Several methods have been used to model and simulate the QM effects of thin dielectrics and high doping density semiconductors. These methods can be divided into two categories: (i) the self-consistent solution of the Schrödinger and Poisson equations [60, 61, 62, 63, 64, 65, 66, 67] and (ii) modification of the classical calculation to account for the QM effects [68, 69, 70, 71, 72, 59, 73, 74, 75, 76, 77, 78, 79, 56]. Solving the Schrödinger-Poisson (SP) equations self-consistently is certainly the more comprehensive and accurate technique for calculating the charge in the MOS gate stack. However, this method of simulation is computationally intensive and time consuming and is primarily a forward model; i.e. it is hard to use in the extraction of gate stack parameters from experimental data. Modifying the classical method of calculation is computationally much cheaper compared to a self-consistent SP solver and can be used to extract experimental data. Unfortunately, methods of the second kind are limited, especially for alternative materials.

Quantum mechanical corrections to the classical method have been performed previously in a variety of ways. Hänsch *et al.* [68] proposed a reduction in the silicon density of states to account for the charge centroid shift. There, the density of states is reduced near the surface and gradually returned to the proper value in the bulk. Hänsch's model is simple, but the splitting of the bands into discrete energy levels and the resultant band-gap change was not taken into consideration making this model incomplete. The model proposed by van Dort *et al.* [59] includes both the displacement of the charges away from the semiconductor-dielectric interface as well as the splitting of the bands. The discrete sub-bands are calculated under the assumption that the potential well has a triangular shape and the total quantum mechanical effects can be accounted for by modifying the surface potential as follows,

$$n_{\mathrm{QM}} = N_C \times exp(-\frac{qV - q\phi_f}{k_B T}) \times [1 - exp^{-z^2/\lambda_{\mathrm{TH}}}] \tag{3.1}$$

where, N_C is the density of states, q is charge of electron, ϕ_f is Fermi level position, k_B is Boltzmann constant, z is the distance perpendicular to the semiconductor-dielectric interface, λ_{TH} is the thermal wavelength, $\lambda_{\mathrm{TH}} = (\hbar^2/2mkBT)^{1/2}$.

$$\psi_S^{\mathrm{QM}} = \psi_S^{\mathrm{CONV}} + \frac{13}{9}\Delta\epsilon \tag{3.2}$$

where $\frac{13}{9}\Delta\epsilon$ is the change in surface potential due to the combination of both the change in effective band-gap and the shift in charge centroid, which is deduced from an empirical fit to silicon experimental data. The expression for $\Delta\epsilon$ derived by van Dort is,

$$\Delta\epsilon \approx \beta(\epsilon_s/4qk_BT)^{\frac{1}{3}} \times max(E_n(0), 0)^{\frac{2}{3}} \tag{3.3}$$

where, E_n is the electric field perpendicular to the surface of silicon.

The van Dort model harbors a singularity, and Hareland *et al.* [76] modified the van Dort equations to better fit at low doping densities,

$$\begin{aligned}\Delta\epsilon &= \beta\left(\frac{\epsilon_s}{4qk_BT}\right)^{\frac{1}{3}}(\mid E_s \mid -10^5)^{\frac{2}{3}}, E_s > 10^5 kV/cm \\ &= 0, E_s < 10^5 kV/cm.\end{aligned}$$

However, both the van Dort [59] and Hareland [76, 61] models were developed only for inversion in silicon based devices. Accurate modeling of the accumulation capacitance is also necessary to obtain valuable information about the gate stack, including the flat band voltage, EOT, D_{it}, and in some cases border trap density [80]. Therefore, QM effects in accumulation are arguably more important for data extraction in traditional MOSCAP C-V measurement and analysis than inversion. It should also be noted that in weak accumulation and depletion, the electric field is very small and no quantum well is formed rendering QM effects negligible in those operating conditions.

Hareland did propose a QM correction for accumulation [77] which is similar to that of the one for inversion, with the addition of doping density dependent parameters. Hauser and Ahmed [56] proposed a van Dort-like surface potential correction model targeting silicon based MOS devices in the accumulation region,

$$\Delta\epsilon = (\hbar^2/2m^*)^{\frac{1}{3}}(\frac{9}{8}\pi q E_s)^{\frac{2}{3}} \tag{3.4}$$

using m^*, the carrier effective mass, as the comparatively simpler fitting parameter. However, all of the methods discussed thus far, utilized a physical grid to simulate the surface electric field to apply the QM corrections, which is computationally expensive. Vogel *et al.* [81] combined the two methods proposed by Hareland and developed a model (NIST) to simulate the C-V profile for silicon in both accumulation and inversion without the use of a physical grid. In that method, to calculate the field, the effective change in band-gap needs to be calculated. However, the effective widening of the band-gap is dependent on the electric field hence requiring a simultaneous solution of two inter-dependent equations.

3.1.3 Description of the Model

In this work, we combine aspects of all of those prior models, achieving a rapid C-V simulation and extraction tool that does not require a physical grid nor the solution of the aforementioned inter-dependent equations. As a result, the computational time is reduced tremendously. Moreover, as will be shown in the later sections, the model proposed here can be applied to any bulk semiconductor (Si, Ge, SiGe, GaAs, InGaAs, etc.), once the proper QM corrections are benchmarked and applied. The software, which we call C-V Alternative Channel Extraction (CV ACE), is developed using C++ programming language. The program can simulate a forward model in less than 50 ms, which is orders of magnitude faster than fully solving the Schrödinger-Poisson equations, which can take several hours.

Classical Method

Our method starts with calculating the number of both holes and electrons for a wide range of Fermi level positions ($\phi_s = (E_F - E_i)/q$) using the Fermi-Dirac integral of order 1/2 taking non-parabolic bands into account (important for alternative channel materials especially III-V semiconductors),

$$n = N_C \Im_{\frac{1}{2}}(\eta_c) \qquad \text{and} \qquad p = N_V \Im_{\frac{1}{2}}(\eta_v) \tag{3.5}$$

where,

$$N_C = 2\left(\frac{2\pi m_0 m_e k_B T}{h^2}\right)^{3/2} \tag{3.6a}$$

$$N_V = 2\left(\frac{2\pi m_0 m_h k_B T}{h^2}\right)^{3/2} \tag{3.6b}$$

$$\Im_{\frac{1}{2}}(\eta) = \frac{2}{\sqrt{\pi}} F_{\frac{1}{2}}(\eta) \tag{3.7}$$

$$F_{\frac{1}{2}}(\eta) = \int_0^\infty \frac{(1+2\xi\alpha)\sqrt{\xi(1+\xi\alpha)}d\xi}{1+e^{\xi-\eta}}. \tag{3.8}$$

$$\eta_C = \frac{E_F - E_C}{k_B T} \qquad \text{and} \qquad \eta_V = \frac{E_V - E_F}{k_B T} \tag{3.9}$$

$m_0 = 9.11 \times 10^{-31} kg$ is rest mass of electron

$m_e =$ is electron effective mass in conduction band

$m_h =$ is electron effective mass in valence band

E_C is conduction band edge energy measured from the intrinsic energy E_i

E_V is valence band edge energy measured from E_i

α is the non-parabolicity factor which is calculated in the usual manner [82, 83],

$$\alpha = \frac{(1-m_e)^2}{E_g}. \tag{3.10}$$

The Fermi level in the bulk is determined by,

$$p - n + N_d - N_a = 0 \tag{3.11}$$

where,

$$N_d = N_{\text{dop}} / \left(1 + 2e^{(E_F - E_C - E_g/2)/(k_B T)}\right) \tag{3.12}$$

$$N_a = N_{\text{dop}} / \left(1 + 4e^{(-(E_V - E_F) - E_g/2)/(k_B T)}\right) \tag{3.13}$$

where, N_{dop} is the magnitude of the bulk doping density. The bulk potential is determined from E_F, which is found by solving (3.11),

$$\phi_B = E_{F,\text{bulk}}/q. \tag{3.14}$$

The surface potential is calculated from the initial Fermi level position and the calculated bulk Fermi level position,

$$\psi_s = \phi_s - \phi_B. \tag{3.15}$$

The surface electric field is calculated by integrating the number of carriers with respect to the potential from the semiconductor bulk to the surface,

$$E_s = \sqrt{| \frac{-2q}{\epsilon_s \epsilon_0} \int_{\text{Bulk}}^{\text{Surface}} (p - n + N_d - N_a) d\phi \, |}. \tag{3.16}$$

The semiconductor charge is calculated using,

$$Q_s = -\text{sign}(\psi_s)\epsilon_s \epsilon_0 E_s \tag{3.17}$$

and the substrate capacitance is,

$$C_s = \frac{dQ_s}{d\psi_s}. \tag{3.18}$$

The work function difference between the semiconductor and the gate metal is,

$$\phi_{\text{ms}} = \phi_m - (\chi_s + \frac{E_g}{2} - \phi_B) \tag{3.19}$$

where, $\chi_s =$ is the electron affinity of the semiconductor. The flat band voltage is calculated using,

$$V_{\text{fb}} = \phi_{\text{ms}} - \frac{Q_f}{C_{\text{ox}}} \tag{3.20}$$

where, Q_f is the fixed charge density in the oxide. For the interface state defect density, the charge is calculated using the Fermi-Dirac distribution,

$$Q_{\rm it} = q \int_{-\infty}^{\infty} \frac{D_{\rm it} dE}{1 + e^{\frac{E-\phi_s}{k_B T}}}. \tag{3.21}$$

and the capacitance due to interface states is calculated,

$$C_{\rm it} = \frac{dQ_{\rm it}}{d\psi_s}. \tag{3.22}$$

Including the interface state response, the gate voltage and total capacitance is calculated by,

$$V_g = V_{\rm fb} + \psi_s - \frac{Q_s}{C_{\rm ox}} + \frac{Q_{\rm it}}{C_{\rm ox}} \tag{3.23}$$

$$C = \left(\frac{1}{C_{\rm ox}} + \frac{1}{C_s + C_{\rm it}/(1 + \omega^2 \tau^2)} \right)^{-1} \tag{3.24}$$

where, τ is the time constant of the interface states and $\omega = 2\pi f$, is the angular frequency of the AC signal during measurement.

For device parameter extraction, a non-linear least squares curve fitting algorithm [84, 85] is employed. The semiconductor parameters that are used in the classical simulation are given in Table 3.1.

Quantum Mechanical Correction

To correct the classical calculations for quantum mechanical (QM) effects, the surface potential is modified according to the following equation,

$$\psi_s^{\rm QM} = \psi_s^{\rm CONV} + \Delta\epsilon/q. \tag{3.25}$$

The correction to the surface potential ($\Delta\epsilon/q$) due to quantum mechanical effects depends on the transverse electric field as follows,

$$\Delta\epsilon = \beta (\frac{\epsilon_s \epsilon_0}{4 q k_B})^{\frac{1}{3}} (f(E_s))^{\gamma} \tag{3.26}$$

where,

$$f(E) = (\frac{(E)^2}{ae^{-(|E|/\sigma)^2} + \mid E \mid^{4/3}})^{3/2}. \tag{3.27}$$

$f(E)$ is a function to eliminate the flat band singularity at $E_s = 0$ [86], where a and σ are adjustable parameters and dependent on the semiconductor material. β and γ have different values in accumulation and inversion and also are different for p-type and n-type semiconductors. It should be noted that the a, σ, γ, and β terms do not have any physical significance. They are fitting parameters that enable us to map the classical C-V simulations to quantum mechanically correct C-V simulations empirically.

The conventionally calculated surface potential (ψ_s^{CONV}) in (3.17) and (3.18) is substituted with the modified surface potential (ψ_s^{QM}). The rest of the equations, (3.19) - (3.24) are used to complete the simulation.

Table 3.1. Semiconductor parameters used in CV ACE

	Si	Ge	Si_xGe_{1-x}			GaAs	$In_xGa_{1-x}As$	
x	-	-	0.5	0.6	0.75	-	0.2	0.53
ϵ_s	11.7	16.2	13.95	13.5	12.83	12.90	13.23	13.9
$\chi_s(eV)$	4.05	4	4.05	4.05	4.05	4.07	4.24	4.51
$E_g(eV)$	1.12	0.66	0.92	0.96	1.02	1.42	1.14	0.75
m_e	1.08	0.56	1.06	1.06	1.06	0.063	0.055	0.041
m_h	0.81	0.34	0.58	0.62	0.63	0.51	0.49	0.46

Self Consistent Schrödinger-Poisson Solver

To find the quantum mechanical correction factors, we first solve the Schrödinger and Poisson (S-P) equations self consistently to generate a fully quantum mechanically correct C-V curve. We then empirically map the simulation described in section 3.1.3 to that S-P solution. For this purpose, Prof. William Vandenberghe has developed a self-consistent Schrödinger-Poisson solver, which we use here [87]. We account for holes and electrons and take our

simulation region in the semiconductor large enough to encompass the depletion region so that the capacitance in accumulation, depletion, and inversion can be calculated quantum mechanically. The Schrödinger equation is solved for each inequivalent valley invoking the effective mass approximation. We denote the x-direction as the direction in which the electric field is applied and the y-z direction as the two perpendicular directions. The valleys whose axes align to the xyz-direction, such as the X-valleys in a (100) oriented wafer, are given their respective masses along the different directions. If the valleys do not align with the axes, e.g., for the L-valleys in a (100) oriented wafer, the mass tensor is projected on the xyz-directions. The Schrödinger equation is uniformly discretized in the x-direction using the finite difference method and solved using a sparse-eigenvalue solver.

The charge is computed by integrating over k_y and k_z weighing each wave function with the Fermi-Dirac distribution and by accounting over valley and spin degeneracy. Electrons and holes present a negative and positive contribution to the charge density respectively. Poisson's equation is discretized on the same grid as the Schrödinger equation and in the bulk, Neumann boundary conditions are applied while at the oxide-semiconductor interface, mixed boundary conditions are applied to account for the gate bias and the potential drop over the oxide. The Schrödinger equations for different valleys are solved self-consistently with Poisson's equation using Broyden's method [88]. Obtaining the charge from the Poisson-Schrödinger equation for two biases $V-\delta V/2$ and $V+\delta V/2$, the capacitance can be calculated as

$$C(V) = \frac{(Q(V+\delta V/2) - Q(V-\delta V/2))}{\delta V} \tag{3.28}$$

3.1.4 Model Validation

Classical simulation

Fig. 3.4 shows the resultant capacitance-voltage profiles obtained from CV ACE simulations using both Fermi-Dirac (FD) and Maxwell-Boltzmann (MB) distribution functions and com-

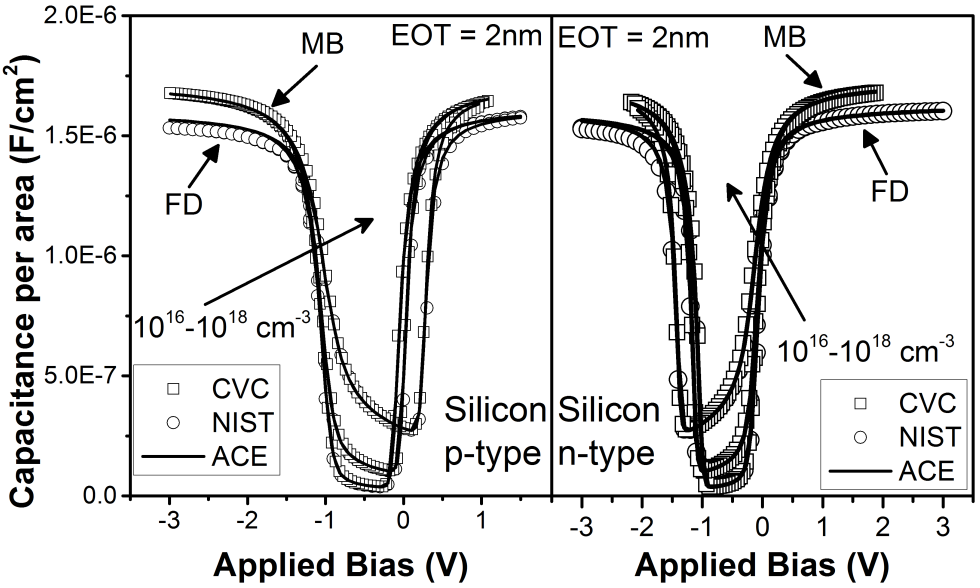


Figure 3.4. Comparison between CVC (NCSU)[56], NIST[81], and CV ACE for classically calculated $10^{16}cm^{-3}$ – $10^{18}cm^{-3}$ (a) n and (b) p-type doped Si with 2 nm EOT. CV ACE matches these other accepted codes for both MB and FD distribution functions.

pares the output to the CVC and NIST simulations for different doping densities without using any quantum mechanical corrections. The NCSU CVC code utilizes Maxwell-Boltzmann statistics while the NIST code uses full Fermi-Dirac statistics. Differences between the calculations using the two different distribution functions are observed in both accumulation and inversion as expected. Importantly, CV ACE is in excellent agreement with both CVC (MB) and NIST (FD) except in the negative bias range for the NIST code, i.e. in accumulation for p-type and inversion for n-type silicon. This difference originates from the differing values of the valence band density of states used by the two different simulators; $1.2 \times 10^{19}cm^{-3}$ in the NIST simulator and $1.8 \times 10^{19}cm^{-3}$ in CV ACE. If the value of valence band density states is set to $1.2 \times 10^{19}cm^{-3}$ in CV ACE, it fits identically to the data simulated by the NIST simulator. So, for all doping densities simulated and over a wide range of EOTs (not shown), the CV ACE classical calculation is validated with other accepted codes for both types of distribution functions. From here on, the simulations and extractions for CV ACE use FD statistics.

Self consistent Schrödinger-Poisson solver

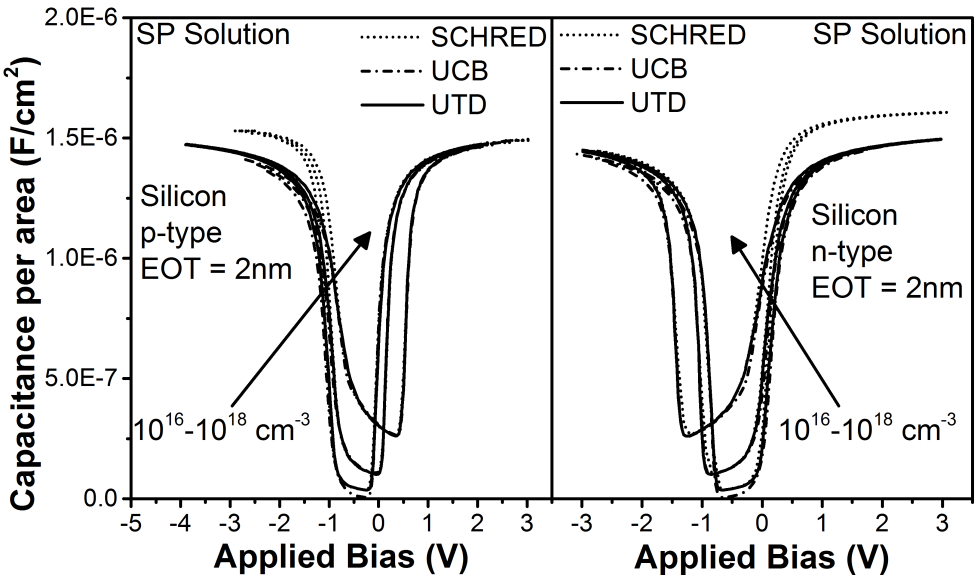


Figure 3.5. Comparison between different SP solvers SCHRED [89], UCB[90], and UTD for $10^{16}cm^{-3}$ – $10^{18}cm^{-3}$ (a) n and (b) p-type doped Si with 2 nm EOT is used in the simulations. The UTD code compares favorably with the other SP solvers.

To validate the UTD Schrödinger-Poisson solver, we compared our code to other available SP solvers. Fig. 3.5 shows the UTD SP solution compared to the same gate stack simulated using SCHRED [89] and a code from University of California Berkeley [90]. The UTD program produces nearly identical C-V profiles to the UCB code. In inversion and depletion, SCHRED also matches the UTD SP closely but SCHRED C-V profiles have higher capacitance in accumulation compared to the UTD and UCB codes as it does not solve the Schrödinger equation in accumulation. As a result, in the accumulation region for both n and p type semiconductors, SCHRED shows classical C-V profiles. The slight differences between the solvers comes from the different values of silicon parameters used in the solvers. In this paper, the semiconductor parameter values are the same for both the quantum mechanical simulations and classical simulations, which are given in Table 3.1.

QM Correction Factor Extraction using SP Solver

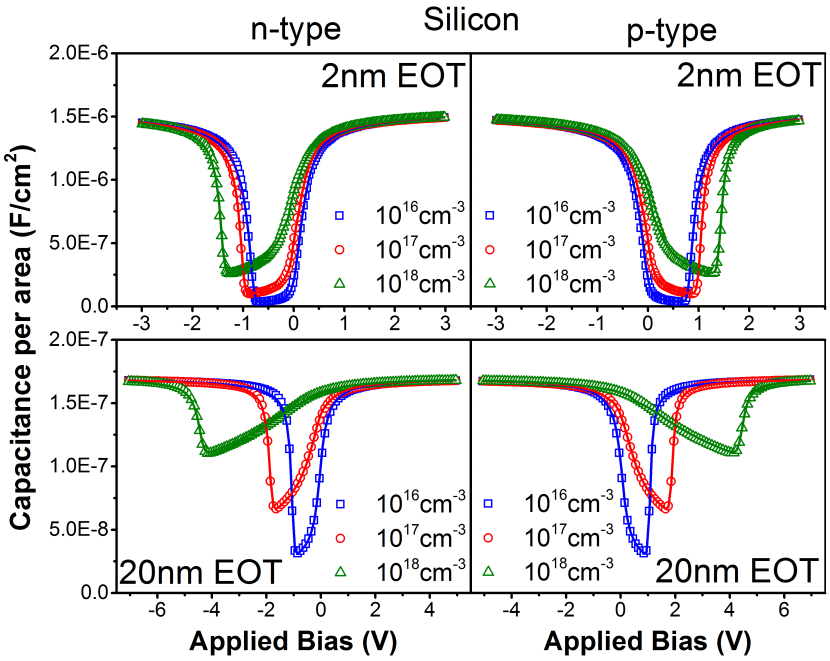


Figure 3.6. Quantum mechanical effects corrected CV curve compared to Schrödinger-Poisson solver for silicon for both n and p- type of different doping densities and EOTs

We extract the quantum mechanical correction parameters used in (3.25), using a non-linear least squares method fitting the corrected C-V simulation data to the full UTD Schrödinger-Poisson solutions for a variety of gate stacks on the various semiconductors. There are 10 parameters to characterize the QM corrections in a material- $\beta_{\mathrm{acc/inv},n/p}$ and $\gamma_{\mathrm{acc/inv},n/p}$ in inversion and accumulation for both n-type and p-type semiconductor. Additionally, a and σ are independent of the type of doping and only dependent on the semiconductor itself. However, σ has the same value for all the semiconductors described in this work and can therefore be considered a constant. These parameters for individual semiconductors are extracted by empirically fitting to the SP solver data.

In Figs. 3.6, 3.7, 3.8, 3.9, 3.10, 3.11, and 3.12, the results of the QM corrected classical C-V simulations fitted to the full SP solver calculations are shown for various semiconductors

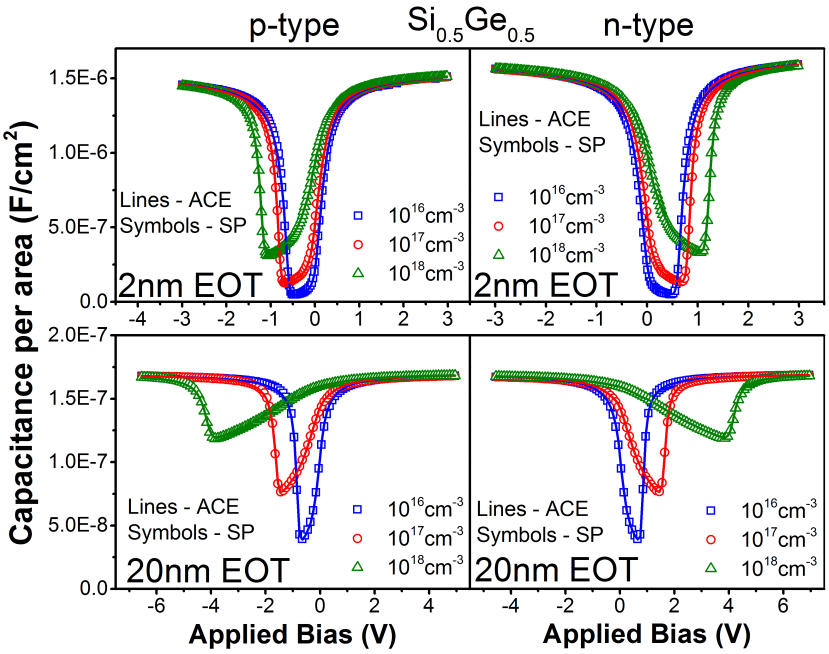


Figure 3.7. Comparison between QM corrected CV ACE simulations (lines) with SP solution (open symbols) for n and p-type $Si_{0.5}Ge_{0.5}$ with different doping densities and EOTs. CV ACE errors are less than 1%.

with a wide range of doping densities and oxide thicknesses. All the fits have a root-mean-squared (RMS) error of less than 1% and the extracted correction factors are given in Table 3.2. As stated before, these fitting parameters are empirical parameters that do not have any real physical significance other than that they accurately capture the QM calculated capacitance. It can be seen from Figs. 3.6, 3.7, 3.8, 3.9, 3.10, 3.11 and 3.12, that the correction factors for a specific semiconductor with a specific type of dopant, are valid over the full range of EOTs and doping densities of interest. For III-V semiconductors (GaAs, $In_{0.2}Ga_{0.8}As$ and $In_{0.53}Ga_{0.47}As$), only the Γ-valley is used for extraction of the quantum correction parameters. For the X and L-valleys, the energy gap and effective masses are different than those of Γ-valley and a more complex model would be required for quantum correction.

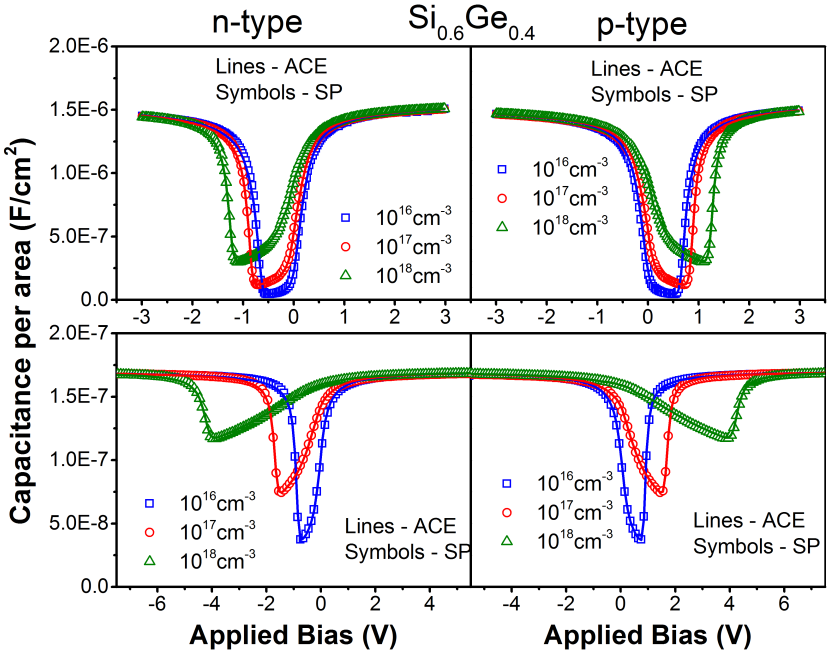


Figure 3.8. Comparison between QM corrected CV ACE simulations (lines) with SP solution (open symbols) for n and p-type $Si_{0.6}Ge_{0.4}$ with different doping densities and EOTs. CV ACE errors are less than 1%.

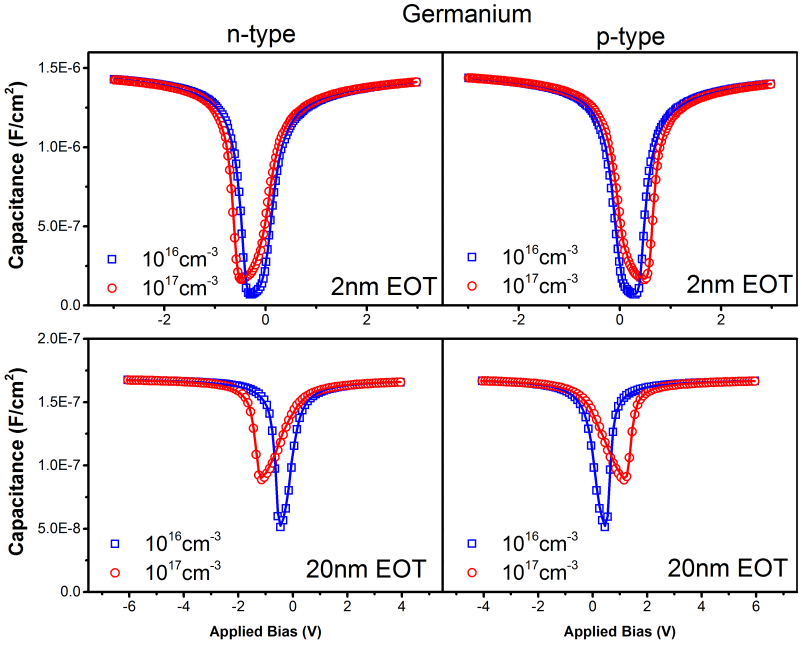


Figure 3.9. Quantum mechanical effects corrected CV curve compared to Schrödinger-Poisson solver for germanium for both n and p-type of different doping densities and EOTs

Table 3.2. Quantum Mechanical correction factors for different semiconductors

	n-type				p-type					
	β_{inv} (eV.cm)	γ_{inv}	β_{acc} (eV.cm)	γ_{acc}	β_{inv} (eV.cm)	γ_{inv}	β_{acc} (eV.cm)	γ_{acc}	a ((V/cm)$^{4/3}$)	σ ((V/cm))
Silicon	-4.39×10^{-8}	0.64	4.60×10^{-8}	0.63	5.75×10^{-8}	0.62	-3.6×10^{-7}	0.65	$2.38{\times}10^{6}$	10^{10}
Germanium	-5.02×10^{-8}	0.66	7.01×10^{-8}	0.60	4.23×10^{-8}	0.63	-6.44×10^{-8}	0.65	$1.38{\times}10^{5}$	10^{10}
$Si_{0.5}Ge_{0.5}$	-3.81×10^{-8}	0.64	1.18×10^{-8}	0.57	1.89×10^{-8}	0.69	-8.57×10^{-8}	0.59	$1.88{\times}10^{6}$	10^{10}
$Si_{0.6}Ge_{0.4}$	-4.04×10^{-8}	0.64	1.17×10^{-7}	0.57	1.99×10^{-8}	0.69	-8.95×10^{-8}	0.59	$1.93{\times}10^{6}$	10^{10}
$Si_{0.75}Ge_{0.25}$	-4.39×10^{-8}	0.64	1.17×10^{-7}	0.58	1.72×10^{-8}	0.70	-1.18×10^{-7}	0.57	$2.09{\times}10^{6}$	10^{10}
GaAs	-5.36×10^{-8}	0.63	9.15×10^{-8}	0.57	4.16×10^{-8}	0.63	-1.14×10^{-7}	0.58	$3.52{\times}10^{5}$	10^{10}
$In_{0.2}Ga_{0.8}As$	-1.47×10^{-8}	0.76	1.57×10^{-7}	0.54	5.93×10^{-8}	0.60	-5.02×10^{-8}	0.67	$1.22{\times}10^{5}$	10^{10}
$In_{0.53}Ga_{0.47}As$	-9.26×10^{-8}	0.60	3.15×10^{-8}	0.65	2.96×10^{-8}	0.65	-1.54×10^{-7}	0.56	$4.81{\times}10^{6}$	10^{10}

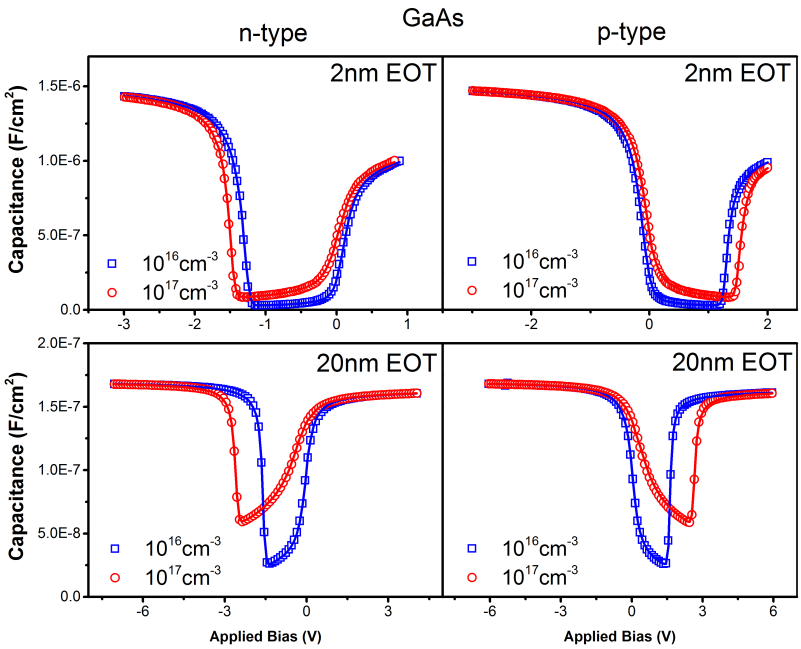


Figure 3.10. Comparison between QM corrected CV ACE simulations (lines) with SP solution (open symbols) for n and p-type GaAs with different doping densities and EOTs. CV ACE errors are less than 1%.

3.1.5 Comparison to Experimental C-V

Silicon

CV ACE can be used to analyze C-V data from MOS devices based on a multitude of semiconductors. In this section, to show the viability of this quantum correction model, a couple of select silicon based MOS device are analyzed using CV ACE. In later sections, MOS devices from alternative channel semiconductors (Ge and InGaAs) will be analyzed in detail using CV ACE.

Two silicon samples were fabricated by our SEMATECH collaborators on p-type silicon with chemically grown SiO_2 and Atomic Layer Deposition (ALD) deposited HfO_2 with a metal gate. The measured high-frequency C-V profiles are analyzed in both CVC and CV ACE and the fits are shown in Fig. 3.13. From the fits, it can be seen that both CV ACE and CVC have very good fits to the experimental C-V profiles obtained from both samples.

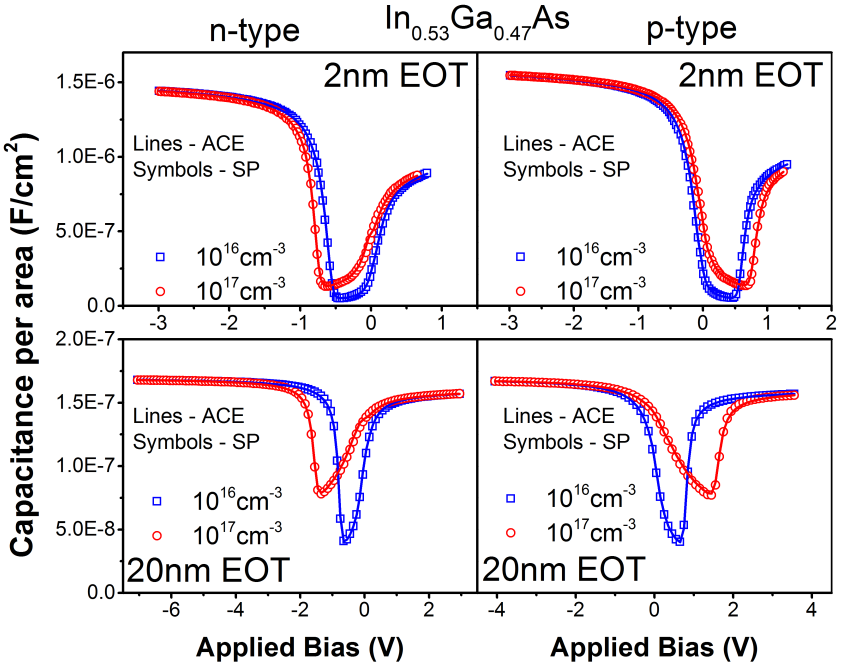


Figure 3.11. Comparison between QM corrected CV ACE simulations (lines) with SP solution (open symbols) for n and p-type $In_{0.53}Ga_{0.47}As$ with different doping densities and EOTs. CV ACE errors are less than 1%.

Comparing to the NCSU model, CV ACE actually has a better fit to the experimental data (<0.5% RMS error). In both cases, extracted EOTs using CV ACE are lower than the extracted EOTs using the NCSU model. This difference in extracted values originates from the fact that in CVC the QM correction factors were obtained by mapping the model to experimental data, and hence has an inherent uncertainty in the measured dielectric thickness. Conversely in CV ACE, the QM corrections are benchmarked to SP solver data, which is free from the uncertainty that exists in physical measurements. Fig. 3.14 shows the disparity between the simulated C-V profiles from CVC with quantum mechanical corrections and from the SP solution, where CVC shows higher capacitance in accumulation compared to both the SP solver and CV ACE for a given EOT = 1 nm for both n and p-type doping. From this difference it can be concluded that for a specific C-V profile, CVC would slightly over-estimate the thickness of the dielectrics.

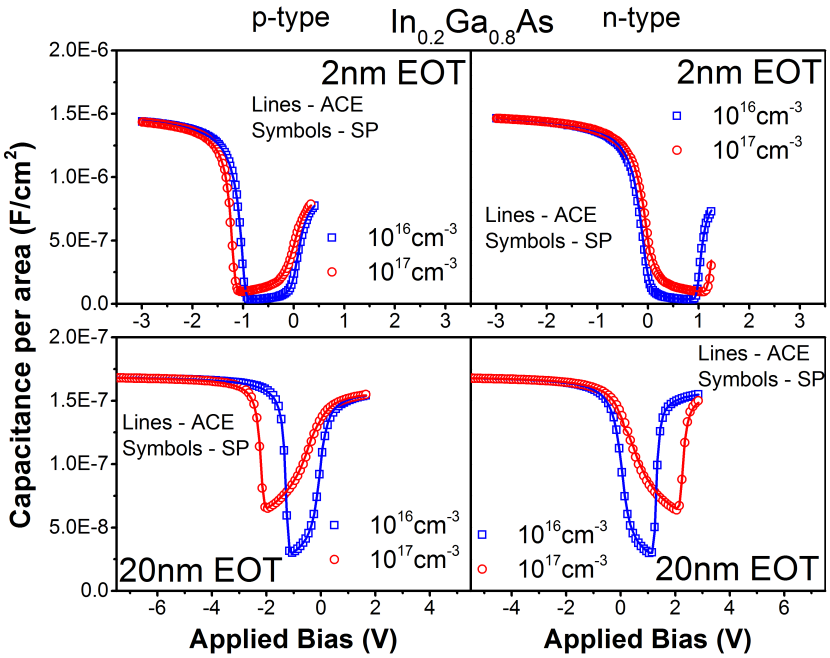


Figure 3.12. Comparison between QM corrected CV ACE simulations (lines) with SP solution (open symbols) for n and p-type $In_{0.20}Ga_{0.80}As$ with different doping densities and EOTs. CV ACE errors are less than 1%.

3.2 Extraction of device parameters

Capacitance-voltage measurement and analysis is highly useful for deducing important information about metal-oxide-semiconductor (MOS) gate stacks. Parameters such as the equivalent oxide thickness (EOT), substrate doping density, flatband voltage, fixed oxide charge, density of interface traps (D_{it}), and effective gate work function can all be extracted from experimental C-V curves. However, to extract these gate stack parameters accurately, the correct models must be utilized. In section 3.1, we described the modeling and implementation of a C-V code that can be used for alternative channel semiconductors in conjunction with high-k gate dielectrics and metal gates. Importantly, this new code (CV ACE) includes the effects of non-parabolic bands and quantum capacitance, enabling accurate models to be applied to experimental C-V curves. In this section, we demonstrate the capabilities of this

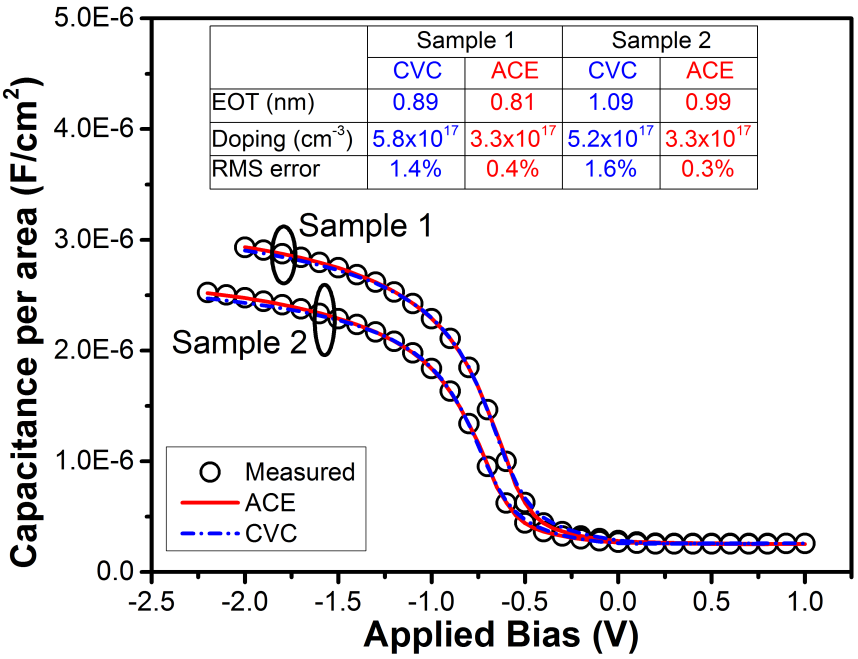


Figure 3.13. CV ACE and CVC fits to experimental Si/high-k gate stacks. CV ACE has a lower RMS error than CVC. EOTs using CV ACE are lower than CVC due to a more accurate benchmarking methodology.

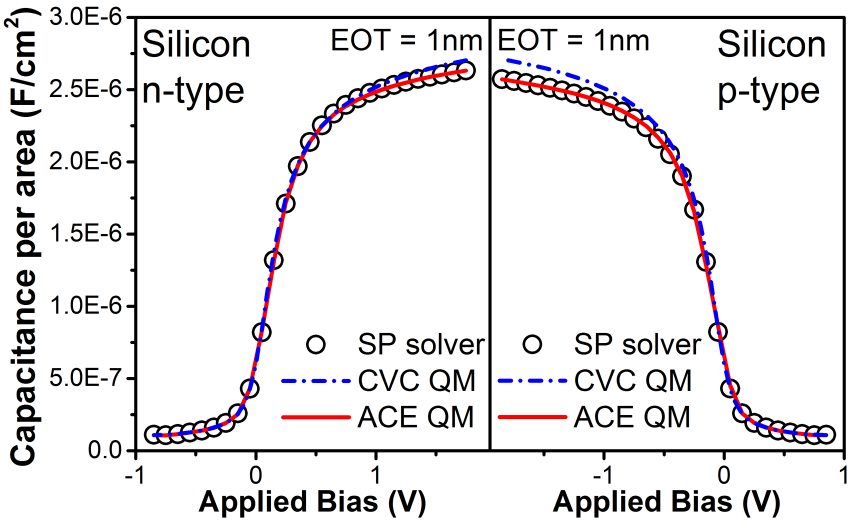
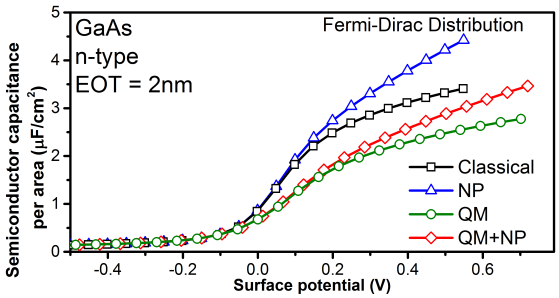


Figure 3.14. Simulated C-V curves for n and p-type Si with $10^{17} cm^{-3}$ doping and 1 nm EOT. CV ACE matches the SP data but CVC overestimates the capacitance in accumulation due to difference in benchmarking methodology.

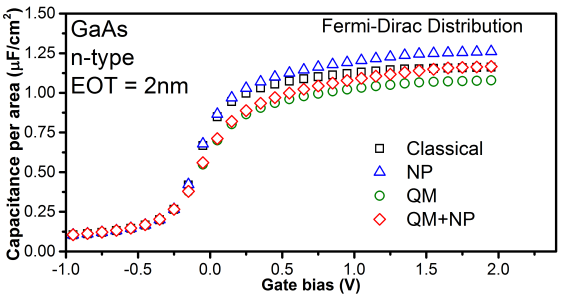
new code to extract accurate parameters including EOT and D_{it} profiles from experimental high-k on Ge and InGaAs gate stacks.

C-V simulation and extraction tools have been previously developed for Si-based MOS gate stack analysis. The most widely used among these is the aforementioned NCSU CVC program [56]. This program has been heavily used since its publication to aid with gate stack process development by enabling the extraction of equivalent oxide thickness (EOT), doping density, and the flat band voltage. However, CVC was implemented with silicon's band structure only and is therefore inaccurate when used for MOS devices based on any other semiconductor. Additionally, because Si has such a high-quality native oxide with very low interface defect density, CVC was developed without the capability of extracting a detailed D_{it} distribution as a function of energy. D_{it} analysis is a critical component to process development of high-k/high-mobility semiconductor gate stacks due to the lack of a stable, high-quality native oxide on Ge and III-Vs. For example, while the native oxide of germanium, GeO_2, has good passivating properties [7] it suffers from the physical characteristics of being hygroscopic, soluble in water, and thermal instability. Because of GeO_2's solubility in water in particular, integrating high-k dielectrics is challenging as the ALD processes, necessary for scaled high-k dielectric deposition on FinFETs, may utilize de-ionized water (DIW) as an oxidizing agent, which damages and partially etches the germanium oxide layer. III-V materials have even worse native oxides in addition to dimers and antisite defects. Ga_2O_3 and As_2O_3, have been correlated to poor device performance necessitating that the high-k dielectrics be deposited directly on the III-V semiconductor. However, the interface of those dielectrics with the III-V semiconductors are usually not atomically abrupt, resulting in a thin disordered region at the interface [91, 21, 22]. This disordered region causes carriers to tunnel through the region into III-V related defects and oxide related border traps, resulting in anomalous C-V characteristics that make process development and analysis challenging.

Due to the small effective mass and density of states, the surface Fermi level in III-V-based MOS devices moves deep into the conduction band. Therefore, the non-parabolicity of the



(a) Substrate capacitance vs. surface potential



(b) Total gate capacitance measured vs. applied gate bias

Figure 3.15. Gate capacitance vs gate bias

conduction band in III-V semiconductors and quantum mechanical effects must be accurately considered [83]. Fig. 3.15a shows the semiconductor capacitance vs. surface potential for GaAs calculated 1) classically with parabolic bands, 2) classically with non-parabolic bands, 3) with parabolic bands including the quantum capacitance, and 4) fully combining non-parabolic bands with the quantum capacitance. The total resultant capacitance vs. gate voltage, using each of these models, is shown in Fig. 3.15b. It can be seen that the use of non-parabolic bands increases the capacitance while QM effects reduce the capacitance and change the shape of the curve. This illustrates how critical it is to use the correct models when extracting data from experimental C-V curves. If the incorrect model is used, extracted EOTs, V_{fb}, and the magnitude and distribution of D_{it} will all be inaccurate. CV ACE addresses these issues by having implemented the band structure of alternative semiconductors and allowing for a detailed extraction methodology that includes interface state capacitance. The code incorporates a wide range of semiconductors and dielectrics with the capability to implement customized gate stacks as well. Fermi-Dirac carrier statistics, non-parabolic bands, and quantum mechanical effects are all implemented with options to turn each of these off as the user desires. Interface state capacitance is implemented using a common model for well-behaved systems (like Si). A more complex C_{it} model is also implemented for III-Vs that accurately captures frequency dispersion in accumulation that

arises from tunneling. CV ACE is enabled to accommodate models and CV measurements performed at variable temperatures and variable frequencies to allow for a more accurate extraction of D_{it}. And importantly for the quick turnaround times necessary in process development, CV ACE enables extremely fast simulation and extraction.

3.2.1 CV Simulation and Extraction Calculations

In CV ACE, the fitting parameters (the equivalent oxide thickness, substrate doping density, and D_{it}) are varied, and the simulated C-V profiles are then compared to the experimental C-V curves. The fitting parameters that minimize the normalized RMS error between the measured and simulated C-V profiles are then extracted and the software reports the EOT, $\mathrm{V_{fb}}$, doping density, and D_{it} distribution that provided this best fit. The normalized RMS error is calculated by,

$$\mathrm{Error_{rms}} = 100 \times \sqrt{\frac{\sum_{i=1}^{n}(C_{\mathrm{exp},i} - C_{\mathrm{sim},i})^2}{n \times \overline{C_{\mathrm{exp}}}}} \tag{3.29}$$

where, C_{exp} is the measured capacitance and C_{sim} is the simulated capacitance for the same gate bias voltage and n is the total number of bias points. For this purpose, a nonlinear least squares method based on the Levenberg-Marquadt Algorithm (LMA) [84, 85] is utilized for robustness. Because of the very fast forward simulation capabilities of CV ACE, no look-up table needs to be generated, and the calculation of the Jacobian matrix in the LMA is fast enough to enable a rapid curve fitting procedure for the extraction of the gate stack parameters from experimentally measured C-V curves. The interface state density distribution, D_{it}(E), used in equation (3.30) has been implemented in CV ACE to enable almost any D_{it} profile. To facilitate this capability, multiple mathematical functions are available. A polynomial function, with the user option to utilize up to the 10th order, enables significant flexibility in modeling and extracting D_{it} distributions,

$$D_{\mathrm{it}}(E_t) = e^{(a_{0,\mathrm{it}} + a_{1,\mathrm{it}}E_t + a_{2,\mathrm{it}}E_t^2 + \ldots + a_{10,\mathrm{it}}E_t^{10})} \tag{3.30}$$

where, E_t is the energy of the trap away from the intrinsic Fermi level (E_i) and a_0 to a_{10} are polynomial coefficients. For example, a constant D_{it} distribution can be achieved using the 0th order function while a parabolic distribution can be simulated using the 2nd order. Higher order functions are often the best choice when extracting from experimental C-V curves associated with high-k on high-mobility gate stacks.

The nonlinear least squares fitting method, described above, then also includes the selected D_{it} distribution as a fitting parameter. Something that must always be considered when doing modeling that utilizes curve fitting is the uniqueness of the fit, i.e., obtaining different extracted parameters from the same data set with similar errors from the fitting procedure. As will be discussed in later sections, the recommended procedure for obtaining accurate extracted parameters and profiles from experimental data includes the simultaneous fitting of two C-V curves from the same device, measured at different frequencies (since C_{it} is frequency dependent). This simultaneous fitting, for two sets of data that by definition must have the same EOT, doping density, and D_{it} distribution provides the necessary parameter constraints for satisfactory uniqueness.

3.2.2 Extracting $\mathbf{D_{it}}$ for "Well-Behaved" Systems

Interface state density affects the measured C-V profile significantly and the wide variety of band structures and density of states in various semiconductors results in C-V profiles that are differently impacted by interface states. For Si devices, the high density of states results in a high substrate capacitance that minimizes the impact of the interface state capacitance, especially for the relatively low D_{it} associated with the Si-SiO_2interface. Even for a relatively high interface defect density like those associated with HfO_2 on Si ($\sim 10^{12} cm^2 eV^1$), the impact on the measured C-V is usually fairly small and observed only in the depletion region of the C-V profile where the substrate capacitance is low (the frequency dependent D_{it} "hump"). SiGe and Ge tend to have higher values of D_{it} because of the aforementioned issues

with passivating Ge and the instability of GeO_2. When the frequency dependent response is "well-behaved" as in the systems just described, the typical methods for extracting D_{it} are sufficient (when using the correct band structure for the semiconductor). From a single high-frequency C-V curve, the D_{it} can be extracted by assuming that the D_{it} cannot respond to the AC signal and the interface trap capacitance in (3.24) is zero. The interface traps do, however, respond to the DC bias as the surface potential is affected by the interface states, in effect "delaying" the semiconductor's response to the applied bias as calculated using (3.23). This method of using the "stretchout" to extract the D_{it} is the basis of the Terman method [34] and is implemented in CV ACE.

As alluded to earlier, a more complete technique for extracting D_{it} profiles is to simultaneously fit two different C-V curves from the same device, measured at different frequencies. This Modified High-Low Method [34] once again assumes that the C_{it} is zero for the high frequency (100 kHz or higher) C-V curve while all interface traps respond to the low AC frequency (typically 100 Hz). The fitting procedure then varies the EOT, doping density, and D_{it} distribution to simultaneously match the stretchout in the high-frequency curve and the low frequency C_{it} response. The "modified" term describing this method is to indicate that oftentimes utilizing different measurement temperatures in conjunction with the different frequencies can help to enhance or suppress the AC C_{it} response. For example, to ensure no C_{it} response, one may perform the high-frequency measurement at 77K to "freeze-out" the trap response while maintaining room temperature measurement for the low frequency curve. As long as the user inputs the appropriate temperatures before extraction, CV ACE can accurately handle this multi-frequency, multi-temperature analysis. Also implemented in CV ACE is the capability of using the trap time constant in (3.24) as another fitting parameter in conjunction with the Modified High-Low Method. Using a high order polynomial function for the trap time constant,

$$\tau(E_t) = e^{-(a_{0,\tau}+a_{1,\tau}E_t+a_{2,\tau}E_t^2+...+a_{10,\tau}E_t^{10})} \tag{3.31}$$

the user can simulate the frequency dependent $D_{\rm it}$ response using (3.31), eliminating the need to assume $C_{\rm it} = 0$ in the high frequency curve.

3.2.3 Extracting D_{it} for III-V systems

For III-V materials, the interface state response is much more complex [92]. III-Vs generally have a much lower carrier effective mass and density of states compared to silicon. This manifests itself in a one order of magnitude lower substrate capacitance for III-Vs relative to Si for the same EOT and substrate doping density. As a result, the total measured gate capacitance for III-V devices is significantly affected by the interface state capacitance ($C_{\rm it}$). An additional problem that arises from defects in III-V/high-k gate stacks is the well know anomalous frequency dispersion in accumulation [93]. This frequency dispersion has been observed for a wide range of dielectrics including Al_2O_3, HfO_2, and ZrO_2, on a variety of III-V substrates including GaAs, $In_{0.53}Ga_{0.47}As$, $In_{0.20}Ga_{0.80}As$ and InAs. When frequency dispersion is observed in measured III-V C-Vs, it is necessary to modify (3.21), (3.22), and (3.24) above and various research groups have developed different models to capture the observed frequency dispersion. The Disorder Induced Gap States (DIGS) model [91, 21, 22] and the distributed Border Trap (BT) model [94, 80, 95] employ the same basic principal, i.e. tunneling of carriers to traps away from the crystalline semiconductor interface. As shown in [22], both the DIGS and BT models accurately capture the measured capacitance over typical measurement frequencies (e.g., 100 Hz to 1 MHz). The DIGS model is implemented in CV ACE, where the capacitance from interface states is calculated by,

$$C_{\rm DIGS} = \frac{q^2 N_{\rm t0}}{2\kappa}(\omega\tau_0)^{\frac{\alpha}{2\kappa}} \int_0^{\frac{1}{\omega\tau_0}} (z)^{\frac{\alpha}{2\kappa}} tan^{-1}(z^{-1}) dz \tag{3.32}$$

where,

α is the decay constant

$N_{\rm t0}$ is the trap density at the interface

$\kappa = \sqrt{\frac{2m^*_{\text{ox}}\Delta E_C}{\hbar^2}}$ is the attenuation coefficient of decaying electron wave function

m^*_{ox} is the electron effective mass in the oxide

ΔE_C is the conduction band offset between the dielectric and the semiconductor.

In this model, the total capacitance is calculated by,

$$C_{\text{sim}} = \left(\frac{1}{C_{\text{ox}}} + \frac{1}{C_s + C_{\text{DIGS}}} \right)^{-1} \tag{3.33}$$

The tunneling distance into the disordered layer that is probed at a given frequency can be approximated by,

$$x_{\text{tunneling}} = \frac{1}{2\kappa} \ln \left(\frac{1}{\omega \tau_0} \right) \tag{3.34}$$

In this model, the measured capacitance is calculated using (3.32) and (3.33) in conjunction with (3.23). Two C-V curves measured at different frequencies (and oftentimes different temperatures as well) enable more accurate extractions using this model. For convenience and to avoid incorrect local minima in the fitting procedure, a guideline to use CV ACE in the extraction of device parameters and Dit using multi-frequency C-V curves is given here.

1. Select the high frequency measurement, disable the AC and DC D_{it} calculation options, and run the fitting procedure to obtain a first approximation of the EOT and doping density.

2. Select the low frequency measurement, enable the AC C_{it} calculation on the low frequency data set, enable the DC D_{it} calculation, and run the fitting procedure to extract the D_{it} using the modified high-low method as given in section 3.2.2.

3. If the user desires to use the trap time constant as a fitting parameter, enable the AC C_{it} calculation on the high frequency measurement as well, enable the time constant toggle, and run the fitting procedure.

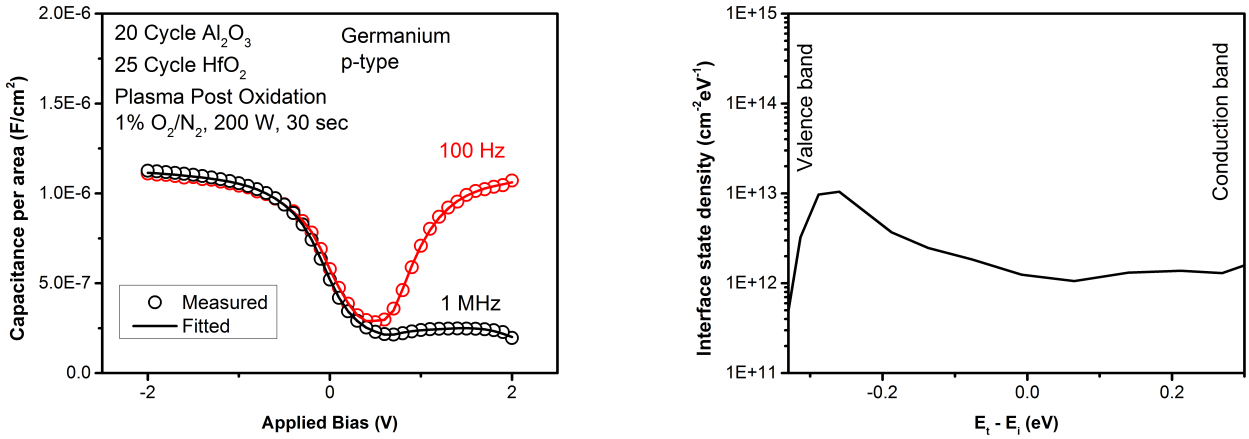
4. For III-V semiconductors with frequency dispersion in accumulation, it is suggested that the previous steps be completed before enabling the DIGS model. This helps to reduce the fitting and extraction. Additionally, the value of κ in (3.32) must be input by the user for the appropriate conduction band offset for the specific dielectric/semiconductor system being studied. Then by running the extraction procedure, EOT, doping density, and interface state and time constant density profile can be fitted to the experimental data.

Germanium

High-k MOS devices were fabricated on p-type (0.01–0.04 Ω.cm) Ge wafers. The wafers were cleaned sequentially in acetone, IPA, and DIW for 1 minute each prior to loading into the ALD chamber. 20 cycles of Al_2O_3 was deposited using TMA and DIW followed by 25 cycles of HfO_2 was deposited using TDMA-Hf and DIW all at 250°C. The sample was then transferred to a Plasma Enhanced Chemical Vapor Deposition (PECVD) chamber and exposed to 1% oxygen in argon at 200 W power and 1000 mTorr pressure for 30 seconds (see chapter 4 for more details). 20 nm of TiN followed by 40 nm of W was deposited by RF sputtering. 15 nm of Ti and followed by 50 nm of Al were deposited on as the backside of the wafer for back contact. The sample was then annealed at 400°C for 30 min in forming gas (5% H_2 in a balance of N_2). C-V measurements were performed in a conventional Cascade probe station at 100 Hz and 1 MHz AC signal at room temperature (300 K).

To analyze the measured data, first only the C-V profile of 1 MHz is fitted, without considering any interface state density i.e. using (3.24) with D_{it} set to zero. After this C-V profile is fitted, the 100 Hz data is used in conjunction with the 1 MHz data. D_{it} is considered in 100 Hz data but not in 1 MHz data analysis. After that it was observed that the stretchout of the simulated C-V profile does not match with the experimental data, indicating increased DC response but not increased AC response. In other words, both the

high and low frequency data is needed to be fitted while considering time constant of the interface states. After time constant is enabled in both high and low frequency simulation, a very good fit was obtain. In this way, an accurate profile of the interface states are extracted along with quantum mechanically correct EOT.



(a) Capacitance-Voltage profile (b) Interface state density (D_{it}) profile

Figure 3.16. Fit to germanium experimental data using CV ACE

The measured MOSCAP C-V and the fitted data (with RMS error less than 1%) as well as the extracted interface state profile is shown in Fig. 3.16. The extracted interface state density profile shows a low mid-gap D_{it} of about $10^{12} cm^{-2} eV^{-1}$, which increases near the valence band edge to about $10^{13} cm^{-2} eV^{-1}$. Ge based MOS devices, analyzed using CV ACE will be further discussed in chapters 4 and 5.

InGaAs

$In_{0.53}Ga_{0.47}As$ grown on lattice-matched InP substrates and doped with silicon (n-type) to a density $10^{17} cm^{-3}$ were fabricated at SEMATECH as part of an exercise to evaluate different Dit extraction methodologies on III-Vs (the Golden Wafer experiment). The $In_{0.53}Ga_{0.47}As$ was cleaned in IPA for 1 min and in 1% HF for 5 seconds and then rinsed with de-ionized (DI) water. A bi-layer dielectric was then deposited using ALD. 2 nm of Al_2O_3 deposited

using TMA and DI water was followed by 5 nm of ZrO_2 layer deposited using zirconium tert-butoxide (ZTB) and DI water all at 250°C. The formation of the dielectric was followed by a post deposition anneal (PDA) of 500°C in N_2, 200 nm of TaN deposition was used as the gate metal, and a post metallization anneal (PMA) of 400°C in N_2. No forming gas anneal (FGA) was performed. C-V measurements were again performed using a Cascade probe station at 100 Hz and 100 kHz AC signal at room temperature (300 K). For analysis of the measured C-V, three of the methods described in the last section have been performed using CV ACE. The simulated C-V profiles using the various methods are shown in Fig. 3.17. The corresponding extracted interface states are shown in Figs. 3.18. In all the simulations non-parabolicity of the conduction band was used along with the quantum mechanical corrections described earlier. The extracted parameters for the different methods are compared in table 3.3.

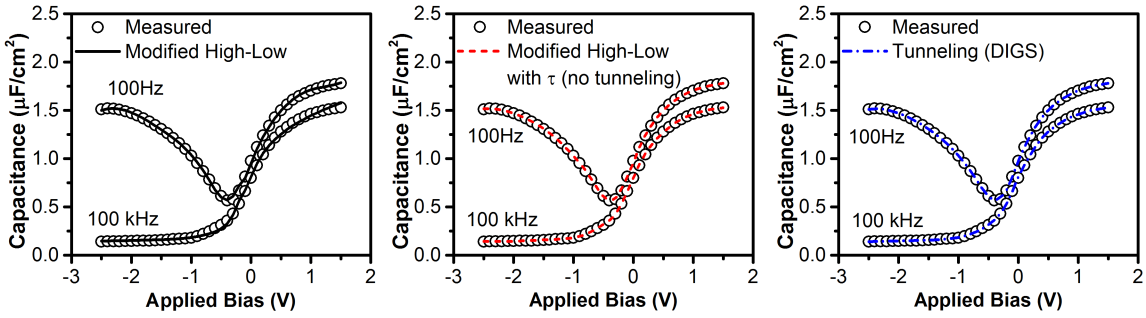


Figure 3.17. Fit to $In_{0.53}Ga_{0.47}As$ experimental data using various methods.

Table 3.3. Comparison of $In_{0.53}Ga_{0.47}As$ C-V analysis using different methods

	Method 1	Method 2	Method 3
EOT (nm)	1.20	1.54	1.69
Doping (cm^{-3})	2.4×10^{17}	7.7×10^{16}	1.5×10^{17}
RMS error	1.6%	0.5%	0.3%

In the first method, it was assumed that all of the D_{it} can respond to the AC signal at 100 Hz, i.e. $1/C = 1/C_{ox} + 1/(C_s + C_{it})$. The CV curve measured at 100 kHz has no

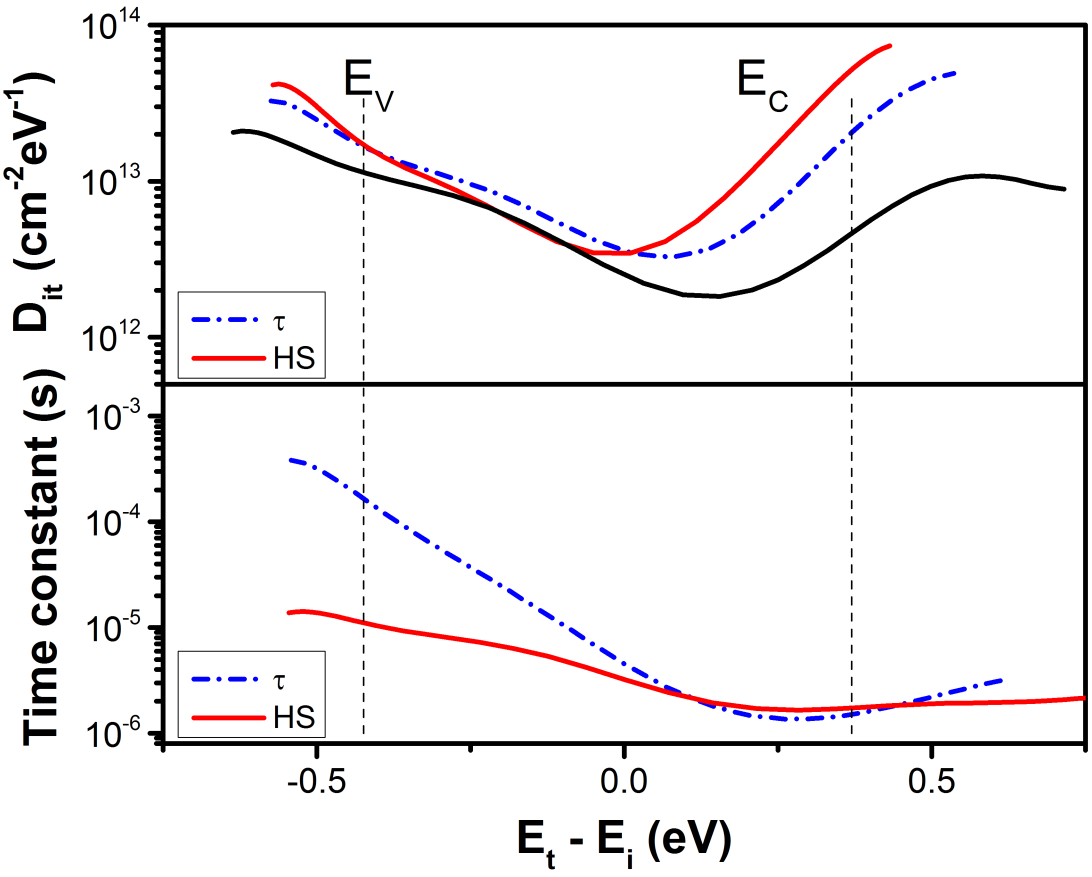


Figure 3.18. Extracted interface state density profile from $In_{0.53}Ga_{0.47}As$ experimental data using various methods.

D_{it} response to the AC signal, i.e. $1/C = 1/C_{\text{ox}} + 1/C_s$ with the D_{it} impacting the surface potential only. The resultant fitting is inaccurate, especially for the high-frequency C-V profile. The EOT extracted using this method is smaller than the expected EOT from the thicknesses of the deposited dielectric layers. From observing where the fitted data does not match the experimental curve, it is obvious that the 100 kHz is not the "true" high-frequency C-V profile as it shows a slight "hump" from the interface states, indicating that the D_{it} can respond to the AC signal even at 100 kHz. This means that for accurate analysis and extraction from the measured data, we must account for the AC C_{it} response for both frequencies.

Enabling CV ACE to utilize the frequency dependent C_{it} even for the 100 kHz curve using (3.24), results in a significantly better fit (RMS error 0.5%). Also, the extracted EOT is much closer to the value expected from the actual deposited gate stack. However, the experimental curves are observed to have a large frequency dispersion in the accumulation region which indicates that the DIGS model should probably be utilized by calculating the capacitance with (3.33). Utilizing the DIGS model, the simulated C-V curves are in excellent agreement with the measured C-V profiles and the extracted EOT and doping density are extremely close to the expected values based on the device fabrication.

Each of the last two extraction methods utilize the trap time constant as a fitting parameter. The interface state distribution from those two models shows a similar shape. However, near the conduction band edge, the DIGS model shows a lower D_{it} value compared to the modified high-low method. This is because in the DIGS model, the frequency dependent response is accommodated by a volumetric defect density due to the ability to tunnel to traps away from the interface. The DIGS model matches with other experimental measures as well. The trap time constant profile extracted using CV ACE matches remarkably measured trap time constants from conductance data [96] as shown in Fig. 3.19. From (3.34), the depth away from the crystalline III-V interface at which the volumetric density of traps can respond is calculated to be ~ 0.3 nm consistent with XPS observations of a disruption of the III-V interface by oxygen [93]. These tunneling distance values are obtained for a κ value of $5 \times 10^7 cm^{-1}$ which is consistent with the values reported in previous work for this semiconductor/dielectric band offset.

The large difference observed in extracted time constant near the valence band from the two models originates from the inherent difference in the methods used. In the 2nd method (modified high low with time constant, frequency dependent C_{it}), the extracted time constant is slower (higher value of time constant), whereas in the DIGS model, it is faster (lower value of time constant) near the valence band. The slower time constant

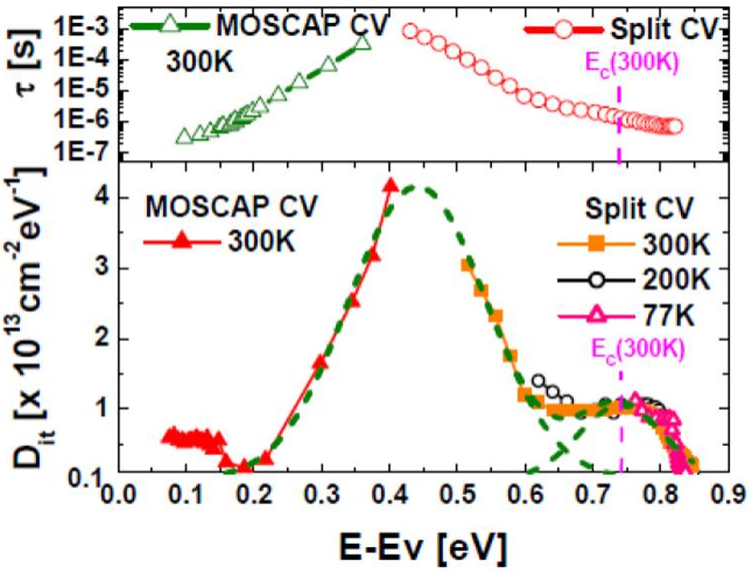


Figure 3.19. Experimentally determined time constant and interface state profile from conductance data ©[2010] IEEE.

extracted from the modified high low with time constant method includes the time it takes for the carriers to tunnel to/from the defects along with the time constant associated with populating/depopulating of the defect states. On the other hand, in the DIGS model, the time constant due to tunneling is incorporated into the model itself and so the extracted time constant in this method is only from the time constant from the populating/depopulating the defect states (which is the more accurate definition of the trap time constant). This trapping/detrapping is much faster than when the tunneling of carriers is included in the time constant and hence the large difference in extracted time constant near the valence band.

3.2.4 Conclusion

In conclusion, CV ACE, has been shown to have enormous flexibility in analyzing experimentally measured CV profiles from MOS devices on a variety of semiconductors with high-k dielectrics. Various models and capabilities for C-V and D_{it} simulation have been

implemented in the program based on the observed nature of these interfaces, including a tunneling model for III-V frequency dispersion. Initial results using CV ACE to analyze high-k devices on Ge and InGaAs exhibit excellent fits with extracted parameters that agree well with both expected values and other experimental observations.

CHAPTER 4

POST ALD PLASMA OXIDATION FOR GERMANIUM SURFACE PASSIVATION

4.1 Introduction

While germanium has a number of attractive properties which make it suitable as a replacement for Si, including its higher electron and hole mobility and compatibility with existing silicon-based technologies, it also suffers from a number of issues, primarily its low thermal budget and a high interface state density. A number of approaches to the passivation of these surface defects have been explored in recent years. It has been shown that thermally grown GeO_2 provides the lowest interface state density [7, 41]. However, GeO_2 is inferior to high-k dielectrics for highly-scaled devices due to its lower dielectric constant. High-k dielectrics provide the physical thickness to reduce leakage current while maintaining the equivalent oxide thickness of a thin GeO_2 layer. However, direct deposition of high-k dielectrics on Ge surfaces result in a poor-quality interface with a high density of electrically active defects [97]. The use of a thin, thermally grown GeO_2 to passivate the Ge surface before high-k deposition is not feasible due to the previously mentioned water solubility as de-ionized Water (DIW) is used in the ALD deposition of high-k dielectrics. Several other dielectric materials have been investigated including ZrO_2 [98] and germanium based dielectrics GeON and Ge_3N_4 [99] although none provide sufficiently low defect densities. Passivation using ozone oxidation also proves to be underwhelming [100, 43, 101]. Metal oxide doped GeO_2 shows to have very good thermal and structural characteristics [102, 103, 104], including reduced solubility in water. However, in these films, the interface passivation is not good enough to be implemented in advanced MOS devices. One of the most promising methods is the growth

of a GeO_2 passivation layer, using post ALD plasma oxidation, as first described by Zhang *et. al* [10]. The plasma post oxidation (PPO) method is particularly interesting because it oxidizes the germanium surface (forming a GeO_x passivation layer) after the ALD deposition of the high-k dielectric, when the solubility of GeO_2 is irrelevant. An oxygen plasma is used, in which the ionized oxygen diffuses through the high-k material, resulting in the growth of GeO_x at the high-k/Ge interface. This results in a high-k/GeO_2/Ge heterostructure which combines the passivation of GeO_2 with the low EOT of the high-k dielectric. Interestingly, even though the passivating layer is not stoichiometric GeO_2, it sufficiently passivates the germanium surface to result in high carrier mobility [105, 8, 106]. The previous studies of this PPO method have used an oxygen plasma generated by electron cyclone resonance (ECR). To integrate this method into large scale semiconductor manufacturing, the use of a more conventional technique such as Plasma Enhanced Chemical Vapor Deposition (PECVD) is of interest. PECVD is already a fundamental technique in microelectronics fabrication and is favored for the large degree of control it provides over the deposition rate and ambient. There has been no previous investigation into the use of PECVD in the PPO passivation of Ge for use in high-k/Ge devices.

4.2 Passivation using N_2O Plasma

N_2O was used as a starting point to test if using PECVD is a valid and feasible technique to achieve this PPO method. N_2O is chosen because it is widely used in the industry as an oxidizer. Pure oxygen is not chosen because of the difficulty in producing a plasma with pure oxygen.

4.2.1 Experiment 1 – Initial Study for Validation

Experiment

In this experiment, four samples have been used to test the validity of the PPO method using N_2O. The samples underwent the following process:

1. Samples were cleaned with DIW for 5 min.
2. ALD deposition
   (a) Sample 1 and 2 – 36 cycles of Al_2O_3 deposition were performed using TMA and DIW precursors.
   (b) Sample 3 and 4 – 5 cycles of Al_2O_3 deposition were performed using TMA and DIW precursors, followed by 25 cycles of HfO_2 deposition using TDMA-Hf and DIW precursors.
3. Plasma oxidation was performed in the PECVD chamber at 250°C with 400 W RF power for 10 min. The gas flow was 500 sccm and the chamber pressure was 500 mTorr. Samples 2 and 4 were exposed to the plasma, while samples 1 and 3 were kept as controls.
4. All samples were analyzed using XPS.

Results and Discussion

In the XPS spectra of the Ge $3d$ core level, as shown in Fig. 4.1, it can be seen that before plasma oxidation, the samples with 36 cycles of Al_2O_3 deposition are dominated by the Ge-Ge substrate peak (doublet at 29.3 eV), along with trace evidence of sub-oxide states at higher binding energy. The sample with 5 cycles of Al_2O_3 + 25 cycles of HfO_2 but no plasma,on the other hand, shows a significant amount of germanium oxide (32.8 eV). Acquisition of the Al

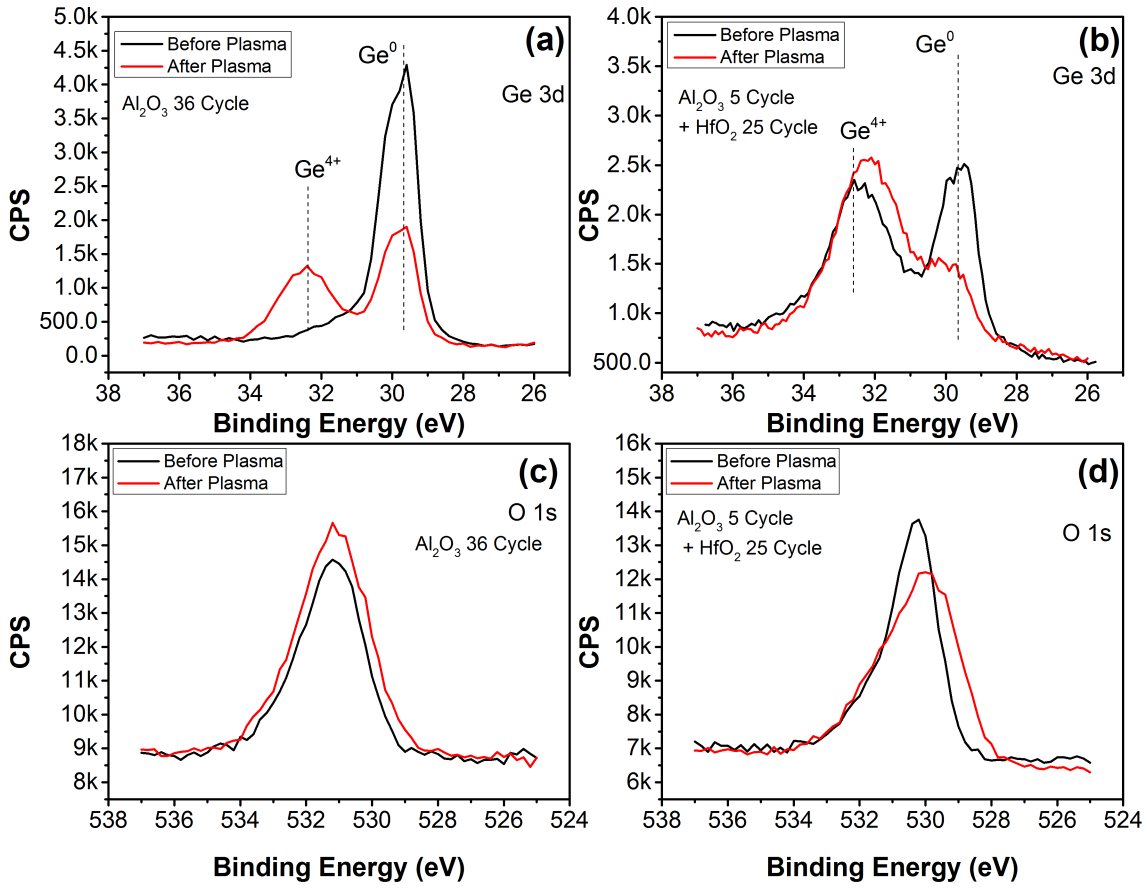


Figure 4.1. Ge 3d and O 1s spectra of before and after N_2O PPO of (a) and (c) Ge with 36 cycles of Al_2O_3 deposited, and (b) and (d) Ge with 5 cycles of Al_2O_3 and 25 cycles of HfO_2 deposited. The large peak of Ge^{4+} confirms oxidation of germanium through the Al_2O_3.

2p spectra for this sample shows no detectable signal indicating that the deposited Al_2O_3 is below the XPS detection limits as shown in Fig. 4.2. This would mean that even if a small amount of Al_2O_3 were deposited it would not be full coverage, and this would then result in oxidation of the Ge upon atmospheric exposure. In both samples, after plasma exposure we see an increase in GeO_x and a decrease in Ge-Ge peak areas which is consistent with the oxidation of the Ge surface. As the GeO_x thickness increases, the Ge-Ge peak is attenuated, leading to the reduction in peak area. The oxidation of the Ge surface following the PPO treatment is confirmed by the increase in the O 1s peak area in both samples. This increase is less noticeable as the O 1s spectra are dominated by the signal from the Al_2O_3 layer. This

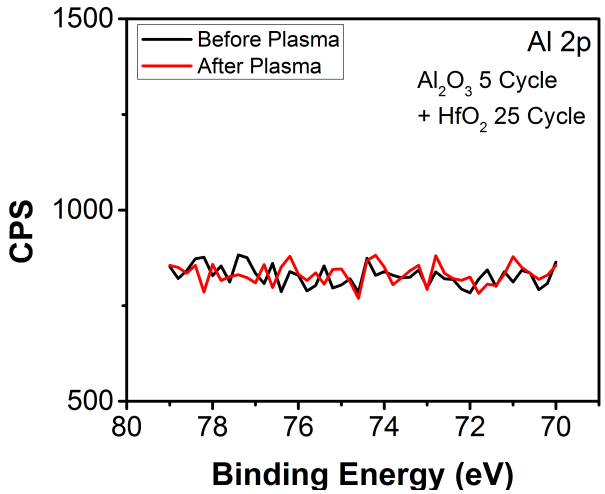


Figure 4.2. Al $2p$ spectra of before and after N_2O PPO of Ge with 5 cycles of Al_2O_3 and 25 cycles of HfO_2 deposited shows absence of Al_2O_3

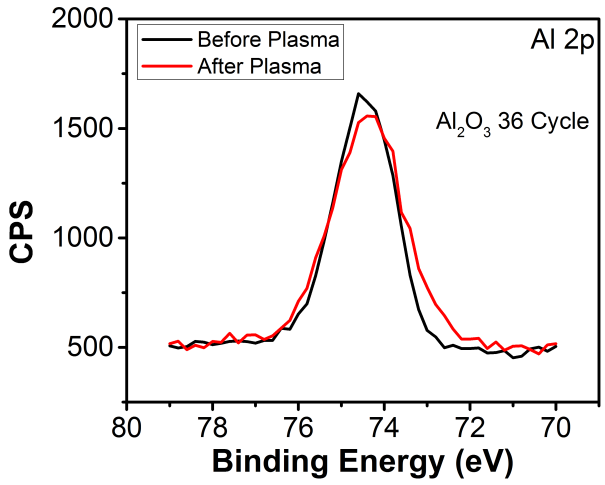


Figure 4.3. Al $2p$ spectra of before and after N_2O PPO of Ge with 36 cycles of Al_2O_3 deposited

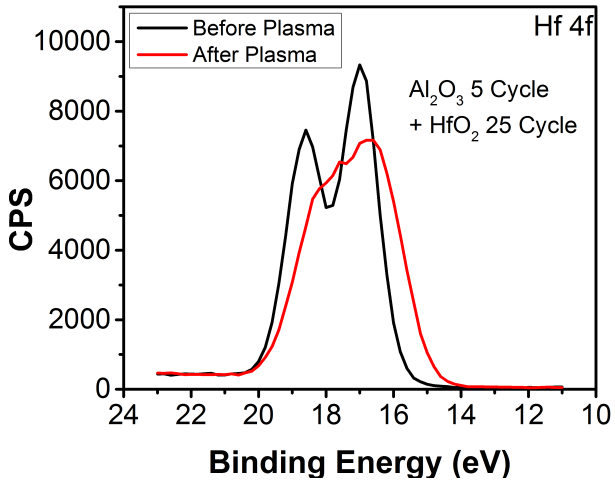


Figure 4.4. Hf 4*f* spectra of before and after N_2O PPO of Ge with 5 cycles of Al_2O_3 and 25 cycles of HfO_2 deposited. Inter-mixing of Hf and germanium is observed.

confirms that the post-ALD plasma oxidation of the buried high-k/Ge interface is possible using PECVD.

The Al 2*p* spectra shown in Fig. 4.3, broadens after plasma exposure. However, the total area of the peak does not change, possibly indicating that there is some change in the local bonding structure due to the diffusion of the oxygen ions through the Al_2O_3 layer. The Hf 4*f* spectra shown in Fig. 4.4 are interesting because they show a significant change after exposure to the N_2O plasma. This is consistent with similar behavior observed in [10], where the absence of an Al_2O_3 layer between Ge and HfO_2 causes intermixing of germanium oxides and hafnium oxide forming HfGeO during plasma exposure, and creating a large number of electrically active defects. For the implementation of PECVD for the PPO and passivation of Ge in advanced MOS devices, this inter-mixing needs to be prevented and it is suggested in [10] that Al_2O_3 may be used to prevent the inter-mixing of germanium and hafnium oxides. In the following experiments, an Al_2O_3 interlayer between the Ge and HfO_2 layers is used unless otherwise mentioned.

Table 4.1. Sample split for experiment 2

Sample	Al_2O_3	HfO_2	Pressure	FGA
1	0 cycle	25 cycle	500 mTorr	350°C 30 min
2	10 cycle	25 cycle	500 mTorr	350°C 30 min
3	20 cycle	25 cycle	500 mTorr	350°C 30 min
4	20 cycle	25 cycle	200 mTorr	350°C 30 min

In conclusion, exposure to N_2O plasma environment is shown to be viable method to passivate germanium surfaces for MOS device application.

4.2.2 Experiment 2 – Thickness Study of Al_2O_3 as a Barrier Layer

Experiment

As observed in the previous experiment, an Al_2O_3 interlayer is important to prevent inter-diffusion during the plasma processing, and the subsequent formation of HfGeO. However, to achieve an ultra-low EOT, the Al_2O_3 layer needs to be thin. If the Al_2O_3 layer is too thin though, inter-mixing between germanium and hafnium oxides may still occur. The germanium top surface needs to be passivated but excess oxidation will lead to a thicker GeO_x layer, and thus increased EOT. One way to control the oxidation rate is to control the amount of oxidizer in the plasma, in this case N_2O. The amount of N_2O present can be controlled by the chamber pressure. The number of molecules is proportional to the pressure inside the chamber.

In this experiment, the effect of the thickness of the Al_2O_3 layer and the pressure in the PECVD chamber on the electrical characteristics of an MOS structure is tested. The sample split used is described in Table 4.1.

The samples were fabricated using the following process:

1. Ge p-type (100) wafers with resistivities of 0.01-0.04 ohm-cm (corresponding to doping densities of $10^{17} - 10^{18} cm^{-3}$) were used.

2. All samples were cleaned sequentially with acetone, isopropyl alcohol (IPA), and DIW for 2 minutes each.

3. ALD

   (a) Either 0/10/20 cycles of Al_2O_3 were deposited using TMA and DIW precursors.

   (b) 25 cycles of HfO_2 were deposited using TDMA-Hf and DIW precursors.

4. Plasma oxidation parameters:

   (a) The chamber pressure was 200 mTorr, the flow rate of N_2O was 400 sccm, the plasma power was 100 W, and the exposure time was 30 sec.

   (b) The chamber pressure was 500 mTorr, the flow rate of N_2O was 400 sccm, the plasma power was 100 W, and the exposure time was 30 sec.

5. The metal deposition consisted of 10 nm of TiN followed by 100 nm of W.

6. The devices were lithographically patterned and etched.

7. The backside metal was deposited, consisting of 15 nm of Ti followed by 50 nm of Al.

8. The samples underwent a forming gas anneal (FGA) at 350°C for 30 min.

C-V measurements were performed using a Cascade probe station equipped with an Agilent 4284 LCR meter. The measurements were performed at room temperature and using frequencies from 100 Hz to 1 MHz.

Results and Discussion

The measured C-V profiles as a function of the number of Al_2O_3 cycles is shown in Fig. 4.5. As expected, in sample 1, where there is no Al_2O_3 layer there is a considerable leakage current and, as a result, the C-V profile is very noisy. Intermixing between the GeO_x and

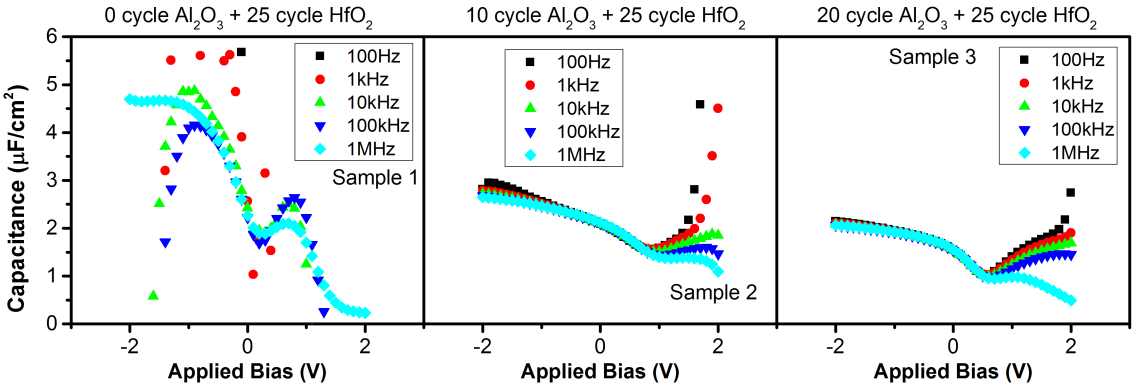


Figure 4.5. Measured C-V data of samples 1, 2 and 3 showing the impact of the number of Al_2O_3 cycles on the device performance. 20 cycle Al_2O_3 shows the best C-V characteristics.

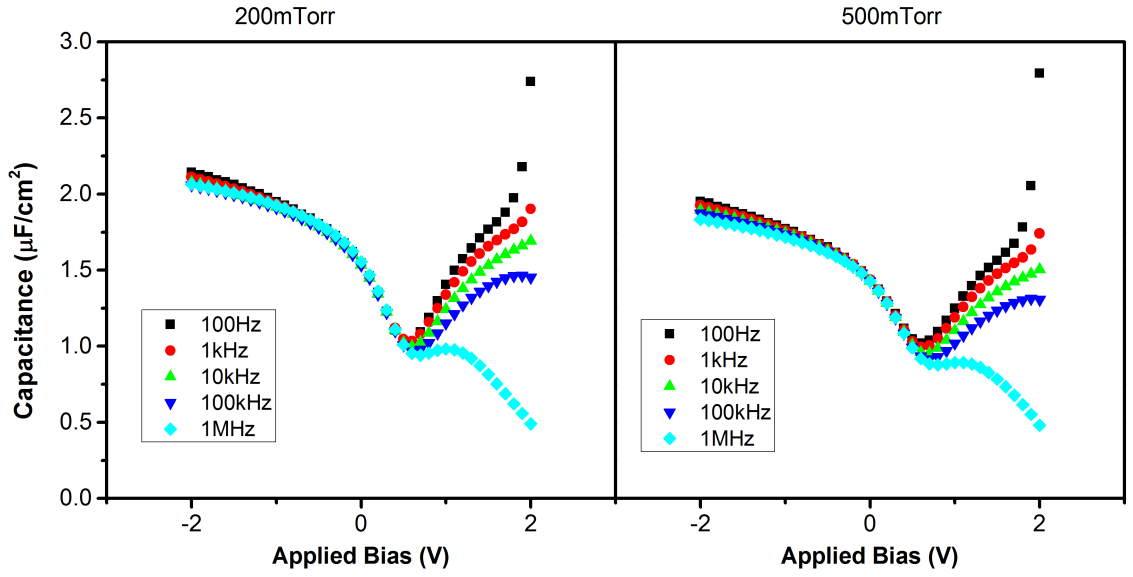


Figure 4.6. Measured C-V data of samples 4 and 5 shows the minimal effect of chamber pressure on the device performance

HfO_2 layers, which may result in the formation of some HfGeO as previously reported, may also play a role. In sample 2 with 10 cycles of Al_2O_3 , the electrical characteristics have improved to some degree, as seen by the noise reduction. However, from the shape of the C-V curves for sample 2, there is a high amount of leakage and a large response in the inversion region caused by a large density of interface states which may be caused by partial inter-mixing of germanium oxide and hafnium oxide. This suggests that the thickness of the ALD Al_2O_3 layer is not sufficient in this sample. The maximum value of capacitance (and the high leakage current) in this sample suggests that the Al_2O_3 layer is thin. C-V plots of sample 3 show a stark improvement in the electrical characteristics compared to previous samples, especially in the accumulation region, suggesting that 20 cycles of Al_2O_3 is sufficient to reduce the leakage current and may also help in preventing the inter-mixing of GeO_x and HfO_2. However, there is still a large defect response present in the 0.5-2 V bias range, indicating an unpassivated germanium surface and the estimated thickness from the C-V profile indicates no EOT degradation, even though the samples are exposed to a N_2O plasma for 30 seconds. The impact of chamber pressure is shown in Fig. 4.6. Sample 4, which was exposed to plasma at 200 mTorr pressure, shows a slight increase in the maximum capacitance compared to sample 3, which was exposed to plasma at 500 mTorr pressure. However, the difference is within the experimental error (typically 10% for deposition processes). The EOT degradation estimated from the maximum capacitance in accumulation indicates that both samples have an oxidized Ge interface. However, a large defect response remains indicating there is still a high density of interface states present at the Ge interface in both samples. This experiment has shown that, the Al_2O_3 thickness is important for the PPO process. Additionally, the ambient pressure has little impact on the interface properties indicating that the oxidation rate is not greatly affected by the ambient pressure.

4.2.3 Experiment 3 – Effect of Forming Gas Temperature

Forming Gas Anneal

In modern semiconductor fabrication, many deposition and etch processes are typically performed using a plasma, e.g., sputter deposition of metals and etching of metals. As a result, the gate dielectric is exposed to the high energy particles, which can damage the dielectric and can form interface traps at the semiconductor/dielectric interface. A forming gas anneal is widely used in device fabrication to passivate the plasma induced damage at the interface [107]. Forming gas is a mixture of hydrogen and nitrogen. Hydrogen is well known to react violently with oxygen in the atmosphere and is considered extremely hazardous. However, if hydrogen is mixed with N_2, the mixture is much more stable. Usually in a forming gas, the most common composition is 5% H_2, 95% N_2.

Experiment

In this experiment, the effect of increased temperature in a forming gas anneal (FGA) is investigated. A FGA step at the end of fabrication is used in all of the samples in this chapter to heal any damage caused by the gate metal deposition. The previously discussed samples used an FGA temperature of 350°C, but here we investigate the impact of the FGA temperature on the resultant device performance. Sample 1 was annealed at 350°C in forming gas, while sample 2 was annealed at 400°C. The rest of the process flow is the same as that described before in section 4.2.2.

Results and Discussion

In Fig. 4.7, the measured C-V profile of samples 1 and 2 are shown. In sample 1, the 1 MHz profile shows a D_{it} hump in the depletion region, which is substantially reduced in sample 2, indicating that damage formed in the dielectric during the gate metal sputter deposition

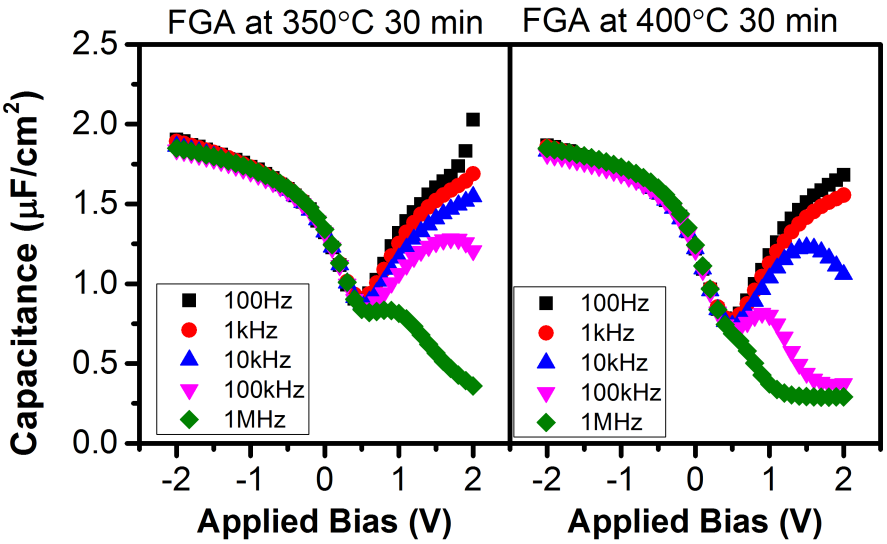


Figure 4.7. Measured C-V data of samples 1 and 2 comparing the effect of FGA at different temperatures. FGA at 400°C shows much better 'healing' compared to FGA at 350°C.

process is healed further by the higher FGA temperature. This is consistent with previous reports of the FGA treatment of MOS devices [107]. Due to the improved characteristics provided by the 400°C FGA anneal, this will be the FGA temperature used in all subsequent devices in this chapter.

4.3 Passivation using 25%O_2/Ar Plasma

As discovered in the previous experiments, plasma oxidation using N_2O provided an improved interface in addition to challenges with uniformity and repeatability. There are several alternative gases that can be used for this PPO method. 25%O_2/Ar was chosen as the next oxidizer. However, the PECVD tool (PD01 in the UTD clean-room) used in the previous experiments is not equipped to handle any oxidizing gas other than N_2O. Recently, the clean-room facility at UTD acquired another similar PECVD (PD02) tool fitted with a wider range of gases and that is flexible enough to add new gases as necessary. We decided to use 25%O_2/Ar balanced in Ar as suggested in numerous reports on PPO of Ge by the Takagi group [26, 22, 27]. A higher percentage of oxygen or pure oxygen was not attempted

as, again, it is hard to ignite the plasma with a high proportion of O_2. Argon is one of the easiest gases for plasma ignition so this O_2/Ar mixture is a natural choice.

4.3.1 Experiment 1 – Initial Study to Validate the use of 25% O_2/Ar

Experiment

In this experiment, another validation study is performed for the viability of using 25% O_2/Ar to passivate the germanium interface using PPO. For a complete understanding of the similarities and differences between the use of N_2O and 25% O_2/Ar in the PPO process the following samples were fabricated. A range of different plasma powers and exposure times were explored.

1. Ge p-type (100) wafers with resistivities of 0.01-0.04 ohm-cm (corresponding to dopant densities of $10^{17} - 10^{18} cm^{-3}$) were used.
2. The samples were cleaned sequentially with acetone, IPA, and DIW for 2 minutes each.
3. ALD
   (a) 20 cycles of Al_2O_3 were deposited with TMA and DIW precursors.
   (b) 25 cycles of HfO_2 were deposited with TDMA-Hf and DIW precursors.
4. Plasma oxidation parameters
   (a) The chamber pressure was 200 mTorr and the 25% O_2/Ar flow rate was 400 sccm.
   (b) The plasma powers used were 100 W, 200 W, 300 W, and 400 W.
   (c) The exposure times attempted were 5 s, 15 s, and 30 s.
5. The metal deposition consisted of 10 nm of TiN and 100 nm of W.
6. The devices were lithographically patterned and etched.

7. The backside metal was deposited, consisting of 15 nm of Ti and 50 nm of Al.

8. The sample underwent FGA at 400°C for 30 min.

Results and Discussion

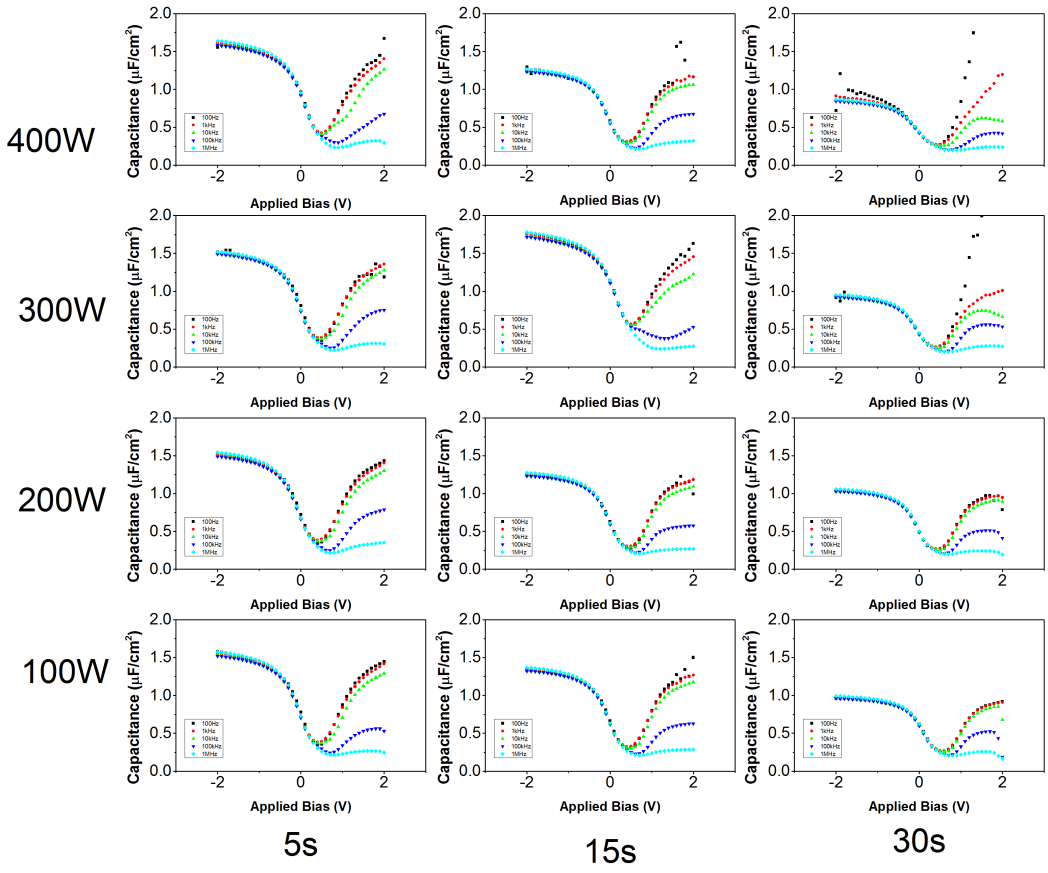


Figure 4.8. Measured C-V data of samples 1 and 2 comparing the effect of FGA at different temperatures

Discussion

In Fig. 4.8, the measured C-V data is shown for a range of powers and for different times. From the C-V plots, it can be seen that a drastic improvement in the quality of the C-V curves is seen in comparison to the PPO process using N_2O, indicating that the 25% O_2/Ar process

is much more effective at passivating the Ge interface. EOT degradation does occur and is observed to be independent of the plasma power used but dependent on the PPO exposure time. It is expected that GeO_x growth would be linearly dependent on the plasma exposure time. However, independence of the power in the plasma power was not expected. The higher the plasma power, the higher the density of free radicals in the plasma. Consequently, it was expected that with an increase in plasma power, the GeO_x growth should increase and subsequently a decrease in the maximum accumulation capacitance would be observed. The sample exposed to 300 W plasma for 15 sec shows a different defect response in positive bias leading to concerns about process uniformity and repeatability.

4.3.2 Experiment 2 – Repeatability Study

Experiment

In this experiment, the previous study was repeated to investigate the repeatability of the PPO process using 25% O_2/Ar . Additionally, a change in plasma pressure was also attempted as a solution to the potential non-repeatability issue.

1. Ge p-type (100) wafers with resistivities of 0.01-0.04 ohm-cm (corresponding to dopant densities of $10^{17} - 10^{18} cm^{-3}$) were used.
2. The samples were cleaned sequentially with acetone, IPA, and DIW for 2 minutes each.
3. ALD
   (a) 20 cycles of Al_2O_3 were deposited with TMA and DIW precursors.
   (b) 25 cycles of HfO_2 were deposited with TDMA-Hf and DIW precursors.
4. Plasma oxidation parameters
   (a) The chamber pressures used were 50 mTorr, 200 mTorr, and 500 mTorr.

(b) The flow rate 25% O_2/Ar flow rate was 400 sccm.

(c) The plasma powers used were 100 W, 200 W, 300 W, and 400 W.

(d) The exposure times attempted were 5 s, 15 s, and 30 s.

5. The metal deposition consisted of 10 nm of TiN and 100 nm of W.

6. The devices were lithographically patterned and etched.

7. The backside metal was deposited, consisting of 15 nm of Ti and 50 nm of Al.

8. The sample underwent FGA at 400°C for 30 min.

Results and Discussion

In Fig. 4.9 the measured C-V plots of the repeated experiments are shown. Comparing Fig. 4.9 to Fig. 4.8, it can be seen that samples that have gone through the same process have very different C-V profiles. Fig. 4.8 shows lower capacitance values in the 0.5-2 V bias range at higher frequencies compared to Fig. 4.9, due to lower interface defect densities. Also, all of the C-V profiles in Fig. 4.9 show no evidence of EOT degradation compared to the sample not exposed to the plasma in Fig. 4.10. This suggests that the GeO_x passivation layer is not formed in any of the samples shown in Fig. 4.9.

This confirms the concerns over difficulties in getting repeatable plasmas using the PECVD chamber for the PPO process. This is further confirmed, in the sub experiment where the chamber pressure was varied, as shown in Fig. 4.11. A high degradation of EOT is observed in some samples, e.g., the samples exposed to plasma at 200 mTorr pressure and a power of 200 W, 300 W and 400 W. This suggests that in samples with a large EOT degradation, the growth rate of the GeO_x passivation layer is high, estimated to be 1-2 nm/sec. While the samples with zero to little EOT degradation, have little or no passivation layer.

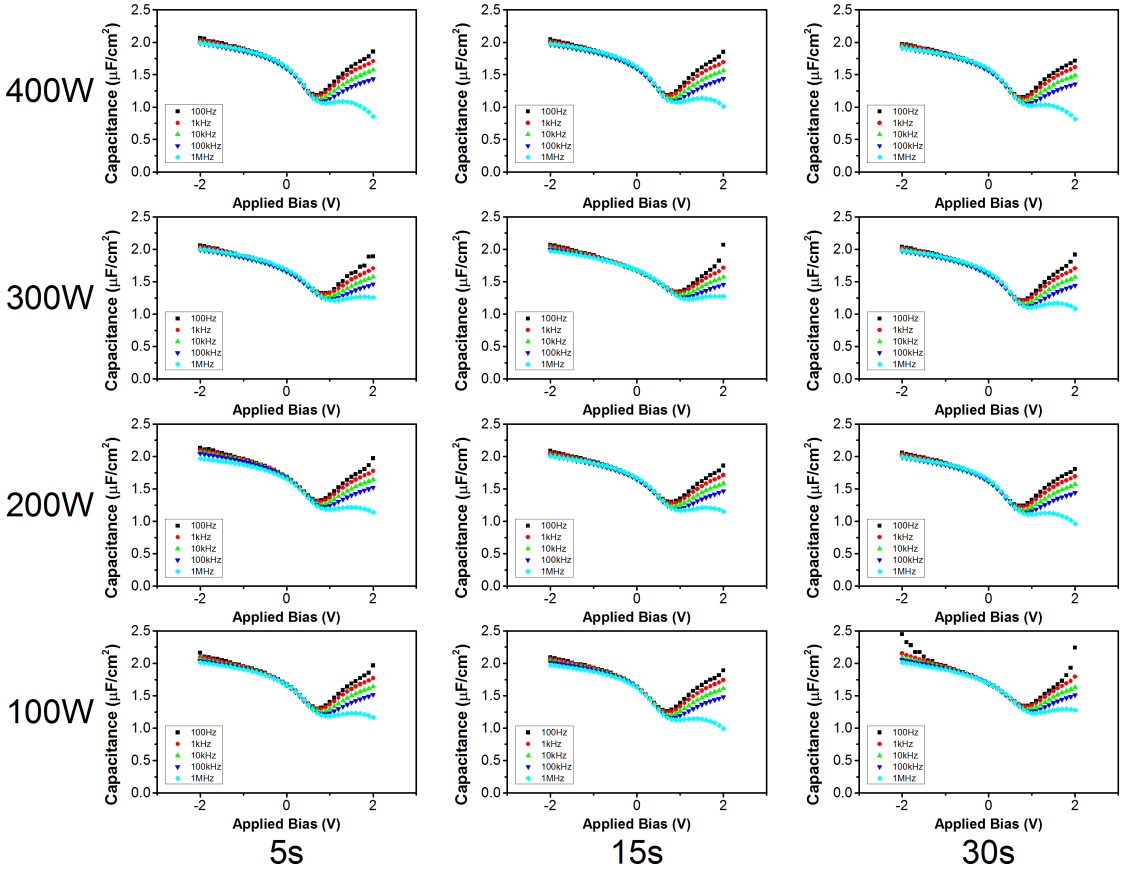


Figure 4.9. Measured C-V data of Ge MOSCAP samples showing the effect of exposure to plasma for different lengths of time and different plasma powers.

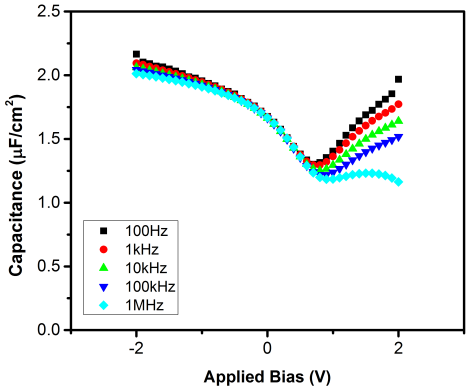


Figure 4.10. Measured C-V data of Ge MOSCAP which is not exposed to plasma during fabrication shows large interface state response.

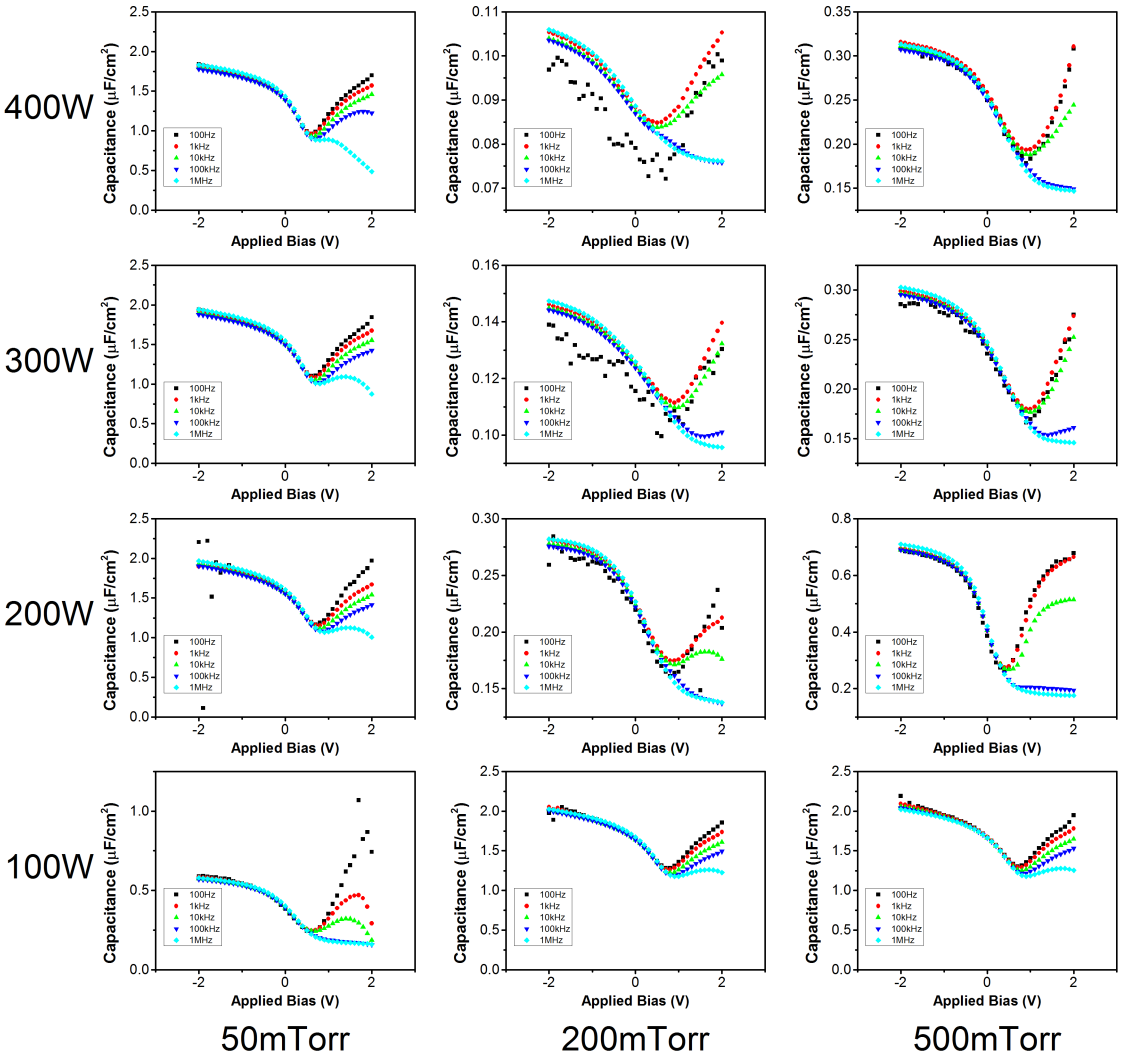


Figure 4.11. Measured C-V data of Ge MOSCAP samples showing the effect of exposure to plasma at various pressures and different plasma powers. Comparing the previous experiments non uniformity and non repeatability is confirmed.

The high growth rate determined above (1-2 nm/sec) is undesirable for low EOT MOS devices as the GeO_x formation is not sufficiently controllable. One way to reduce the growth rate is to use a thicker high-k dielectric to reduce the amount of diffusion of oxygen ions through the high-k to the Ge surface. However, that defeats the goal of achieving low EOT MOS devices using this process. Another way to reduce the rate of oxidation is to limit the number of oxygen atoms in the plasma. As discussed before, a reduction of the chamber pressure will decrease the density of oxygen atoms inside the chamber. However, it is widely known that the uniformity of the deposited film is better at higher pressure. The other way to reduce the oxygen atom density in the plasma is to use a gas with a lower percentage of oxygen.

Additionally, it was observed that at 300 W and 400 W, the plasma becomes unstable with a flickering observed inside the chamber. To improve the plasma stability in the future experiments, a plasma power of less than 250 W is used.

4.4 Passivation using 1% O_2/Ar Plasma

4.4.1 Experiment – Effect of Reduced Oxygen Content

Experiment

As discussed in the previous section, a lower density of oxygen atoms in the plasma may provide better control of the passivation of the germanium surface by controlling the growth rate of the GeO_x. One way of reducing the density of oxygen atoms in the process gas is to dilute the oxygen in a neutral carrier gas, typically argon as it is one of the easiest gases with which to generate a plasma. The previously used 25% O_2/Ar mixture is replaced with a lower oxygen content 1% O_2/Ar in this set of experiments. At the same time, for better uniformity, a much higher chamber pressure was used here compared to the previous experiments. The manufacturer designed the PECVD tool to have a maximum safe operating pressure of 1000 mTorr and we decided to use this chamber pressure in the following experiment.

The total modified process flow is given below:

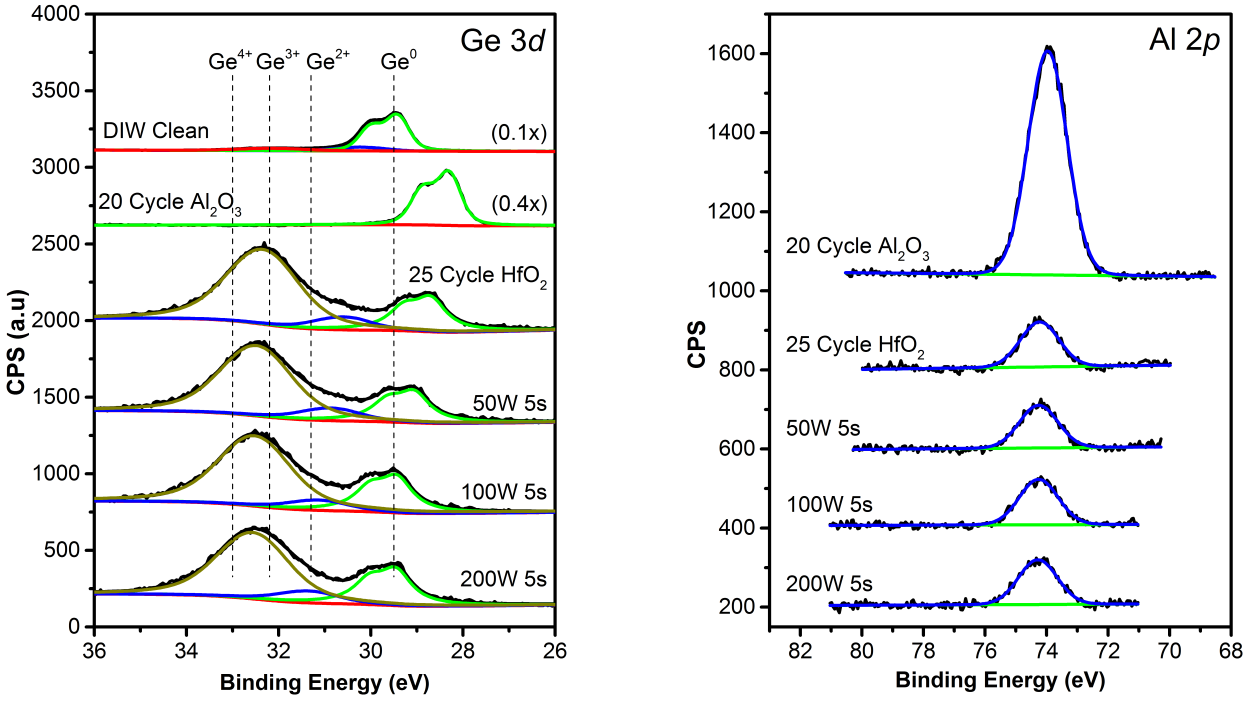
1. Ge p-type (100) wafers with resistivities of 0.01-0.04 ohm-cm (corresponding to dopant densities of $10^{17} - 10^{18} cm^{-3}$) were used.
2. The samples were cleaned sequentially with acetone, IPA, and DIW for 2 minutes each.
3. ALD
   (a) 20 cycles of Al_2O_3 were deposited with TMA and DIW precursors.
   (b) 25 cycles of HfO_2 were deposited with Hf and DIW precursors.
4. Plasma oxidation parameters
   (a) The chamber pressure was 1000 mTorr with 400 sccm flow of 1% O_2/Ar
   (b) The plasma powers used were 50 W, 100 W, and 200 W.
   (c) The exposure times attempted were 5 s, 15 s, and 30 s.
5. The metal deposition consisted of 20 nm of TiN and 40 nm of W.
6. The devices were lithographically patterned and etched.
7. The backside metal was deposited, consisting of 15 nm of Ti and 50 nm of Al.
8. The sample underwent FGA at 400°C for 30 min.

In this experiment, some samples were taken out after the plasma exposure for XPS analysis. The samples taken for XPS analysis are given in Table 4.2.

After the XPS analysis was finished, samples 2, 3, 4, and 5 were returned to the cleanroom and reinserted into the process flow for MOSCAP fabrication. All of the XPS spectra are calibrated by using the adventitious C 1s peak at 284.8 eV.

Table 4.2. Samples for analysis with XPS

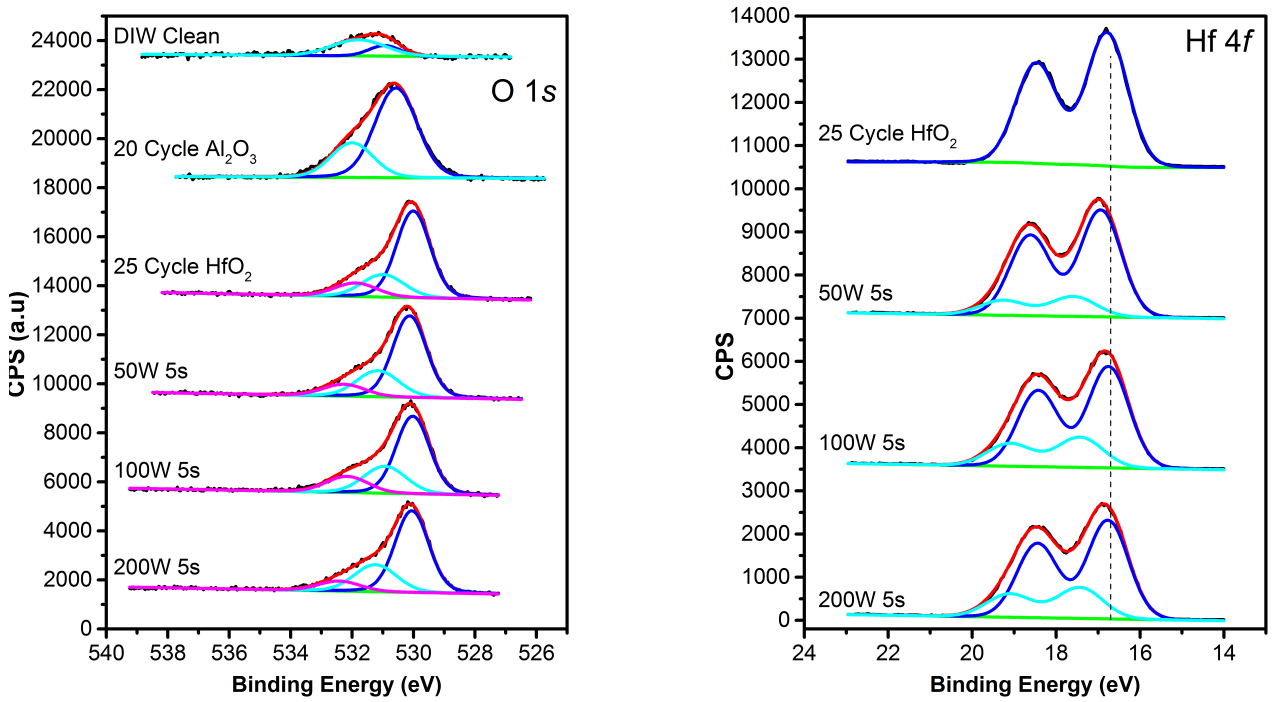
Sample #	ALD	Plasma
0	No ALD	No plasma
1	20 cycle Al_2O_3	No plasma
2	20 cycle Al_2O_3 + 25 cycle HfO_2	No plasma
3	20 cycle Al_2O_3 + 25 cycle HfO_2	50 W 5 sec
4	20 cycle Al_2O_3 + 25 cycle HfO_2	100 W 5 sec
5	20 cycle Al_2O_3 + 25 cycle HfO_2	200 W 5 sec



(a) Ge 3d spectra

(b) Al 2p spectra

Figure 4.12. (a) Ge 3d and (b) Al 2p spectra of samples in different phases of fabrication process. Al_2O_3 deposition shows large amount of fixed charge density. Plasma exposure seems to help reducing fixed charge density. Al_2O_3 seems unaffected to plasma exposure.



(a) O 1s spectra

(b) Hf 4f spectra

Figure 4.13. O 1s and Hf 4f spectra of samples in different phases of fabrication process. both O 1s and Hf 4f spectra appears stable.

Results and Discussion

In Fig. 4.12, the Ge 3d and Hf 4f spectra for the samples are shown. In the Ge 3d spectra, the sample after DIW clean is dominated by the large Ge-Ge substrate peak with a small signal from germanium oxide at higher binding energy. For better comparison with the rest of the samples, the number of counts per second (CPS) in this spectra were divided by 10. This shows that the DIW clean was successful in removing the majority of the surface oxide from the Ge surface. The remaining germanium oxides either remain following the DIW clean or may be formed during the sample transport from the clean room to the load lock of the XPS tool, which takes around 10 minutes.

After 20 cycles of Al_2O_3 deposition, the Ge 3d peak is decreased in intensity due to the attenuation from the deposition of Al_2O_3 on top. This peak has also been divided by a

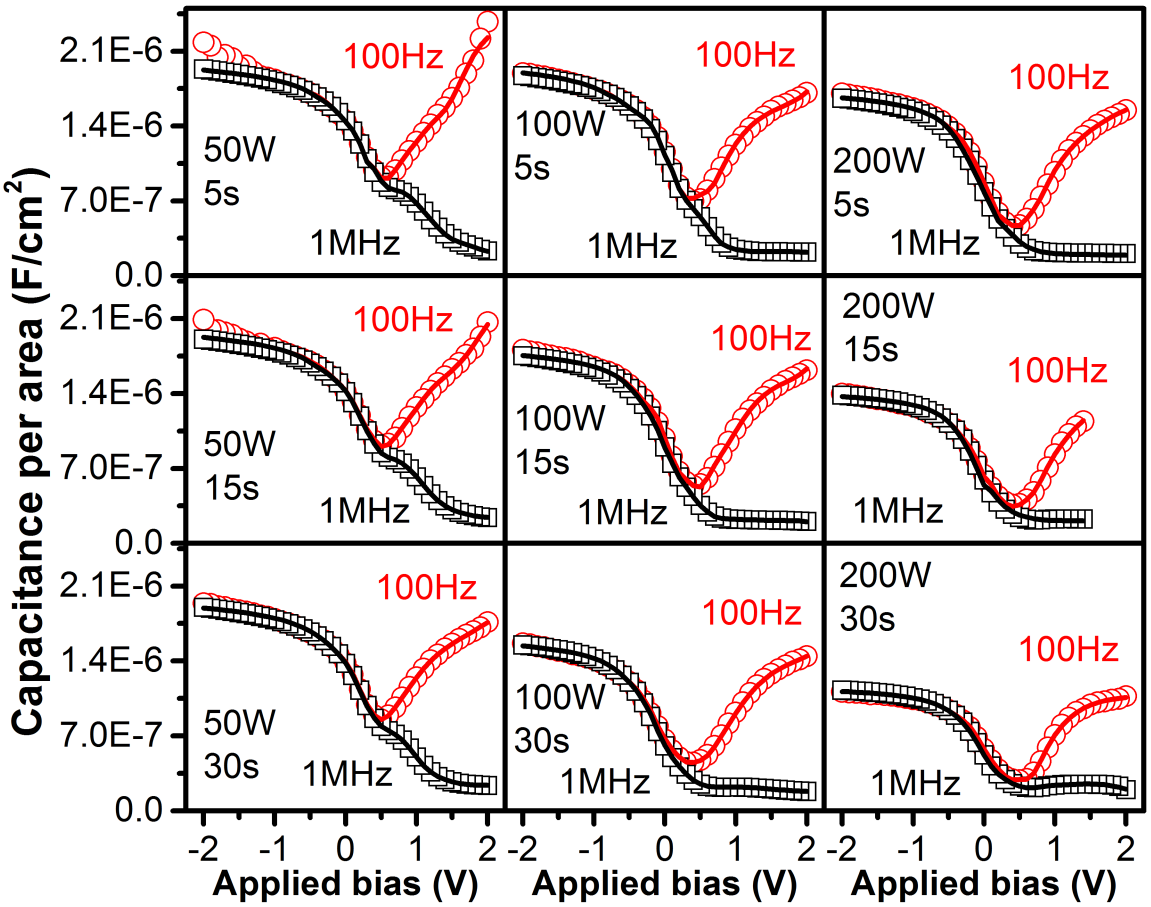


Figure 4.14. Measured and fitted C-V data of germanium samples exposed to plasma shows good passivation characteristics.

factor of 2.5 for easy comparison to the rest of the samples. The germanium oxide intensity is reduced to below the detection limit, suggesting that the germanium oxides are consumed during the Al_2O_3 deposition process. This 'self cleaning effect' of the TMA used in the ALD Al_2O_3 process is well known to scavenge oxygen from the native oxide of the substrate [53]. The Ge $3d$ peak for this sample is shifted to lower binding energy by 1.0 eV. According to [108, 109], Al_2O_3 contains negative fixed charge, mainly originating from excess oxygen close to the Al_2O_3/Ge interface. This negative charge is responsible for the observed peak shift to lower binding energy. The XPS spectra do indicate the presence of excess oxygen in

the deposited Al_2O_3 consistent with oxygen interstitials previously observed in ALD grown Al_2O_3.

From the Al $2p$ spectra in Fig. 4.12b, a large peak is observed, consistent with the deposition of Al_2O_3. For this sample, in the oxygen spectra, the peak can be deconvoluted into two peaks. However, as the Ge $3d$ spectra does not show any oxidation states, it can be deduced that the main peak at 530 eV is from Al_2O_3, while the other peak may be simply due to adsorbed C-O or O-H.

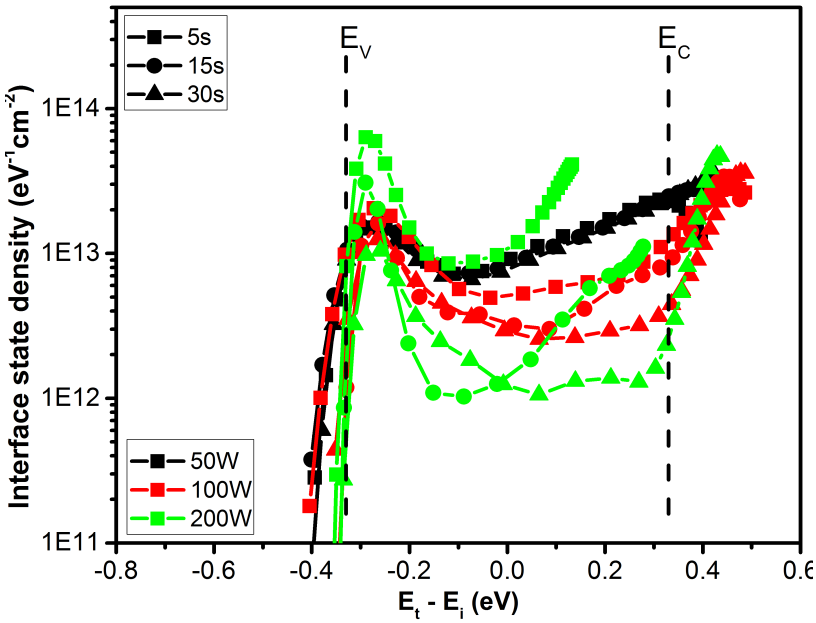


Figure 4.15. Extracted D_{it}

In the next sample, 25 cycles of HfO_2 were deposited on top of the Al_2O_3 using ALD. The Hf $4f$ spectra is shown in Fig. 4.13b. From the Hf $4f$ spectra, a sharp doublet is observed, indicating the deposition of a good quality HfO_2. The O $1s$ spectra shows an additional peak in this sample compared to the previous sample, which is consistent with the presence of an additional oxide, from the deposited HfO_2. In the Ge $3d$ spectra, two peaks related to Ge-O bonds are present, the peak at 32.8 eV is due to the GeO_2, while the peak at 31.0 eV is due to Ge sub-oxides. As the HfO_2 deposition process consists of pulses of DIW vapor, this DIW

vapor can diffuse through the Al_2O_3 layer and oxidize the germanium top surface. In the Al $2p$ spectra, the Al $2p$ peak intensity is suppressed by the presence of the HfO_2 layer on top, but the peak shape remains unchanged. From the Ge $3d$ spectra, the germanium bulk peak position is moved to a slightly higher binding energy compared to the previous sample, where only Al_2O_3 was deposited. This suggests that the negative fixed charges are either removed by the HfO_2 deposition process or the HfO_2 layer consists of a significant amount of positive fixed charges that results in a zero-net charge, as previously reported in [108].

After the HfO_2 deposition, the sample is exposed to 50 W of 1% O_2/Ar plasma for 5 sec. In this sample, the Al $2p$ spectra remains identical to the sample before plasma exposure, indicating no reaction or damage to the Al_2O_3 layer due to plasma exposure. The Hf $4f$ peak, on the other hand shows a shift to higher binding energy and peak broadening which can be fitted with a second peak. The appearance of this second peak may be attributed to damage from the plasma exposure or the formation of a thin layer of HfAlO at the interface of Al_2O_3 and HfO_2. However, there is no evidence of HfAlO formation in the Al $2p$ spectra. Additionally, the Ge $3d$ spectra shows a slight shift of the bulk germanium peak position to higher binding energy compared to the previous sample, which was not exposed to the plasma process. The germanium oxide peaks remain the same as the sample which was never exposed to plasma, indicating that the 50 W plasma used in this sample may not be adequate for germanium surface passivation. This is confirmed by the C-V measurement shown in Fig. 4.14, where the C-V profile for the samples exposed to 50 W plasma for 5, 15, and 30 sec shows no improvement in D_{it} reduction or EOT degradation.

In the samples exposed to plasma with 100 W and 200 W of power, the Ge^0 peaks shift to higher binding energy, reaching the same position as the Ge^0 peak in the DIW cleaned sample. This indicates a continued neutralization of the oxide fixed charges as a function of plasma power. The O $1s$ and the Al $2p$ spectra in these samples are virtually identical to the sample not exposed to plasma. This shows the stability and durability of the Al_2O_3

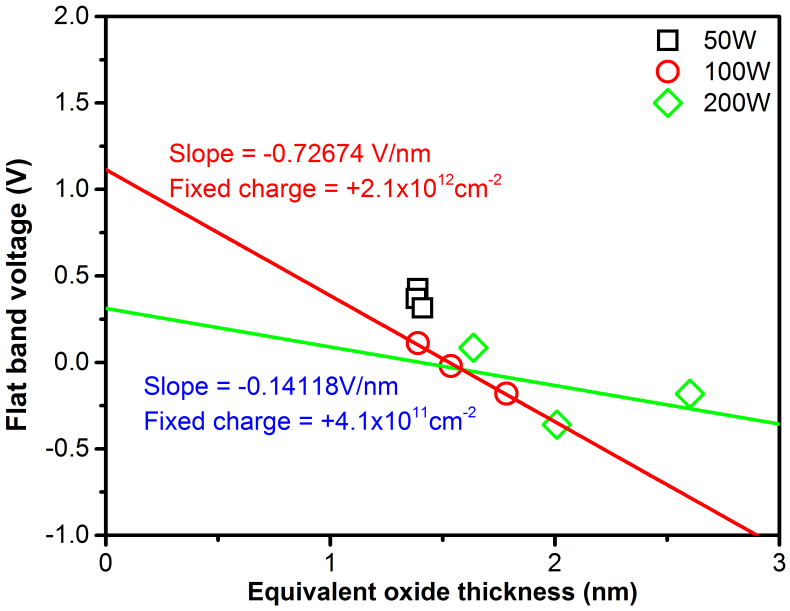


Figure 4.16. Flat band voltage vs. EOT plot shows the fixed charge density in the gate stack. 200 W samples show higher density of fixed charge.

layer to the plasma exposure. The Hf $4f$ spectra, however, shows the same peak broadening observed in the previous sample, which was exposed to 50 W plasma. From the C-V data in Fig. 4.14, the samples exposed to 100 W and 200 W plasma, show a significant improvement over the sample exposed to 50 W plasma. A reduction in the D_{it} 'hump' in the depletion region of the C-V profile measured at 1 MHz is observed for both samples, but, in the sample exposed to 200 W plasma, it is completely gone. In the sample exposed to 100 W plasma a small 'hump' is still observed. This indicates that for the sample exposed to 200 W plasma for 5 sec, the passivation of the Ge top surface is improved compared to the sample exposed to the 100 W plasma. This is evident in the C-V measurement which is much more sensitive to defects compared to XPS, where we don't see a significant difference in the Ge $3d$ spectra between these two samples.

In the samples exposed to 100 W plasma for 15 sec, the D_{it} 'hump' in the C-V profile measured at 1 MHz is completely gone, indicating a similar degree of passivation to the sample exposed to 200 W plasma for 5 sec. This is also shown in Fig. 4.15, where the C-V

profiles are fitted and the interface state density profile is extracted using ACE. The two samples – 100 W for 15 sec and 200 W for 5 sec have similar values for the interface state density at the valence band edge and have similar EOT as shown in Fig. 4.17, where the EOT extracted is plotted for different exposure times.

From Fig. 4.17, it can again be seen that the 50 W plasma is not adequate to passivate the germanium surface. For the 100 W and 200 W plasma samples, an almost linear increase in EOT is observed with exposure time. However, as the 200 W plasma has a higher free radical density due to the increased power in the plasma, the growth rate of germanium oxide is almost double (0.04 nm/sec) that of the 100 W plasma (0.02 nm/sec). In both cases, however, the growth is low enough to be easily controllable. However, from the flat band voltage vs. EOT plot in Fig. 4.16, it can be seen that the 100 W plasma samples may have a higher density of positive fixed charge in the gate stack.

From Fig. 4.15, it can be seen that in almost all samples, the interface state density distribution has a peak near the valence band edge. For the 50 W samples, the C-V profiles are nearly identical for all exposure times, resulting in an almost identical interface state density distribution. The 200 W samples have higher D_{it} values near the valence band edge, possibly because of plasma induced damage. For 100 W and 200 W samples, with increased PPO exposure time, the magnitude of the interface state density profile gets significantly reduced. This is most obvious for the sample exposed to plasma at 200 W power, where the D_{it} reduced by an order of magnitude in going from 5 sec to 30 sec of PPO exposure. However, this 200 W plasma for 30 sec also has the highest EOT. For samples exposed to plasma at 100 W, there is an expected decrease in the magnitude of the interface state density with exposure time. However, the peak near the valence band is also present in these samples. Among all these samples, there is a general trend of increased EOT with reduced interface state density. However, for highly scaled devices, both EOT and interface state density need to be low simultaneously. Using this PPO process with 1% O_2/Ar, a good

compromise can be reached by exposing the germanium to a plasma of 200 W for 5 sec or 100 W for 15 sec.

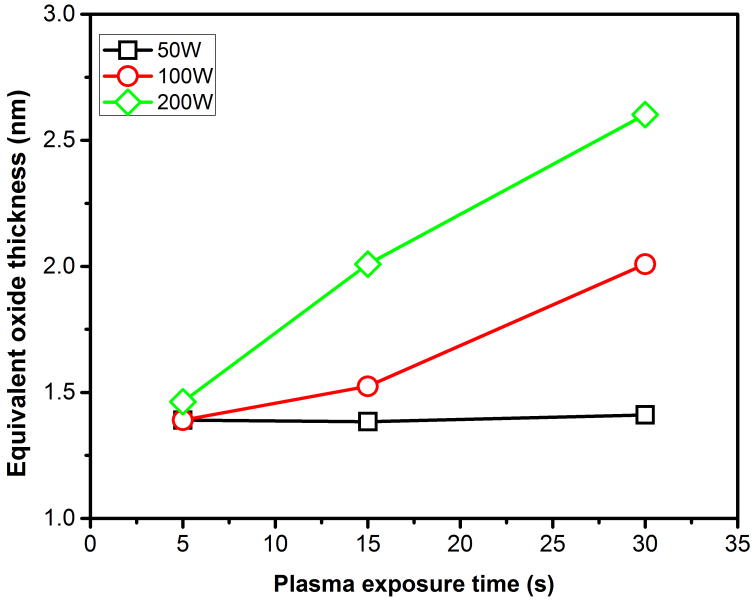


Figure 4.17. EOT increases linearly with plasma exposure time

4.5 Conclusion

To summarize, a new method of germanium passivation using post plasma oxidation (PPO) in a PECVD tool is demonstrated. Initially, N_2O was used to verify the validity of this method. XPS analysis confirmed the ability of PECVD to oxidize the Ge surface after ALD deposition of a high-k dielectric. MOS capacitors were fabricated using this method and were found to have moderately good electrical characteristics with a large number of interface state defects present. An Al_2O_3 interlayer was found to be essential to prevent HfO_2 reacting with germanium substrate and forming HfGeO, while changes in the plasma chamber pressure appear to have no effect on the electrical characteristics of the devices fabricated. Post metal deposition forming gas anneal (FGA) at a temperature of 400°C, was demonstrated to be important in the fabrication of these devices due to the healing effect of

defects originated from the sputter damage during gate metal deposition. This resulted in improved electrical characteristics following the higher temperature (400°C) FGA treatment.

Non-uniform oxidation of the Ge substrate was observed using the N_2O plasma as well as for oxidation using a 25% O_2/Ar mix. Additionally, 25% O_2/Ar was shown to have a much higher oxidation rate, resulting in poor control of the germanium passivation layer thickness. To address these issues, 1% O_2/Ar was used to reduce the oxygen density in the PECVD chamber, which resulted in a much more controllable process. Additionally, increased pressure during oxidation was shown to improve the repeatability and uniformity of the passivation layer. XPS analysis shows that excess oxygen interstitial sites are present in the ALD Al_2O_3, which acts as a fixed charge in the Al_2O_3 layer. However, plasma exposure, combined with the deposition of a HfO_2 layer seems to help in neutralizing this fixed charge. For use of this process into device fabrication, both 100 W and 200 W power may be used.

In conclusion, the post ALD plasma exposure process discussed in this chapter, has been shown to passivate the germanium surface and reduce the interface state density significantly while maintaining a good controllability on the EOT degradation and fixed charge density, under certain conditions. The result of this is an improved high-k/Ge interface applicable to advanced MOS devices.

CHAPTER 5

EFFECTIVE WORK FUNCTION TUNING OF GERMANIUM MOS DEVICES

5.1 Introduction

A low threshold voltage is necessary for optimal MOSFET device performance. Effective work function (EWF) tuning of the high-k/metal gates in an MOS device is an important technique to obtaining low threshold voltages of the device. There are many ways to control the effective work function of a gate stack. The most obvious one is to use a metal with the desired value of the vacuum work function. However, many metals chemically react with the dielectrics which changes the work function and, even without chemical interactions, the work functions of metals are strongly dependent on the surface upon they are deposited.

In advanced silicon based MOS devices, HfO_2 in conjunction with TiN as the gate metal is typically the gate stack utilized. This gate stack has a complex interface with many variables that contribute to the effective work function [110, 54] and significant research has been done on this stack to control the effective work function [111, 112, 113, 114, 115, 116, 117, 118] in silicon based MOS devices.

Researchers at UTD [111], previously demonstrated a method to obtain EWF control in $Si/HfO_2/TiN$ gate stacks by using a low temperature anneal in an N_2 containing ambient. In that work, oxygen atoms diffuse into and through the TiN lattice. During this process, any nitrogen vacancies in the TiN are filled by the oxygen atoms and some N atoms are displaced by O atoms. The displaced N atoms, in turn, diffuse toward the TiN/HfO_2 interface which causes a significant modification of the EWF through dipole formation at the TiN/HfO_2

interface. The electrostatic potential with respect to the Fermi level of the TiN is increased, resulting in an increase in effective work function of the TiN gate metal.

Effective work function tuning in germanium based devices with the HfO_2/TiN stack proves to be much more difficult compared to silicon [119, 120, 121, 122, 123], mostly because the Ge's lower thermal budget and lack of proper Ge surface passivation in low EOT MOS devices [97, 98, 99, 100, 43, 101, 102, 103, 104]. The work in the previous chapter of this dissertation, described a method to passivate Ge using a post-ALD, PECVD generated oxygen plasma. We now utilize that interface to enable Ge/GeO_x/Al_2O_3/HfO_2/TiN gate stacks to study EWF control through low-temperature O_2 containing anneals similar to those used in [111] on Si devices. We fabricate MOS capacitors using these techniques and then utilize CV ACE (described in chapter 3) to extract the EOT and V_{fb} of the devices to determine the EWF as a function of anneal. CV ACE also enables an analysis of any electrical degradation (EOT and D_{it}) caused by the processing.

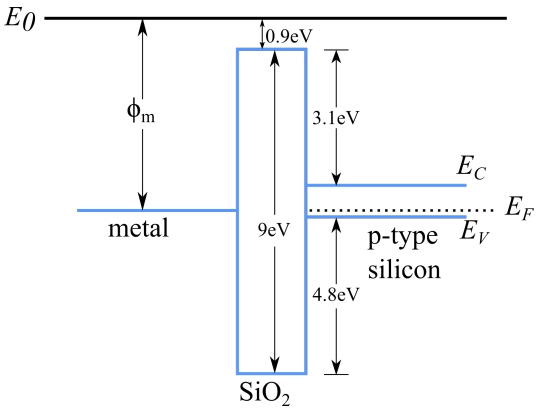


Figure 5.1. Flat band condition in a MOSCAP.

From the flat band condition shown in Fig. 5.1, it can be deduced that the flatband voltage of a MOSCAP is dependent upon the work function fo the metal (ϕ_m) and the semiconductor (ϕ_m),

$$V_{fb} = \phi_m - \phi_s \tag{5.1}$$

However, in practice the gate dielectric may have fixed charge which changes the potential across the gate stack. Accounting for fixed charge (Q_f), the (5.1) can be rewritten as,

$$V_{\text{fb}} = \phi_m - \phi_s - \frac{Q_f}{C_{\text{ox}}} \tag{5.2}$$

which can be rewritten as,

$$V_{\text{fb}} = \phi_m - \phi_s - Q_f t_{\text{ox}}/\epsilon_{\text{ox}}/A \tag{5.3}$$

This equation can be extremely useful for the characterization of an MOS gate stack. By changing the dielectric thickness, t_{ox}, of the MOS system and plotting the extracted flatband voltage as a function of the equivalent oxide thickness of the dielectric, the fixed charge density can be calculated from the slope of the generated curve. Also, by extrapolating the linear fit of that curve to $t_{\text{ox}} = 0$, the effective work function of the gate metal can be calculated if one knows the semiconductor work function (which is typically well known from the doping density). To vary the thickness in this work and enable the methods just described, we varied the PPO exposure times to increase the interfacial GeO_x as demonstrated in chapter 4.

5.2 Experimental Details

The temperatures used in [111] for the post-TiN anneals (400°C and 500°C), while low for silicon are high for germanium's thermal budget [124, 8]. Hence, 350°C , 400°C and 450°C are explored here. The full split of the samples in this experiment is given in Table 5.1. One goal in these techniques is to manipulate the HfO_2/TiN interface with O and N. Therefore, the TiN must be thin enough to enable those species to diffuse through that material. But typically, 10 nm of gate metal is too thin to prevent damage during device measurement and additional environmental contamination during air exposure. To solve this issue, 10 nm TiN is deposited first, followed by the RTA in 100% N_2 and 10% O_2/N_2 at different temperatures.

After the RTA step, the samples were again loaded into the sputter deposition chamber and another layer of TiN metal was deposited followed by 40 nm of W cladding. The full process flow is given below.

1. The wafers are cleaned using acetone, iso-propyl alcohol and DIW for 2 min each.
2. The wafers are loaded into the ALD chamber where 20 cycle of Al_2O_3 and 25 cycle of of HfO_2 is deposited at 250°C.
3. After high-k deposition, the samples were exposed to a 200 W plasma for 10, 20, or 30 sec to plasma post oxidize the germanium.
4. The samples were then loaded into the sputter tool and 10 nm TiN was deposited on all samples.
5. Different samples were then annealed at different temperatures under different atmospheres as given in Table 5.1. Each sample was annealed for 30 sec.
6. The samples were again loaded into the sputter tool to deposit an additional 10 nm TiN and 40 nm of W cladding.
7. Standard photolithography processes were employed to pattern the active area.
8. Areas outside of the active areas were etched in a chlorine based high density plasma.
9. The photoresist was removed and the samples were cleaned of any residue from the lithography and etch process.
10. 15 nm of Ti followed by 50 nm of Al was sputter deposited on the back of the samples to make back contacts.
11. All samples were annealed in forming gas (5% H_2 in N_2) for 30 minutes.

C-V measurements were performed and analyzed using ACE as described in chapter 3.

Table 5.1. Sample definition of effective work function tuning experiment

Plasma	RTA in N_2			RTA in 10% O_2/N_2		
10s	350°C	400°C	450°C	350°C	400°C	450°C
20s	350°C	400°C	450°C	350°C	400°C	450°C
30s	350°C	400°C	450°C	350°C	400°C	450°C

5.3 Results and Discussion

5.3.1 C-V profile

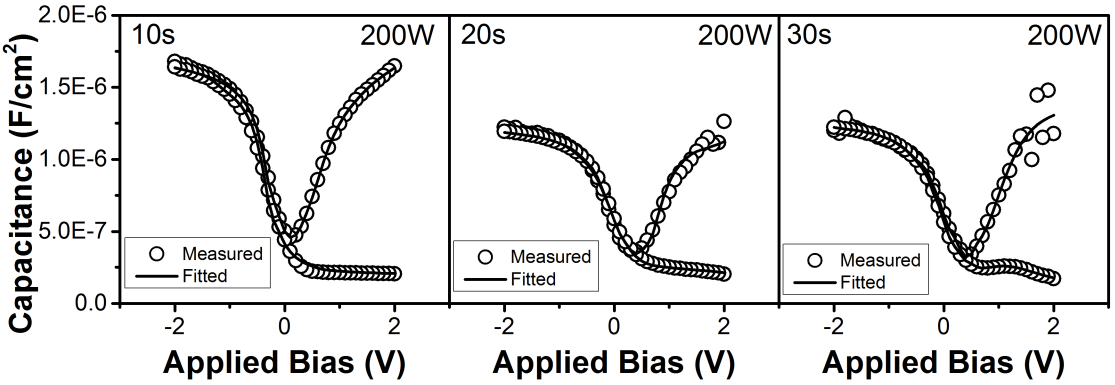


Figure 5.2. C-V profiles of the samples not annealed using RTA shows expected behavior of EOT degradation as a function of plasma exposure time

In Fig. 5.2, the measured C-V profiles of the sample with no anneal, i.e. as deposited, are shown. It can be seen that the simulated C-V profiles from ACE match extremely well to the experimental data. In Fig. 5.2, with an increase in plasma exposure time, the maximum accumulation capacitance decreases. Instead of linear decrease in maximum accumulation capacitance, Fig. 5.2 shows that the samples with 20 and 30 sec plasma exposure have a similar maximum value of the accumulation capacitance, suggesting that the germanium oxide growth is similar in the samples.

In Figs 5.3 and 5.4, the measured C-V profiles of the samples annealed in N_2 and 10%O_2/N_2, respectively are shown. Using CV ACE, the experimental data was analyzed

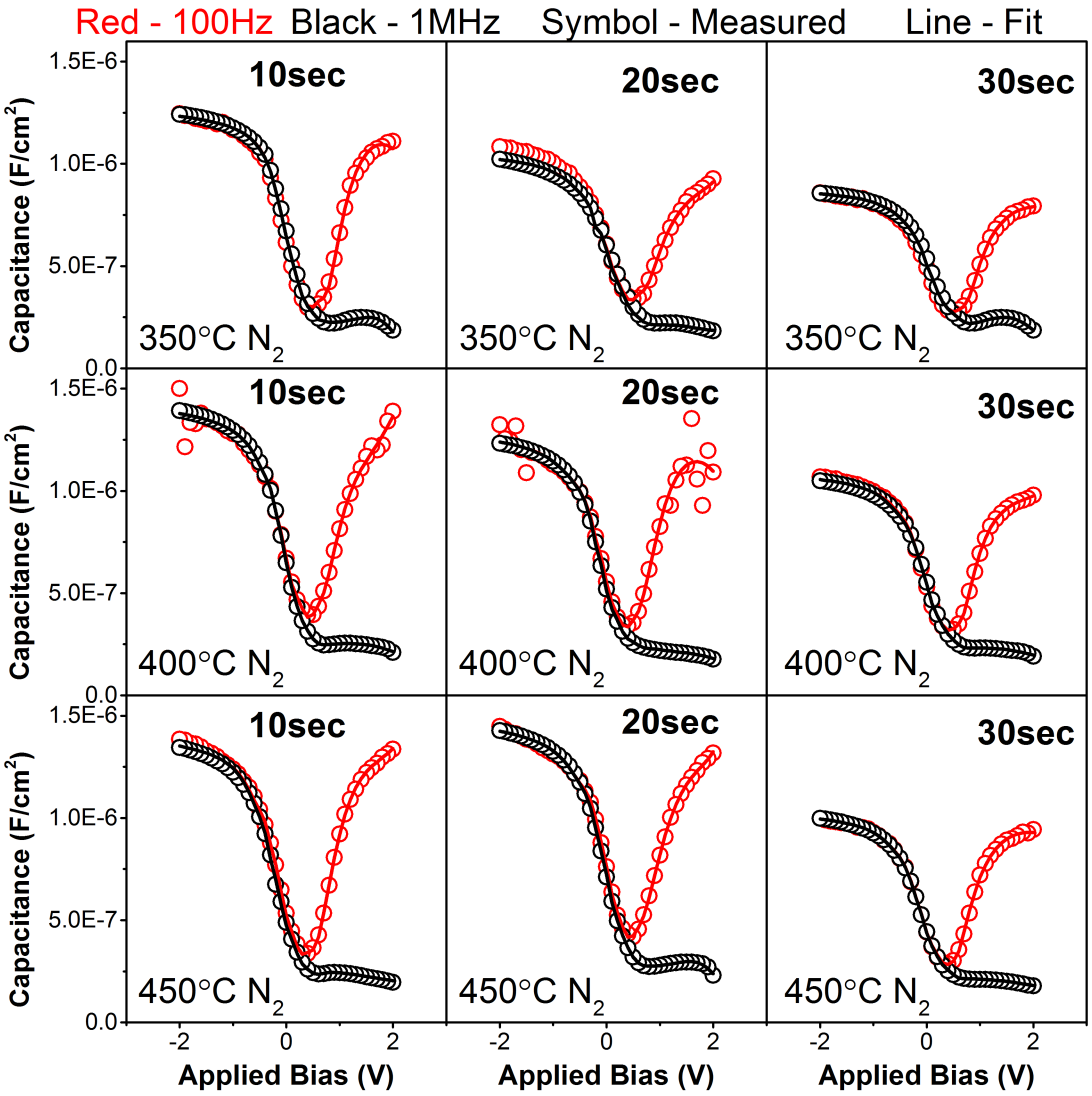


Figure 5.3. C-V profiles of the samples annealed in nitrogen at different temperatures using RTA

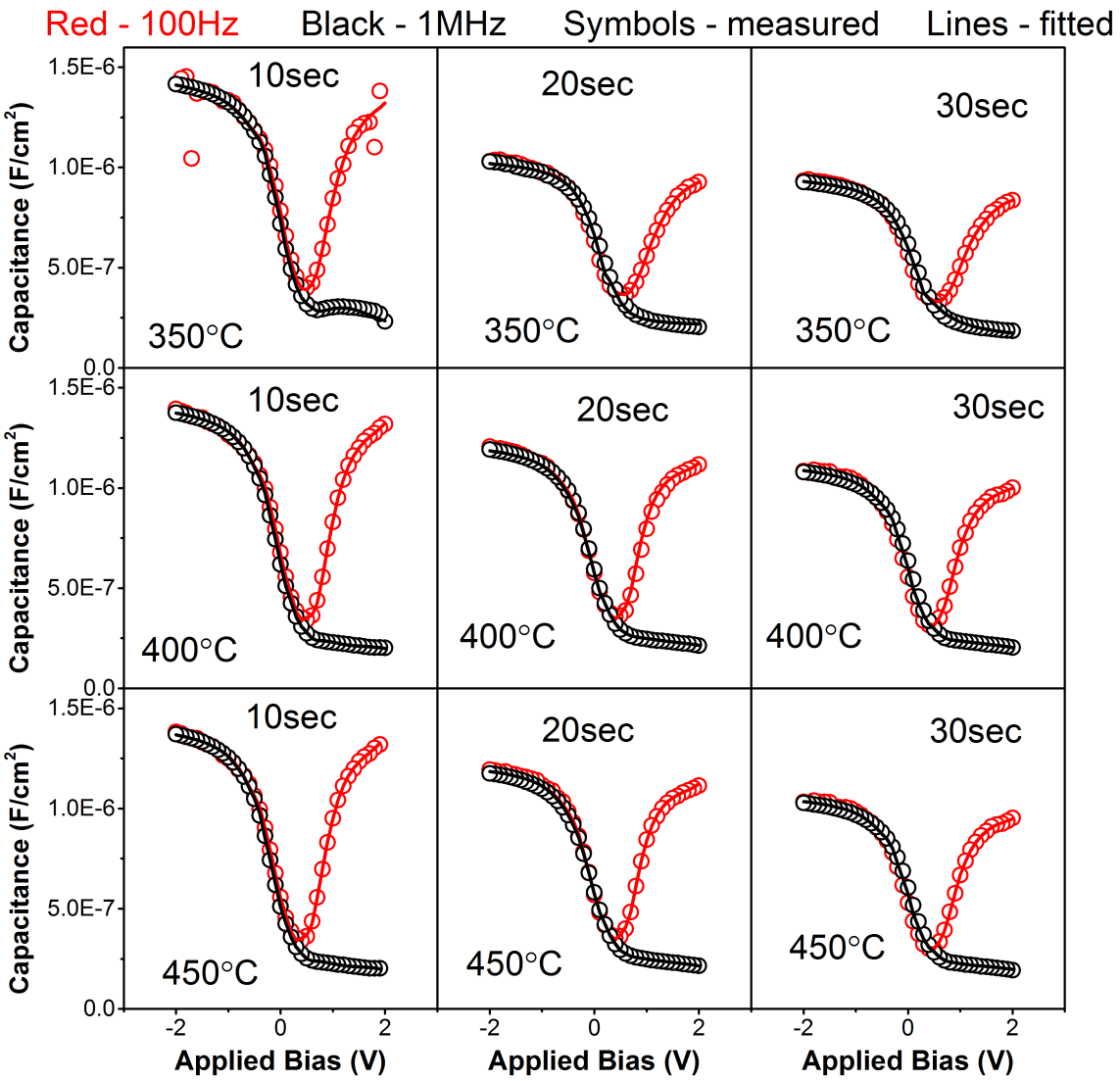


Figure 5.4. C-V profiles of the samples annealed in 10% O_2/N_2 at different temperatures using RTA

and fitted using the method described in chapter 3. The simulated C-V profiles fit the experimental data well. In both figures, a general trend of decreased maximum capacitance in accumulation is observed with increased plasma exposure time as expected.

5.3.2 Interface State Profile

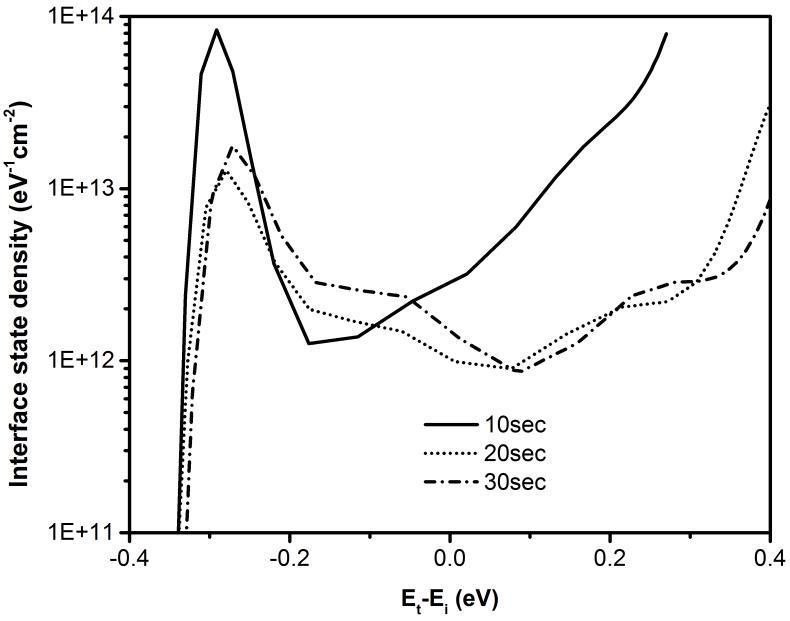
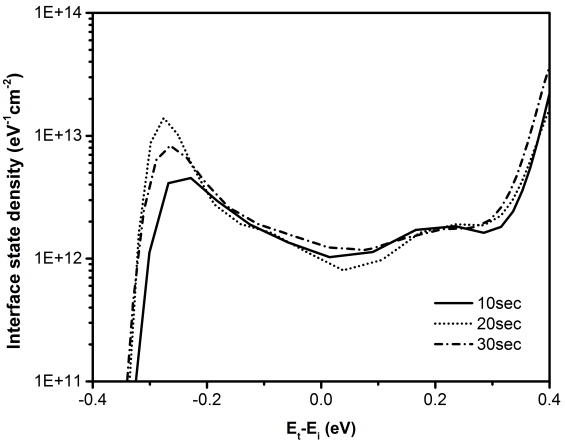


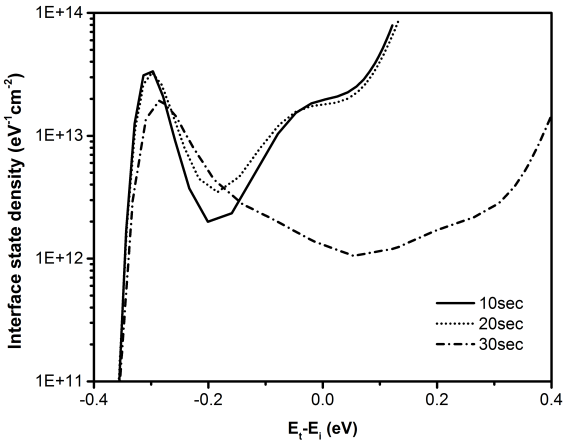
Figure 5.5. Interface state profiles of the samples not annealed using RTA

The extracted interface state density for the as deposited samples are shown in Fig. 5.5. It can be seen that the interface state density profile extracted for the as deposited samples are consistent with PPO data shown in chapter 4, with a peak interface state density near the valence band. As expected, Fig. 5.5 shows that the 10 sec plasma exposure results in a higher interface state density compared to the 20 sec and 30 sec PPO exposed samples, which are very similar in Dit profile. In the 20 sec and 30 sec samples, the interface state density is much lower, especially around midgap.

In Figs. 5.6, 5.7, and 5.8, the extracted interface state density profile from the fitted C-V measurements are shown for the samples that were annealed at 350°C and 450°C in

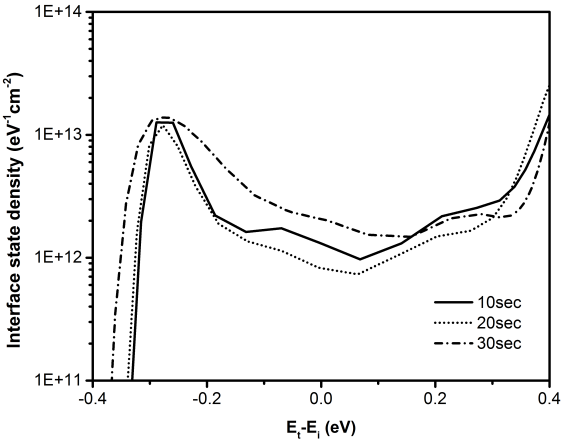


(a) Nitrogen anneal

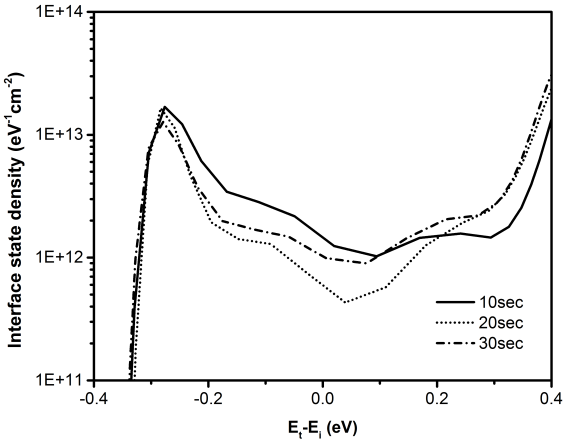


(b) 10% O_2/N_2 anneal

Figure 5.6. Interface state density profiles of the samples annealed in nitrogen and 10% O_2/N_2 at 350°C using RTA extracted from fitting procedure with ACE

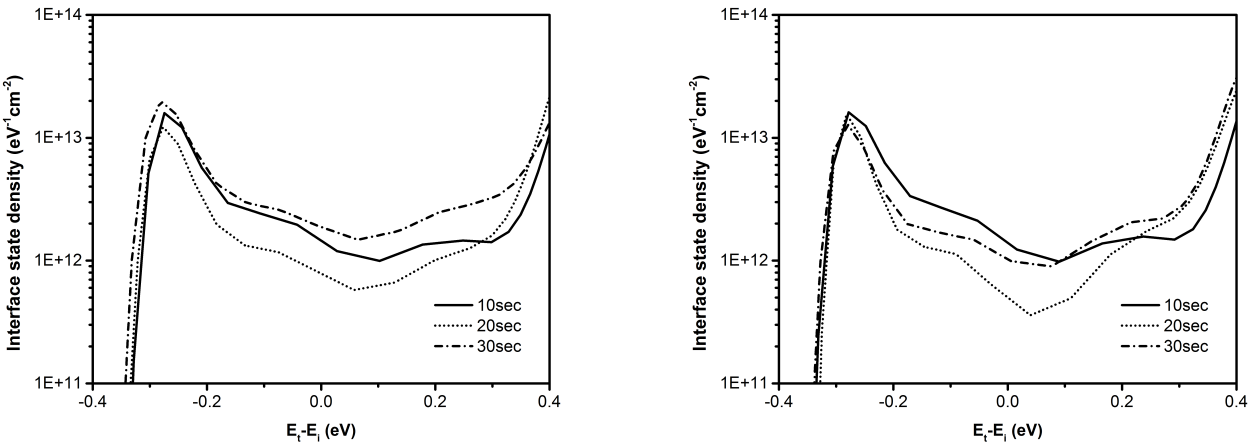


(a) Nitrogen anneal



(b) 10% O_2/N_2 anneal

Figure 5.7. Interface state density profiles of the samples annealed in nitrogen and 10% O_2/N_2 at 400°C using RTA extracted from fitting procedure with ACE



(a) Nitrogen anneal (b) 10% O_2/N_2 anneal

Figure 5.8. Interface state density profiles of the samples annealed in nitrogen and 10% O_2/N_2 at 450°C using RTA extracted from fitting procedure with ACE

the different environments. For the samples annealed in N_2, the extracted D_{it} appears very similar to the as deposited samples of indicating minimal effect of the post TiN anneal on the D_{it} in these samples. For the samples annealed in 10% O_2/N_2, while the samples show a high density of interface states near the valence band edge like the as deposited and N_2 annealed samples, the midgap D_{it} is reduced quite a bit following a 30 sec 10% O_2/N_2 exposure.

5.4 Effective Work Function Extraction

In Fig. 5.9 and Fig. 5.10, the flatband voltages vs. EOTs are extracted and plotted from the fitted C-V data for of all samples annealed in N_2 and 10% O_2/N_2. Firstly, and of critical importance, all the samples that have undergone post TiN RTA in either N_2 or 10% O_2/N_2 show an increased EOT indicating that this process degrades the electrical thickness of the Ge gate stack, contrary to Si devices. Germanium has a lower thermal budget compared to silicon, and these anneals are unacceptable to maintain low EOT. Even samples annealed in nominally only N_2 shows this EOT increase. Residual oxygen in the gas lines carrying the N_2 or in the RTA tool was also observed to oxidize samples even in Si devices, but here for Ge, the impact is much greater.

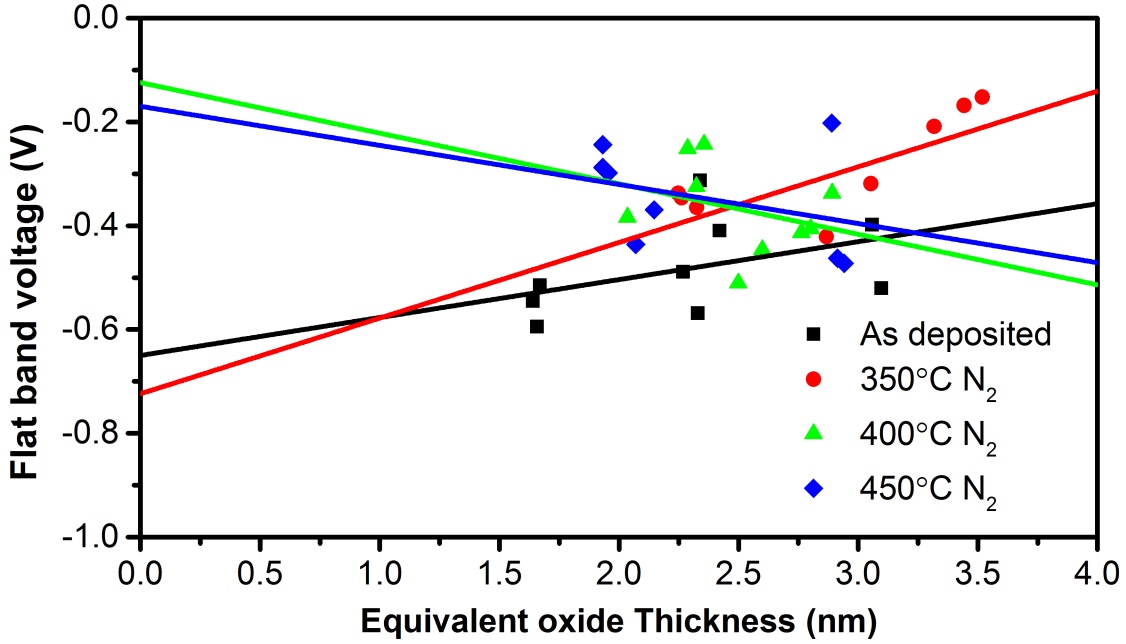


Figure 5.9. Flat band voltage vs. EOT plot showing the fixed charge density and shift in effective work function due to rapid thermal anneal in N_2 atmosphere at different temperatures

Despite the degradation in the electrical thickness, we can still observe some interesting trends in the V_{fb} vs. EOT plots shown in Figs. 5.9 and 5.10. Looking at the slopes of the linear fits to each annealing conditions data set allows us to make observations about the fixed charge induced by the annealing process. The as deposited, 350°C N_2 and 350°C 10% O_2/N_2 annealed samples seem to share a similar negative fixed charge density. In contrast, when the samples are annealed at 400°C and 450°C in either environment, we see the polarity of the fixed charge switch from negative to positive. These temperatures appear to significantly disturb the sensitive Ge/GeO_x/high-k gate stack obtained with the PPO process, causing a degradation in the electrical properties and possibly suggesting that the PPO process is not robust.

The observed increase in the effective work function following the 350°C 10% O_2/N_2 anneal is certainly consistent with the effects observed in Si EWF tuning. This hints that the same dipole related mechanism is occurring in Ge based gate stacks as well. Even the

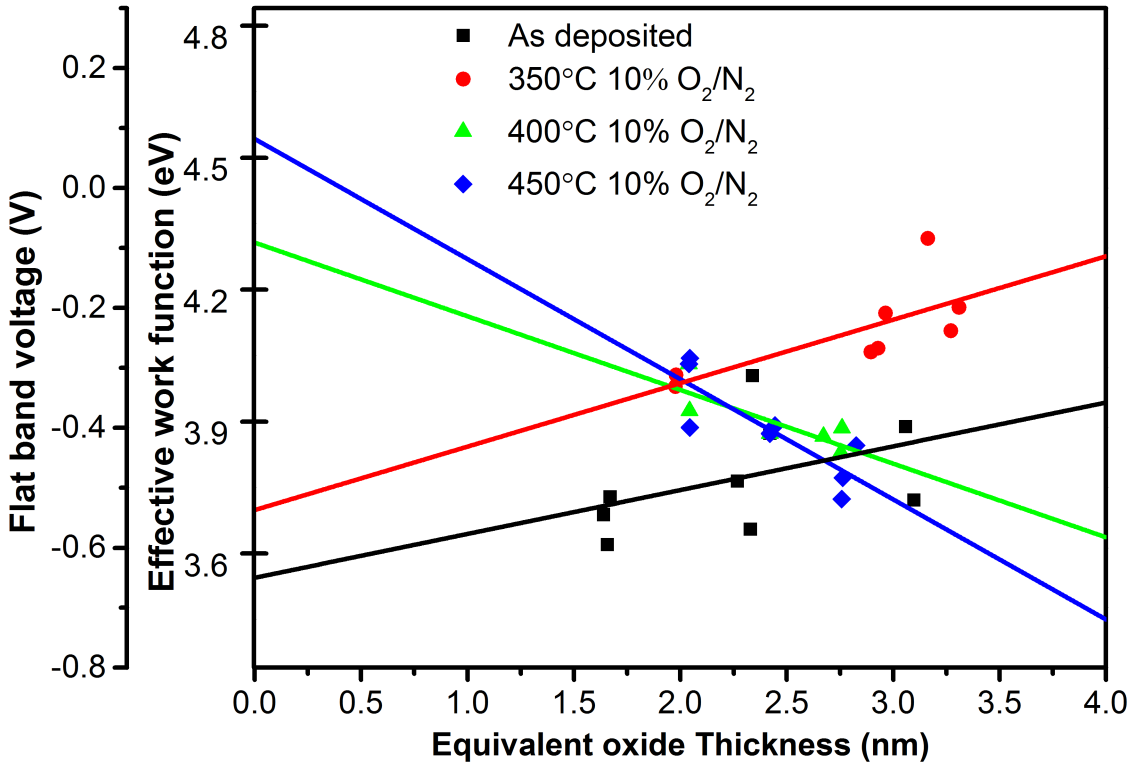


Figure 5.10. Flat band voltage vs. EOT plot showing the fixed charge density and shift in effective work function due to rapid thermal anneal in $10\%O_2/N_2$ atmosphere at different temperatures

higher temperature anneals do seem to move the EWF to higher values. However, the degradation of the electrical thickness and the change in fixed charge indicates that the process window is very narrow and at much lower temperatures than for Si. While these results are less promising than hoped for, they still demonstrate the usefulness of CV ACE to analyze alternative channel material/high-k based devices for process development and process induced degradation.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The primary objective of this dissertation was to enable tools to accelerate process flow development of MOS device fabrication for high-k on high mobility alternative channel materials. One of the primary bottlenecks in the semiconductor industry is the lack of available software for the rapid analysis of the electrical characterization of devices based on these high mobility alternative channel materials. In highly scaled devices, the electric field at the interface is sufficiently large to show significant quantum mechanical effects in the measured C-V profiles. Additionally, the non-parabolicity of the conduction band in III-V materials and the availability of a wide range of high-k dielectrics increases the complexity of their C-V analysis.

To address this issue, we developed a model which takes into account quantum corrections which can be applied to a number of these alternative channel materials including Si_xGe_{1-x}, Ge, InGaAs, and GaAs. The C-V simulation using this QM correction model is orders of magnitude faster compared to a full band Schrodinger-Poisson solver. The simulated C-V is directly benchmarked to a self consistent Schrodinger-Poisson solution for each bulk semiconductor material and from the benchmarking process the QM correction parameters are extracted.

In high mobility materials, the interface state density can significantly impact the C-V profile. This in turn affects the parameters extracted from the C-V data of the high mobility semiconductor/high-k interface, which are crucial to fully understand the interface properties and expedite process development. Additionally, III-V materials show an anomalous

frequency dispersion in the accumulation region, which originates from the disordered III-V semiconductor interface and can be accurately modeled using a carrier tunneling model. The QM correction model, along with the interface state density model, are implemented into our software program, C-V Alternative Channel Extraction (CV ACE), which can extract device parameters such as EOT, doping and V_{fb} density as well as the interface state density profile using multiple measurements performed at different frequencies and temperatures, simultaneously. The program was used to analyze experimentally measured C-V profiles and the extracted device parameters show excellent agreement with the known device structure and previously published results.

CV ACE has been applied in the development of a process flow for germanium interface passivation in Ge based MOS devices using a GeO_x interlayer. A post ALD plasma oxidation (PPO) process was developed using RF plasma in a PECVD chamber and demonstrated significant surface passivation. Various gases were investigated and while 25% O_2/Ar was found to passivate the surface the growth rate of the GeO_x interlayer was too high. Reducing the oxygen content to 1% O_2/Ar was found to reduce the growth rate and provide excellent control over the degradation of EOT.

The plasma power used in the 1% O_2/Ar PPO process has a significant impact on the interface state density. A 200 W plasma, shows more valence band edge interface state response, while a 50 W plasma seems to be inadequate for germanium surface passivation. A 100 W plasma with 1% O_2/Ar was found to provide the best combination of EOT and low D_{it} and is concluded to be the optimum process for PPO of germanium surfaces.

CV ACE and PPO were then utilized to investigate other process development challenges. A study of the impact of low temperature anneals on Ge-based MOS devices was found to result in a degradation of the electrical thickness and a change in fixed charge, indicating that the process window is very narrow and at much lower temperatures than for Si.

6.2 Future Work

The quantum correction model described in this work is highly flexible. The model can be used to simulate and analyze unconventional materials based interfaces. For example, CV ACE has been successfully demonstrated to analyze wide band gap materials, including ZnO based thin film transistors (TFT). In addition to ZnO based devices, the model is also being used for crystalline oxides on InGaAs based MOS device analysis. For widespread use of CV ACE, several additional features should be added:

1. Batch processing of a large number of C-V data sets would allow the semiconductor industry to generate interface state density profiles mapped to the wafer and pin point process development issues.

2. Modification of the model to include novel materials like transition metal dichalcogenide (TMDs) and topological insulators. These materials have different band structures and interesting material properties. TMDs are being considered for the next generation of ultra low power devices. Bulk TMDs have an indirect band-gap. However, in monolayer form, the band-gap becomes direct and is located at the K-point. By applying this model to these advanced materials, the research can be progressed at an accelerated pace.

3. Implement this model to 2-D and 3-D analysis for advanced device structures. 3-D devices such as FinFETs, have shown excellent control over the channel due the gate's effect on the channel from three directions. By modifying the SP solution and quantum correction model in CV ACE for use in 2-D and 3-D, this code can be applied to future technology architectures.

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