HIGH-SPEED AND LOW-POWER PIPELINED SAR ADCS

WITH PASSIVE RESIDUE TRANSFER AND DYNAMIC AMPLIFIER

by

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Hai Huang, PhD
The University of Texas at Dallas, 2017

Supervising Professor: Yun Chiu, PhD

High speed analog to digital converters (ADCs) are critical blocks in wideband wireline and wireless communication systems. This dissertation presents the designs of two high-speed pipelined successive-approximation-register (SAR) ADCs with the passive residue transfer technique and the process, voltage and temperature (PVT) stabilized dynamic amplifier. The passive residue transfer technique can effectively and efficiently replace the bandwidth-limiting residue amplifier in the medium-resolution pipelined SAR ADC. As a result, the time and power consumption associated with the residue amplification are mostly removed and the ADC can obtain considerable speed improvement. Although dynamic amplifiers are employed in recent published pipelined SAR ADCs to achieve fast residue amplifications, the gain instability still limits the ADC's conversion accuracy when the supply voltage and ambient temperature varies. A PVT-stabilized dynamic amplifier based on the replica technique is reported to mitigate the gain variation over process, voltage and temperature changes.

The first design is an 8 bit 1.2 GS/s pipelined SAR ADC with the passive residue transfer. It also utilizes the 2b-1b/cycle hybrid conversion scheme with an appropriate resolution partition to

further enhance the conversion speed. The prototype ADC measured a signal-to-noise plus distortion ratio (SNDR) of 43.7 dB and a spurious-free dynamic range (SFDR) of 58.1 dB for a Nyquist input. The ADC consumes the total power dissipation of 5.0 mW and achieves a Walden FoM of 35 fJ/conversion-step at a sample rate of 1.2 GS/s. Although it is fabricated with a 65 nm process, the prototype ADC still achieves the same conversion speed as prior research works fabricated in a 32 nm process.

The PVT-stabilized dynamic amplification technique is experimentally validated by the second ADC which is a 12 bit 330 MS/s pipelined SAR ADC also in 65 nm CMOS. The maximum measured gain variations are 1.5% and 1.2% for the supply voltage varying from 1.25 V to 1.35 V and the temperature varying from −5 ℃ to 85 ℃, respectively; the corresponding SNDR variations of the ADC are <1 dB. This prototype ADC measures an SNDR of 63.5 dB and a Walden FoM of 15.4 fJ/conv.-step for a near-Nyquist input. The conversion speed of this prototype ADC is 65% faster than the pipelined SAR ADCs with a similar SNDR published recently.

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# CHAPTER 1

# INTRODUCTION[1]

## 1.1 MOTIVATION

Communication systems such as ultra-wideband radios, serial link and broadband Ethernet transceivers demand high-speed analog-to-digital converters (ADCs) with low power consumption. The successive-approximation-register (SAR) conversion architecture is an attractive option for these applications due to its low analog complexity and excellent power efficiency. However, compared to the flash and pipeline architectures, the serial conversion process of the SAR ADC still dramatically limits its conversion speed. In recent years, a few speed-acceleration techniques for non-interleaved, single-channel SAR ADC have been reported [1]-[7], which will be briefly reviewed below.

First, an asynchronous clocking scheme was used in [1] and [2] to reduce the SAR loop delay. In the conventional synchronous design, the time allocated to all bit cycles is the same and decided by the slowest cycle, resulting in some idle time in the faster bit cycles. In contrast, for asynchronous clocking, the time for each SAR cycle is independently assigned based on the comparator's decision delay in this cycle, therefore eliminating the wasted time and increasing the overall conversion speed.

Second, resolving multiple bits in each SAR cycle is a popular way of increasing the ADC throughput [3], [4]. Ideally, the conversion speed (excluding the input sampling time) of a multi-

[1] ©2017 IEEE. Portions Adapted, with permission, from H. Huang, L. Du, and Y. Chiu, "A 1.2-GS/s 8-bit Two-Step SAR ADC in 65-nm CMOS with Passive Residue Transfer," *IEEE J. Solid-State Circuits*, 2017

bit SAR ADC can be improved by a factor which is the number of bits converted in each cycle. One drawback of this structure is that its resolution is restricted by the comparator offset—just like the flash ADC, it is necessary to limit the comparator offset to less than half an LSB in each conversion cycle to avoid any gross conversion errors. In addition, a multi-bit SAR ADC also requires two digital-to-analog converters (DACs), i.e., a signal DAC (SIG-DAC) and a reference DAC (REF-DAC). The former is used to perform the sampling and successive approximations of the signal, whereas the latter is to supply multiple threshold voltages for all the comparators involved during the SAR cycles. Naturally, this setup invites a mismatch problem between the SIG-DAC and the REF-DAC [4].

Third, the two-step pipeline SAR is another structural extension to the conventional SAR ADC for breaking the speed limit [5], [6]. Its overall quantization is partitioned into two steps and an accurate amplifier is needed to transfer the conversion residue from the first stage to the second. Typically, the conversion throughput and power consumption of the two-step approach are limited in part by the achievable bandwidth and power efficiency of the residue amplifier, respectively. This is particularly true for ultra-high-speed scenarios, wherein the parasitic capacitance of the amplifier is comparable to its capacitive loading so burning more power to increase the bandwidth becomes ineffective.

In this dissertation, the passive residue transfer technique and the process, voltage and temperature (PVT) stabilized dynamic amplifier are presented in an attempt to push the conversion speed limit of pipelined SAR architecture. Benefiting from the passive residue transfer, the residue amplifier in medium-resolution pipelined SAR ADC is removed and a faster residue transfer that also consumes less power is obtained. Additionally, targeting high resolution

ADCs, the PVT-stabilized dynamic amplification with a fast settling speed is developed to further improve the conversion throughput without sacrificing the accuracy. Moreover, two prototype ADCs with passive residue transfer and dynamic amplifier were designed and implemented in a 65 nm CMOS process to prove the effectiveness of these techniques.

## 1.2 ORGANIZATION

This dissertation is organized as follows. First, the operation principles and analysis of the passive residue transfer are provided in Chapter 2. Second, the circuit implementation of the prototype ADC design with passive residue transfer is described in Chapter 3. Chapter 4 presents the working principles of PVT-stabilized dynamic amplifier and the prototype ADC design. Lastly, Chapter 5 summarizes and concludes my work during Ph.D. period.

# CHAPTER 2

# PASSIVE RESIDUE TRANSFER[2]

In general, there are two approaches to transfer the residue voltage passively. One is termed the *attenuated* passive residue transfer while the other one is the *non-attenuated* passive residue transfer. In this chapter, the operation principles, advantages and disadvantages of the two approaches will be introduced.

## 2.1 ATTENUATED PASSIVE RESIDUE TRANSFER

The working principle of the attenuated passive residue transfer is illustrated in Figure 2.1. First, the sampling switch $S_1$ turns on and the first-stage DAC samples the input signal. Then, the first stage performs the coarse conversion. Once the conversion is done, the residue voltage will be generated by the first-stage DAC while the second-stage DAC is reset. After that, the transfer switch $S_2$ turns on and the second-stage DAC is utilized to share the charge stored on the first-stage DAC. Lastly, when the switch $S_2$ turns off, the second stage starts the fine conversion.

A critical problem associated with this approach is the residue signal attenuation stemming from the charge sharing between the two DACs. Obviously, the signal attenuation brings about a stringent constraint on the noise of the second-stage comparator, thereby dictating more power consumption. The signal attenuation also reduces the input voltage of the second-stage comparator and increases the decision time inevitably. Furthermore, this method needs an

[2] ©2017 IEEE. Portions Adapted, with permission, from H. Huang, L. Du, and Y. Chiu, "A 1.2-GS/s 8-bit Two-Step SAR ADC in 65-nm CMOS with Passive Residue Transfer," *IEEE J. Solid-State Circuits*, 2017

explicit clock phase for resetting the DAC, potentially reducing the timing budget of the second stage (see Figure 2.1).

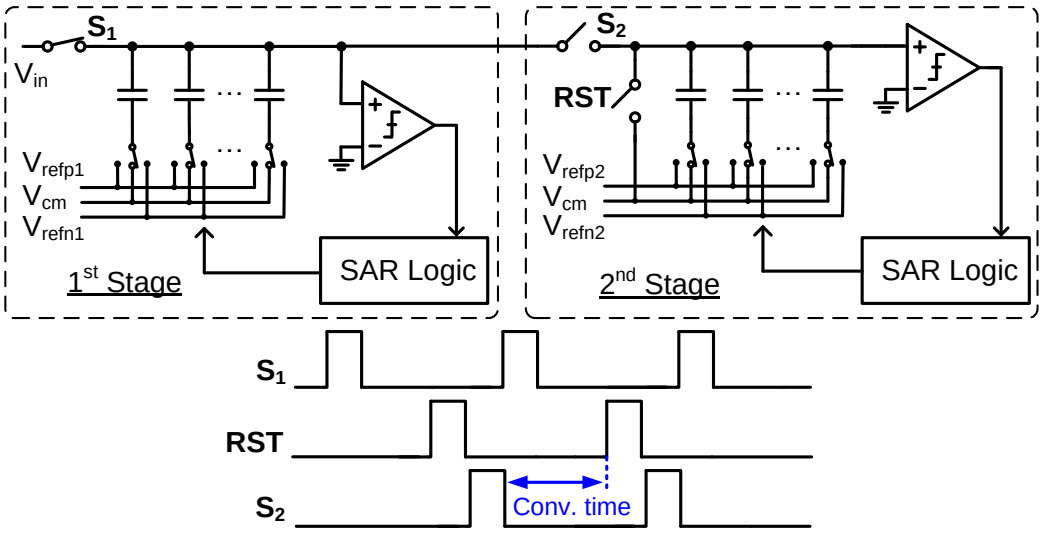



Figure 2.1. Schematic and timing diagram of attenuated passive residue transfer

## 2.2 NON-ATTENUATED PASSIVE RESIDUE TRANSFER

### 2.2.1 OPERATION PRINCIPLE

The non-attenuated passive residue transfer, as shown in Figure 2.2, is to employ two DACs in a ping-pong configuration to alternately transfer the residue voltage from the first stage to the second [9], [10]. To begin with, both the sampling switch $S_1$ and transfer switch $S_{2a}$ or $S_{2b}$ turn on and the input signal is sampled by the DACs of both stages. Then the sampling switch $S_1$ turns off and the first stage performs the coarse conversion as well as the generation of the residue voltage. Note that, in this period, the second stage A or B is idle and its DAC just appears as a "parasitic capacitor" to the first-stage DAC. Once the residue generation completes, the transfer switch $S_{2a}$ or $S_{2b}$ turns off and the residue is acquired by the second stage immediately.

Finally, the second stage A or B is activated for the fine conversion. This process is repeated with alternate participation of different second stages A and B.

Because the DAC in the second stage doesn't need to be reset explicitly before transferring the residue, the second stage can utilize the whole period to quantize the residue voltage (see Figure 2.2) and its timing burden can be effectively alleviated. Since the residue signal is not attenuated, this technique not only accelerates the decision of the second-stage comparator but also provides some SNR benefit relative to the attenuated passive residue transfer. For power consumption, considering that the ping-pong stages work alternately (i.e., one works while the other is mostly idle), the total power of its comparators and SAR logic are similar to that of the conventional structure without ping pong. For a two-step ADC, the noise of the first-stage comparator impacts the residue voltage and the first-stage digital output equally but with opposite polarity, resulting in a noise cancellation in the overall digital output of the ADC [11]. As the noise of the first-stage comparator doesn't contribute to the overall noise budget of the ADC, it can be reasonably downsized to save power. In summary, this approach does not suffer too much power penalty in comparison to the one-step conventional SAR structure.

A drawback of this technique is the area overhead due to the ping-pong second stages [9],[10]. In addition, when the first stage is quantizing the sampled input, the second-stage DAC just appears as a "parasitic capacitor" to the first stage. Naturally, the reference level of the first stage is attenuated by the second-stage DAC during the bit cycles. Fortunately, for high-speed ADCs, the input signal swing is normally restricted by the linearity of the S/H instead of the reference swing [3], [7], so the reference attenuation problem has a minor effect on the overall ADC accuracy. However, for high-resolution ADC, the reference attenuation problem may limit

the ADC's input swing and finally reduce the input swing of the second-stage comparator. This means the second-stage comparator in this structure need to consume more power than that in conventional SAR ADC to achieve the same noise performance. Note that the input parasitic capacitors of the comparators attenuate the reference levels of the first and the second stages by different factors, which equivalently modify the exact value of the inter-stage gain and dictate a gain calibration.

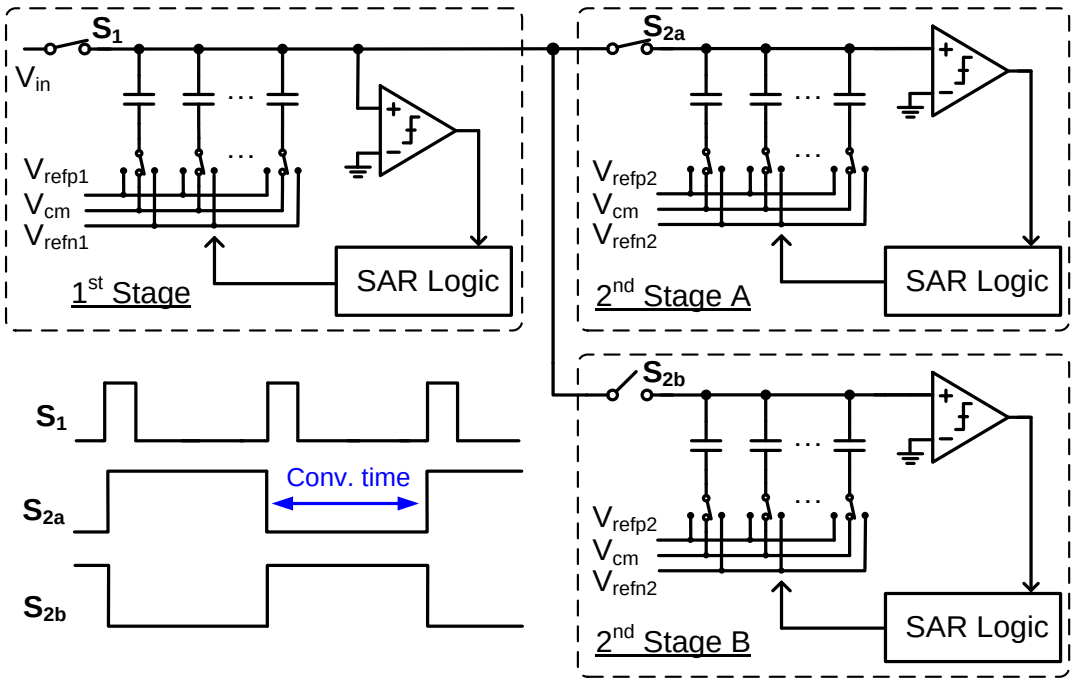



Figure 2.2. Schematic and timing diagram of non-attenuated passive residue transfer

Due to its speed and SNR benefits, this approach is utilized in the prototype ADC for transferring the residue voltage passively. As a consequence of the non-attenuated passive residue transfer, no bandwidth-limiting amplifier is employed in the design and a fast, as well as power efficient, residue transfer is attained.

### 2.2.2 KT/C NOISE ANALYSIS

For the non-attenuated passive residue transfer, two sampling operations are involved in one conversion cycle. Its kT/C noise is supposedly different from that of the conventional sampling scheme and needs to be investigated [9]. The analysis can be approached by the circuit model shown in Figure 2.3, where $C_1$ and $C_2$ are the total DAC capacitances of the first and second stages, respectively. For a two-step ADC, only the output noise stored on $C_2$ contributes to the overall noise budget. The output noise on $C_2$ consists of the noise due to the sampling switch $S_1$ ($V_{o1}$) and that induced by the transfer switch $S_2$ ($V_{o2}$). To simplify the analysis, these two parts of output noise are studied separately. In Figure 2.3(a), when the sampling switch $S_1$ turns off, the output noise power can be derived as

$$\overline{V_{o1}^{\,2}} = \frac{kT}{C_1 + C_2}. \tag{2-1}$$

In Figure 2.3(b), the noise power equals to

$$\overline{V_{n2}^{\,2}} = \frac{kT(C_1 + C_2)}{C_1 C_2}, \tag{2-2}$$

so the output noise power $V_{o2}^{\,2}$ coming from the transfer switch $S_2$ is expressed as

$$\overline{V_{o2}^{\,2}} = \left(\frac{C_1}{C_1 + C_2}\right)^2 \overline{V_{n2}^{\,2}} = \frac{kTC_1}{(C_1 + C_2)C_2}. \tag{2-3}$$

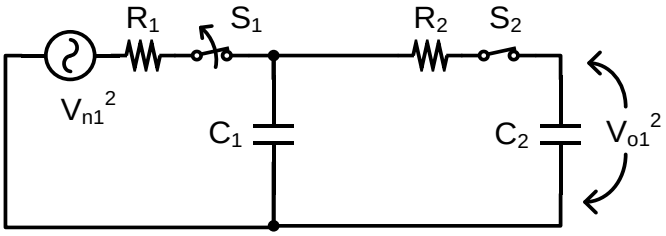
The total output noise power on $C_2$ is the summation of the noise power in (2-1) and (2-3) and can be simplified to

$$\overline{V_{on}^{\,2}} = \overline{V_{o1}^{\,2}} + \overline{V_{o2}^{\,2}} = \frac{kT}{C_2}. \tag{2-4}$$

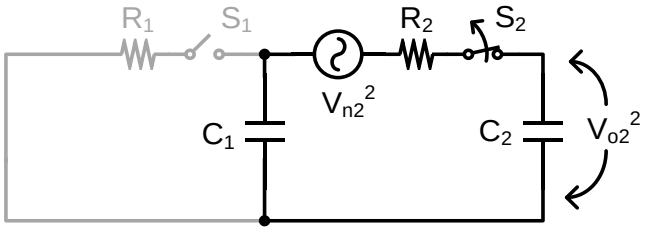
Interestingly, (2-4) indicates that the total noise power is unrelated to the capacitance $C_1$ and only decided by $C_2$! This simple result can also be explained using the so-called equipartition theorem from statistical mechanics [12], [13]. According to the equipartition theorem, any energy storage element (capacitors in Figure 2.3) in thermal equilibrium keeps an average noise energy with a value of kT/2. As a result, for the circuit in Figure 2.3, we can easily obtain

$$\overline{\frac{1}{2}C_2 V_{on}^{\,2}} = \frac{kT}{2}, \tag{2-5}$$

$$\overline{V_{on}^{\,2}} = \frac{kT}{C_2}. \tag{2-6}$$




(a)




(b)

Figure 2.3. The circuit model for the kT/C noise analysis of passive residue transfer: (a) the sampling and (b) the residue transfer

It can be seen clearly from Figure 2.4 that the aforementioned noise analysis matches the PNOISE simulation results of the circuit in Figure 2.3 accurately. Guided by (2-4), $C_2$ in the prototype ADC is chosen to be 15.5 fF and the corresponding kT/C noise power is roughly equal to half of the quantization noise power.

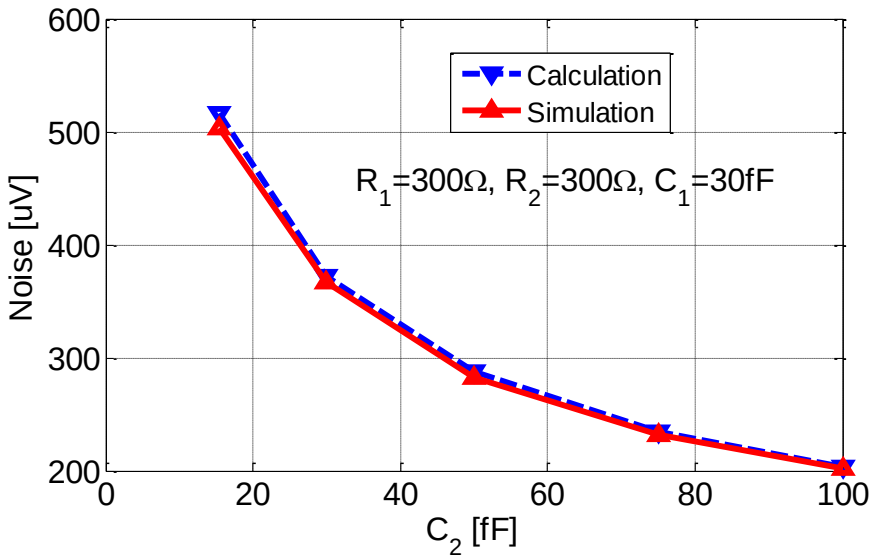



Figure 2.4. Simulated kT/C noise and the calculated kT/C noise

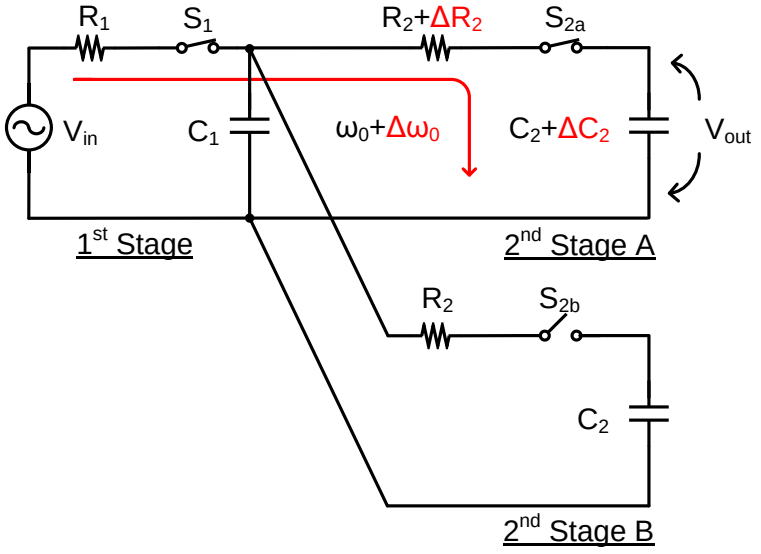



Figure 2.5. Bandwidth mismatch of the sampling network with non-attenuated passive residue transfer

The transfer function of the sampling network in Figure 2.5 can be derived as

$$H(s) = \frac{1 + sR_2C_{SER}}{(\frac{s}{\omega_n})^2 + \frac{s}{\omega_0} + 1}, \tag{2-7}$$

where $\omega_n$ and $\omega_0$ are

$$\omega_n = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \tag{2-8}$$

$$\omega_0 = \frac{1}{R_1C_1 + (R_1 + R_2)C_2}, \tag{2-9}$$

and $C_{SER}$ is the capacitance in series,

$$C_{SER} = \frac{C_1C_2}{C_1 + C_2}. \tag{2-10}$$

The phase shift of the sampling network can be calculated and simplified to (for $\omega << \omega_0$, it can be observed that $\omega$ is also much smaller than $\omega_n$),

$$\begin{aligned} \varphi(\omega) &= \arctan \omega R_2C_{SER} - \arctan \frac{\omega / \omega_0}{1 - (\omega / \omega_n)^2} \\ &\approx \arctan \omega R_2C_{SER} - \arctan \frac{\omega}{\omega_0}. \end{aligned} \tag{2-11}$$

The relative phase shift stemming from the on-resistance mismatch ($\Delta R_2$) between the two transfer switches is

$$\begin{aligned} \Delta\varphi(\omega) &\approx \left[ \frac{\omega C_{SER}}{1 + \omega^2 {R_2}^2 {C_{SER}}^2} - \frac{\omega C_2}{1 + (\omega / \omega_0)^2} \right] \Delta R_2 \\ &\approx (\frac{\omega C_{SER}}{1 + \omega^2 {R_2}^2 {C_{SER}}^2} - \omega C_2) \Delta R_2. \end{aligned} \tag{2-12}$$

So the corresponding timing mismatch can be expressed as

$$\Delta t(\omega) \approx (\frac{C_{SER}}{1+\omega^2 R_2{}^2 C_{SER}{}^2} - C_2)\Delta R_2$$
$$\approx -C_2(1-\frac{1}{(1+\frac{C_2}{C_1})\left[1+\omega^2 R_2{}^2(\frac{C_1 C_2}{C_1+C_2})^2\right]})\Delta R_2. \quad (2\text{-}13)$$

For a sinusoidal input signal the signal-to-distortion ratio (SDR) due to the timing mismatch can be expressed as [14]

$$SDR = -20\log \omega\Delta t(\omega)$$
$$\approx -20\log\left[\omega(\frac{R_2 C_{SER}}{1+\omega^2 R_2{}^2 C_{SER}{}^2} - R_2 C_2)\frac{\Delta R_2}{R_2}\right] \quad (2\text{-}14)$$

In order to verify the aforementioned analysis, the SDRs calculated from (2-14) and acquired from circuit simulations are plotted in Figure 2.6 for contrast.

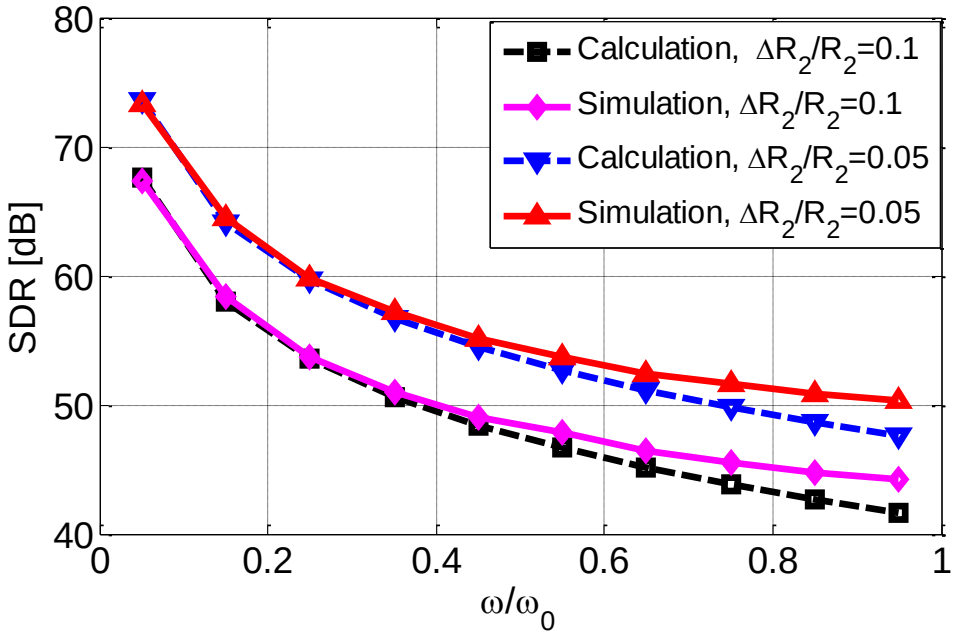



Figure 2.6. Simulated SDR and the SDR calculated from equation (2-14)

It can be seen that the model matches the circuit simulation results with less than 1dB deviation as $\omega/\omega_0$ approaches 0.5. In (2-13), it's interesting to note that the timing mismatch $\Delta t(\omega)$ is reduced with a decreasing value of $C_2$ or $R_2$. An intuitive way to understand this is that for a small $C_2$ or $R_2$ the common first stage ($R_1$ and $C_1$) effectively constitutes a relatively large portion of the time constant of the sampling network (see equation (2-9)), resulting in a small bandwidth sensitivity on the on-resistance mismatch. As we discussed in the last subsection, $C_2$ determinates the kT/C noise and it cannot be too small. In the prototype design, the transfer switches are bootstrapped for a small on-resistance, which guarantees a sufficient SDR for an 8 bit ADC according to equation (2-14).

# CHAPTER 3

# PIPELINED SAR ADC WITH PASSIVE RESIDUE TRANSFER[3]

## 3.1 2B-1B/CYCLE CONVERSION SCHEME

The architecture of the prototype ADC with non-attenuated passive residue transfer is illustrated in Figure 3.1. To further enhance the conversion speed, a 2b/cycle conversion scheme is utilized in the first stage. In the prototype design, comparator offsets are calibrated in a foreground manner to remove their impact on the overall conversion accuracy. The 2b/cycle scheme requires two DACs, i.e., a signal DAC and a reference DAC, to implement the 2 bit quantization per cycle. Without doubt, this setup introduces a potential mismatch issue between the two DACs. In Figure 3.1, the SIG-DAC is loaded with four comparators whereas the REF-DAC is only connected to two comparators. The input parasitic capacitance of the comparators causes a systematic gain mismatch between the SIG-DAC and the REF-DAC. Hence, two dummy comparators (not shown in Figure 3.1) are connected to the output node of the REF-DAC to avoid the systematic mismatch. The random mismatch between the capacitors in SIG-DAC and REF-DAC is normally bounded by 1% (causing a 0.16-LSB error on the residue) [18]. Therefore, the inter-stage redundancy with a value of ±4 LSBs can tolerate this error induced by any small random mismatch between the two DACs.

From the speed standpoint, making both the first and second stages 2b/cycle will probably deliver the highest conversion speed. However, due to the lack of residue amplification, the LSB

[3] ©2017 IEEE. Portions Adapted, with permission, from H. Huang, L. Du, and Y. Chiu, "A 1.2-GS/s 8-bit Two-Step SAR ADC in 65-nm CMOS with Passive Residue Transfer," *IEEE J. Solid-State Circuits*, 2017

size of the second stage is much smaller than that of the first stage. The comparator offsets and the mismatch between the SIG-DAC and the REF-DAC will make it difficult for the second stage to achieve the desired resolution. As an alternative, a 1b/cycle conversion scheme is applied to the second stage in this work, in which the single comparator offset does not bring about any DNL errors but merely an input-referred offset.

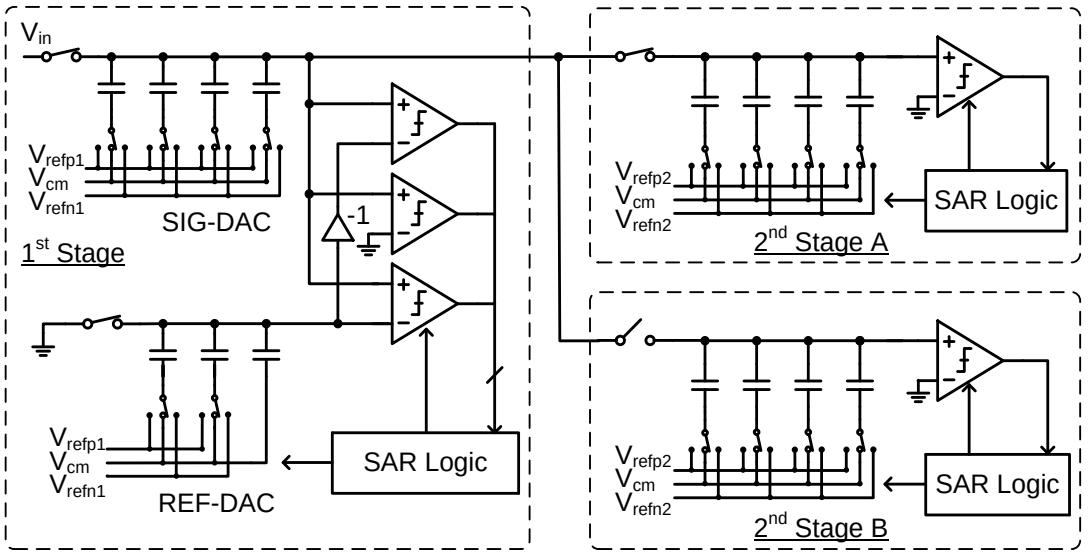



Figure 3.1. Architecture of the 2b-1b/cycle two-step SAR ADC with passive residue transfer(a single-ended version is shown for simplicity)

Besides the conversion scheme, the resolution partition between the 2b/cycle first stage and 1b/cycle second stage also affects the overall throughput significantly. Considering that a 1b redundancy is needed to absorb the decision error in the first stage and the kickback noise of the second-stage comparator, there are two options for this partition: 1) 3×2b for the first stage and 3×1b for the second; 2) 2×2b for the first and 5×1b for the second. While option 1) appears to be more balanced (i.e., resolving 3 cycles for each stage), the 2b/cycle operation consumes more time than the 1b/cycle counterpart because of the increased logic complexity; and besides some

additional time needs to be allocated to the first stage for sampling. Thus, the first stage becomes the speed bottleneck and some conversion time of the second stage is wasted, as Figure 3.2 illustrates. Circuit simulation reveals that the maximum throughput for this option is limited to 1 GS/s.

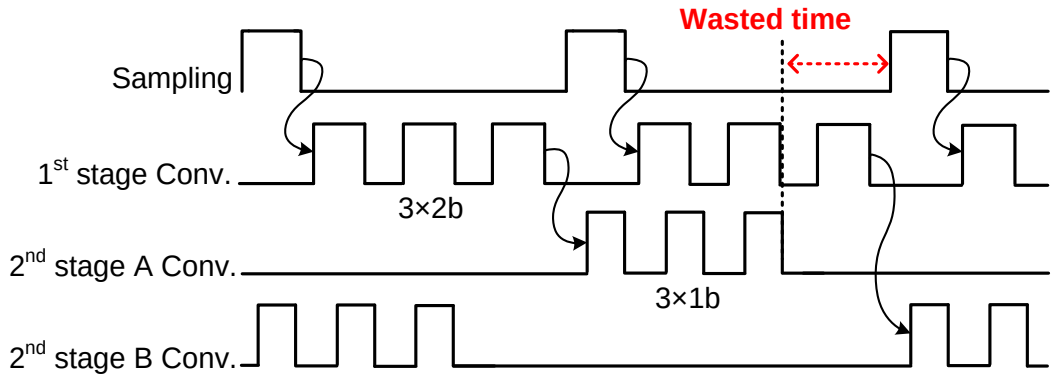



Figure 3.2. Timing diagram of the first resolution partition: 3×2b for the first stage and 3×1b for the second stage

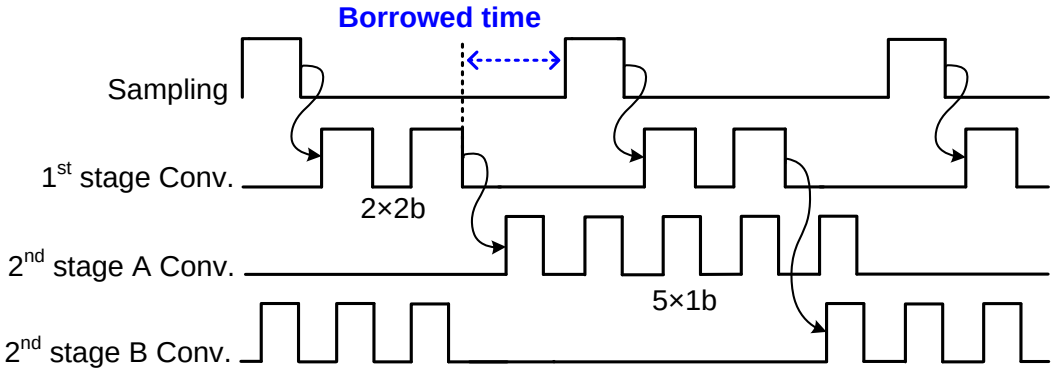



Figure 3.3. Timing diagram of the second resolution partition: 2×2b for the first stage and 5×1b for the second stage

The prototype ADC is realized with option 2), in which the first stage resolves 4bits and the remaining 5bits are assigned to the second stage. The second stage becomes the speed bottleneck in this scenario. Fortunately, the asynchronous time allocation enables time borrowing and

somewhat relieves the timing burden of the second stage. This is depicted in Figure 3.3, wherein once the last cycle of the first stage completes, the residue transfer is triggered and the second stage starts conversion immediately after that. Typically, the two conversion cycles of the first stage complete before the next sampling edge arrives, thus the rest of the time can be lent to the second stage. Unlike the first option, there is no conversion time wasted in this case. According to simulation, the ADC can be clocked maximally at 1.3 GS/s, which is significantly improved relative to the first option.

## 3.2 CAPACITIVE DACS

The schematic of the capacitive DACs is depicted in Figure 3.4. As mentioned in section 2, the total capacitance of the second-stage DAC is chosen to be 15.5 fF for the sake of kT/C noise. Because of this small capacitance, the DAC becomes vulnerable to the kickback noise of the second-stage comparator. The kickback noise is injected into the DAC output only when the comparator is activated and the impact disappears once the comparator is reset, implying that the effect is memory-less (i.e., confined to the current bit cycle only) and can be considered as a form of DAC incomplete settling error. Therefore, the second-stage DAC employs a non-binary structure with an LSB capacitor of 1.5C to tolerate the kickback noise [15], [16] (maximally tolerating ±1.5 mV differential kickback noise). Owing to the absence of residue gain, the quantization range of the second stage needs to be scaled down to roughly align with the residue voltage range. A large scaling capacitor could be added in the second-stage DAC to downscale the reference voltage [6], which unfortunately enlarges the input capacitive loading dramatically. In this design, a second reference $V_{ref2}$ is applied to the second stage, obviating the large input loading issue. The calibrated reference $V_{ref2}$ is chosen to be about $1/18 V_{ref1}$, which introduces a

redundancy of about ±4 LSBs (±15 mV) to tolerate the error resulting from any random mismatch between the SIG-DAC and the REF-DAC and any potential DAC settling errors during the coarse cycles.

Since the reference level of the first-stage SIG-DAC is attenuated by the second-stage DAC, it is desirable to choose a large ratio for the DAC sizes between the first and second stages. On the flip side, however, considering the input loading and the performance of the S/H, the capacitance of the first-stage DAC should not be too large. In this work, this capacitance is chosen to be twice as large as the second-stage DAC, resulting in a reference attenuation factor of 2/3. To obtain a nominally identical attenuation factor as that of the SIG-DAC, a scaling capacitor of 17.5C is added to the REF-DAC.

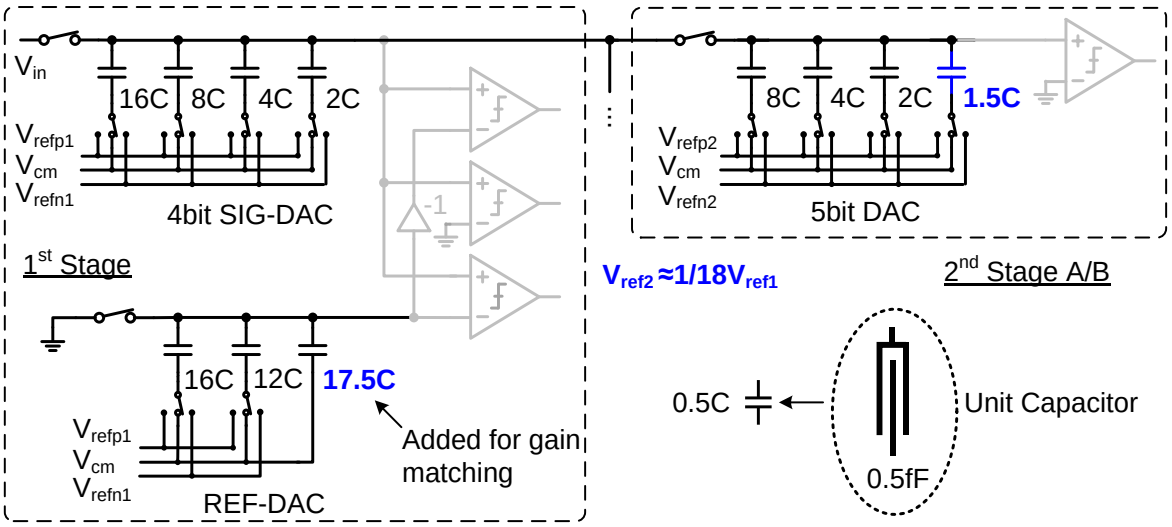



Figure 3.4. Schematic of capacitive DACs in the prototype ADC

The unit capacitors in the DACs are realized with fringing metal capacitors of 0.5 fF [17]. The LSB capacitor has a capacitance of 1.5 fF and it is supposed to achieve good matching for an 8 bit ADC [18]. In the prototype, we also exploited the fact that the DACs of the two stages

are independent to minimize the capacitance spread, which is 8 (16C/2C) instead of 64 given an overall 8 bit resolution [7]. This small capacitance spread not only leads to a small input capacitive loading of 45.5 fF, but also reduces the overall area of the DACs significantly.

### 3.3 TRANSFER SWITCH

As analyzed earlier, the smaller the on-resistance of the transfer switch, the better the bandwidth matching becomes. Moreover, because the second-stage DAC participates in the coarse conversion via the transfer switch, it is preferred to lower its on-resistance to reduce the impact on the DAC settling accuracy. Therefore, in the prototype design, bootstrapped switches with a reasonably large size are utilized to lower the on-resistance. In addition, the inter-stage redundancy can partly alleviate DAC settling errors during the coarse cycles due to the impact of the transfer switch.

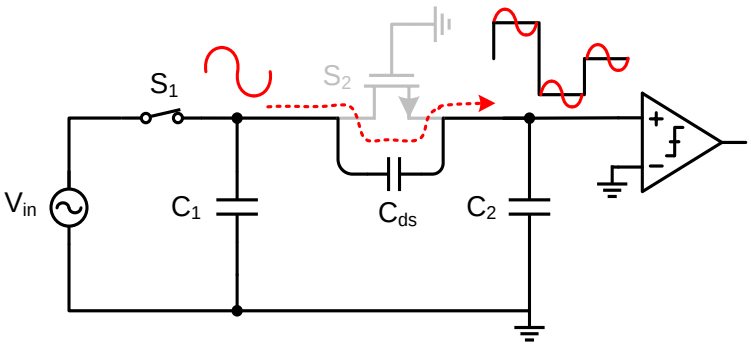



Figure 3.5. Signal feed-through caused by the drain-source capacitance of the transfer switch

Another potential issue related to the transfer switch is the signal feed-through. As illustrated in Figure 3.5, when the transfer switch is off, the signal on the summing node of the first-stage DAC will couple to the summing node of the second stage through the $C_{ds}$ of the transfer transistor. This interference can potentially cause dynamic offsets for the second stage

and degrade its conversion accuracy. T-switch is one option for isolating the off-switch coupling, but it exhibits a large on-resistance due to the series connection of transistors. Dummy switch that cross-connect the summing nodes of the first stage and the second stage are added to cancel the signal feed-through error [19]. Naturally, the effect of the feed-through compensation depends highly on the matching between the dummy switch and the transfer switch and it is not guaranteed over manufacturing variations. To further mitigate the feed-through problem, some source and drain contacts in the layout of the transfer switch and dummy switch are removed (as shown in Figure 3.6), resulting in a more than 10× reduction of $C_{ds}$ [20]. Additionally, one can also add ground shields over the source and drain regions without contacts to achieve a more than 30× reduction [21].

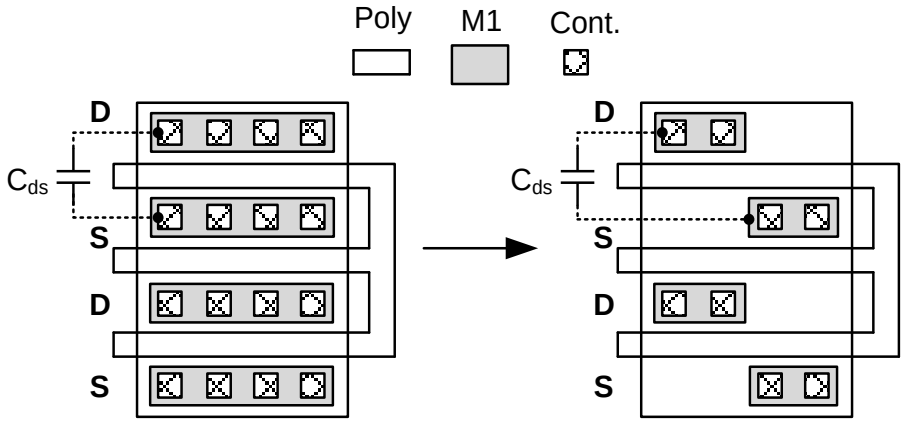



Figure 3.6. Layout of transfer switch with small drain-source capacitance

## 3.4 COMPARATOR AND DYNAMIC REGISTER

The strong-arm latch in Figure 3.7, which exhibits a high regeneration speed and consumes only dynamic power, is used as the comparators in this work. An extra differential pair is introduced to facilitate the foreground offset calibration. To reduce the impact of the calibration

pair on the speed and noise performance of the comparator, its size is set to a quarter of the main input pair. Since the comparator decision time constitutes a critical part of the SAR loop delay, its input common-mode voltage is set to 800 mV to boost the regeneration speed [22]. The input-referred noise power of the comparator in the second stage is designed to be half of the quantization noise power. So, the comparator noise and the kT/C noise together lead to an SNR degradation of 3 dB to the overall ADC.

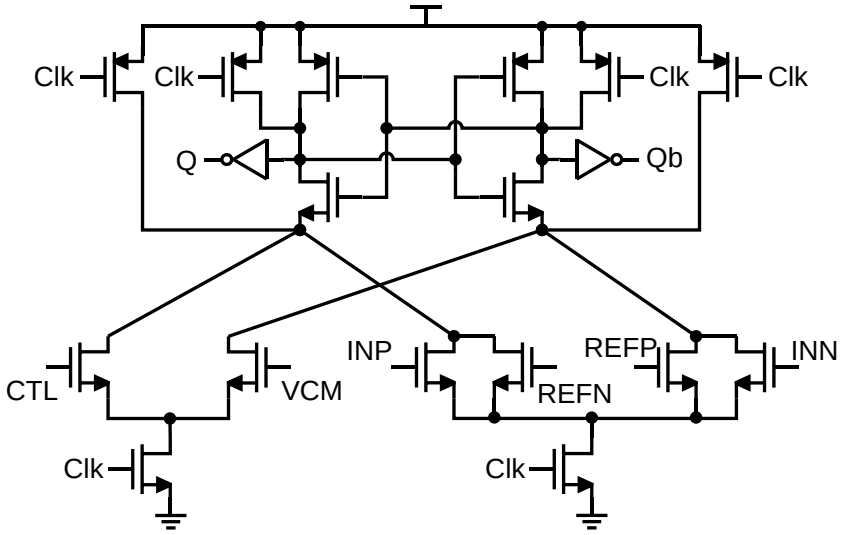
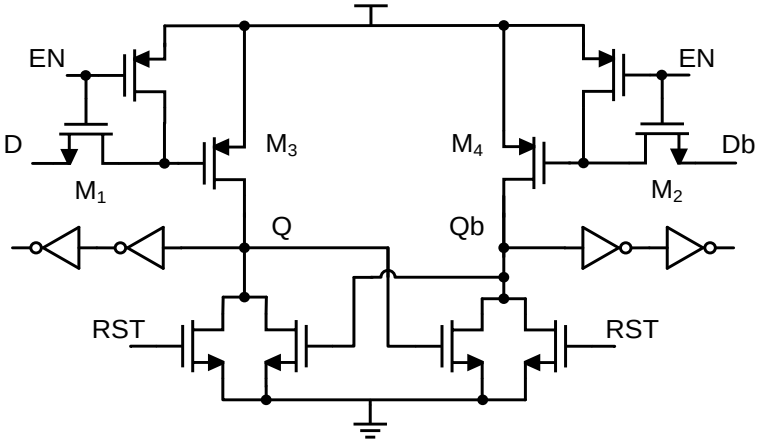


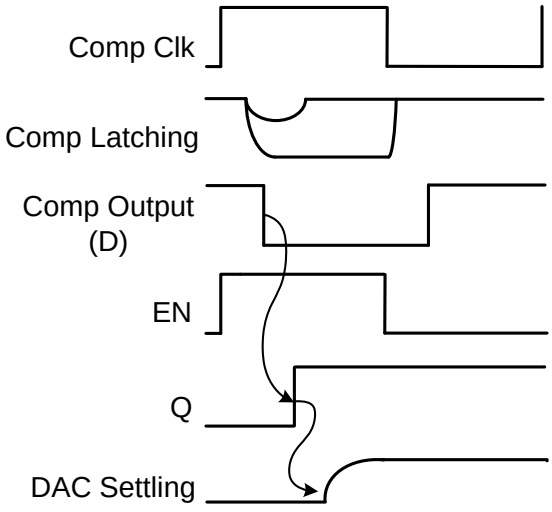

Figure 3.7. Dynamic comparator with an extra input pair for offset calibration

To implement the successive approximation operation, a set of registers are utilized to capture the comparator outputs and then feed the outputs back to the DAC as quickly as possible. The delay from the comparator output to the DAC switches is also a critical part of the SAR loop delay. In this design, the dynamic register in Figure 3.8 (modified from [4] and [23]) is adopted to minimize this delay. Unlike the conventional D-flip flop, this dynamic register is directly triggered by the comparator output (i.e., level sensitive) instead of by an additional latching clock, so the extra delay from the comparator output to the latching clock is removed.

Furthermore, in each bit cycle only one dynamic register is enabled (EN=1) and connected to the comparator through $M_1$ and $M_2$, leading to a small capacitive loading to the comparator. When the dynamic register completes regeneration, it will be disconnected from the comparator (EN=0) and the gates of $M_3$ and $M_4$ will be pulled up to $V_{DD}$, making the register insensitive to the interference from the comparator output.




(a)




(b)

Figure 3.8. (a) Schematic of the dynamic register and (b) Timing diagram of the dynamic register

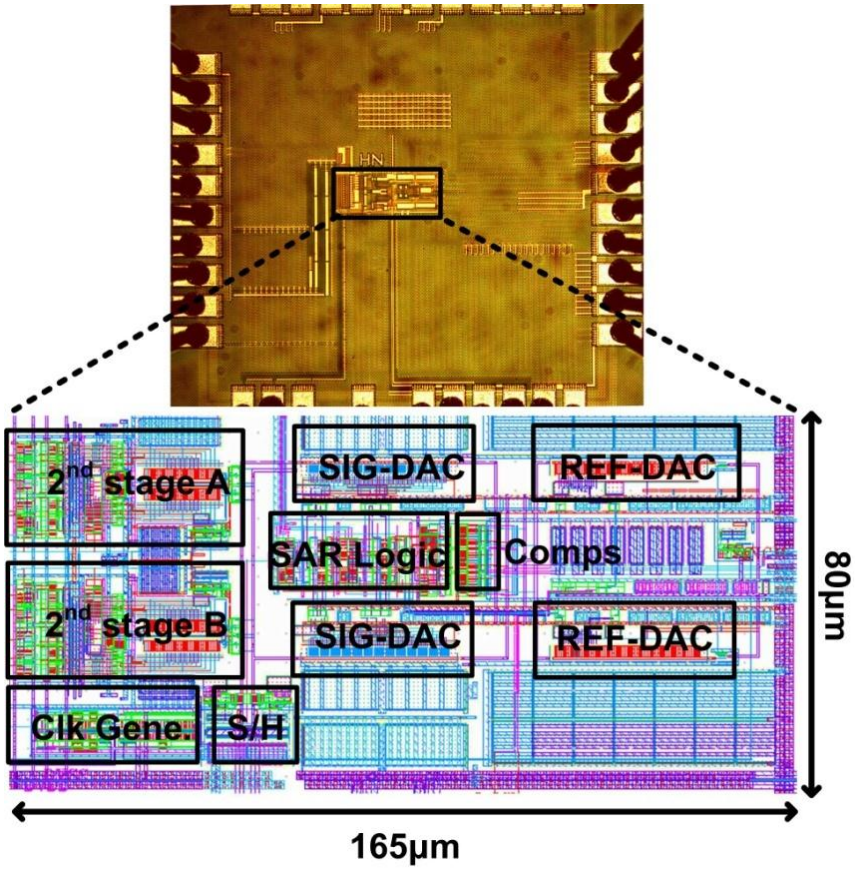



Figure 3.9. Die photo

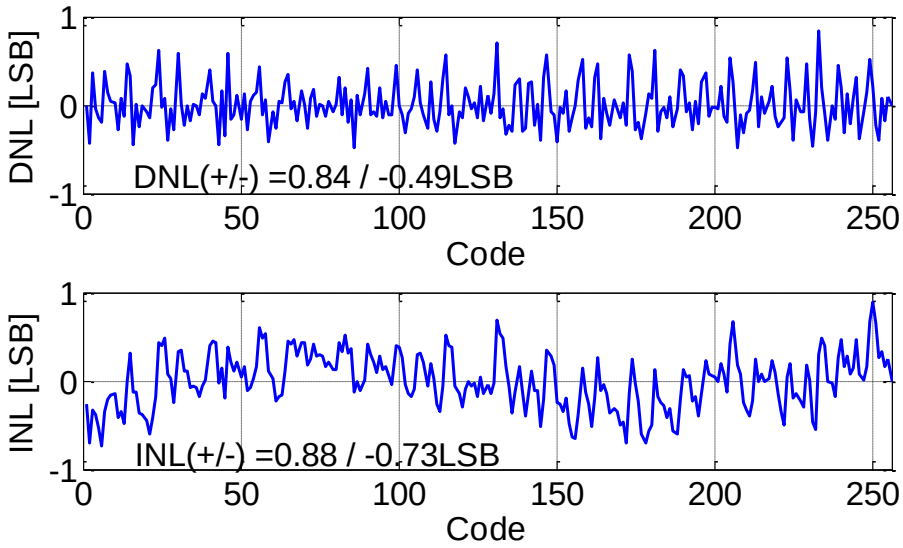
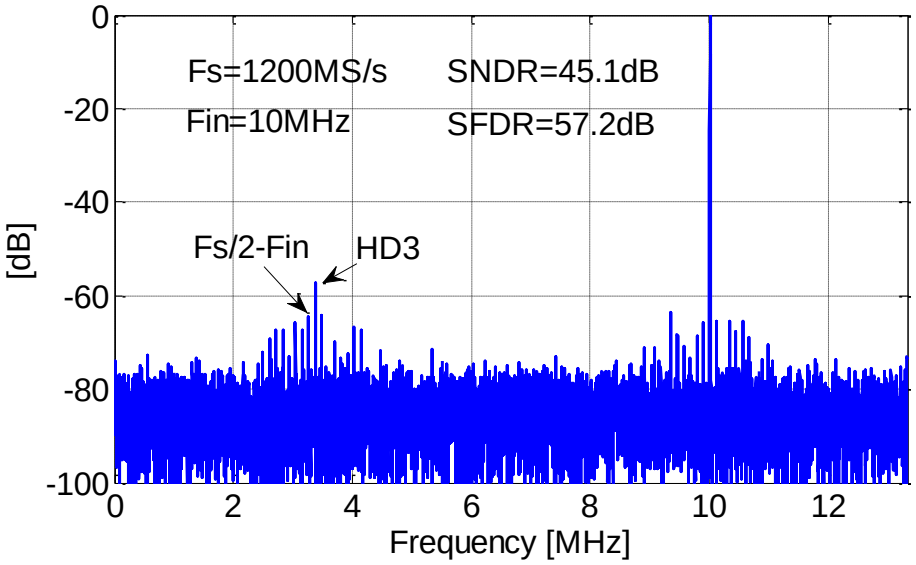
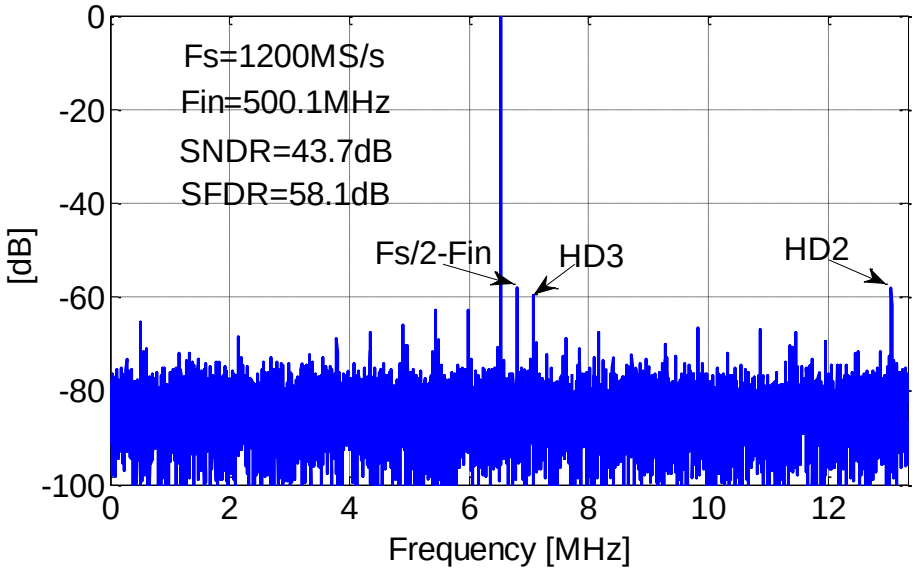



Figure 3.10. Measured DNL and INL profiles

### 3.5 MEASUREMENT RESULTS




(a)




(b)

Figure 3.11. Measured ADC spectra at 1.2 GS/s with (a) a near-DC input and (b) a near-Nyquist input (both decimated by 45×)

The prototype ADC was fabricated in a 65 nm CMOS process. A die photo is shown in Figure 3.9. The ADC occupies an active area of 165 μm×80 μm. The measured DNL and INL profiles after comparator offset calibration are shown in Figure 3.10. The maximum DNL and INL are +0.84/−0.49 LSBs and +0.88/−0.73 LSBs, respectively.

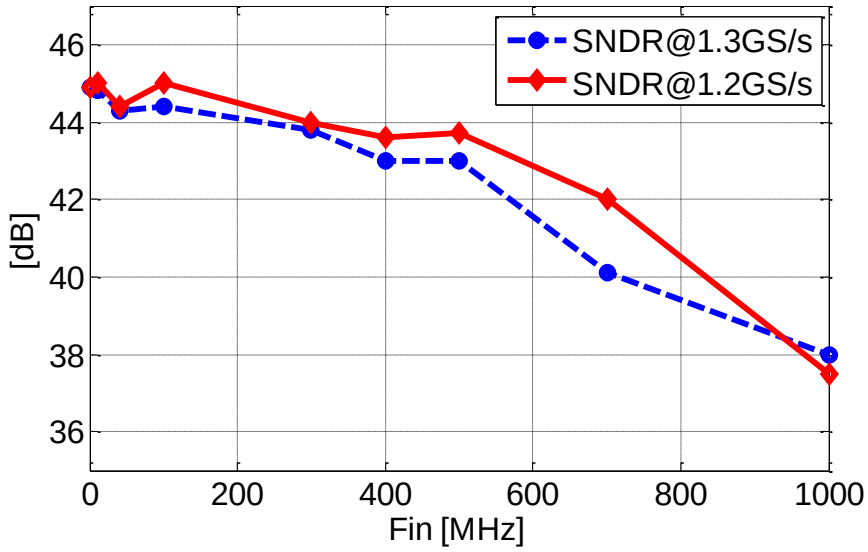



Figure 3.12. Measured SNDR at 1.3 GS/s and 1.2 GS/s vs. input frequency

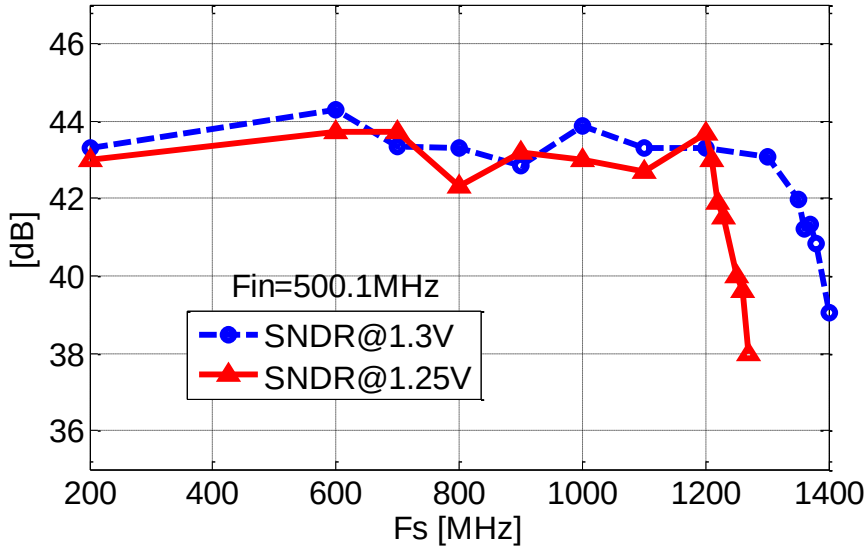



Figure 3.13. Measured SNDR at1.3 V and 1.25 V supplies vs. sampling frequency

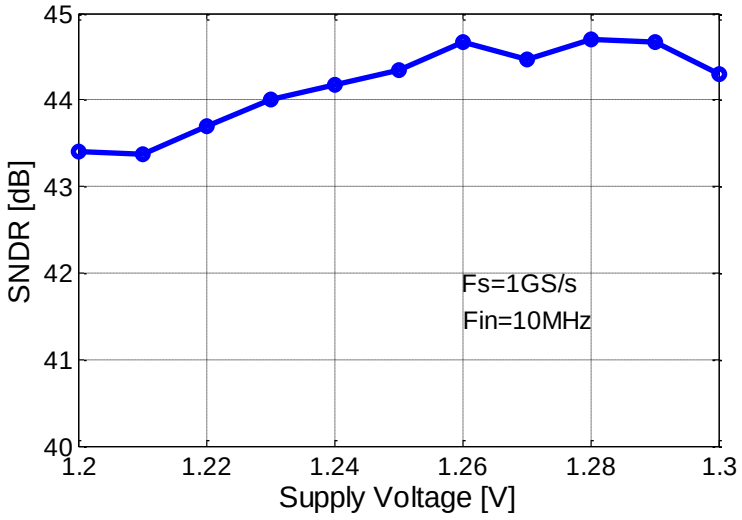



Figure 3.14. Measured SNDR vs. supply voltage

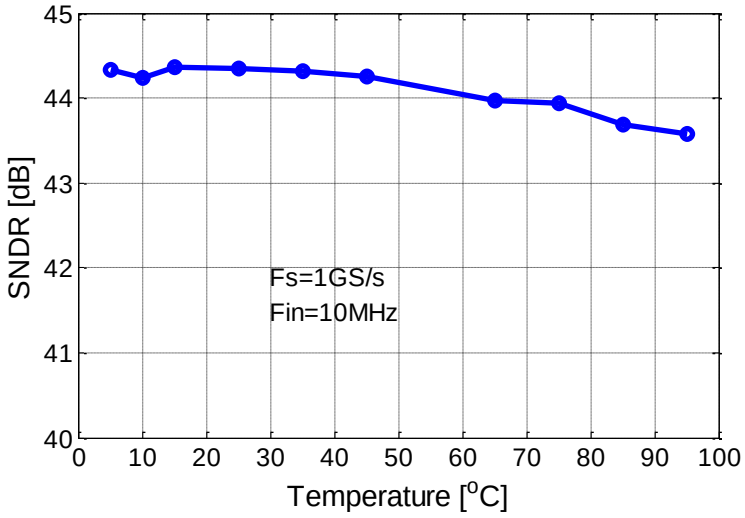



Figure 3.15. Measured SNDR vs. ambient temperature

The dynamic performance of the ADC after static radix calibration (including inter-stage gain calibration) and ping-pong gain mismatch calibration is shown in Figure 3.11; the achieved signal-to-noise plus distortion ratio (SNDR) is 45.1 dB and the spurious-free dynamic range (SFDR) is 57.2 dB for a 10 MHz input. For a 500.1 MHz input, the measured SNDR is 43.7 dB

and the SFDR is 58.1 dB (42.5 dB and 56.8 dB with only offset calibration, respectively). The spurious tone produced by bandwidth mismatch limits the SFDR when the input frequency approaches the Nyquist value, at which the second harmonic also pops up, most likely induced by the phase imbalance between the differential input traces. Figure 3.12 summarizes the measured SNDR for various input frequencies at 1.25 V and 1.3 V supply voltages. The effective resolution bandwidth of the ADC is larger than 600 MHz and the ENOB remains above 6 bits with even a 1 GHz input. Figure 3.13 plots the measured SNDR with a 500.1 MHz input at 1.25 V and 1.3 V power supplies versus the sampling frequency. The SNDR fluctuation is suspected to be caused by the input signal coupling through the $C_{ds}$ of the sampling switch. Limited by the comparator speed, the SNDR starts to drop rapidly around 1.2 GS/s and 1.3 GS/s sample rates.

Table 3.1 Power Consumption Breakdown

| Sample Rate<br>@ Supply | 1.2 GS/s<br>@ 1.25 V | 1.3 GS/s<br>@ 1.3 V |
|---|---|---|
| Analog Circuits | 2.3 mW (46%) | 2.71 mW (47%) |
| Digital Circuits | 2.42 mW (48%) | 2.8 mW (48%) |
| DAC Reference | 0.28 mW (6%) | 0.29 mW (5%) |
| Total | 5 mW | 5.8 mW |

During the test, the power supply voltage and the temperature were also swept to check the robustness of this design. When the supply voltage varies from 1.2 V to 1.3 V, the measured SNDR fluctuates by 1.3 dB (see Figure 3.14). Figure 3.15 shows the temperature dependency of the measured SNDR. The SNDR variation between 5 ℃ and 95 ℃ is around 0.8 dB. The small SNDR fluctuations demonstrated in Figure 3.14 and Figure 3.15 also prove that the advocated

non-attenuated passive residue transfer has a stable gain response over supply voltage and temperature variations.

Table 3.2 Performance Summary

| | | |
|---|---|---|
| CMOS Tech. [nm] | 65 | |
| Resolution [bits] | 8 | |
| Supply Voltage [V] | 1.25 | 1.3 |
| Sample Rate[GS/s] | 1.2 | 1.3 |
| Power [mW] | 5 | 5.8 |
| Area [$mm^2$] | 0.013 | |
| DNL [LSBs] | +0.84/-0.49 | |
| INL [LSBs] | +0.88/-0.73 | |
| SNDR [dB]@fin=500MHz | 43.7 | 43.1 |
| SFDR [dB]@fin=500MHz | 58.1 | 57.8 |
| FoM [fJ/conv.step] | 35 | 38 |

Table 3.1 presents the breakdown of the power consumption. 46% of the power (2.3 mW) is consumed by the comparators and the bootstrapped circuits while 48% (2.42 mW) is spent on the clock generator and the SAR logic. The power consumption of the DAC references only takes 6% of the total (0.28 mW). Table 3.2 summarizes the performance of the prototype ADC at 1.25 V and 1.3 V power supplies. Clocked at 1.2 GS/s, the ADC achieves an SNDR of 43.7 dB and consumes a total power of 5.0 mW, culminating in a conversion figure of merit (FoM) of 35 fJ/conversion-step.

Table 3.3 Performance Comparison

| Works | VLSI'12 Chan [25] | VLSI'12 Lien [26] | JSSC'15 Hong [4] | JSSC'13 Kull [7] | This work | |
|---|---|---|---|---|---|---|
| Architecture | 2b/cycle SAR,TI | 2b/cycle SAR | 2b/cycle SAR | SAR | Two-step SAR | |
| CMOS Tech.[nm] | 65 | 28 | 45 | 32 SOI | 65 | |
| Resolution[bits] | 8 | 8 | 7 | 8 | 8 | |
| Sample Rate[GS/s] | 1 | 0.75 | 1 | 1.2 | 1.2 | |
| Power [mW] | 4 | 4.5 | 7.2 | 3.1 | 5.0 | |
| Area [$mm^2$] | 0.013 | 0.004 | 0.016 | 0.0015 | 0.013 | |
| SNDR [dB] | 42.8 | 43.2 | 40.8 | 39.3 | 43.7 | 42.5† |
| SFDR [dB] | 58.5 | 57.5 | 50.6 | 50 | 58.1 | 56.8† |
| FoM [fJ/conv.step] | 34 | 41 | 80 | 34 | 35 | 39† |

† Measured with only offset calibration

Table 3.3 compares this work to some state-of-the-art designs reported recently. Thanks to the passive residue transfer and the 2b-1b/cycle conversion scheme, this work achieves the highest conversion speed among the high-speed SAR ADCs published recently. One point should be noted is that even with a 65 nm bulk process the prototype ADC still achieves a comparable speed to another design fabricated in a 32 nm SOI process. As illustrated in the table, this work also attains a very similar SNDR and power efficiency as the best counterpart designs.

## 3.6 SUMMARY

A 1.2 GS/s, 8 bit two-step SAR ADC based on passive residue transfer and a 2b-1b/cycle conversion scheme has been reported in this chapter. Attributing to the passive residue transfer, the time and power consumption associated with residue production are mostly removed and the

SAR ADC can further improve its throughput, manifested by the comparison with recently reported high-speed SAR ADCs of similar resolutions. Meanwhile, a 2b-1b/cycle conversion scheme with a proper resolution partition is employed to further enhance the conversion speed. Fabricated in a 65 nm CMOS process, the prototype ADC achieves an SNDR of 43.7 dB and a FoM of 35 fJ/conversion-step at a sample rate of 1.2 GS/s with a near-Nyquist frequency input.

# CHAPTER 4

# PIPELINED SAR ADC WITH PVT-STABILIZED DYNAMIC AMPLIFIER[4]

## 4.1 RESIDUE AMPLIFICATION IN PIPELINED SAR ADCS

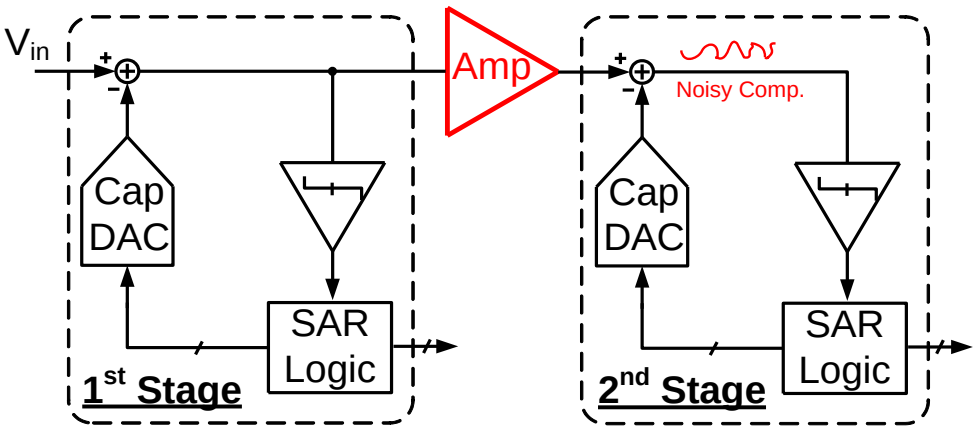



Figure 4.1. Block diagram of pipelined SAR ADC

Let's firstly revisit the block diagram of a typical pipelined SAR ADC shown in Figure 4.1, which is made up of two separate SAR ADCs and a residue amplifier in between. As mentioned earlier, the amplifier can be removed by using passive residue transfer. However, for high resolution pipelined SAR ADCs, the noise of second-stage comparator contributes to the overall noise budget significantly. As the DAC output approaches the input signal successively, the comparator noise needs to be decreased exponentially, resulting in a exponential increase on the power consumption of the second-stage comparator as illustrated in Figure 4.2. Normally, the residue amplifier is utilized in high resolution pipelined SAR ADCs to attenuate the noise

[4] ©2017 IEEE. Portions Adapted, with permission, from H. Huang, S. Sarkar, B. Elies, and Yun Chiu. "A 12b 330MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving <1dB SNDR variation", 2017 IEEE International Solid-State Circuits Conference, 2017

coming from the second stage. Because of the residue amplification, the requirement on the noise of second-stage comparator is relaxed, naturally decreasing the power consumption of the comparator. As we can see from Figure 4.3, because of the only one high-energy event of the amplifier, the power efficiency of the pipelined SAR ADC with residue amplifier is still better than the counterpart without residue amplifier.

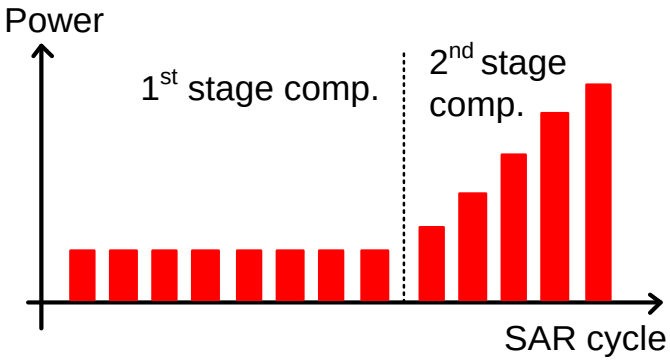



Figure 4.2. Power consumption of pipelined SAR ADC with passive residue transfer

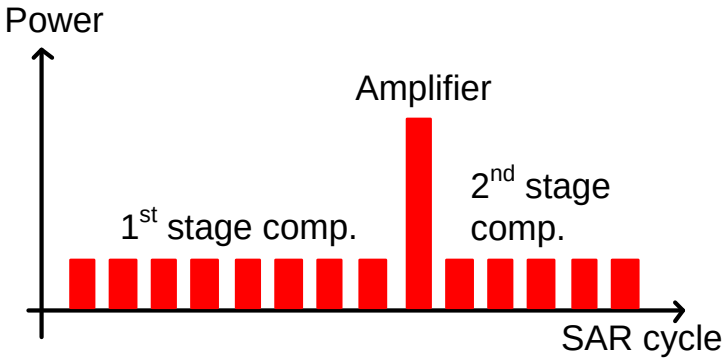



Figure 4.3. Power consumption of pipelined SAR ADC with residue amplifier

As the conversion speed and power efficiency of SAR ADCs have been significantly improved in the past decade, the residue amplifier becomes one of the most critical factors limiting the performance of pipelined SAR ADC. This is particularly true for scenarios targeting high speed and high resolution.

Operational amplifier is a traditional approach to implement the residue amplifier for pipelined SAR ADC. Unfortunately, as CMOS technology scales, the op-amp design becomes increasingly more difficult due to the decreasing intrinsic gain. Although some techniques such as gain boosting and multistage amplifier can be used to increase the gain, these techniques bring about considerable signal swing and speed penalties.

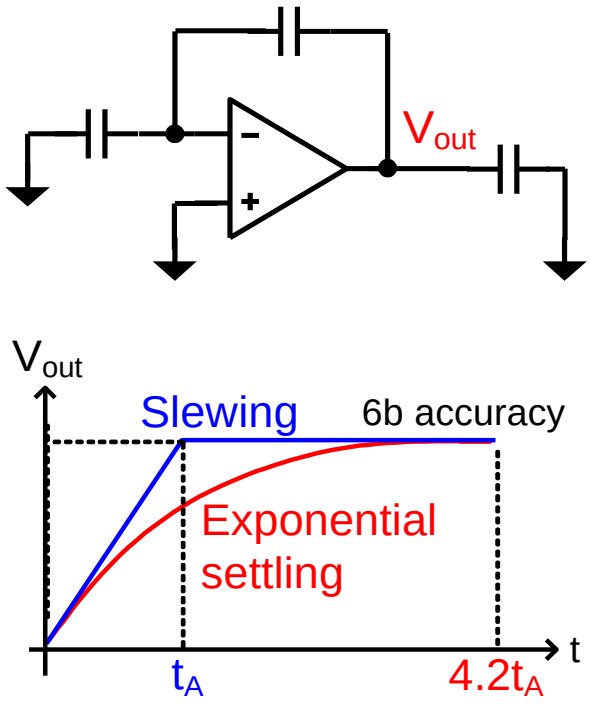



Figure 4.4. Opamp-based residue amplifier and its exponential settling curve

As we all know, during the amplification, the opamp output voltage normally settles to the final value with an exponential trajectory. Essentially, this settling behavior is very time inefficient. As shown in Figure 4.4, for a 6bit settling accuracy, the required settling time of opamp is about four times longer than that of the amplifier with a slewing settling. Because of this inefficient settling behavior, op-amp-based residue amplifier has to consume a lot of power to meet the settling time requirement.

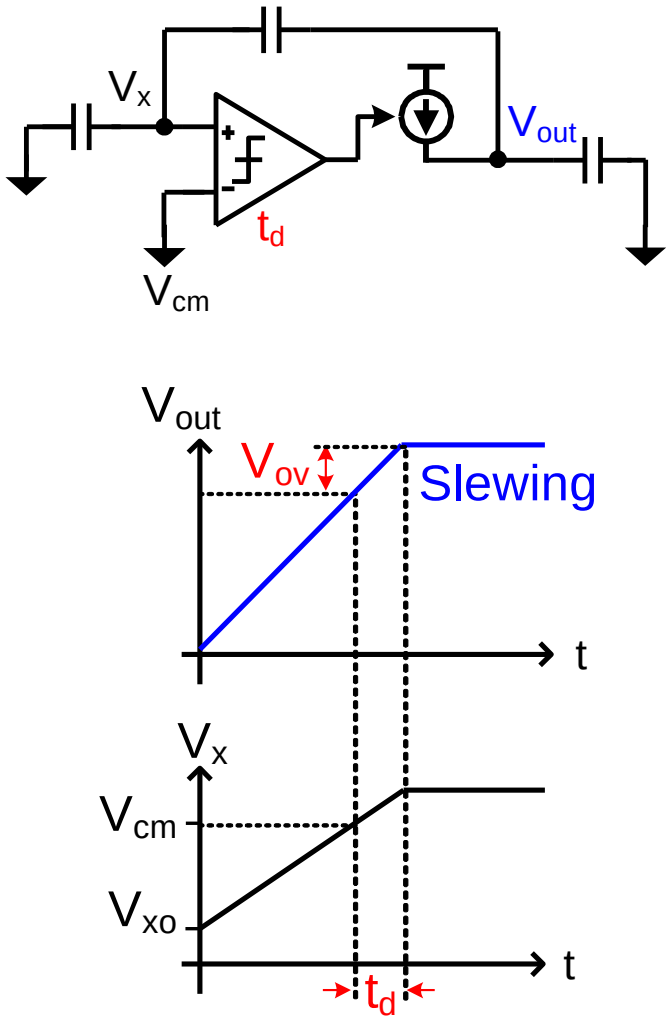



Figure 4.5. Comparator-based residue amplifier and its overshoot problem

Unlike the conventional opamp, the comparator-based residue amplifier in Figure 4.5 achieves the slewing settling and thus its associated benefits [27]. However, the finite delay of the comparator introduces an overshoot problem which unfortunately degrades the settling accuracy of the amplifier. As demonstrated in Figure 4.6, with the help of another fine discharging phase, the overshoot can be partly reduced at the cost of settling speed. Moreover, the voltage drop across the reference's resistor is a function of input signal. This will cause data-

dependent modulation of reference voltage and bring second-order bowing to the transfer function of the whole ADC [28].

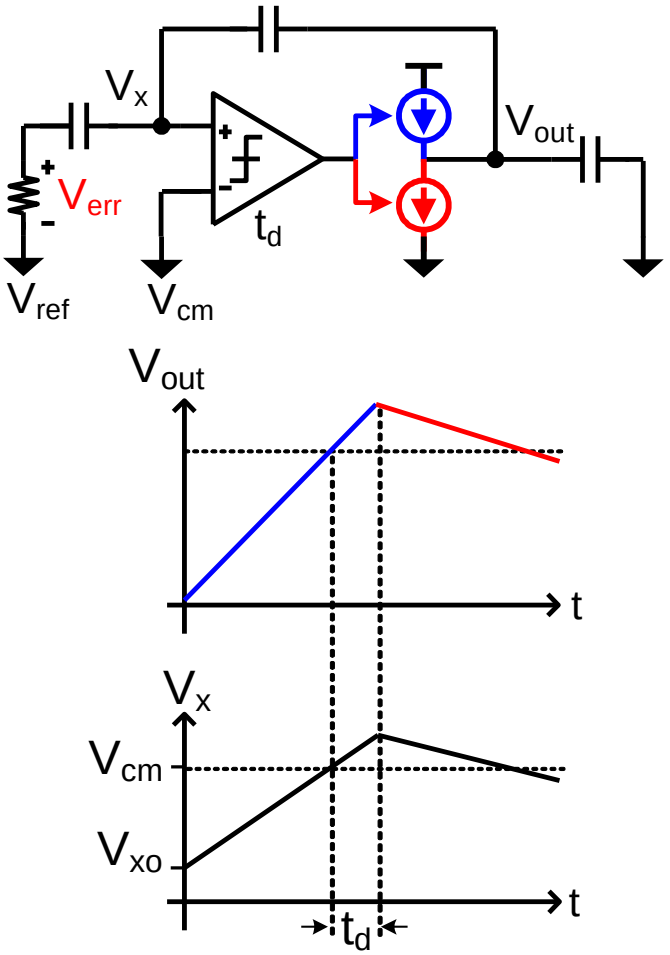



Figure 4.6. Overshoot cancellation with another fine discharge phase

In addition to the comparator-based residue amplifier, open-loop dynamic amplifier is another amplification technique with a slewing settling behavior [29]. Figure 4.7 shows the schematic and operation principle of the open-loop dynamic amplifier. First, in the reset phase, the outputs are pre-charged to the supply voltage. Then, triggered by the clock phase $\Phi_A$, the outputs start to discharge with the slew rates depending on the inputs. Lastly, when the clock $\Phi_A$ turns low, the amplified outputs are sampled by the load capacitors. Since there is no feedback

applied in this circuit, the dynamic amplifier doesn't suffer from the overshoot problem. Furthermore, the dynamic nature of this amplifier allows it to consume zero static current, leading to an excellent power efficiency.

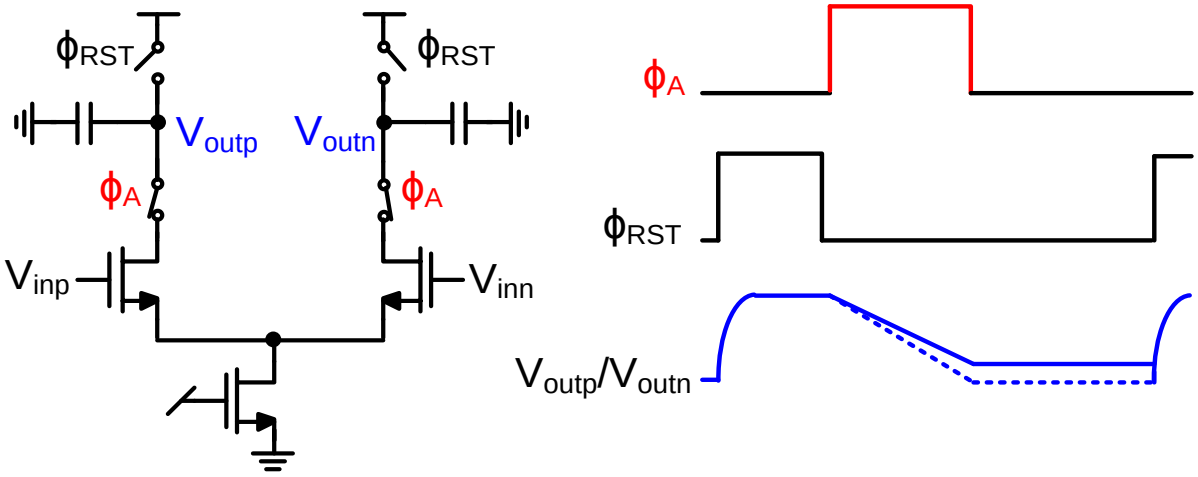



Figure 4.7. Schematic and operation waveforms of open-loop dynamic amplifier

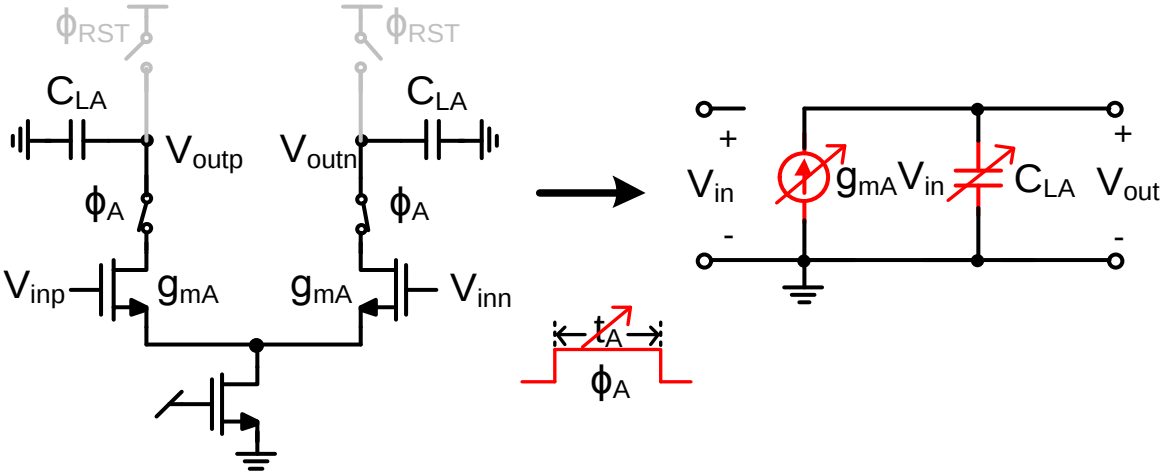



Figure 4.8. Circuit model for open-loop dynamic amplifier

Unfortunately, the advantages of dynamic amplifier are accompanied by the problem of gain instability. To better understand this issue, as shown in Figure 4.8, the dynamic amplifier is

modeled as an input-controlled current source charging or discharging a load capacitor. According to this model, the gain can be easily derived as:

$$V_{out} = \frac{g_{mA} V_{in}}{C_{LA}} \cdot t_A. \tag{4-1}$$

Because the transconductance ($g_{mA}$), load capacitance ($C_{LA}$) and slewing time ($t_A$) are non-constant over PVT variations, the gain can potentially drift dramatically.

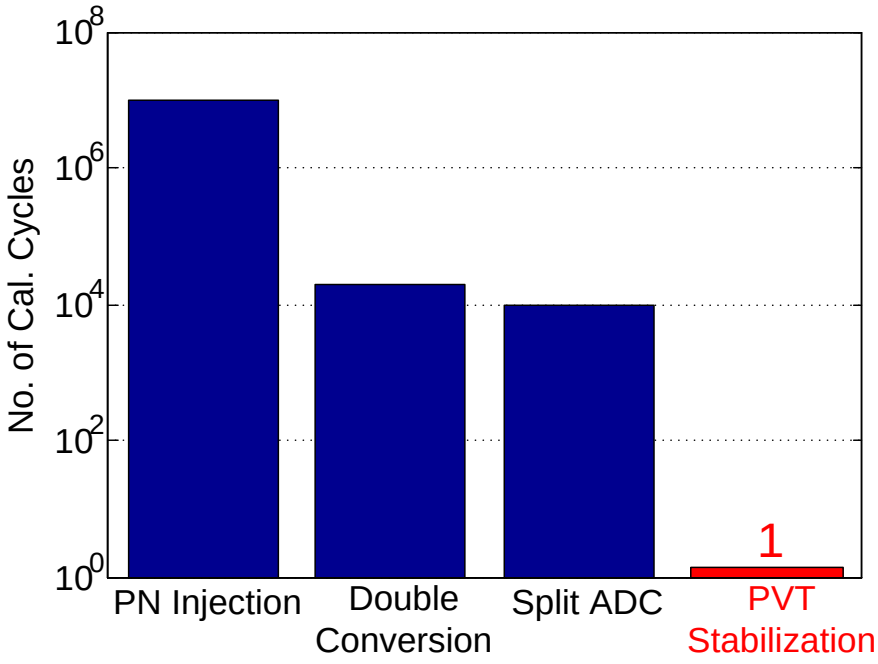



Figure 4.9. Long convergence time of digital background calibration

The conventional way to compensate for gain instability is to employ continuous background calibration [30]. However, as we can see in Figure 4.9 these calibrations suffer from long convergence time [16][31]. Furthermore, most of these calibrations exhibit some constraints on the statistical property of the input signal. Next section will present an analog background approach to stabilize the voltage gain [32]. This stabilization technique can response to the environmental changes within one conversion cycle. And it can work immediately after power up.

This feature enables its application in some scenarios wherein the startup time of the ADC is also important.

## 4.2 PVT-STABILIZED DYNAMIC AMPLIFIER

Although the absolute value of transconductance and load capacitor can vary a lot over PVT changes, the ratio between two capacitors and that between two transconductances can be very stable in monolithic forms. If the slewing time $t_A$ in equation (4-1) can be proportionally set to $C_L/g_m$ as follows:

$$t_A \propto \frac{C_L}{g_m}, \tag{4-2}$$

where $C_L$ and $g_m$ are the load capacitance and transconductance of a replica amplifier, then the gain expression becomes the product of the capacitor ratio and gm ratio,

$$A_v \propto \frac{C_L}{C_{LA}} \cdot \frac{g_{mA}}{g_m}. \tag{4-3}$$

and this voltage gain should be stable over PVT variations. So the key point here is how can we relate the slewing time $t_A$ with $C_L/gm$?

To answer this question, let's take a look at the single-pole replica amplifier in Figure 4.10. When the single-pole amplifier is driven by a small step input, its output displays an exponential settling curve plotted in the right part of Figure 4.10. It is interesting to note that the beginning part of the exponential curve can be approximated as a ramp whose slew rate contains the ratio

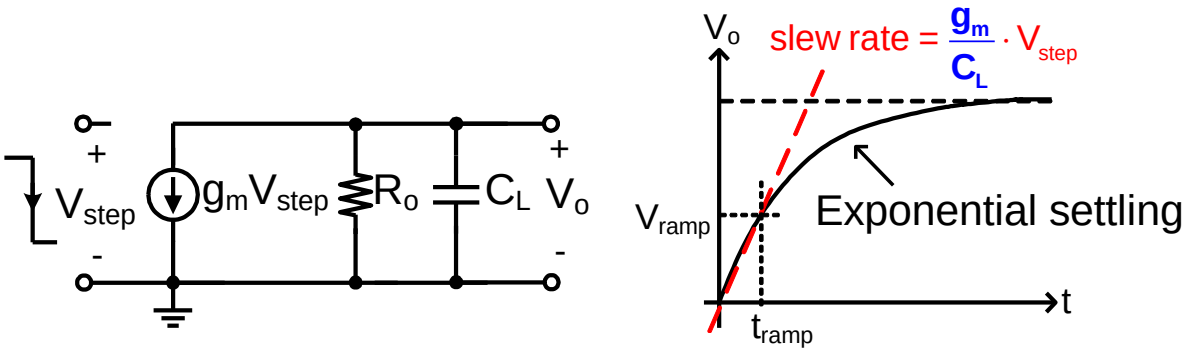



Figure 4.10. The step response of single-pole amplifier

$g_m/C_L$. To ensure this approximation, the single-pole amplifier should not enter into the slewing region and this poses a constraint on the amplitude of step input,

$$V_{step} < 2\sqrt{2}V_{ov}, \tag{4-4}$$

where $V_{ov}$ is the overdrive voltage of the input pair of this amplifier.

The ramp cure in Figure 4.10 can be described as,

$$V_{ramp} = \frac{g_m}{C_L} \cdot V_{step} \cdot t_{ramp}. \tag{4-5}$$

when a voltage to time conversion (V2T) is applied to the ramp, the time $t_{ramp}$ which correlates to $C_L/g_m$ can be obtained:

$$t_{ramp} = \frac{C_L}{g_m} \cdot \frac{V_{ramp}}{V_{step}} \tag{4-6}$$

Let's plug $t_{ramp}$ into the gain expression of the conventional dynamic amplifier (4-1), the gain eventually becomes the product of the capacitor ratio, gm ratio and voltage ratio:

$$A_v = \frac{C_L}{C_{LA}} \cdot \frac{g_{mA}}{g_m} \cdot \frac{V_{ramp}}{V_{step}}. \tag{4-7}$$

Assuming that $V_{ramp}$ and $V_{step}$ are generated from the same reference voltage, their ratio will remain constant. Since all these ratios are constant in monolithic forms, the gain of PVT-stabilized dynamic amplifier is expected to be very constant over PVT variations.

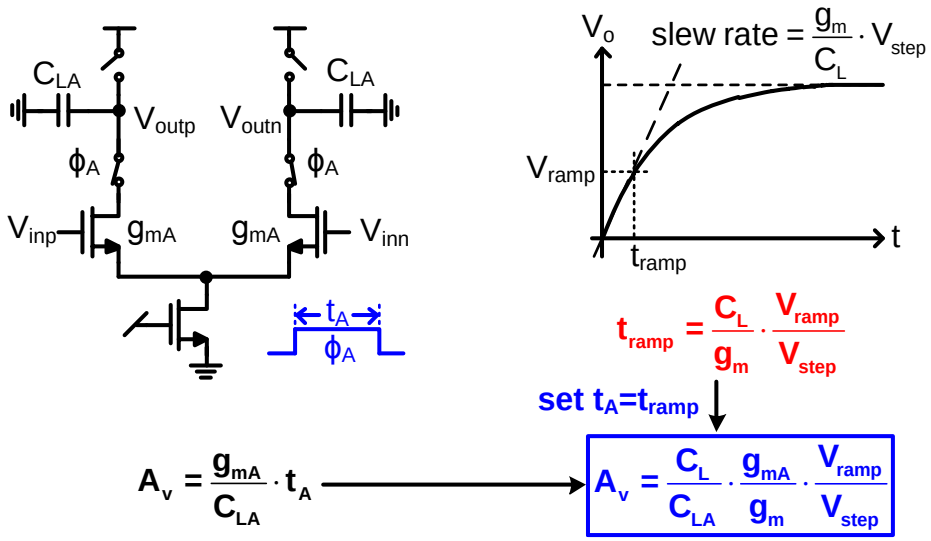



Figure 4.11. Overall concept of PVT stabilization technique

With the concept of PVT stabilization technique in our mind, let's move on to the circuit implementation. As show in Figure 4.12, the PVT-stabilized dynamic amplifier consists of a single-pole amplifier, a V2T converter and a conventional dynamic amplifier.

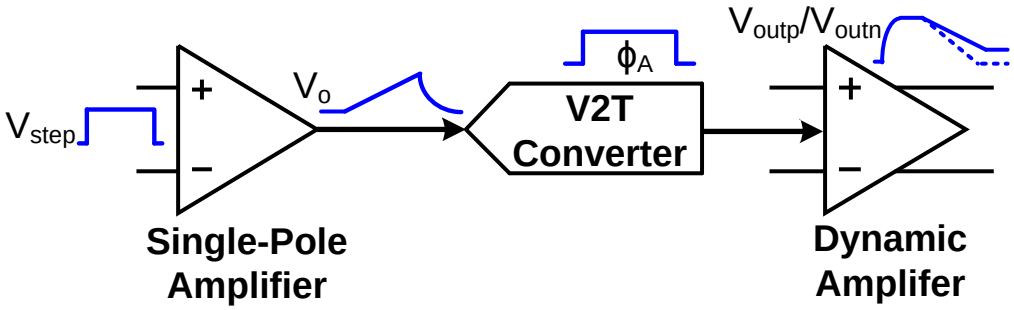



Figure 4.12. Structure of PVT stabilized dynamic amplifier

Figure 4.13 shows the schematic of the single-pole amplifier. The circuit operates as follows. First, in the reset phase, both the input and output of this amplifier are reset. After that, the capacitors $C_1$ are switched to generate a step input which drives the single-pole amplifier to ramp. The step input voltage is expressed as

$$V_{step} = V_{stepp} - V_{stepn} = \frac{C_1}{C_1 + C_2} \cdot 2V_{ref} \tag{4-8}$$

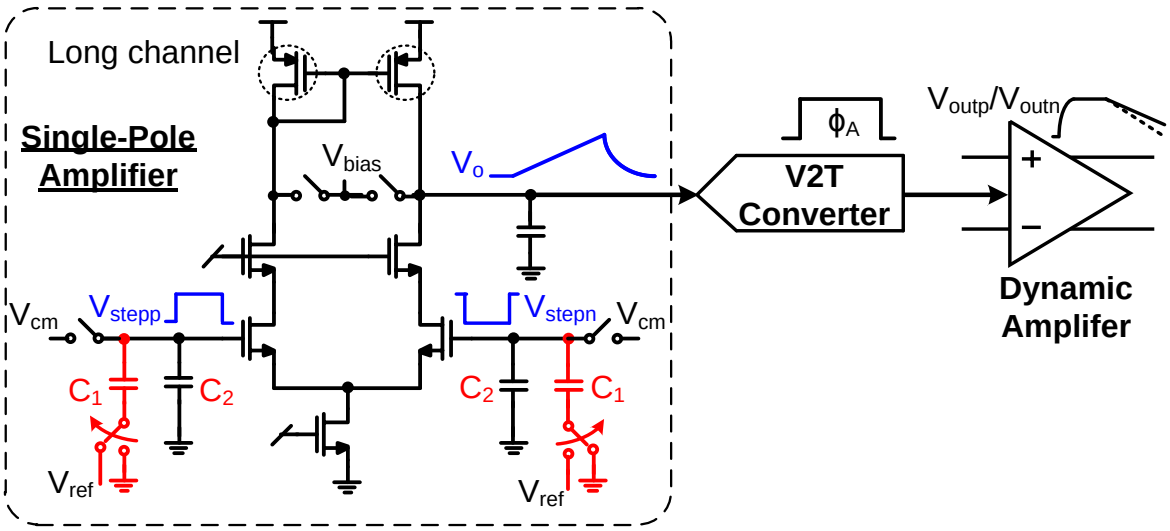



Figure 4.13. Circuit schematic of single-pole amplifier

The voltage to time (V2T) converter is implemented with cascaded inverters as shown in Figure 4.14. To reject any pulse width modulation due to common-mode PVT variations, a pseudo-differential V2T converter is employed instead of a single-ended one. The V2T converter operates as follows. When the single-pole amplifier is resetting, the V2T converters are disconnected from the single-pole amplifier. Meanwhile, the first-stage inverters work in the auto-zeroing mode [33] and all capacitors sample the bias voltage. After that, these two sampling

switches turn off and the capacitors $C_3$ and $C_4$ are switched to add a fraction of reference voltage to the summing nodes. So the threshold voltages of V2T converters are set to $V_{thp}$ and $V_{thn}$,

$$V_{thp} = V_{bias} + \frac{C_3}{2C_{tot}} \cdot V_{ref}, \tag{4-9}$$

$$V_{thn} = V_{bias} + \frac{C_4}{2C_{tot}} \cdot V_{ref}. \tag{4-10}$$

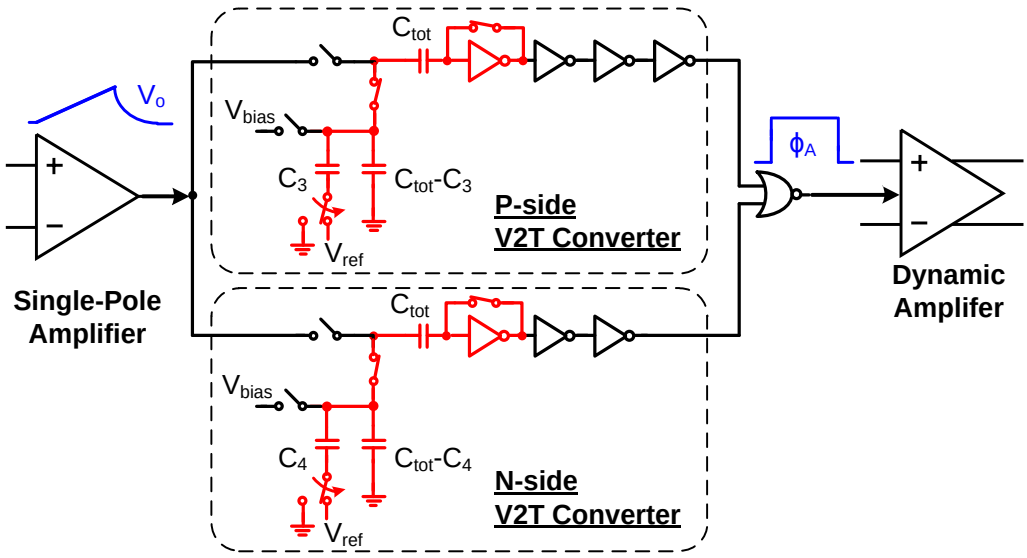



Figure 4.14. Circuit schematic of voltage to time converters

When the single-pole amplifier is ramping, V2T converters are connecting to the single-pole amplifier. Once the ramp signal crosses the threshold voltage of N-side V2T converter, the output clock $\Phi_A$ will turn high and the dynamic amplifier starts to discharge the load capacitor. When the ramp signal crosses the threshold voltage of P-side V2T converter, clock $\Phi_A$ turns low and the dynamic amplifier stops discharging the load capacitor. Note that the voltage difference between $V_{thp}$ and $V_{thn}$ actually defines the quantity $V_{ramp}$,

$$V_{ramp} = V_{thp} - V_{thn}$$
$$= \frac{C_3 - C_4}{2C_{tot}} \cdot V_{ref} \cdot \tag{4-11}$$

Figure 4.15 shows the schematic of the dynamic amplifier wherein cascode transistors are added to improve the linearity of the amplifier.

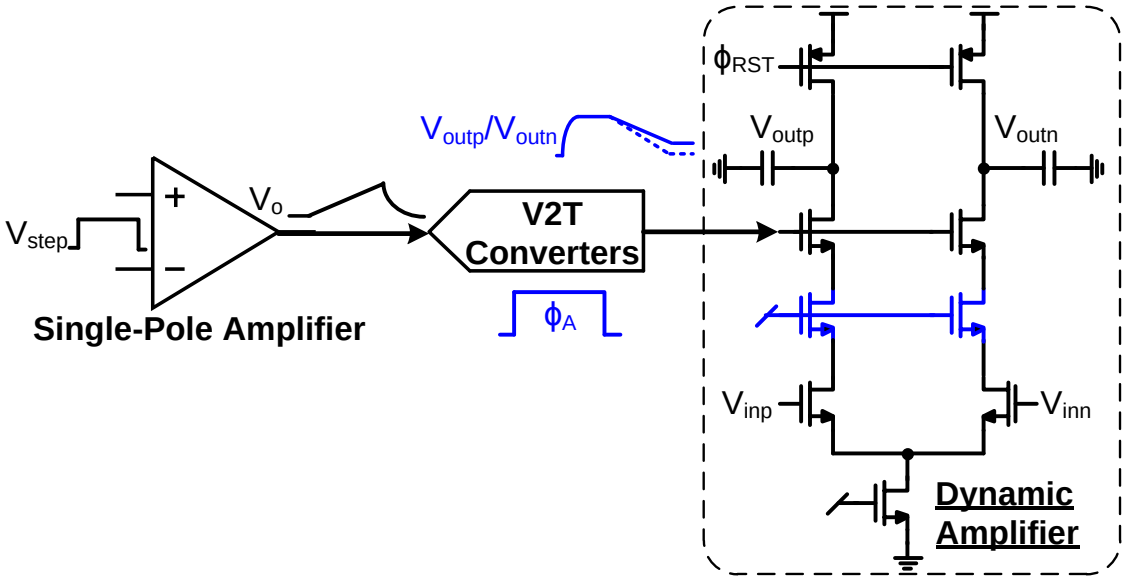



Figure 4.15. Circuit schematic of dynamic amplifier

The overall schematic and gain expression of PVT-stabilized dynamic amplifier are illustrated in Figure 4.16. The gain is finally derived as the product of capacitor ratios and transistor size ratio:

$$A_v = \frac{C_L}{C_{LA}} \cdot \frac{g_{mA}}{g_m} \cdot \frac{V_{ramp}}{V_{step}}$$
$$= \frac{C_L}{C_{LA}} \cdot \frac{W_A}{W} \cdot \frac{(C_1 + C_2) \cdot (C_3 - C_4)}{4C_1 \cdot C_{tot}} \cdot \tag{4-12}$$

Considering that both the capacitor ratio and the transistor size ratio are stable over PVT variations, this voltage gain is expected to remain constant. Besides, it is worth mentioning that the reference voltage, $V_{ref}$, doesn't show up in the final gain expression, which means this reference voltage doesn't need to be precisely set.

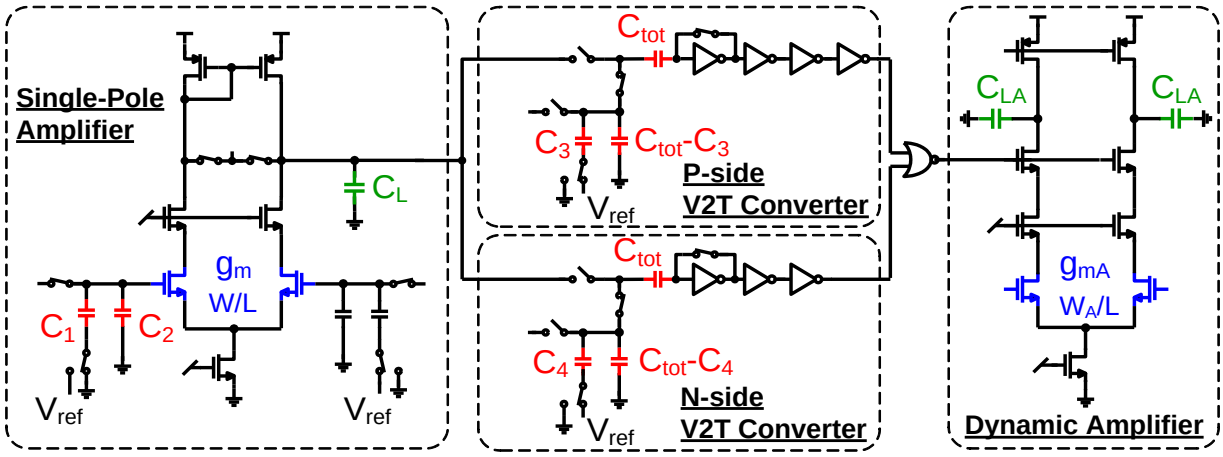



Figure 4.16. Overall schematic of PVT-stabilized dynamic amplifier

## 4.3 PROTOTYPE 12B 330MS/S ADC

### 4.3.1 ADC ARCHITECTURE

Figure 4.17 demonstrates the schematic of prototype 12b 330MS/s ADC. To improve the conversion speed, a 2b/cycle conversion scheme is utilized in the first stage SAR ADC [4]. In this scheme, the comparator offsets can potentially degrade the overall conversion accuracy. So, in the work, the comparator offsets are calibrated in a foreground way. From the speed standpoint, making the second stages also 2b/cycle will probably deliver the highest conversion speed. However, due to the small inter-stage gain (5x), the LSB size of the second stage is much smaller than that of the first stage. So the comparator offsets and the mismatch between the SIG-DAC

and REF-DAC will make the second stage difficult to achieve the desired resolution. In this work, 1b/cycle is applied to the second stage.

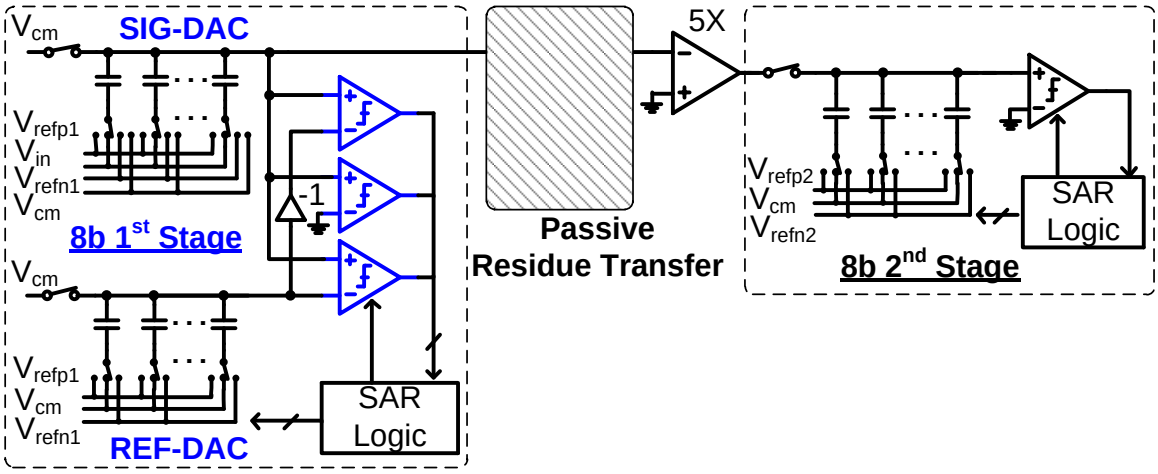



Figure 4.17. Schematic of the prototype pipelined SAR ADC

In this design, the first stage is designed to contain 1bit redundancy for tolerating the comparator offset variations during the coarse conversion cycles. Furthermore, 2bit inter-stage redundancy is allocated to cover small decision errors in the first stage as well as offset drifts of the amplifier and comparators. For this prototype, a one-time power-up calibration was performed to correct the bit weights, gain and offset of the residue amplifier.

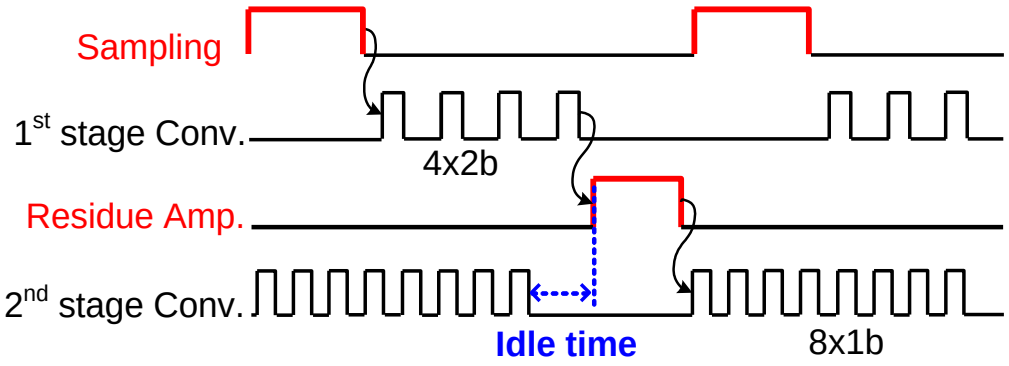



Figure 4.18. Timing diagram of conventional pipelined SAR ADC without passive residue transfer

The timing diagram shown Figure 4.18 reveals the speed limiting factor of the prototype ADC. As can be seen, significant amount of the timing budget is allocated to the input sampling and residue amplification. Therefore, the total conversion time of the first stage is longer than that of the second stage and the first stage becomes the speed bottleneck of the whole ADC.

Fortunately, passive residue transfer is an effective remedy to break this speed bottleneck [8][9]. Its working principle is depicted in Figure 4.19. First, when the first stage is performing the coarse conversion, the transfer capacitor is reset to 0. Once the coarse conversion is done, the LSB capacitor in the first-stage DAC is switched to generate the residue voltage. Then, the transfer switch turns on and the transfer capacitor is utilized to sample the residue voltage. After the residue voltage has been sampled by the transfer capacitor, the first stage is released to sample the next input. Meanwhile, the residue voltage held by the transfer capacitor is amplified.

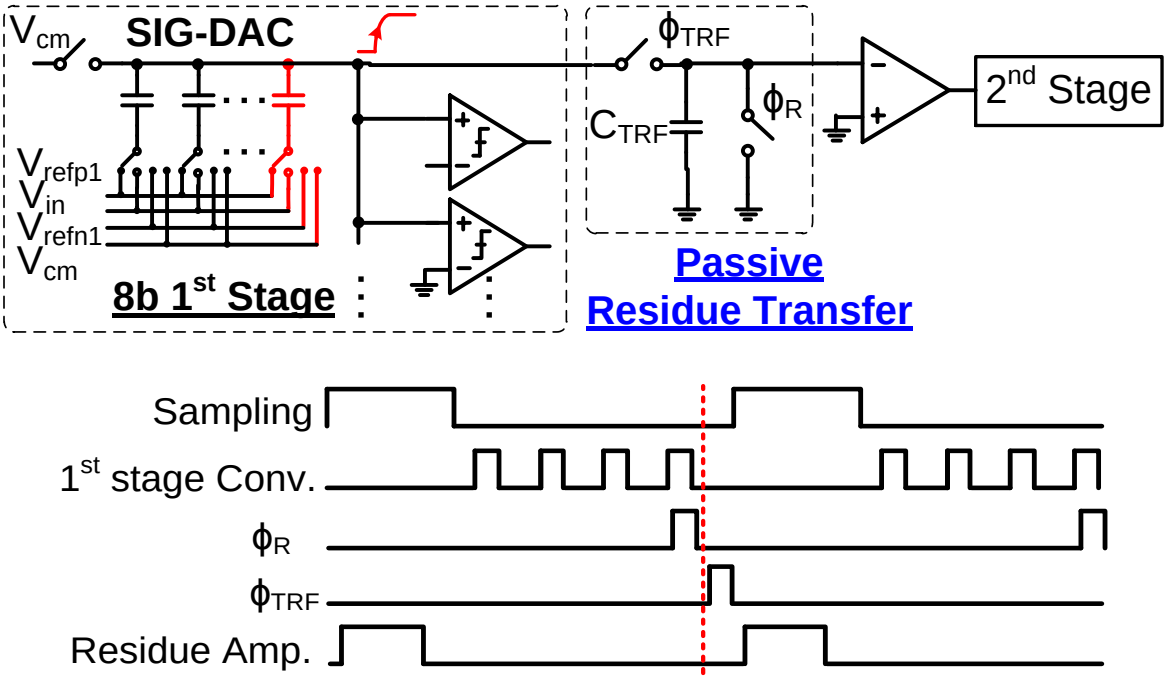



Figure 4.19. Schematic and timing diagram of passive residue transfer

Thanks to the passive residue transfer, the first stage doesn't participate in the residue amplification, so its timing budget is cut down significantly. There is no free lunch. The drawback of this technique is the residue attenuation due to the charge sharing between the DAC and transfer capacitor $C_{TRF}$. To minimize the attenuation effect, a small transfer capacitor would be desirable. On the other hand, the transfer capacitor cannot be too small because it also directly determines the kT/C noise. For the prototype ADC, according to simulation result shown in , the optimum value of the transfer capacitor $C_{TRF}$ is estimated to be 30% of the total DAC capacitance.

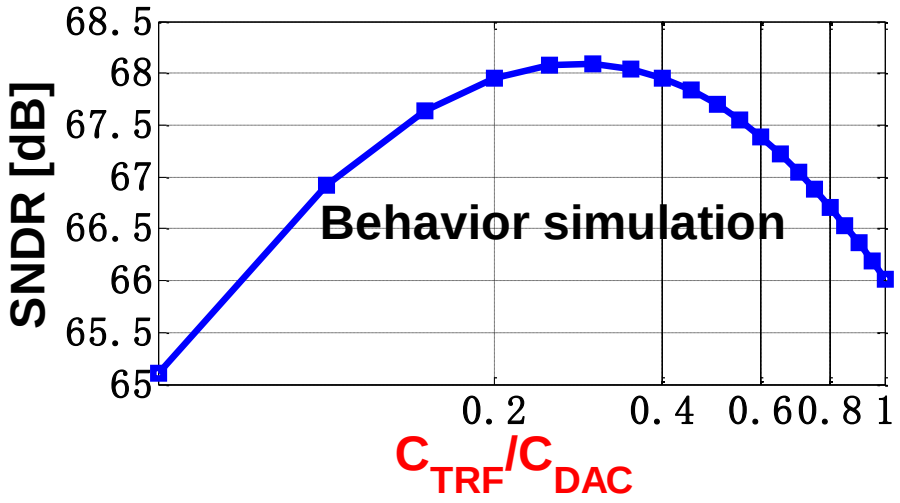



Figure 4.20. Simulated SNR versus $C_{TRF}/C_{DAC}$

### 4.3.2 COMPARATOR WITH KICKBACK CANCELLATION

Figure 4.21 shows the schematic of the dynamic comparator used in the prototype ADC. Generally, the kickback noise is a potential problem for this dynamic comparator. Once the comparator is activated, the source and drain of the input transistors will fall to ground. Through the parasitic capacitors, this falling transition causes kickback noise on the input. As mentioned

previously, due to the small inter stage gain, the LSB size of the second stage is not very large. So the second stage becomes vulnerable to the kickback noise of the second-stage comparator.

In this work, dummy transistors are utilized to cancel the kickback noise [34]. When the comparator is triggered, the source and drain of the dummy transistor will turn to the supply voltage. Ideally, this rising transition of dummy transistor supplies all the charge drawn by the turn-on action of input transistor. As a result, the input doesn't need to provide any charge and the input can get rid of the kickback noise.

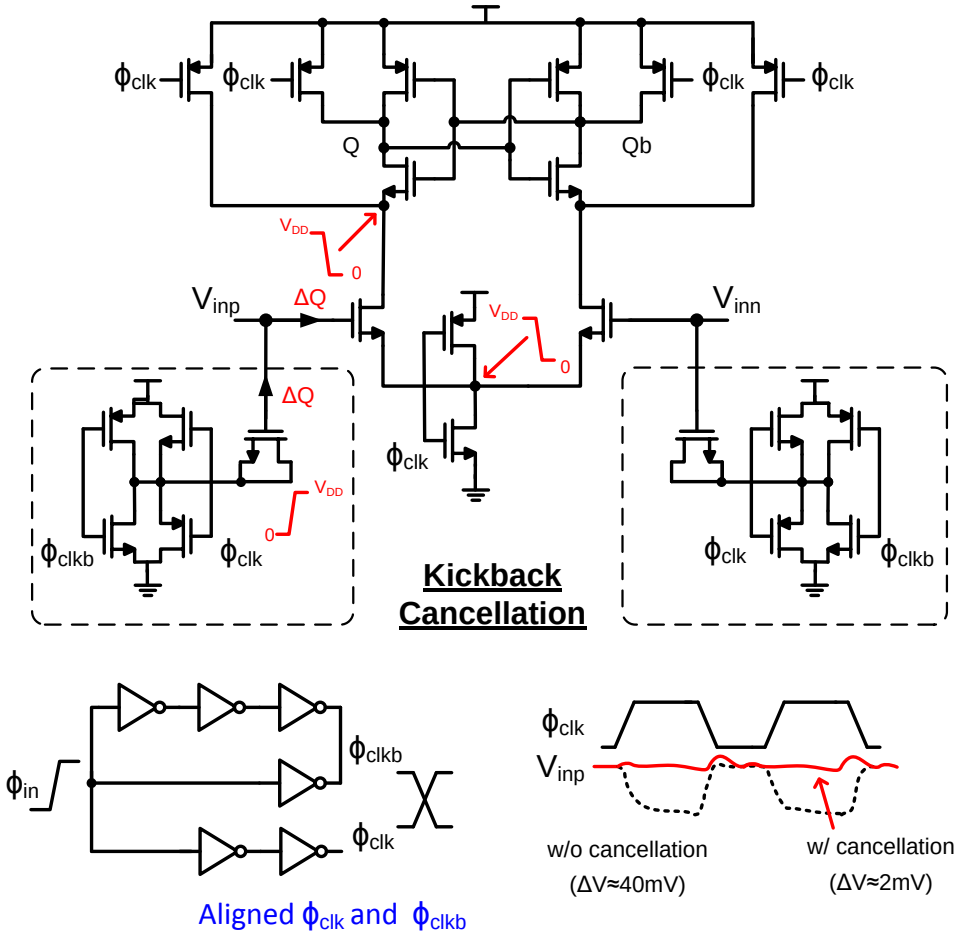



Figure 4.21. Circuit schematic of the dynamic comparator with kickback noise cancellation

## 4.4 MEASUREMENT RESULTS

Figure 4.22 demonstrates the die photo of the prototype ADC, which was fabricated in a 65 nm CMOS process and occupies an active area of 0.08 $mm^2$. Figure 4.23 shows the measured DNL and INL profiles. The maximum DNL and INL are both less than 1 LSB.

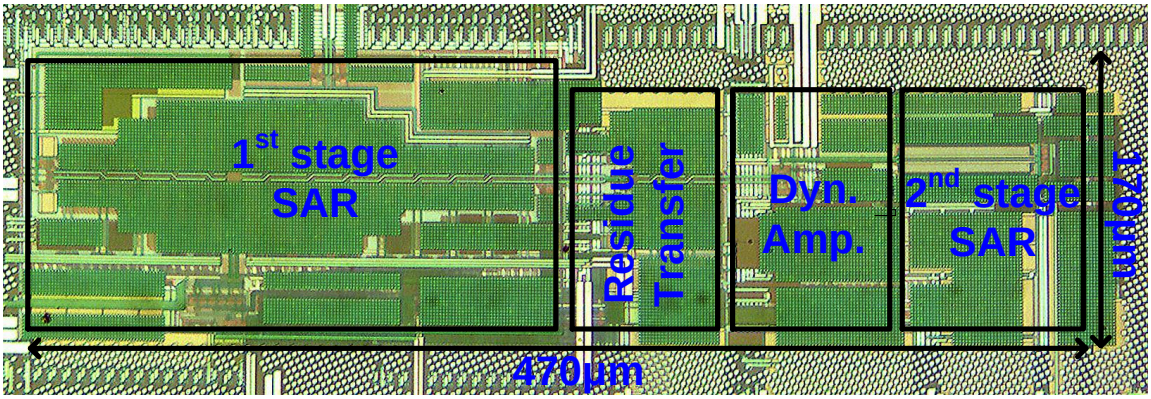



Figure 4.22. Die photo

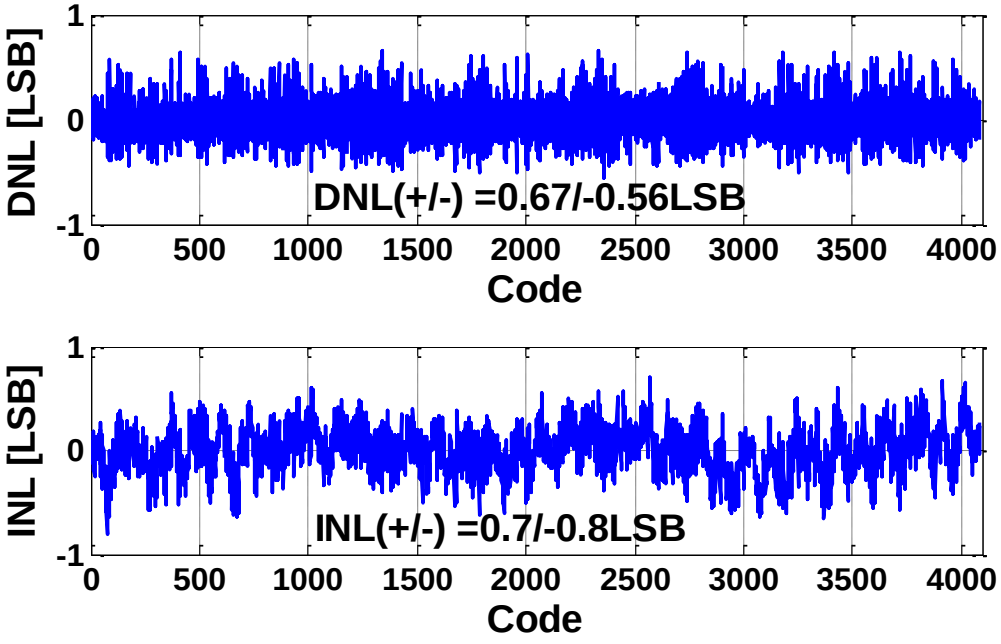
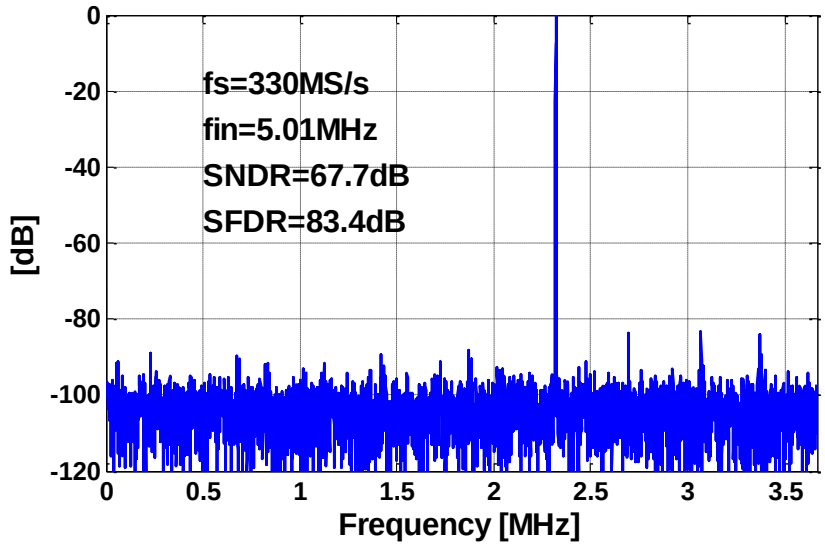
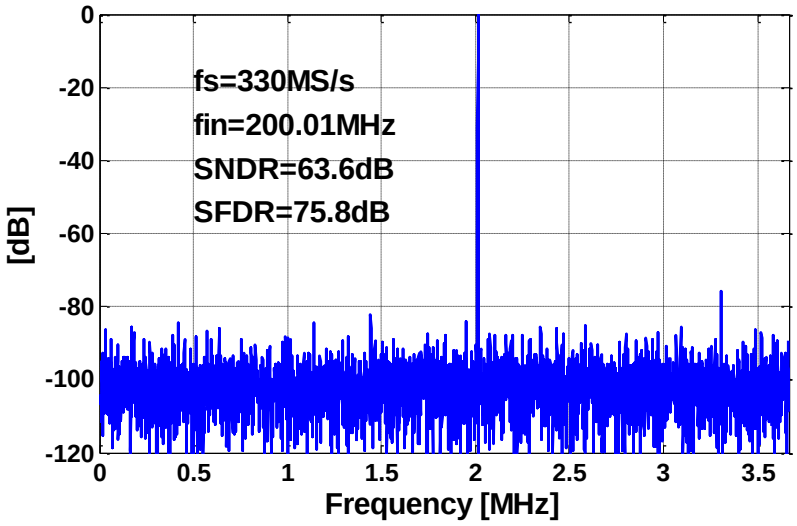



Figure 4.23. INL and DNL

The measured output spectrum of the ADC is shown in this. For a 5 MHz input, the achieved SNDR is 67.7 dB and the SFDR is 83.4 dB. For a 200 MHz input, the ADC measured an SNDR of 63.6 dB and an SFDR of 75.8 dB.




(a)




(b)

Figure 4.24. Measured ADC spectra at 330 MS/s with (a) a 5 MHz input and (b) a 200 MHz (both decimated by 45×)

Figure 4.25 summarizes the dynamic performance versus the input frequency. As can be seen, the SNDR remains above 60 dB even with a 500 MHz input. Figure 4.26 depicts the dynamic performance of prototype ADC versus sample rate.

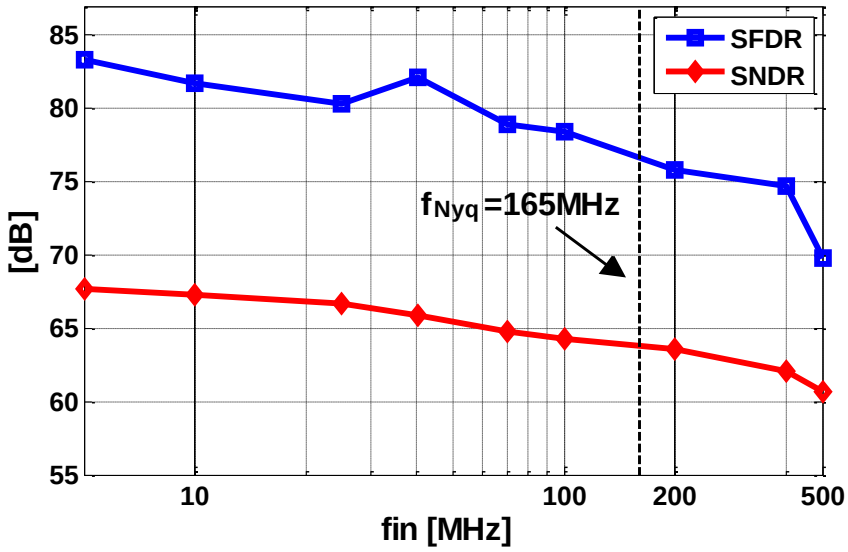



Figure 4.25. Measured SNDR and SFDR vs. input frequency

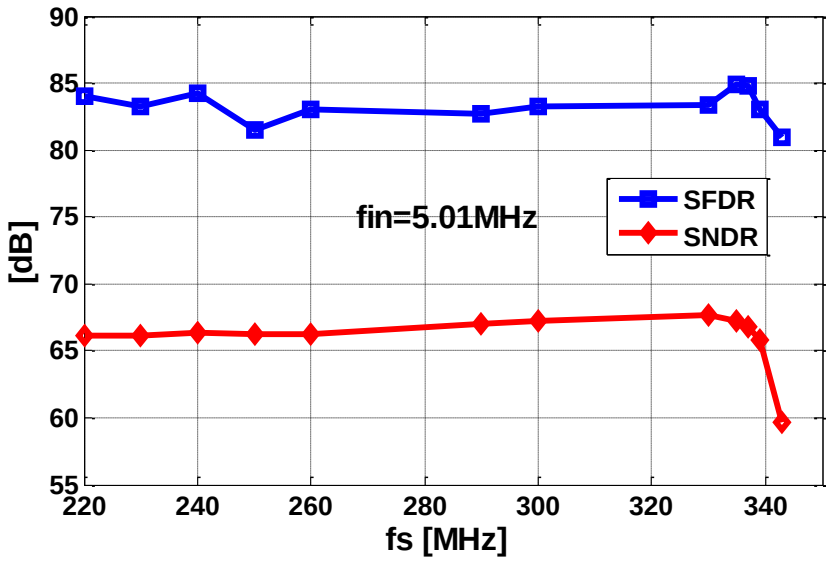



Figure 4.26. Measured SNDR and SFDR vs. sample rate.

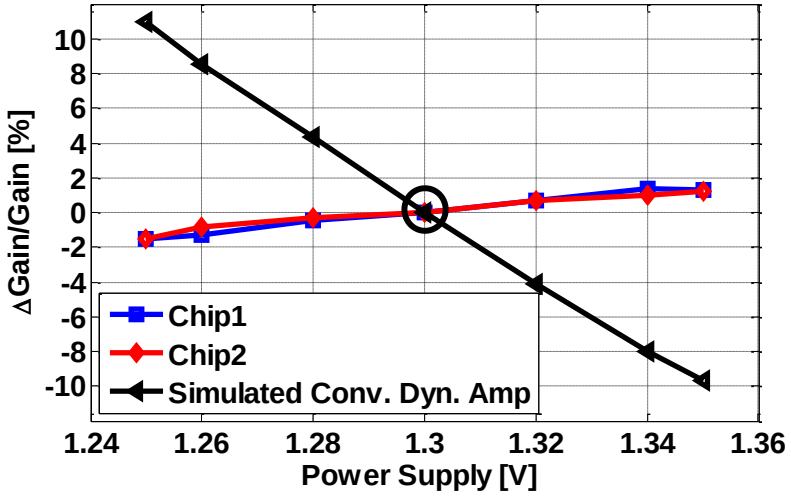



Figure 4.27. Measured residue gain versus the supply voltage

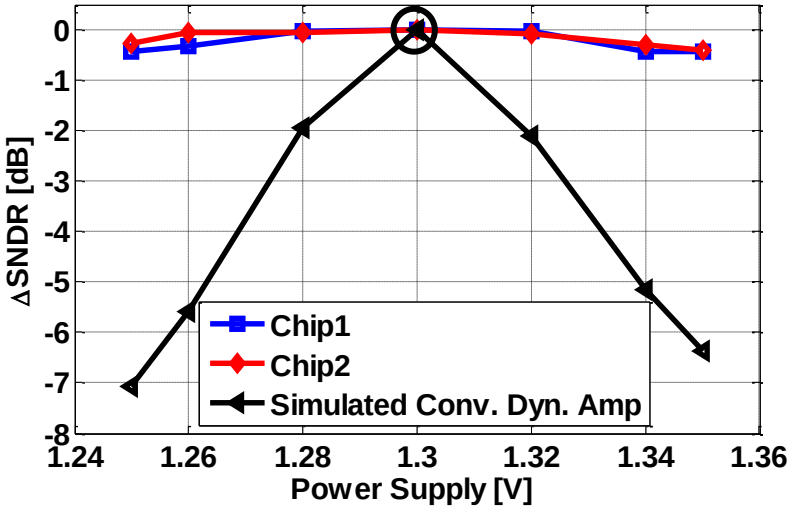



Figure 4.28. Measured SNDR versus the supply voltage

The plots in Figure 4.27 shows the measured residue gain versus the supply voltage. For comparison, the simulated gain of the conventional dynamic amplifier is also plotted. Over the supply voltage range from 1.25 V to 1.35 V, the maximum gain variation is reduced from 11% to 1.5%. With PVT stabilization, the maximum SNDR variation shown in Figure 4.28 is improved from 7 dB to 0.5 dB over the same supply voltage range. The measured residue gain versus the

temperature is demonstrated in Figure 4.29. Over the temperature range from −5 ℃ to 85 ℃, the maximum gain variation is reduced from 14% to 1.2%. Over the same temperature range, the maximum SNDR variation illustrated in Figure 4.30 is improved from 8.6 dB to 0.8 dB.

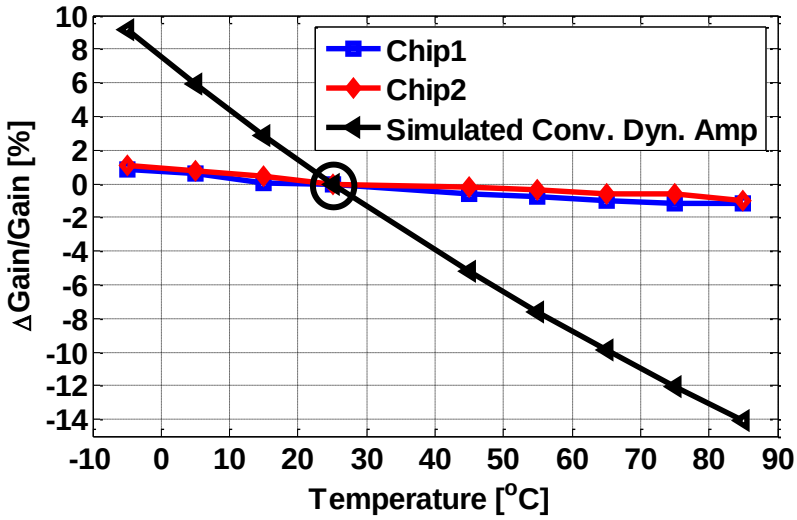



Figure 4.29. Measured residue gain versus temperature

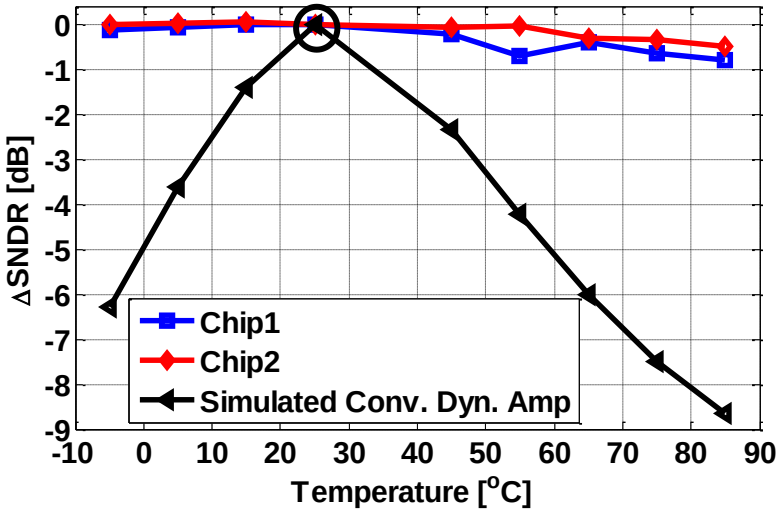



Figure 4.30. Measured SNDR versus temperature

The prototype ADC was fabricated through an multi-project wafer program, so only chips at typical corner were provided by the foundry and we couldn't measure the residue gain at different corners. As an alternative, the simulated gain of PVT-stabilized dynamic amplifier versus the process corners are supplied in Figure 4.31.

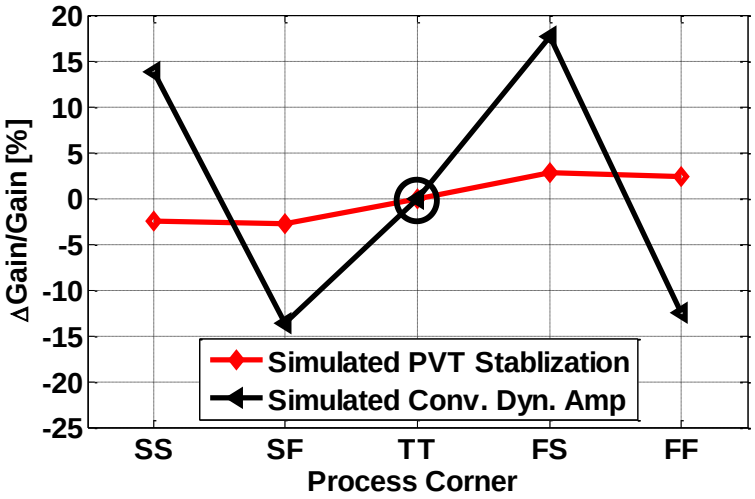



Figure 4.31. Simulated residue versus process corner

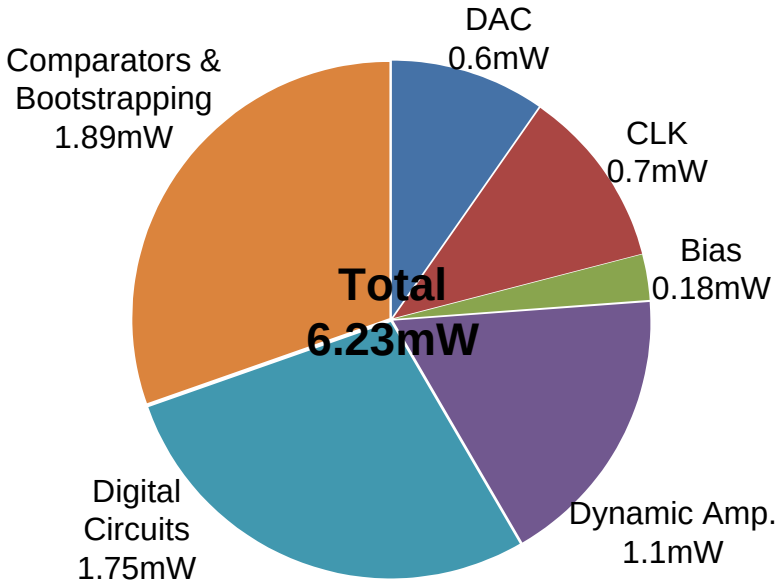



Figure 4.32. Power consumption breakdown of prototype ADC

The power consumption breakdown of this ADC is presented in Figure 4.32. Clocked at 330 MS/s, the ADC consumes a total power of 6.23 mW, leading to a figure of merit (FoM) of 167.7 dB. Figure 4.33 compares the prototype ADC to the state-of-the-art single-channel ADCs with an SNDR larger than 60 dB. It can be seen that, the figure of merit of this work is 6.2 dB larger than that of the previous design with a similar conversion speed. In terms of conversion speed, this prototype ADC is 65% faster than the previous SAR or Pipelined SAR ADCs.

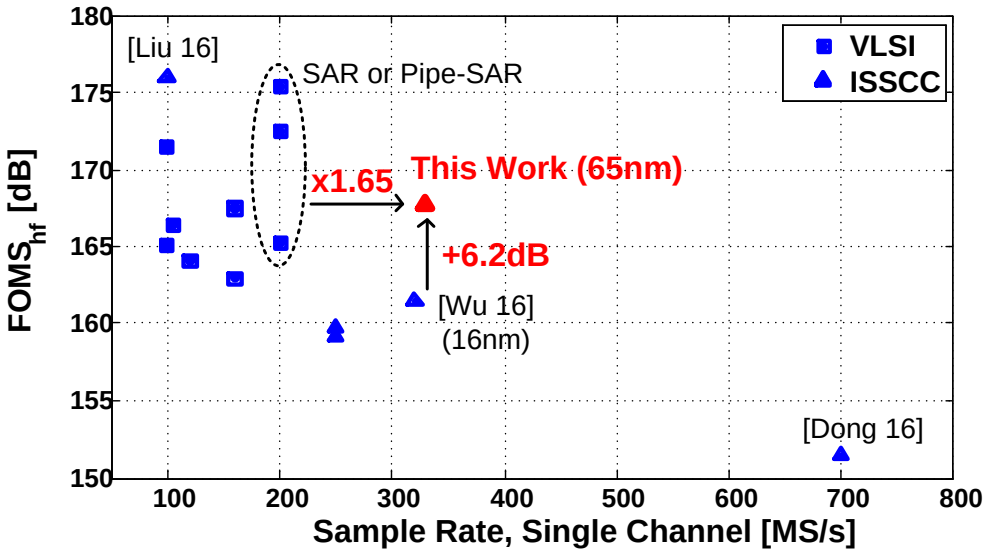



Figure 4.33. Performance comparison

## 4.5 SUMMARY

In this chapter, a PVT-stabilized dynamic amplifier is reported for high-speed pipelined SAR ADCs for the first time. Thanks to this technique, the prototype ADC measures less than 1dB SNDR fluctuations. With passive residue transfer, the prototype also achieves the highest sample rate among single-channel SAR ADCs with a competitive FoM.

# CHAPTER 5

# CONCLUSION

High speed ADCs with low power consumption are greatly demanded by a lot of applications such as high-speed links, wireless transceivers, radars and portable instruments. This dissertation presents the passive residue transfer technique and the PVT-stabilized dynamic amplifier to push the speed limit of pipelined SAR ADCs without sacrificing the power efficiency.

Owing to the passive residue transfer technique, the bandwidth-limiting residue amplifier in medium-resolution pipelined SAR ADC can be removed to effectively reduce the time consumed by the residue transfer, resulting in a significant speed improvement. A 8 bit prototype ADC with this technique was designed and fabricated in a 65 nm process, which measured a SNDR of 43.7 dB and a SFDR of 58.1 dB for a near-Nyquist input. Although with a old process, the prototype ADC still achieves a comparable speed to prior designs fabricated in a 32 nm process. Clocked at 1.2 GS/s, the ADC consumes a total power of 5 mW, yielding a Walden FoM of 35 fJ/conversion-step.

The second part of this dissertation focuses on boosting the conversion speed of high-resolution pipelined SAR ADC with residue amplifier. Dynamic amplifier is an emerging high-speed amplification technique but with the gain uncertainty over PVT variations. To mitigate the gain instability, a novel PVT stabilization technique with a single-pole amplifier used as the replica circuit is proposed. The small gain variations shown in the measurement and simulation results prove the effectiveness of the PVT stabilization technique. Thanks to this technique, the 12 bit prototype ADC measured less than 1 dB SNDR variation over supply voltage and ambient

temperature changes. Furthermore, assisted by the passive residue transfer, the ADC achieves a very competitive conversion speed, which is 65% faster than the previous SAR or pipelined SAR ADCs with a similar SNDR.

For the future works, the second ADC can be redesigned to a three-stage pipelined SAR ADC, which would relax the timing burden of each stages and provide some speed improvement. Since the input of the third stage is the amplified DC signal, the non-attenuated passive transfer technique in section 2.2 can be employed to replace the second residue amplifier without introducing the bandwidth mismatch issue. As mentioned earlier, the passive residue transfer removes the time for residue amplification and can bring about additional speed improvement. To further enhance the conversion speed, the time interleaved structure probably can be employed. However, some new problems such as the timing skew, gain and offset mismatch between sub ADCs are introduced, necessitating a complicated digital background calibration.

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## BIOGRAPHICAL SKETCH

Hai Huang received the B.S. degree and the M.Sc. degree in electrical engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2010 and 2013. He has been pursuing his Ph.D. degree at The University of Texas at Dallas, Richardson, TX, USA since 2013. From June 2015 to September 2015, he was an intern with Analog Devices, MA, USA, where he investigated ring amplifiers and dynamic amplifiers. His main research interests include data converters and emerging low power amplifiers.

Mr. Huang received the first prize of National Undergraduate Electronic Design Contest in Sichuan section in 2009. He also was a recipient of the Analog Devices Outstanding Student Designer Award in 2014.

# CURRICULUM VITAE

## Hai Huang

## Education

University of Texas at Dallas Aug. 2013–May 2017

Ph.D. in Electronic Engineering

University of Electronic science and Technology of China Sept. 2006–Jul. 2013

M.Sc. degree in Circuits and Systems

B.Sc. degree in Electronic Information Engineering

## Work Experience

Jun. 2015-Sept. 2015 Intern at Analog Devices (Wilmington, USA)

- Investigated ring amplifiers for ultra low power pipelined SAR ADC
- Developed compensation techniques to mitigate the gain variation of low power dynamic amplifier

Jul. 2010-Sept. 2010 Intern at Fujitsu (Chengdu, China)

- Based on C language, three motion-sensing games running on ARM11 processor were developed for Digital Television

## Research Projects

Sept. 2015-Oct. 2016 Design of 12bit 330MS/s Pipelined SAR ADC

May 2016-Aug. 2016 A Single Op-amp Fourth-Order ΣΔ ADC

Feb. 2014-Jul. 2015 Design of 8bit 1.2GS/s Pipelined SAR ADC

Sept. 2013-Feb. 2014 Estimation of Timing Skew in Time-Interleaved ADC

Apr. 2012-Jul. 2013 Design of 0.5V 11b Self-calibrated ADC

Mar. 2011-Feb. 2012 A 0.5V 6-to-10b Resolution Scalable ADC

Apr. 2009-Jul. 2009 DC to AC Power Converter

## Publications

- H. Huang et al., "A 12b 330MS/s Pipelined SAR ADC with PVT-Stabilized Dynamic Amplifier Achieving <1dB SNDR Variations", Accepted by International Solid-State Circuits Conference 2017
- H. Huang, D. Ling, and Y. Chiu, "A 1.2 GS/s 8 bit Two-Step SAR ADC in 65 nm CMOS with Passive Residue Transfer", Accepted by IEEE Journal of Solid-State Circuits.
- H. Huang, D. Ling, and Y. Chiu, "A 1.2GS/S 8bit Two-Step SAR ADC in 65nm CMOS with Passive Residue Transfer", The IEEE Asian Solid-State Circuits Conference 2015.
- X. Y. Wang, H. Huang, and Q. Li, "Design Considerations of Ultra-Low Voltage Self-Calibrated SAR ADC", IEEE Transactions on Circuits and Systems-II 2014.
- H. Huang, X. Y. Wang, and Q. Li, "Design considerations of Ultra-Low-Voltage Self-calibrated SAR ADC", the 10th International Conference on Sampling Theory and Applications 2013.
- H. Huang, K. Ao, and Q. Li, "A 0.5V Rate-Resolution Scalable SAR ADC with 63.7dB SFDR", International Symposium on Circuits and Systems 2013.

## Awards

1. Analog Device Inc Outstanding Student Designer Award at Feb. 2014
2. 1st Prize in the Sichuan Division of National Undergraduate Electronic Design Contest at Dec. 2009
3. 1st Prize in the Electronic Design Competition of Sichuan province in Jan. 2009
4. 1st Prize in the Electronic Design Competition of Texas Instrument at Nov. 2009

## Skills

1. Data Converter, Power Converter and other Mixed-signal circuit design
2. Circuit board design for measurements
3. Electronic test tools
4. System design with MATLAB and C